DATABOOK

1992 DEVICES

Systems Logic

Imaging

Storage

WESTERN DIGITAL

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Data Sheet and Device Status Definitions

Status in Data Sheet Footer	Device Status	Definition
ADVANCED INFORMATION AND DATE	Initial Production	This data sheet contains information prior to device characterization. Western Digital Corporation reserves the right to change specifications at any time without notice in order to improve overall design and operation.
DATE	Full Production	This data sheet contains final specifications. The information has been updated and published as of the date indicated. Western Digital Corporation reserves the right to change specifications at any time without notice in order to improve overall design and operation.

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From its manufacturing, assembly and test facilities throughout the world, Western Digital is committed to producing the highest quality semiconductor, board-level and intelligent disk drive products available.

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Western Digital recognizes the importance of power conservation in todays new battery operated computers. Our laptop core logic chip sets offer extensive power management features. In addition, Western Digital offers devices that require only 3.3 volts for operation rather than the typical 5.0 volts. LVCMOS offers a greater operating range than the current 5V logic, thereby reducing power consumption and extending battery life.

The wide operating range will make it possible to eliminate the power regulator and directly connect a notebook system to a battery, thus increasing power efficiency and reducing component requirements. The combination of power management, lower operating voltage, and the elimination of the power supply regulator can mean a 35 to 40 percent savings in system power.

Interarchitecture Solutions For Desktop Systems

WD7600A System Chip Set for 80286 or 80386SX desktop systems
WD7700 System Chip Set for 80386SX desktop systems
WD7900 System Chip Set for 80386SX desktop systems

Components:

WD76C10A single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- system speed up to 25 MHz
- .9 micron CMOS design
- 80C286 or 80386SX interface

OR:

WD7710 single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- system speed up to 25 MHz
- .9 micron CMOS design
- integrated 8K cache data and TAG RAM
- 80386SX interface

OR:

WD7910 single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- system speed up to 25 MHz
- .9 micron CMOS design
- integrated 8K cache data and TAG RAM
- 80386SX interface
- VLBI support

WD76C20 single-chip storage

- floppy control, IDE control, real-time clock, CMOS RAM, chip select decodes
- 1.25 micron CMOS design
- data transfer in DMA or non-DMA modes
- chip select logic generation

WD76C30 single-chip data communications

- serial/parallel I/O control, programmable coprocessor clock, floppy frequency generator, keyboard clock, baud rate generator, AT-bus clock, interrupt multiplexor
- 1.25 micron CMOS design
- FIFO port operation

WD90C30 single chip video

- fully integrated VGA video control
- optional video RAMDAC and video clock
- .9 micron CMOS design

ICS90C61A -- video graphics array clock

Western Digital Interachitecture Intelligent Drives

Caviar™ Drives:

- one-inch, 42, 62, 85, and 125 Mbyte formatted capacities, sub-17 milliseconds
- CacheFlow™, adaptive segmented cache
- Automatic head parking, advanced defect management and embedded sector servo control

Piranha™ Drives:

- 3.5-inch, 106- and 212-Mbyte formatted capacities, sub-15 milliseconds
- CacheFlow, adaptive segmented cache
- Automatic head parking, advanced defect management and embedded sector servo control

Interarchitecture Solutions For Portable Systems

WD7600ALP System Chip Set for 80286 or 80386SX portable systems
WD7700LP System Chip Set for 80386SX portable systems
WD7900LP System Chip Set for 80386SX portable systems

Components:

WD76C10ALP single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- extensive set of power management features, CPU sleep and auto speed switch modes
- system speed up to 25 MHz
- 80C286 or 80386SX interface
- .9 micron CMOS design

OR:

WD7710LP single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- extensive set of power management features, CPU sleep and auto speed switch modes
- system speed up to 25 MHz
- 80386SX interface
- .9 micron CMOS design
- integrated 8K data cache

OR:

WD7910LP single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- extensive set of power management features, CPU sleep and auto speed switch modes
- system speed up to 25 MHz
- 80386SX interface
- SMI and VLBI support
- .9 micron CMOS design
- integrated 8K data cache

WD76C20 single-chip storage

- floppy control, IDE control, real-time clock, CMOS RAM, chip select decodes
- 1.25 micron CMOS design
- data transfer in DMA or non-DMA
- chip select logic generation

WD76C30 single-chip data communications

- serial/parallel I/O control, programmable coprocessor clock, floppy frequency generator, keyboard clock, baud rate generator, AT-bus clock, interrupt multiplexor
- 1.25 micron CMOS design
- FIFO port operation

WD90C20A/WD90C22 single-chip video

- full VGA video support with laptop RAMDAC
- optional video clock
- supports 32-color, gray-scale palette (64-color grey-scale with WD90C22)
- .9 micron CMOS design

ICS90C64 -- video graphics array clock

Western Digital Interarchitecture Intelligent Drives*

AH260 Tidbit™ Drive:

- 2.5-inch, 0.75 inches high
- 63.2 Mbyte formatted capacity
- Sub-16 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

AH280 Tidbit™ Drive:

- 2.5-inch, 0.75 inches high
- 85.5 Mbyte formatted capacity
- Sub-16 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

Low Voltage (3.3 Volt) Interarchitecture Solutions

WD7600ALV System Chip Set for 80286 or 80386SX portable systems
WD7900LV System Chip Set for 80386SX portable systems

Components:

WD76C10ALV single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- extensive set of power management features, CPU sleep and auto speed switch modes
- 3.3 volt operation
- 80C286 or 80386SX interface
- .9 micron CMOS design

OR:

WD7910LV single-chip core logic

- memory control, CPU control, DMA interrupts, buffers, AT-bus control
- extensive set of power management features, CPU sleep and auto speed switch modes
- 3.3 volt operation
- 80386SX interface
- VLBI support
- .9 micron CMOS design
- integrated 8K data cache

WD76C20LV single-chip storage

- floppy control, IDE control, real-time clock, CMOS RAM, chip select decodes
- 3.3 volt operation
- 1.25 micron CMOS design
- data transfer in DMA or non-DMA
- chip select logic generation

WD76C30DLV single-chip data communications

- serial/parallel I/O control, programmable coprocessor clock, floppy frequency generator, keyboard clock, baud rate generator, AT-bus clock, interrupt multiplexor
- 3.3 volt operation
- 1.25 micron CMOS design
- FIFO port operation

WD90C26 single-chip LCD video

- full VGA video support with laptop RAMDAC
- 3.3 volt operation
- optional video clock
- supports 64 TrueShade™, gray shades
- .9 micron CMOS design

ICS90C64 -- video graphics array clock

Western Digital Interarchitecture Intelligent Drives*

AH260 Tidbit™ Drive:

- 2.5-inch, 0.75 inches high
- 63.2 Mbyte formatted capacity
- Sub-16 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

AH280 Tidbit™ Drive:

- 2.5-inch, 0.75 inches high
- 85.5 Mbyte formatted capacity
- Sub-16 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

* For more information on Western Digital's intelligent drives, call 1.714.932.4900.

WD16C451, WD16C551

Enhanced Asynchronous Communications Element (ACE) with Parallel Port

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DESCRIPTION

The low-power CMOS WD16C451/WD16C551 is a single-device solution for serving one serial I/O port and one bidirectional parallel port on the IBM PC, PC XT, PC AT, PS/2, and compatible systems. The WD16C451/WD16C551 is an enhanced ACE with a bidirectional parallel port. The ACE performs parallel-to-serial conversion on output and serial-to-parallel conversion on input. It is programmable, independent, and has a maximum recommended data rate of 512K baud.

The WD16C451 family (WD16C451, WD16C451A, WD16C451B) is a WD16C450 ACE plus a bidirectional parallel data port.

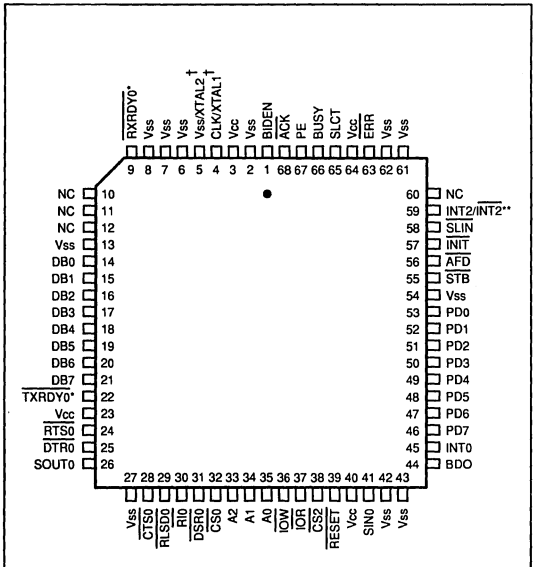
The WD16C451 and WD16C451A parallel port supports a Centronics-compatible printer interface. The parallel port, together with the serial port, provides IBM PC XT, PC AT and compatibles with a single-device solution for serving both ports. The WD16C451A is further enhanced by its crystal input capability.

The WD16C451B, also enhanced by its crystal input capability, supports a PS/2-compatible printer port interface. The parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for serving both ports.

The WD16C551 is a WD16C550 Enhanced ACE plus a compatible PS/2 bidirectional parallel port. After power-up and hardware reset, the ACE is functionally compatible with WD16C450 (Character Mode). The ACE in the WD16C551 has been enhanced with 16-byte FIFO buffers on both the receive and transmit lines, allowing an additional mode of operation called FIFO Mode. The FIFO Mode, only available in WD16C551, can be activated through software, relieving CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in multitasking environments. The WD16C551 also has DMA signaling between the FIFO buffers and host CPU allowing single-character or multicharacter transfers. The recommended maximum data rate is 512 Kbaud with an 8.0 MHz clock rate. The PS/2 parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for servicing both ports.

1.2 FEATURES

- Fully programmable serial interface characteristics including:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no parity bit generation/detection
  - 1, 1-1/2, or 2 stop-bit generation
  - DC to 512 Kbaud rate generation
- Tri-state TTL drive capabilities for bidirectional data bus and control bus
- Loopback controls for communications link fault isolation
- Line break generation and detection
- False start-bit detection



* INTERNAL NO CONNECTS FOR WD16C451/16C451A/16C451B, RXRDY0 (PIN 9) AND TXRDY0 (PIN 22) FOR WD16C551.
** INT2 FOR WD16C451/16C451A AND INT2 FOR WD16C551/16C451B.

FIGURE 1-1. 68-PIN QUAD

- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals
- Fully prioritized independent interrupt system controls
- CMOS implementation for high-speed, low-power requirements
- 68-pin QUAD package

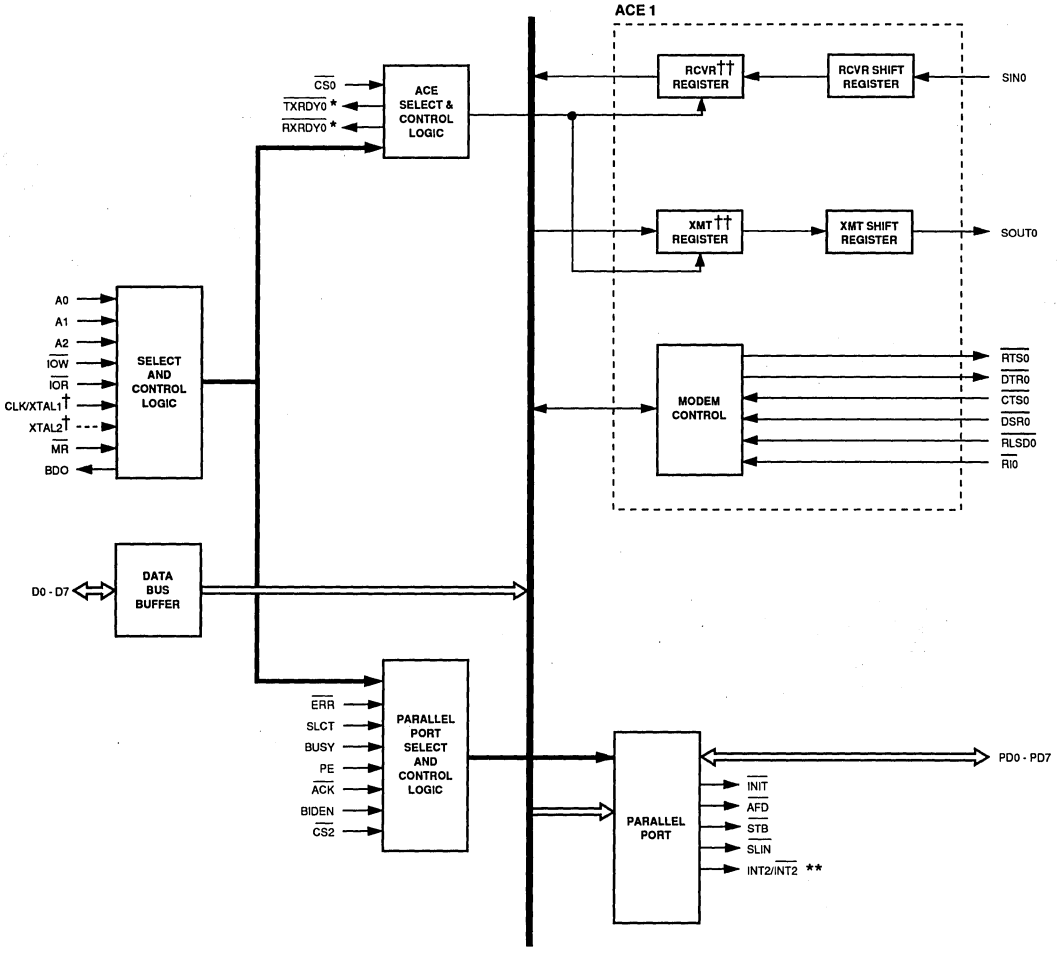
AVAILABLE VERSIONS

WD16C451 with:
- Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface

WD16C451A with:
- Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface
- Crystal-controlled external clock input

WD16C451B with:
- PS/2-compatible bidirectional parallel port
- Crystal-controlled external clock input

WD16C551 with:
- PS/2-compatible bidirectional parallel port
- 16-byte transmit and receive FIFO buffers for CPU relief during high-speed data transfer
- Programmable 1-, 4-, 8-, or 14-byte FIFO threshold levels on each receive channel
- Two modes of DMA signaling for transfer of data characters to and from FIFO buffers

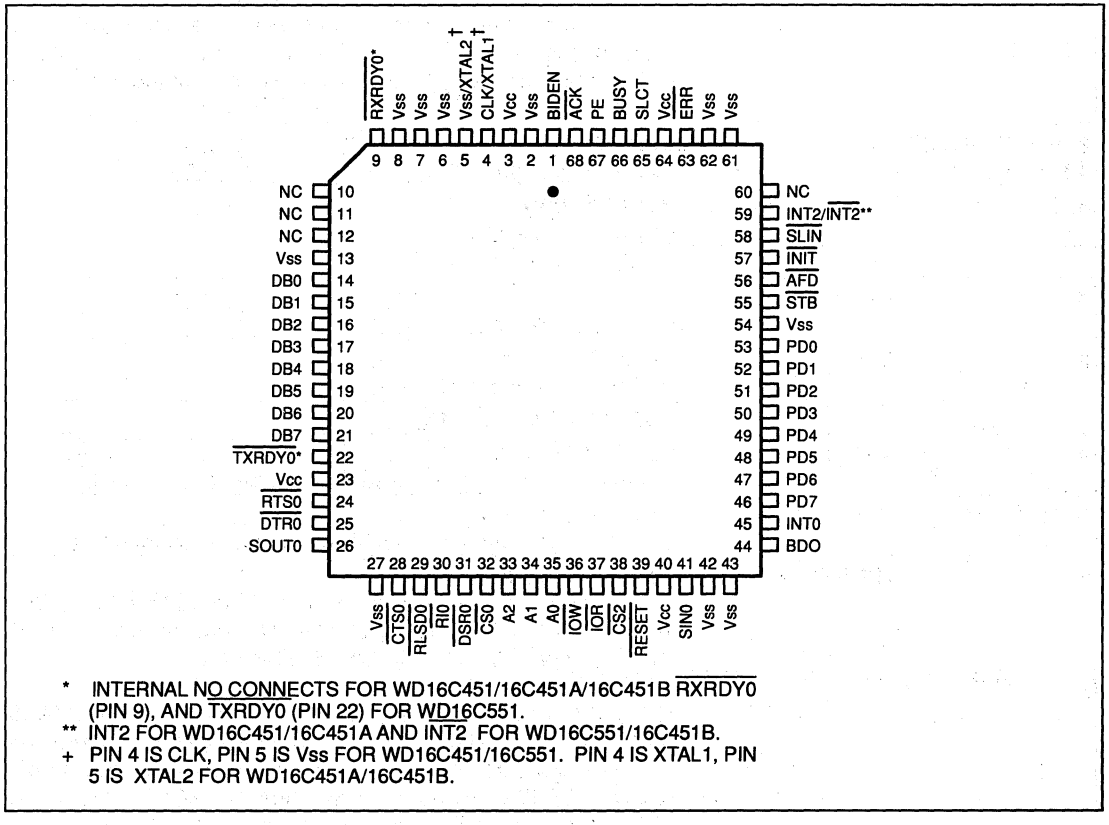


(*) TXRDY0 and RXRDY0 for WD16C551 only.
(**) INT2 for WD16C451/16C451A, INT2 for WD16C551/16C451B.
(†) CLK for WD16C451/16C551, XTAL1 and XTAL2 for WD16C451A/16C451B.
(††) 16-byte FIFO buffers for WD16C551.

FIGURE 1-2. WD16C451/WD16C55A BLOCK DIAGRAM

2.0 SIGNAL DESCRIPTIONS

Figure 2-1 illustrates the 68-Pin QUAD assembly. Table 2-1 lists all signal descriptions.



* INTERNAL NO CONNECTS FOR WD16C451/16C451A/16C451B RXRDY0 (PIN 9), AND TXRDY0 (PIN 22) FOR WD16C551.
** INT2 FOR WD16C451/16C451A AND INT2 FOR WD16C551/16C451B.
\+ PIN 4 IS CLK, PIN 5 IS Vss FOR WD16C451/16C551. PIN 4 IS XTAL1, PIN 5 IS XTAL2 FOR WD16C451A/16C451B.

FIGURE 2-1. WD16C451/WD16C551 68-PIN QUAD ASSEMBLY PIN DESIGNATIONS

PIN	MNEMONIC	DESCRIPTIONS
1	BIDEN	**Bidirectional Enable** Input signal in WD16C451/16C451A when low enables the parallel port data lines as outputs. When high, the WD16C451/16C451A will hold the parallel port data pins in a high-impedance state, allowing these pins to be driven with data. The BIDEN input signal on the WD16C551/16C451B works in conjunction with the DIR bit (see Table 6-3) to control the direction of the parallel port data bit.
2, 6-8, 13, 42, 27, 43, 54, 61, 62	Vss	**Ground** System signal ground.
3, 23, 40, 64	Vcc	**Power Supply** +5V power supply.
		WD16C451/16C551
4	CLK (Times 1)	**Clock Input** External clock input.
5	Vss	**Ground** System signal ground.
		WD16C451A/16C551B
4	XTAL1	**External Clock In** Connects the crystal to the ACE baud rate divisor circuit.
5	XTAL2	**External Clock Out** Connects the crystal to the ACE baud rate divisor circuit.
9	$\overline{\text{RXRDY0}}$ ♦	**$\overline{\text{Receiver Ready}}$** Receiver ready output is used to signal DMA transfer to the CPU from the ACE. Two modes of operation are available in FIFO Mode, and one (Mode 0) in Chararacter Mode. Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, RXRDY will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. RXRDY will go inactive when the RCVR FIFO buffer (FIFO Mode), or holding register (Character Mode) is empty. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, $\overline{\text{RXRDY}}$ will go active (low) when the trigger level or time out has been reached. $\overline{\text{RXRDY}}$ goes inactive (high) when the FIFO buffer is empty.
(♦) These pins are internal no-connects on the WD16C451.		

TABLE 2-1. SIGNAL DESCRIPTIONS

PIN	MNEMONIC	DESCRIPTION
10-12	NC	**No connection** Internally not connected.
14-21	DB0-DB7	**Data Bits** Tri-state, bidirectional communication lines between the internal registers and Data Bus. D0 is the LSB and the first serial transmitted or received bit.
22	$\overline{\text{TXRDY0}}$♦	**$\overline{\text{Transmitter Ready FIFO Control}}$** Transmit ready output is used to signal. DMA transfer to the CPU from the ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode. Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, TXRDY will be active (low) if there are no characters in the Xmit FIFO buffer (FIFO Mode) or Xmit holding register (Character Mode). TXRDY will go inactive after the first character is loaded. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one or more unfilled position in the Xmit FIFO TXRDY0 will be active (low). TXRDY0 goes inactive when the FIFO buffer is completely full.
24	RTS0	**$\overline{\text{Request to Send}}$** Output when low informs the MODEM or data set that the ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
25	$\overline{\text{DTR0}}$	**$\overline{\text{Data Terminal Ready}}$** Output when low informs the MODEM or data set that the ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
26	SOUT0	**Serial Data Output** Transmitted Serial Data Out to the communication link from the ACE.SOUT is set to a marking condition (logical 1) on a Master Reset.
28	$\overline{\text{CTS0}}$	**$\overline{\text{Clear to Send}}$** Input from DCE to the ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
(♦) These pins are internal no-connects on the WD16C451.		

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	DESCRIPTION
29	RLSD0	**Received Line Signal Detect** IInput from the DCE indicating that the ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the MODEM Status Register reflects this value.
30	$\overline{RI0}$	**Ring Indicator** Input when low indicates a ringing signal being received by the MODEM or data set. This logical value is reflected in bit 6 of the MODEM status Register.
31	$\overline{DSR0}$	**Data Set Ready** When low, this input signal from the communication link indicates that it is ready to exchange data with the ACE. Bit 5 of the associated MODEM Status Register reflects the DSR logical state.
32	$\overline{CS0}$	**Chip Select 0** Chip Select input when active (low) selects serial channel 0.
33 thru 35	A2, A1, A0	**Address lines A2-A0** These three inputs are used to select an internal register of the ACE, or parallel port.
36	$\overline{IOW}$	**Input/Output Write Strobe** Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0 or CS2 to be ACE parallel port, respectively.
37	$\overline{IOR}$	**Input/Output Read Strobe** Input active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
$\overline{38}$	CS2	**Chip Select 2** Chip Select input when active (low), enables the line printer port.
39	$\overline{Reset}$	Reset Input when active (low), will force the device into an idle mode where all serial data activity is suspended. The device will remain in an idle state until programmed to begin data activities.
41	SIN0	**Serial Data Inputs** Received Serial Data Input from the communication link to the ACE. Data on the serial data inputs are disabled when exercising loopback mode, and internally connected to their respective SIN lines.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	DESCRIPTION
44	BDO	**Bus Buffer Output** Output goes active when either the serial channel or the parallel port is serial channel or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).
45	INT0	**Serial Channel Interrupt** Tri-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46-53	PD7-PD0	**Parallel Data Bits** Bidirectional data port which provides parallel input and output to the system. The 8 lines are held in a high impedance state when BIDEN is high.
55	$\overline{STB}$†	Line Printer Strobe Output line, when active, provides the line printer with a signal to latch the data currently on the parallel port.
56	$\overline{AFD}$†	**Line Printer Autofeed** Output line, when active, provides a signal for the line printer to autofeed continuous form paper.
57	INIT†	**Line Printer Initialize** Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	$\overline{SLIN}$†	**Line Printer Select** Output line, when active (low), selects the printer.
59	INT2/$\overline{INT2}$††	**Interrupt Printer Port** Tri-state output enabled by bit 4 of WCR. For the WD16C451/16C451A, INT2 goes active high on the rising transition of $\overline{ACK}$ and reset (low) on the falling transition of $\overline{ACK}$. For the WD16C551/16C451B, INT2 goes active low on the rising edge of $\overline{ACK}$. INT 2 is reset (high) on the rising edge of $\overline{IOR}$, when reading the parallel port status register.
60	NC	**No connection** Internally not connected.
63	$\overline{ERR}$	**Line Printer Error** Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.
(†) These outputs are open drain with internal pull-ups. (††) This pin is INT2 fro WD16C451/16C451A and $\overline{INT2}$ for WD16C551/16C451B.		

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	DESCRIPTION
65	SLCT	**Line Printer Select** Input from the line printer that goes high when the line printer has been selected.
66	BUSY	**Line Printer Busy** Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	**Line Printer Paper Empty** Input from the line printer goes high when the printer is out of paper.
68	$\overline{\text{ACK}}$	**Line Printer Acknowledge** Input from the line printer that goes low to confirm the data transfer from the WD16C451/16C551 to the printer was successful.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

3.0 SERIAL CHANNEL REGISTERS

3.1 SERIAL PORT REGISTER ADDRESSING

Chip Select ($\overline{CSO}$): When $\overline{CSO}$ is low, registers for the serial channel can be accessed.

Master Reset:
A low level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an Idle Mode. (Registers are not reset by this operation.) Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to return to a known state without resetting the system.

Chip Select ($\overline{CSO}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.
Register Select (A0, A1, A2): To select a register for read or write operation, see table 2-1

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING

1

4.0 ACE OPERATIONAL DESCRIPTION

4.1 MASTER RESET

A low-level input on this pin causes the ACE to reset to the condition listed in Table 4-1.

4.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in Table 4-2. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	BDO = $\overline{RCLK}$ • IOR (At Master Reset, the CPU sets RCLK and $\overline{IOR}$ = Low when device is selected.)	High
INT0 (RCVR ERRS)	Master Reset/Read LSR	Low
INT0 (RCVR DATA READY)	Master Reset/Read RBR	Low
INT2 (WD16C451/WD16C451A)	Master Reset/$\overline{ACK}$ (High)	Low
$\overline{INT2}$ (WD16C551/WD16C451B)	Master Reset/Read PPSR	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO Counter (WD16C551 Only)	MR or FCR1 • FCR0 or ΔFCR0	All Bits Low
XMIT FIFO Counter (WD16C551 only)	MR or FCR1 • FCR0 or $\overline{\Delta FCR0}$	All Bits Low
FIFO CONTROL (WD16C551 only)	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	In Tri-state Mode, Unless $\overline{IOR}$ = Low or $\overline{IOW}$ = Low when Device is Selected	Tri-state Data (ACE to CPU) Data (CPU to ACE)

TABLE 4-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

	REGISTER ADDRESS					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3) ♦	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled ♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)
(♦) These bits are 0 in Character Mode.						

TABLE 4-2. ACCESSIBLE WD16C451/WD16C551 REGISTERS

REGISTER ADDRESS						
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15
(♦) These bits are 0 in Character Mode.						

TABLE 4-2. ACCESSIBLE WD16C451/WD16C551 REGISTERS (Contd)

4.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

4.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4-3, 4-4, and 4-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2	2.860

TABLE 4-3. BAUD RATES USING 1.8432 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3	14.285

TABLE 4-4. BAUD RATES USING 3.072 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 4-5. BAUD RATES USING 80.0 MHz CLOCK

4.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 4-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level). When in FIFO Mode, an FE is associated with a particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits). Bit 4 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received requires the SIN pin be high for at lease one-half bit time.

When in FIFO Mode BI is associated to the particular character in the FIFO buffer, and this bit is set when the associated character is in the top of the FIFO buffer.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits except bit 7 of the Status Register can be set or reset by writing to the register.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. This bit also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO buffer. The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs: the Transmitter FIFO buffer is empty and there have not been at least two chaacters in the Transmitter FIFO buffer at the same time since the last time that Transmitter FIFO buffer was empty. The first transmitter interrupt after changing the first bit of the FIFO Control Register will be immediate if it is enabled.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and

Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO buffer and SMIT Shift Register are both empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO buffer. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO buffer.

4.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 3-2)

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see Table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO buffer during the last four character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 4-6. INTERRUPT CONTROL FUNCTIONS

4.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in Table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

4.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer to as a general purpose register.

4.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFO buffers, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFO buffers. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFO buffers does not automatically clear. Resetting FCR0 will clear all characters from RCVR Error FIFO. The FIFOs should be cleared immediately after changing to FIFO mode. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR Error FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (See pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

5.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 4.2

Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

NOTE:
The DTR output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

Bit 3: This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control outputs (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. The resetting of these interrupts is the same as in normal ACE operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0

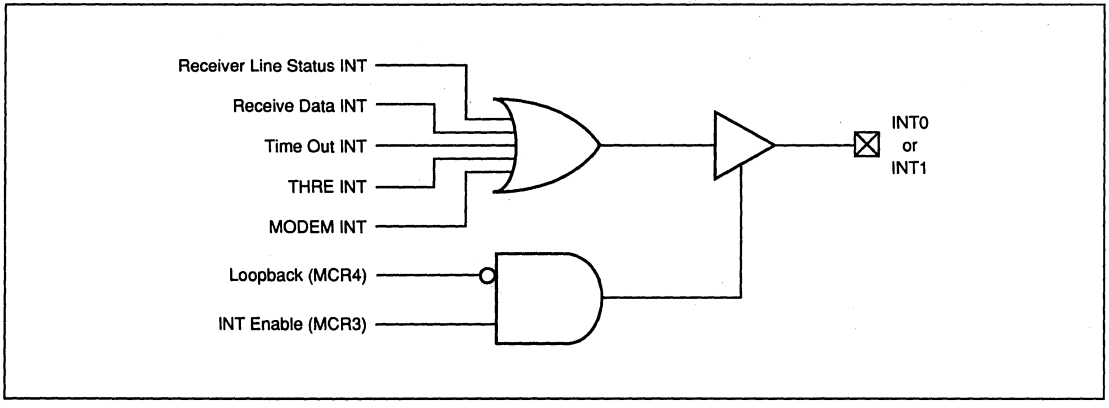


FIGURE 5-1. INTERRUPT SIGNAL LOGIC

6.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. Besides this information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3.2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

6.1 FIFO INTERRUPT MODE OPERATION NOTES

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt occurs when:
   a. There is at least one byte in the RCVR FIFO buffer
   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
   c. The most recent CPU read from the FIFO buffer has exceeded 4 continuous character times.

   The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.
2. When the RCVR FIFO buffer reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO buffer level falls below the trigger level.

6.2 FIFO POINTER NOTES

The RCVR FIFO has an internal pointer that automataically points to the RCVR Data byte to be read and the associated Status byte. Reading the RCVR Data byte will increment the internal counter, whereas reading the Status byte will not. The Status byte should always be read prior to the Data byte associated with it.

6.3 FIFO POLLING MODE OPERATION NOTES

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

7.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics-type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to Tables 7-1 and 7-2.)

Register Descriptons:

Read Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

Read Status Register

Bits 0 through 1: These bits are set to a logic one.

Bits 2: This bit represents the status of the $\overline{INT}$ pin. This bit is only available in the WD16C551/ WD16C451B.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to Table 7-2.

Read Control Register

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to Table 7-2.

Note: These values reflect the signal on the open drain outputs, not necessarily the value in the write control register.

A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Data
1	1	1	0	Invalid

TABLE 7-1. PARALLEL PORT (CS2=0) REGISTER ADDRESSES

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	$\overline{INT}$ ♦	Init	Init	Data Bit 2
3	Data Bit 3	Error	Slin	Slin	Data Bit 3
4	Data Bit 4	Slct	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	DIR ♦	Data Bit 5
6	Data Bit 6	Ack	1	1	Data Bit 6
7	Data Bit 7	Busy	1	1	Data Bit 7

(♦) These bits are 0 in Character Mode.

TABLE 7-2. ACCESSIBLE PARALLEL PORT REGISTERS

Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

Bits 5 through 7: These bits always return to a logic one.

Write Port Register

Bits 0 through 7: These bits correspond to the data to be placed on the parallel bus. This register is used to write data to the parallel bus based on Table 7-3.

Write Control Register

Bits 0 through 4: Writing to these bits will set the output of the corresponding pins.

Bit 5: The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus in extended mode, as described in the table below. This bit is only availabe in the WD16C551/WD16C451B, and is a write-only bit.

PORT MODE	PORT DIRECTION	PIN 1 BIDEN	DIRECTION BIT
Extended	Write	1	O
Extended	Write	0	X
Extended	Read	1	1
Compatible	Write	0	N/A
Compatible	Read	1	N/A

TABLE 7-3. PARALLEL PORT OPERATION MODES

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Control	Master Reset	All bits low.
Data (Write)	Master Reset	All bits low.
Data (Read)	Master Reset	Data
Status	Master Reset	Bits 0-2 are high, Bits 3-7 are ERR, SLCT, PE, ACK and Busy inputs.
INT2	Master Reset	High Impedance
$\overline{\text{SLIN}}$	Master Reset	High
$\overline{\text{INIT}}$	Master Reset	Low
$\overline{\text{AFD}}$	Master Reset	High
$\overline{\text{STB}}$	Master Reset	High

TABLE 7-4. REGISTERS/SIGNALS PARALLEL PORT RESET CONTROL

8.0 TYPICAL APPLICATIONS

Figures 8-1 and 8-2 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

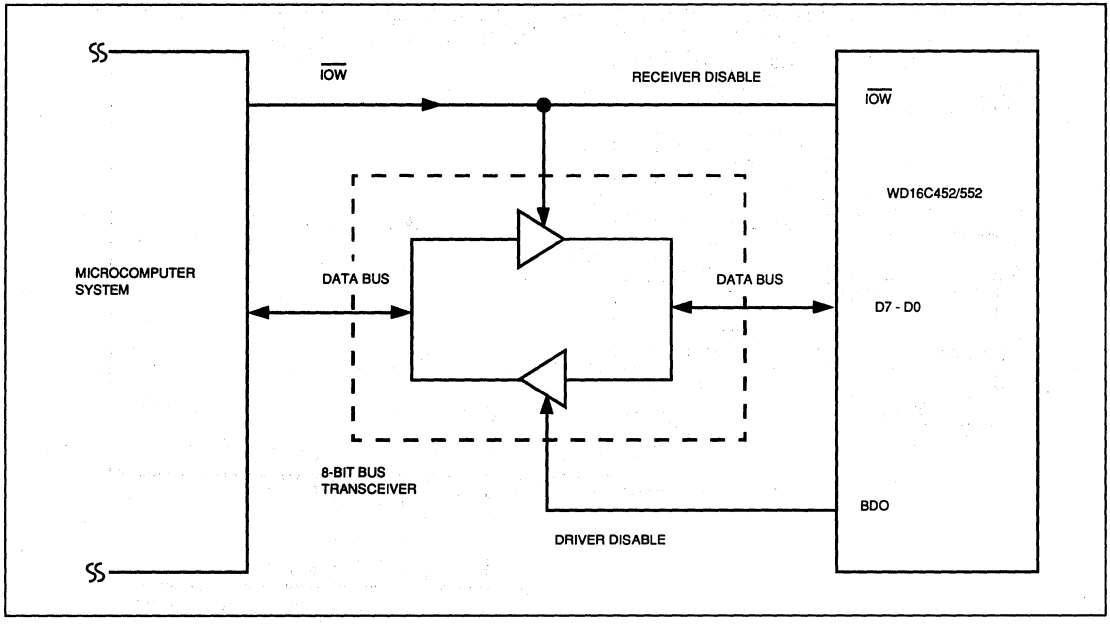


FIGURE 8-1. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

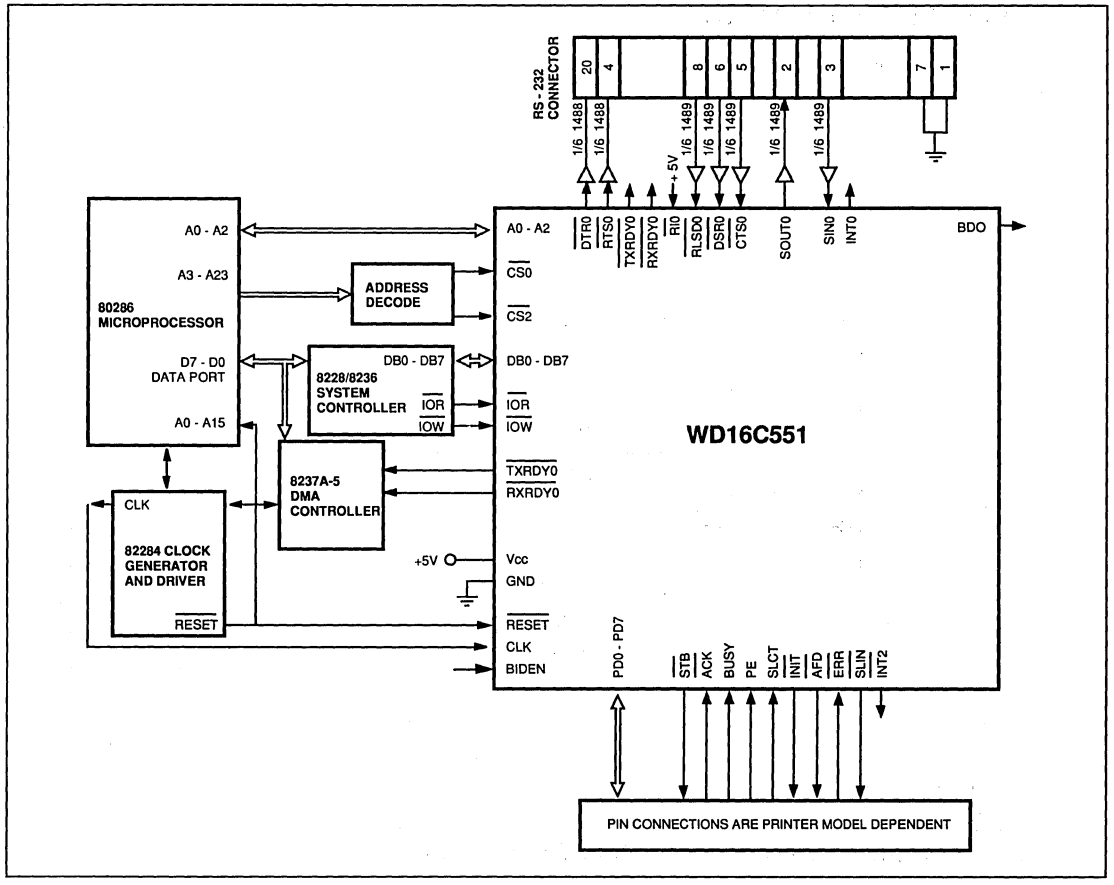


FIGURE 8-2. TYPICAL 16-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE WD16C551

9.0 CRYSTAL MANUFACTURERS (Partial List)

American Time Products Division
Frequency Control Products Inc
Woodside, NY 11337

Bliley Electric Company
Erie, PA 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, PA 17013

Q-Matic Corporation
Costa Mesa, CA 92626

CRYSTAL SPECIFICATIONS

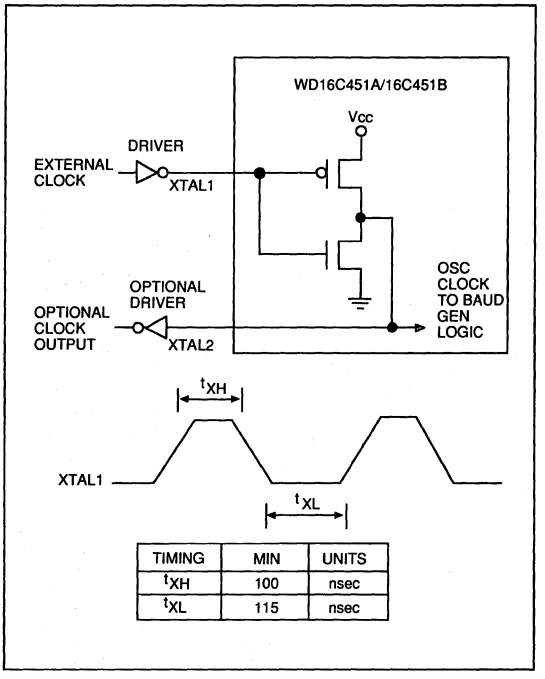
Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz

Type: Microprocessor Crystal

Temp. Range: 0°C (32°F) to +70°C (158°F)

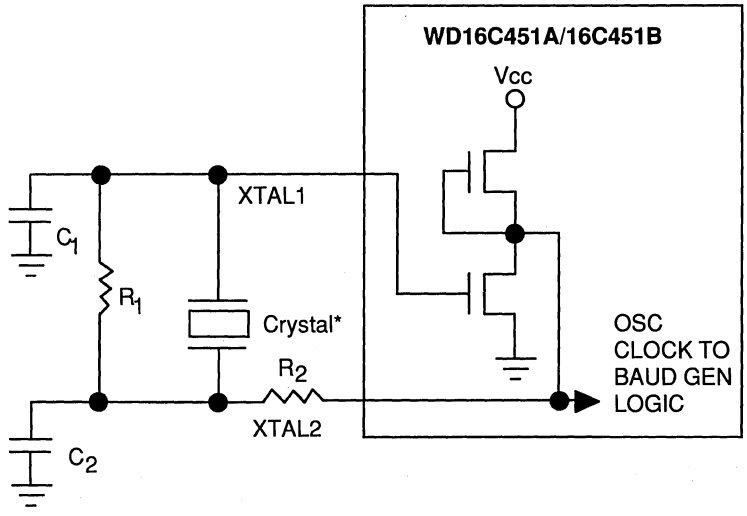
Series Resistance:
- 200-500 Ohms at 1.8432 MHz
- 100-200 Ohms at 3.072 MHz
- 20-40 Ohms at 8.0 MHz

Series Resonant
Overall Tolerance: ± 0.01%



TIMING	MIN	UNITS
t_{XH}	100	nsec
t_{XL}	115	nsec

FIGURE 9-1. EXTERNAL CLOCK INPUT (8.0 MHz MAXIMUM)



Crystal	R_1	R_2	C_1	C_2
8.0 MHz	1M Ohm	0-100 Ohm	5-10 pF	20-40 pF
3.1 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF
1.8 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF

EXAMPLE

FIGURE 9-2. TYPICAL CRYSTAL OSCILLATOR NETWORK

APPENDIX A

A.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages
With respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C451/WD16C551 ..... 300 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB, SLIN, AFD (NOTE). Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = 4.0 mA on DB0-DB7. Ioh = 15.0 mA on PD0-PD7. Ioh = 0.55 mA on INIT, AFD, STB, SLIN. Ioh = 0.2 mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.25V, no loads on outputs: SIN0, SIN1, DSR0, DSR1, RLSD0, RLSD1, CTS0, CTS1, RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
Iil	Input Leakage		æ10	uA	Vcc = 5.25V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage		±10	uA	Vin = 0.0V, 5.25V.
Idl	Data Bus Leakage		±10	uA	Vout = 0.4V, Vout = 4.6V Data Bus in High Impedance State.
Ioz	Tri-state Leakage		±20	uA	Vcc = 5.25V, GND = 0V, Vout = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE: The $\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{INIT}$ outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state, each input will sink a minimum of 20 mA. The internal pull-ups generate 2.0 mA of internal Iol.

Ta = 0°C (32°F) to = 70°C (158°F), Vcc = +5V±5%, Vss = 0V, unless otherwise specified.

TABLE A-1. DC OPERATING CHARACTERISTICS

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**TYP**	MAX	**UNITS**	**TEST CONDITIONS**
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

TABLE A-2. CAPACITANCE

1

APPENDIX B

B.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to + 70°C (158°F), Vss = +5V ±5%

TIMING DIAGRAMS

FIGURE NUMBER	TITLE
B-1	Receiver Timing
B-2	Transmitter Timing
B-3	MODEM Control Timing
B-4	Read Cycle Timing
B-5	Write Cycle Timing
B-6	RCVR FIFO Signaling Timing for First Byte
B-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
B-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
B-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-11	Transmitter DMA Mode 1 (FCR3 = 1)
B-12	Parallel Port Timing
B-13	WD16C451/WD16C451A Parallel Port Input Timing
B-14	WD16C551/WD16C451B Parallel Port Input Timing

TABLE B-1. WD16C451/WD16C551 TIMING DIAGRAMS

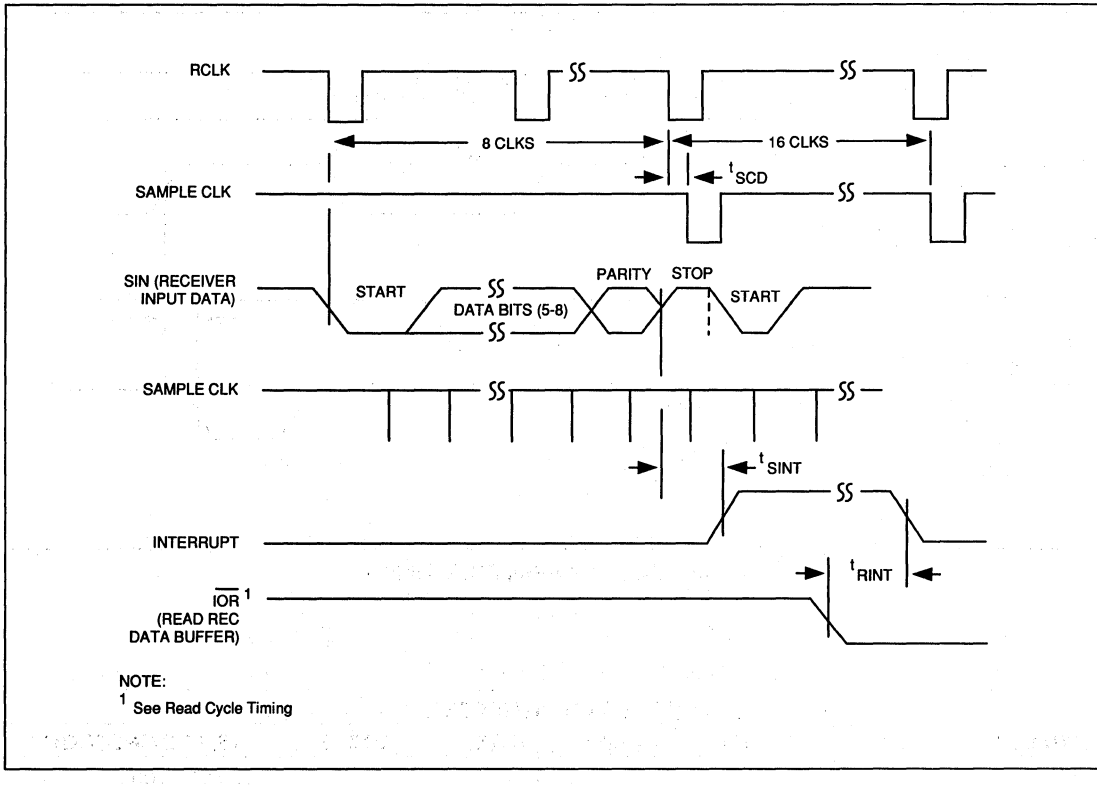


FIGURE B-1. RECEIVER TIMING

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tSCD	Delay from RCLK† to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrup		17♦	RCLK† Cycles	100 pF Load
tRINT	Delay from IOR (RD RBR) Reset Interrupt		1	µs	100 pF Load

(♦) When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

TABLE B-2. RECEIVER TIMING

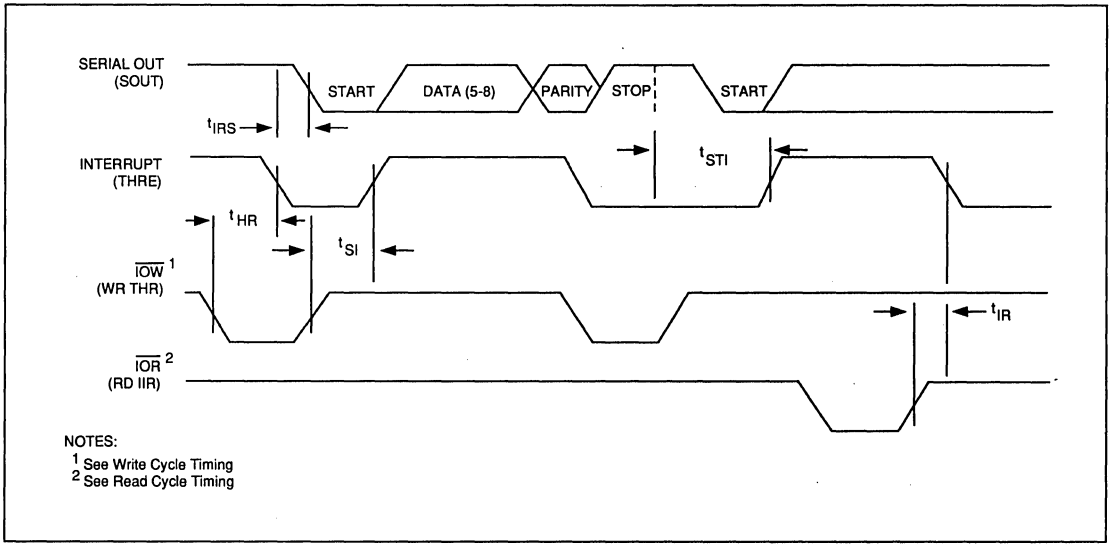


FIGURE B-2. TRANSMITTER TIMING

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tHR	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	TCLK† Clock Cycles	
tSI*	Delay from Initial Write to Interrupt	16	24	TCLK† Clock Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	TCLK† Clock Cycles	
tIR	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load
tSXA	Delay from Start to TXRDY Active	0	8	TCLK† Clock Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	300	ns	

(†) TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.
(*) In FIFO Mode, tSI might extend to beginning of Stop bit. See Line Status Register for details.

TABLE B-3. TRANSMITTER TIMING

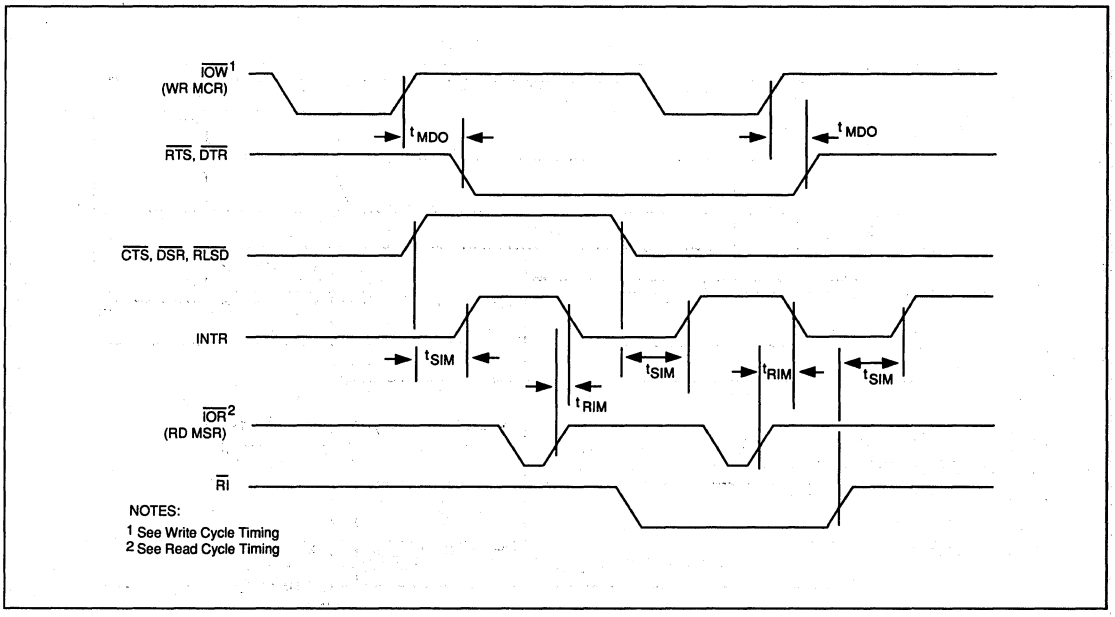


FIGURE B-3. MODEM CONTROL TIMING

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tMDO	Delay from IOW (WR MCR) to Output		200	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from IOR (RD MSR)		250	ns	100 pF Load

TABLE B-4. MODEM CONTROL TIMING

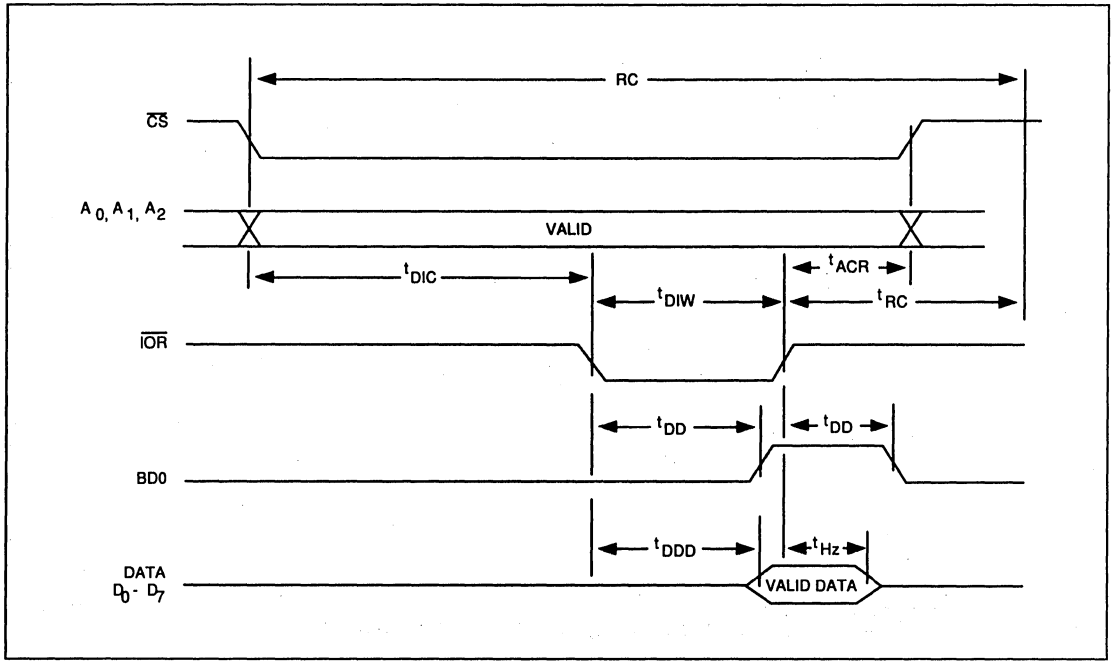


FIGURE B-4. READ CYCLE TIMING

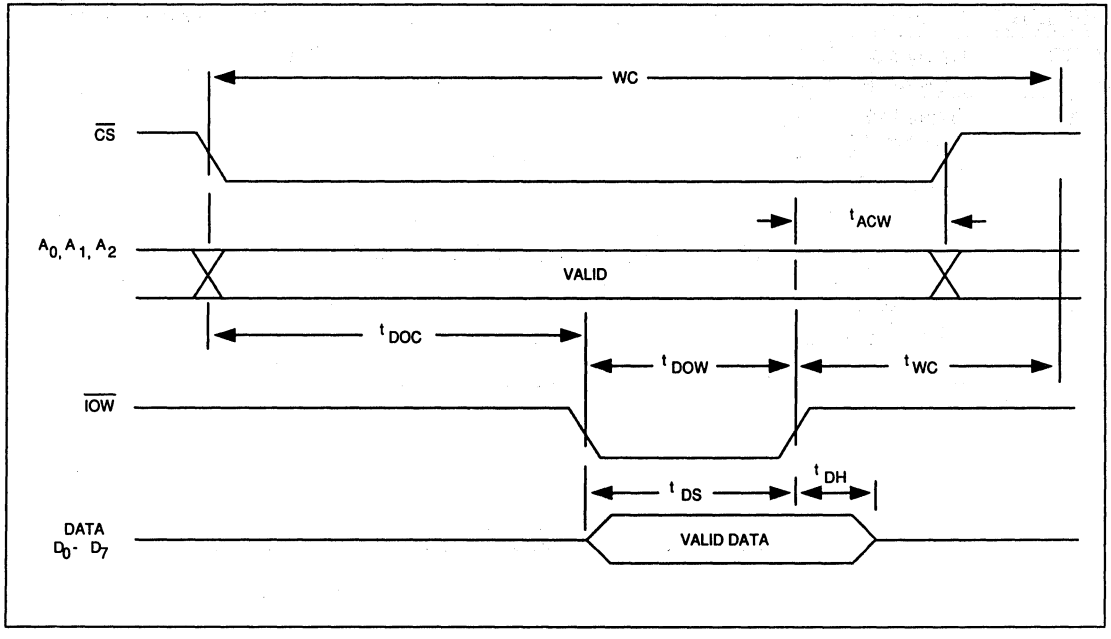


FIGURE B-5. WRITE CYCLE TIMING

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
tRC	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = tDIC + tDIW + tRC + 20 nsec	280		ns	1TTL Load
t_{DD}	$\overline{IOR}$ to Driver Enable (BDO) Delay		60	ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to Data		100	ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 nsec	280		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{MR}	Master Reset Pulse Width	5.0		µs	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse	55		ns	1TTL Load
t_{XL}	Duration of Clock LOW Pulse	55		ns	External Clock (8.0 MHz Max.)

TABLE B-5. READ/WRITE CYCLE TIMING

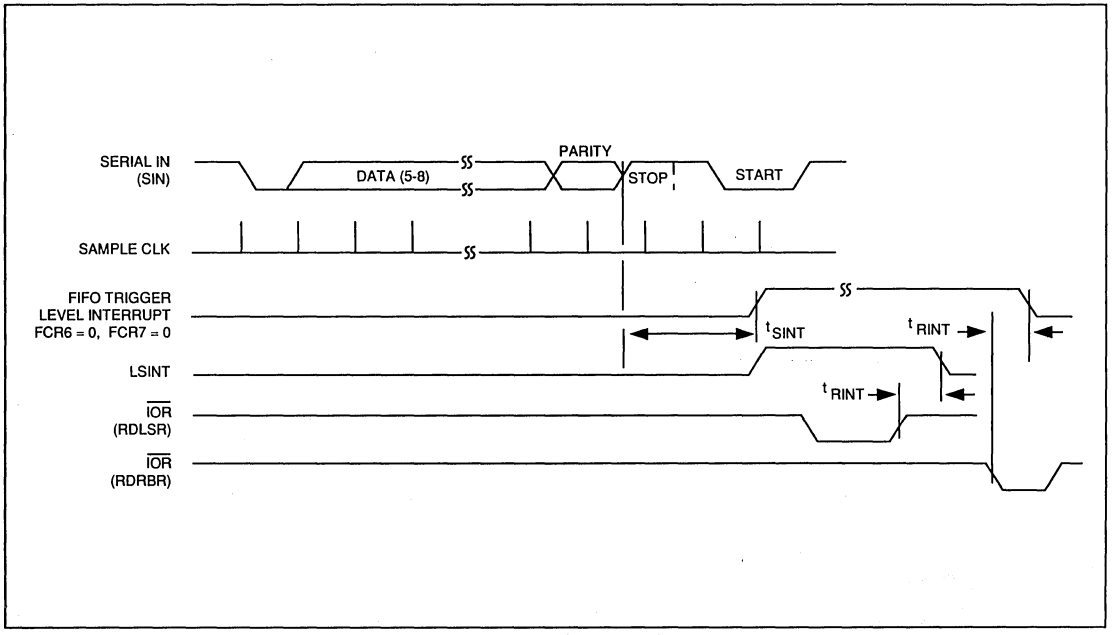


FIGURE B-6. RCVR FIFO SIGNALING TIMING FOR FIRST BYTE

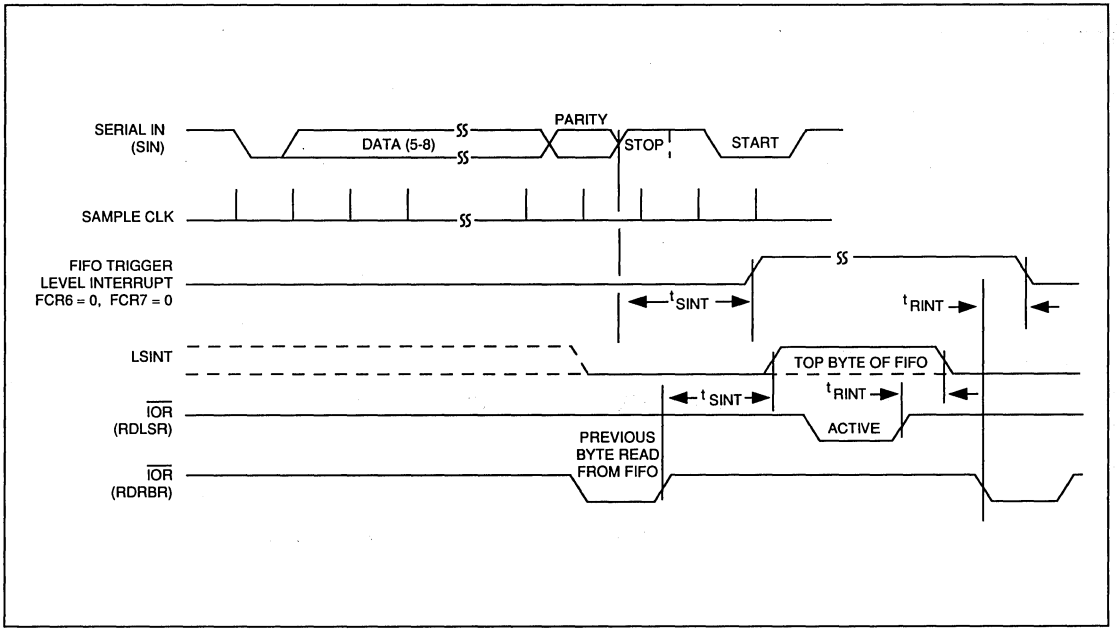


FIGURE B-7. RCVR FIFO SIGNALING TIMING AFTER FIRST BYTE (RBR Already Set)

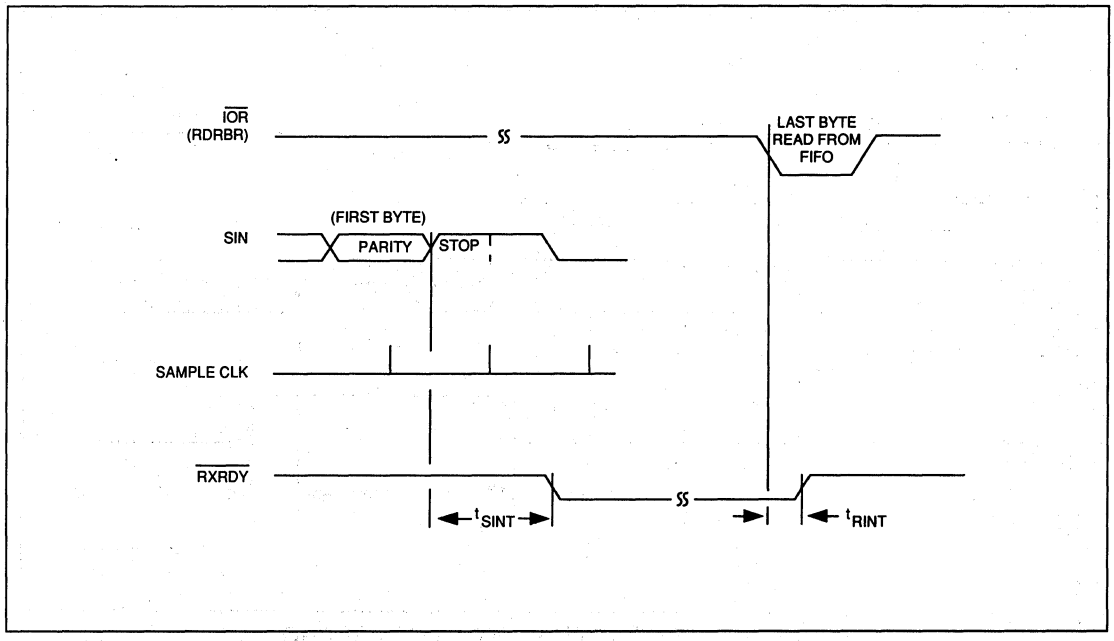


FIGURE B-8. RECEIVER DMA MODE 0 TIMING (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

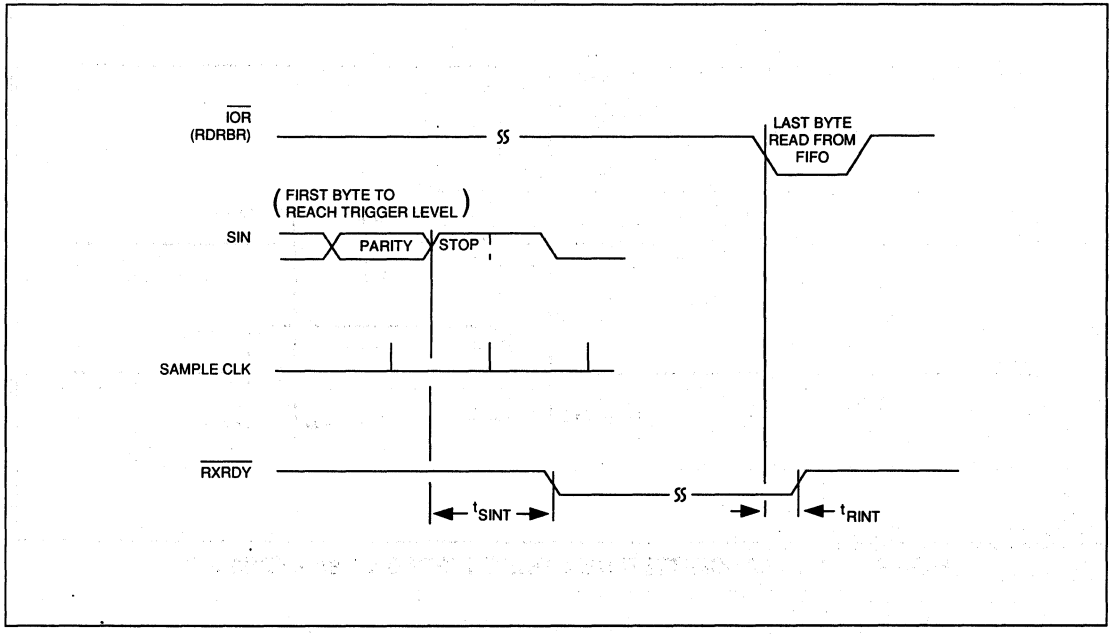


FIGURE B-9. RECEIVER DMA MODE 1 TIMING (FCR0=1 and FCR3=1)

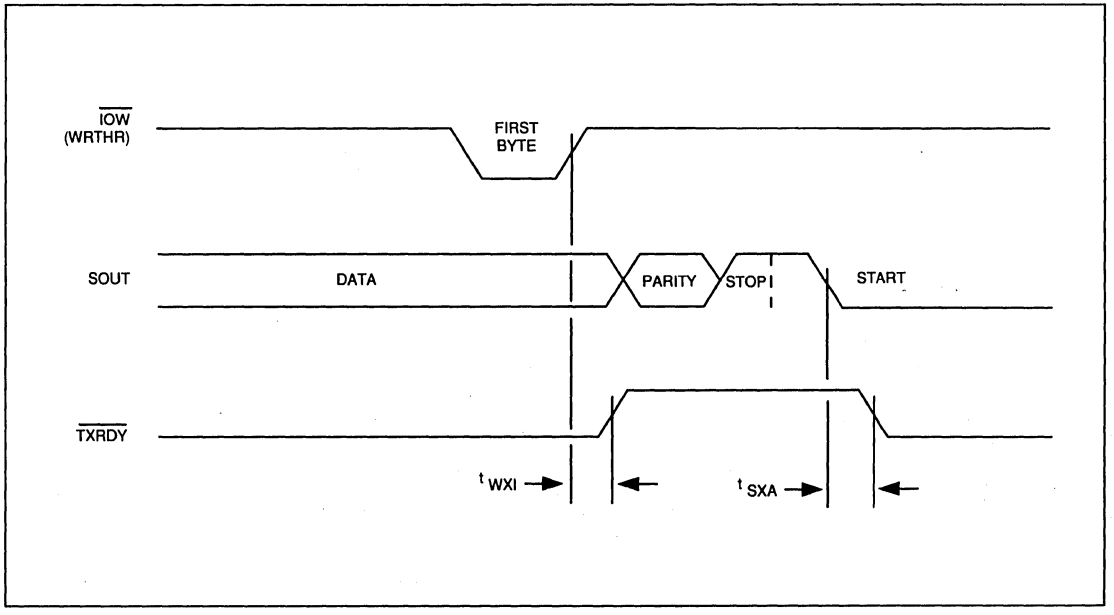


FIGURE B-10. TRANSMITTER DMA MODE 0 TIMING
(FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

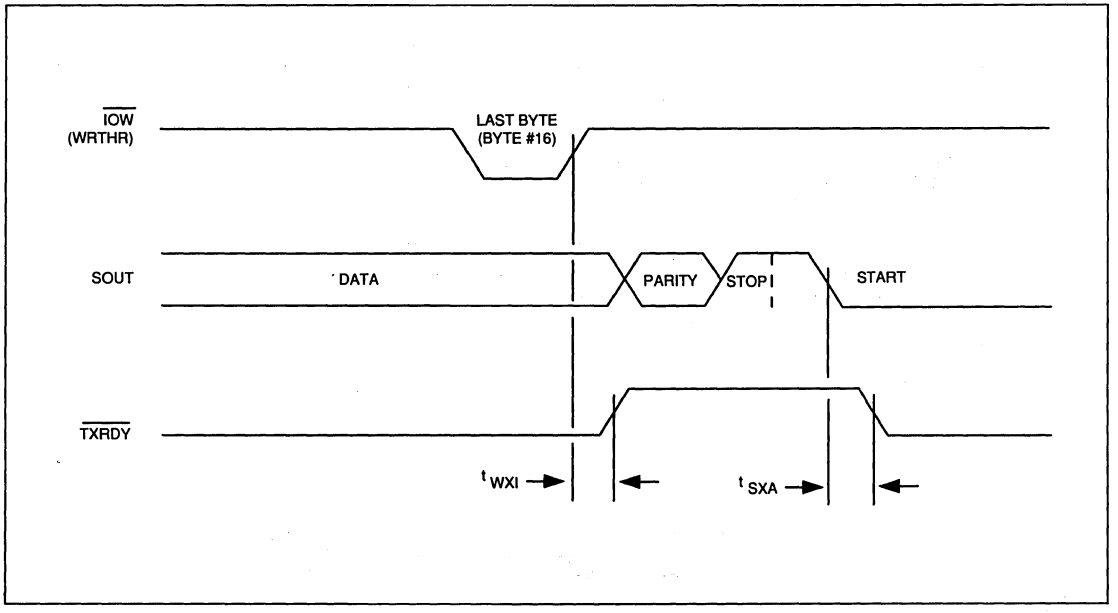
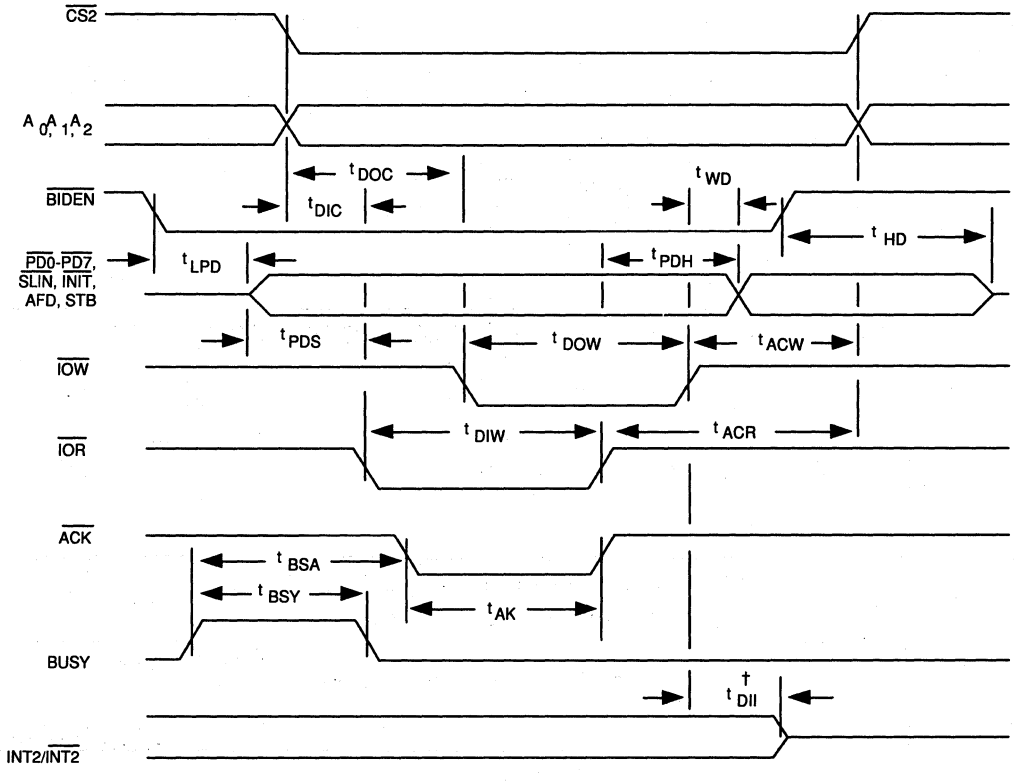


FIGURE B-11. TRANSMITTER DMA MODE 1 (FCR0 = 1 and FCR3 = 1)



† t_{DII} is the delay from the positive transition of $\overline{IOW}$ only when the Write Cycle, bit 4 of the Write Control Register (IRQ Enable Bit) is low.

FIGURE B-12. PARALLEL PORT TIMING

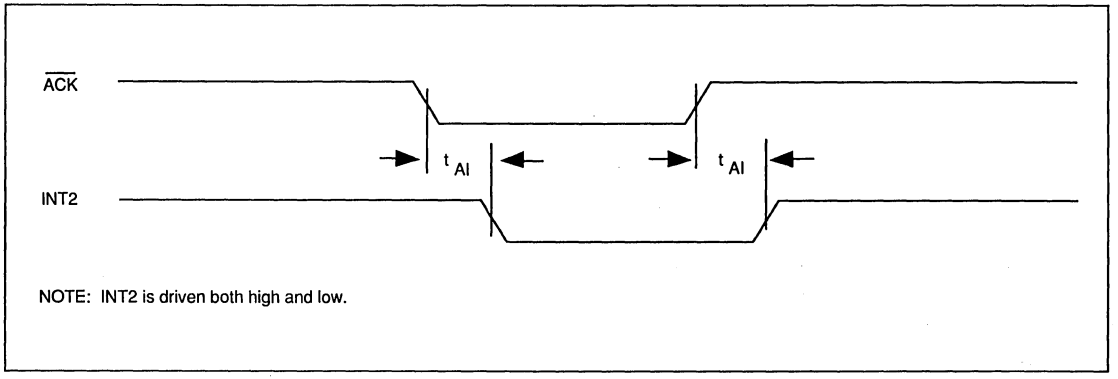


FIG. B-13. WD16C451/WD16C451A PARALLEL PORT INTERRUPT TIMING

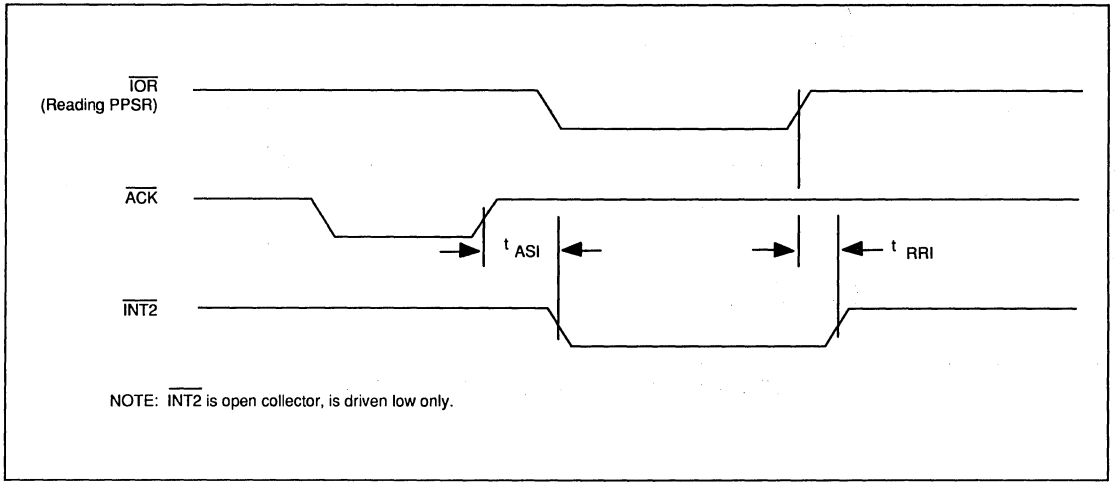


FIG. B-14. WD16C551/WD16C451B PARALLEL PORT INTERRUPT TIMING

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, SLIN, INIT, AFD, STB		1	µs	No External Pull-up Resistor and 50 pF load
t_{HD}	BIDEN High to PD0-PD7 Tri-State		120	ns	
t_{LPD}	BIDEN Low to PD0-PD7 Delay		100	ns	
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$			ms	Printer Dependent
t_{BSY}	BUSY Width			µs	Printer Dependent
t_{AK}	$\overline{ACK}$ Width			µs	Printer Dependent
t_{AI}	INT2 Delay from $\overline{ACK}$ (WD16C451)		60	ns	1 TTL Load
t_{ASI}	$\overline{ACK}$ to set interrupt (WD16C551)		60	ns	1 TTL Load
t_{RRI}	Read Parallel Port Status Register (PPSR) to reset INT2		60	ns	1 TTL Load
tDII	$\overline{IOW}$ high to INT2/$\overline{INT2}$ Tri-state	0	100	ns	1 TTL Load

TABLE B-6. PARALLEL PORT TIMING

1

APPENDIX C

C.O PACKAGE DIAGRAM

Figure C-1 illustrates the 68-Pin QUAD plastic package showing dimensions in inches.

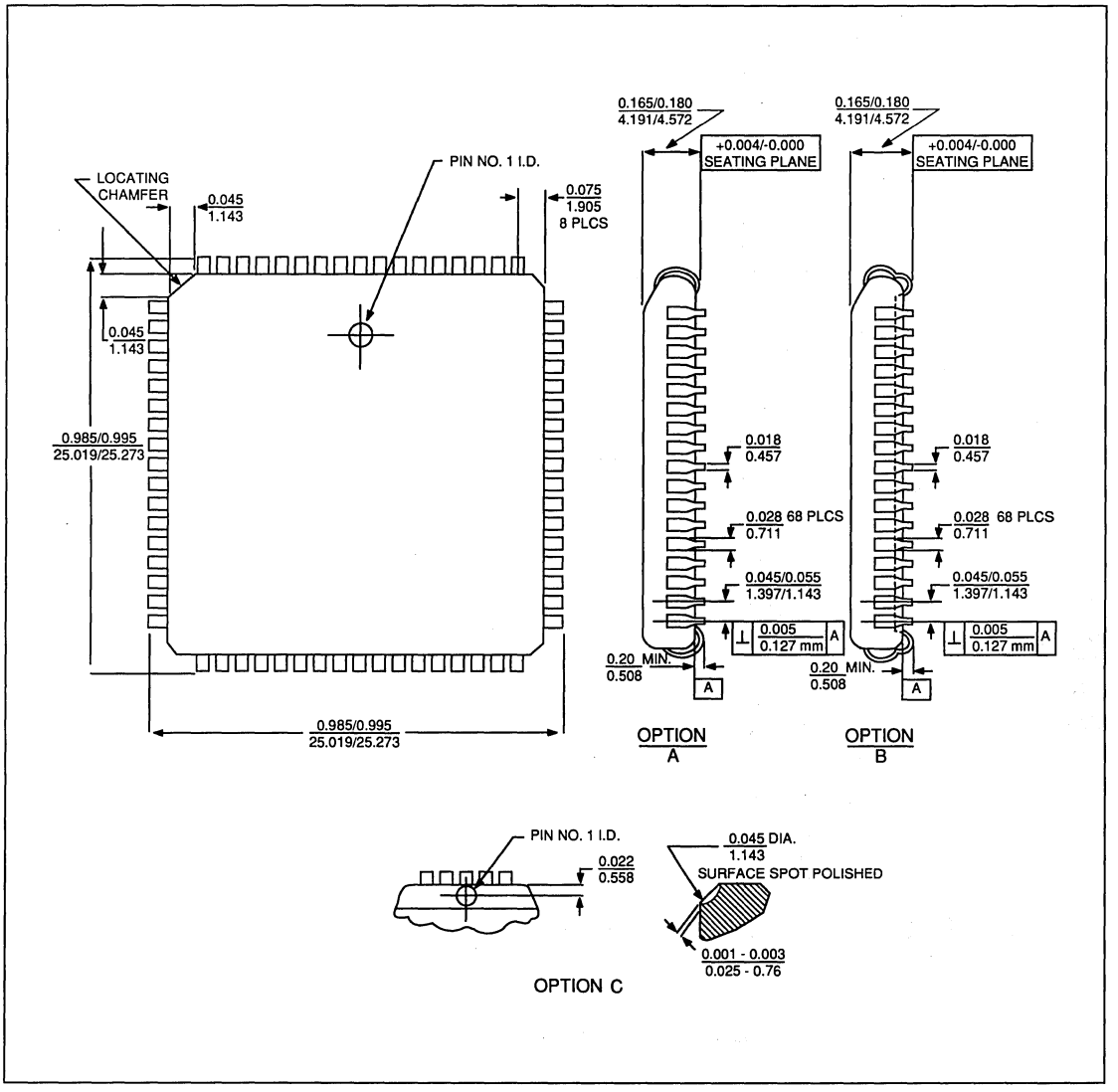


FIGURE C-1. 68-PIN QUAD PLASTIC PACKAGE

WD16C452, WD16C552

Dual Enhanced Asynchronous Communications Element (ACE) with Parallel Port

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The low power CMOS WD16C452/552 is a single device solution for serving two serial input/output ports simultaneously and one bi-directional parallel port for the IBM PC XT, PC AT, PS/2, and compatible systems. The WD16C452 parallel port is compatible with the Centronics printer port and IBM Serial/Parallel Adapter, and each ACE is programmable and compatible with a WD16C450. The WD16C552 parallel port is compatible with the IBM PS/2 bidirectional parallel port and each ACE is compatible with the WD16C550. Each ACE in the WD16C552 is programmable, and it is capable of buffering up to 16 bytes of data for transmission and up to 16 bytes of data upon reception, relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in a multitasking environment. DMA signaling, between the internal FIFO buffers and host CPU, allows single or multiple character transfers. Each ACE has a maximum recommended data rate of 512K with a clock frequency of 8.0 MHz.

1.2 FEATURES

- Two fully programmable serial I/O channels (DC to 512K baud)
- Tri-state TTL drive capabilities for bi-directional data bus and control bus on each channel
- Loopback controls for communications link fault isolation for each ACE
- Line break generation and detection for each ACE
- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals for each channel
- Fully prioritized independent interrupt system controls for each channel
- 16 byte FIFO buffers on both transmit and receive of each channel for CPU relief during high speed data transfer †
- Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each receive channel †
- Two modes of DMA signaling available for transfer of data characters to and from FIFO buffers †
- Bidirectional Centronics compatible parallel port for direct printer interface
- PS/2 compatible bidirectional parallel port †
- CMOS implementation for high speed and low power requirements

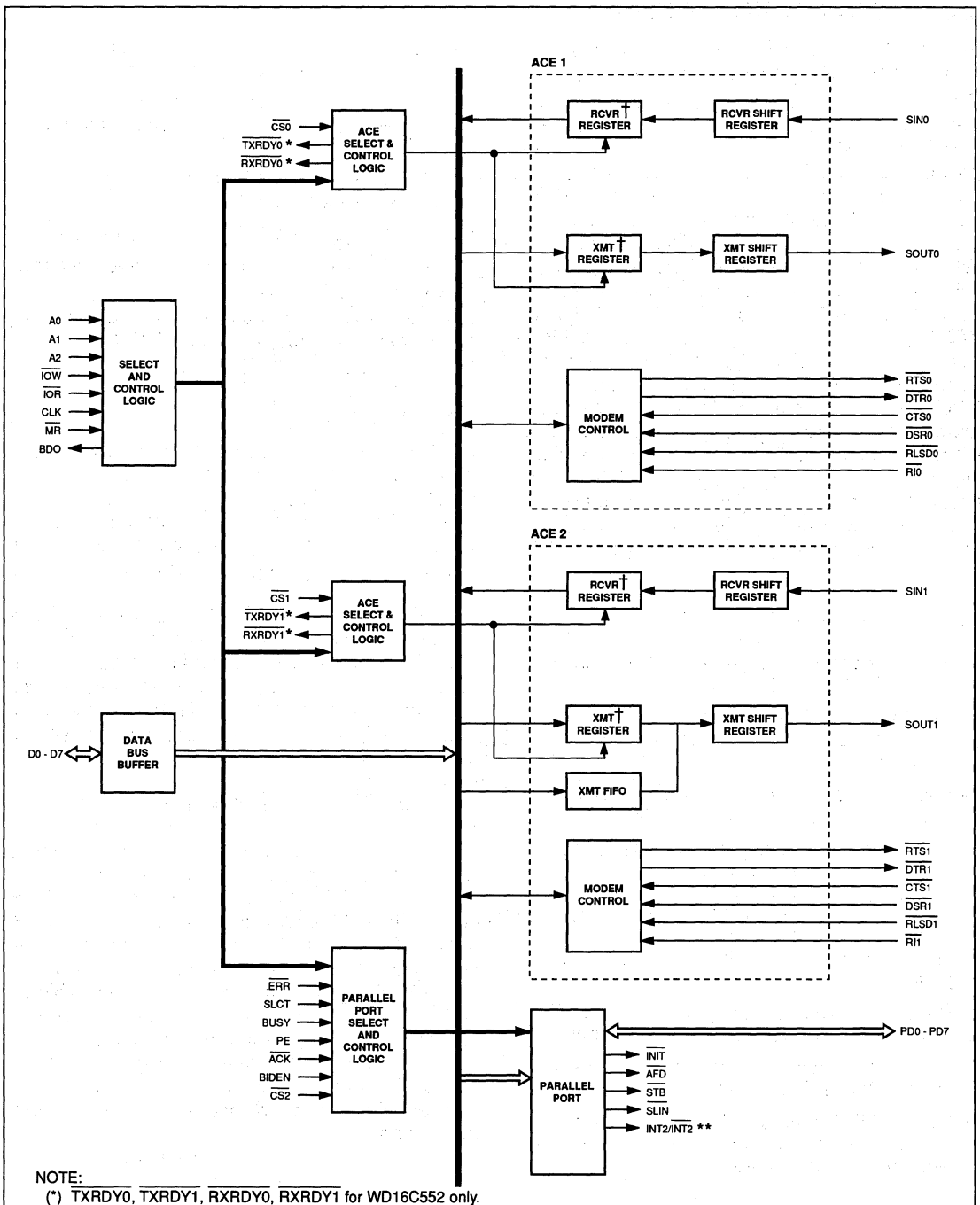
(†) The FIFO mode of operation and PS/2 compatible parallel port are not available in the WD16C452.

1.3 GENERAL

The WD16C452/WD16C552 is a dual ACE, plus a bidirectional parallel port. The two ACE's perform parallel-to-serial conversion on the output and serial-to-parallel conversion on the input. Each ACE is programmable, independent, and has a maximum recommended data rate of 512K baud.

The WD16C452 is a dual channel version of the WD16C450 ACE, plus a bidirectional parallel data port which supports a Centronics compatible printer interface. The parallel port, together with the two serial ports, provides IBM PC XT, PC AT, and compatibles with a single device solution for serving three ports.

The WD16C552 is a dual channel version of the WD16C550 Enhanced ACE, plus a compatible PS/2 bidirectional parallel port. After power-up and hardware reset, each ACE is functionally compatible to the WD16C450 (Character Mode). Each ACE in the WD16C552 has been enhanced with 16 byte FIFO buffers on both the receive and transmit lines, allowing an additional mode of operation called FIFO mode. FIFO mode (only available in WD16C552), can be activated through software, relieving the CPU of excessive overhead due to interrupts. The PS/2 parallel port, together with the two serial ports, provides IBM PS/2 and compatibles with a single device solution for serving three ports.



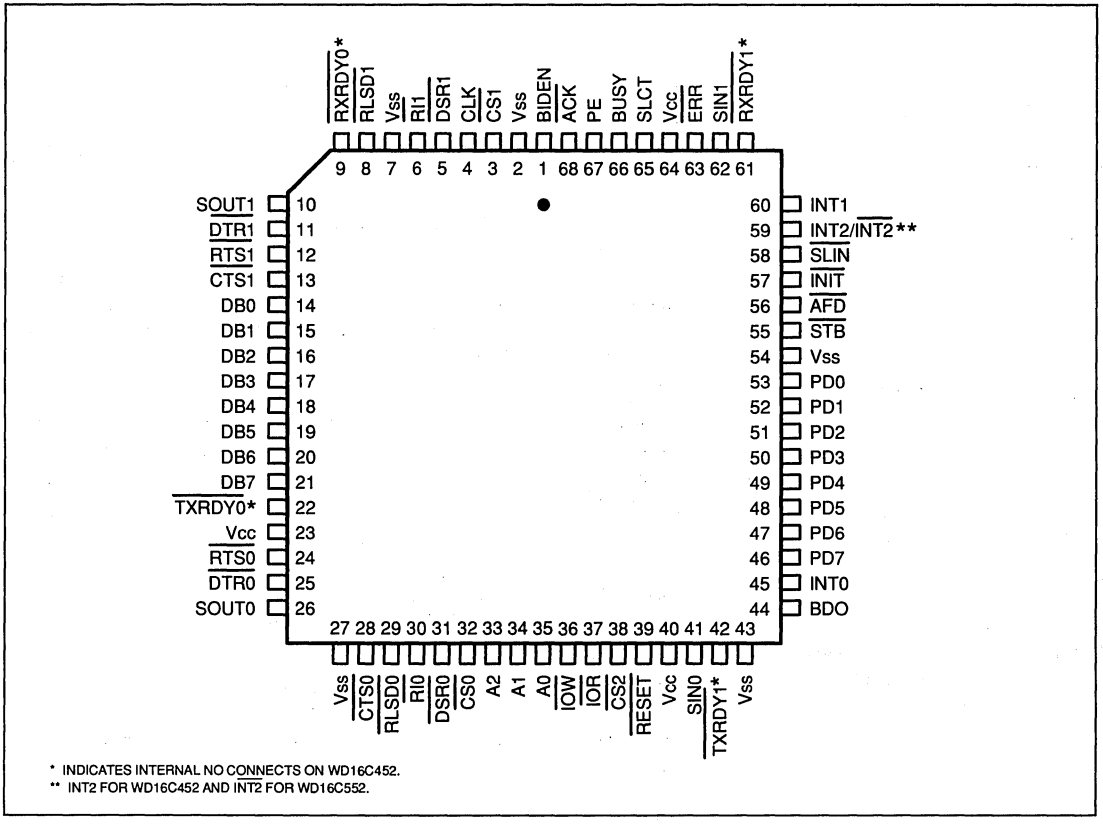
NOTE:
(*) TXRDY0, TXRDY1, RXRDY0, RXRDY1 for WD16C552 only.
(**) INT2 for WD16C452, INT2 for WD16C552.
(†) 16-byte FIFOs for WD16C552.

FIGURE 1-2. WD16C452/WD16C552 BLOCK DIAGRAM

2.0 SIGNAL DESCRIPTIONS

Figure 2-1 illustrates the 68-pin QUAD assembly.
Table 2-1 lists all signal descriptions.

2



* INDICATES INTERNAL NO CONNECTS ON WD16C452.
** INT2 FOR WD16C452 AND INT2 FOR WD16C552.

FIGURE 2-1. WD16C452/WD16C552 68-PIN QUAD ASSEMBLY

PIN	MNEMONIC	DESCRIPTION
1	BIDEN	**Bidirectional Enable** Input signal in the WD16C452, when low enables the parallel port data lines as outputs. When high the WD16C452 will hold the parallel port data pins in a high impedance state, allowing these pins to be driven with data. The BIDEN input signal on the WD16C552 works in conjunction with the DIR bit (see Table 7-3) to control the direction of the parallel port data bit.
2, 7, 27,43, 54	Vss	**Ground** System signal ground.
3	$\overline{CS1}$	**Chip Select 1** Chip Select input when active (low), selects serial channel 1.
4	CLK (1 time)	**Clock Input** External clock input.
5, 31	$\overline{DSR1}$, $\overline{DSR0}$	**Data Set Ready** When low, this input signal from the communication link indicates that it is ready to exchange data with the associated ACE. Bit 5 of the associated MODEM Status Register reflects the logical state of $\overline{DSR}$.
6, 30	$\overline{RI1}$, $\overline{RI0}$	**Ring Indicator** Input when low indicates, for the associated ACE, a ringing signal is being received by the MODEM or data set. This logical value is reflected in bit 6 of the associated MODEM Status Register.
8, 29	$\overline{RLSD1}$, $\overline{RLSD0}$	**Received Line Signal Detect** Input from the DCE indicating that the associated ACE is receiving a signal which meets its signal quality conditions. Bit 3 of the associated MODEM Status Register reflects this value.
9, 61	$\overline{RXRDY0}$, RXRDY1♦	**Receiver Ready** Receiver ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode. Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, $\overline{RXRDY}$ will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. $\overline{RXRDY}$ will go inactive when the RCVR FIFO (FIFO Mode), or holding register (Character Mode) is empty. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, $\overline{RXRDY}$ will go active (low) when the trigger level or time out has been reached. $\overline{RXRDY}$ goes inactive (high) when the FIFO is empty.

(♦) These pins are internal no connects on the WD16C452.

TABLE 2-1. SIGNAL DESCRIPTIONS

PIN	MNEMONIC	DESCRIPTION
10, 26	SOUT1, SOUT0	**Serial Data Output** Transmitted Serial Data Out to the communication link from the associated ACE. The SOUT signal is set to a marking condition (logical 1) upon a Master Reset.
11, 25	$\overline{DTR1}$, $\overline{DTR0}$	**Data Terminal Ready** Output when low informs the MODEM or data set that the associated ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
12, 24	$\overline{RTS1}$, $\overline{RTS0}$	**Request to Send** Output when low informs the MODEM or data set that the associated ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
13, 28	$\overline{CTS1}$, $\overline{CTS0}$	**Clear to Send** Input from DCE to the associated ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
14 - 21	DB0-DB7	**Data Bits** Tri-state, bidirectional communication lines between the ACE and Data Bus. D0 is the least significant bit (LSB) and the first serial transmitted or received bit.
22, 42	$\overline{TXRDY0}$♦,$\overline{TXRDY1}$♦	Transmitter Ready FIFO Control Transmit ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode. Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, $\overline{TXRDY}$ will be active (low) if there are no characters in the Xmit FIFO (FIFO Mode) or Xmit holding register (Character Mode). $\overline{TXRDY}$ will go inactive after the first character is loaded. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one, or more, unfilled position in the Xmit FIFO $\overline{TXRDY}$ will be active (low). $\overline{TXRDY}$ will go inactive when the FIFO is completely full
23, 40, 64	Vcc	**Power Supply** +5V power supply.
32	$\overline{CS0}$	Chip Select 0 Chip Select input when active (low) selects serial channel 0.
33 - 35	A2, A1, A0	**Address lines A2-A0** These three inputs are used to select an internal register of the ACE, or parallel port.

(♦) These pins are internal no connects on the WD16C452.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	DESCRIPTION
36	$\overline{IOW}$	**Input/Output Write Strobe** Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0, CS1, or CS2 to be ACE#1, ACE#2, or parallel port (respectively).
37	$\overline{IOR}$	**Input/Output Read Strobe** Input active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
38	$\overline{CS2}$	**Chip Select 2** Chip Select input when active (low), enables the line printer port.
39	$\overline{Reset}$	**Reset** Input when active (low), will force the device into an idle mode in which all serial data activities are suspended. The device will remain in an idle state until programmed to begin data activities.
41, 62	SIN0, SIN1	**Serial Data Inputs** Received Serial Data Input from the communication link to the associated ACE. Data on the serial data inputs are disabled when exercising loopback mode, and internally connected to their respective SIN lines.
44	BDO	**Bus Buffer Output** Output goes active when either serial channel, or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).
45, 60	INT0, INT1	**Serial Channel Interrupts** Tri-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending for theassociated ACE. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46 - 53	PD7-PD0	**Parallel Data Bits** Bidirectional data port which provides parallel input and output to the system. The eight lines are held in a high impedance state when $\overline{BIDEN}$ is high.
55	$\overline{STB}$†	**Line Printer Strobe** Output line, when active, provides the line printer with a signal to latch the data currently on the parallel port.
56	$\overline{AFD}$†	**Line Printer Autofeed** Output line, when active, provides a signal for the line printer to autofeed continuous form paper.

(†) These outputs are open drain with internal pull-ups.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	DESCRIPTION
57	$\overline{\text{INIT}}$†	**Line Printer Initialize** Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	$\overline{\text{SLIN}}$†	**Line Printer Select** Output line, when active (low), selects the printer.
59	INT2/$\overline{\text{INT2}}$††	**Interrupt Printer Port** Tri-state output enabled by bit 4 of WCR. For the WD16C452, INT2 goes active (high) on the rising transition of $\overline{\text{ACK}}$ and reset (low) on the falling transition of $\overline{\text{ACK}}$. For the WD16C552 INT2 goes active (low) on the rising edge of $\overline{\text{ACK}}$. $\overline{\text{INT2}}$ is reset (high) on the rising edge of $\overline{\text{IOR}}$, when reading the parallel port status register.
63	$\overline{\text{ERR}}$	**Line Printer Error** Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.
65	SLCT	**Line Printer Select** Input from the line printer that goes high when the line printer has been selected.
66	BUSY	**Line Printer Busy** Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	**Line Printer Paper Empty** Input from the line printer goes high when the printer is out of paper.
68	$\overline{\text{ACK}}$	**Line Printer Acknowledge** Input from line printer that goes low to confirm the data transfer from the WD16C552 to the printer was successful.

(†) These outputs are open drain with internal pull-ups.
(††) This pin is INT2 for WD16C452 and $\overline{\text{INT2}}$ for WD16C552.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

3.0 SERIAL CHANNEL REGISTERS

The WD16C552 contains two serial ports. Therefore, the following registers exist in duplicate, one per channel.

3.1 SERIAL PORT REGISTER ADDRESSING

Chip Select ($\overline{CS0}$, $\overline{CS1}$): When $\overline{CS0}$ is low, registers for serial channel 0 can be accessed, and when CS1 is low, registers for serial channel 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$) should ever be low at any time (an invalid condition).

Master Reset:
A low level input on this pin causes the ACE to reset to the condition listed in Table 4-1.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an Idle Mode. (Registers are not reset by this operation.) Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to return to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

Register Select (A0, A1, A2): To select a register for read or write operation, see Table 3-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING

4.0 ACE OPERATIONAL DESCRIPTION

4.1 MASTER RESET

A low-level input on this pin causes the ACE to reset to the condition listed in Table 4-1.

4.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in Table 4-2. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	BDO = $\overline{RCLK \cdot IOR}$ (At Master Reset, the CPU sets RCLK and $\overline{IOR}$ = Low when device is selected.)	High
INT0,1 (RCVR ERRS)	Master Reset/Read LSR	Low
INT0,1 (RCVR DATA READY)	Master Reset/Read RBR	Low
INT2 (WD16C452)	Master Reset/$\overline{ACK}$ (High)	Low
$\overline{INT2}$ (WD16C552)	Master Reset/Read PPSR	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO Counter (WD16C552 only)	MR or FCR1• FCR0 or ΔFCR0	All Bits Low
XMIT FIFO Counter (WD16C552 only)	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL (WD16C552 only)	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	InTri-state Mode, Unless IOR = Low or IOW = Low when Device is Selected	Tri-state Data (ACE to CPU) Data (CPU to ACE)

TABLE 4-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

	REGISTER ADDRESS					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)♦	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

(♦) These bits are 0 in Character Mode.

TABLE 4-2. ACCESSIBLE WD16C452/WD16C552 REGISTERS

	REGISTER ADDRESS					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO♦ (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

(♦) These bits are 0 in Character Mode.

TABLE 4-2. ACCESSIBLE WD16C452/WD16C552 REGISTERS (Contd)

4.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

4.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4-3, 4-4, and 4-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2	2.860

TABLE 4-3. BAUD RATES USING 1.8432 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3	14.285

TABLE 4-4. BAUD RATES USING 3.072 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 4-5. BAUD RATES USING 8.0 MHz CLOCK

4.5 LINE STATUS REGISTER

This 8-bit read and write register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 4-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 by the CPU reading the data in the Receiver Buffer Register (for Character Mode).

In FIFO Mode, Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it occurs. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level). Bit 3 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. When in FIFO Mode, an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits). Bit 4 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received requires the SIN pin be high for at least one-half (1/2) bit time.

When in FIFO Mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits except bit 7 of the Status Register can be set or reset by writing to the register.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. This bit also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO. The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs: the Transmitter FIFO is empty and there have not been at least two characters in Transmitter FIFO at the same time since the last time that Transmitter FIFO was empty. The first transmitter interrupt after changing the first bit of FIFO Control Register will be immediate if it is enabled.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 when both trans-

mitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO and XMIT Shift Register are both empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no additional errors in the FIFO.

4.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 4-2).

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 4-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see Table 4-6).

Bits 4 and 5: These bits are always logic 0.
Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

INTERRUPT IDENTIFICATION REGISTER					INTERRUPT SET AND RESET FUNCTIONS		
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 4-6. INTERRUPT CONTROL FUNCTIONS

4.7 INTERRRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in Table 4-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

4.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer as a general purpose register.

4.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from RCVR Error FIFO. The FIFOs should be cleared immediately after changing to FIFO mode. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR Error FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

5.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 4-2.

Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

NOTE:
The DTR output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

Bit 3: This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs (CTS, DSR, RLSD, and $\overline{RI}$) are disconnected; and the four MODEM Control bits (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

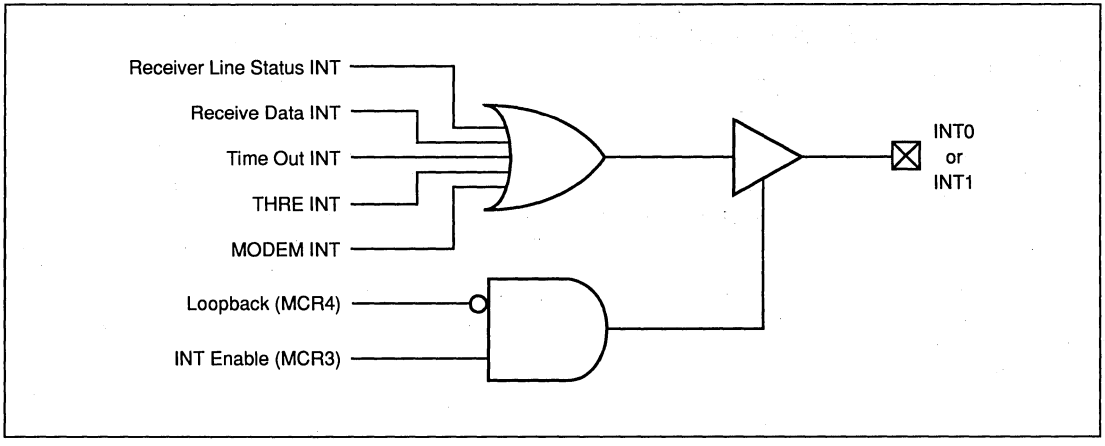


FIGURE 5-1. INTERRUPT SIGNAL LOGIC

6.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 4-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timed interrupt occurs when:
   a. There is at least one byte in the RCVR FIFO.
   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2 When the RCVR FIFO reaches its programmed trigger level, the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Pointer Notes:

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte to be read and the associated Status byte. Reading the RCVR Data byte will increment the internal counter, whereas reading the Status byte will not. The Status byte should always be read prior to the Data byte associated with it.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode, the user can poll the LSR directly to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately, either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated on the Interrupt pin in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

7.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics-type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to Tables 7-1 and 7-2.)

Register Descriptions:

Read Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

Read Status Register

Bits 0 through 1: These bits are set to a logic one.

Bit 2: This bit represents the status of the $\overline{INT}$ pin. This bit is only available in the WD16C552.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to Table 7-2.

Read Control Register

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to Table 7-2. NOTE: These values reflect the signal on the open drain outputs, not necessarily the value in the write control register.

Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Control
1	1	1	0	Invalid

TABLE 7-1. PARALLEL PORT (CS2=0) REGISTER ADDRESSES

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	$\overline{INT}^{\blacklozenge}$	$\overline{Init}$	$\overline{Init}$	Data Bit 2
3	Data Bit 3	$\overline{Error}$	Slin	Slin	Data Bit 3
4	Data Bit 4	Slct	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	DIR$^{\blacklozenge}$	Data Bit 5
6	Data Bit 6	$\overline{Ack}$	1	1	Data Bit 6
7	Data Bit 7	Busy	1	1	Data Bit 7

TABLE 7-2. ACCESSIBLE PARALLEL PORT REGISTERS

Bits 5 through 7: These bits always return to a logic one.

Write Port Register

Bits 0 through 7: These bits correspond to the data to be placed on the parallel bus. This register is used to write data to the parallel bus based on Table 7-3.

Write Control Register

Bits 0 through 4: Writing to these bits will set the output of the corresponding pins.

Bit 5: The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus in extended mode, as described in the table below. This bit is only available in the WD16C552, and is a write only bit.

PORT MODE	PORT DIRECTION	PIN 1 BIDEN	DIRECTION BIT
Extended	Write	1	0
Extended	Write	0	X
Extended	Read	1	1
Compatible	Write	0	N/A
Compatible	Read	1	N/A

TABLE 7-3. PARALLEL PORT OPERATION MODES

REGISTER/ SIGNAL	RESET CONTROL	RESET STATE
Control	Master Reset	All bits low.
Data (Write)	Master Reset	All bits low.
Data (Read)	Master Reset	Data
Status	Master Reset	Bits 0-2 are high, Bits 3-7 are ERR, SLCT, PE, ACK and Busy inputs.
INT2	Master Reset	High Impedence.
$\overline{\text{SLIN}}$	Master Reset	High.
$\overline{\text{INIT}}$	Master Reset	Low.
$\overline{\text{AFD}}$	Master Reset	High.
$\overline{\text{STB}}$	Master Reset	High.

TABLE 7-4. PARALLEL PORT RESET CONTROL OF REGISTERS & SIGNAL

8.0 TYPICAL APPLICATIONS

Figures 8-1 and 8-2 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

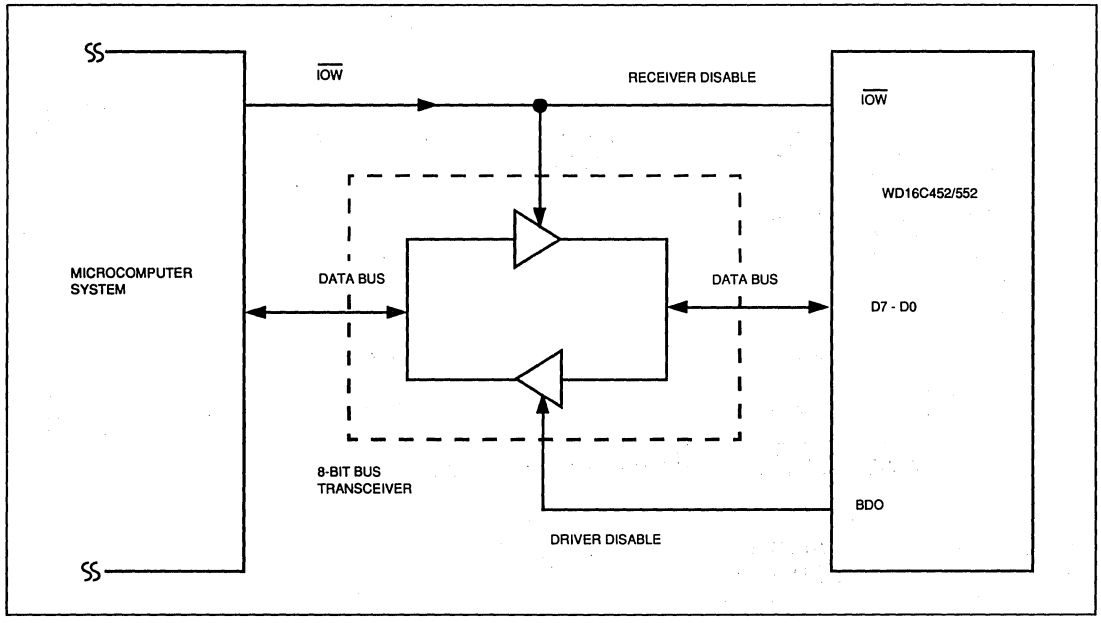


FIGURE 8-1. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

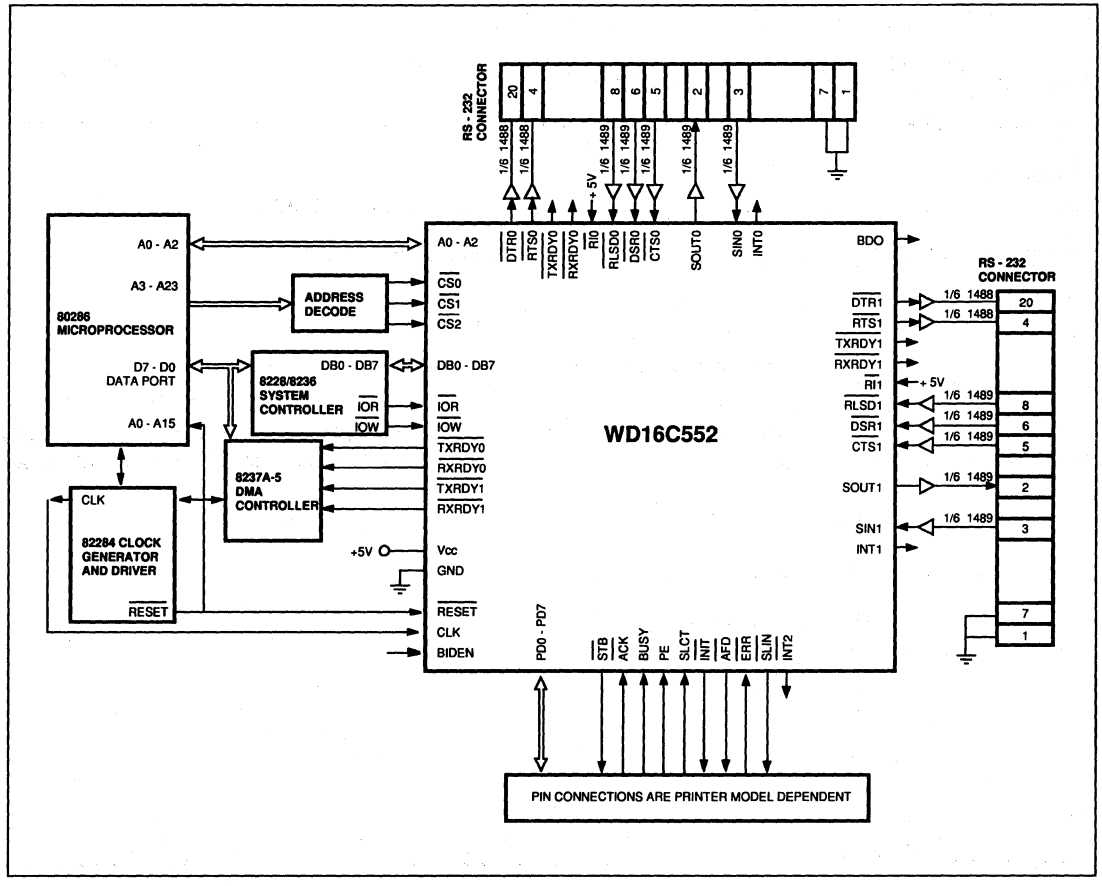


FIGURE 8-2. TYPICAL 16-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE WD16C552

APPENDIX A

A.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias . . . . . .0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . .-65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages
with respect to Vss . . . . . .-0.5V to +7.0V

Power Dissipation WD16C452/WD16C552 . . . . . .300 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics.

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB , SLIN, AFD (NOTE). Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB0-DB7. Ioh = -15.0 mA on PD0-PD7. Ioh = -0.55 mA on INIT, AFD, STB, SLIN. Ioh= -0.2 mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.25V, no loads on outputs: SIN0, SIN1, DSR0, DSR1, RLSD0, RLSD1, CTS0, CTS1, RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
Iil	Input Leakage		±10	µA	Vcc = 5.25V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage		±10	µA	Vin = 0.0V, 5.25V.
Idl	Data Bus Leakage		±10	µA	Vout = 0.4V, Vout = 4.6V Data Bus in High Impedance State.
Ioz	3 State Leakage		± 20	µA	Vcc = 5.25V, GND = 0V, Vout = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE:
The SLIN, AFD, STB and INIT outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state, each input will sink a minimum of 20 mA. The internal pull-ups generate 2.0 mA of internal Iol.

TABLE A-1. DC OPERATING CHARACTERISTICS
Ta = 0°C (32°F) to =70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, Unless Otherwise Specified.

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 TYP	MAX	UNITS	TEST CONDITIONS
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

TABLE A-2. CAPACITANCE
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

APPENDIX B

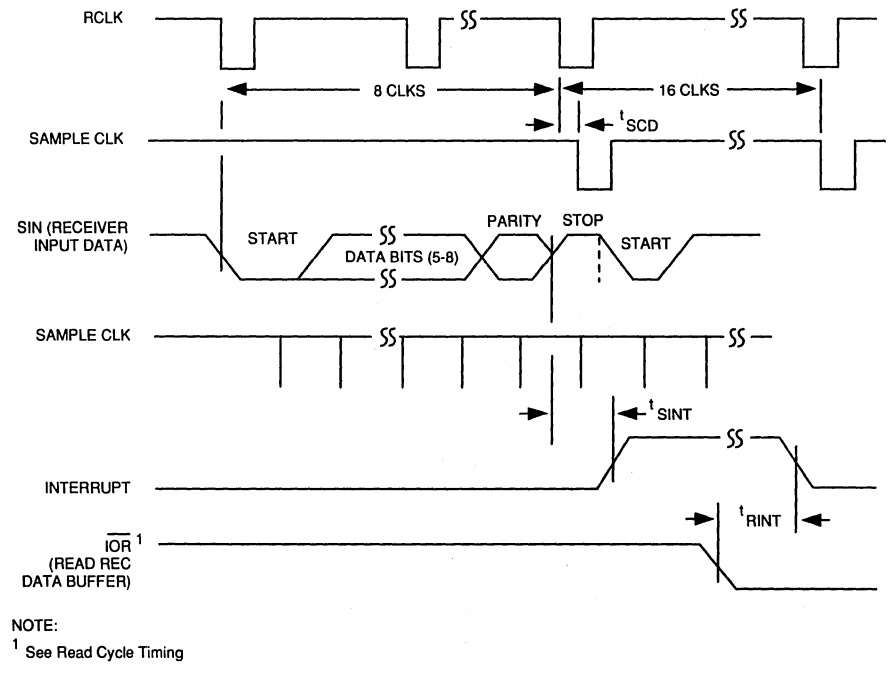
B.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%

B.1 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
B-1	Receiver Timing
B-2	Transmitter Timing
B-3	MODEM Control Timing
B-4	Read Cycle Timing
B-5	Write Cycle Timing
B-6	RCVR FIFO Signaling Timing for First Byte
B-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
B-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
B-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-11	Transmitter DMA Mode 1 (FCR3 = 1)
B-12	Parallel Port Timing
B-13	WD16C452 Parallel Port Interrupt Timing
B-14	WD16C552 Parallel Port Interrupt Timing

TABLE B-1. WD16C452/WD16C552 TIMING DIAGRAMS



NOTE:
1 See Read Cycle Timing

FIGURE B-1. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK† to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		17♦	RCLK† Cycles	100 pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt		1	µs	100 pF Load

(♦) When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data.
RCLK is equivalent to 16 times the baud rate clock.

TABLE B-2. RECEIVER TIMING

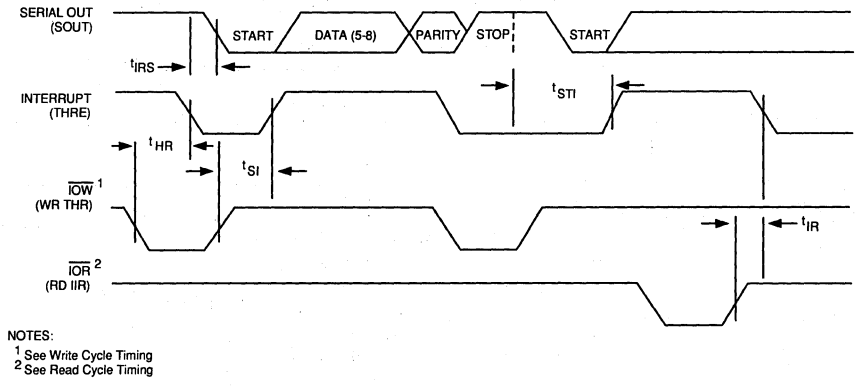


FIGURE B-2. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
^tDIW	IOR Strobe Width	125		ns	1TTL Lpad
^tRC	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = $^tDIC + ^tDIW + ^tRC$ + 20 nsec	280		ns	1TTL Load
^tDD	IOR to Driver Enable (BDO) Delay		60	ns	1TTL Load
^tDDD	Delay from IOR to Data		100	ns	1TTL Load
^tHZ	IOR to Floating Data Delay	0	100	ns	1TTL Load
^tDOW	IOW Strobe Width	100		ns	1TTL Load
^tWC	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + $^tDOC + ^tDOW + ^tWC$ + 20 nsec	280		ns	1TTL Load
^tDS	Data Setup Time	30		ns	1TTL Load
^tDH	Data Hold Time	30		ns	1TTL Load

TABLE B-3. TRANSMITTER TIMING

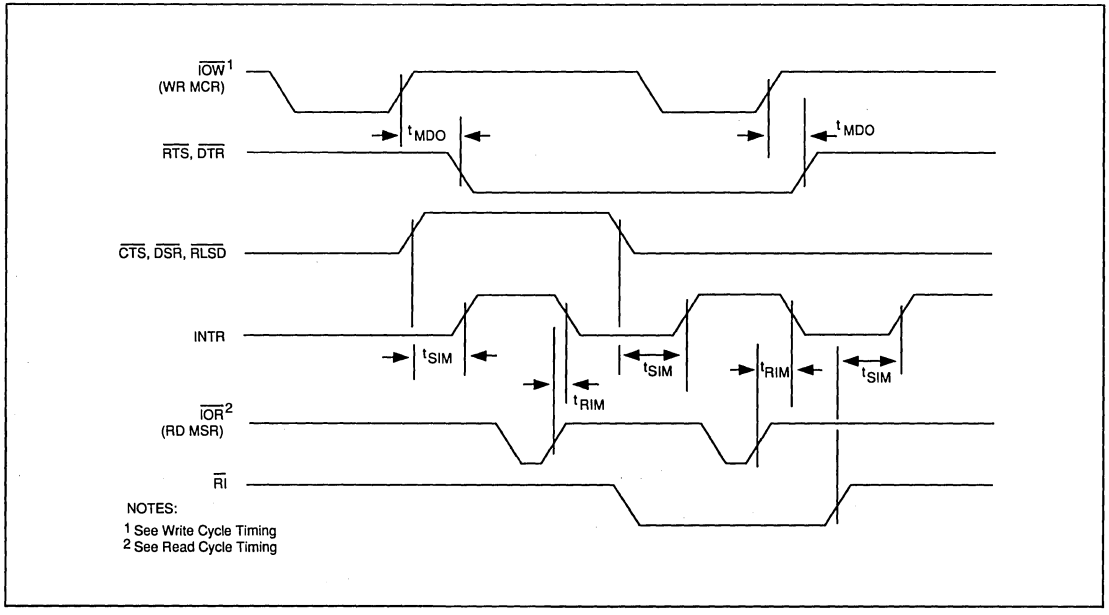


FIGURE B-3. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
^{t}MDO	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
^{t}SIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
^{t}RIM	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		250	ns	100 pF Load

TABLE B-4. MODEM CONTROL TIMING

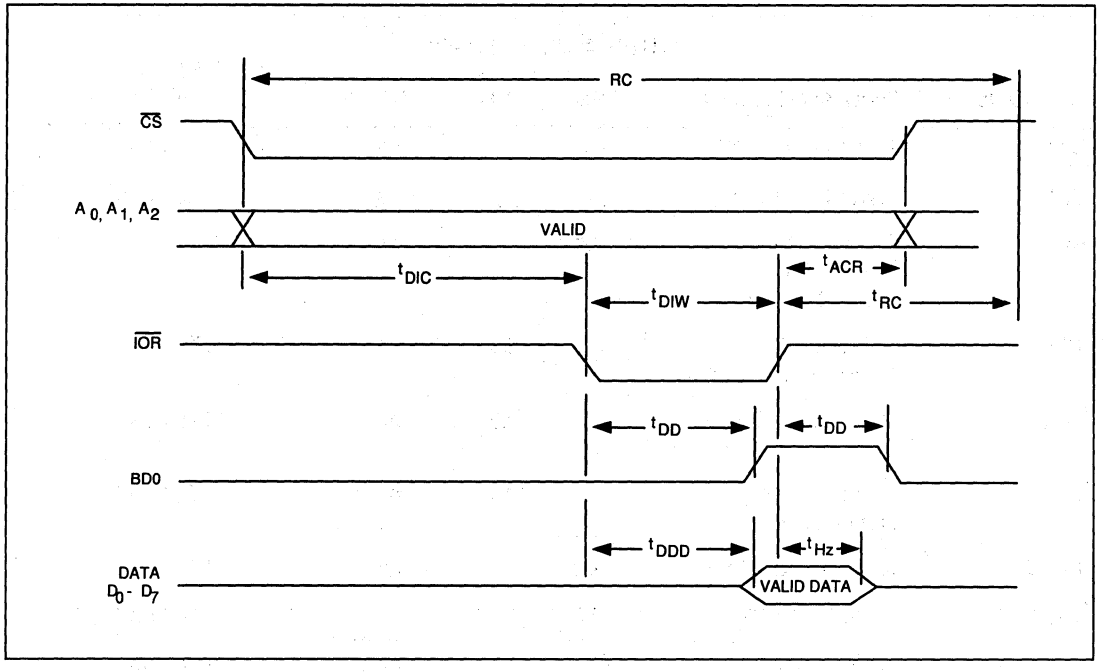


FIGURE B-4. READ CYCLE TIMING

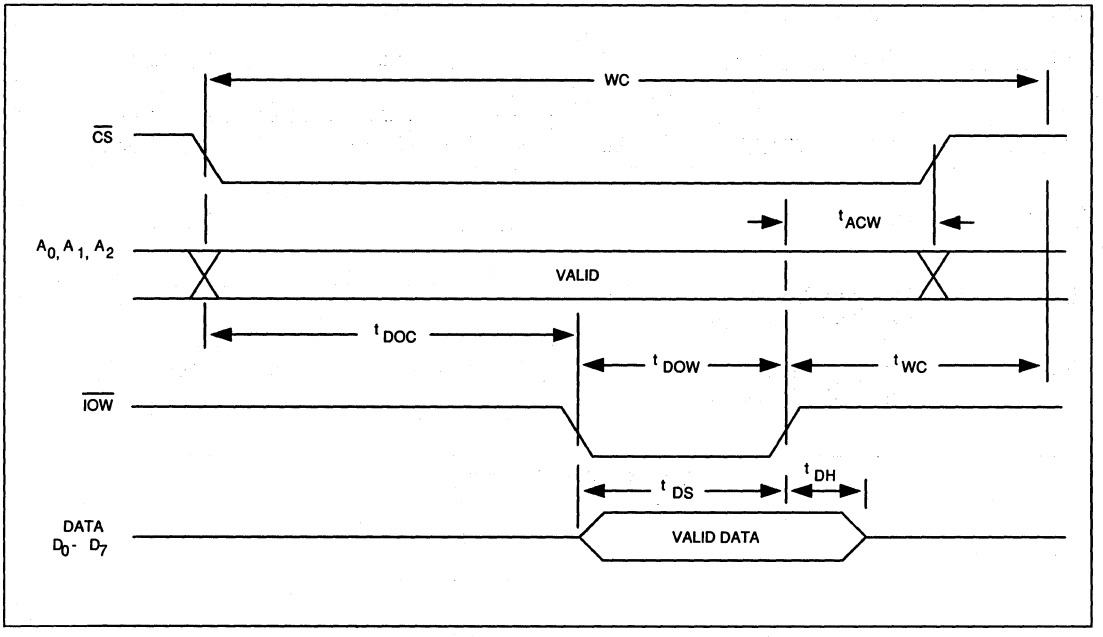


FIGURE B-5. WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
^tDIW	IOR Strobe Width	125		ns	1TTL Lpad
^tRC	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = $^tDIC + ^tDIW + ^tRC$ + 20 nsec	280		ns	1TTL Load
^tDD	IOR to Driver Enable (BDO) Delay		60	ns	1TTL Load
^tDDD	Delay from IOR to Data		100	ns	1TTL Load
^tHZ	IOR to Floating Data Delay	0	100	ns	1TTL Load
^tDOW	IOW Strobe Width	100		ns	1TTL Load
^tWC	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = $+ ^tDOC + ^tDOW + ^tWC$ + 20 nsec	280		ns	1TTL Load
^tDS	Data Setup Time	30		ns	1TTL Load
^tDH	Data Hold Time	30		ns	1TTL Load

TABLE B-5. READ/WRITE CYCLE TIMING

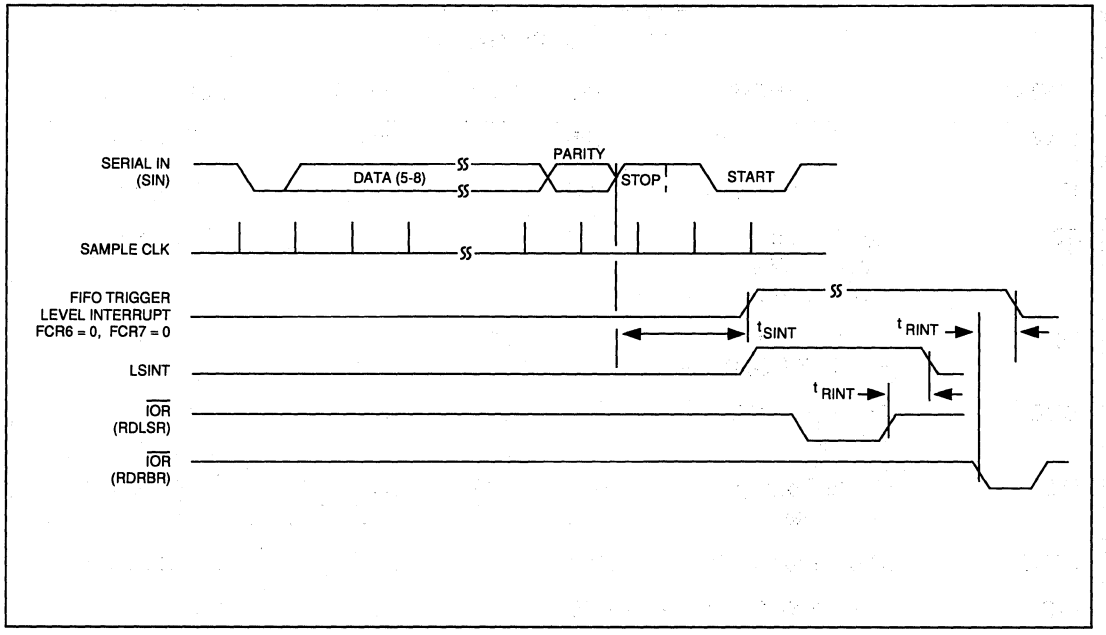


FIGURE B-6. RCVR FIFO SIGNALING TIMING FOR FIRST BYTE

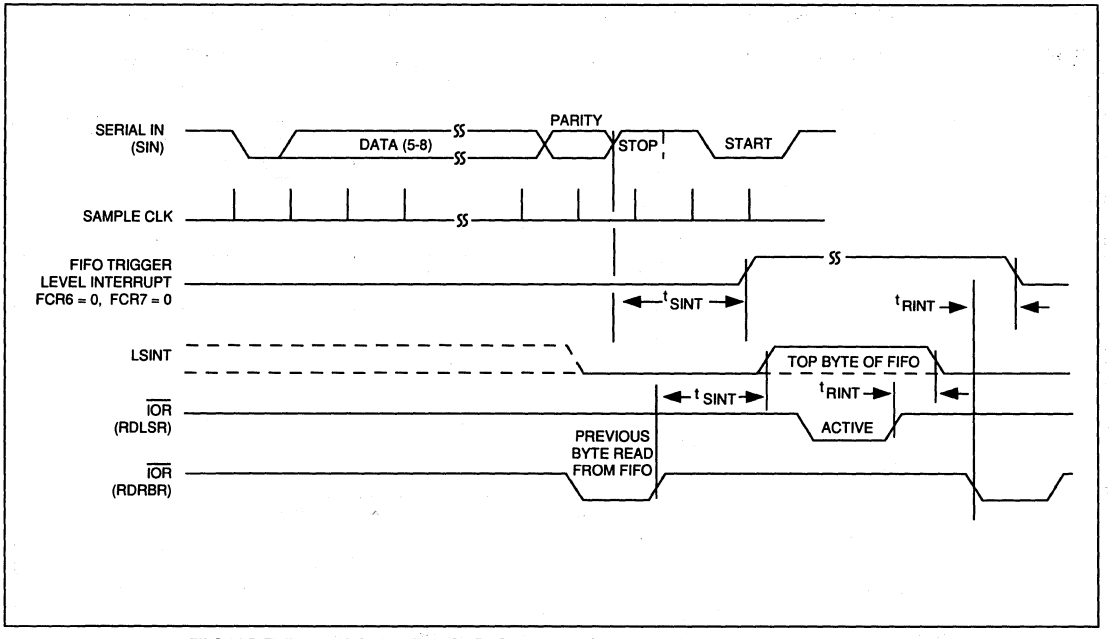


FIGURE B-7. RCVR FIFO SIGNALING TIMING AFTER FIRST BYTE (RBR Already Set)

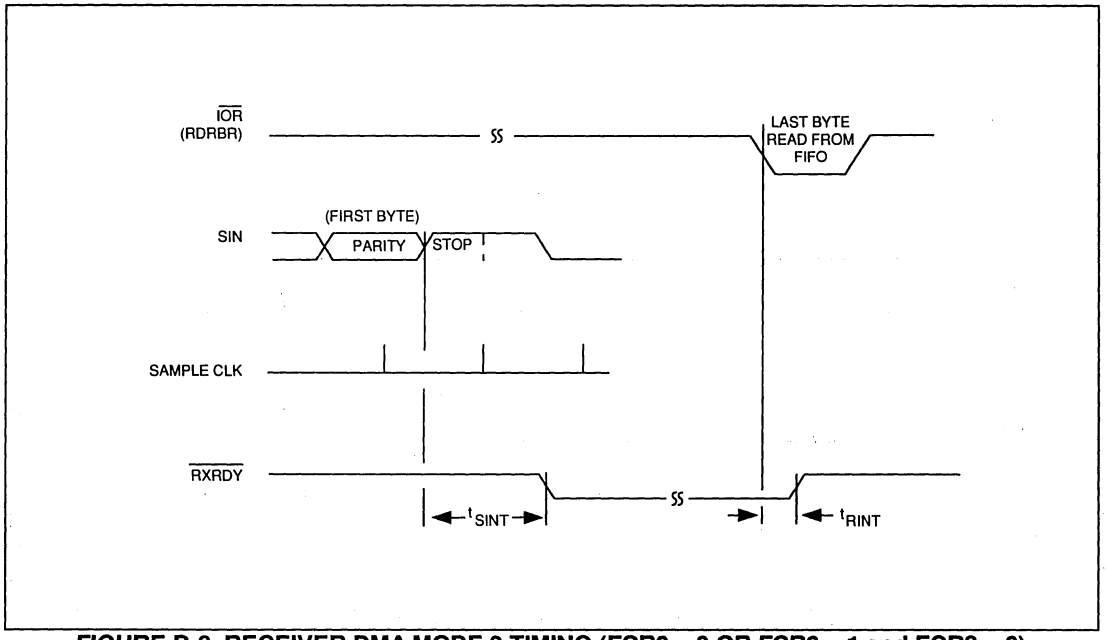


FIGURE B-8. RECEIVER DMA MODE 0 TIMING (FCR0 = 0 OR FCR0 = 1 and FCR3 = 0)

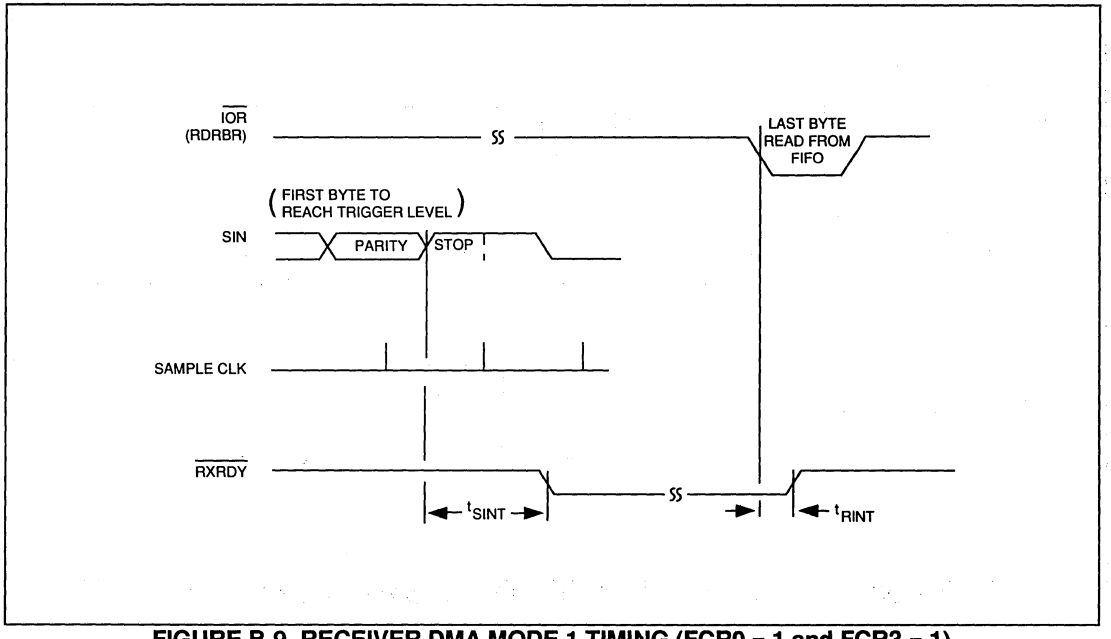


FIGURE B-9. RECEIVER DMA MODE 1 TIMING (FCR0 = 1 and FCR3 = 1)

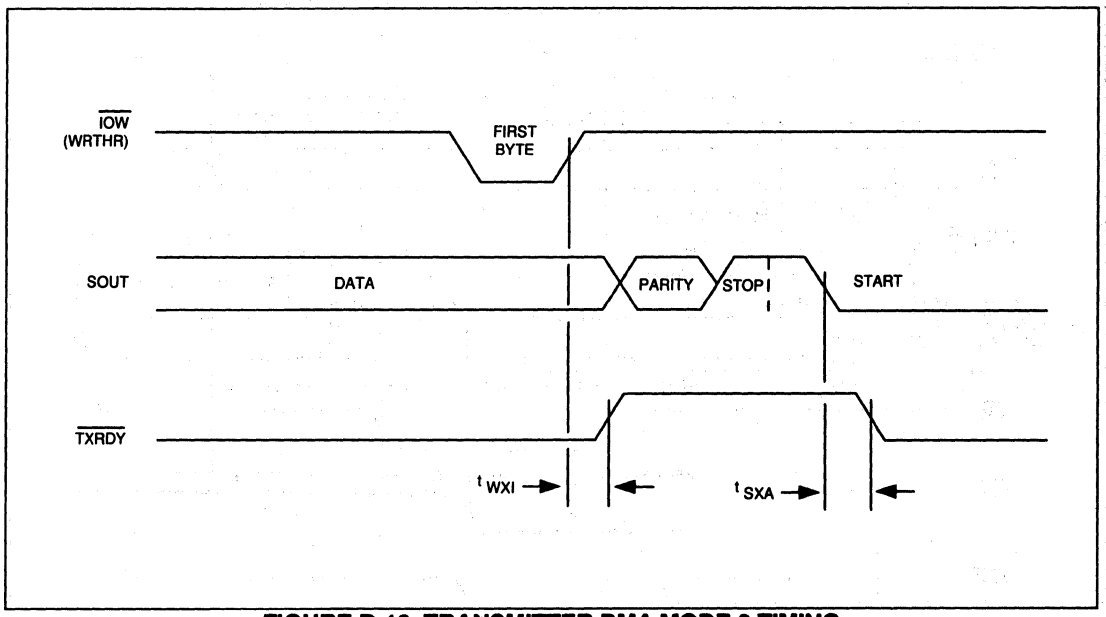


FIGURE B-10. TRANSMITTER DMA MODE 0 TIMING (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

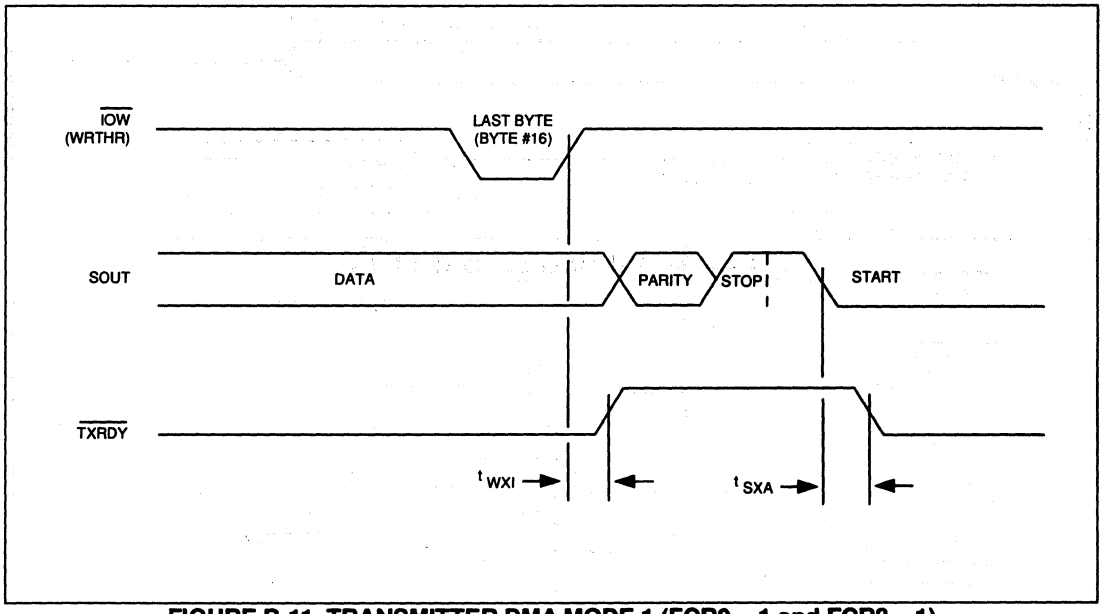
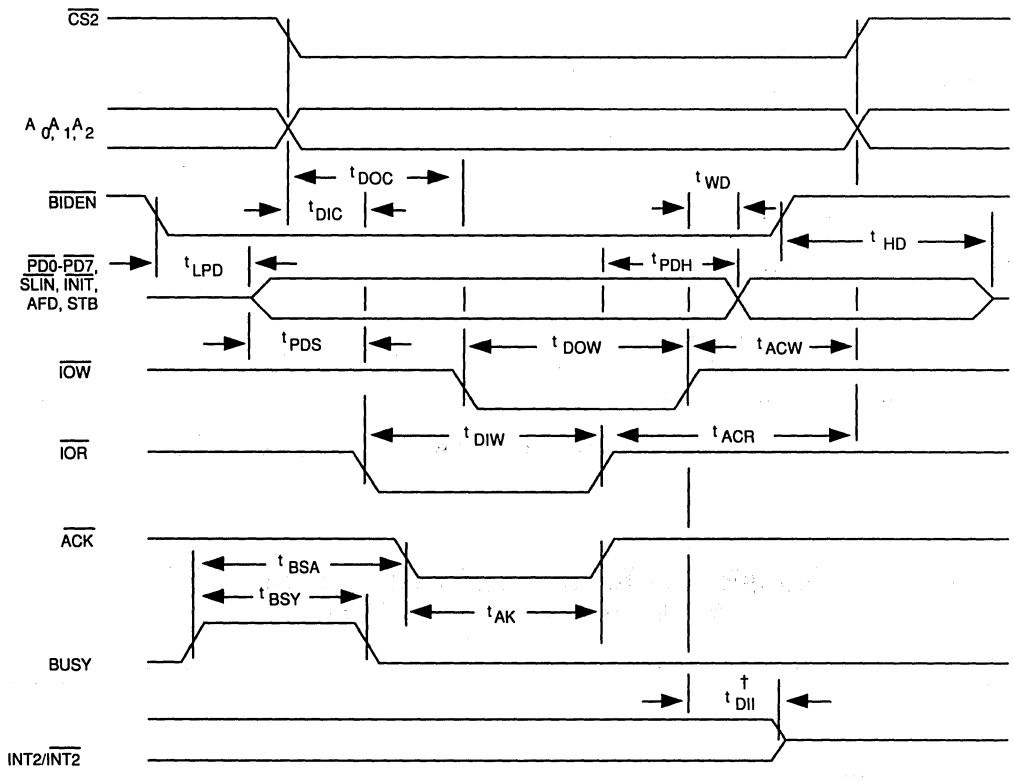


FIGURE B-11. TRANSMITTER DMA MODE 1 (FCR0 = 1 and FCR3 = 1)



† t_{DII} is the delay from the positive transition of $\overline{IOW}$ only when the Write Cycle, bit 4 of the Write Control Register (IRQ Enable Bit) is low.

FIGURE B-12. PARALLEL PORT TIMING

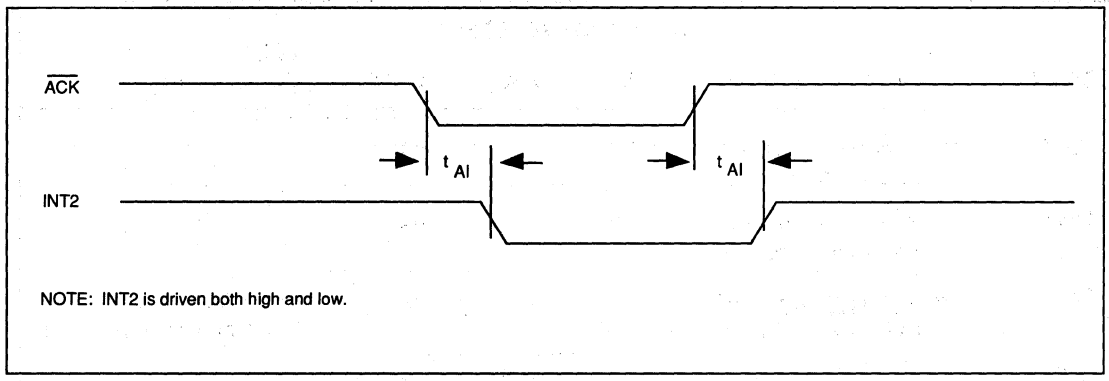


FIGURE B-13. WD16C452 PARALLEL PORT INTERRUPT TIMING

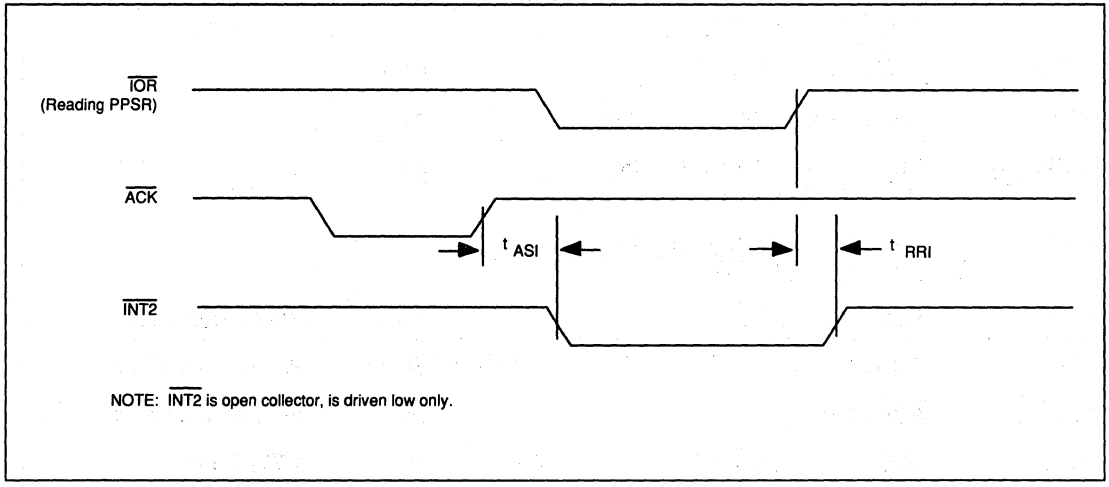


FIGURE B-14. WD16C552 PARALLEL PORT INTERRUPT TIMING

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, $\overline{SLIN}$, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF Load
t_{HD}	$\overline{BIDEN}$ High to PD0-PD7 tri-state		120	ns	
t_{LPD}	$\overline{BIDEN}$ Low to PD0-PD7 Delay		100	ns	
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$			ms	Printer Dependent
t_{BSY}	BUSY Width			µs	Printer Dependent
t_{AK}	$\overline{ACK}$ Width			µs	Printer Dependent
t_{AI}	INT2 Delay from $\overline{ACK}$ (WD16C452)		60	ns	1 TTL Load
t_{ASI}	$\overline{ACK}$ to set interrupt (WD16C552)		60	ns	1 TTL Load
t_{RRI}	Read Parallel Port Status Register (PPSR) to reset $\overline{INT2}$.		60	ns	1 TTL Load
tDII	$\overline{IOW}$ High to INT2/$\overline{INT2}$ tri-state	0	100	ns	1 TTL Load

TABLE B-6. PARALLEL PORT TIMING

APPENDIX C

C.0 PACKAGE DIAGRAM

Figure C-1 illustrates the 68-pin QUAD plastic package showing dimensions in inches.

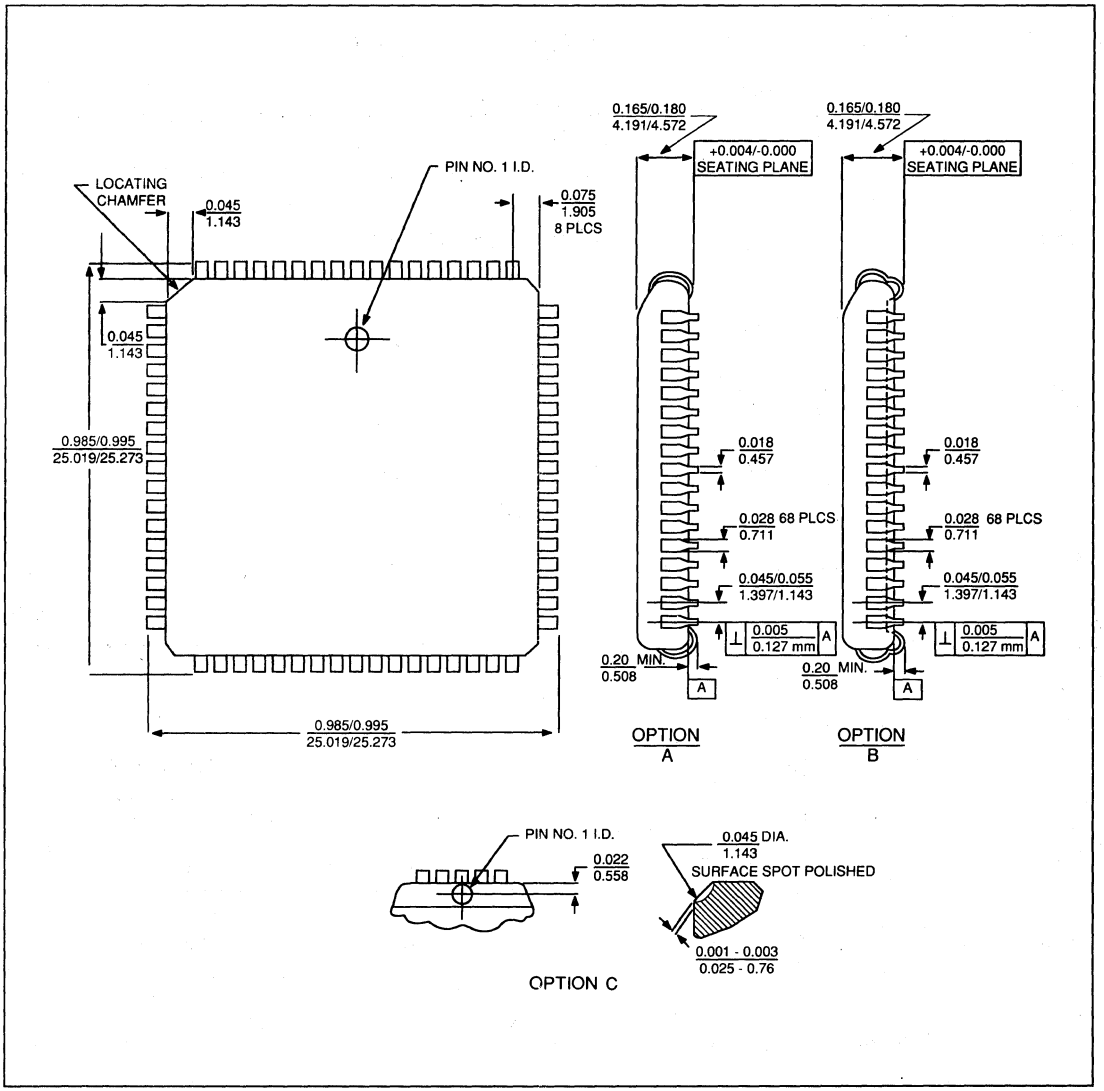
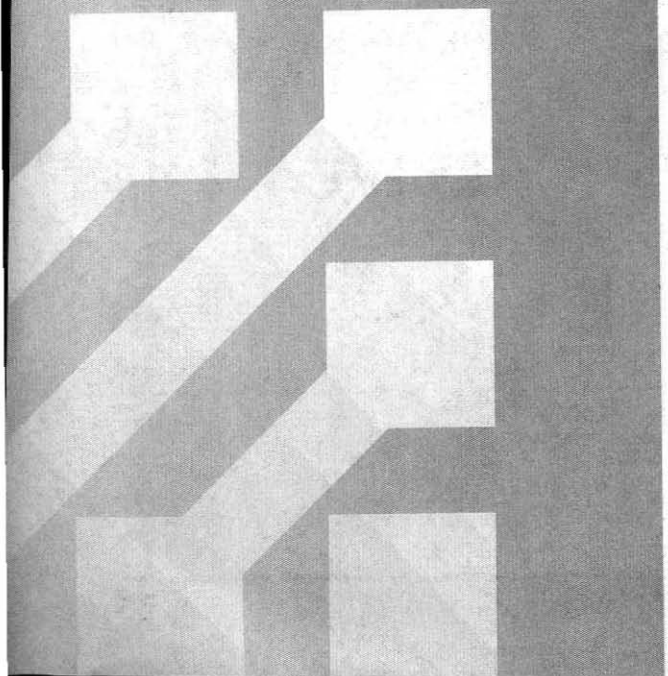


FIGURE C-1. 68-PIN QUAD PLASTIC PACKAGE

WD16C550

Enhanced Asynchronous Communications Element (ACE) with FIFOs



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LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the National NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive overhead during high data rates due to interrupts.

1.2 FEATURES

- Designed to be easily interfaced to most 8-, 16-, and 32-bit microprocessors
- Generating and stripping of serial asynchronous data control bits (start, stop, parity)
- Provides 16-byte FIFO buffers on the transmitter and receiver for CPU relief during high speed data transfer
- FIFO or Character Modes are user selectable
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16} -1) and generates the internal clock
- Independent receiver 16X clock input
- MODEM interface capabilities
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1 1/2-, or 2-stop bit generation
  - baud rate generation (dc to 512K baud)
- False start bit detector
- Complete status reporting capabilities
- Three-state TTL drive capabilities for bi-directional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communication link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Single +5 Volt power supply
- CMOS implementation for high speed and low power requirements
- Available in 40-Pin DIP and 44-Pin QUAD packages

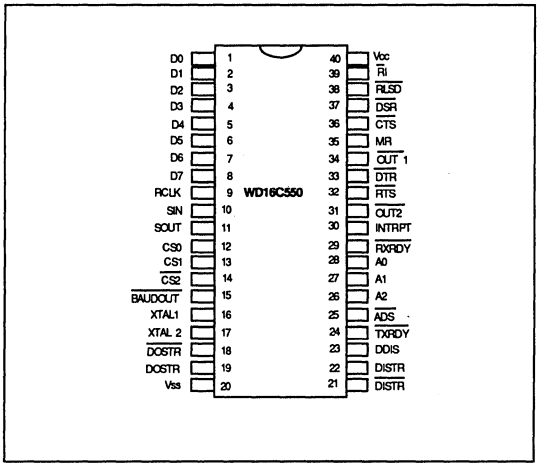


FIGURE 1-1. 40-PIN DIP

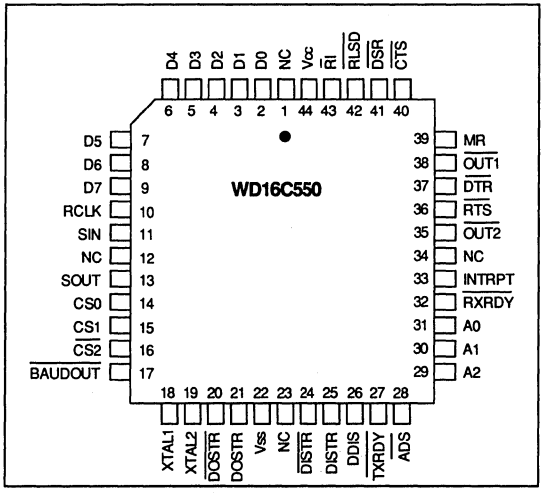


FIGURE 1-2. 44-PIN QUAD

1.3 GENERAL

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) with FIFOs (hereafter referred to as ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive interrupt overhead during high data rates.
(Refer to figure 1-1.)

In FIFO Mode, internal 16-byte FIFOs (with an additional 3 error data bits per byte in the receiver FIFO) are located on the transmitter and receiver lines. Two FIFO control pins have been added for signaling of DMA transfers.

The ACE is a software-oriented device using a three-state, 8-bit, bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format,in order of transmission and reception, is a start bit, followed by 5 to 8 data bits, a parity bit (if programmed) and 1-, 1 1/2- (5-bit format only), or 2-stop bits (all but the 5-bit format). The maximum recommended data rate is 512K baud.

Internal registers enable the user to program various types of interrupts, MODEM controls, and character formats. The user can read the status of the ACE at any time, monitoring word conditions, interrupts and MODEM status.

An additional feature of the ACE is a programmable baud rate generator capable of dividing a TTL signal clock by a divisor of 1 to $(2^{16} - 1)$.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by user's software.

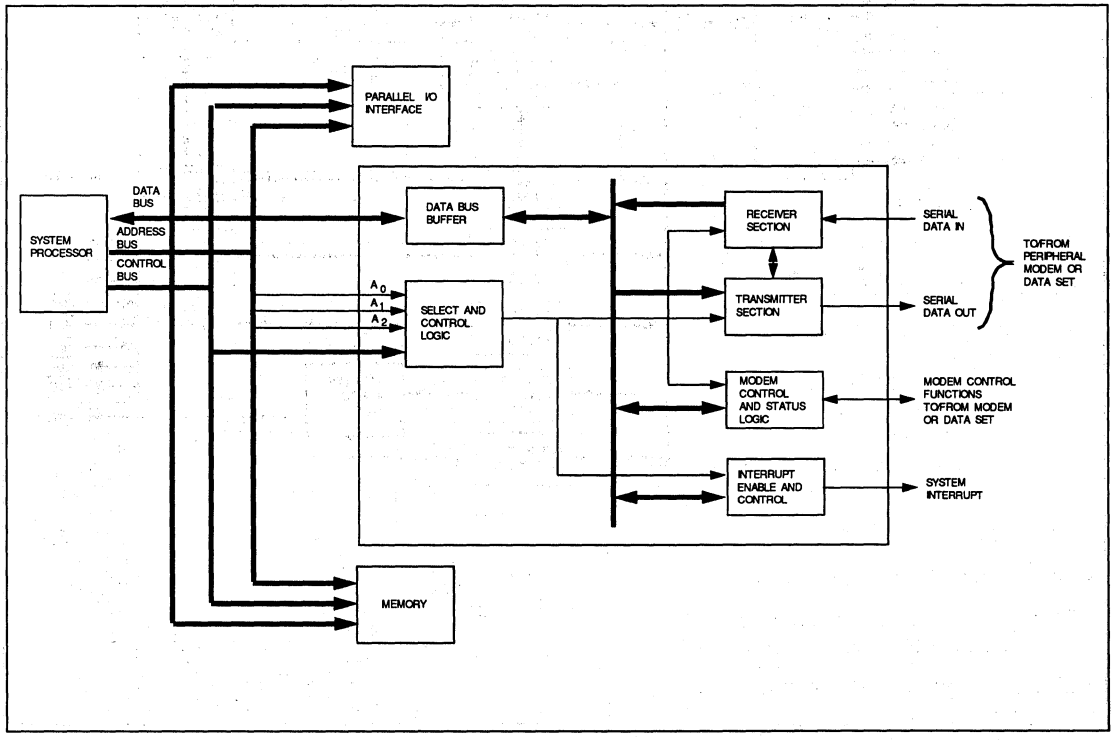


FIGURE 1-3. WD16C550 GENERAL SYSTEM CONFIGURATION

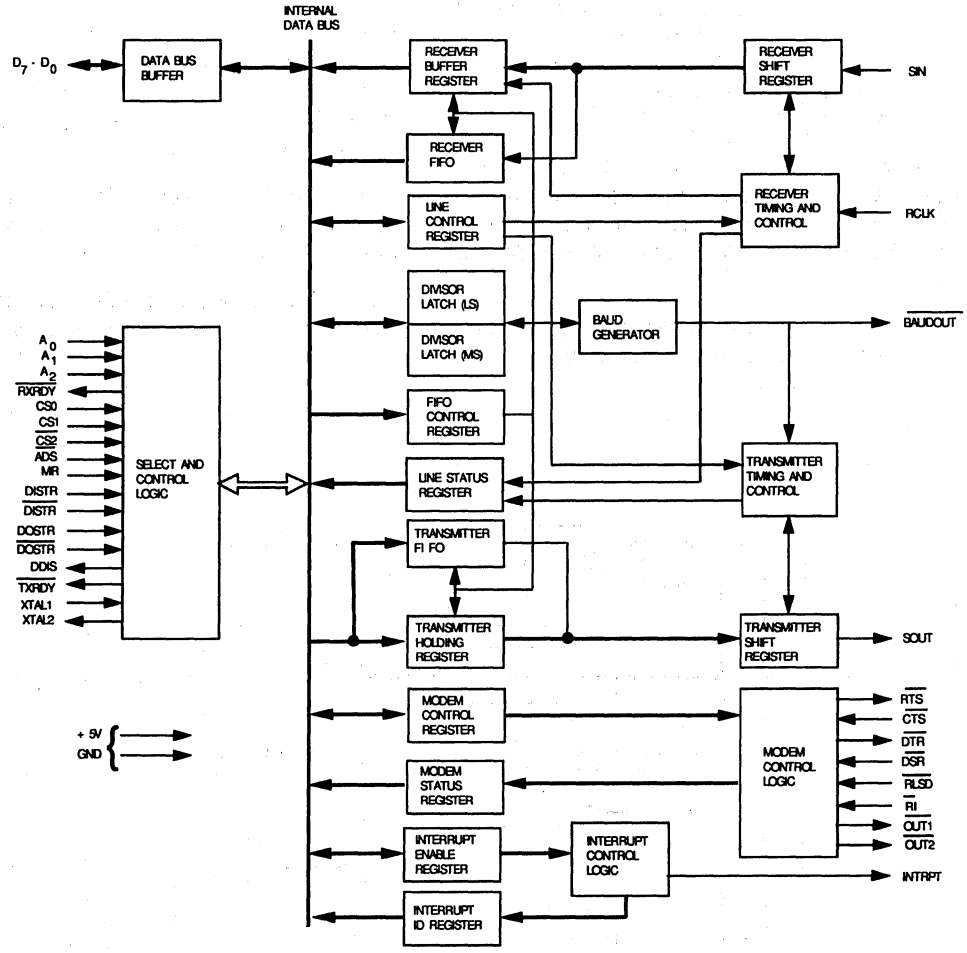


FIGURE 1-4. WD16C550 BLOCK DIAGRAM

2.0 CHIP SELECTION AND REGISTER ADDRESSING

2.1 ADDRESS STROBE ($\overline{ADS}$)

When low, provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$). (Refer to figure 1-2.)

NOTE:
The rising edge (↑) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is required for latching, this input can be tied permanently low.

2.2 CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The definition of a chip selected is CS0, CS1 both high and $\overline{CS2}$ low. Chip selection is complete when latched by ADS or $\overline{ADS}$ is tied low.

2.3 REGISTER SELECT (A0, A1, A2)

To select a register for read or write operation, see table 2-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status (read only)
X	1	1	0	MODEM Status
X	1	1	1	Scratch Pad
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2-1. REGISTER ADDRESSING

3.0 ACE OPERATIONAL DESCRIPTION

3.1 MASTER RESET

A high-level input on this pin causes the ACE to reset to the condition listed in table 3-1.

3.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in table 3-2. For individual register descriptions, refer to the following pages under register heading.

3

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 Permanent)
Interrupt Identification Register		Bit 0 is High, and Bits 1-3, 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register		All Bits Low
MODEM Control Register		All Bits Low (0-3 forced and and 4-7 Premanent)
Line Status Register		Bits 0-4 and 7 forced Low, Bits 5 and 6 forced High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 - Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)		
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either $\overline{\text{Divisor Latch}}$	Low
DDIS	DDIS = $\overline{\text{RCLK}} \bullet \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low when device is selected.)	High
INTRPT (RCVR ERRS)	Master Reset/LSR	Low
INTRPT (RCVR DATA READY)	Master Reset/Read RBR	
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$		
$\overline{\text{DTR}}$		
$\overline{\text{OUT 1}}$		
RCVR FIFO	MR or FCR1 • FCR0 or ΔFCR0	All Bits Low
XMIT FIFO	MR or FCR2 • FCR0 or ΔFCR0	

TABLE 3-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNAL

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
FIFO CONTROL	Master Reset	All Bits Low (Bits 0-3, 7 forced Low; Bits 4 and 5 Permanently Low)
D7 - D0 Data Bus Lines	In THREE-STATE Mode, Unless DISTR = HIGH or DOSTR = HIGH when device is selected	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

TABLE 3-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNAL

	REGISTER ADDRESS					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0		Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending ID Bit 0 (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1		Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2		Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3		Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)*	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4		0		Reserved	Even Parity Select (EPS)
5	Data Bit 5		0			StickParity (STP)
6	Data Bit 6		0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7		0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

* These bits are 0 in Character Mode.

TABLE 3-2. ACCESSIBLE WD16C550 REGISTERS

REGISTER ADDRESS						
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	**MODEM Control Register**	**Line Status Register**	**MODEM Status Register**	**Scratch Pad Register**	**Divisor Latch (LSB)**	**Divisor Latch (MSB)**
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0		Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1		Bit 9
2	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2		Bit 10
3	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3		Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4		Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5		Bit 13
6		Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6		Bit 14
7		Error in RCVR FIFO* (EIRF)	Received Line Signal Detect (RLSD)	Bit 7		Bit 15

* These bits are 0 in Character Mode.

TABLE 3-2. ACCESSIBLE WD16C550 REGISTERS (Continued)

3.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

See Crystal Specifications.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2*	2.860

TABLE 3-3. BAUD RATES USING 1.8432 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
5600	3*	14.285

TABLE 3-4. BAUD RATE USING 3.072 MHz CLOCK

* Smallest allowable divisor when using corresponding clock.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1*	2.344

TABLE 3-5. BAUD RATE USING 8.0 MHz CLOCK

3.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode, Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level).

When in FIFO Mode, an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator and is a read-only bit. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode, this bit is set when the XMIT FIFO is empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to table 3-2)

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

INTERRUPT IDENTIFICATION REGISTER					INTERRUPT SET AND RESET FUNCTIONS		
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT FLAG	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0		Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 3-6. INTERRUPT CONTROL FUNCTIONS

3.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the chip Interrupt (INTRPT) output signal. Its contents are indicated in table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the WD16C550. It is a read/write register that can be used by the programmer as a general purpose register.

3.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from both FIFOs. The FIFOs should be cleared before changing modes. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register is not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

4.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 3-2.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE:
The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxilliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{RTS}$, $\overline{DTR}$, $\overline{OUT2}$, $\overline{OUT1}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

5.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 3-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

NOTE:
Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to OUT1 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to OUT2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

FIFO OPERATION NOTES

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt will occur if the following is true:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

   The timeout counter uses RCLK for an input to calculate character times; therefore, this delay is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

6.0 TYPICAL APPLICATIONS

Figures 6-1 and 6-2 show how to use the ACE device in an 80286 system and in a microcomputer system with a high-capacity data bus.

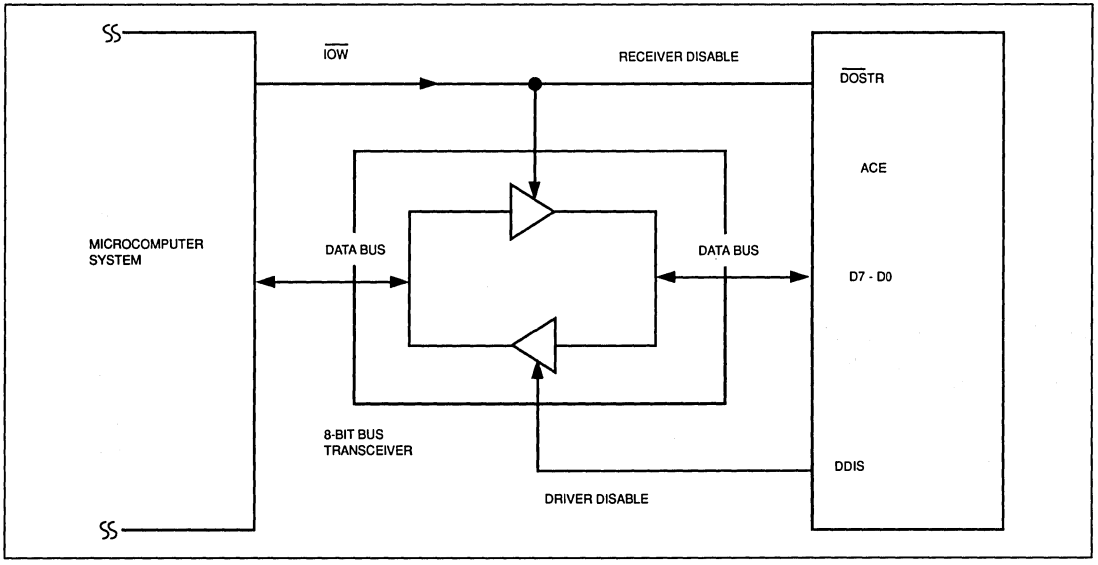


FIGURE 6-1. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

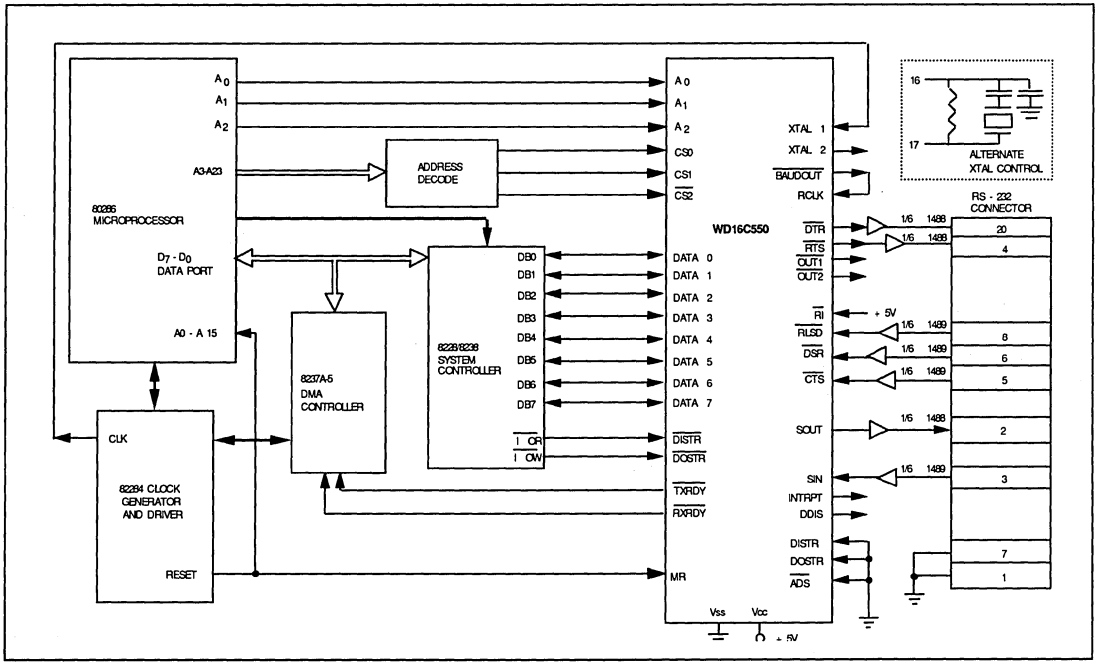


FIGURE 6-2. TYPICAL 16-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE

7.0 CRYSTAL MANUFACTURERS

American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Erie, Pennsylvania 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626

CRYSTAL SPECIFICATIONS

Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz.
Type: Microprocessor Crystal

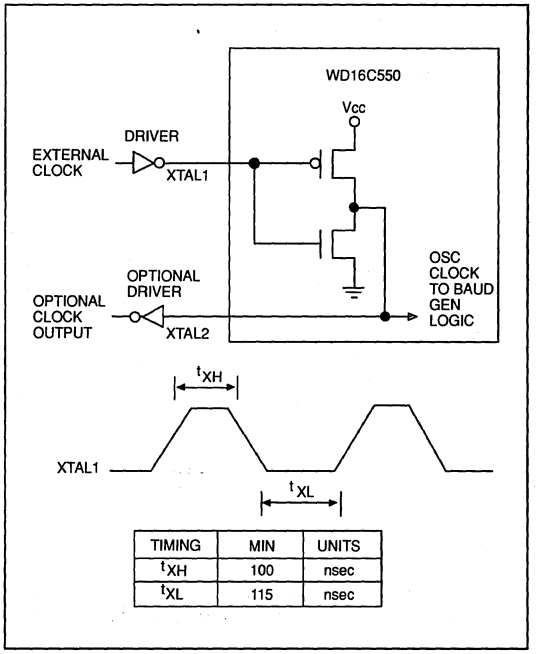
Temperature Range: 0°C(32°F) to + 70°C(158°F)

Series Resistance: 200 Ohms to 500 Ohms
(1.8432 MHz)

100 Ohms to 200 Ohms
(3.072 MHz)

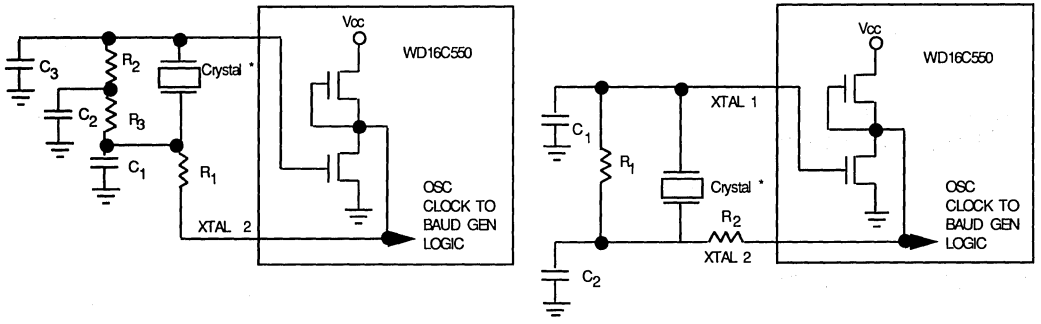
20 Ohms to 40 Ohms
(8.0 MHz)

Series Resonant
Overall Tolerance: ±0.01%



TIMING	MIN	UNITS
t_{XH}	100	nsec
t_{XL}	115	nsec

FIGURE 7-1. EXTERNAL CLOCK INPUT (8.0 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01pF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01pF	10-15pF

Crystal	R_1	R_2	C_1	C_2
8.0 MHZ	1 M?	1.68K	22pF	40pF
3.1 MHz	1 M?	1.5K	10-30pF	40-60pF
1.8 MHz	1 M?	1.0K	5-15pF	50-100pF

FIGURE 7-2. TYPICAL CRYSTAL OSCILLATOR NETWORKS

* See Crystal Specifications

APPENDIX A

A.0 PIN DESIGNATIONS

Figures A-1 and A-2 illustrate the 40-pin DIP and 44-pin QUAD assemblies. Table A-1 lists all pin designations.

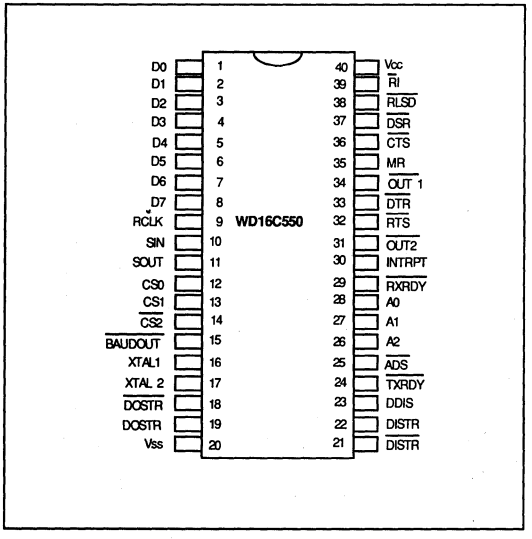


FIGURE A-1. WD16C550 40-PIN DIP ASSEMBLY PIN DESIGNATIONS

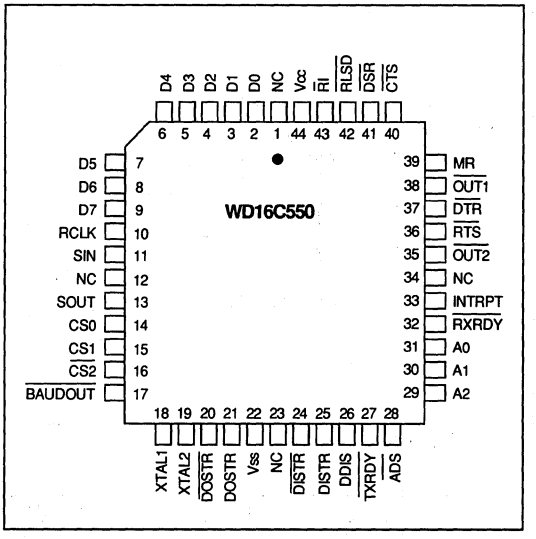


FIGURE A-2. WD16C550 44-PIN QUAD ASSEMBLY PIN DESIGNATONS

PIN DIP	PIN QUAD	MNEMONIC	DESCRIPTION
1-8	2-9	D0 - D7	**Data Bus** 3-state, bidirectional communication lines between the ACE and Data bus. All prepared TX and assembled REC data, Control characters, and Status information are transferred via the data (D0-D7).
9	1-10	NC	**No Connection** No connection.
10	11	RCLK	**Receive Clock** This input is the 16X baud rate clock for the receiver section of the chip. May be tied to BAUDOUT (pin 15 for DIP package and/or pin 17 for QUAD package).
10	11	SIN	**Serial Input** Received Serial Data In from the communications link (peripheral device, modem or data set).
-	12	NC	**No Connection** No connection.
11	13	SOUT	**Serial Output** Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12	14	CS0	**Chip Select** When CS0 and CS1 are high, and CS2 is low, chip is selected. Selection is complete when the address strobe ADS latches the chip select signals.
13	15	CS1	**Chip Select 1** Same as CS0.
14	16	$\overline{CS2}$	**$\overline{Chip\ Select\ 2}$** Same as CS0.
15	17	$\overline{BAUDOUT}$	**$\overline{BAUDOUT}$** 16X clock signal for the transmitter section of the ACE. The clock rate is equal to the oscillator frequency divided by the vidisor loaded into the divisor latches. The $\overline{BAUDOUT}$ signal may be used to clock the receiver by tying to RCLK (pin 9 for DIP package and/or pin 10 for QUAD package).

TABLE A-1. SIGNAL DESCRIPTION

PIN DIP	PIN QUAD	MNEMONIC	DESCRIPTION
16	18	XTAL1	**External Clock In** These pins connect the crystal or signal clock to the ACE baud rate divisor circuit. See Figure 7-1 and 7-2 for circuit connection diagrams.
17	19	XTAL2	**External Clock Out** Same as XTAL1.
18	20	$\overline{\text{DOSTR}}$	**Data Out Strobe** When the chip has been selected, a low $\overline{\text{DOSTR}}$ or high DOSTR will latch into the selected WD16C550 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state, DOSTR - high or DOSTR - low.
19	21	DOSTR	**Data Out Strobe** Same as $\overline{\text{DOSTR}}$.
20	22	Vxx	**Ground** System signal ground.
-	23	NC	**No Connection** No connection.
21	24	$\overline{\text{DISTR}}$	**Data In Strobe** When chip has been selected, a low $\overline{\text{DISTR}}$ or high DISTR will allow a read of the selected WD16C550 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state, DISTR - high or DISTR - low.
22	25	DISTR	**Data In Strobe** Same as $\overline{\text{DISTR}}$.
23	26	DDIS	**Driver Disable** Output goes low whenever data is being read from the ACE. Can be used to reverse data direction of external transceiver.
24	27	$\overline{\text{TXRDY}}$	**Transmit Ready** $\overline{\text{TXRDY}}$ output is used to DMA transfers. Two modes of operation are available when using FIFO mode, and one (Mode 0) is available when using character mode. Mode 0 (FCR0=0 or FCR0=1 and FCR3=0): DMA transfers are interleaved between bus cycles. In character mode with FCR3=0, $\overline{\text{TXRDY}}$ will be active (low) if there are no characters in the XMIT FIFO (FIFO mode) or Xmit Holding Register (CHAR mode). $\overline{\text{TXRDY}}$ will go inactive after the first character is loaded.

TABLE A-1. SIGNAL DESCRIPTION (Continued)

PIN DIP	PIN QUAD	MNEMONIC	DESCRIPTION
			Mode 1: Multiple DMA bursts are made until TXMT is empty or XMIT is full. In FIFO mode (FCR=1) with FCR3=1, if there is at least one unfilled position in the Xmit FIFO, TXRDY will be active (low). TXRDY will go inactive after the first character is loaded into the Xmit FIFO.
25	28	ADS	**Address Strobe** When low, provides latching for Register Select (A0,A1,A2) and Chip Select (CS0,CS1,CS2). Note: The rising edge (↑) of the ADS signal is required when the Register Select (A0,A1,A2) and the Chip Select (CS0,CS1,CS2) signals are not stable for the duration of a read or write operation. If not required, the ADS input can be tied permanently low.
26 27 28	29 30 31	A2 A1 A0	**Register Select A2** **Register Select A1** **Register Select A0** These three inputs are used to select an internal register of the ACE during a read or a write. See Table 2-1.
29	32	RXRDY	**Receiver Ready** Receiver Ready output is used to signal DMA transfers. Two modes of operation are available when using FIFO mode, and one mode (Mode 0) is available when using Character Mode. Mode 0: DMA transfers are interleaved between bus cycles. When in Character Mode (FCR0=0) or in the FIFO mode (FCR0=1), with FCR3 = 0, and there is at least 1 character in the Rcvr FIFO Register or Rcvr Holding Register, the RXRDY will be active (low). It will go inactive when the Rcvr FIFO (FIFO Mode) or Holding Register (Character Mode) is empty. Mode 1: Multiple DMA bursts are made until RCVR FIFO is empty or XMIT FIFO is full. In FIFO Mode (FCR0=1) and FCR3=1, will go active (low) when the trigger level or time out has been reached. RXRDY becomes inactive (high) when the FIFO is empty.

TABLE A-1. SIGNAL DESCRIPTION (Continued)

PIN DIP	PIN QUAD	MNEMONIC	DESCRIPTION
30	33	INTRPT	**Interrupt** Output goes high whenever an enabled interrupt is pending.
-	34	NC	**No Connection** No connection.
31	35	$\overline{Out2}$	**Output 2** User-designated output that can be programmed by Bit 3 of the Modem Control Register (Out2 goes low when Bit 3=1).
32	36	$\overline{RTS}$	**Request to Send** Output when low informs the modem or data set that the ACE is ready to transmit data. See Modem Control Register.
33	37	$\overline{DTR}$	**Data Terminal Ready** Output when low informs the modem or data set that the ACE is ready to receive data.
34	38	$\overline{Out1}$	**Output 1** User-designated output that can be programmed by Bit 2 of Modem Control Register (Out1 goes low when Bit 2=1).
35	39	MR	**Master Reset** When high, clears the registers to the states as indicated in Table 3-1.
36	40	$\overline{CTS}$	**Clear to Send** Input from DCE indicating remote device is ready to transmit data. See Modem Status Register.
37	41	$\overline{DSR}$	**Data Set Ready** Input from DCE used to indicate the status of the local data set. See Modem Status Register.
38	42	$\overline{RLSD}$	**Receiver Line Signal Detect** Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Status Register.
39	43	$\overline{RI}$	**Ring Indicator** Input when low indicates that a ringing signal is being received by the modem or data set. See Modem Status Register.
40	44	Vcc	**+5V** +5 Volt supply.

TABLE A-1. SIGNAL DESCRIPTION (Continued)

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias .....0°C (32°F) to 70°C (158°F)

Storage Temperature
Ceramic .....-65°C (-85°F) to +150°C (302°F)
Plastic .....-50°C (-58°F) to +125°C (257°F)

All Input or Output Voltages
with respect to Vss .....-0.5V to +7.0V

Power Dissipation WD16C550 .....40mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

SYMBOL	CHARACTERISTIC	WD16C550 MIN	MAX	UNITS	TEST CONDITIONS
Vil x	Clock Input Low Voltage	-0.5	0.8	V	
Vih x	Clock Input High Voltage	0.2	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 1.6mA on all outputs
Voh	Output High Voltage	2.4		V	Ioh = -100µA
Icc	(AV) Average Power Supply Current (Vcc)		8	mA	Vcc = 5.25V Ta = 25°C. No (Vcc) loads on SIN, DSR,RLSD, CTS. RI = 2.0V. All other inputs = 0.8V. Baud rate generator at 8 MHz. Baud rate at 512K.
Iil	Input Leakage		±15	uA	Vcc = 5.25V. Vss = 0V. All other pins floating.
Icl	Clock Leakage		±10	uA	Vin = 0V, 5.25V
Idl	Data Bus Leakage		±10	uA	Vout = 0.0V Vout = 5.25V Data Bus is at High-Impedance State
Vilmr	MR Schmitt Vil		0.8	V	
Vihmr	MR Schmitt Vih	2.0		V	

TABLE B-1. DC OPERATING CHARACTERISTICS
Ta = 0°C (32°F) to +70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, Unless Otherwise Specified.

SYMBOL	CHARACTERISTIC	WD16C550 TYP	MAX	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

TABLE B-2. CAPACITANCE
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

APPENDIX C

C.O AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%,

C.1 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Baud Rate Generator Timing
C-2	Receiver Timing
C-3	Transmitter Timing
C-4	MODEM Control Timing
C-5	Read Cycle Timing
C-6	Write Cycle Timing
C-7	RCVR FIFO Signaling Timing for First Byte
C-8	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-9	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-10	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-11	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-12	Transmitter DMA Mode 1 (FCR0 = 1 and FCR3 = 1)

TABLE C-1. WD16C550 TIMING DIAGRAMS

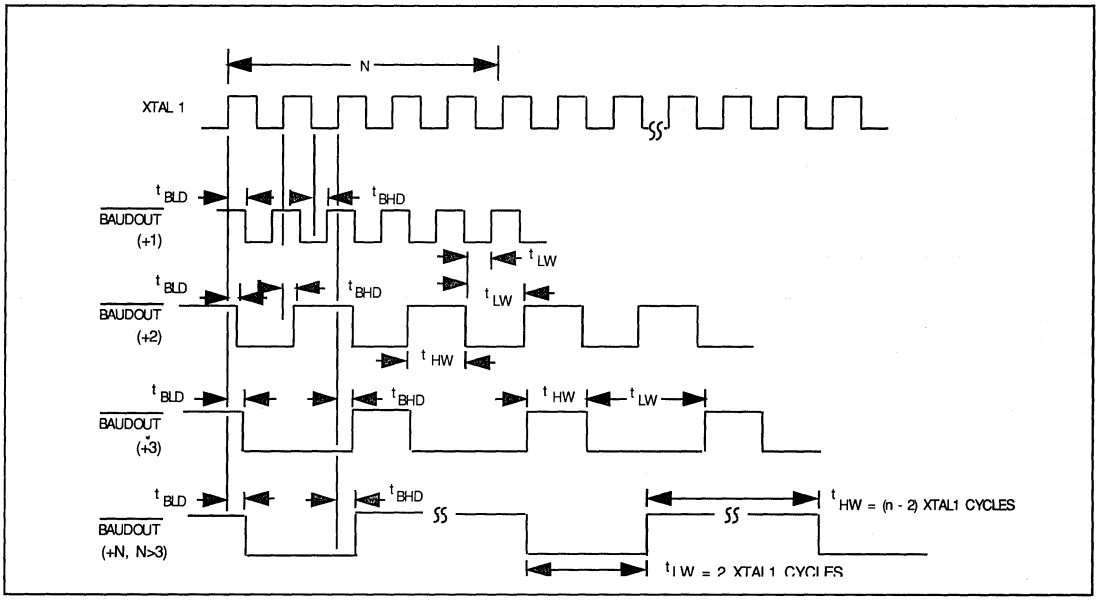


FIGURE C-1. BAUD RATE GENERATOR TIMING

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
N	Baud Rate Divisor	1	$(2^{16} - 1)$		
tBLD	Baud Output Negative Edge Delay		100	nsec	100pF Load
tBHD	Baud Output Positive Edge Delay		100	nsec	100pF Load
tLW	Baud Output Low Time	32		nsec	100pF Load (fx = 8. 0 MHz÷1)
tHW	Baud Output High Time	30		nsec	100pF Load (fx = 8. 0 MHz÷1)

TABLE C-2. BAUD RATE GENERATOR TIMING

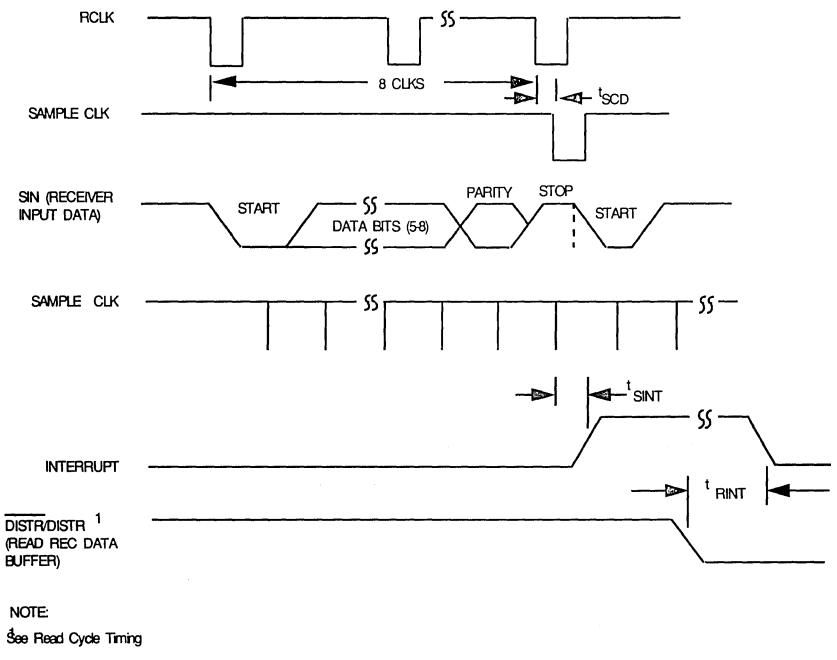


FIGURE C-2. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK to Sample Time		2	µsec	
tSINT	Delay from Stop to Set Interrupt		1*	RCLK Cycles	100pF Load
tRINT	Delay from DIST/DISTR (RD RBR) Reset Interrupt	0.250	1	µsec	100pF Load

TABLE C-3. RECEIVER TIMING

* When receiving the first byte in FIFO mode tSINT (only for timeout or trigger level interrupt) will be delayed 3 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 8 RCLK cycles.

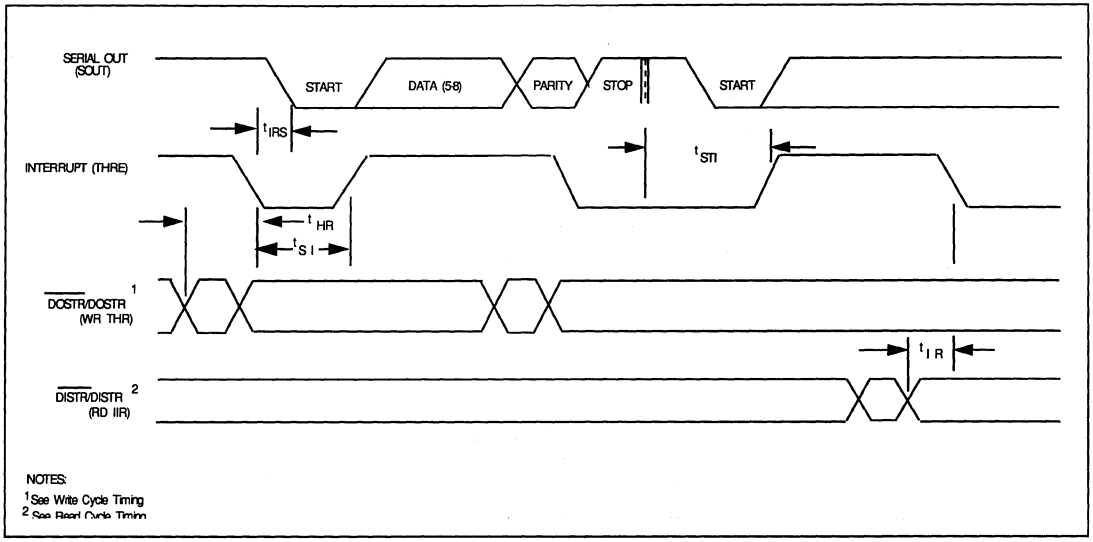


FIGURE C-3. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tHR	Delay from $\overline{\text{DOSTR}}$/ DOSTR (WR THR) to Reset Interrupt		0.175	µsec	100pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSI	Delay from Initial Write to Interrupt	16	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	$\overline{\text{BAUDOUT}}$ Cycles	
tIR	Delay from $\overline{\text{DISTR}}$/ DISTR (RD IIR to Reset Interrupt (THRE)		0.250	µsec	100pF Load
tSXA	Delay from Start to TXRDY Active	0	8	$\overline{\text{BAUDOUT}}$ Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	0.195	µsec	

TABLE C-4. TRANSMITTER TIMING

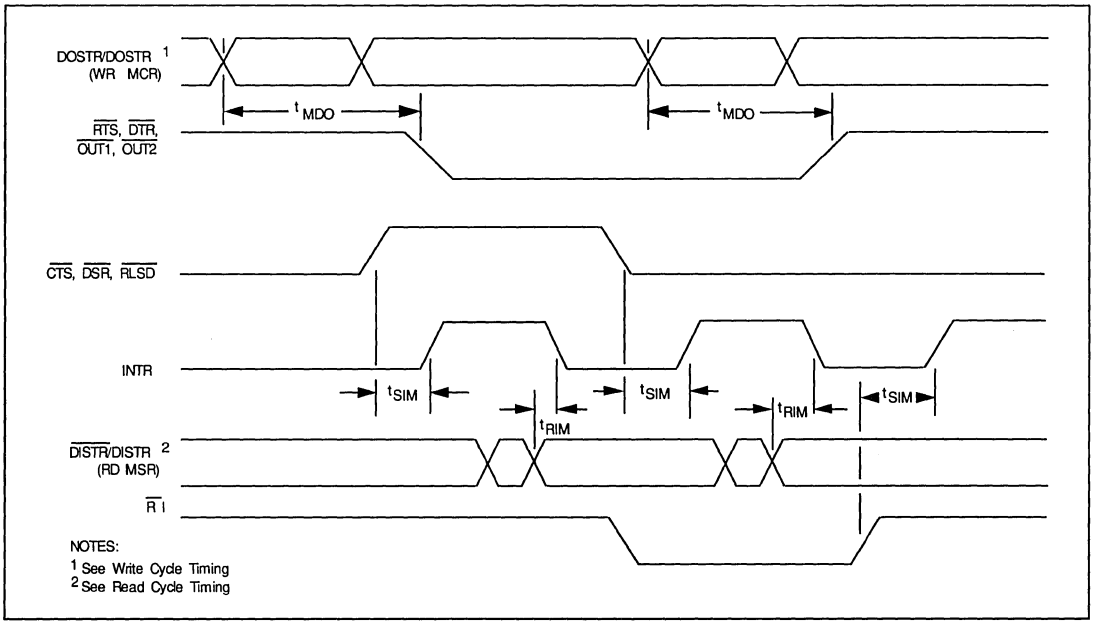


FIGURE C-4. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from DOSTR/ DOSTR (WR MCR) to Output		0.200	µsec	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		0.250	µsec	100pF Load
t_{RIM}	Delay to Reset Interrupt from DISTR/ DISTR (RD MSR)		0.250	µsec	100pF Load

TABLE C-5. MODEM CONTROL TIMING

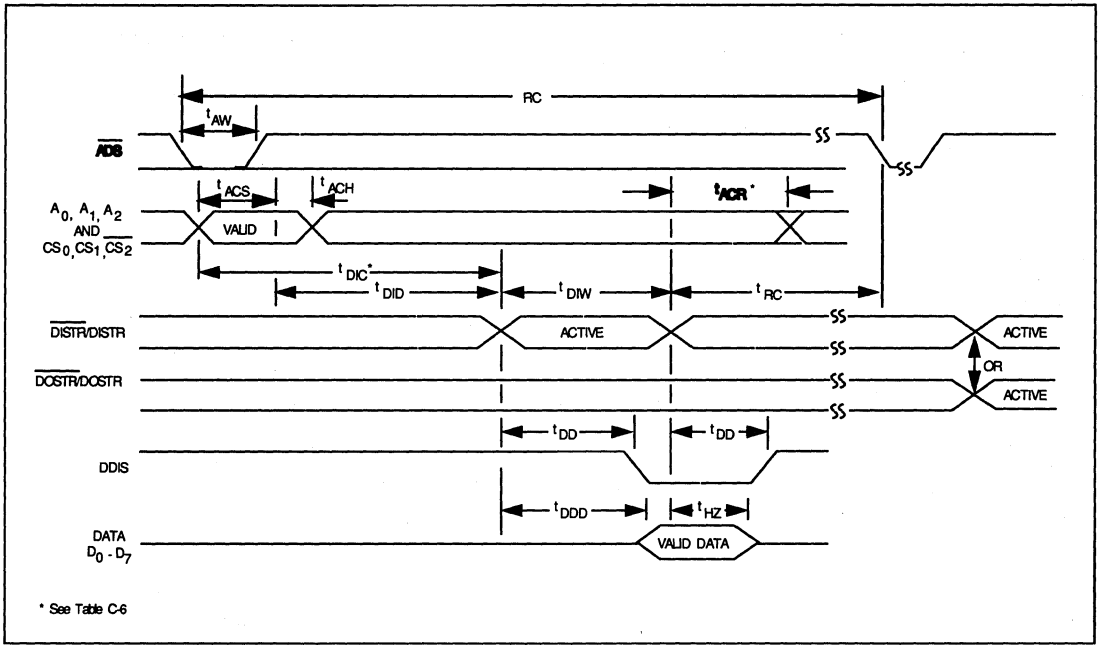


FIGURE C-5. READ CYCLE TIMING

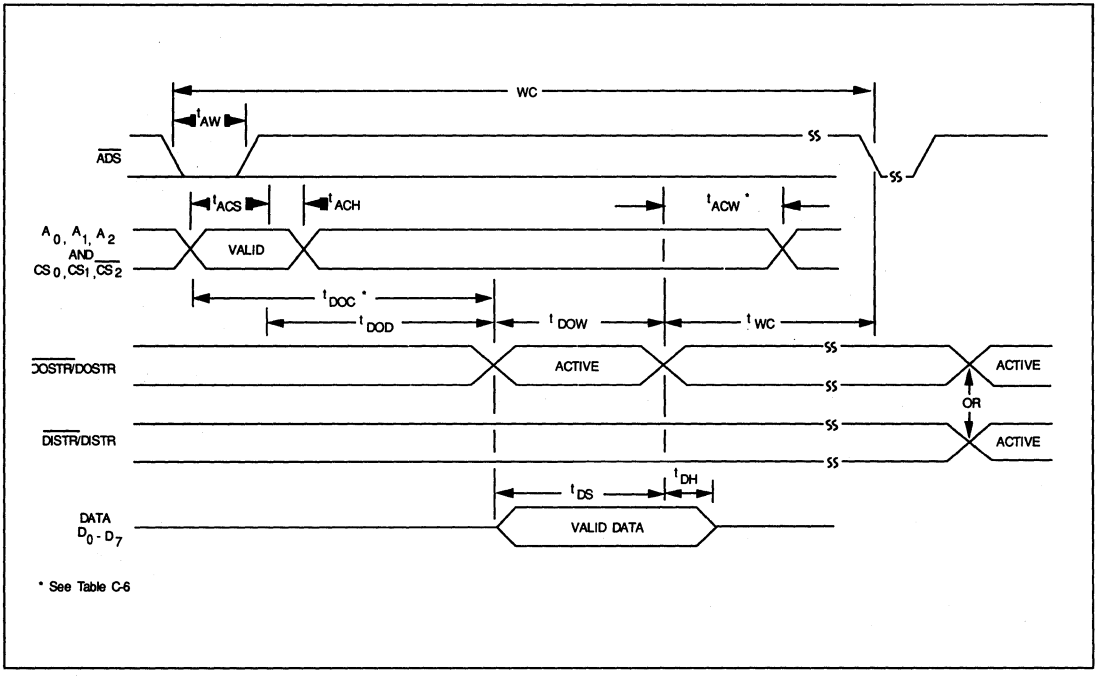


FIGURE C-6. WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Strobe Width	60		nsec	1TTL Load
t_{ACS}	Address and Chip Select Setup Time	60		nsec	1TTL Load
tACH	Address and Chip Select Hold Time	0		nsec	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from latch			nsec	1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	125		nsec	1TTL Load
t_{RC}	Read Cycle Delay	125		nsec	1TTL Load
RC	Read Cycle = tACS + tDID + tDIW + tRC + 20 nsec	280		nsec	1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay		60	nsec	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/ DISTR to Data		100	nsec	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	0	100	nsec	1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay from Latch			nsec	1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	100		nsec	1TTL Load
t_{WC}	Write Cycle Delay	150		nsec	1TTL Load
WC	Write Cycle =tACS + t_{DOD} + t_{DOW} + t_{WC} + 20 nsec	280		nsec	1TTL Load
t_{DS}	Data Setup Time	30		nsec	1TTL Load
t_{DH}	Data Hold Time	30		nsec	1TTL Load
t_{DIC}*	DISTR/DISTR DELAY from Select or Address	30		nsec	1TTL Load
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select or Address	30		nsec	1TTL Load
t_{ACR}*	Address and Chip Select Hold Time from DISTR/DISTR	20		nsec	1TTL Load
t_{ACW}*	Address and Chip Select Hold Time from DOSTR/DOSTR	20		nsec	1TTL Load
t_{MR}	Master Reset Pulse Width	5.0		µsec	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse	55		nsec	
t_{XL}	Duration of Clock LOW Pulse	55		nsec	External Clock (8.0 MHz Max.)

* Only applicable when $\overline{ADS}$ is permanently low.

TABLE C-6. READ/WRITE CYCLE TIMING

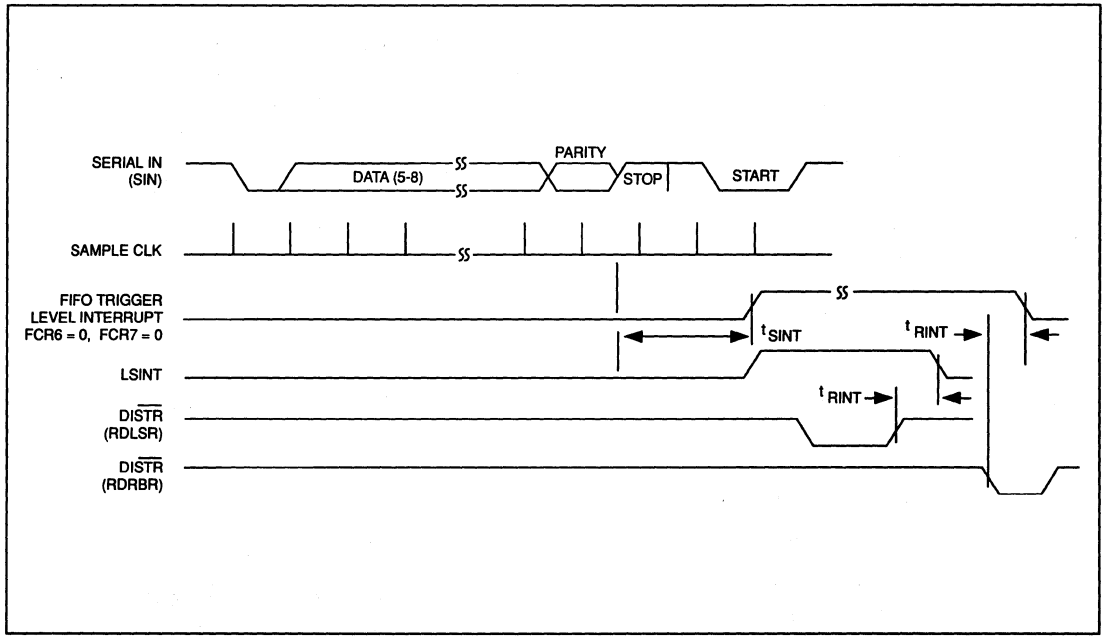


FIGURE C-7. RCVR FIFO SIGNALING TIMING FOR FIRST BYTE

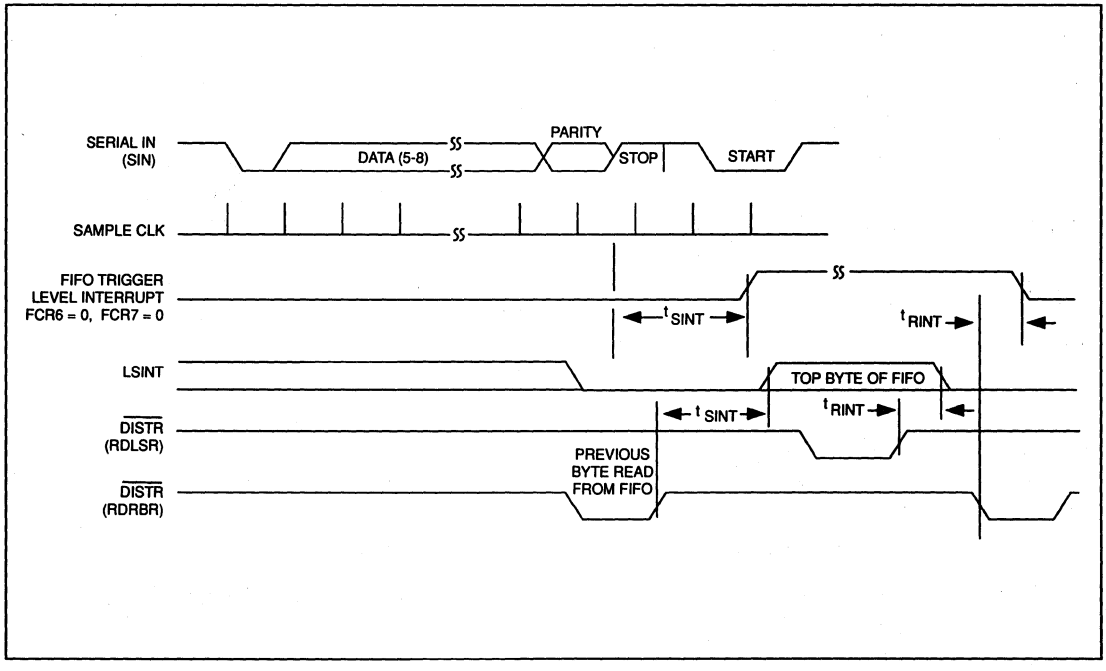


FIGURE C-8. RCVR FIFO SIGNALING TIMING AFTER FIRST BYTE

(RBR ALREADY SET)

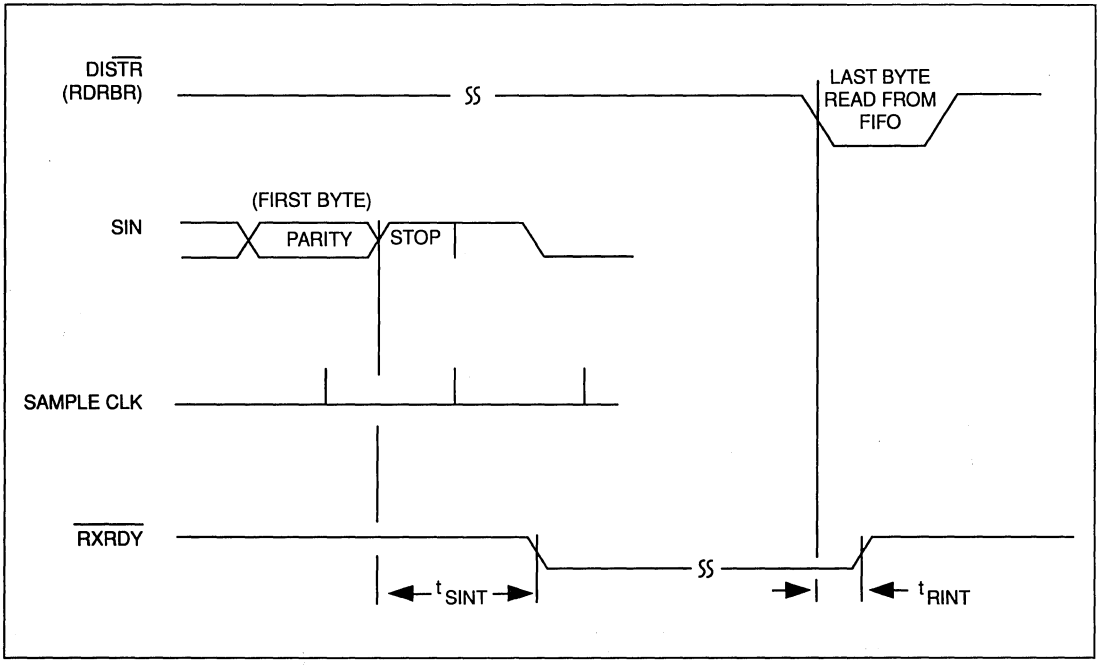


FIGURE C-9. RECEIVER DMA MODE 0 TIMING

(FCR0=0 or FCR0=1, FCR3=0)

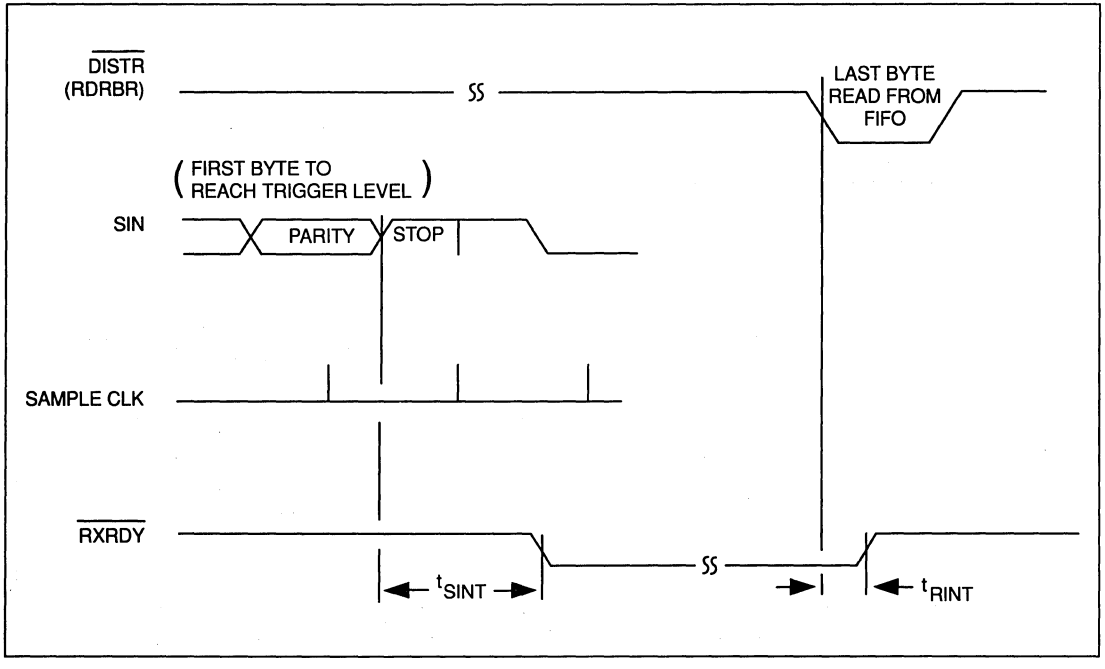


FIGURE C-10. RECEIVER DMA MODE 1 TIMING (FCR0=1 OR FCR3=1)

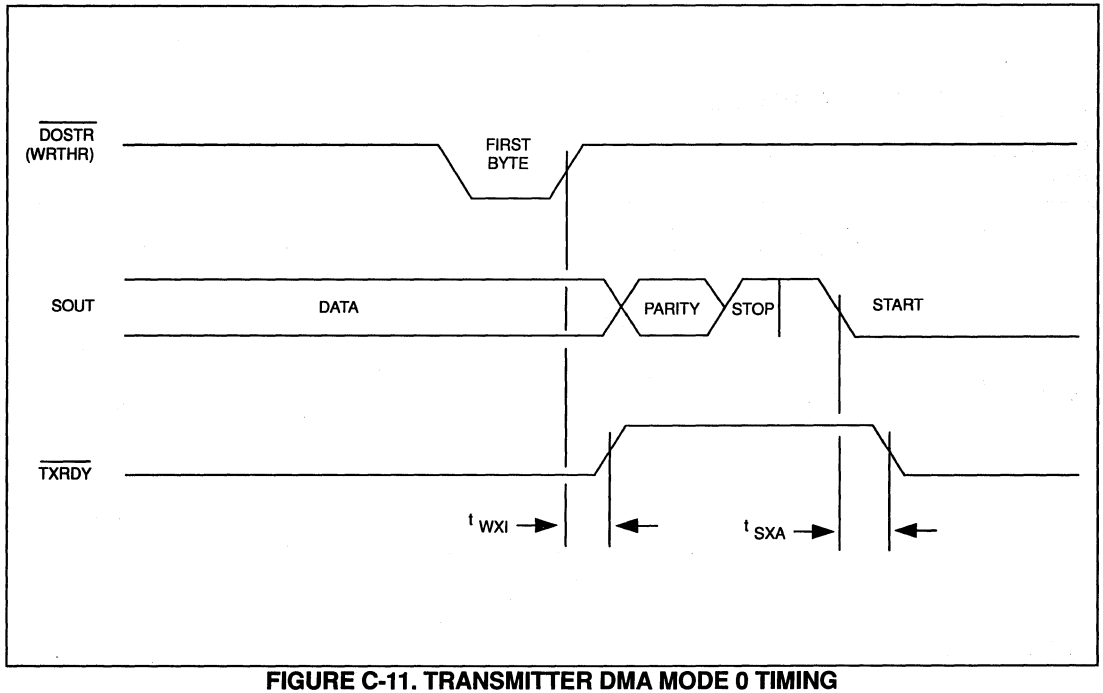


FIGURE C-11. TRANSMITTER DMA MODE 0 TIMING
(FCR0=0 or FCR0=1 and FCR3=0)

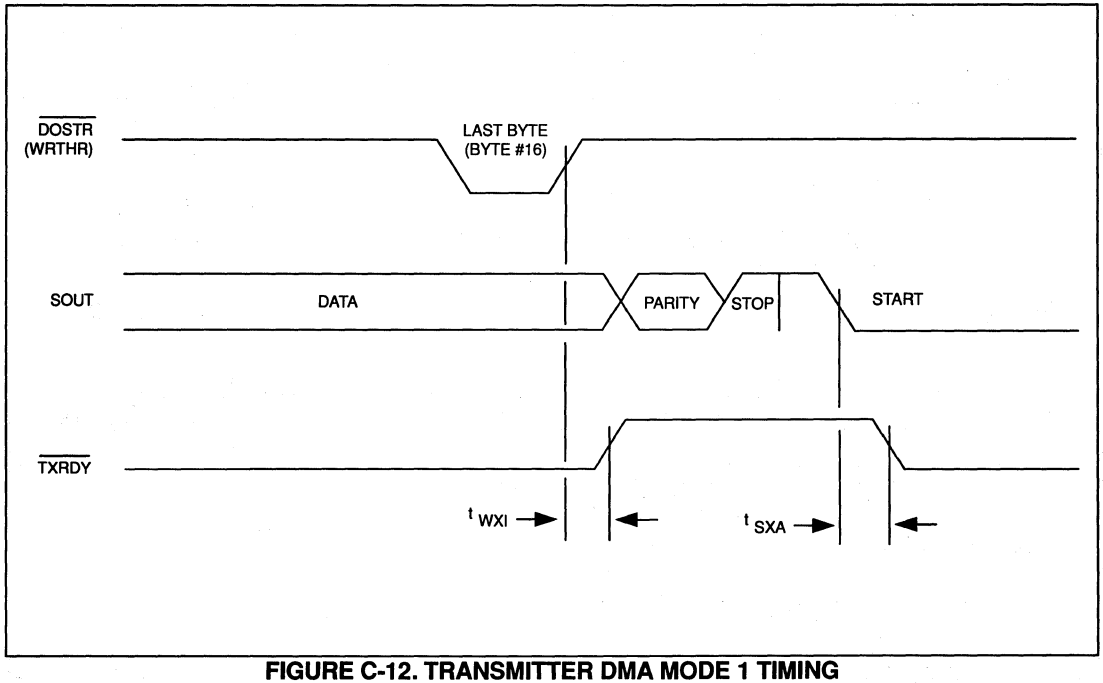


FIGURE C-12. TRANSMITTER DMA MODE 1 TIMING
(FCR0=0 or FCR0=1 and FCR3=0)

APPENDIX D

D.O PACKAGE DIAGRAMS

Figures D-1, D-2, and D-3 illustrate the 40-pin DIP packages and 44-pin QUAD package showing dimensions in inches.

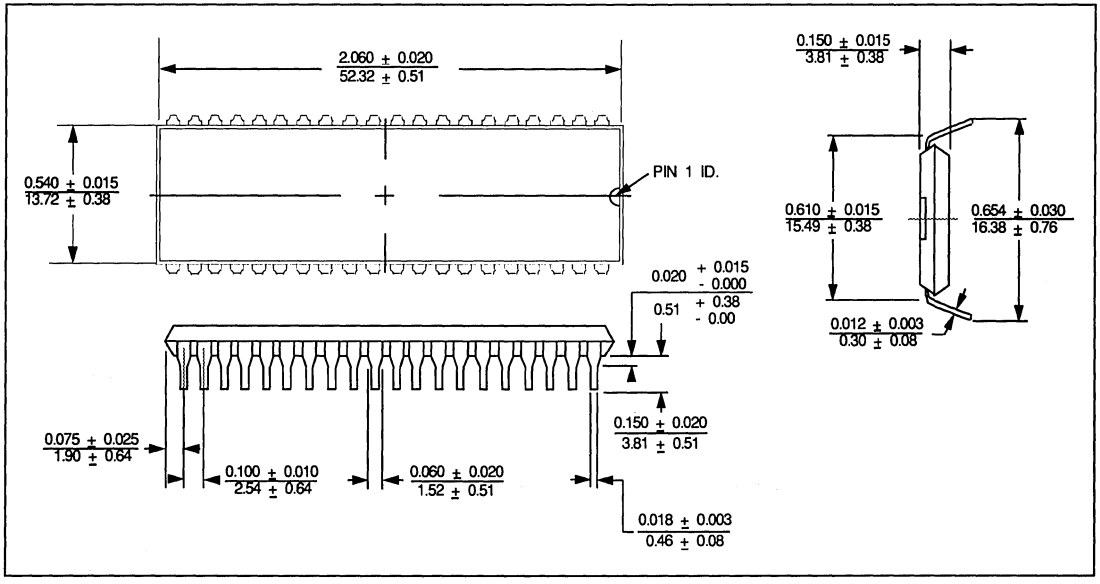


FIGURE D-1. 40-PIN LEAD PLASTIC "PL"

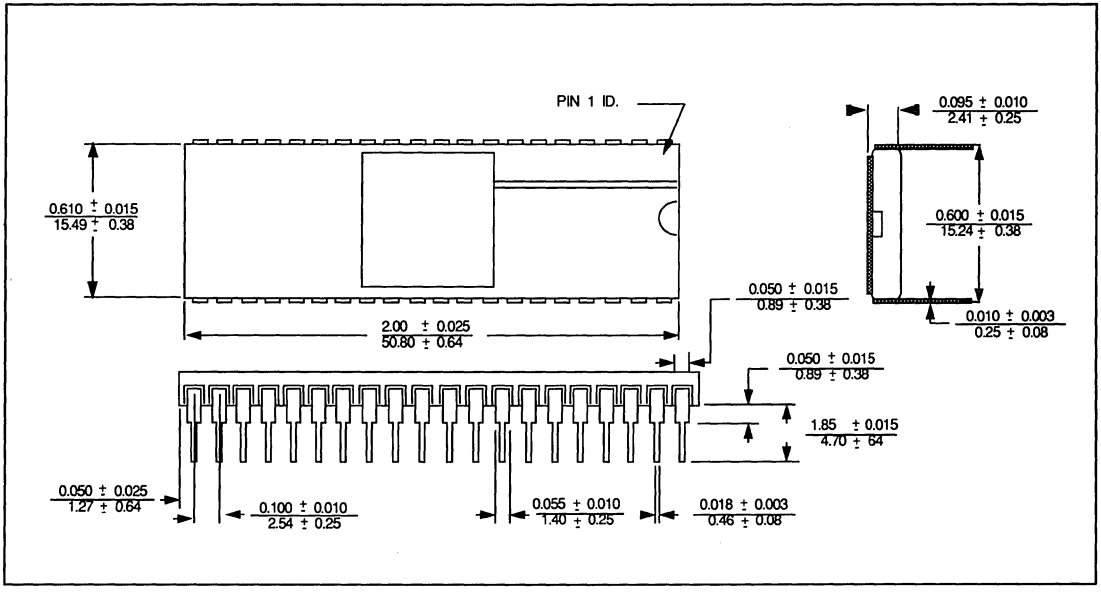


FIGURE D-2. 40-PIN LEAD CERAMIC "AL"

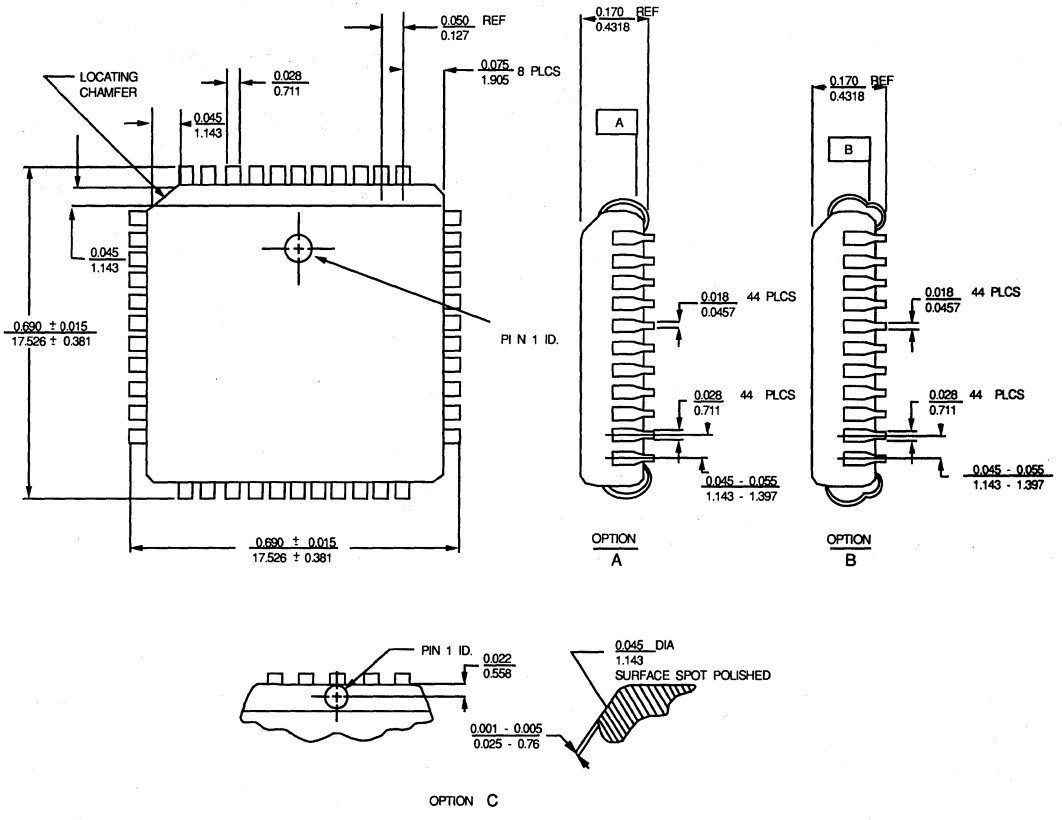


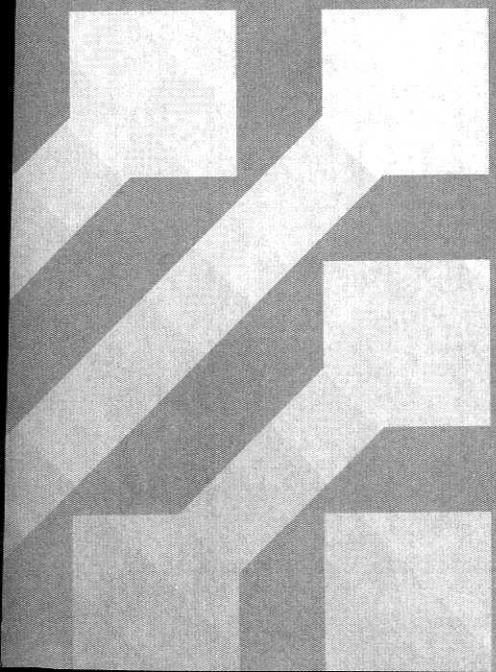
FIGURE D-3. 44-PIN QUAD LEAD PLASTIC "JM"

WD76C10A/LP/LV

ISA-Based System Controller

for 80386SX and 80286

Desktop and Portable Compatibles



WESTERN DIGITAL

TABLE OF CONTENTS

4

APPENDIX

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD76C10A, WD76C10ALP and WD76C10ALV System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances, the WD76C10A, WD76C10ALP and WD76C10ALV operate similarly and are referred to in this document as the System Controller. Where there are differences, the devices are identified specifically.

1.2 FEATURES

Features Common to WD76C10A, WD76C10ALP and WD76C10ALV:

- Operates at speeds of 16 MHz, 20 MHz and 25 MHz.
- Interfaces with 80286 or 80386SX CPUs.
- Supports memory in four banks with 64 Kbit, 256 Kbit, 1 Mbit or 4 Mbit DRAMs.
- Page mode zero wait state access at 25 MHz with 70 ns DRAM.
- Supports up to 16 Mbyte of real memory or 32 Mbyte of EMS memory.
- Maintains controlled propagation delay for 80386SX reset.
- Employs an internal self-tuning delay line for DRAM control.
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise.
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and VGA BIOS may be mapped into one physical PROM.
- Advanced 64 Kbyte and 128 Kbyte ROM shadowing allows main BIOS and video BIOS shadowing, along with 320 Kbyte and 256 Kbyte remap to extended or expanded memory.
- Parity generation and checking.
- Low power 0.9 micron CMOS technology.
- 132-pin JEDEC plastic QUAD flat package (PQFP)

Additional Features Of WD76C10ALP Only:

- System Activity Monitor (SAM).
- Power control with suspend and resume.
- Processor stop clock.
- CAS before RAS slow refresh for portable applications.
- Automatic processor clock speed switching.

Additional Features Of WD76C10ALV Only:

- Internal logic is powered by a 3.3 volt supply to extend battery life upto two times.

1.3 GENERAL DESCRIPTION

The WD76C10A is designed for use in a high performance desktop AT computer, using an 80286 or 80386SX processor of up to 25 MHz. The WD76C10ALP has the features of the WD76C10A and is designed to operate in a high performance notebook/laptop AT compatible computer using an 80286 or 80386SX processor. With the exception of the 80286 modes, the WD76C10ALV has all the capabilities of the WD76C10ALP plus the ability to operate with a 3.3 volt power supply.

1.3.1 WD76C10A

The WD76C10A contains a high performance memory controller with programmable modes of operation. It supports non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, 1 Mbit or 4 Mbit DRAM may be controlled, allowing up to 16 Mbytes of real or 32 Mbytes EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used. In addition, the WD76C10A controls page mode DRAM or static column DRAM with page mode operation.

The on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line infor-

mation is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

The WD76C10A interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.2 WD76C10ALP

In addition to supporting all the features of the WD76C10A, the WD76C10ALP also supports portable notebook/laptop computers. To provide this support, the WD76C10ALP makes use of Power Management Control (PMC) for powering down peripherals or the processor, processor stop clock, slow clock, automatic processor clock speed switching modes and CAS before RAS slow refresh. Suspend and resume is supported when low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 5 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

The System Activity Monitor (SAM) provided by WD76C10ALP is a transparent feature that replaces the functions previously performed by software. It determines when the system has been idle for a previously programmed period of time and determines a clean break point in which to perform power down activities such as suspend.

1.3.3 WD76C10ALV

The WD76C10ALV supports all of the 80386SX mode functions and features supplied by the WD76C10ALP. In addition, the WD76C10ALV has improved the PC notebook/laptop design by operating with a 3.3 volt ± 0.3V power supply which extends the battery life up to two times.

The WD76C10ALV does not support 80286 modes.

The DC operating Characteristics and AC timing specifications that differ from the WD76C10A/LP are presented in the Appendix.

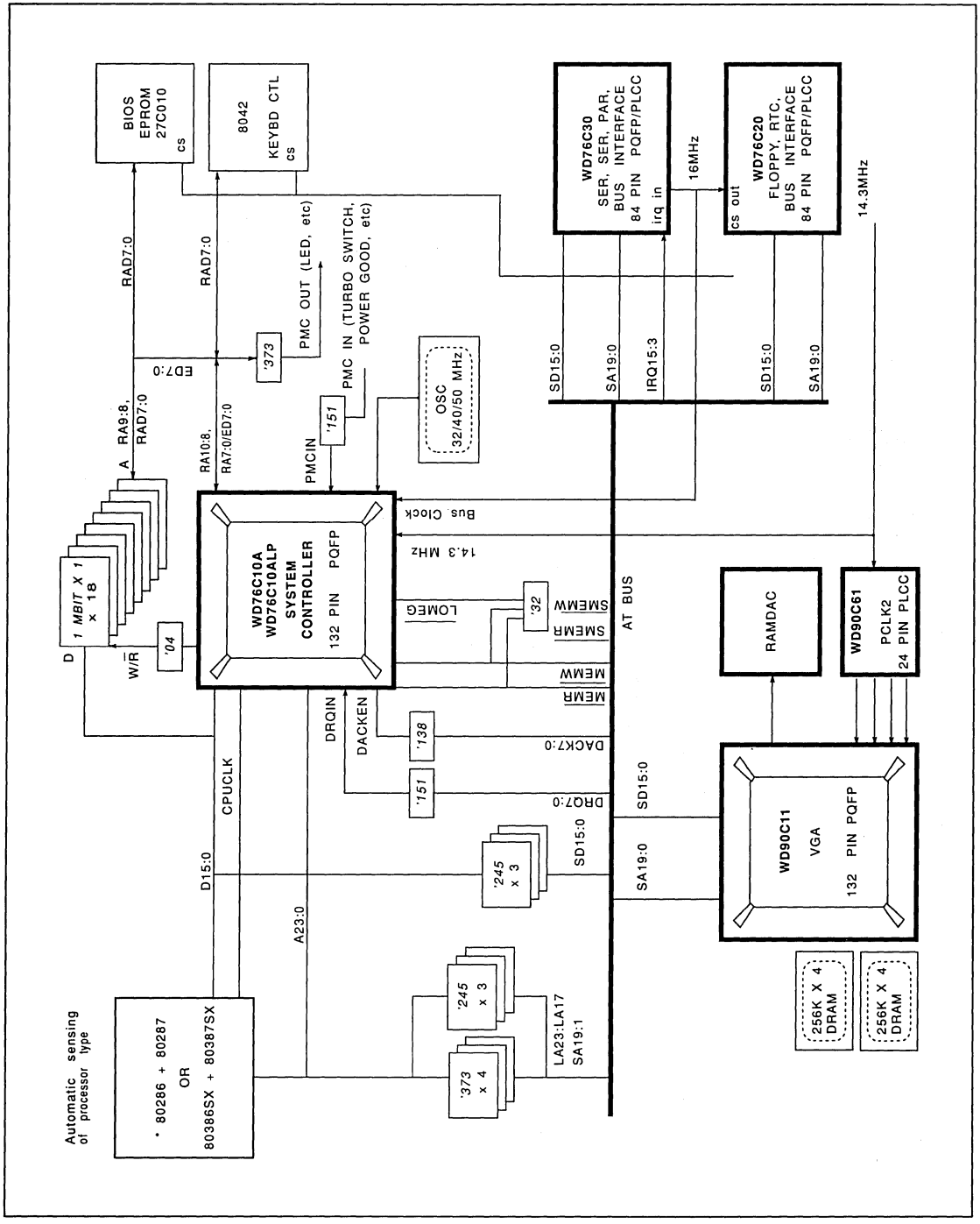


FIGURE 1-1. SYSTEM BLOCK DIAGRAM

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control (WD76C10ALP only)
- Register File

Sections 2.1 through 2.8 provide an overview of these blocks and are described in more detail in sections 4 through 9.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal, which it uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal. It is at this time that the type of processor in use (80286, 80287 or 80386SX, 80387SX) is determined by examining the S1[W/R#] signal.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the S1[W/R#] signal. This block also controls whether the CPUCLK is to be an input or output. While both devices have the ability to reduce the processor clock rate, only the WD76C10ALP has the ability to stop the clock to the processor. The WD76C10ALP also has the ability to power down the processor, at which time it tristates signals CPUCLK, READY, HOLD, INTRQ and NMI.

2.4 NUMERIC PROCESSOR CONTROL

Both System Controllers support an 80287 or 80387SX processor.

2.5 DATA BUS

The Data Bus is a 16 bit (two bytes) bidirectional bus that connects to the processor's, System Controller, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory. Both versions of the System Controller supports non-page mode memory and independent two-way interleave page mode access to the DRAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD76C10ALP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD76C10ALP tristates the CPUCLK, READY, HOLD, INTRQ and NMI output signals to the main processor.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port 1872H, serve more than one area. In this instance the register description appears only in one section but is referred to in all appropriate sections.

The registers, and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072H and E872H and Port 70H Shadow Register at E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72H - Read only

Bits 11-03 are particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
T				DMA #2 CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1 CH3	CH2	CH1	CH0	P			

Signal Name	Default At RSTIN
All signals	None

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bit 03 - P, Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, section 4.3

Bits 02-00 - Not used, state is ignored

2.8.2 Lock/Unlock Register

Port Address F073H - Write only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
L/UL							

Signal Name	Default At RSTIN
All signals	None

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -
11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -
Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

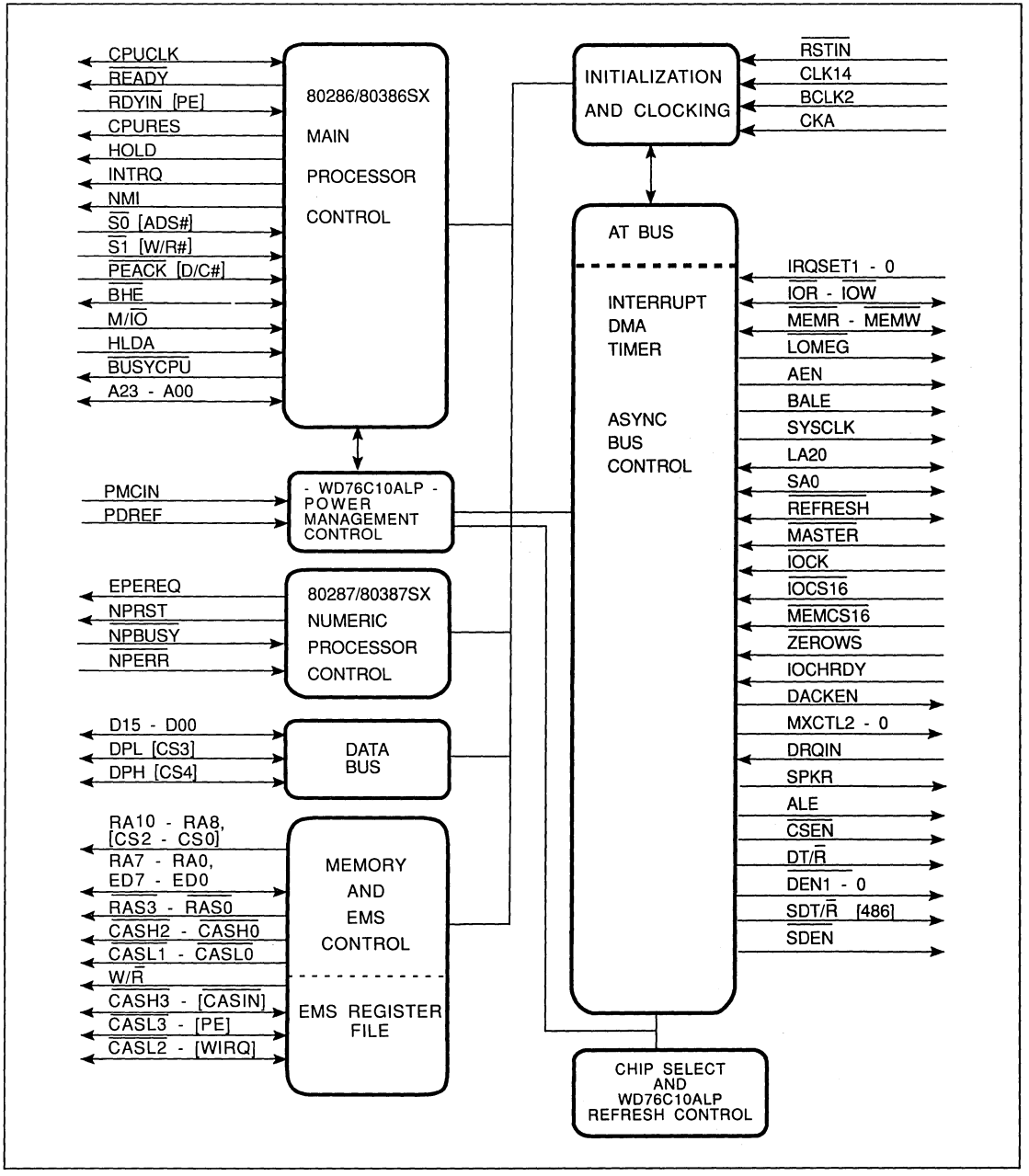


FIGURE 2-1. WD76C10A/LP/LV BLOCK DIAGRAM

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	7.5, Table 7-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real-Time Clock Address Register	No	5.8.1
071 - 07F odd	Real-Time Clock Data Register	No	5.8.2
080 - 09F	(except 092H) DMA Page Registers	No	5.6.4
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	CLEAR 287 BUSY	No	5.3.2
00F1	RESET 287/387SX	No	5.3.3
1072	CPU Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	7.1
2872	Chip Selects	Yes	7.2
3072	Programmable Chip Select Address	Yes	7.3
3872	Memory Control	Yes	6.2.1
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
6072	RAM Shadow And Write Protect	Yes	6.2.4
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
7072	PMC Output Control 7:0	Yes	8.3
7872	PMC Output Control 15:8	Yes	8.3
8072	PMC Timers	Yes	8.4
8872	PMC Inputs 7:0	Yes	8.5
9072	NMI Status	Yes	8.7
9872	Diagnostic	Yes	9.1
A072	Delay Line	Yes	9.2
A872	Test Enable	Yes	9.3
B072	Activity Monitor Control	Yes	8.11
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	8.6
D072	Serial/Parallel Shadow Register	Yes	8.8
D472	Interrupt Controller Shadow	Yes	8.9
D872	Activity Monitor Mask	Yes	8.12
DC72	Test Status	Yes	9.4
E072	EMS Page Register Pointer	No	6.4.2
E472	Port 70H Shadow	No	8.10

TABLE 2-1. REGISTER INDEX

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	7.5, Table 7-1
F472	48 MHz Oscillator Enable	Yes	7.5, Table 7-1
F872	Cache Flush	Yes	7.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	No	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX (cont.)

3.0 SIGNAL DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - RA5/ED5	35 - NPRST	68 - D11	102 - A9
2 - Vcc	36 - LOMEG	69 - Vcc	103 - A8
3 - RA4/ED4	37 - MEMW	70 - D12	104 - A7
4 - RA3/ED3	38 - MEMR	71 - D13	105 - A6
5 - Vss	39 - IOW	72 - D14	106 - A5
6 - RA2/ED2	40 - IOR	73 - D15	107 - A4
7 - RA1/ED1	41 - BHE	74 - DT/R	108 - A3
8 - RA0/ED0	42 - NPERR	75 - DEN1	109 - A2
9 - CASH2	43 - PEACK [D/C#]	76 - DEN0	110 - IRQSET1
10 - CASL2 [WIRQ]	44 - M/IO	77 - SYSCLK	111 - IRQSET0
11 - RAS2	45 - S0 [ADS#]	78 - CPURES	112 - MXCTL0
12 - CASH3 [CASIN]	46 - S1 [W/R#]	79 - BALE	113 - MXCTL1
13 - CASL3 [PE]	47 - READY	80 - A23	114 - MXCTL2
14 - RAS3	48 - HLDA	81 - A22	115 - CSEN
15 - DPH [CS4]	49 - HOLD	82 - A21	116 - DACKEN
16 - DPL [CS3]	50 - BCLK2	83 - IOCK	117 - PDREF - WD76C10ALP
17 - RSTIN	51 - RDYIN [CKA] [PE]	84 - CLK14	118 - PMCIN
18 - DRQIN	52 - CPUCLK	85 - NPBUSY	119 - W/R
19 - IOCHRDY	53 - BUSYCPU	86 - A0 [BLE#]	120 - CASH0
20 - ZEROWS	54 - NMI	87 - A1	121 - CASL0
21 - IOCS16	55 - INTRQ	88 - A20	122 - RAS0
22 - MEMCS16	56 - D0	89 - A19	123 - CASH1
23 - SPKR	57 - D1	90 - A18	124 - CASL1
24 - SA0	58 - D2	91 - A17	125 - RAS1
25 - LA20	59 - D3	92 - A16	126 - RA10 [CS2]
26 - MASTER	60 - D4	93 - A15	127 - RA9 [CS1]
27 - ALE	61 - D5	94 - A14	128 - RA8 [CS0]
28 - AEN	62 - D6	95 - A13	129 - Vss
29 - SDEN	63 - D7	96 - A12	130 - RA7/ED7
30 - SDT/R [486]	64 - D8	97 - A11	131 - RA6/ED6
31 - Vcc	65 - D9	98 - Vss	132 - Vss
32 - REFRESH	66 - D10	99 - Vss	
33 - Vss	67 - Vss	100 - A10	
34 - EPEREQ		101 - Vcc	

TABLE 3-1. SIGNAL/PIN ASSIGNMENTS

NOTE: Some pins are multi-functional depending upon the mode of operation. The alternate signal for these pins is enclosed in [ ].

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		INITIALIZATION AND CLOCKING		
17	$\overline{\text{RSTIN}}$	$\overline{\text{System Reset}}$	I	$\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at power up. For a detailed description, refer to Section 4, Initialization And Clocking.
50	BCLK2	Bus Clock	I	BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock. For additional information, refer to section 4, Initialization And Clocking.
84	CLK14	Clock 14	I	CLK14 is derived from a 14.318 MHz crystal and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
		AT BUS		
40	$\overline{\text{IOR}}$	$\overline{\text{I/O Read}}$	I/O	$\overline{\text{IOR}}$ is an output and is asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. $\overline{\text{IOR}}$ is an input during Master Mode.
39	$\overline{\text{IOW}}$	$\overline{\text{I/O Write}}$	I/O	$\overline{\text{IOW}}$ is an output and is asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. $\overline{\text{IOW}}$ is an input during Master Mode.
38	$\overline{\text{MEMR}}$	$\overline{\text{Memory Read}}$	I/O	$\overline{\text{MEMR}}$ is an output and is asserted by the System Controller when a memory read access to the AT bus is to take place. $\overline{\text{MEMR}}$ is an input during Master Mode.

TABLE 3-2. SIGNAL DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
37	$\overline{\text{MEMW}}$	Memory Write	I/O	$\overline{\text{MEMW}}$ is an output and is asserted by the System Controller when a memory write access to the AT bus is to take place. $\overline{\text{MEMW}}$ is an input during Master Mode.
36	$\overline{\text{LOMEG}}$	First Megabyte	O	$\overline{\text{LOMEG}}$ is asserted when the AT bus address is below 1 Mbyte. Used with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ to generate $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$.
28	AEN	Address Enable	O	AEN is asserted by the System Controller while performing DMA and Refresh cycles.
79	BALE	AT Bus Address Latch Enable	O	Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
77	SYSCLK	System Clock	O	In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.
25	LA20	Early Address 20	I/O	When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
24	SA0	System Address 0	I/O	When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line. When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
32	REFRESH	Refresh	I/O	As an output, REFRESH is asserted by the System Controller to refresh memory on the AT Bus. As an input, REFRESH is asserted by the Bus Master in conjunction with MEMR to refresh memory on the AT Bus and DRAM controlled by the System Controller.
26	MASTER	Master	I	MASTER is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, MEMR, MEMW, IOR, and IOW to become input signals.
83	IOCK	I/O Check	I	When asserted, IOCK indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
21	IOCS16	16 Bit I/O Cycle	I	Initiates a 16 bit I/O AT bus cycle.
22	MEMCS16	16 Bit Memory Cycle	I	Initiates a 16 bit memory AT bus cycle.
20	ZEROWS	Zero Wait States	I	Initiates a zero wait AT bus cycle.
19	IOCHRDY	I/O Channel Ready	I	Initiates wait states during AT bus cycles.
116	DACKEN	DACK Enable	O	When DACKEN is asserted, MXCTL2-0 are used to generated DACK7-5, 3-0 and BUS_RST. Refer to Table 5-1 and Figure 5-1.
114	MXCTL2	Multiplexer Control 2	O	MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0 and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and RESCPU. Refer to Table 5-1 and Figure 5-1.
113	MXCTL1	Multiplexer Control 1	O	
112	MXCTL0	Multiplexer Control 0	O	

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
18	DRQIN	Multiplexed DRQ Inputs	I	DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1.
110	IRQSET1	Interrupt Request Set 1	I	IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
111	IRQSET0	Interrupt Request Set 0	I	IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, $\overline{\text{RESCPU}}$, $\overline{\text{IRQ8}}$, IRQ9 - IRQ11, IRQ14 and IRQ15. Refer to Table 5-1 and Figure 5-1.
23	SPKR	Speaker	O	SPKR drives the speaker transistor and is used for diagnostics.
27	ALE	Address Latch Enable	O	ALE is used to clock the SA1 - SA19 address latches.
115	$\overline{\text{CSEN}}$	$\overline{\text{Chip Select Enable}}$	O	When asserted, DPH, DPL, and RA10-RA8 are used to generate one of 28 different chip selects. Refer to Table 7-1.
74	DT/$\overline{\text{R}}$	Data Transmit/ $\overline{\text{Receive}}$	O	DT/$\overline{\text{R}}$ controls the direction of the AT Data Bus D00 - D15. When DT/$\overline{\text{R}}$ is high, data is directed to the AT Bus. When DT/$\overline{\text{R}}$ is low, data is transferred from the AT bus.
76	$\overline{\text{DEN0}}$	$\overline{\text{Data Bus Enable 0}}$	O	When asserted, $\overline{\text{DEN0}}$ enables the low order byte data buffer.
75	$\overline{\text{DEN1}}$	$\overline{\text{Data Bus Enable 1}}$	O	When asserted, $\overline{\text{DEN1}}$ enables the high order byte data buffer.
29	$\overline{\text{SDEN}}$	$\overline{\text{Swap Data Enable}}$	O	$\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
30	SDT/$\overline{R}$ [486]	Swap Data Transmit/ $\overline{\text{Receive}}$ [80486]	I/O	SDT/$\overline{R}$ [486] is tristated by a 50K pullup resistor internal to the WD76C10A when $\overline{\text{RSTIN}}$ at pin 17 is low. **SDT/$\overline{R}$ Mode - Output** When SDT/R is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{R}$ is low, it directs data from the high byte of the AT bus to the low byte. Forcing SDT/$\overline{R}$ high while $\overline{\text{RSTIN}}$ is low selects the SDT/$\overline{R}$ mode. Holding SDT/$\overline{R}$ high as $\overline{\text{RSTIN}}$ goes high maintains the SDT/$\overline{R}$ mode. **80486 Mode - Input** Selecting 80486 mode sets the SRC bit in Port 1072H to 1. This causes $\overline{\text{RDYIN}}$ at pin 51 to be the default processor clock source input. Forcing SDT/$\overline{R}$ low while $\overline{\text{RSTIN}}$ is low selects the 80486 mode. Holding SDT/$\overline{R}$ low as $\overline{\text{RSTIN}}$ goes high, maintains the 80486 mode. The SDT/$\overline{R}$ pin may may be forced low at reset with a 5K pulldown resistor or an open collector or tristate driver, driven by $\overline{\text{RSTIN}}$.
		MAIN PROCESSOR CONTROL		
52	CPUCLK	Processor Clock	I/O	CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at Port Address 1072H. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.
47	$\overline{\text{READY}}$	$\overline{\text{Processor Ready}}$	O	$\overline{\text{READY}}$ is an output to the processor.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MAIN PROCESSOR CONTROL (CONT.)		
51	RDYIN/CKA/ PE	Processor Ready In/ Alternate Clock/ Parity Error	I	Whether pin 51 is to be used as RDYIN, CKA or PE is determined by the Memory Control Register at Port Address 3872H. RDYIN is used in a discrete cache system and indicates a hit or miss. CKA may be used as an alternate source for CPUCLK processor clock. When used as PE, it indicates a parity error from an external memory controller.
78	CPURES	Main Processor Reset	O	CPURES is a synchronous processor reset signal.
49	HOLD	Hold Request	O	Processor hold cycle request.
55	INTRQ	Interrupt Request	O	Processor interrupt cycle request.
54	NMI	Non-Maskable Interrupt	O	Processor non-maskable interrupt cycle request.
45	S0 [ADS#]	Processor Status 0 [Address Status]	I	In the 80286 mode this pin is S0. In the 80386SX mode this pin is ADS#.
46	S1 [W/R#]	Processor Status 1 [Write Read]	I	In the 80286 mode pin 46 is S1. In the 80386SX mode pin 46 is W/R#
4	BHE	Bus High Enable	I/O	As an input, BHE indicates a transfer of the high byte on the processor data bus. BHE is an output during DMA transfers.
43	PEACK [D/C#]	Processor Extension Acknowledge [Data/Control]	I	In the 80286 mode, pin 43 is PEACK . In the 80386SX mode, pin 43 is D/C#.
44	M/IO	Memory or I/O	I	Processor Memory cycle or I/O Status cycle.
48	HLDA	Hold Acknowledge	I	Processor hold acknowledge.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MAIN PROCESSOR CONTROL (cont.)		
53	$\overline{\text{BUSYCPU}}$	$\overline{\text{Processor Busy}}$	O	Numeric Processor Busy (80287 or 80387SX) signal to CPU (80286 or 80386SX).
80 - 82 88 - 97 100 102 - 109 87 86	A23 - A21 A20 - A11 A10 A9 - A2 A1 A0 [BLE#]	Processor Address A23 through A00 [Bus Low Enable]	I/O	A23 through A1 are address lines from the 80286 or 80386SX. A0 is address bit A0 for the 80286, BLE# for the 80386SX, and is controlled by SA0 (AT Bus pin 24) during Master Mode operations. A21, A19 through A1 are outputs during refresh and DMA cycles and inputs in other modes. A20 and A0 are outputs during refresh, DMA and Master mode cycles and inputs in other modes.
		NUMERIC PROCESSOR CONTROL		
34	EPEREQ	Extend PERQ	O	PERQ extend signal to the 80386SX for IRQ13 handling. Used only for the 80386SX.
35	NPRST	Numeric Processor Reset	O	Reset to the numeric processor 80287 or 80387SX.
42	$\overline{\text{NPERR}}$	$\overline{\text{Numeric Processor Error}}$	I	Error signal from the numeric processor 80287 or 80387SX.
85	$\overline{\text{NPBUSY}}$	$\overline{\text{Numeric Processor Busy}}$	I	Busy signal from the numeric processor 80287 or 80387SX.
		DATA BUS		
73 - 70 68 66 - 56	D15 - D12 D11 D10 - D0	Data Bit 15 - Data Bit 12, Data Bit 11 Data Bit 10 - Data Bit 0	I/O	The Data Bits are connected directly to the Local and Numeric processors, DRAM data and AT Bus data transceivers.
16	DPL [CS3]	Data Parity Low Byte [Chip Select 3]	I/O	For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.
15	DPH [CS4]	Data Parity High Byte [Chip Select 4]	I/O	For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MEMORY AND EMS CONTROL		
126 127 128	RA10/CS2 RA9/CS1 RA8/CS0	DRAM Address Bit 10 through DRAM Address Bit 8, Chip Select 2 through Chip Select 0	O	The DRAM Address Bus is multi-functional. During DRAM cycles, RA10 through RA0 select the DRAM Row and Column.
130 131 1 3 4 6 7 8	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	DRAM Address Bit 7 through DRAM Address Bit 0, EDATA 7 through 0	I/O	During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.
14 11 125 122	$\overline{RAS3}$ $\overline{RAS2}$ $\overline{RAS1}$ $\overline{RAS0}$	Row Address Select 3 through Row Address Select 0	O	$\overline{RAS3}$ through $\overline{RAS0}$ are designed to access the DRAM without the use of external drivers.
12, 9, 123, 120	$\overline{CASH3}$ $\overline{[CASIN]}$ $\overline{CASH2}$ $\overline{CASH1}$ $\overline{CASH0}$	Column Address Select High 3 through Column Address Select High 0	I/O O O O	$\overline{CASH3}$ [$\overline{CASIN}$] is tristated by a 50K pullup resistor internal to the WD76C10A when $\overline{RSTIN}$ at pin 17 is low. **$\overline{CAS}$ Output Mode** $\overline{CASH3}$ through $\overline{CASH0}$ operate as output signals and are designed to access the DRAM without the use of external drivers. Forcing $\overline{CASH3}$ [$\overline{CASIN}$] high while $\overline{RSTIN}$ is low, selects the $\overline{CASH3}$ Output Mode. Holding $\overline{CASH3}$ [$\overline{CASIN}$] high as $\overline{RSTIN}$ goes high, maintains the $\overline{CASH3}$ Output Mode. **$\overline{CAS}$ Input Mode** In this mode pins 12, 13 and 10 function as input pins controlled by $\overline{CASIN}$, PE and WIRQ. $\overline{CASH2}$, $\overline{CASH1}$ and $\overline{CASH0}$ (pins 9, 123 and 120) remain output signals. Forcing $\overline{CASH3}$ [$\overline{CASIN}$] low while $\overline{RSTIN}$ is low, selects the $\overline{CAS}$ Input Mode. Holding $\overline{CASH3}$ [$\overline{CASIN}$] low as $\overline{RSTIN}$ goes high, maintains the $\overline{CAS}$ Input Mode.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MEMORY AND EMS CONTROL (cont.)		
				The CASH3 [CASIN] pin may be forced low at reset with a 5K pulldown resistor or an open collector or tristate driver, driven by RSTIN.
13	CASL3 [PE]	Parity Error	I/O	**CAS Output Mode**
10	CASL2 [WIRQ]	Weitek Interrupt	I/O	CASL3 through CASL0 are designed to access the DRAM without the use of external drivers.
124	CASL1	Column Address Select Low 3 through Column Address Select Low 0	O	
121	CASL0		O	
				CAS Input Mode - PE When CAS Input Mode is selected by [CASIN] on pin 12, and bits 13 and 12 of Port 3872H are both 1, pin 13 becomes an input and represents a Parity Error. A parity error is indicated by the low to high transition of the PE signal.
				CAS Input Mode - WIRQ When CAS Input Mode is selected by [CASIN] on pin 12, pin 10 becomes an interrupt signal typically connected to IRQ13, the error signal of a Weitek coprocessor.
				When WIRQ goes from low to high, an IRQ13 is generated to the system.
119	W/R	Write/Read	O	W/R is output as a high signal to write to memory and output as a low signal to read from memory. W/R should be buffered before use.

TABLE 3-2. SIGNAL DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
POWER MANAGEMENT CONTROL				
117	PDREF	Power Down Refresh	I	PDREF is a 64 KHz signal from the WD76C20. During power down, PDREF is passed internally to pin 32 ($\overline{\text{REFRESH}}$).
118	PMCIN	Power Management Control Input	I	PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
MISCELLANEOUS				
5, 33, 67, 98, 99, 129 132	Vss		I	Ground (7 pins)
2, 31, 69, 101	Vcc		I	+5 Volts (4 pins)

TABLE 3-2. SIGNAL DESCRIPTION cont.

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, RSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor. At this time the System Controller also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which are decoded externally as BUS_RST (DACK4), see sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the System Controller enters the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD76C20 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds higher than 50 MHz, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872H. The PMC control output 0 tristates the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by SCHH or SCH (CPU Clock Control Register - bits 01 or 00, at Port Address 1072H) or divided down by CLK_SPD (bits 14-12). Only the WD76C10ALP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle. The other method can be used when the CPUCLK is an

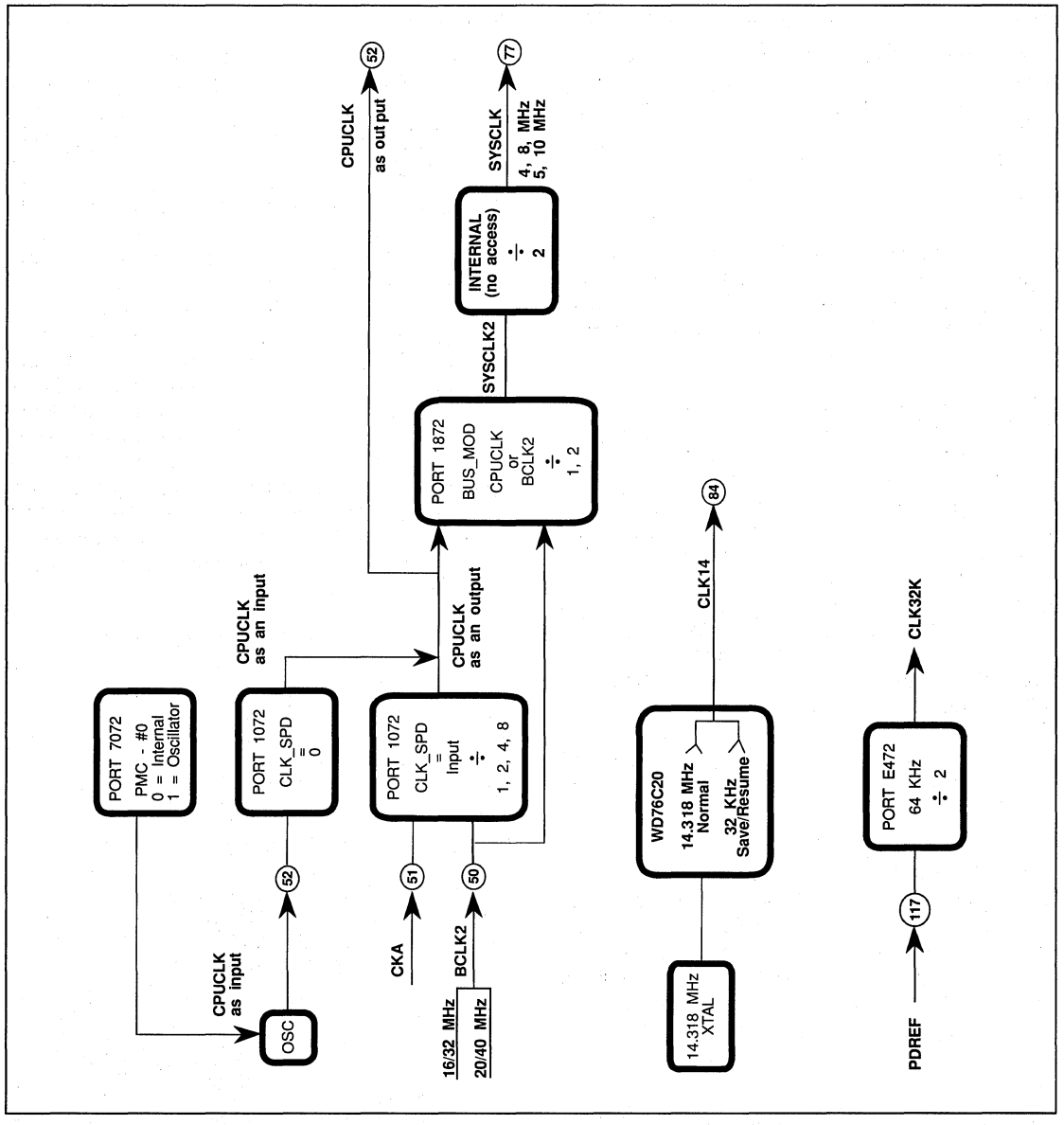


FIGURE 4-1. CLOCK CONTROL

output or input and generated by an external oscillator. In this case, EXT_HOLD is used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is determined by SRC (CPU Clock Control Register - bit 15 at Port Address 1072H). SRC is set automatically at power up reset, if a clock source is present at pin 51 (CKA).

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072H - Read and Write

15	14	13	12	11	10	09	08
SRC	CLK_SPD			AUT_ FST	ALT_CLK_SPD		

07	06	05	04	03	02	01	00
EXT_HOLD						SCHH	SCH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	000/001
AUT_FST ☆	0
ALT_CLK_SPD ☆	000
EXTEND_HOLD	0000
Bits 03, 02	None
SCH ☆	0
SCHH ☆	0

☆ Featured only in the WD76C10ALP

Bit 15 - SRC, CPUCLK Clock Source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

Default Value

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state within 64 clocks after RSTIN is de-asserted.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after RSTIN is de-asserted, or when operating in the 80486 Mode. The 80486 Mode is selected by holding SDT/R low during RSTIN transition from low to high.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK Clock Speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD *defaults to 000 or 001 at power up. Changing the CPUCLK from an input (CLK_SPD = 000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One ms later, CPUCLK becomes active as an output. One ms and 16 CPUCLK clocks (or one ms) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated due to the clock driver not being able to synchronously switch the clock. The one ms and 16 clocks or one ms. selection is made through the Diagnostic Register at Port 9872H.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source (* Default value).
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (* Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

* Based upon the value of CLOCK_DIR_IN at power up (refer to Table 5-1, Figure 5-1 and section 5.1.2).

Bit 11 - AUT_FST, Automatic Processor Clock Speed Switching
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When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-2. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-2 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-1 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-1. The EXT_HOLD field must be 0000 when AUT_FST = 1.

TURBO	AUTO_FST	CPU CLOCK SPEED
0	0	CLK_SPD
0	1	CLK_SPD
1	0	ALT_CLK_SPD
1	1	CLK_SPD or ALT_CLK_SPD

TABLE 4-1. CLOCK SWITCH SELECTION

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access or processor reset	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-2. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate Clock Speed
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ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value).

0 0 1 - Equals source.

0 1 0 - Equals source div by 2.

0 1 1 - Equals source div by 4, 25% duty cycle.

1 0 0 - Equals source div by 4, 75% duty cycle.

1 0 1 - Equals source div by 8, 12% duty cycle.

1 1 0 - Equals source div by 8, 88% duty cycle.

Bits 07-04 - EXT_HOLD, Extend Processor Hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external TURBO signal is asserted, EXT_HOLD is forced to 0000. When the external TURBO signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value).

0 0 0 1 - 1 µs hold after refresh.

0 0 1 0 - 2 µs hold after refresh.

0 0 1 1 - 3 µs hold after refresh.

0 1 0 0 - 4 µs hold after refresh.

↕

1 1 0 1 - 13 µs hold after refresh.

1 1 1 0 - 14 µs hold after refresh.

1 1 1 1 - 15 µs hold after refresh.

Bits 03-02 - Reserved for future use, must be set to zero

Bit 01 - SCHH, Stop CPUCLK at next Halt and Hold.
Featured only in the WD76C10ALP

SCHH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10ALP rather than an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate selected by the Refresh Control Register at Port 2072H.

SCHH = 0 -
Normal processor clock (default value).

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

Bit 00 - SCH, Stop CPUCLK at next Hold
Featured only in the WD76C10ALP

SCH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10ALP instead of an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate as selected by the Refresh Control Register at Port 2072H.

SCH = 0 -
Normal processor clock (Default value).

SCH = 1 -
Stop processor clock at next processor hold cycle.

4

5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8) and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external 74F138, 3 to 8 Decoder for desktop systems, or 74ACT138, 3 to 8 Decoder for laptop systems, uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 74F151, 8 to 1 Multiplexer for desktop systems, or 74ACT151, 8 to 1 Multiplexer for laptop systems, to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1. This controls the default value of CLK_SPD in the CPU Clock (CPUCLK) Control Register at Port 1072H. See section 4.2.4.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA, DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{RSTIN}$ to determine ROM data width (ROM8). The $\overline{RESCPU}$ and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus And Terminal Count (TC) Signal

The AT Address Bus SA19-00 and $\overline{BHE}$ are generated from A19-00 with external latches and tristate buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and $\overline{CSEN}$ are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD76C10A, the $\overline{TURBO}$ signal may be connected directly to PMCIN. In the WD76C10ALP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{IRQ8}$	IRQ12	$\overline{TURBO}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	$\overline{RESCPU}$	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

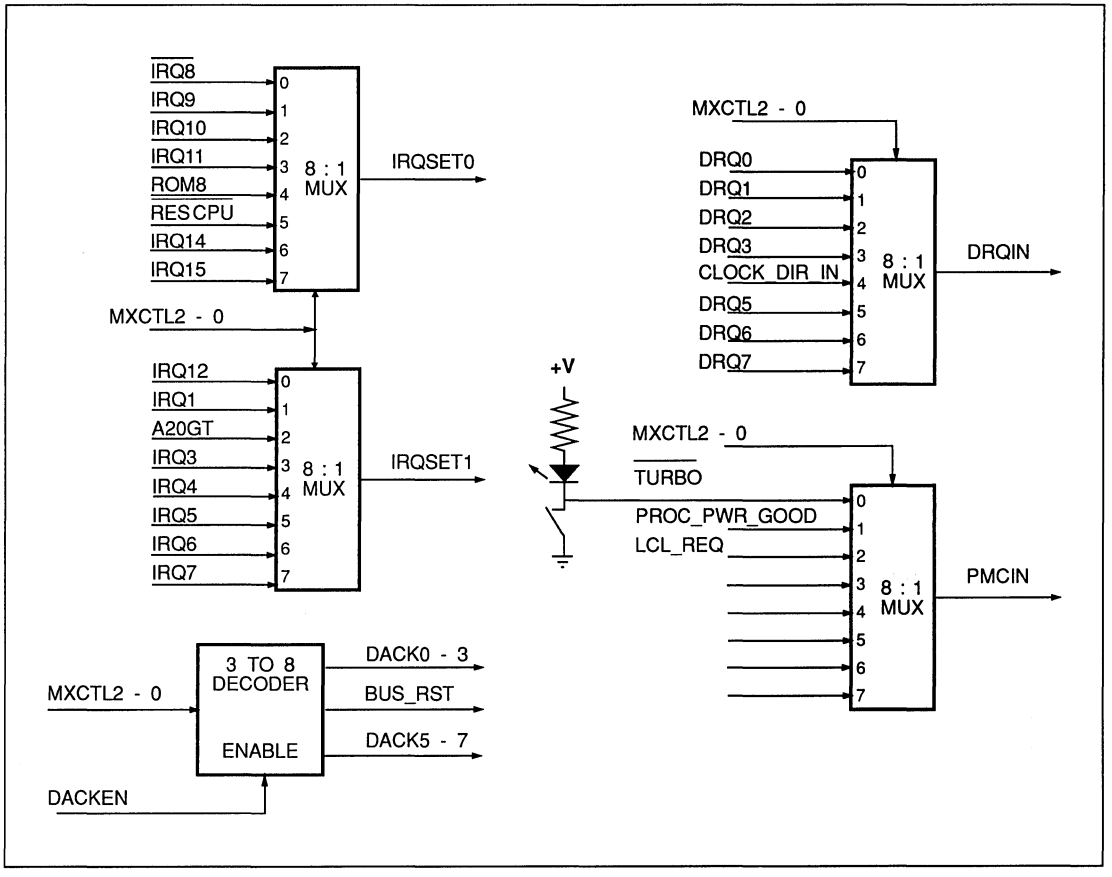


FIGURE 5-1. MXCTL2-0 MULTIPLEXING

5.3 NUMERIC PROCESSOR

5.3.1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872H - Read and Write

15	14	13	12	11	10	09	08
NP_BSY	PRO_PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI16	WSM_16	WSI8		WSM8	

Signal Name	Default At RSTIN
NP_BSY	0
PRO_PD ☆	0
Bit 12	None
FPD ☆	0
BUS_MOD	00
BRQ_DEL	00
BAK_DEL	11
WSI_16	0
WSM_16	0
WS18	10
WSM8	10

☆ Featured only in the WD76C10ALP

Bit 15 - NP_BSY, Numeric Processor Busy

NP_BSY must be set for systems using an 80286 CPU where the CPU runs faster than the AT bus. The causes BUSYCPU to be asserted early during any CPU write to I/O ports F8H through FFH. BUSYCPU is de-asserted at the end of the I/O write if the coprocessor has not asserted its own NPBUSY by this time. Early assertion of BUSYCPU is necessary to prevent a loss of synchronization between the 80286 and 80287. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Force an early BUSYCPU for I/O writes to coprocessor addresses F8H through FFH. (Default value).

NP_BSY = 1 -
Normal BUSYCPU assertion.

Bit 14 - PRO_PD, Processor Power Down
Featured only in the WD76C10ALP

When PRO_PD has been changed from zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated at the next Halt State and the expansion bus will continue to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD76C10ALP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power (Default value).

PRO_PD = 1 -
Start processor power down sequence.

Bit 13 - FPD, Full Power Down
Featured only in the WD76C10ALP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except RSTIN, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Power Down) from Port 7072H is set. This enables the powering down of all chips except DRAM, WD76C10ALP, WD76C20, WD76C30 and WD90C20. The WD76C20 provides PDREF

(a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the REFRESH signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at Port 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port 8872H input is high. The tristated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus Mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

- 0 0 - Bus logic uses BCLK2 divided by 2 (Default value).
- 0 1 - Bus logic uses BCLK2 divided by 1.
- 1 0 - Bus logic uses CPUCLK divided by 2.
- 1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

- 0 0 - 1 Bus clock delay (Default value).
- 0 1 - .5 Bus clock delay.
- 1 0 - No clock delay.
- 1 1 - Reserved.

Bits 07, 06 - BAK_DEL, Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

- 0 0 - No delay.
- 0 1 - -.5 Bus clock delay.
- 1 0 - -1 Bus clock delay.
- 1 1 - +.5 Bus clock delay (Default value)

Bit 05 - WSI16, Wait State for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state (Default value).

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait State for 16 bit Memory

WSM16 = 0 -
1 Bus clock wait state (Default value).

WSM16 = 1 -
2 Bus clock wait state.

Bits 03, 02 - WSI8, Wait State for 8 bit I/O

WSI8
03 02 -

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

Bits 01, 00 - WSM8, Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

5.3.2 Numeric Processor Busy (NPBUSY) Reset

Port Address 0F0H - Write only

Writing any data to this port resets the 80287 busy signal (de-asserts NPBUSY). The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H - Write only

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	8 MHz	ASYNC	0X	01	01
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	00
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA controller #1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA controller #2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1. Table 5-4 indentifies the Controller/-Channel location and function.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

Single Transfer Mode - 01

In single transfer mode, the channel makes one transfer for each request. The word count is decremented, and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the $\overline{MASTER}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or $\overline{MEMW}$ signals.

Write - 01

A write transfers data from an I/O device to memory.

Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address Hex	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
080-09F			DMA Page Register
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008H, 0D0H - Write only

The Command Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

Signal Name	Default At RSTIN
All signals	0

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008H, 0D0H - Read only

Bits 3-0 are reset by RSTIN, writing any data to Port Address 00DH or 0DAH (see section 5.4.14) or when read by a Status Read Command.

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0 TC

Signal Name	Default At RSTIN
CH3_DRQ - CH0_DRQ	None
CH3_TC - CH0_TC	0

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009H, 0D2H - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
					CRQ	CH#	

Signal Name	Default At RSTIN
All signals	0

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a RSTIN, or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H - Write only

7	6	5	4	3	2	1	0
					SE_ MA	CH#	

Signal Name	Default At RSTIN
All signals	1

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH - Write only

Writing any data to this register resets all Masks. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH - Write only

7	6	5	4	3	2	1	0
				CH3_ MA	CH2_ MA	CH1_ MA	CH0_ MA

Signal Name	Default At RSTIN
All signals	1

Bits 7-4 - Not used, state is ignored

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00BH, 0D6H - Write only

This register selects the mode and type of transfer for each channel. Refer to sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_ MOD		AD_ DEC	AUTO	TRA_ TYP		CHA# SEL	

Signal Name	Default At RSTIN
All signals	None

Bits 7, 6 - TRA_MOD, Transfer Mode

TRA_MOD 7	6	
0	0	- Demand
0	1	- Single
1	0	- Block
1	1	- Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP

3	2	
0	0	0 - Verify
0	1	1 - Write
1	0	0 - Read
1	1	1 - Not used

Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL

1	0	
0	0	0 - Channel 0
0	1	1 - Channel 1
1	0	0 - Channel 2
1	1	1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H - Write only

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip flop is reset, bits 7-0 are accessed, and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see section 5.4.14). In either case, the data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.14 Master Clear Rgister

Port Addresses 00DH, 0DAH - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.15 DMA Mode Shadow Register

Port Address B872H - Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt controller #1 is in the I/O space of 020H to 021H and interrupt controller #2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	RTC
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

Interrupt Controller	Address Hex	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Signal Name	Default At RSTIN
All signals	None

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1

Bit 3 - L_T, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bit 2 - I2 H_L, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

Port Addresses 0A1H - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H - Write only

A Slave does not have ICW4.

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Not Special Fully Nested Mode

S F N M = 1 -
Special Fully Nested Mode

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT 7	6	5	
0	0	0	- Clear Rotate On Automatic EOI
0	0	1	- Non-specific EOI
0	1	0	- Not used
0	1	1	- Specific EOI
1	0	0	- Set Rotate on Automatic EOI
1	0	1	- Rotate on Non-Specific EOI
1	1	0	- Set Priority
1	1	1	- Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV 2	1	0	
0	0	0	- Interrupt Level 0
	↕		
1	1	1	- Interrupt Level 7

5.5.3.3 OCW3

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ISR	

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM 6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 - No Poll Command

P_C = 1 - Poll Command

Bits 1-0 - IRR_ISR, Interrupt Request Register and Interrupt Service Register

IRR_ISR 1	0	
0	0	- Not used
0	1	- Not used
1	0	- Read Interrupt Request Register
1	1	- Read Interrupt Service Register

5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040H	Timer 0 Count/Status	Read/Write
041H	Timer 1 Count/Status	Read/Write
042H	Timer 2 Count/Status	Read/Write
043H	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

Address 9	8	7	6	5	4	3	2	1	0	Decodes	Hex
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PIO)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real-Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real-Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092H)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087H	DMA Channel 0
0083H	DMA Channel 1
0081H	DMA Channel 2
0082H	DMA Channel 3
008BH	DMA Channel 5
0089H	DMA Channel 6
008AH	DMA Channel 7
008FH	Refresh

TABLE 5-9. PAGE REGISTER DECODES

NOTE

Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

5.8 NMI AND REAL-TIME CLOCK

5.8.1 Real-Time Clock Address Register

Port Address 070H-07EH even - Write only

There is only one RTC Address Register. All even number addresses from 070H through 07EH access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
RTC6 - RTC0	None

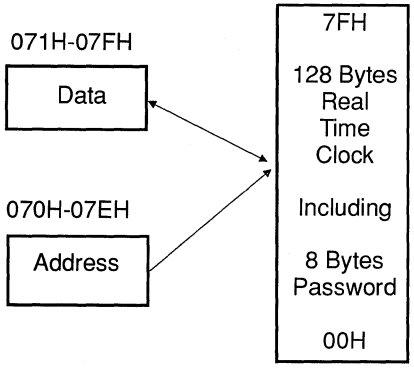
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real-Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real-Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071H-07FH.



5.8.2 Real-Time Clock Data Register

Port Address 071H-07FH odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071H through 07FH access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to section 7.2).

7	6	5	4	3	2	1	0
Real-Time Clock Data							

5.8.3 Lock Pass, Alternate A20G And Hot Reset

Port Address 092H - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
Bits 7-4, 2	None
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by $\overline{RSTIN}$.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

Bit 0 - HOT_RST, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Port Address 061H- 06FH odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

Odd numbered Port Addresses 061H through 06FH provide access to parity error and I/O Channel Check of the expansion bus.

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity Error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O Channel Check from the expansion bus (read only)

IOCK = 0 -
No I/O Channel Check Error

IOCK = 1 -
I/O Channel Check Error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O Channel Check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable Parity Error Check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by Port Address register 6072H, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled

Bit 1 - ENSPK, Enable Speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA10 through RA0. During I/O cycles, RA10, RA9 and RA8 become CS2, CS1 and CS0 and, along with CS3, are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA10 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM, plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{MEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128 Kbyte to 640 Kbyte, 256 Kbyte to 640 Kbyte and 512 Kbyte to 640 Kbyte.

When disabling any on-board DRAM, the register at Port Address 6872H must not be programmed to enable the on-board Lower EMS Page Frame.

The WD76C10A and WD76C10ALP provide support for DRAM banks to be independent or two-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size.

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872H - Read and Write

15	14	13	12	11	10	09	08
PG_ CAS		CA		PG	ILV		

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS	0
CA	00
PG	0
ILV	00
SIZE_BNK3	00
SIZE_BNK2	00
SIZE_BNK1	00
SIZE_BNK0	00

Bit 15 - PG_CAS, Page Mode CAS Width

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks. This is required for 80386SX Pipeline mode.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache Mode

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the $\overline{\text{RDYIN}}$ signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the $\overline{\text{RDYIN}}$ (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)

0 1 - Cache Mode enabled. $\overline{\text{RDYIN}}$ at pin 51 indicates discrete cache hit or miss.

1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the Discrete Cache controller.

1 1 - External Memory Controller. Pin 51 may be used as the alternate clock CKA. When $\overline{\text{CAS}}$ Input Mode is enabled, PE on pin 13 becomes an input and represents an error. (See pin 12 description in Table 3-2 on selecting $\overline{\text{CAS}}$ Mode.)

Bit 11 - PG, Page Mode

PG = 0 - Non-page mode (Default value)
Word interleaving is employed when bank interleaving is enabled by ILV.

PG = 1 - Page mode
Page mode interleaving is performed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In Non-page Mode (PG = 0), word interleaving is employed. In Page Mode (PG = 1), Page Mode interleaving is used. Four way interleave is only supported in Page Mode with four banks of 4 Mbit × 16 DRAMs installed. Interleave of 64 Kbit × 16 DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size and assigned the same starting address when they are interleaved together.

ILV 10 09 08

- 0 0 0 - No interleaving performed
- 0 0 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are not interleaved
  Banks 0 and 1 must be the same size
- 0 1 0 - Banks 0 and 1 are not interleaved
  Banks 2 and 3 are interleaved
- 0 1 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are interleaved
  (Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.)
- 1 0 0 - Page Mode four way interleave
  (Banks 0, 1, 2 and 3 must have 4 Mbit × 16 DRAM installed.)

Bits 07, 06 - SIZE_BNK3, Size of Bank 3

The WD76C10A and WD76C10ALP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK3
07 06

- 0 0 - 64 Kbit × 16 (Default value)
- 0 1 - 256 Kbit × 16
- 1 0 - 1 Mbit × 16
- 1 1 - 4 Mbit × 16

Bits 05, 04 - SIZE_BNK2, Size of Bank 2

The WD76C10A and WD76C10ALP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK2
05 04

- 0 0 - 64 Kbit × 16 (Default value)
- 0 1 - 256 Kbit × 16
- 1 0 - 1 Mbit × 16
- 1 1 - 4 Mbit × 16

Bits 03, 02 - SIZE_BNK1, Size of Bank 1

The WD76C10A and WD76C10ALP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK1
03 02

- 0 0 - 64 Kbit × 16 (Default value)
- 0 1 - 256 Kbit × 16
- 1 0 - 1 Mbit × 16
- 1 1 - 4 Mbit × 16

Bits 01, 00 - SIZE_BNK0, Size of Bank 0

The WD76C10A and WD76C10ALP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK0
01 00

- 0 0 - 64 Kbit × 16 (Default value)
- 0 1 - 256 Kbit × 16
- 1 0 - 1 Mbit × 16
- 1 1 - 4 Mbit × 16

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 1 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 0 start address					

Port Address 5072H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 3 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 2 start address					

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes. For three banks of the same size, in which two are interleaved, the two interleaved banks must be placed at a lower starting address than the third bank.

RAM SIZE	PAGE SIZE	BANK SIZE
64 Kbits X 1	512 Bytes	128 Kbytes
256 Kbits X 1	1024 Bytes	512 Kbytes
1 Mbits X 1	2048 Bytes	2048 Kbytes
4 Mbits X 1	4096 Bytes	8192 Kbytes

6.2.3 Split Starting Address

Port Address 5872H - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At $\overline{RSTIN}$
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	00
SPLIT_SIZE	00
Bits 01, 00	None

Bit 15 - EN_BK3, Enable Bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value)

EN_BK3 = 1 -
Bank 3 is enabled

Bit 14 - EN_BK2, Enable Bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value)

EN_BK2 = 1 -
Bank 2 is enabled

Bit 13 - EN_BK1, Enable Bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value)

EN_BK1 = 1 -
Bank 1 is enabled

Bit 12 - EN_BK0, Enable Bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value)

EN_BK0 = 1 -
Bank 0 is enabled

Bits 11, 10 - DRAM_DRV, DRAM Driver Strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

DRAM_DRV
11 10

0 0 - Full strength DRAM address drive, up to 350 pF (Default value)

0 1 - Low strength DRAM address drive, up to 100 pF

1 0 - Medium strength DRAM address drive, up to 180 pF

1 1 - High strength DRAM address drive, up to 260 pF

Bits 09, 08 - SP SIZE, Split Size

The split is implemented by moving the block of memory between 0A0000H through 0FFFFFH to another area. The destination area must start on a 512 Kbyte boundary. If BIOS is to be shadowed, the split size must be 320 Kbyte for a 64 Kbyte shadow or 256 Kbyte for a 128 Kbyte shadow, and the RAM Shadow And Write Protect Register (Port 6072H) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000H (640 Kbyte) to 100000H (1024 Kbyte) is available for remapping. The remapping may start at 100000H, providing 384 Kbyte of extended memory, or may start at 0F0000H to allow BIOS shadowing, with 320 Kbyte of extended memory. Only a single bank may be split. The bank to be split must be at least 512 Kbyte or larger.

SPLIT SIZE

09 08

0 0 - No split (Default value)

0 1 - 256 Kbyte split, memory moved from 0A0000H to 0DFFFFH

1 0 - 320 Kbyte split, memory moved from 0A0000H to 0EFFFFH

1 1 - 384 Kbyte split, memory moved from 0A0000H to 0FFFFFH

Bits 07-02 - A24-A19, Split Starting Address

Bits 01, 00 - Not used, state is ignored

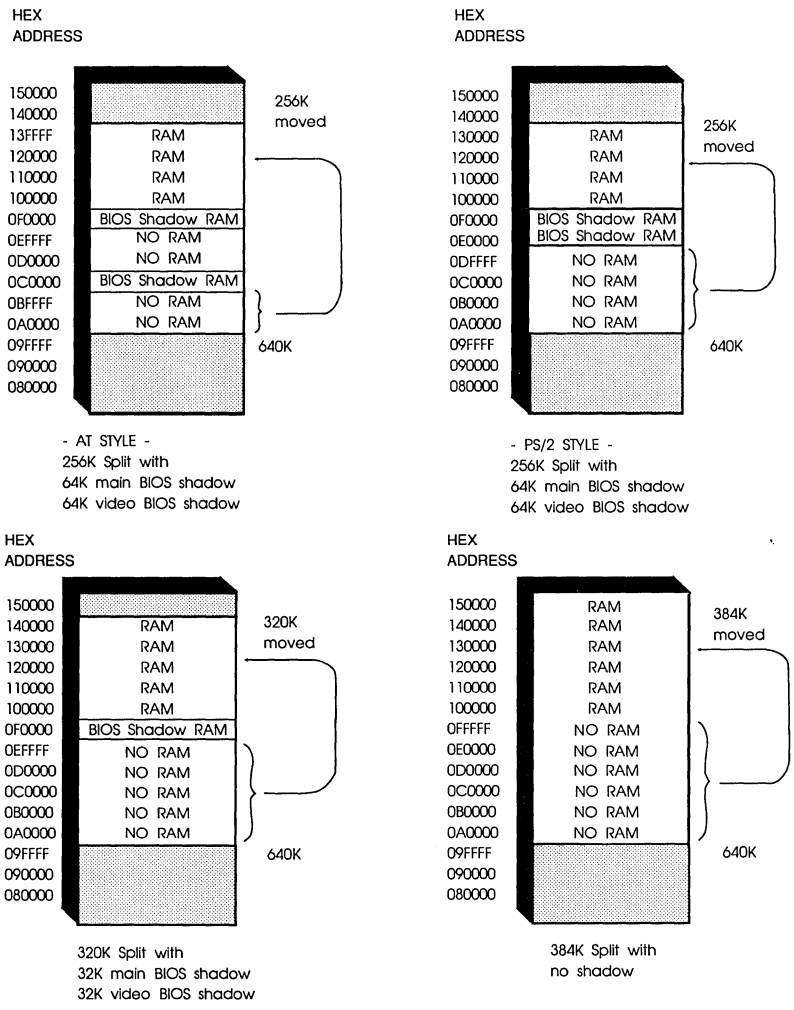


FIGURE 6-1. SPLIT SIZE

6.2.4 RAM Shadow And Write Protect

Port Address 6072H - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
X_ MEM		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	00
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	00
X_MEM	0
Bit 06	None
VB_SIZ	00
ROM_TYP	00
BL_MOU ☆	00

☆ Featured only in the WD76C10ALP

Bit 15, 14 - DIS_MEM, Disable On-board Memory

DIS_MEM
15 14

0 0 - On-board memory from 128 KB to 640 KB not disabled (Default value).

0 1 - On-board memory from 512 KB to 640 KB disabled.

1 0 - On-board memory from 256 KB to 640 KB disabled.

1 1 - On-board memory from 128 KB to 640 KB disabled.

Bit 13 - HM_WP, High Memory Write Protect Enable

This bit enables the write protection for the memory boundary established by the register at Port C072H.

HM_WP = 0 -
High memory write protect not enabled (Default value).

HM_WP = 1 -
High memory write protect enabled.

Bit 12 - WP, Shadowed BIOS Write Protect Enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value).

WP = 1 -
Write protect for shadowed BIOS enabled.

Bit 11 - INV_PAR, Invert Parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value).

INV_PAR = 1 -
Invert parity when writing to on-board DRAM.

Bit 10 - PAR_DIS, Parity Checking Disabled

Parity checking is normally enabled or disabled by Port 061H. Setting PAR_DIS overrides the Port 061H setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by Port 061H (Default value).

PAR_DIS = 1 -
Parity checking disabled.

Bits 09, 08 - SHD, Shadow BIOS

Before the BIOS can be shadowed, the SPLIT_SIZE field in the Split Starting Address Register at Port 5872H must be programmed to non-zero.

ROM at FE0000H - FFFFFFH, the top of 16 MByte address space is never shadowed.

Option SHD 11 should be used when Video Remap Function is desired (i.e. Video BIOS in the lower half of EPROM shows up at C0000H).

64 Kbyte of system BIOS at 0F0000H - 0FFFFFH, and up to 64 Kbyte of video BIOS at 0C0000H - 0CFFFFH, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000H - 0FFFFFH. When SHD is set to 11, the video BIOS appears at 0C0000H - 0CFFFFH rather than 0E0000H - 0EFFFFH.

The video shadow size at 0C0000H - 0CFFFFH is determined by VB_SIZ, the video BIOS size field.

SHD
09 08

☆ 0 0 - No BIOS shadowing, allows 384 KB remap (Default value).

0 1 - 64 KB system BIOS shadow, 0F0000H - 0FFFFFH, allows 320 KB remap.

1 0 - 128 KB system BIOS shadow, 0E0000H - 0FFFFFH, allows 256 KB remap.

☆ 1 1 - 64 KB system BIOS shadow, 0F0000 - 0FFFFF and video BIOS shadow, allows 256 KB remap.

☆ See note following bits 01, 00.

Bit 07 - X_MEM, Shadow BIOS for Read/Write Memory

When SHD (bits 09 and 08) equals 11, X_MEM provides the means of using RAM from E8000H through EFFFFH not being used for video BIOS shadowing, to be used as read/write memory.

X_MEM = 0 - SHD = 11
ROM_TYP = 10 - VB_SIZ = 01

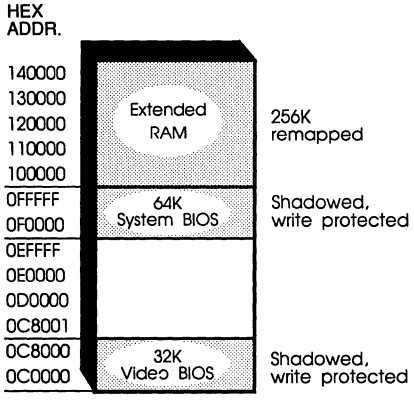


FIGURE 6-2. X_MEM = 0

X_MEM = 1 - SHD = 11
ROM_TYP = 10 - VB_SIZE = 01

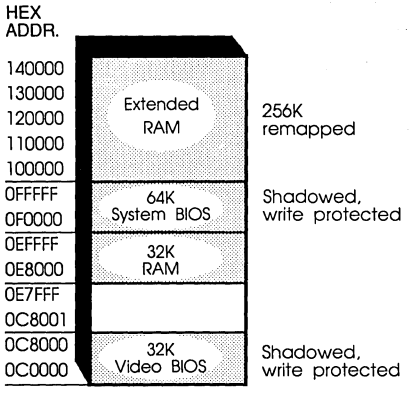


FIGURE 6-3. X_MEM = 1

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS Size

VB_SIZ ☆
05 04

0 0 - 16 KB video BIOS (Default value)

0 1 - 32 KB video BIOS

1 0 - 48 KB video BIOS

1 1 - 64 KB video BIOS

☆ See note following bits 01, 00.

Bits 03, 02 - ROM_TYP, ROM Type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000H - 0FFFFFH or FE0000H - FFFFFFH.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000H - 0FFFFFH or FF0000H - FFFFFFH.

For ROM type 10, CSPROM is asserted when the address is 0F0000H - 0FFFFFH, FF0000H - FFFFFFH or 0C0000H - 0CXFFFH where X is determined by VB_SIZ. This allows either a 128 Kbyte BIOS with a 64 Kbyte system BIOS and a 64 Kbyte video BIOS, or a 64 Kbyte BIOS with a 32 Kbyte system BIOS and a 32 Kbyte video BIOS. The 32 Kbyte video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000H - CX000H and F0000H - FX000H. A

64 Kbyte EPROM needs addresses SA15 - SA0. A 128 Kbyte EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128 KB system BIOS, located at E0000H - FFFFFH
- 0 1 - 64 KB system BIOS, located at F0000H - FFFFFH (Default value)
- ☆ 1 0 - 64 KB or 128 KB shared BIOS System BIOS located at F0000H - FFFFFH, video BIOS located at C0000H - CX000H
- 1 1 - Reserved

☆ See note following bits 01, 00.

Bits 01, 00 - BL_MOU, Backlight Mouse Control
Featured only in the WD76C10ALP

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port 1072H bit 11. Enabling the Backlight Mouse Control also affects the Back/light and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00

- 0 0 - No mouse control (Default value)
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

☆ **NOTE**

When SHD = 11 and X_MEM = 0, or SHD = 00 and ROM_TYP = 10, the portion of 0E0000H DRAM memory that is not mapped to 0C0000H (as determined by VB_SIZ) is not accessible. Once a portion of 0E0000H segment is mapped to 0C0000H, all 0E0000H accesses go to the expansion bus without generation of $\overline{\text{CSPROM}}$. This allows AT bus plug-in boards and/or drivers to access the E0000H segment.

6.2.5 High Memory Write Protect Boundary

Port Address C072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At $\overline{\text{RSTIN}}$
Bits 15-08	None
A24 - A17	00

Bits 15-08 - Not used, state is ignored

Bits 07-00 - A24-A17, Boundary Address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at Port 6072H. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at Port 4072H, the memory timing mode changes immediately. The code that programs this register should be in ROM and not shadowed in RAM.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072H - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_ RAW	NP_WCAS		_NP_RCAS	

07	06	05	04	03	02	01	00
	NP_RAS_ HLD		NP_PWE			NP_WS	

Signal Name	Default At RSTIN
Bits 15, 07	None
NP_MODE	00
NP_RAW	0
NP_WCAS	00
NP_RCAS	00
NP_RAS_HLD	00
NP_PWE	000
NP_WS	00

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-Page Mode

There are two non-page modes available, Mode-00 and Mode-01. Mode-00 provides one processor clock of row address hold time and is used for 1, 2 or 3 wait state memory cycles. Mode-01 provides a half processor clock of row address hold time and is used for 0 wait state memory cycles. Because the memory timing may be adjusted in increments of half a processor clock, Mode-00 is suited for all DRAM and processor speeds.

Mode-01 provides a half processor clock row address hold time, which is usually sufficient for system speeds of 12.5 MHz and slower. This compressed timing allows zero wait state operation.

Table 6-1A shows typically required DRAM speeds and register programming values for various processor speeds. Because DRAM timing varies among manufacturers, the required DRAM speed may differ from those listed in the table.

NP_MODE
14 13

0 0 - Minimum 1 wait state.

0 1 - Minimum 0 wait state.

PROCESSOR SPEED	NP_ MODE	DRAM SPEED	WAIT STATES	REGISTER 4072H
12.5 MHz	01	80 ns	0	3560H
16 MHz	01	53 ns	0	3560H
16 MHz	00	80 ns	1	1025H
20 MHz	00	80 ns	1	1025H
20 MHz	00	100 ns	2	107AH

TABLE 6-1A. TYPICAL DRAM SPEEDS

Bit 12 - NP_RAW, Non-page disable Read After Write

EMS accesses and interleave miss cycles (I/O cycle to device on RAD) may add one additional wait state.

NP_RAW = 0 -
Memory read cycles immediately following a write cycle causes an automatic wait state to be added before initiating the read cycle.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bit 11, 10 - NP_WCAS, Non-page Write CAS Delay

NP_WCAS
11 10

0 0 - CAS write delay 1.0 CLK2
0 1 - CAS write delay 1.5 CLK2
1 0 - CAS write delay 2.0 CLK2
1 1 - CAS write delay 2.5 CLK2

Bit 09, 08 - NP_RCAS, Non-page Read CAS Delay

NP_RCAS
11 10

0 0 - CAS read delay 1.0 CLK2
0 1 - CAS read delay 1.5 CLK2
1 0 - CAS read delay 2.0 CLK2
1 1 - CAS read delay 2.5 CLK2

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS Hold Time

The RAS active delay is reduced by half a clock during writes if NP_WCAS is set to 1X, or during reads if NP_RCAS is set to 1X.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS.

0 1 - RAS active until 1.5 clock after CAS.

1 0 - RAS active until 2.0 clock after CAS.

1 1 - RAS active until 2.5 clock after CAS.

Bits 04-02 - NP_PWE, Non-page CAS Pulse Width Extension

The pulse width is reduced by half a clock during writes if NP_WCAS is set to X1, or during reads if NP_RCAS is set to 1X.

NP_PWE
04 03 02

0 0 0 - No extension (2 CLK2 normal)

0 0 1 - Extended by 0.5 CLK2

0 1 0 - Extended by 1.0 CLK2

0 1 1 - Extended by 1.5 CLK2

1 0 0 - Extended by 2.0 CLK2

1 0 1 - Extended by 2.5 CLK2

1 1 0 - Extended by 3.0 CLK2

1 1 1 - Extended by 3.5 CLK2

Bits 01, 00 - NP_WS, Non-page Wait States

NP_WS makes it possible to unconditionally add wait states to all DRAM cycles. Condional wait states may be added to read after write cycles, EMS accesses and interleave miss cycles, with NP_RAW (bit 12).

NP_WS
01 00

0 0 - No wait states added

0 1 - 1 Wait state added

1 0 - 2 Wait states added

1 1 - 3 Wait states added

TIMING	NUMBER OF CLK2'S	
	MODE-00	MODE-01
Row address to RAS	2	2
RAS width	3 + NPH + NPHB / 2	1 + NPH + NPHB / 2
Row address hold	1	0.5
Column address setup (read)	1 + NPRF / 2	0.5 + NPRF / 2
Column address setup (write)	1 + NPWF / 2	1 + NPWF / 2
RAS hold (read from CAS)	1 + NPHB / 2 - NPRF / 2 + NPH	0.5 - NPRF / 2 + NPH
RAS hold (write)	1 + NPHB / 2 - NPWF / 2 + NPH	0.5 - NPWF / 2 + NPH
CAS width (read)	① + NPCAS + NPCB / 2 - NPRF / 2	① + NPCAS + NPCB / 2 - NPRF / 2
CAS width (write)	① + NPCAS + NPCB / 2 - NPWF / 2	① + NPCAS + NPCB / 2 - NPWF / 2
RAS precharge	2 × (2 + NP_WS) - RAS width	2 × (2 + NP_WS) - RAS width
Column address hold	1 - NPCB / 2	1 - NPCB / 2

① 2 if NPCAS = 0 or 1
1 if NPCAS = 2 or 3

NPWF = Bit 10 NPRF = Bit 08 NPH = Bit 06 NPHB = Bit 05
NPCAS = Bits 04, 03 NPCB = Bit 02 NP_WS = Bits 01, 00

TABLE 6-1B. NON-PAGE MODE TIMING

6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access ☆	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access ☆	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access ☆	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	3
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access, pipline mode ☆	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit, pipeline mode ☆	1
	Read page first access non-pipeline mode ☆	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access ☆	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	3
	Read cache miss, page miss	4

☆ Equal Bank sizes, non-EMS cycle

First access is a page mode memory cycle which immediately follows a refresh, DMA or master cycle. It is not necessary for the DRAMs to be precharged for a first access cycle, since all RAS signals have been high in the previous cycle. This shortens a first access page mode cycle by one wait state. For example, a read page miss, non-pipeline mode in 80386SX mode is four wait states. A read page miss, non-pipeline mode, first access in 80386SX mode is three wait states. All installed DRAMs must be the same size and configuration and the memory cycle cannot be an EMS cycle for a first access to occur.

TABLE 6-2. PAGE MODE WAIT STATES

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64 Kbyte, 256 Kbyte, 1 Mbyte or 4 Mbyte SIMM memory modules.

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	64K NON-INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64K 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64K 4-WAY, 256K 2-WAY INTERLEAVE OR 1 Mb NON-INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	256K 4-WAY, 1 Mb 2-WAY INTERLEAVE OR 4 Mb NON-INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1 Mb 4-WAY OR 4 Mb 2-WAY INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	4 Mb 4-WAY INTERLEAVE										
ROW	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	REFRESH ADDRESS										
ROW	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE NON-INTERLEAVE ADDRESS CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE 2-WAY INTERLEAVE ADDRESS CONFIGURATION

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872H - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	00
Bits 12, 09, 08	None
EMS_EN	00
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS Pointer

The INC bit controls whether or not the EMS Pointer at Port E072H is to be incremented after each read or write of the EMS Page Register at Port E872H.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper Page Frame Location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000H (Default value)

0 1 - Upper page frame starts at C8000H

1 0 - Upper page frame starts at CC000H

1 1 - Upper page frame starts at D0000H

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS Enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming without having to enable a Page Frame. This is useful for initializing the lower Page Frame.

1 0 - Enable upper Page Frame assignments and EMS register programming.

1 1 - Enable upper and lower Page Frame assignments and EMS register programming.

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable Lower Boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17,
LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128 Kbyte below the actual start address. For example, to start EMS at the 1 Mbyte boundary, this field should be set to 07H.

6.4.2 EMS Page Register Pointer

Port Address E072H - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
DLT							
16	15	15	13	12	11	10	9

07	06	05	04	03	02	01	00
DLT		POINTER					
8	7						

Signal Name	Default At RSTIN
DLT	0-0
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in Port 6872H, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at Port E872H. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

Bits 15-06 - DLT, Delay Line Test

In the Delay Line Test Mode, these bits represent the state of internal Delay Line signals.

The Delay Line Test is initiated by bit 8 (TDL) in the Test Enable Register at Port Address A872H.

Bits 05-00 - POINTER, EMS Page Register Number

Decimal number, 00 through 39. When programming this field, the hex equivalent 00 through 27H should be used.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF

EMS registers 32 through 39 (decimal) can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See Port E872H description.

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 (decimal) are enabled or disabled as a block. If the EMS_EN field of Port 6872H is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See Port E872H description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872H - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

There are 40 EMS Page Registers accessible through Port E872H. Only EMS registers 32 through 39 are initialized to zero. EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at Port E072H provides the offset location for Port E872H.

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
Bits 14-12	0
P11-P0	0

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at Port 6872H. When EMS_EN equals 11, the EN bit in this register is treated as a one for the lower Page Frame.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MBytes of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16 Kbytes, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128 Kbytes of memory and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MBytes, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOCHRDY to make the transfer.

NOTE

When using external EMS memory with P11 = 1, EN (bit 15) must be 0.

7.0 PORT CHIP SELECT AND WD76C10ALP REFRESH

This section describes refresh control logic peculiar to the WD76C10ALP and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 7-1 identifies the ports, their Chip Select number, I/O address and function.

7.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H - Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF ☆	0
V_REF ☆	0
CBR_REF ☆	0
CBR_SR	0
SCSI	0
PAR	00
PAR_L	0
SER_A	000
SER_AL	0
SER_B	000
SER_BL	0

☆ Featured only in the WD76C10ALP

Bit 15 - M_REF, Memory Refresh Power Down Mode
Featured only in the WD76C10ALP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and M_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value).

M_REF = 1 -
Slow refresh main on-board memory.

Bit 14 - V_REF, Video Refresh Power Down Mode
Featured only in the WD76C10ALP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and V_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS Before RAS Refresh For On-board DRAM
Featured only in the WD76C10ALP

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not.

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 7-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353XH

Bits 10, 09 - PAR, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 7-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BCH - 3BFH

1 0 - PAR chip select at I/O port 378H - 37FH

1 1 - PAR chip select at I/O port 278H - 27FH

Bit 08 - PAR_L, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, Serial Port A Chip Select

The serial port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port A chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port A chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port A chip select at I/O port 2E8H - 2EFH

Bit 04 - SER_AL, Serial A Port Bus Location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B Serial Port B Chip Select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port B chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port B chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port B chip select at I/O port 2E8H - 2EFH

Bit 00 - SER_BL, Serial B Port Bus Location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_BL = 1 -
Serial port B is located on the expansion data bus

7.2 RTC, PVGA, 80287 TIMING, AND DISK CHIP SELECTS

Port Address 2872H - Read and Write

Bits 12 through 07 and Port Address 3072H control the use and location of the Programmable Chip Select.

15	14	13	12	11	10	09	08
RTC_L	FST_VGA	FST_SCSI	EN_PCS	U_MSK	L_MSK		

07	06	05	04	03	02	01	00
PRG_L	HS_HD		P/S	HS_287	LK_PSW	DS_HD	DS FLP

Signal Name	Default At RSTIN
RTC_L	0
FST_VGA	0
FST_SCSI	0
EN_PCS	0
U_MSK	00
L_MSK	00
PRG_L	0
HS HD	000
P/S	000
HS 287	0
LK PSW	0
DS HD	0
DS FLP	0

Bit 15 - RTC_L, Real-Time Clock

The Real-Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

Bit 14 - FST_VGA, Fast VGA Video

The performance of Western Digital Imaging PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital Imaging PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
One wait state I/O cycle to PVGA

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 SCSI Contoller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS, Enable Programmable Chip Select

The Programmable Chip Select logic is selected with chip select 11 and may be disabled or enabled. See Table 7-1.

EN_PCS = 0 -
Disable Programmable Chip Select (Default value)

EN_PCS = 1 -
Enable Programmable Chip Select

Bit 11 - U_MSK, Upper Address Bits Masked

U_MSK determines whether or not the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

U_MSK = 0 -
A15 through A10 are ignored (Default value).

U_MSK = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK, Lower Address Bits Masked

L_MSK determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

L_MSK
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value).

0 0 1 - A00 is ignored.

0 1 0 - A00, A01 are ignored.

0 1 1 - A00, A01, A02 are ignored.

1 0 0 - A00, A02, A03 are ignored, A01 is not ignored, ver. A-F. A00, A01, A02 A03 are ignored, WD76C10A and newer.

Bit 07 - PRG_L, Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable Chip Select is on the expansion bus.

Bit 06 - HS_HD, High Speed Hard Disk Data Transfer Rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with IOCS16 ignored and the WD76C20 hard disk chip select remaining stable.

NOTE

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives WD-AC280, WD-AC140, WD-AC160, WD-AC2120, WD-AP4200, WD-AB130 and WD-AH260.

HS_HD = 0 -
Compatible bus timing enabled (Default value).

HS_HD = 1 -
High speed hard disk accesses enabled.

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 7-1, chip select numbers 08H through 0BH.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value).

P/S = 1 -
Secondary hard disk and Floppy address selected.

Bit 03 - HS_287, Co-processor 80287 High Speed Timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_287 results in 16 bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value).

HS_287 = 1 -
Fast 80287 timing.

Bit 02 - LK_PSW, Prevent Locking Password

Port 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092H bit 3, Lock_Pass can be set (Default value).

LK_PSW = 1 -
Port 092H bit 3, Lock_Pass can not be set.

Bit 01 - DS_HD, Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

7.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072H - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

Signal Name	Default At RSTIN
All signals	None

7.4 CACHE FLUSH

Port Address F872H - Write only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00

Signal Name	Default At RSTIN
All signals	None

7.5 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 7-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

PORT	I/O HEX ADDRESS	CS HEX #	FUNCTION
ROM Chip Select	N/A	00	Chip Select For BIOS ROM
Keyboard Control	060 - 06E Even	01	Chip Select For 8042
80287	00E0 - 00FF	02	Chip Select For Numeric Processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real-Time Clock	070	05	RTC ALE
Real-Time Clock	071	06	RTC Write Strobe
Real-Time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary Address Secondary Address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary Address Secondary Address
Floppy Control Chip Select	3F7 377	0A	Primary Address Secondary Address (Floppy Enabled, HD Disabled)
Floppy And HD Control Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address
Hard Disk Chip Select	3F6 3F7 ① 376 377 ①	OD	Primary Address Secondary Address

TABLE 7-1. I/O ADDRESS AND CHIP SELECT ASSIGNMENTS

PORT	I/O HEX ADDRESS	CS ② HEX #	FUNCTION
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ②	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ②	
Program Chip Select	PROG	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Floppy Chip Select	3F0 - 3F1 370 - 371	18	Primary Address Secondary Address
Floppy Chip Select	3F3 373	19	Primary Address Secondary Address
Reserved		1E	Reserved
Reserved		1F	Reserved

① IDE Hard disk enabled, floppy disabled

② The CS # (Chip Select number) is the decoded value of CS4 - CS0. If the programmed chip select corresponds to any other decode, the programmed chip select is suppressed. If serial port A and B are programmed for the same address, serial port B chip select is suppressed.

TABLE 7-1. I/O PORT ADDRESS CHIP SELECT ASSIGNMENTS cont.

8.0 POWER MANAGEMENT CONTROL

The WD76C10A supports only the PMC inputs and GATE A20 PMC output. It does not support any of the PMC interrupt functions. The WD76C10ALP/LV supports all PMC inputs, output and interrupt functions.

8.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD76C10ALP/LV is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2 and VCPI.

With the WD76C10ALP/LV a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approch to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

System Activity

System activity denotes periods of time in which the system performs useful tasks. The sources Of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ 0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ 8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A progammable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

Using SAM for System Power Management:

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period, SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation, and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order

to do this, control to the CPU must be relinquished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds, and establish a clean breakpoint for Suspending the system.

Advantages of SAM:

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

   - Detection of system activity for extended periods of time, for the purposes of system timeout.
   - Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program.

7. SAM also carries information on DMA activity state. This is used for determining whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at powerup time on Resume.

NOTE

SAM cannot be used for determining when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2.

4

8.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control Register is used to control the power converter from the processor. The WD76C10ALP/LV holds CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT273 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD76C10ALP/LV's internal registers by way of the PMC logic. The keyboard processor starts a local access by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1

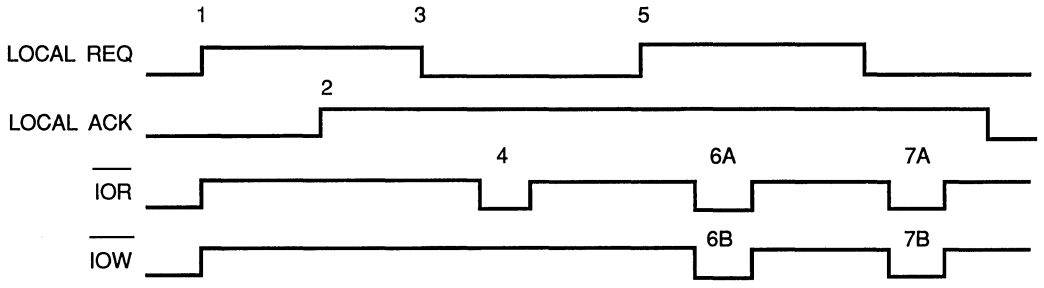
and Table 8-2). The WD76C10ALP/LV arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD76C10ALP/LV asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD76C10ALP/LV on the data bus and drops the LCL_REQ. The WD76C10ALP/LV responds by de-asserting LCL_ACK.

If the opcode specified a register write, data high (D15 through D08) and data low (D07 through D00), bytes are passed to the WD76C10ALP/LV. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD76C10ALP/LV to the keyboard processor.

All special operation registers within the WD76C10ALP/LV may be accessed in this manner without first unlocking the register. See section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 8-1 shows the handshake procedure, followed by the keyboard controller and the WD76C10ALP/LV.

Figures 8-2 and 8-3 represents the power down and power up sequence and control.



1 8042 Requests local data transfer

2 WD76C10ALP/LV returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD76C10ALP/LV reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD76C10ALP/LV Reads high byte

7A WD76C10ALP/LV Read low byte, writes to internal register

FOR READ CYCLE OF WD76C10ALP/LV INTERNAL REGISTER:

6B WD76C10ALP/LV Writes high byte to 8042

7B WD76C10ALP/LV writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	RSV	A15	A14	A13	A12	A11	A10

DIR = 1 - Read register (generates IOW to 8042)

DIR = 0 - Write register (generates IOR to 8042)

FIGURE 8-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

8.3 PMC OUTPUT CONTROL REGISTERS

PMC OUTPUT CONTROL 7:0

Port Address 7072H - Bits 07-00 are Read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Signal Name	Default At RSTIN
All signals	None

Featured only in the WD76C10ALP/LV

PMC OUTPUT CONTROL 15:08

Port Address 7872H - Bits 07-00 are Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

Signal Name	Default At RSTIN
All signals	None

Featured only in the WD76C10ALP/LV

PMC NO.	PMC OUTPUT SIGNAL PORT 7072H	PMC NO.	PMC OUTPUT SIGNAL PORT 7872H
0H	CPU Clock driver enable	8H	User defined
1H	LCD Enable	9H	User defined
2H	Backlight enabled	AH	User defined
3H	LCL_ACK	BH	User defined
4H	LCL_ATN	CH	User defined
5H	Processor powerdown	DH	User defined
6H	Gate A20	EH	User defined
7H	Full powerdown	FH	User defined

TABLE 8-1. PMC OUTPUT SIGNALS

8.4 PMC TIMERS

Port Address 8072H - Read and Write

When no keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 8-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 01 and 00 (BL_MOU) in the RAM Shadow And Write Protect Register at Port Address 6072H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default At RSTIN
BL_TIMEOUT ☆	.0
LCD_TIMEOUT ☆	.0

☆ Featured only in the WD76C10ALP/LV

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 X 5 seconds
FFH - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 X 5 seconds
FFH - LCD enabled

8.5 PMC INPUTS

Port Address 8872H - Read and Write

15	14	13	12	11	10	09	08
PMC_ UPD	EN_ LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD	0
EN_LCL ☆	0
AF7-AF2 ☆	0
IN7-IN0	None

☆ Featured only in the WD76C10ALP/LV

Bit 15 - PMC_UPD, Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (Port Address 7072H) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

Bit 14 - EN_LCL, Enable Local Request
Featured only in the WD76C10ALP/LV

EN_LCL enables the PMCIN 2 to initiate a local access of the WD76C10ALP/LV internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

Bits 13-08 - AF7-AF2, Local Attention Flags
Featured only in the WD76C10ALP/LV

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

Bits 07-00 - IN7-IN0, PMC Inputs 7-0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7 through IN0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 8-2.

8.6 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
Non-maskable Interrupt Enable							

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
Local Attention Enable							

Signal Name	Default At RSTIN
EI7-EI2 ☆	0
EA7-EA2 ☆	0

☆ Featured only in the WD76C10ALP/LV

Bits 15-10 - EI7-EI2, Non-maskable Interrupt enable 7 through 2
Featured only in the WD76C10ALP/LV

EI7 through EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7 through IN_2 in Port 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Non-maskable Interrupt not enabled

EI7-EI2 = 1 -
Non-maskable Interrupt is enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Local Attention Enable
Featured only in the WD76C10ALP/LV

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled

Bits 01, 00 - Not used, state is ignored

4

PMC INPUT NUMBER ①	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER ②
00H	$\overline{\text{TURBO}}$		
01H	PROC_PWR_ GOOD		
02H	LCL_REQ or User Defined	Transition	IF2 or AF2
03H	User Defined	Transition	IF3 or AF3
04H	User Defined	Transition	IF4 or AF4
05H	User Defined	Transition	IF5 or AF5
06H	User Defined	Transition	IF6 or AF6
07H	User Defined	Active Edge	IF7 or AF7

① Port Address 8872H, section 8.5
② Port Address 9072H, section 8.7
Port Address 8872H, section 8.5

TABLE 8-2. PMCIN INPUTS

8.7 NMI STATUS

Port Address 9072H - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
	Non-maskable Interrupt Flags						

Signal Name	Default At RSTIN
IF7-IF2 ☆	0-0

☆ Featured only in the WD76C10ALP/LV

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Non-maskable Interrupt flags 7 through 2
Featured only in the WD76C10ALP/LV

NMI interrupt flags IF7 through IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

Bits 01, 00 - Not used, must be 0

8.8 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN
All signals	None

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

8.9 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the WD76C10A/LP/LV. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

15	14	13	12	11	10	09	08
AMT OUT	DEV		TM7	TS7	S F N M	AUT_ EOI	RA_ EOI

07	06	05	04	03	02	01	00
PLM2 PLM1 PLM0 Priority Level Master			PLS2 PLS1 PLS0 Priority Level Slave			SMM M	SMM S

Signal Name	Default At RSTIN
Bits 15, 12-00	None
Bits 14, 13	00

Bit 15 - AMTOUT, Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

Bit 14, 13 - DEV, Device

DEV identifies the device as WD76C10A/LP/LV or WD7710 and is used in conjunction with VER at Port Address 9872H and SVER at Port Address A872H. DEV, VER and SVER are defined in Table 9.1.

Bit 12 - TM7, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 11 - TS7, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 10 - SFNM, Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD76C10A/LP/LV does not require SFNM for the slave interrupt controller and ignores its state.

Bit 09 - AUT_EOI, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD76C10A/LP/LV does not require AUT_EOI for the slave interrupt controller and ignores its state.

Bit 08 - RA_EOI, Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7 through 5 of OCW2). The WD76C10A/LP/LV does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

Bits 07-05 - PLM2-PLM0, Priority Level Master

PLM2-PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bits 04-02 - PLS2-PLS0, Priority Level Slave

PLS2-PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bit 01 - SMMM, Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

Bit 00 - SMMS, Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

8.10 PORT 70H SHADOW REGISTER

Port Address E472H - Read only

Bits 15 and 14 provide the information required to generate software delays, without incurring the operating system traps that result from accessing I/O Port 0061H in virtual 86 mode. Port 70H Shadow Register may be accessed without first being unlocked, making it possible to read bits 15 and 14 frequently for generating time delays.

Bits 13 and 12 provide interrupt and DMA status information required to determine when the processor may be placed in Sleep Mode.

Bits 07 through 00 provide a means of determining the contents of the write only Real-Time Clock Address Register at Port 0070H, described in section 5.8.1. Since it is necessary to access the Real-Time Clock CMOS RAM during suspend and resume operations, the Port 70H Shadow Register makes it possible to restore the Real-Time Clock to the state in which it was before entering Suspend Mode.

15	14	13	12	11	10	09	08
CLK 32K	REF DT	INT RQ	NO DMA	Reserved			

07	06	05	04	03	02	01	00
I/O Port 0070H Shadow							
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
Bits 11-08	0-0
All other signals	None

Bit 15 - CLK32K

CLK32K is PDREF (at input pin 117) divided by two. CLK32K may be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 µs period and a 50% duty cycle.

Bit 14 - REFDT, Refresh Detect

REFDT changes state on each refresh and is the same as bit 4 in Port Address 0061H described in section 5.9.

Bit 13 - INTRQ, Interrupt Request

This is the state of the INTRQ signal at output pin 55.

Bit 12 - NODMA, No DMA

NODMA = 0 -
A DMA or Bus Master Cycle has occurred within the last 61 µs

NODMA = 1 -
A DMA or Bus Master Cycle has not occurred within the last 30.5 µs

Bits 11-08 - Reserved. Currently defaults to 0000, but is subject to change.

Bit 07-00 -
D_NMI, Disable Non-maskable Interrupt
RTCA6-RTCA0, Real-Time Clock Address

Bits 07 through 00 represent the state of the Disable Non-maskable Interrupt and Real-Time Clock Address as set by the last write to Port Address 0070H.

8.11 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13-11, 08-00 Read and Write
Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in section 8.12.

15	14	13	12	11	10	09	08
IRR AE	CB12	AM TM	ACT LCH	IND ET	ACT AFT	ACT BEF	AM EN

07	06	05	04	03	02	01	00
Coarse Timeout Count AMC7 AMC6 AMC5 AMC4				Fine Timeout Count AMC3 AMC2 AMC1 AMC0			

Signal Name	Default At RSTIN
IRRAE	0
CB12	None
AMTM	0
ACTLCH	None
INDET	None
ACTAFT	None
ACTBEF	None
AMEN	0
AMC7-AMC0	0-0

Bit 15 - IRRAE, Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

Bit 14 - CB12, Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

Bit 13 - AMTM, Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

Bit 12 - ACTLCH, Activity Latch

This latch is always enabled, regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

Bit 11 - INDET, Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07-00) to be reached.

NOTE

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

Bit 10 - ACTAFT, Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -

Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

Bit 09 - ACTBEF, Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -

Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -

Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC7-AMC0 (bits 07-00). It would be necessary for the routine to clear the software counter if ACTBEF were set, since there would have been no activity only for the period of time programmed in AMC7-AMC0.

Bit 08 - AMEN, Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -

Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -

Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected, the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM7-ACM0, INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

Bits 07-04 - AMC7-AMC4, Activity Monitor Counter Coarse

AMC7-AMC4 establish the timeout values from 64 seconds to 16 minutes in 64 second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC	7	6	5	4	
	0	0	0	0	- 0 seconds
	0	0	0	1	- 1 minute, 4 seconds
	0	0	1	0	- 2 minutes, 8 seconds
	0	0	1	1	- 3 minutes, 12 seconds
	0	1	0	0	- 4 minutes, 16 seconds
	0	1	0	1	- 5 minutes, 20 seconds
	0	1	1	0	- 6 minutes, 24 seconds
	0	1	1	1	- 7 minutes, 28 seconds
	1	0	0	0	- 8 minutes, 32 seconds
	1	0	0	1	- 9 minutes, 36 seconds
	1	0	1	0	- 10 minutes, 40 seconds
	1	0	1	1	- 11 minutes, 44 seconds
	1	1	0	0	- 12 minutes, 48 seconds
	1	1	0	1	- 13 minutes, 52 seconds
	1	1	1	0	- 14 minutes, 56 seconds
	1	1	1	1	- 16 minutes, 0 seconds

Bits 03-00 - AMC3-AMC0, Activity Monitor Counter Fine

AMC3-AMC0 establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC	3	2	1	0	
	0	0	0	0	- 0 milliseconds
	0	0	0	1	- 7.8 milliseconds
	0	0	1	0	- 15.6 milliseconds
	0	0	1	1	- 23.4 milliseconds
	0	1	0	0	- 31.3 milliseconds
	0	1	0	1	- 39.1 milliseconds
	0	1	1	0	- 46.9 milliseconds
	0	1	1	1	- 54.7 milliseconds
	1	0	0	0	- 62.5 milliseconds
	1	0	0	1	- 70.3 milliseconds
	1	0	1	0	- 78.1 milliseconds
	1	0	1	1	- 85.9 milliseconds
	1	1	0	0	- 93.8 milliseconds
	1	1	0	1	- 101.6 milliseconds
	1	1	1	0	- 109.4 milliseconds
	1	1	1	1	- 117.2 milliseconds

NOTE

The fine timeout delay (AMC3-AMC0) is added to the coarse timeout delay (AMC7-AMC4) to obtain the total timeout delay.

8.12 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

15	14	13	12	11	10	09	08
PCSM	PMCILS	PMCIS2	PMCIS1	PMCIS0	NMIM	HDDM	COPM

07	06	05	04	03	02	01	00
IMS1	IMS0	IRR8M	IRR7M	IRR0M	ISR8M	ISR7M	ISR0M

Signal Name	Default At RSTIN
All signals	0

Bit 15 - PCSM, Programmable Chip Select Mask

PCSM = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD76C10ALP/LV are considered activity.

PCSM = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD76C10ALP/LV are ignored.

Bit 14 - PMCILS, Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13-11, PMCIS2-0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

Bits 13-11 - PMCIS2-PMCIS0, Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

NOTE

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

PMCIS 2	1	0		
0	0	0	-	PMC input 2 selected
0	0	1	-	PMC input 3 selected
0	1	0	-	PMC input 4 selected
0	1	1	-	PMC input 5 selected
1	0	0	-	PMC input 6 selected
1	0	1	-	PMC input 7 selected
1	1	0	-	Reserved
1	1	1	-	Disabled, no PMC inputs checked

Bit 10 - NMIM, Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

Bit 9 - HDDM, Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

Bit 8 - COPM, Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. For an 80286 system, this is I/O address range 00F8H-00FFH. For an 80386SX system, this is when A23 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

Bits 07, 06 - IMS1-0, Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS1-0 provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

IMS 1 0
0 0 - IRQ5 masked
0 1 - IRQ10 masked
1 0 - IRQ11 masked
1 1 - IRQ15 masked

Bit 05 - IRR8M, Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

Bit 04 - IRR7M, Interrupt Request Register 7 Mask

IRR7M = 0 -
Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -
Parallel Port or Spurious Interrupt (IRR7) is ignored.

Bit 03 - IRR0M, Interrupt Request Register 0 Mask

IRR0M = 0 -
Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -
Time Of Day Interrupt (IRR0) is ignored.

Bit 02 - ISR8M, Interrupt Service Register 8 Mask

ISR8M = 0 -
Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -
Real-Time Clock Interrupt (ISR8) is ignored.

Bit 01 - ISR7M, Interrupt Service Register 7 Mask

ISR7M = 0 -
Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -
Parallel Port or Spurious Interrupt (ISR7) is ignored.

Bit 00 - ISR0M, Interrupt Service Register 0 Mask

ISR0M = 0 -
Time Of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -
Time Of Day Interrupt (ISR0) is ignored.

8.13 SAVE AND RESUME

When the WD76C10ALP/LV is in the Save And Resume Mode, it typically draws less than 500 µA. Figures 8-2 and 8-3 illustrate the steps that the WD76C10ALP/LV goes through during power down and power up.

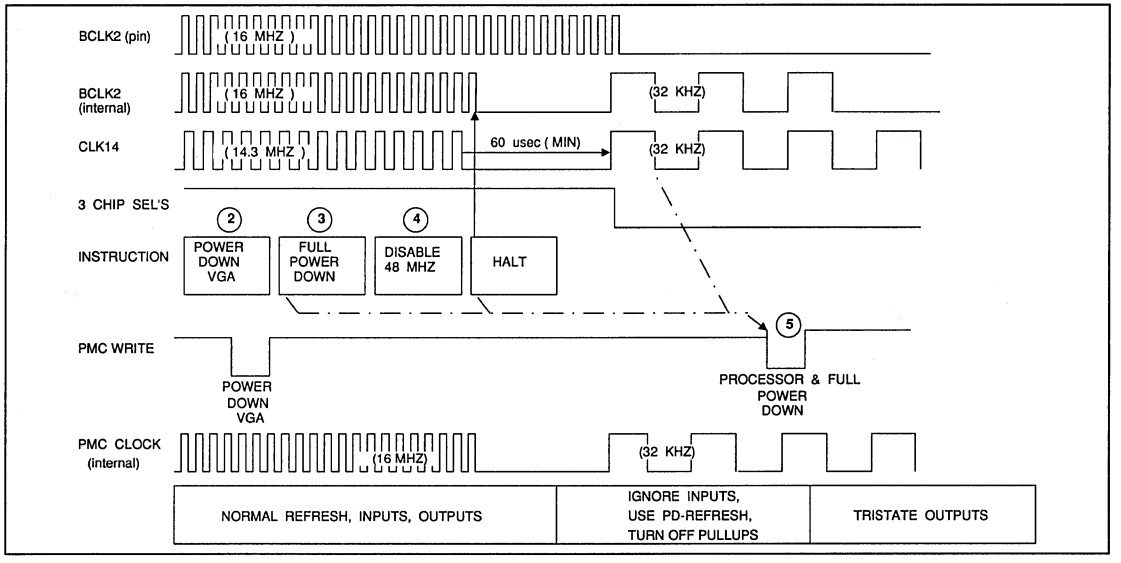


FIGURE 8-2. POWER DOWN

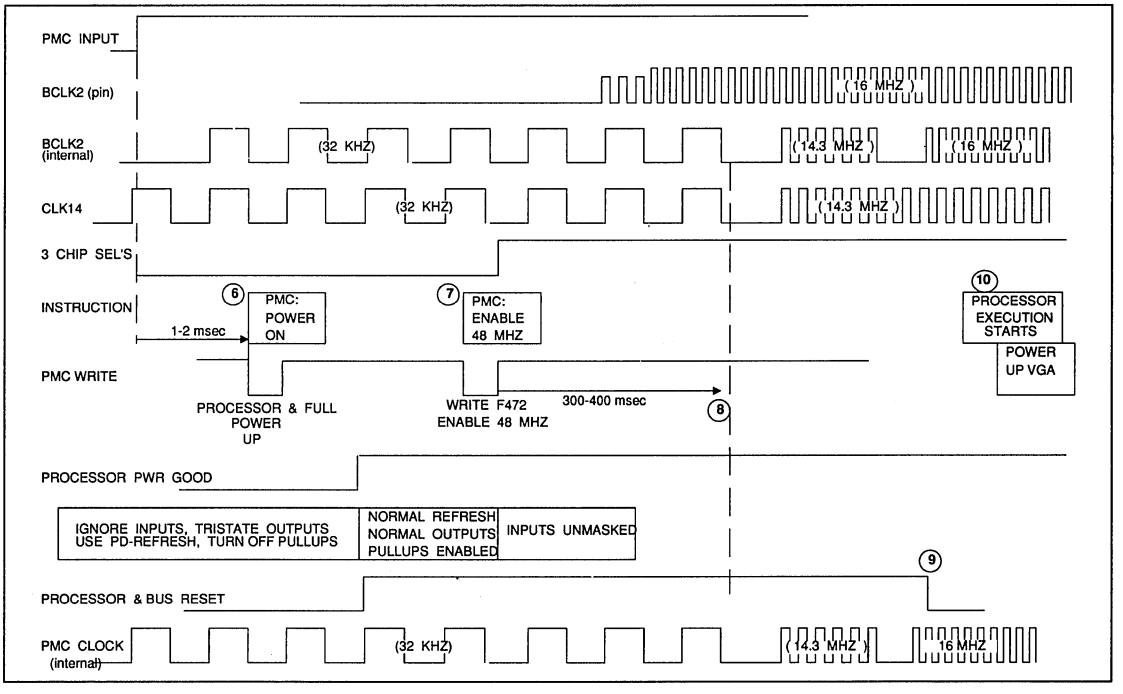


FIGURE 8-3. POWER UP

9.0 DIAGNOSTIC MODE

Simultaneously asserting MASTER, MEMR and MEMW while RSTIN is asserted, causes all output pins to become tristated. The outputs remain tristated if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted and any of the MASTER, MEMR or MEMW are not asserted. This all output tristate mode allows an in-circuit board tester to drive the System Controller's output pins.

9.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

15	14	13	12	11	10	09	08
VER			CLK_ TST	REF_ MAS	AUT_ A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default At RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
AUT_A20	0
Bit 09	None
CLK_SW	0
SX	None
DS	0
DIAG	0-0

Bits 15, 14 ,13 - VER, Version Number

The initial version number is 000 and is incremented with every mask change. If version seven is read, it is necessary to read the device type (DEV) from Port Address D472H, then the secondary version number (SVER) from Port Address A872H. See Table 9-1.

Version

000 WD76C10 Initial Rev. A
001 WD76C10 Rev. B
010 WD76C10 Rev. C
011 WD76C10 Rev. D
100 WD76C10 Rev. E
101 WD76C10 Rev. F
110 WD76C10A Rev. A
111 Extended Versions

PORT ADDRESS D472H DEVICE			PORT ADDRESS A872H SECONDARY VERSION				
Bits 14	13	Device	Bits 15	14	13	12	Version
0	0	WD76C10A	0	0	0	0	A
0	1	WD7710	0	0	0	1	B
1	0	Reserved	0	0	1	0	C
1	1	Reserved	-	-	-	-	
			1	1	1	1	P

TABLE 9-1. EXTENDED VERSION NUMBER

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - AUT_A20, Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 8-1).

AUT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

AUT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX Processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, Diagnostic Function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 9-2. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

4

DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	"
00010	Reserved	10010	"
00011	"	10011	"
00100	"	10100	"
00101	"	10101	"
00110	"	10110	"
00111	"	10111	"
01000	"	11000	"
01001	"	11001	"
01010	"	11010	"
01011	"	11011	"
01100	"	11100	"
01101	"	11101	"
01110	"	11110	"
01111	"	11111	"

TABLE 9-2. DIAGNOSTIC TESTS

9.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default At RSTIN
Bits 15-08	None
LAT	0
DL	0
DELAY	None

Bit 07 - LAT, Latch Output Strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

9.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15-10 Read only
Bits 09-00 Read and Write

The test function bits 07-03 are for factory use only.

15	14	13	12	11	10	09	08
SVER				BF40	BC40	RSVD	TDL

07	06	05	04	03	02	01	00
OLD IHLD	BFC 3	BIST 3	BFC 40	BIST 40	EN_ PLD	DISFA	EN_ LVL

Signal Name	Default At RSTIN
All signals	0-0

Bits 15-12 - SVER, Secondary Version Number.

Refer to VER at Port Address 9872H and Table 9-1.

Bit 11 - BF40, EMS Register Self Test Status

Bit 10 - BC40, EMS Register Self Test Status

Bit 09 - RSVD, Reserved for future use.

Bit 08 - TDL, Test Delay Line.

Bit 07 - OLD_IHLD,

OLD_IHLD = 0 -
SX test not enabled

OLD_IHLD = 1 -
SX test enabled

Bit 06 - BFC3,

BFC3 = 0 -
DMA register file test

BFC3 = 1 -
DMA register file test

Bit 05 - BIST3,

BIST3 = 0 -
DMA register file test

BIST3 = 1 -
DMA register file test

Bit 04 - BFC40,

BFC40 = 0 -
EMS mapping RAM

BFC40 = 1 -
EMS mapping RAM

Bit 03 - BIST40,

BIST40 = 0 -
EMS mapping RAM

BIST40 = 1 -
EMS mapping RAM

Bit 02 - EN_PLD, Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23 through A00, and on processor data lines D15 through D00.

Bit 01 - DISFA, Disable First Access

DISFA = 0 -
First access Page Mode cycles are not disabled.

DISFA = 1 -
First access Page Mode cycles are disabled. Page Miss cycles occur instead.

Bit 00 - EN_LVL, Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of Edge or Level sensed interrupts.

9.4 TEST STATUS REGISTER

Port Address DC72H - Read only

For factory use only.

15	14	13	12	11	10	09	08
Delay Line Status CAL	MED	SLOW	DLT6	DLT5	DLT4	DLT3	DLT2

07	06	05	04	03	02	01	00
DLT1	DLT0	BF34	BF33	BF32	BF31	BF30	BC

Signal Name	Default At RSTIN
All signals	None

Bit 15 - CAL, Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

Bits 14, 13 - MED, SLOW, Medium and Slow

These bits provide information regarding the output buffer strength.

MED	SLOW	
0	0	- Output buffers are set to low strength (fast WD76C10A).
0	1	- Invalid
1	0	- Output buffers are set to medium strength (medium speed WD76C10A).
1	1	- Output buffers are set to full strength (slow WD76C10A).

Bits 12-06 - DLT6-DLT0,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD76C10A.

Bits 05-01 - BF34-BF30,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD76C10A.

Bit 00 - BC

This bit provides information about internal nodes and are for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD76C10A.

10.0 DC ELECTRICAL SPECIFICATIONS

This section provides the DC Operating Characteristics for the WD76C10A/LP. The parameters for the WD76C10ALV that differ from these are marked with an * and appear in the appendix.

10.1 MAXIMUM RATINGS

Supply Voltage (Vcc) with respect to Vss (ground) . . . . . Vcc - Vss ≤ 7.0 Volts

Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to Vdd +0.3 Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)

Power Dissipation . . . . . 600 mW *

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

10.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
Vcc = +5V ±.25V (5%) for WD76C10A and WD76C10ALP *

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tristate And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High *	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current *		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD76C10ALP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 10-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-30	-110	µA	Not suspend and resume mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

M/IO, PEACK, NPERR, NPBUSY, S0, S1, NPRST, CPURES, DPH, DPL

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-30	-110	mA	Not processor down or suspend mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

PMCIN, IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, BHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-30	-110	mA	Not suspend mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

CASL3, CASL2, CASH3, SDT/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-30	-110	mA	RESET IN = 0

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR PINS WITH INTERNAL PULLDOWNS:

A23-A0, D15-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current *	-30	-110	µA	Processor power down or suspend mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage *	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage *	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage *		.4	V	IOUT = 2 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage *	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage *		.4	V	IOUT = 4 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

IOR, IOW, MEMR, MEMW, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage *		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:

REFRESH

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage *		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

11.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into three major categories: Memory Timing, section 11.1, AT Bus Timing, section 11.2 and Processor Timing, section 11.3.

This section provides the AC Operating Characteristics for the WD76C10A/LP. The parameters for the WD76C10ALV that differ from these are marked with an * and appear in the appendix.

Table 11-1 lists the timing tables and figures, and their section location.

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
11-3		80286 - Page Mode Memory Timing	11.1.1
	11-1	80286 - Page Mode First Access Read/Write	11.1.1
	↕		
	11-6	80286 - Page Mode Read Hit Followed By Write Hit	11.1.1
11-4		80286 - Non-Page Mode 00 Memory Timing	11.1.2
	11-7	80286 - Non-Page Mode 00 1 Wait State Write	11.1.2
	11-8	80286 - Non-Page Mode 00 1 Wait State Read	11.1.2
	11-9	80286 - Non-Page Mode 00 2 Wait States Read After Write	11.1.2
11-5		80286 - Non-Page Mode 01 Memory Timing	11.1.3
	11-10	80286 - Non-Page Mode 01 0 Wait State Write	11.1.3
	11-11	80286 - Non-Page Mode 01 0 Wait State Read	11.1.3
11-6		80386SX - Page Mode Memory Timing	11.1.4
	11-12	80386SX - Page Mode, First Access Read/Write	11.1.4
	↕		
	11-17	80386SX - Page Mode, Write Miss Following A Write	11.1.4
11-7		80386SX - Non-Page Mode 00 And Mode 01	11.1.5
	11-18	80386SX - Non-Page Mode 00 1 Wait State Read	11.1.5
	↕		
	11-21	80386SX - Non-Page Mode 00 1 Wait State Read	11.1.5
11-8		CPU Initiated AT Bus Cycles	11.2.1
	11-22	AT Bus I/O Or Memory Read: 8-Bit, Default Timing	11.2.1
	↕		
	11-31	AT Bus I/O Or Memory Write: 16-Bit, Default Timing	11.2.1
11-9		Entering The AT Bus	11.2.2
	11-32	80286 CPU - Asysnchronous CPUCLK To SYSCLK, BREQ Delay = 1/2 Clock	11.2.2
	↕		
	11-37	80386SX CPU - Synchronous CPUCLK To SYSCLK	11.2.2
11-10		Exiting The AT Bus	11.2.3
	11-38	Synchronous AT Bus Cycle Completion, AT Bus Clock = 1/2 CPUCLK	11.2.3
	↕		
	11-41	Asynchronous AT Bus Cycle Completion, BAK_DEL = 0 Or +0.5 AT Bus Cycles	11.2.3
11-11		DMA Entering And Exiting The AT Bus	11.2.4
	11-42	Basic DMA Cycle, Default Timing	11.2.4
	11-43	DMA Cycle, 8-Bit I/O To On-board Memory	11.2.4
	11-44	DMA Cycle, On-board Memory To 8-Bit I/O	11.2.4
11-12		AT Bus Master Cycle	11.2.5
	11-45	AT Bus Master, Bus Acquisition/Release	11.2.5
	11-46	AT Bus Master, Write To On-board Memory	11.2.5
	11-47	AT Bus Master, Read From On-board Memory	11.2.5
11-13		AT Bus Refresh Cycle, Default Timing	11.2.5
	11-48	AT Bus Refresh Cycle, Default Timing	11.2.5

TABLE 11-1. TIMING FIGURE/TABLE NUMBERS

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
11-14		80286 CPU TIMING	11.3
	11-49	80286 - CPURES AND NPRST DURING POWER UP	11.3
	↕		
	11-54	80286 - MISCELLANEOUS TIMING	11.3
11-15		80386SX CPU TIMING	11.3
	11-55	80386SX - CPURES AND NPRST DURING POWER UP	11.3
	↕		
	11-62	80386SX - OUTPUT DELAY TIMING	11.3

TABLE 11-1. TIMING FIGURE/TABLE NUMBERS cont.

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
CPURES	50 pF	NPRST	50 pF	$\overline{BHE}$	50 pF
W/$\overline{R}$	50 pF	ALE	50 pF	$\overline{DEN1}$, $\overline{DEN0}$	50 pF
$\overline{SDEN}$	50 pF	DT/$\overline{R}$	50 pF	SDT/$\overline{R}$	50 pF
MXCTL2 - 0	50 pF	DACKEN	50 pF	$\overline{CSEN}$	50 pF
$\overline{LOMEG}$	50 pF	SPKR	50 pF	$\overline{READY}$	50 pF
$\overline{HOLD}$	50 pF	INTRQ	50 pF	NMI	50 pF
$\overline{BUSYCPU}$	50 pF	EPEREQ	50 pF	A23 - A0	60 pF
CPUCLK	70 pF	SYSCLK	75 pF	$\overline{CASH3}$ - $\overline{0}$ *	75 pF
$\overline{CASL3}$ - $\overline{0}$	75 pF	D15 - D0	100 pF	DPH	100 pF
DPL	100 pF	$\overline{RAS3}$ - $\overline{RAS0}$	150 pF	$\overline{IOW}$	200 pF
$\overline{IOR}$	200 pF	$\overline{MEMW}$	200 pF	$\overline{MEMR}$	200 pF
LA20	200 pF	SA0	200 pF	AEN	200 pF
BALE	200 pF	$\overline{REFRESH}$	200 pF	RA10 - RA0 *	350 pF

TABLE 11-2. SIGNAL LOADING

11.1 MEMORY TIMING

Sections 11.1.1 through 11.1.5 present the memory timing for Page Mode and Non-Page Mode, for the 80286 and 80386SX processors.

Categories are grouped as follows:

80286
- Page Mode
- Non-Page Mode 00
- Non-Page Mode 01

80386SX
- Page Mode
- Non-Page Mode 00 and 01

Mnemonics used in the timing diagrams and tables are defined as:

TC - Command Cycle
TW - Wait State Cycle
TS - Status Cycle
WNRDRAM - Write Not Read DRAM (W/$\overline{R}$ pin 119).

11.1.1 80286 Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T220	Processor address to RAM address valid, Page Hit	32	30
T221	CPUCLK fall to $\overline{CAS}$ fall, 2.5 CLK CAS	36	34
T222	CPUCLK rise to $\overline{CAS}$ rise	29	27
T223	CPUCLK rise to CAS fall, 2.0 CLK CAS	30	26
T224	Processor data to parity valid	25	22
T225	CPUCLK fall to RAM address valid, Page Miss	39	36
T226	CPUCLK fall to WNRDRAM rise	34	31
T227	CPUCLK rise to RAS fall, first access	28	26
T228	CPUCLK fall to column address valid	44	41
T229	CPUCLK fall to WNRDRAM fall	34	31
T232	CPUCLK fall to $\overline{RAS}$ rise, Page Miss	29	27
T233	CPUCLK rise to $\overline{RAS}$ fall, Page Miss	28	26
T234	CPUCLK rise to $\overline{READY}$ rise	24	22
T235	CPUCLK rise to READY fall	24	22

TABLE 11-3. 80286 - PAGE MODE MEMORY TIMING

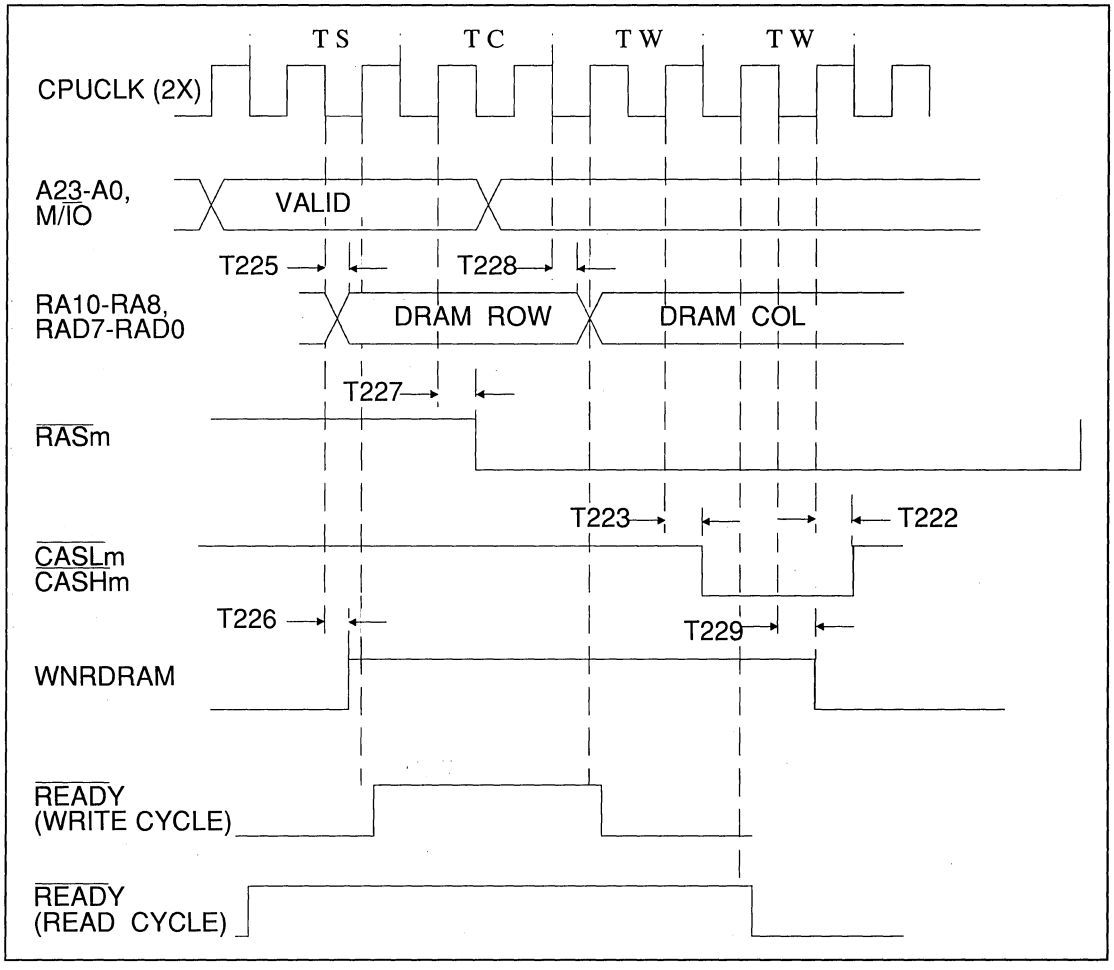


FIGURE 11-1. 80286 - PAGE MODE FIRST ACCESS READ/WRITE

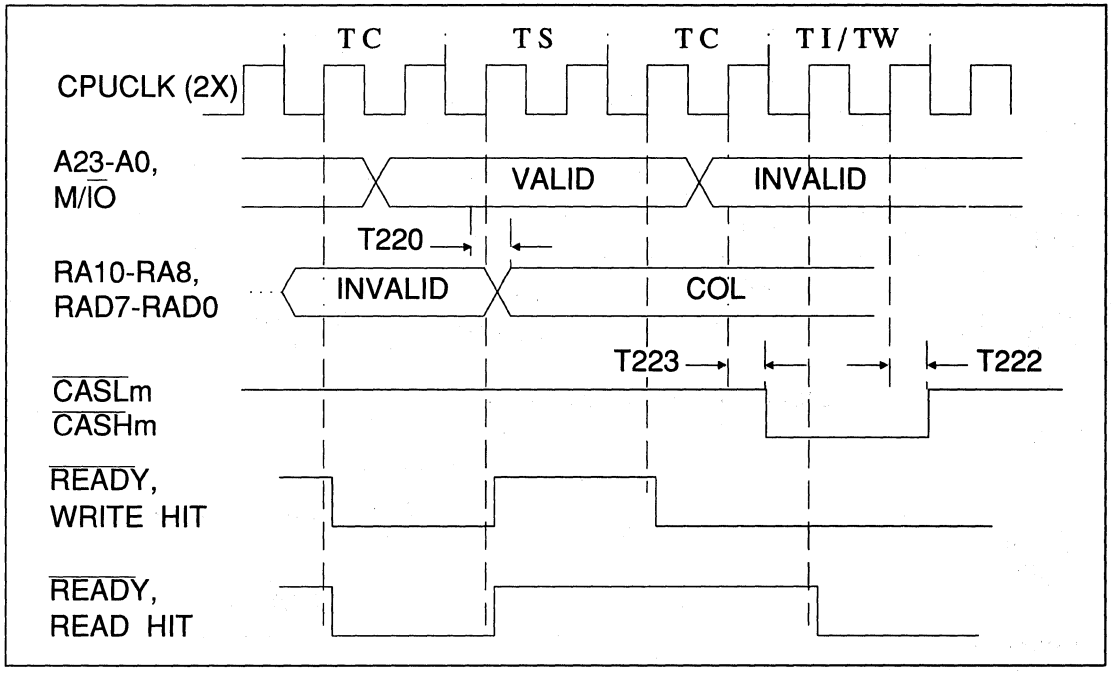


FIGURE 11-2. 80286 - PAGE MODE READ CYCLE FOLLOWED BY A PAGE HIT

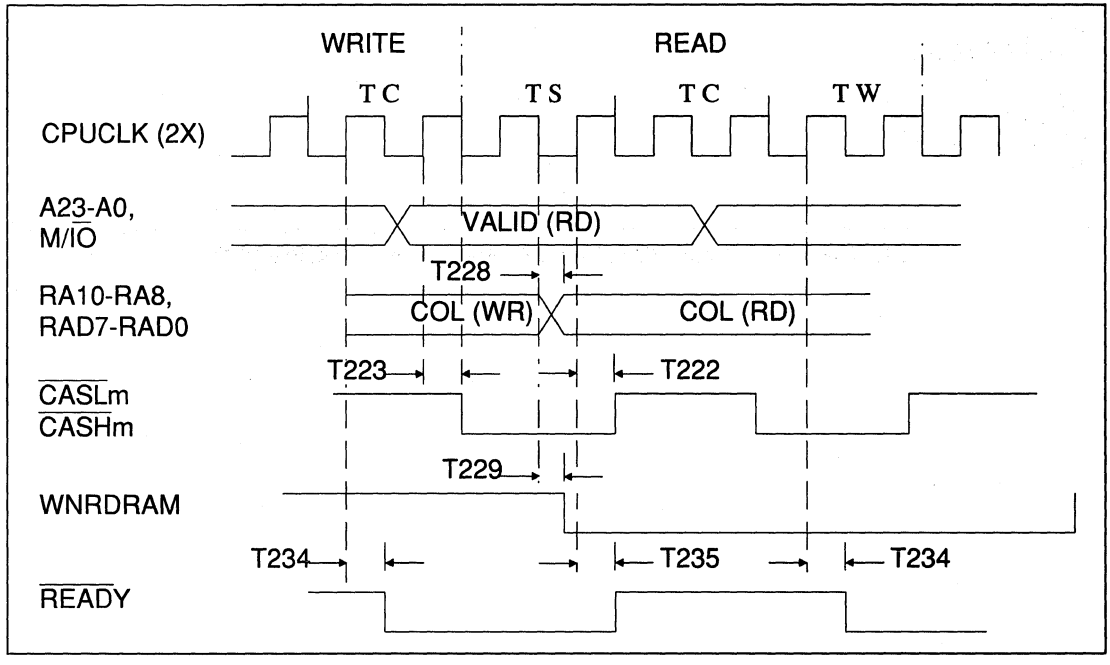


FIGURE 11-3. 80286 - PAGE MODE READ AFTER WRITE

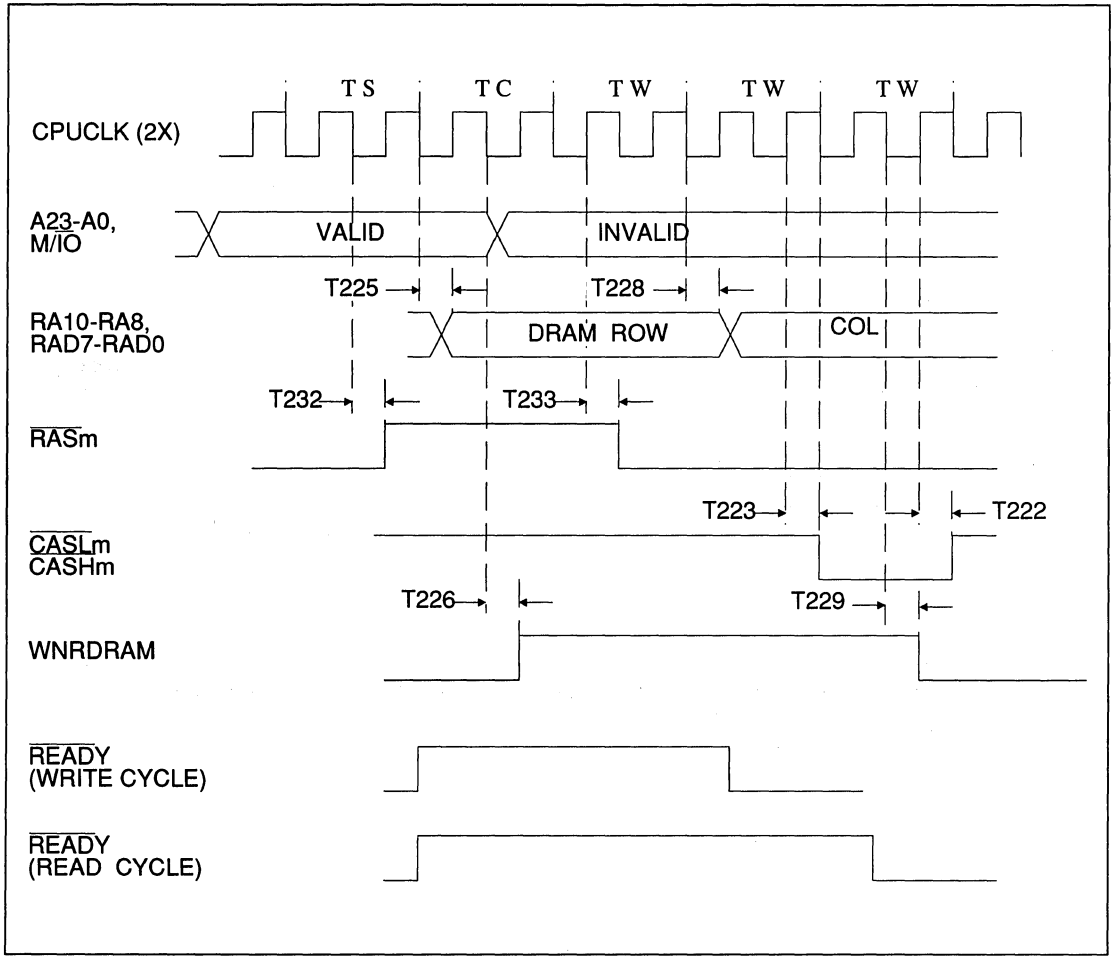


FIGURE 11-4. 80286 - PAGE MODE, PAGE MISS READ/WRITE

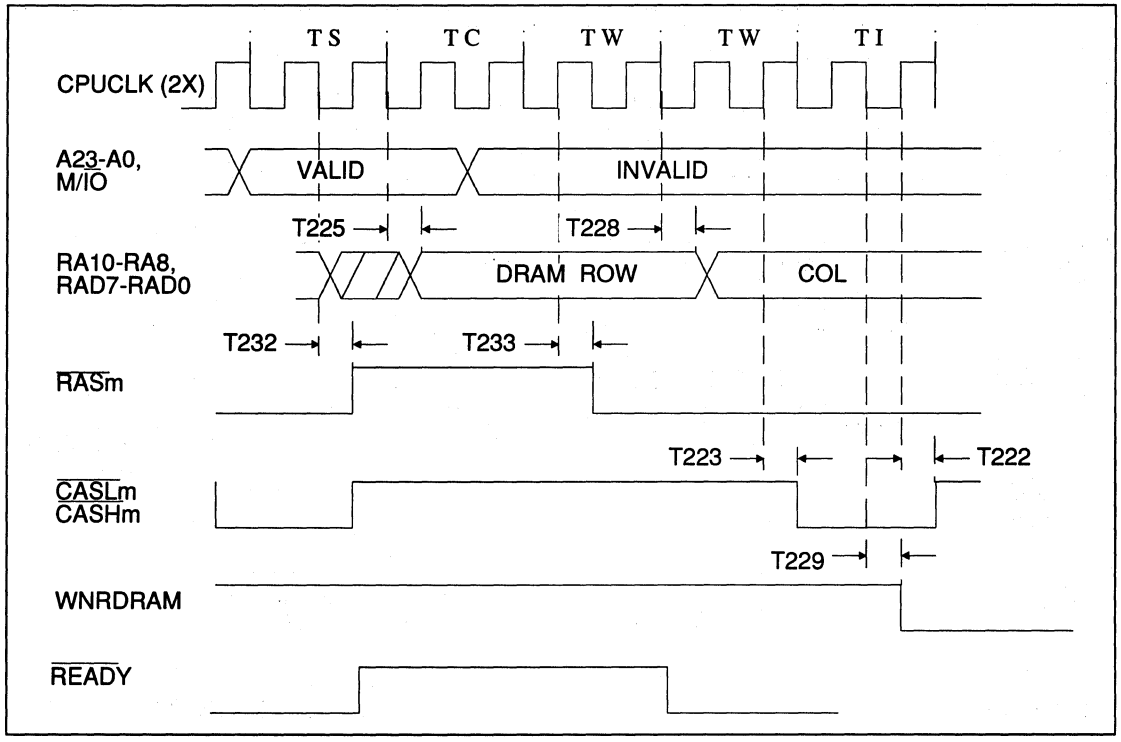


FIGURE 11-5. 80286 - PAGE MODE, WRITE MISS FOLLOWING WRITE

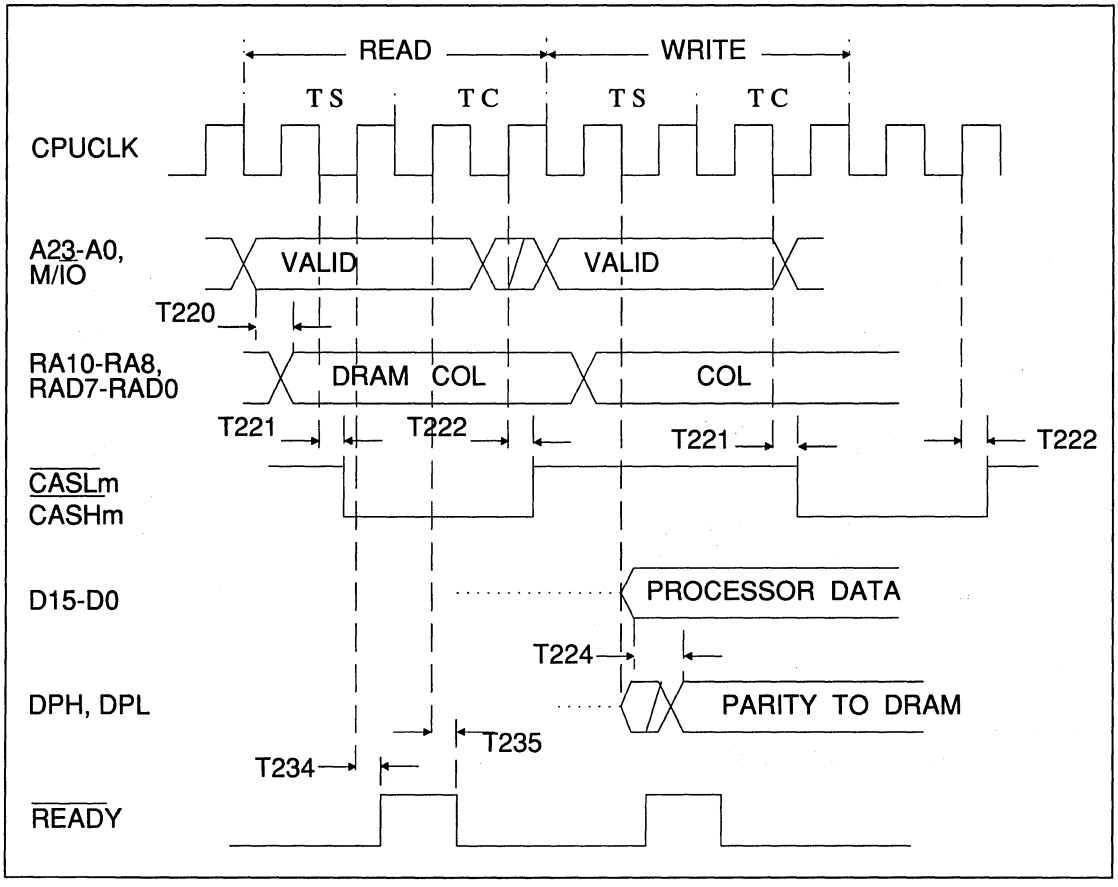


FIGURE 11-6. 80286 - PAGE MODE READ HIT FOLLOWED BY A WRITE HIT

11.1.2 80286 Non-Page Mode 00 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T234	See Table 11-3		
T235	See Table 11-3		
T252	CPUCLK fall to $\overline{CAS}$ rise	33	30
T255	CPUCLK fall to $\overline{RAS}$ fall	35	32
T270	CPUCLK fall to ROW address	46	42
T271	CPUCLK fall to $\overline{CAS}$ fall	37	34
T273	CPUCLK fall to WNRDRAM fall	33	31
T274	CPUCLK fall to WNRDRAM rise	33	31
T275	Data holding tristate. ①	12	12
T276	Clock fall to parity valid	30	27
T277	CPUCLK fall to RAS rise	30	28
T278	CPUCLK fall to COLUMN address valid	41	38
T279	Processor address to ROW address	32	30

① Tristate times are not tested. Timing specifications are derived from simulation.

TABLE 11-4. 80286 - NON-PAGE MODE 00 MEMORY TIMING

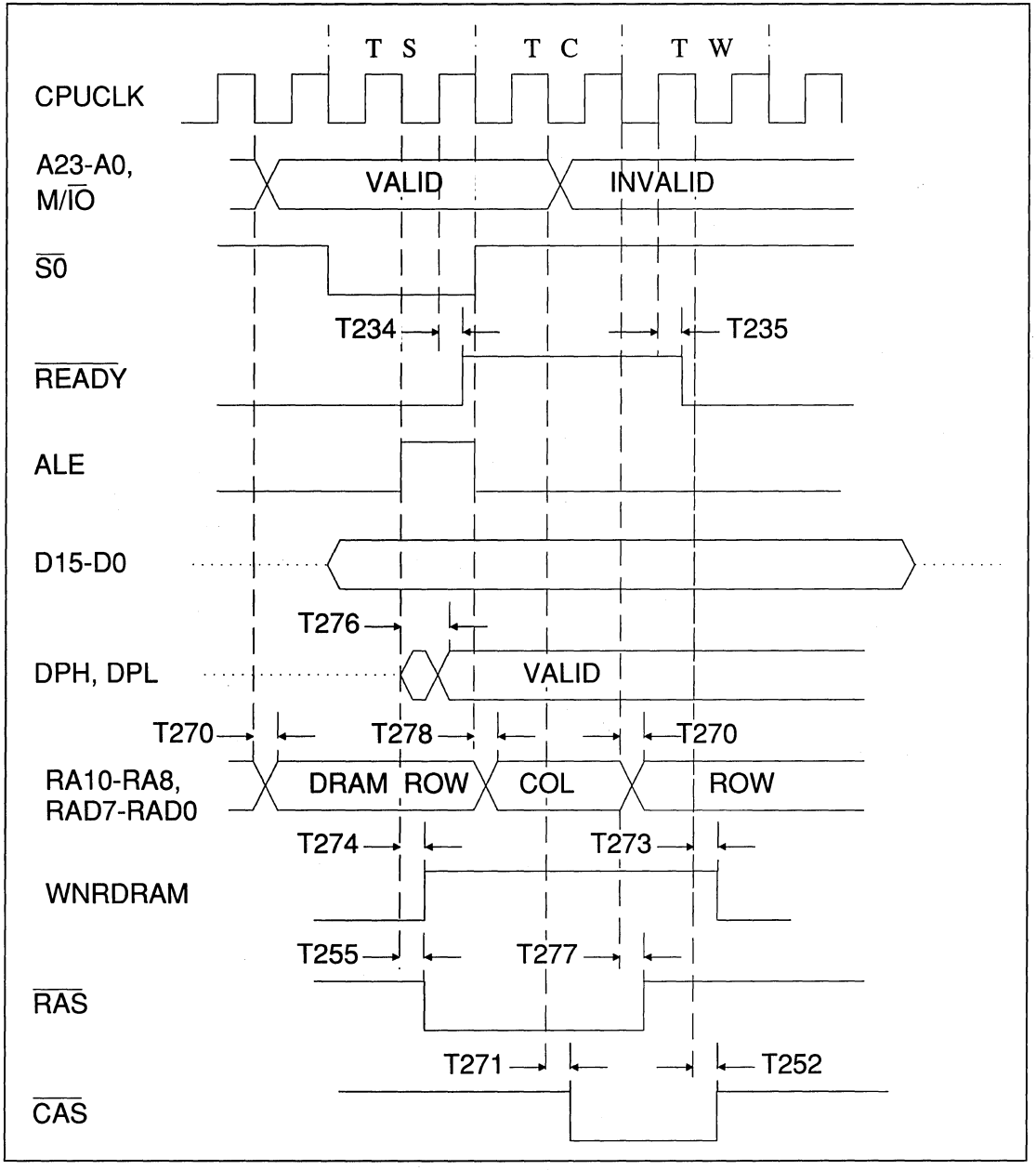


FIGURE 11-7. 80286 - NON-PAGE MODE 00, 1 WAIT STATE WRITE (4072H = 0001)

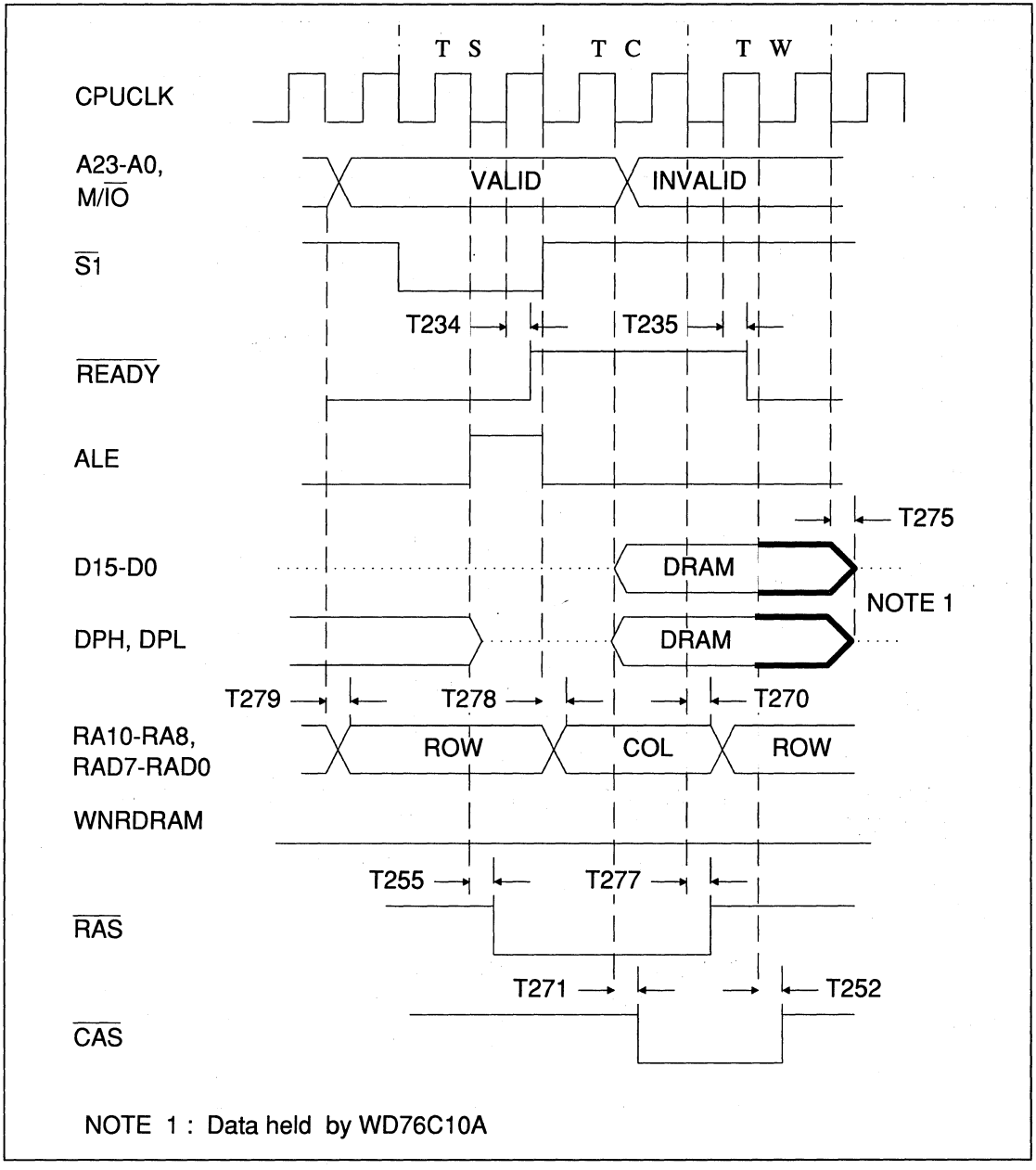


FIGURE 11-8. 80286 - NON-PAGE MODE 00, 1 WAIT STATE READ (4072H = 0001)

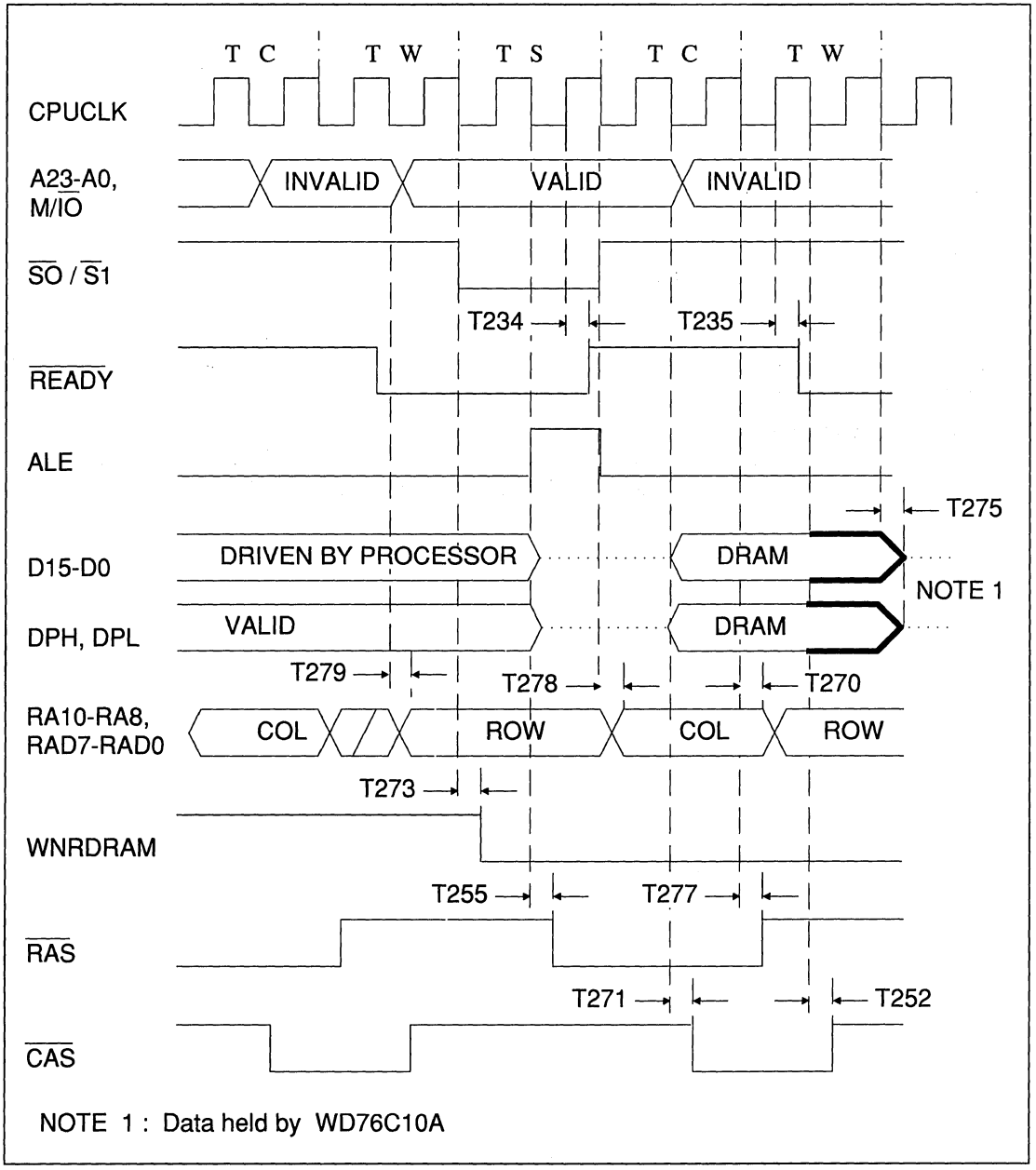


FIGURE 11-9. 80286 - NON-PAGE MODE MODE 00, 2 WAIT STATES READ AFTER WRITE (4072H = 0001)

11.1.3 80286 Non-Page Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T224	See Table 11-3		
T234	See Table 11-3		
T235	See Table 11-3		
T252	See Table 11-4		
T253	CPUCLK fall to WNRDRAM fall	34	31
T254	CPUCLK fall to WNRDRAM rise	34	31
T255	See Table 11-4		
T257	CPUCLK rise to $\overline{RAS}$ rise	35	32
T258	CPUCLK rise to COLUMN address valid	44	40
T276	See Table 11-4		

TABLE 11-5. 80286 - NON-PAGE MODE 01 MEMORY TIMING

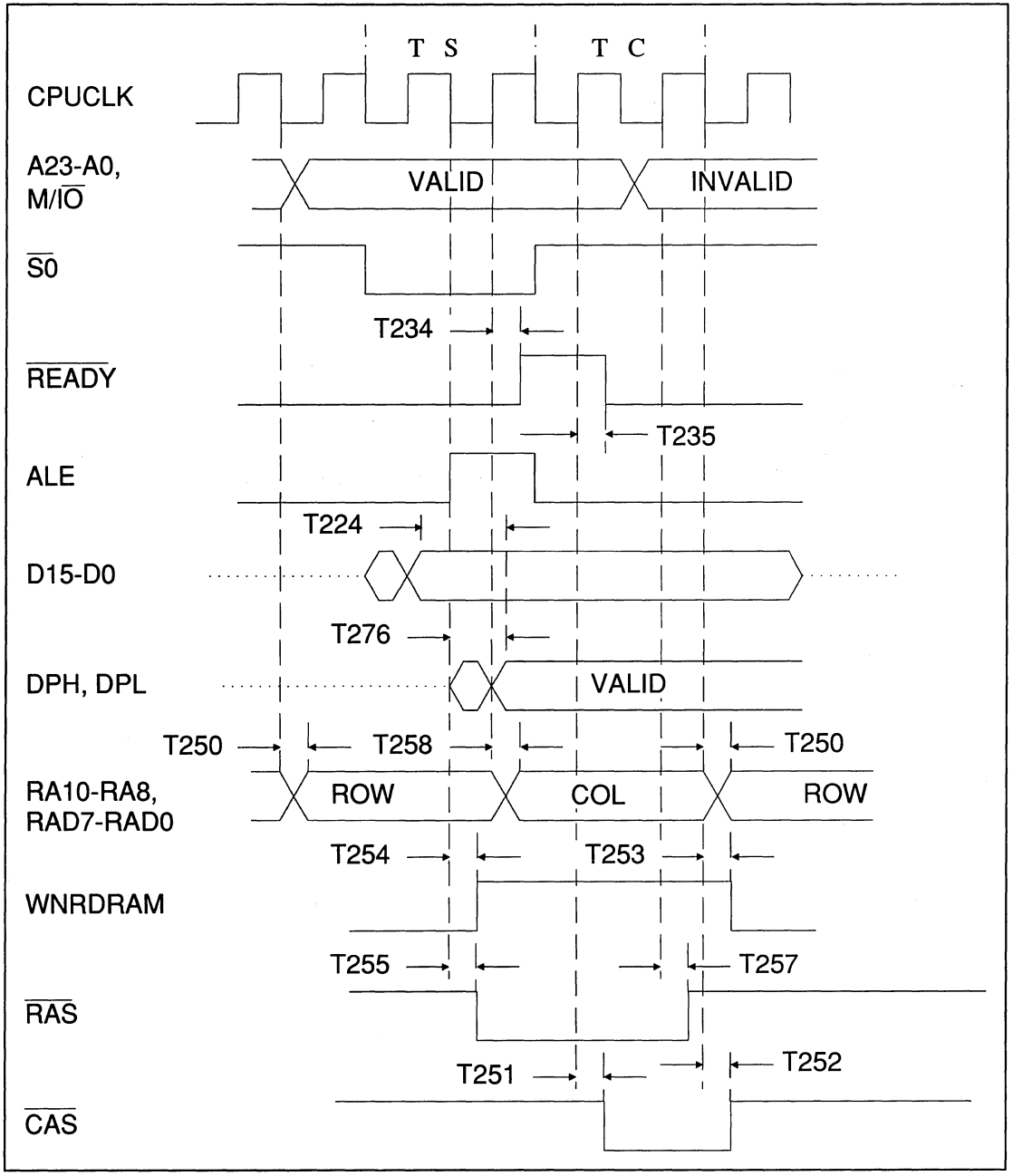


FIGURE 11-10. 80286 - NON-PAGE MODE 01, 0 WAIT STATE WRITE (4072H = 3560H)

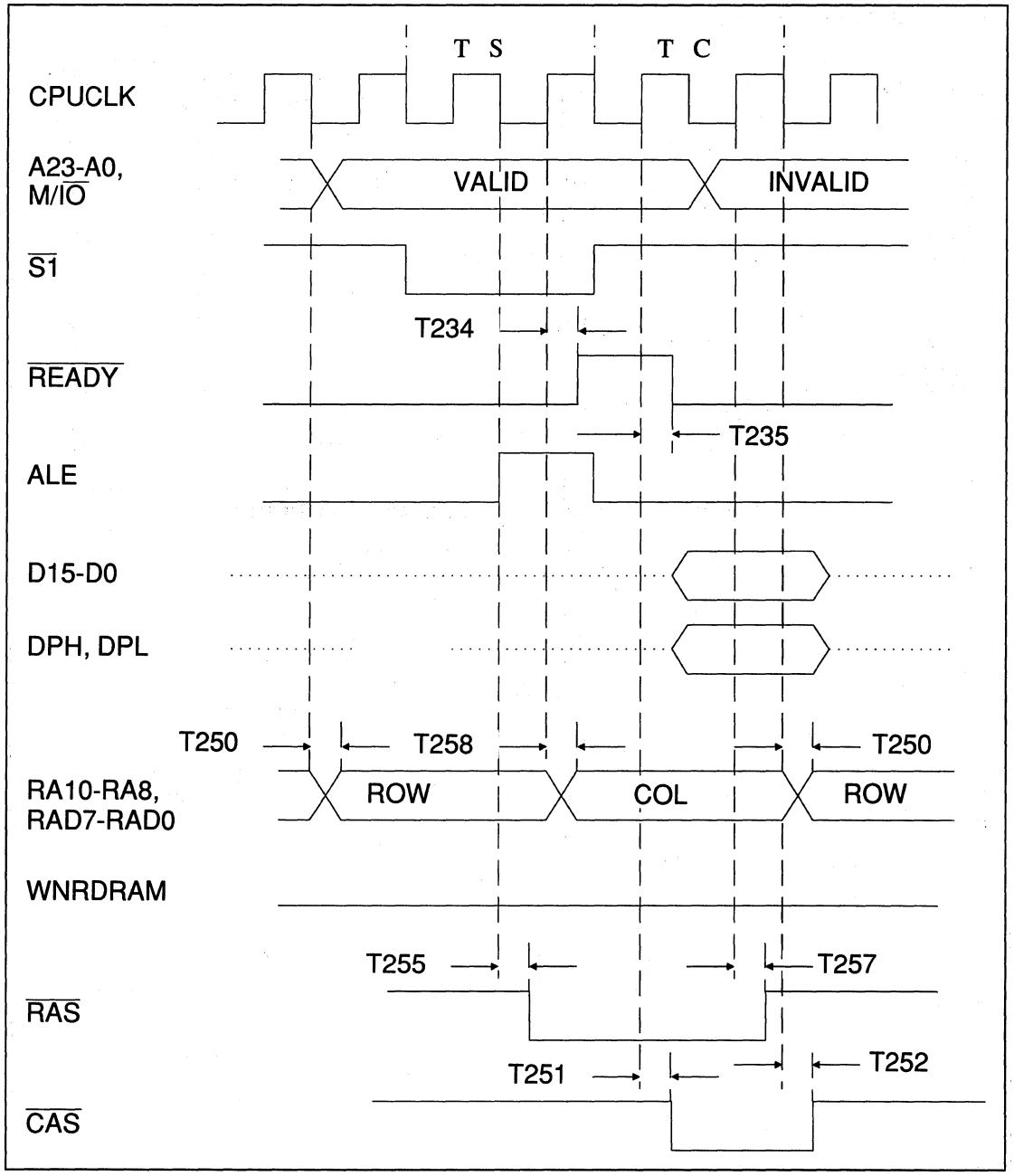


FIGURE 11-11. 80286 - NON-PAGE MODE 01, 0 WAIT STATE READ (4072H = 3560H)

11.1.4 80386SX Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T200	Processor ADDRESS to RAM address valid, Page Hit		34	27
T201	CPUCLK rise to CAS fall, 2.5 CLK CAS		31	25
T202	CPUCLK fall to CAS rise		24	21
T203	CPUCLK fall to CAS fall, 2.0 CLK CAS		27	22
T204	Processor data to parity valid		25	20
T205	CPUCLK rise to RAM address valid, Page Miss		48	43
T206	CPUCLK rise to WNRDRAM rise		31	28
T207	CPUCLK fall to RAS fall, first access		27	21
T208	CPUCLK rise to COLUMN address valid		49	33
T209	CPUCLK rise to WNRDRAM fall		31	28
T212	CPUCLK rise to RAS rise, Page Miss		27	24
T213	CPUCLK fall to RAS fall, Page Miss		27	24
T214	CPUCLK rise to READY fall *		19	18
T215	CPUCLK rise to READY rise *		19	18

TABLE 11-6. 80386SX - PAGE MODE MEMORY TIMING

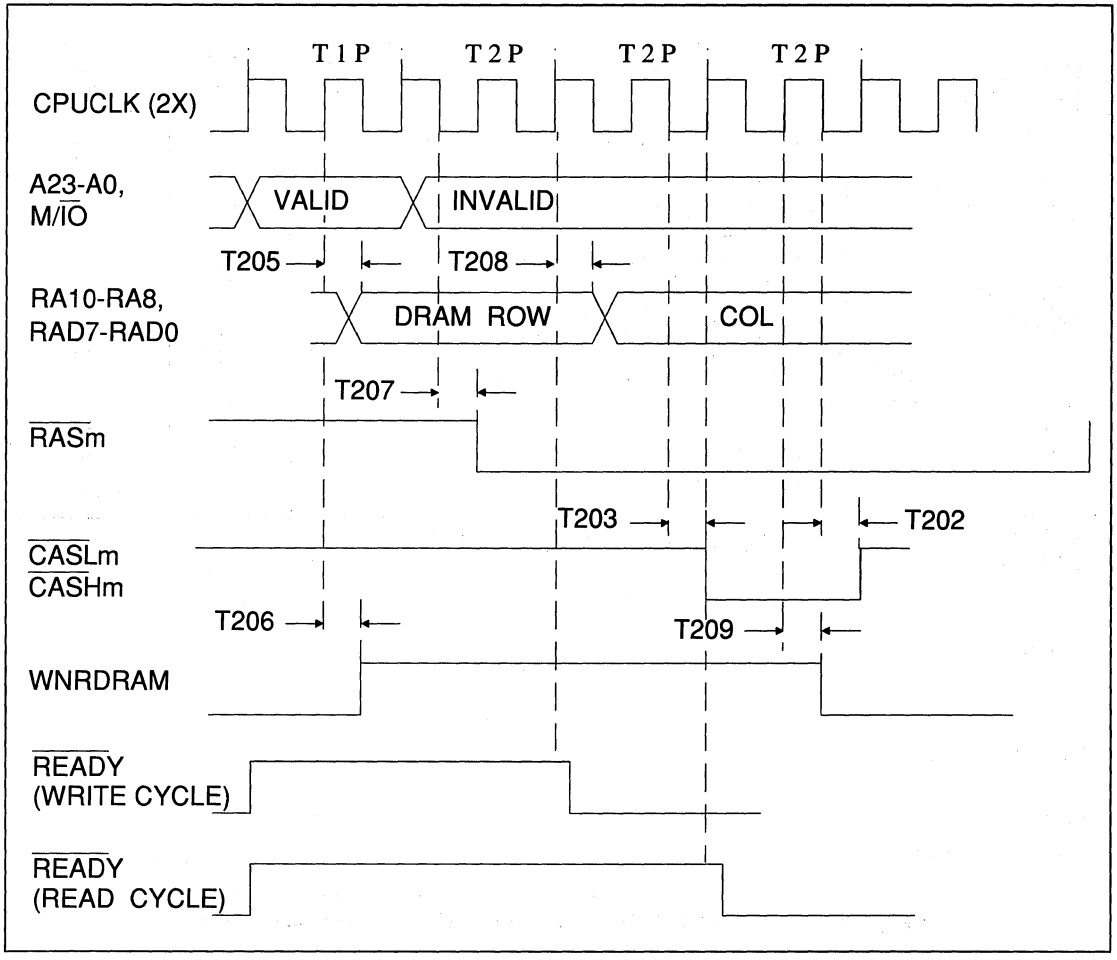


FIGURE 11-12. 80386SX - PAGE MODE, FIRST ACCESS READ/WRITE

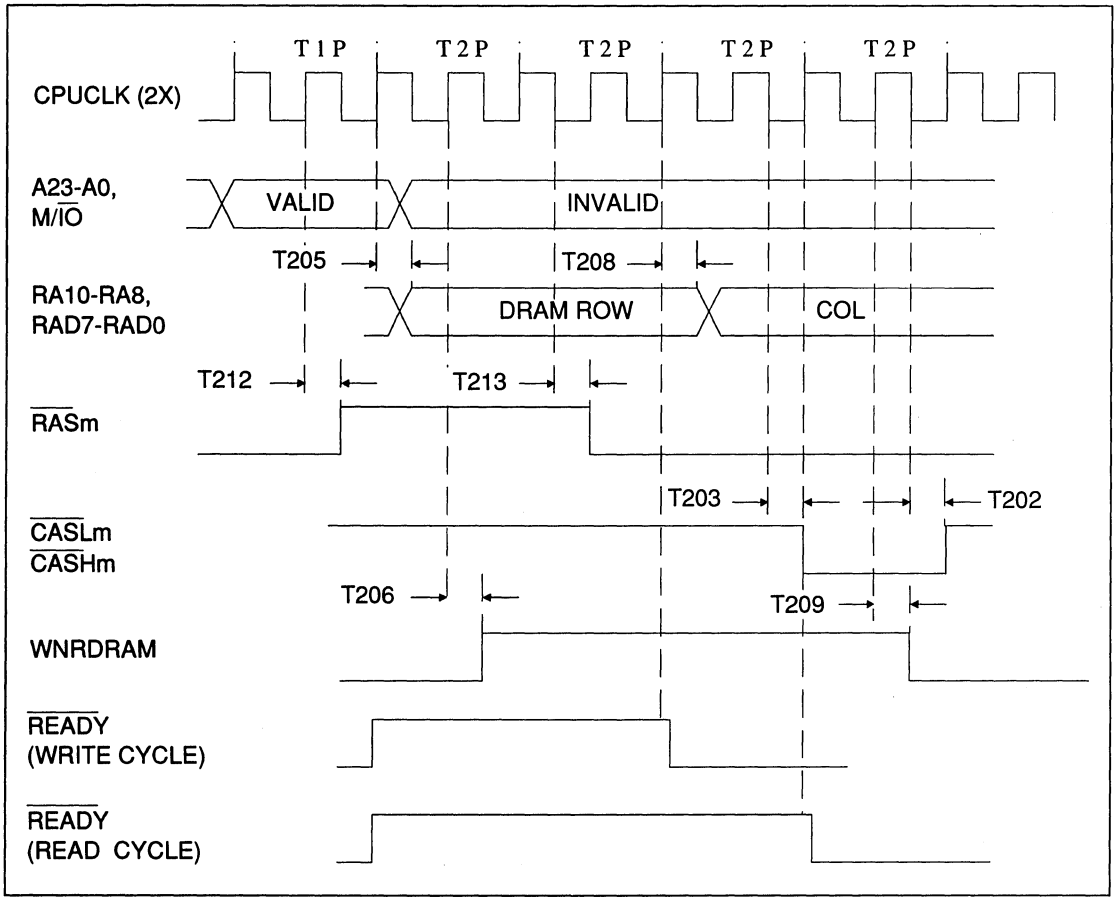


FIGURE 11-13. 80386SX - PAGE MODE, PAGE MISS READ/WRITE

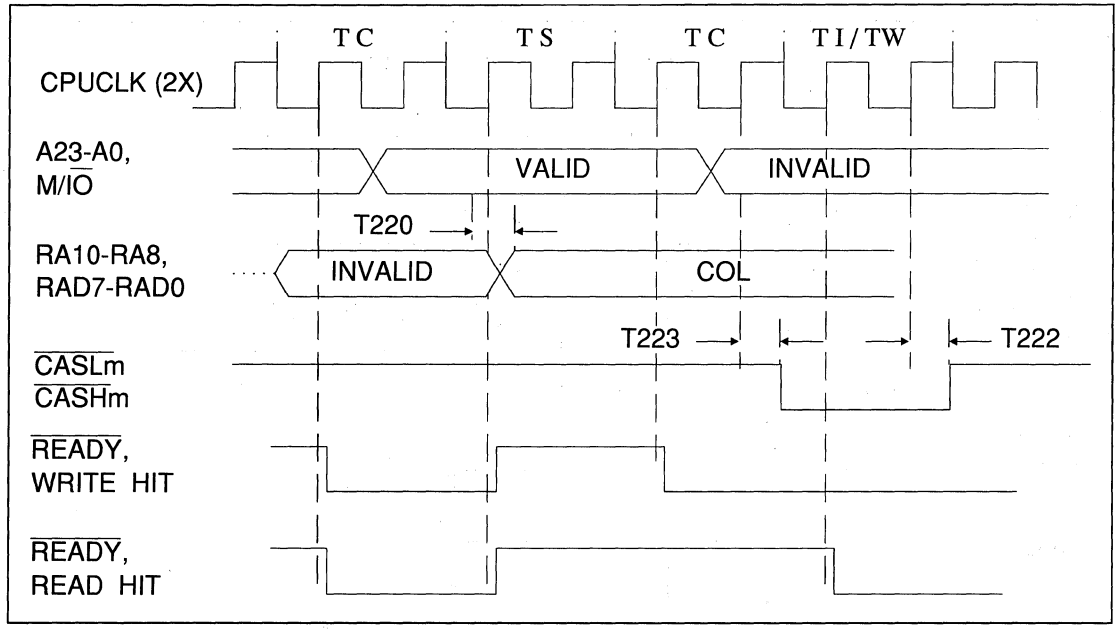


FIGURE 11-14. 80386SX - PAGE MODE, READ CYCLE FOLLOWED BY A PAGE HIT

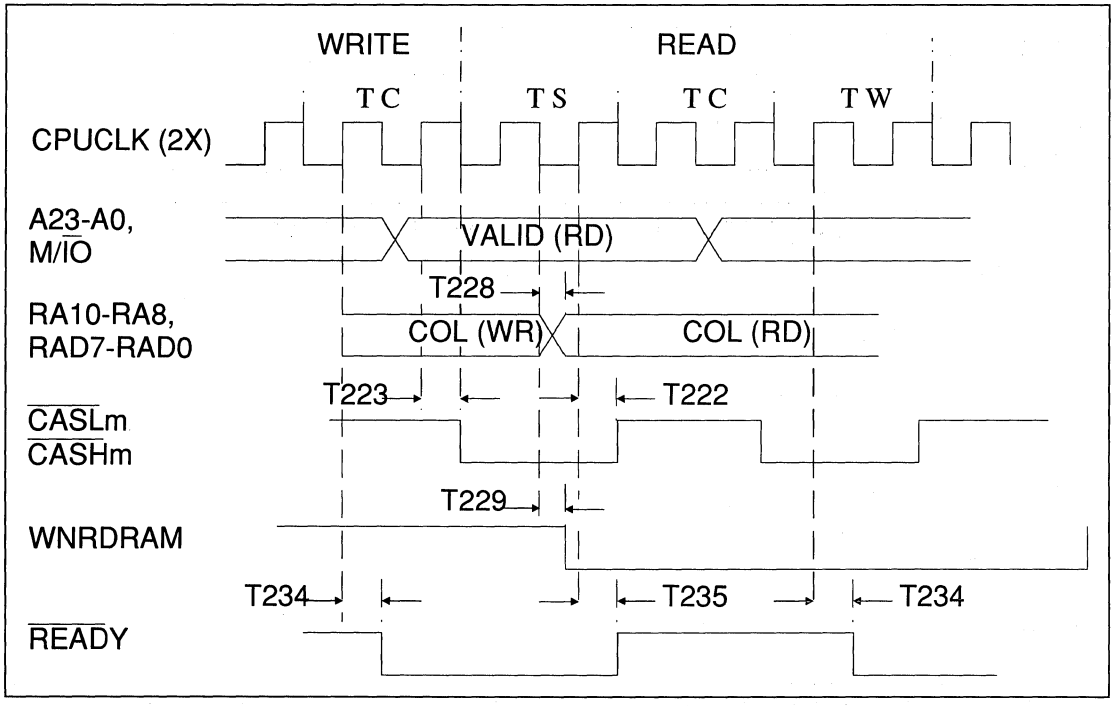


FIGURE 11-15. 80386SX - PAGE MODE, READ AFTER WRITE

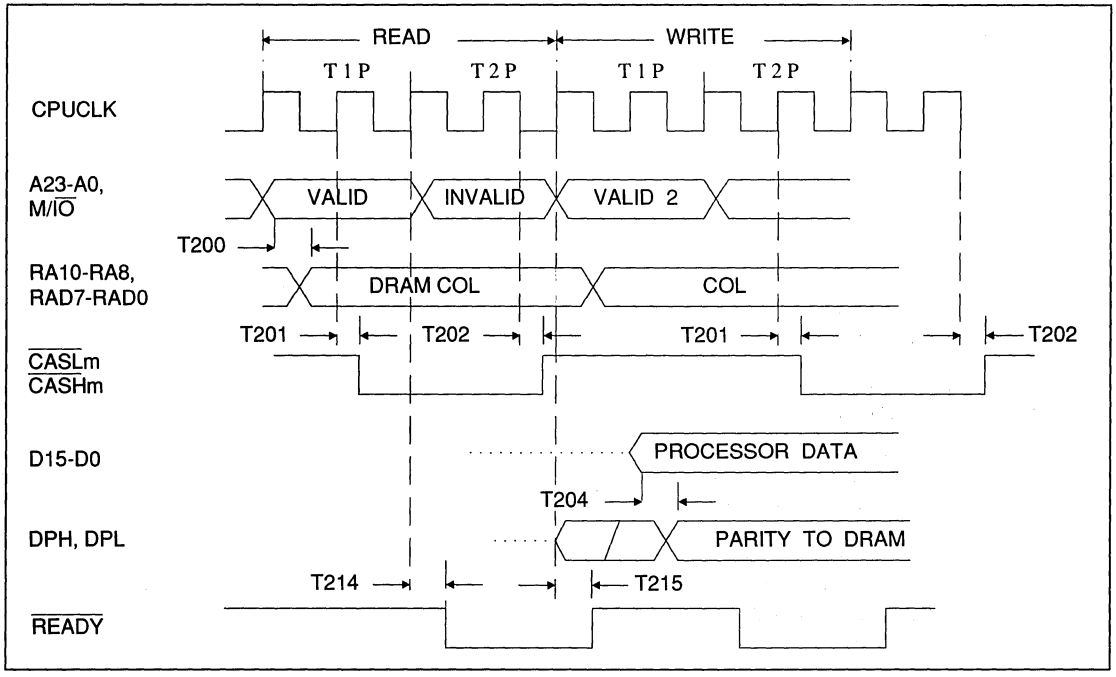


FIGURE 11-16. 80386SX - PAGE MODE, READ HIT FOLLOWED BY A WRITE HIT

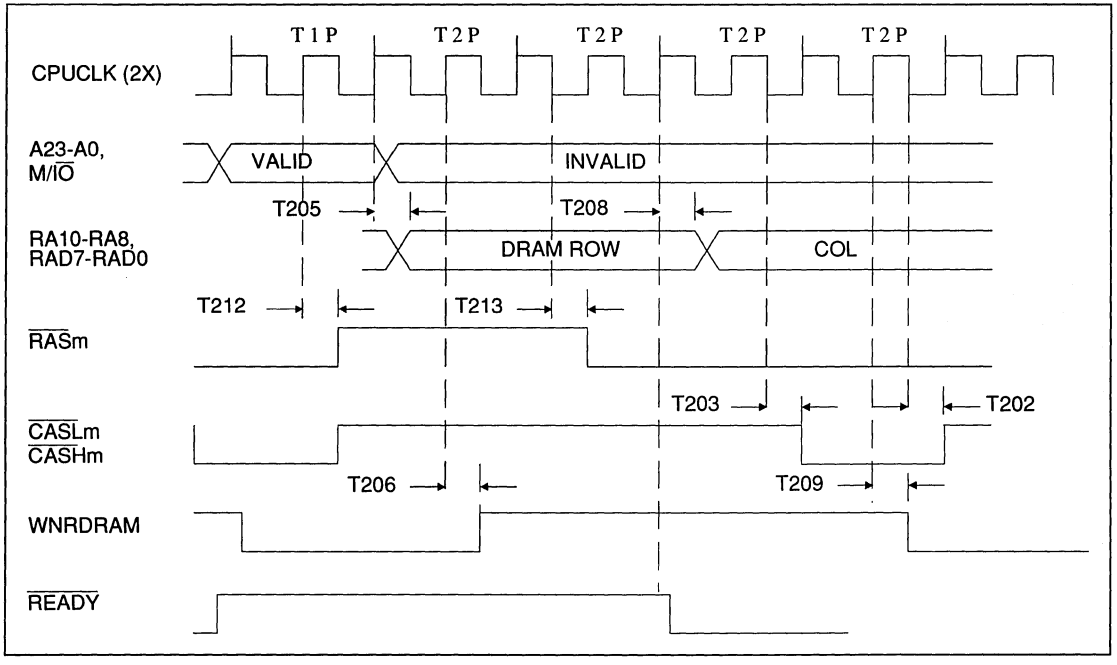


FIGURE 11-17. 80386SX - PAGE MODE, WRITE MISS CYCLE FOLLOWING A WRITE CYCLE

11.1.5 80386SX Non-Page Mode 00 And Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T204	See Table 11-6			
T214	See Table 11-6			
T215	See Table 11-6			
T240	CPUCLK rise to ROW address valid		42	42
T241	CPUCLK fall to CAS fall		27	27
T242	CPUCLK rise to CAS rise		28	24
T243	CPUCLK rise to WNRDRAM fall		28	28
T244	CPUCLK rise to WNRDRAM rise		28	28
T245	CPUCLK rise to RAS fall		25	23
T246	CPUCLK rise to RAS rise		25	23
T247	CPUCLK fall to RAS rise		29	29
T248	CPUCLK fall to COLUMN address valid		44	44
T249	CPUCLK rise to CAS fall		29	29
T260	CPUCLK rise to COLUMN address		43	41

TABLE 11-7. 80386SX - NON-PAGE MODE 00 AND MODE 01 MEMORY TIMING

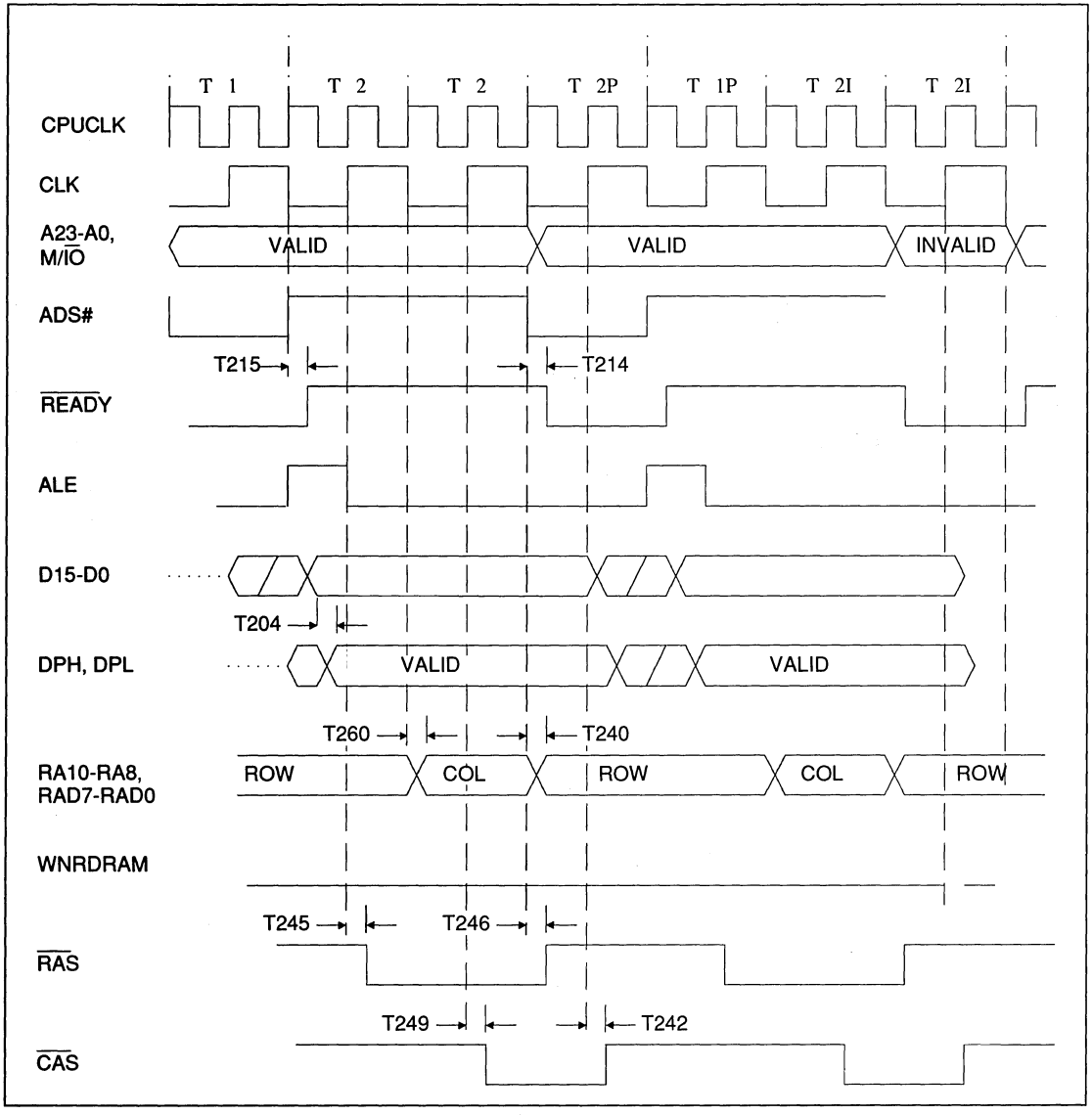


FIGURE 11-18. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE READ (PIPELINE) (4072H = 0001)

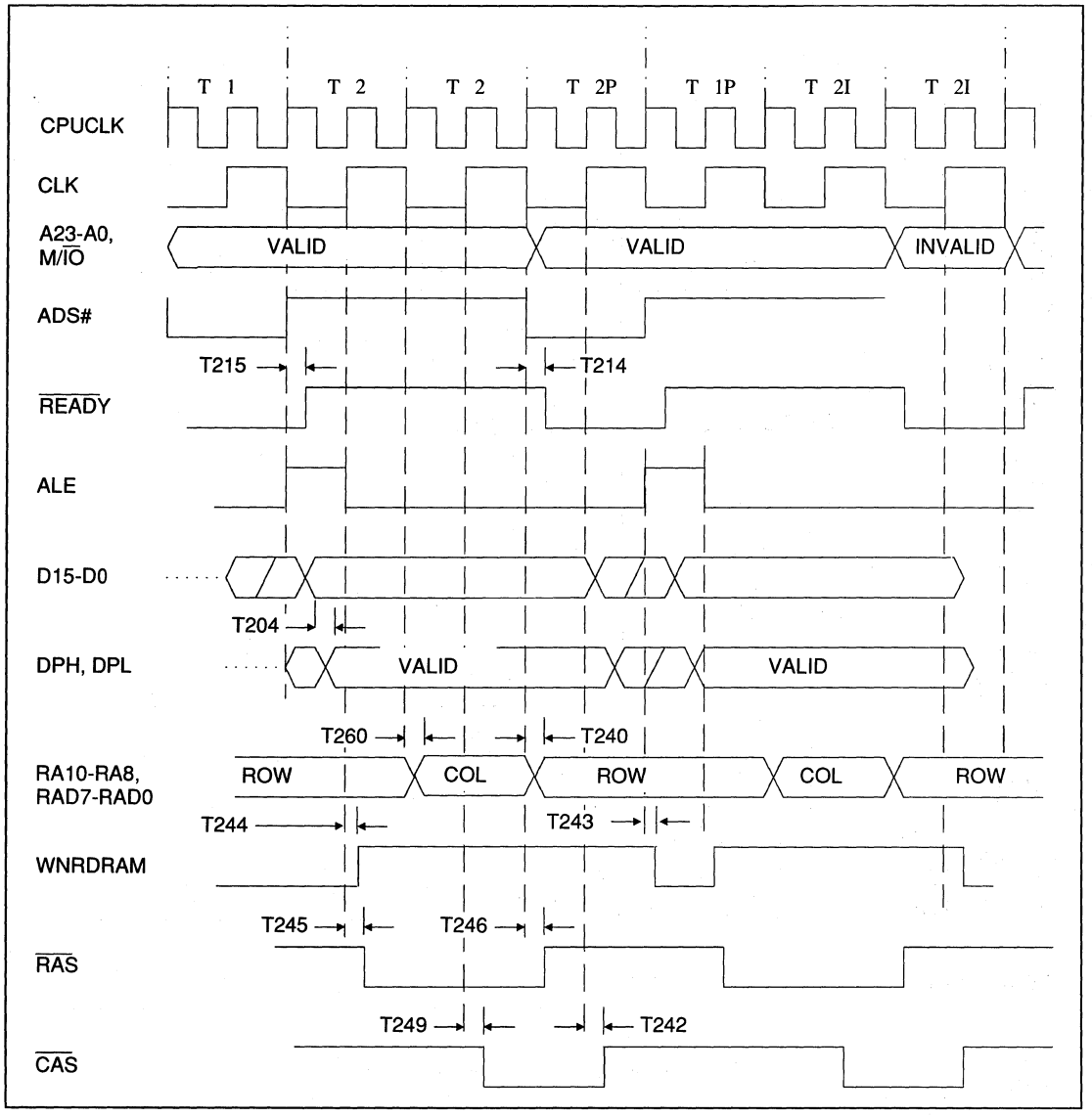


FIGURE 11-19. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE WRITE (PIPELINE) (4072H = 0001)

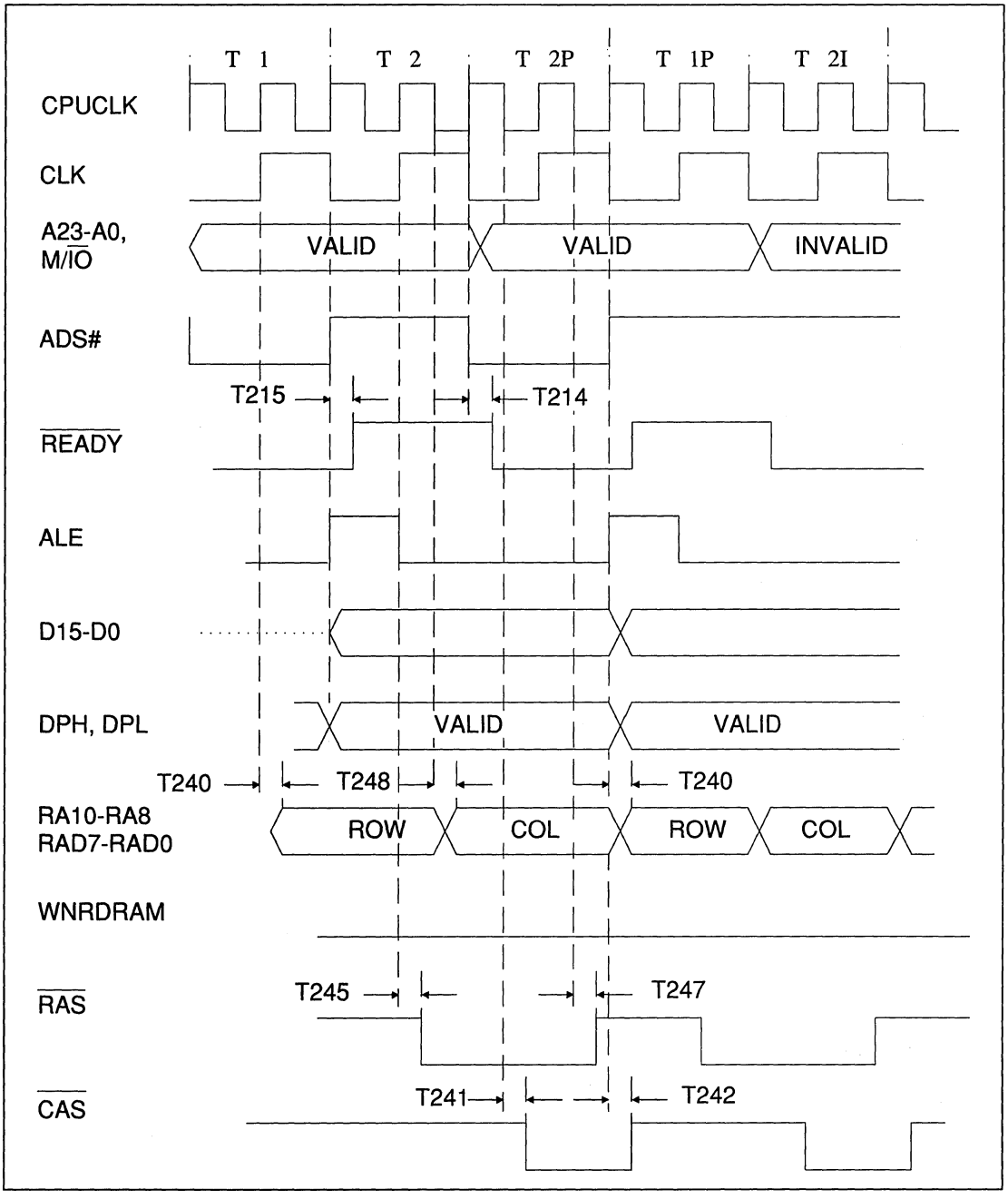


FIGURE 11-20. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

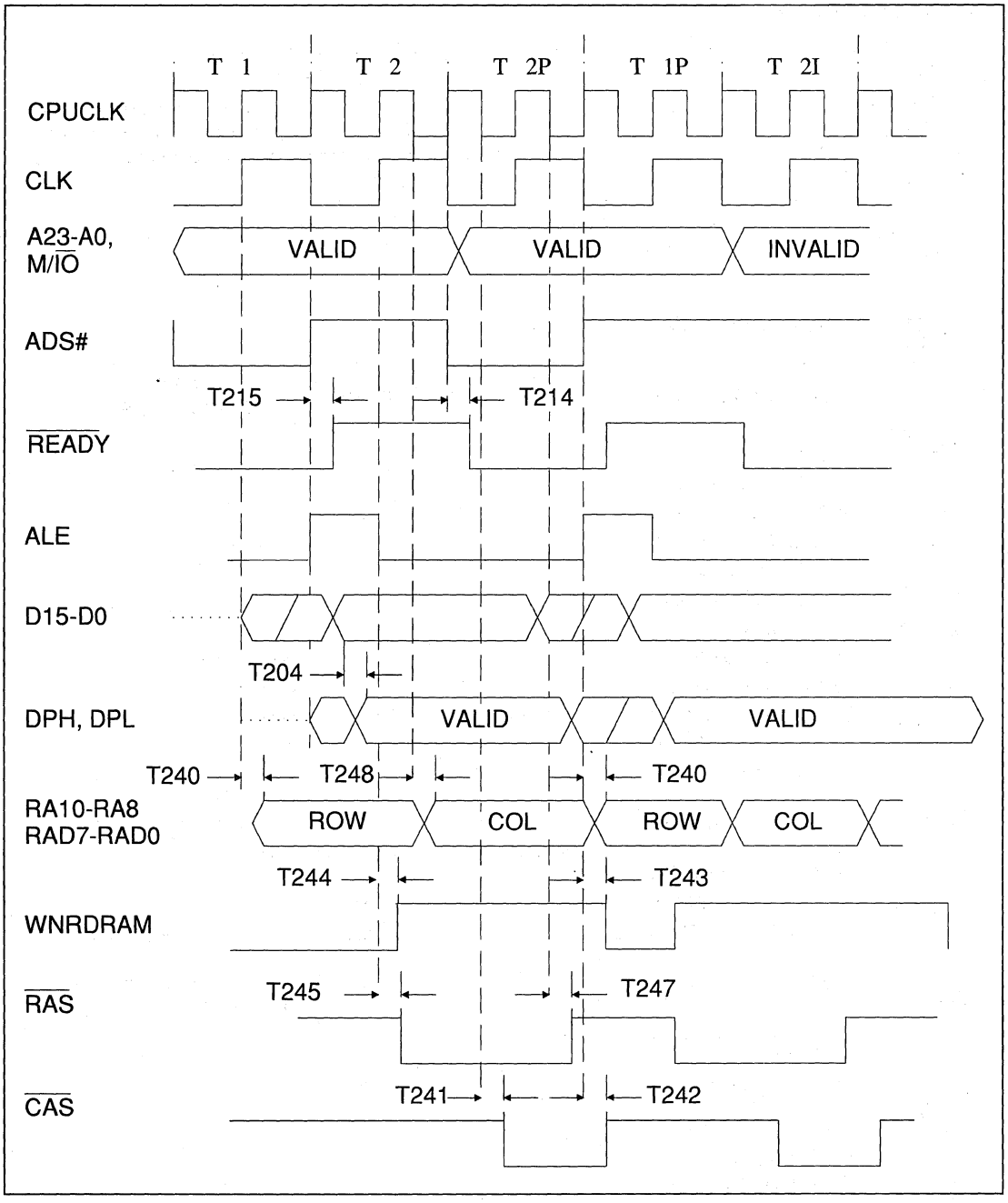


FIGURE 11-21. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

11.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus refresh cycle

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

4

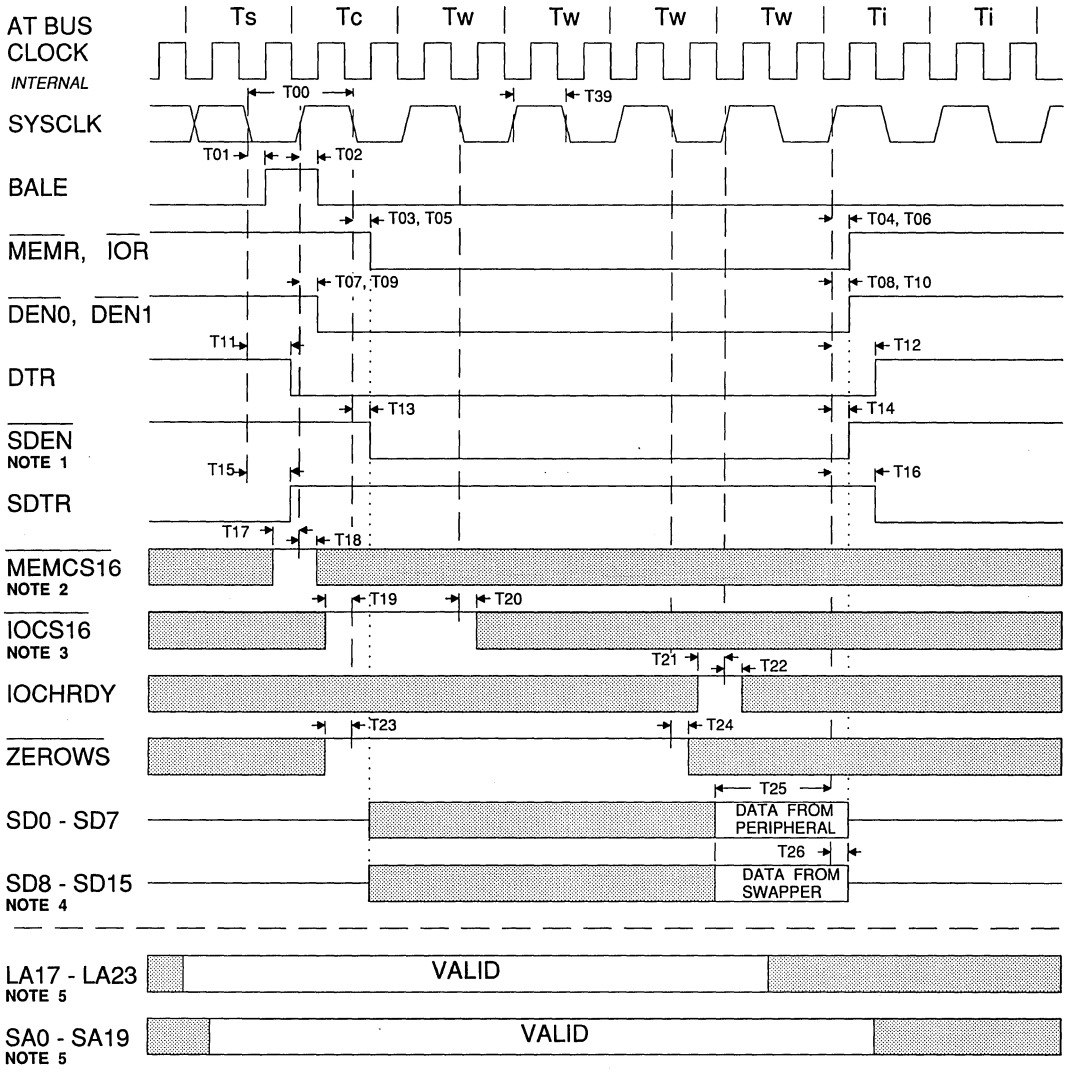
11.2.1 CPU Initiated AT Bus Cycles

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T00	SYSCLK Cycle Time	100		ns	
T01	SYSCLK fall to BALE rise		12	ns	
T02	SYSCLK rise to BALE fall		9	ns	
T03	SYSCLK fall to $\overline{\text{MEMR}}$ fall		9	ns	8-bit cycle
T04	SYSCLK rise to $\overline{\text{MEMR}}$ rise		6	ns	
T05	SYSCLK fall to $\overline{\text{IOR}}$ fall		10	ns	
T06	SYSCLK rise to $\overline{\text{IOR}}$ rise		7	ns	
T07	SYSCLK rise to $\overline{\text{DEN0}}$ fall		7	ns	Read Cycle
T08	SYSCLK rise to $\overline{\text{DEN0}}$ rise		11	ns	Read Cycle
T09	SYSCLK rise to $\overline{\text{DEN1}}$ fall		7	ns	Read Cycle
T10	SYSCLK rise to $\overline{\text{DEN1}}$ rise		9	ns	Read Cycle
T11	SYSCLK fall to DTR fall		19	ns	Delay is number given plus (T00 × 0.25)
T12	SYSCLK rise to DTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T13	SYSCLK fall to $\overline{\text{SDEN}}$ fall		10	ns	
T14	SYSCLK rise to $\overline{\text{SDEN}}$ rise		8	ns	
T15	SYSCLK fall to SDTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T16	SYSCLK rise to SDTR fall		11	ns	Delay is number given plus (T00 × 0.25)
T17	$\overline{\text{MEMCS16}}$ setup time to SYSCLK rise	25		ns	
T18	$\overline{\text{MEMCS16}}$ hold time from SYSCLK rise	0		ns	
T19	$\overline{\text{IOCS16}}$ setup time to SYSCLK fall	23		ns	
T20	$\overline{\text{IOCS16}}$ hold time from SYSCLK fall	0		ns	8-bit cycle

TABLE 11-8. CPU INITIATED AT BUS CYCLES

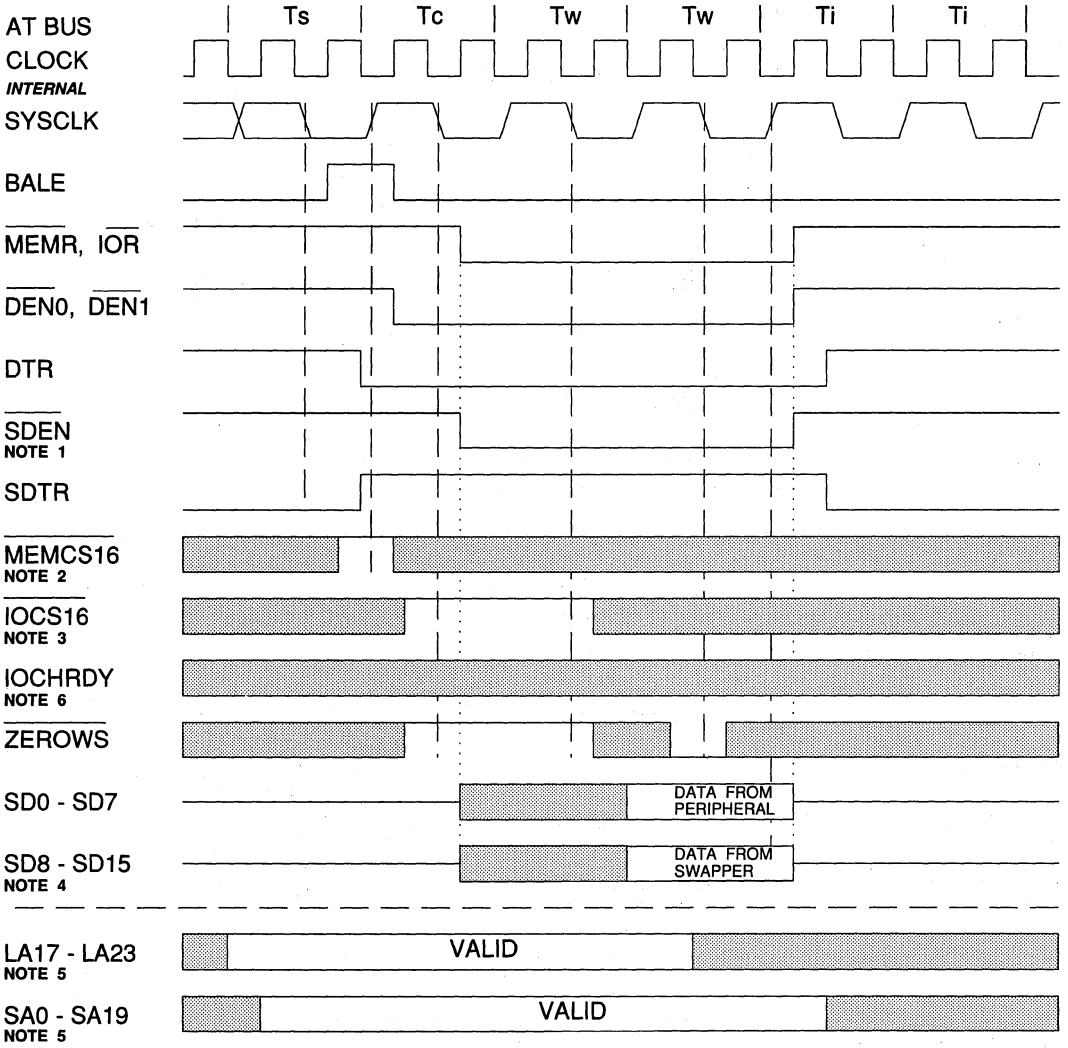
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T21	IOCHRDY setup time to SYSCLK rise	22		ns	
T22	IOCHRDY hold time from SYSCLK rise	0		ns	
T23	$\overline{\text{ZEROWS}}$ setup time to SYSCLK fall	24		ns	
T24	$\overline{\text{ZEROWS}}$ hold time from SYSCLK fall	0		ns	
T25	AT Bus data setup time to SYSCLK rise	22		ns	Total setup time is number given plus delay through AT Bus data buffers.
T26	AT Bus data hold time from SYSCLK rise	0		ns	
T27	SYSCLK fall to $\overline{\text{MEMW}}$ fall		9	ns	
T28	SYSCLK rise to $\overline{\text{MEMW}}$ rise		5	ns	
T29	SYSCLK fall to $\overline{\text{IOW}}$ fall		10	ns	
T30	SYSCLK rise to $\overline{\text{IOW}}$ rise		8	ns	
T31	SYSCLK fall to $\overline{\text{DEN0}}$ fall		10	ns	Write cycle
T32	SYSCLK fall to $\overline{\text{DEN0}}$ rise		9	ns	Write cycle
T33	SYSCLK fall to $\overline{\text{DEN1}}$ fall		10	ns	Write cycle
T34	SYSCLK fall to $\overline{\text{DEN1}}$ rise		9	ns	Write cycle
T35	SYSCLK fall to $\overline{\text{SDEN}}$ rise		11	ns	
T36	SYSCLK fall to SA0 rise		16	ns	Word to byte conversion cycle
T37	SYSCLK rise to $\overline{\text{MEMR}}$ fall		6	ns	16-bit cycle
T38	$\overline{\text{IOCS16}}$ hold time from SYSCLK rise	0		ns	16-bit cycle
T39	SYSCLK high time	-4	0	ns	(T00 ÷ 2) plus number given

TABLE 11-8. CPU INITIATED BUS CYCLES cont.



NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.
NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.
NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-22. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING



NOTE 1: SDEN is asserted only when SA0 is high.

NOTE 2: MEMCS16 is sampled only during memory cycles.

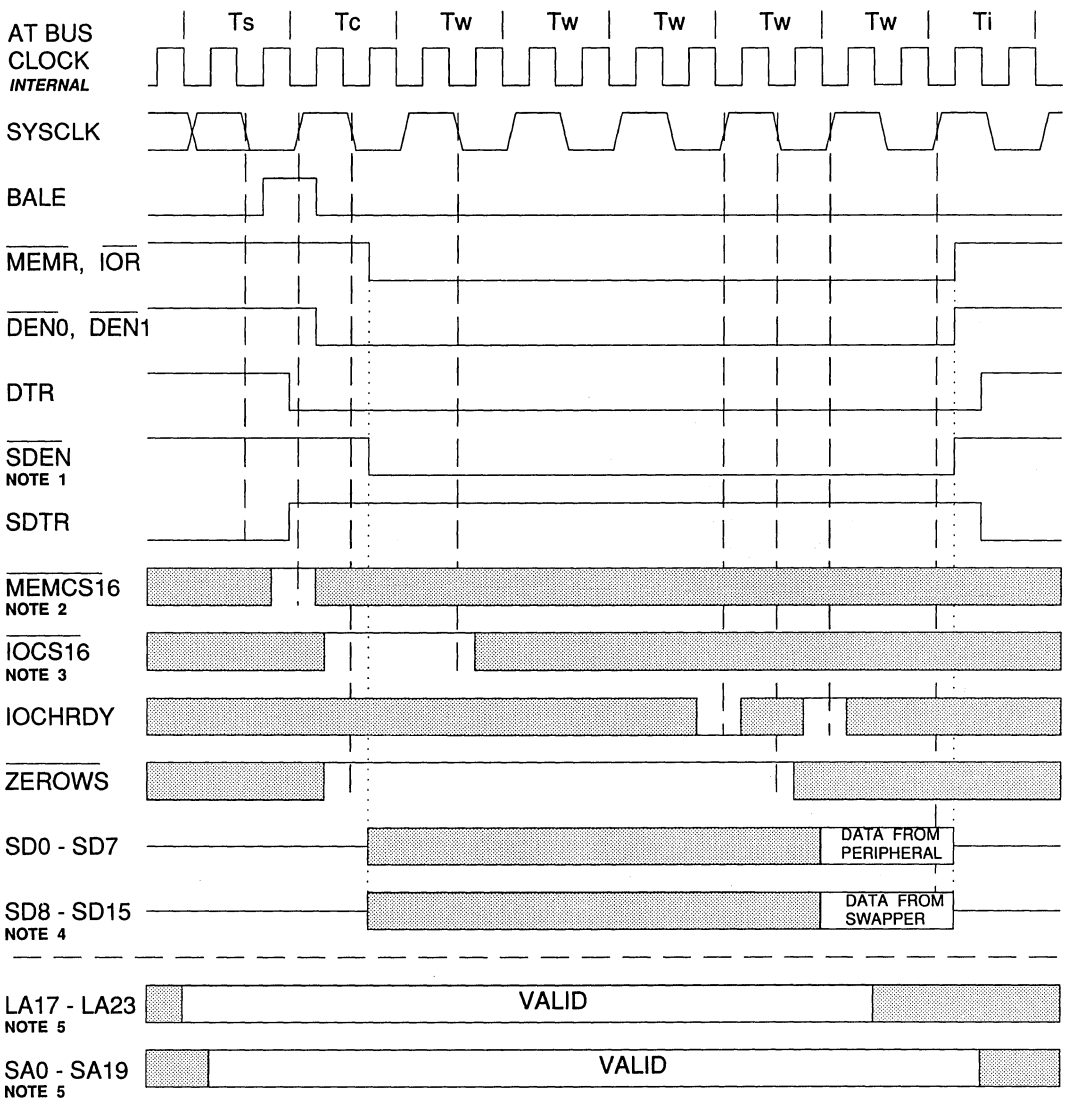
NOTE 3: IOCS16 is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

NOTE 6: IOCHRDY overrides ZEROWS only during the first cycle of a word to byte conversion.

FIGURE 11-23. AT BUS I/O OR MEMORY READ: 8-BIT, ZEROWS ASSERTED



NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.

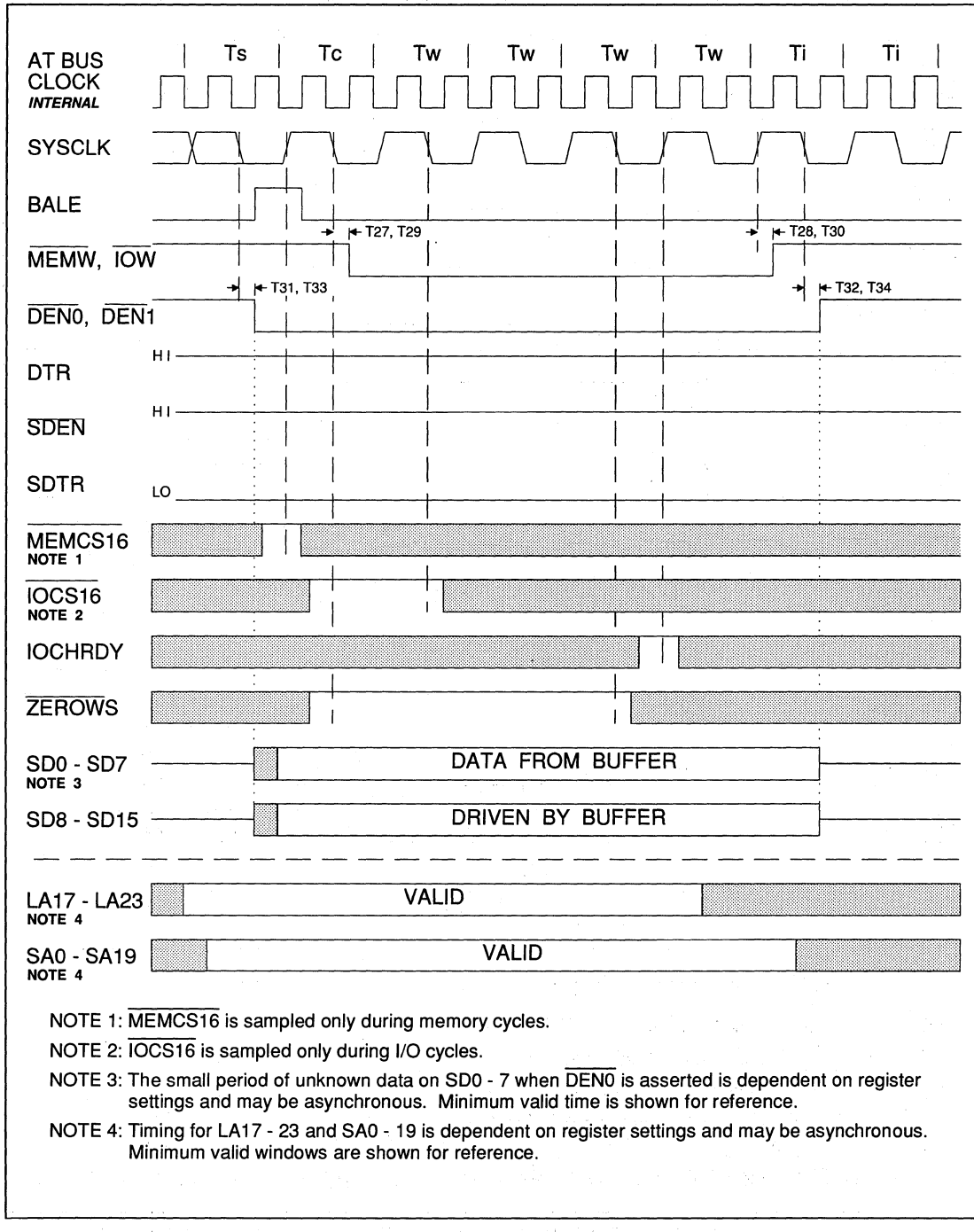
NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-24. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED



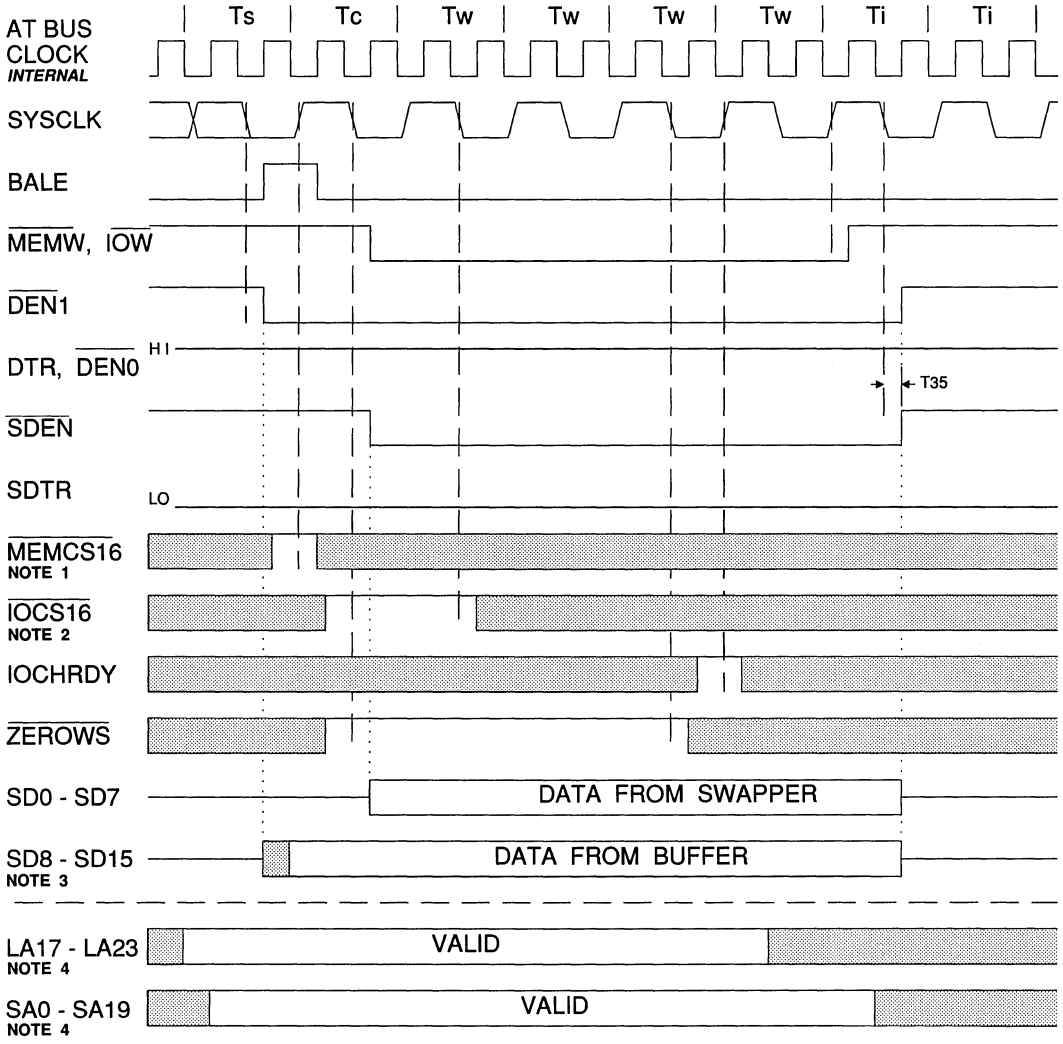
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when $\overline{\text{DEN0}}$ is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-25. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING



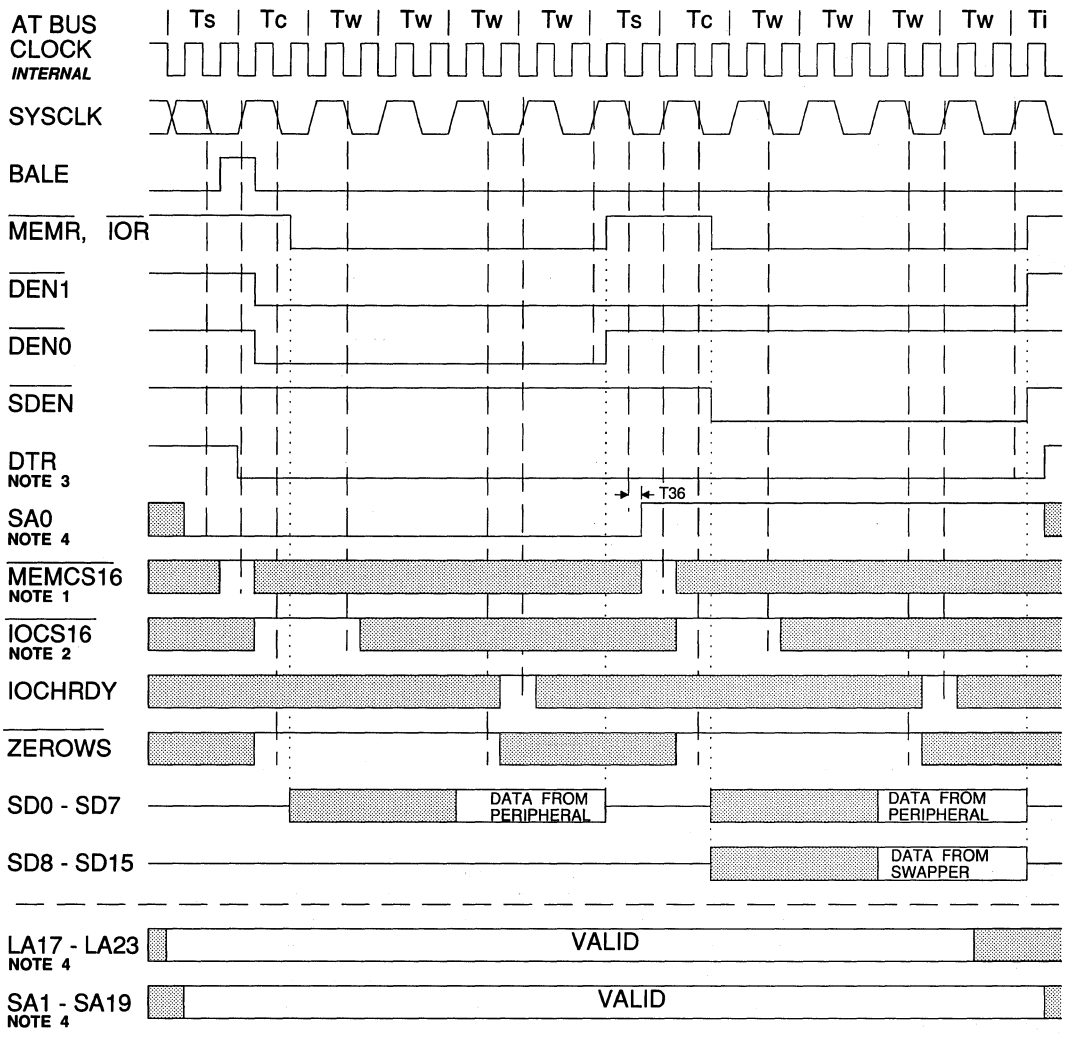
NOTE 1: MEMCS16 is sampled only during memory cycles.

NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD8 - 15 when DEN1 is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-26. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING



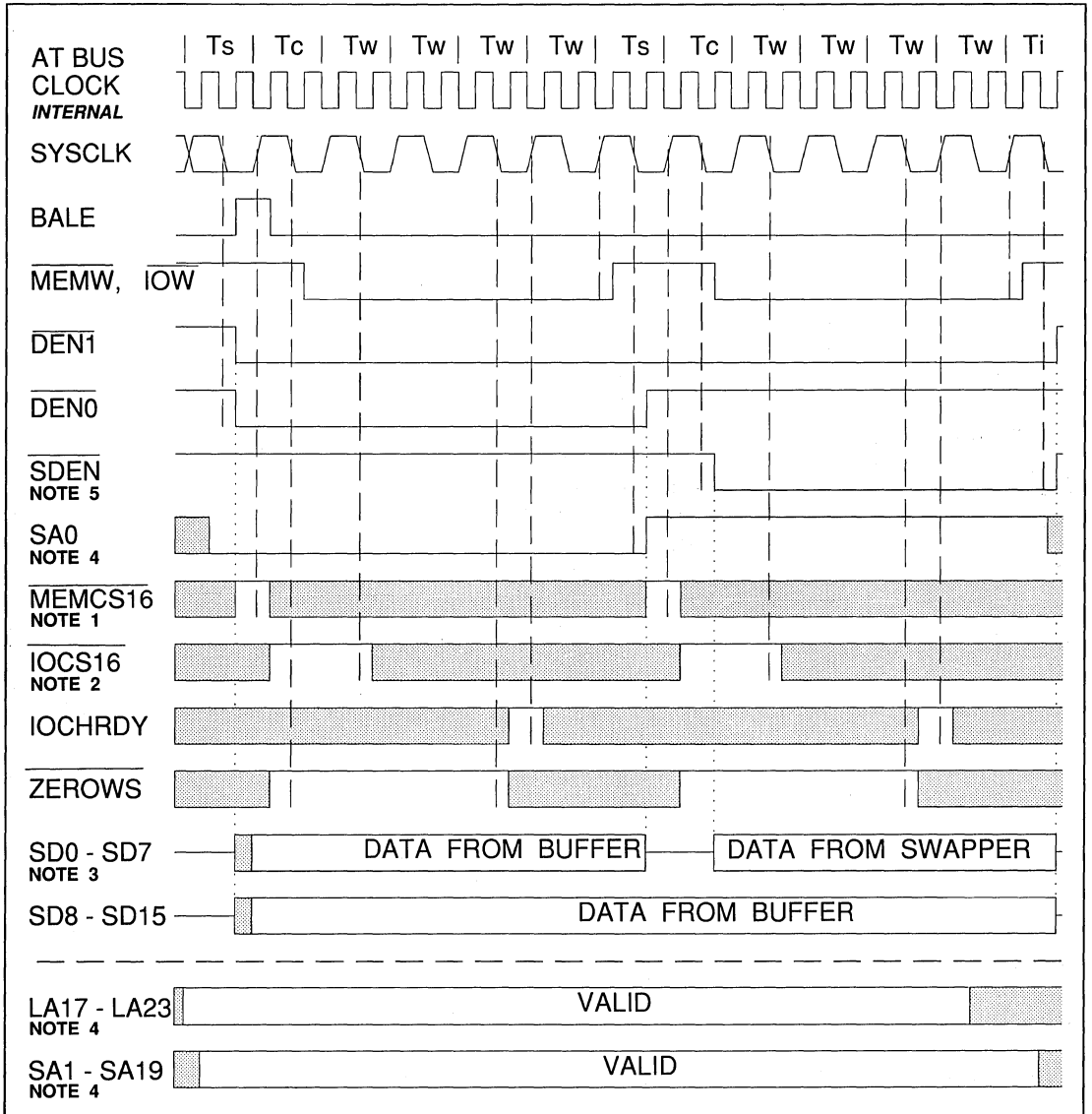
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: SDTR is the inversion of DTR during CPU transfer cycles.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-27. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

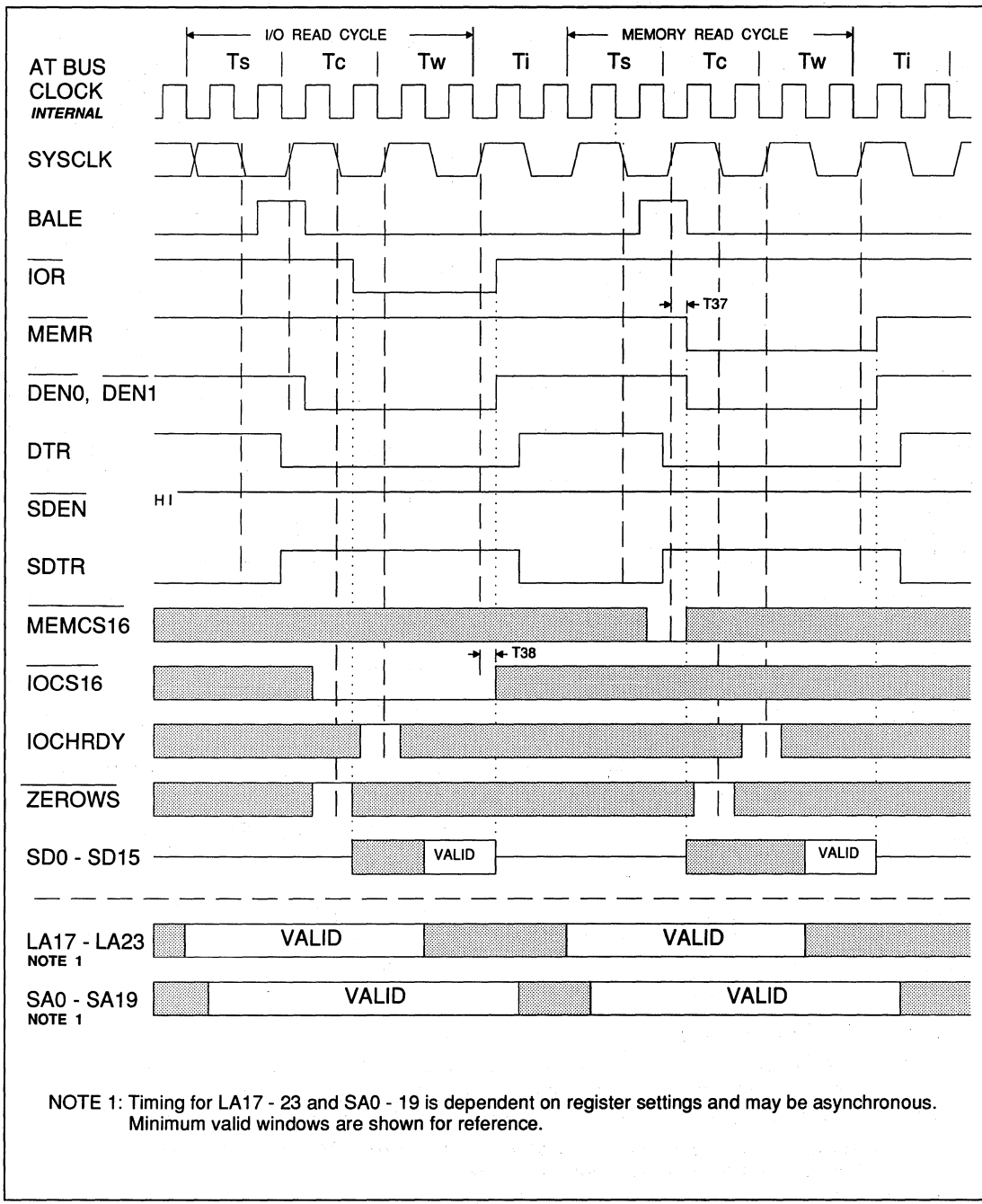
NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when $\overline{\text{DEN0}}$ is asserted is dependent on register settings and may be synchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

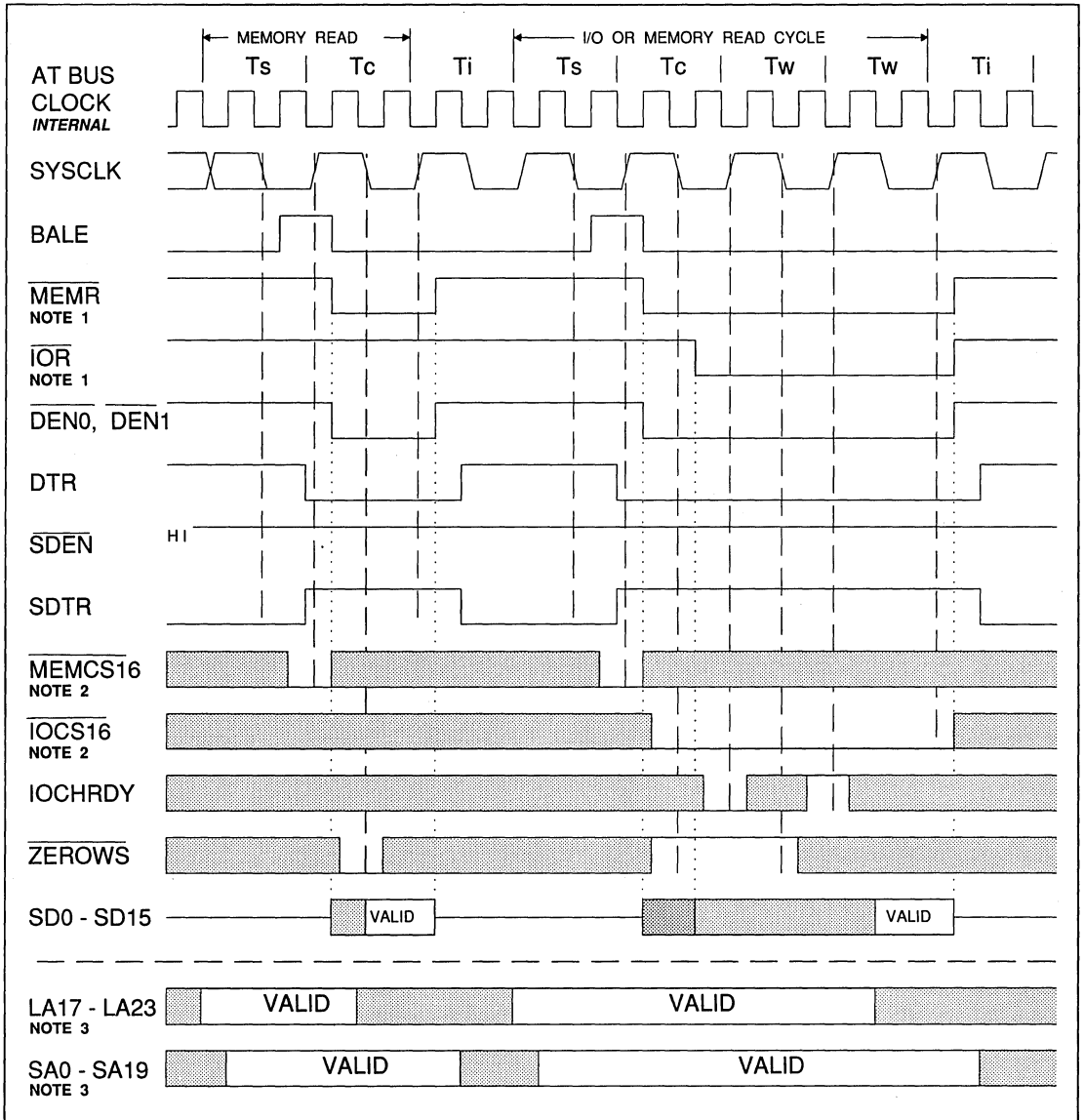
NOTE 5: SDTR remains low and DTR remains high for this cycle.

FIGURE 11-28. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-29. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING

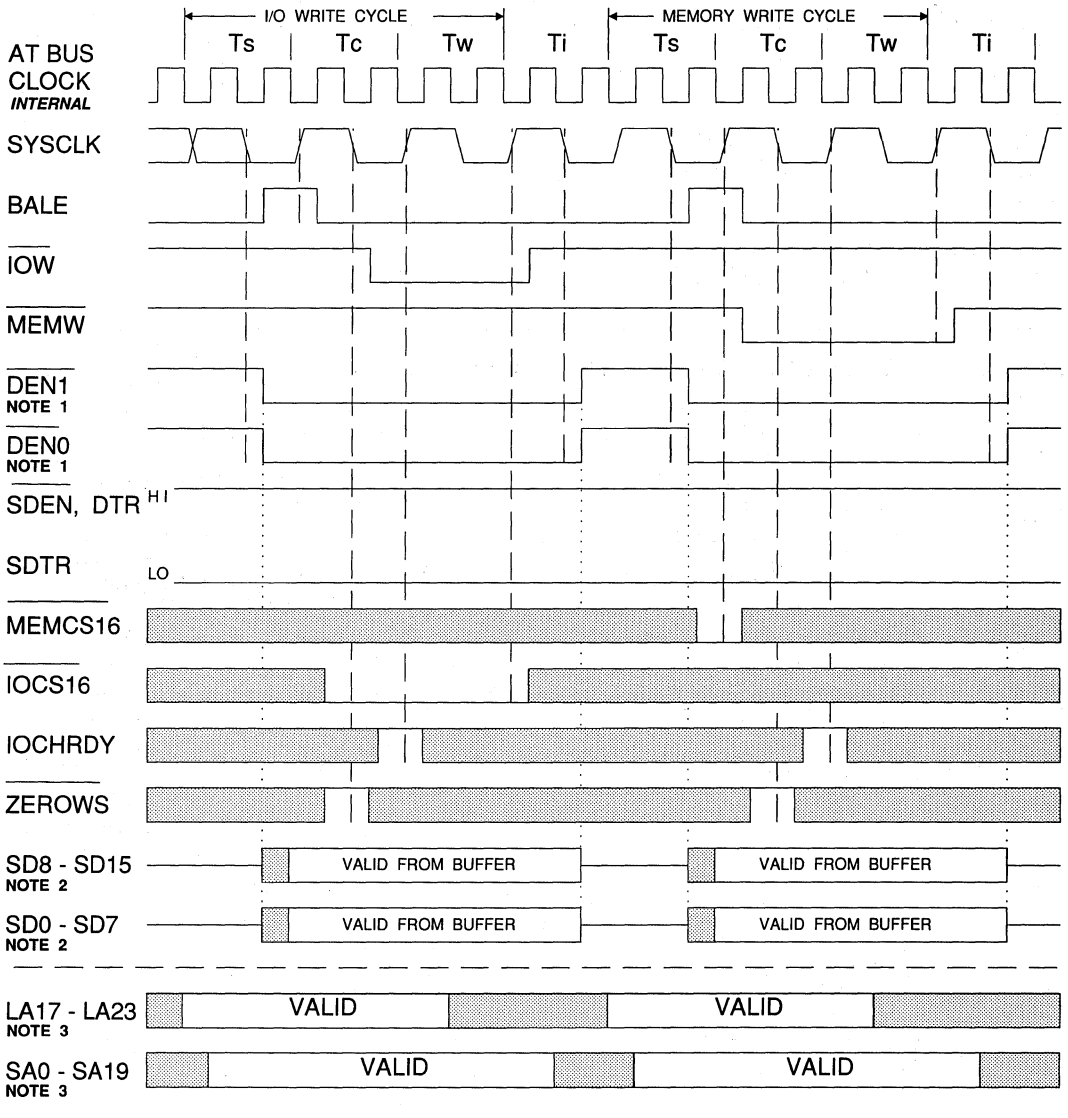


NOTE 1: MEMR and IOR will not be asserted simultaneously. The first cycle must be to memory, as zero wait state I/O cycles are not supported.

NOTE 2: MEMCS16 is sampled only during memory cycles. IOCS16 is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-30. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED



NOTE 1: $\overline{DEN0}$ is asserted only in cycles where SA0 is low. $\overline{DEN1}$ is asserted only in cycles where $\overline{SBHE}$ is low.

NOTE 2: SD8 - SD15 are driven when $\overline{DEN1}$ is low. SD0 - SD7 are driven when $\overline{DEN0}$ is low. The small period of unknown data is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 11-31. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING

11.2.2 Entering The AT Bus

The timing in this section is presented in the following sequence:

80286 CPU

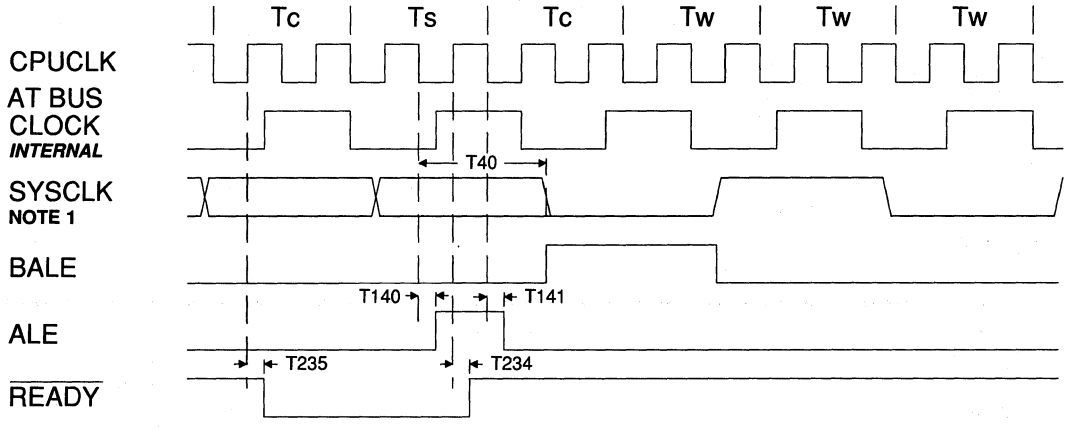
Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

80386SX CPU

Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T40	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	4		ns	Register 1872H: BRQ_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T41	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	9		ns	Register 1872H: BRQ_DEL = 00 BUS_MOD = 0X Delay is number given plus (T00 × 0.5)
T42	CPUCLK fall to SYSCLK fall 80386SX CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T43	CPUCLK rise to SYSCLK fall 80386SX CPU mode.		35	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T44	CPUCLK rise to SYSCLK fall 80286 CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T45	CPUCLK fall to SYSCLK fall 80286 CPU mode.		36	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T140	CPUCLK fall to ALE rise 80286 CPU mode. CPUCLK rise to ALE rise 80386SX CPU mode.		20	ns	
T141	CPUCLK fall to ALE fall 80286 CPU mode. CPUCLK rise to ALE fall 80386SX CPU mode.		20	ns	
T214	See TABLE 11-6				
T215	See TABLE 11-6				
T234	See TABLE 11-3				
T235	See TABLE 11-3				

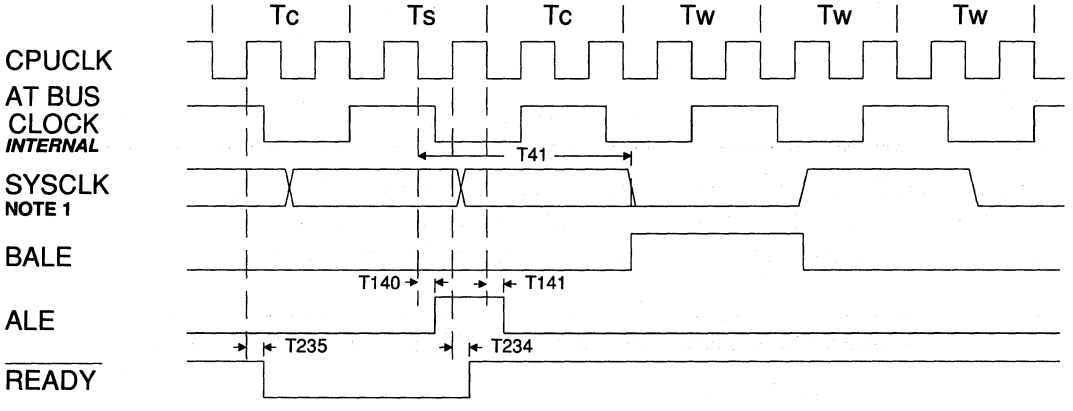
TABLE 11-9. ENTERING THE AT BUS



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

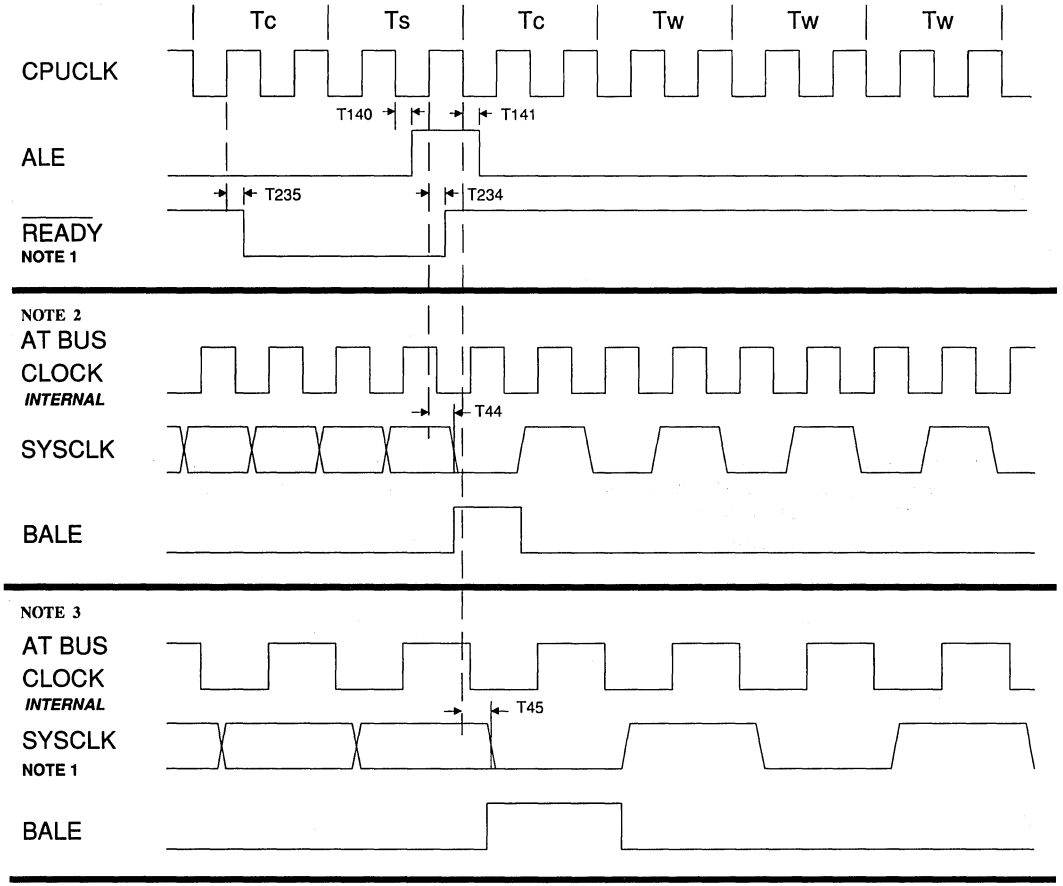
FIGURE 11-32. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1/2 CLOCK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

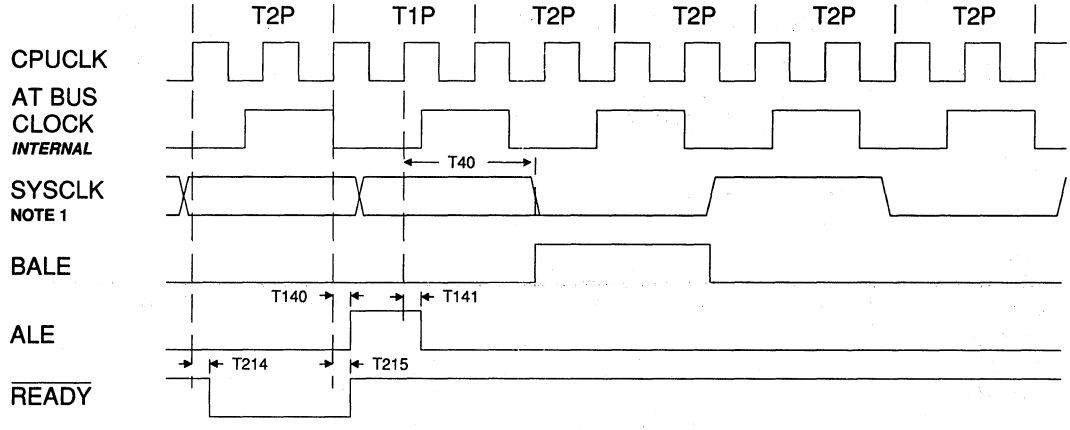
NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 11-33. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1 CLOCK



NOTE 1: $\overline{\text{READY}}$ timing is shown for when the previous cycle was not an AT bus cycle.
NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.
NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

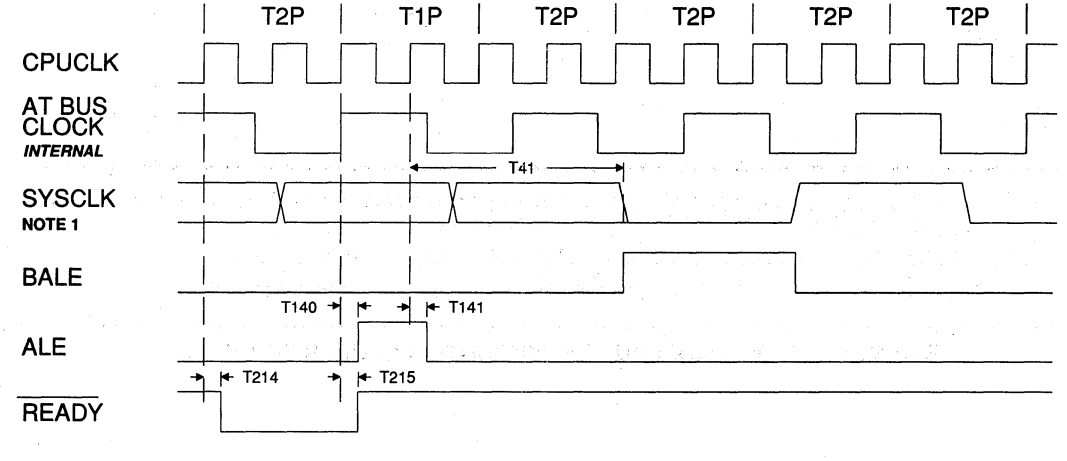
FIGURE 11-34. 80286 CPU - SYCNHRONOUS CPUCLK TO SYSCLK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

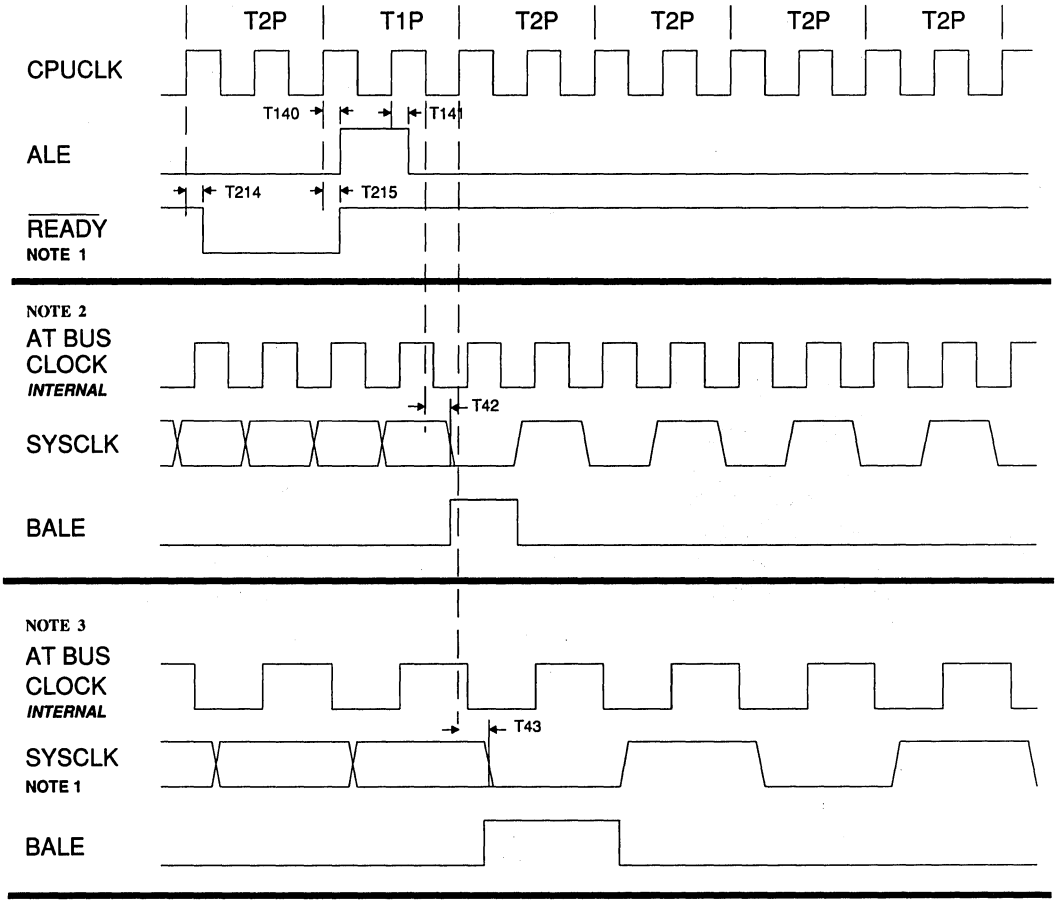
FIGURE 11-35. 80386SX CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1/2 CLOCK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 11-36. 80386SX CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1 CLOCK



NOTE 1: If this AT bus cycle is immediatly preceded by another bus cycle and the BUS_MOD field in register 1872 = 11, READY will fall 1 CPUCLK later than shown.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

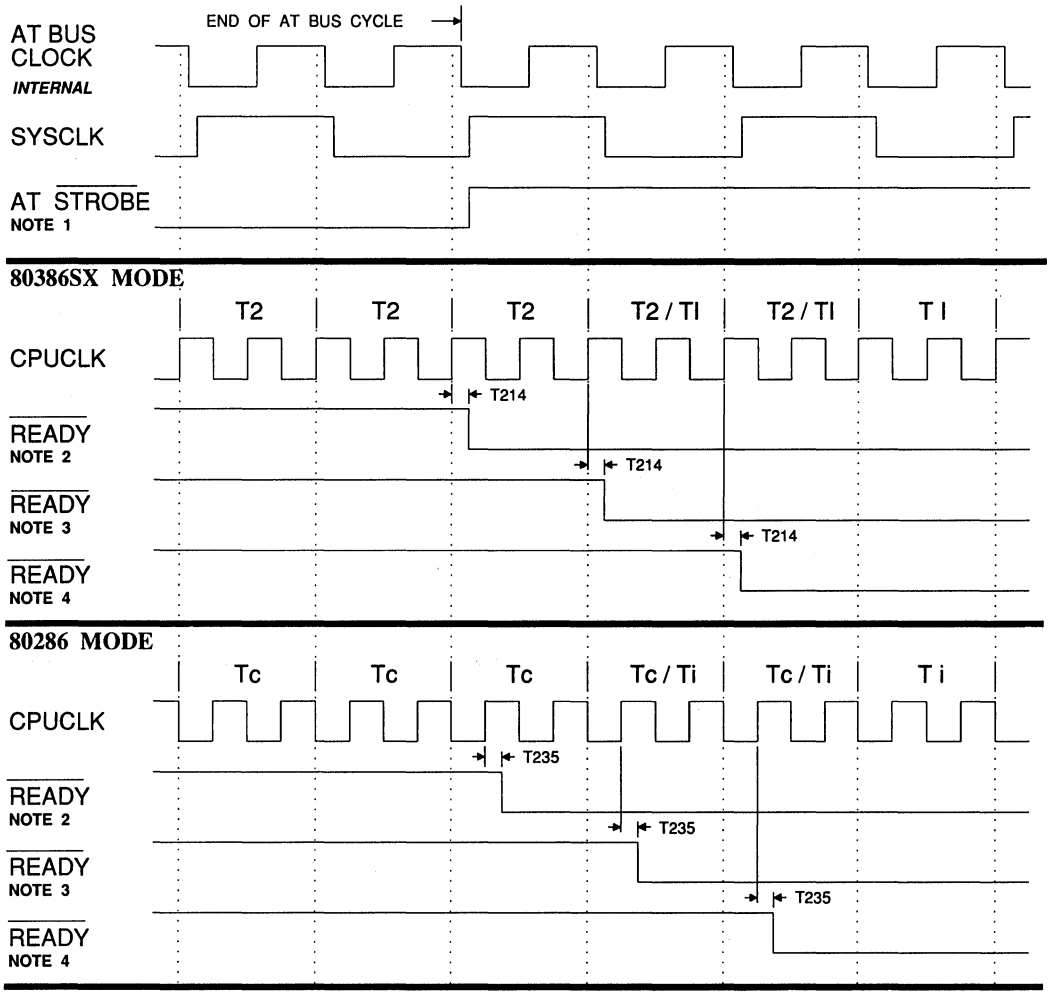
FIGURE 11-37. 80386SX CPU - SYCNHRONOUS CPUCLK TO SYSCLK

11.2.3 Exiting The AT Bus

Exiting a synchronous AT bus is covered first, followed by the asynchronous bus.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T46	SYSCLK fall to CPUCLK	-5		ns	Register 1872H: BAK_DEL = 10 BUS_MOD = 0X
T47	SYSCLK fall to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T48	SYSCLK rise to CPUCLK	-10		ns	Register 1872H: BAK_DEL = 00 BUS_MOD = 0X
T49	SYSCLK rise to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 11 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T144	CPUCLK fall to $\overline{\text{READY}}$ fall, 80286 CPU mode.		24	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T145	CPUCLK fall to $\overline{\text{READY}}$ rise, 80286 CPU mode.		26	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T214	See TABLE 11-6				
T215	See TABLE 11-6				
T234	See TABLE 11-3				
T235	See TABLE 11-3				

TABLE 11-10. EXITING THE AT BUS



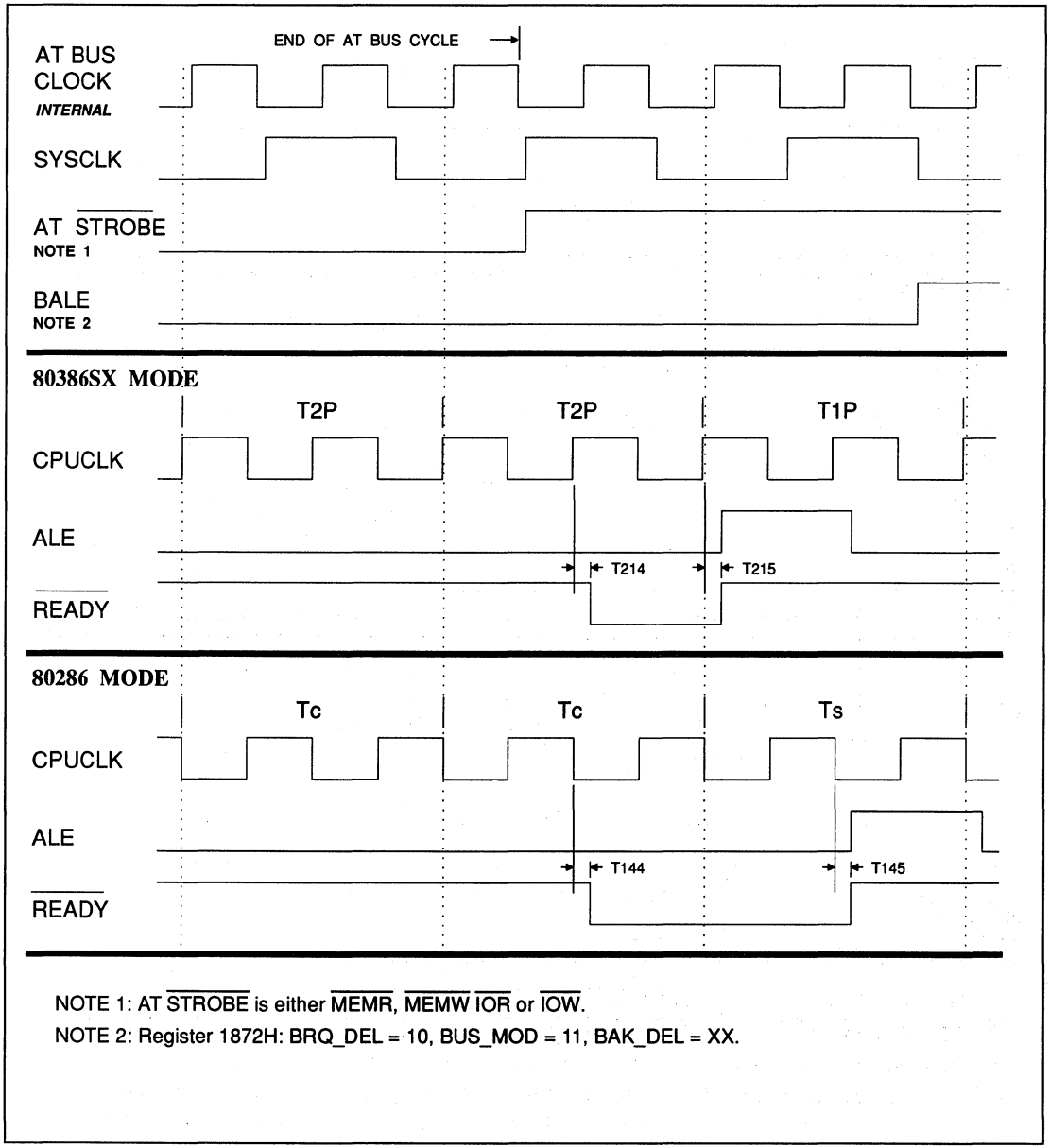
NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BUS_MOD = 10, BAK_DEL = 10 (-1 AT bus clock).

NOTE 3: Register 1872H: BUS_MOD = 10, BAK_DEL = 01 or 00 (-0.5 AT bus clock or no delay).

NOTE 4: Register 1872H: BUS_MOD = 10, BAK_DEL = 11 (+0.5 AT bus clock).

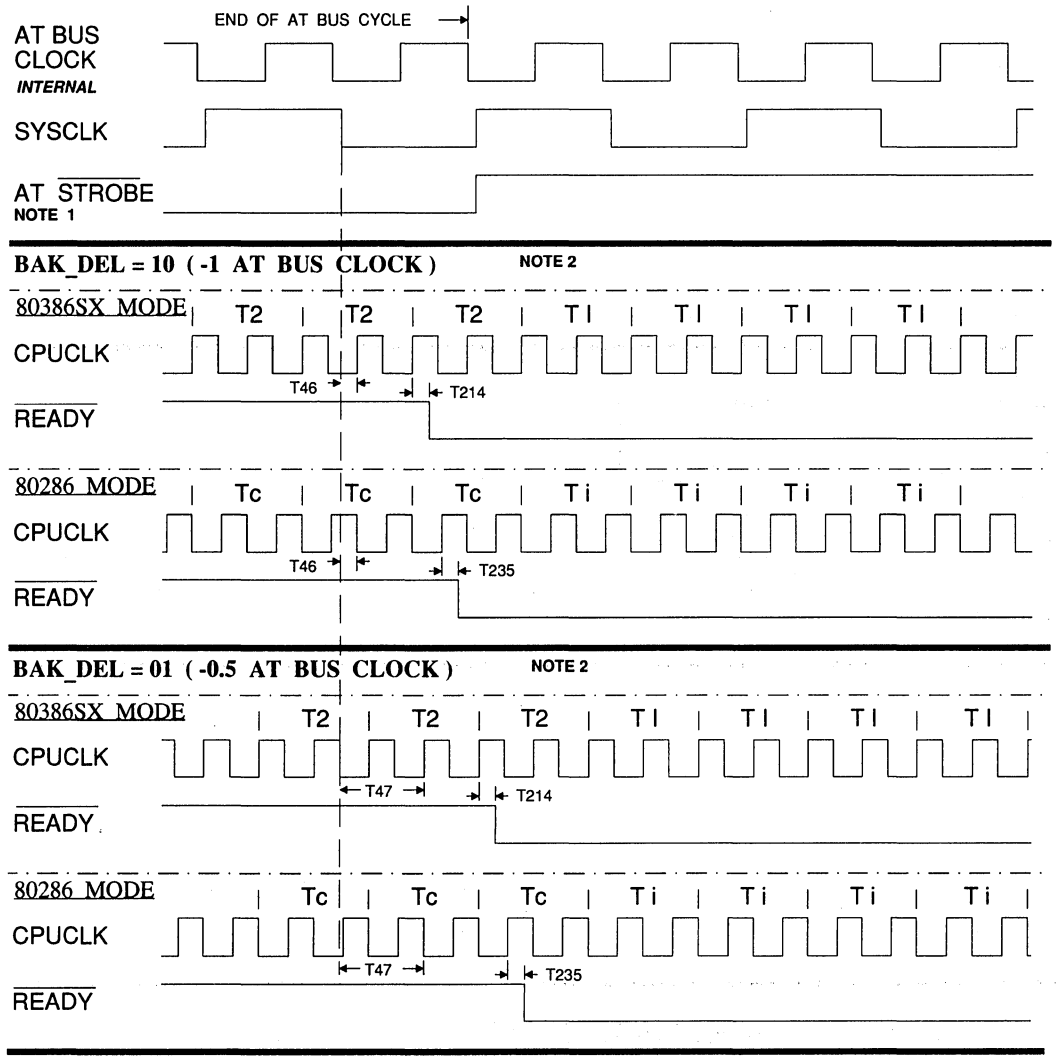
FIGURE 11-38. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 2



NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BRQ_DEL = 10, BUS_MOD = 11, BAK_DEL = XX.

FIGURE 11-39. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 1

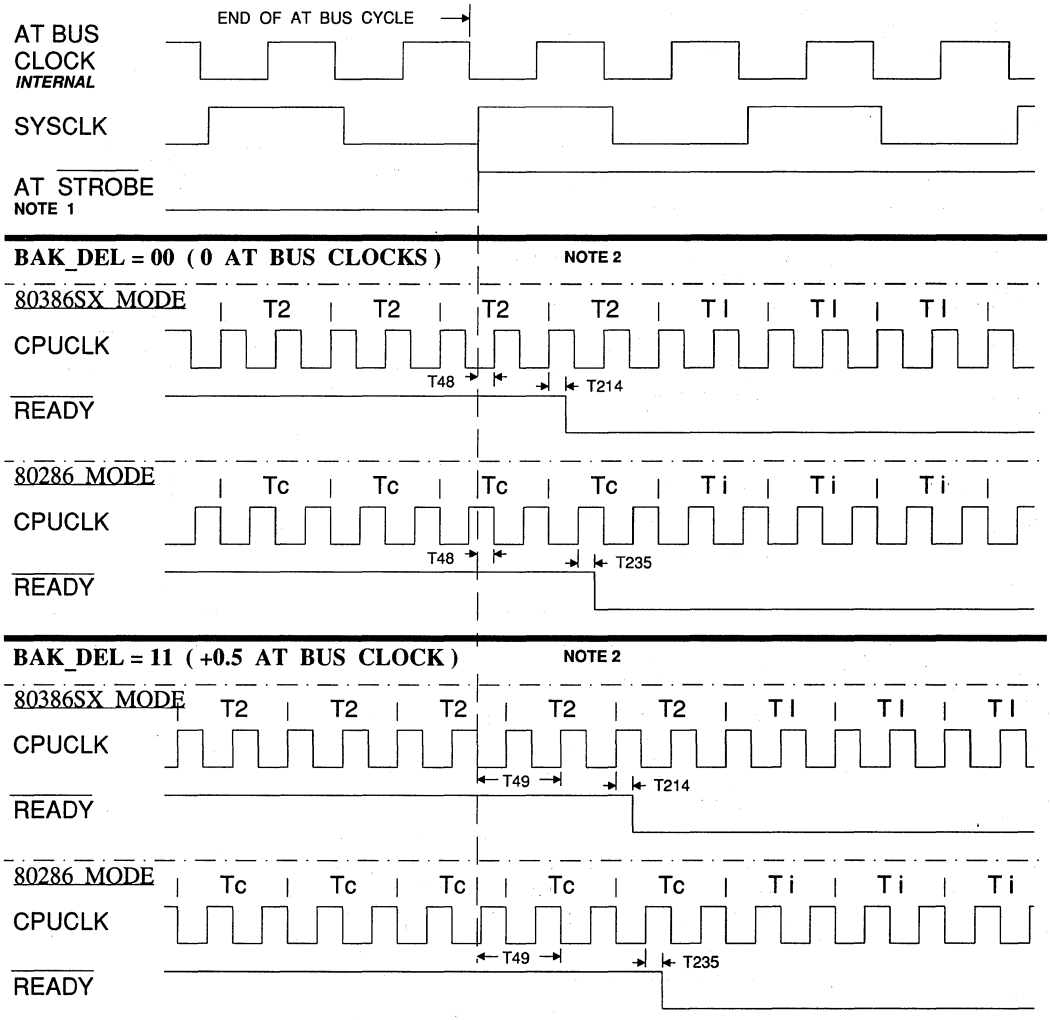


NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 11-40. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = -1 OR -0.5 AT BUS CLOCKS



NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 11-41. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = 0 OR +0.5 AT BUS CLOCKS

11.2.4 DMA Cycles

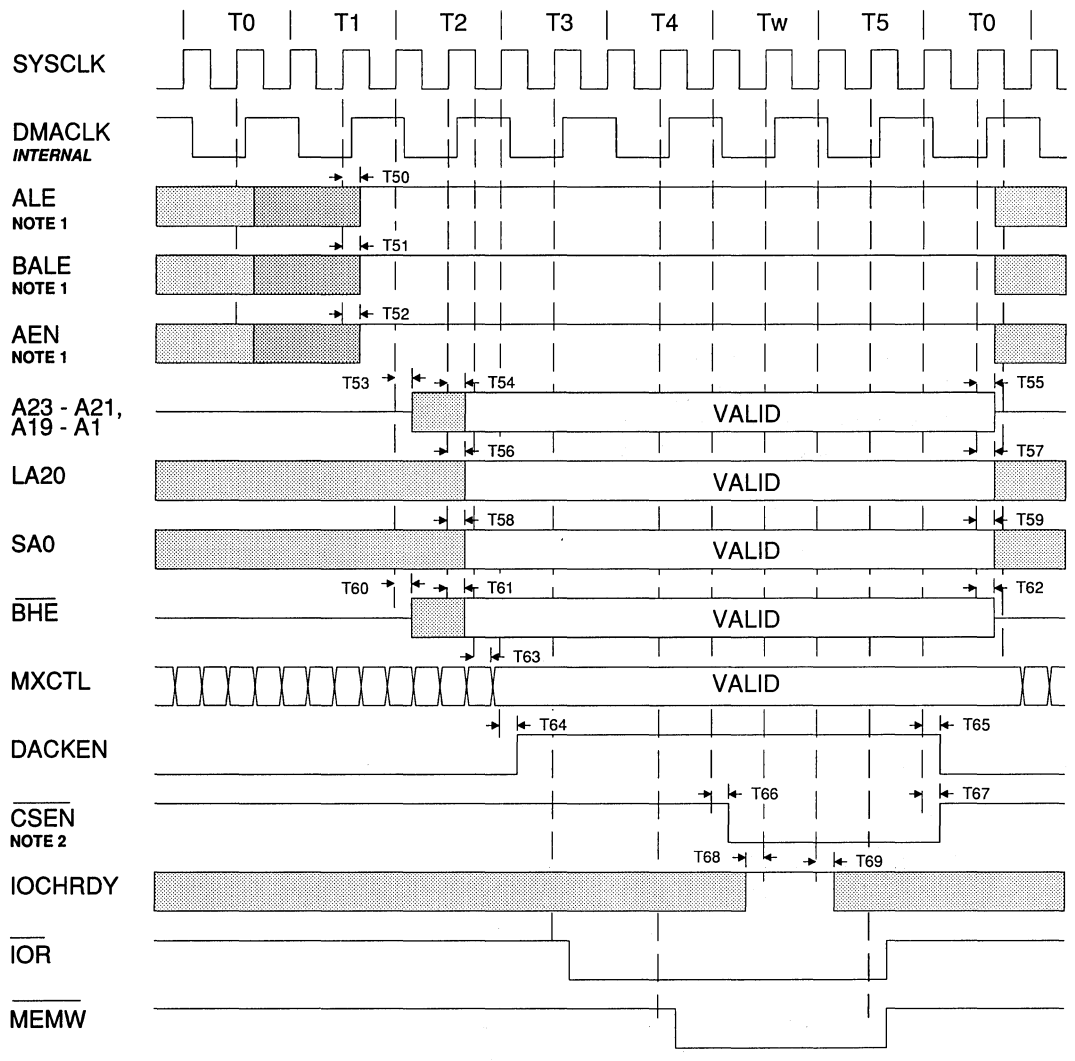
Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T54	SYSCLK rise to Address valid		60	ns	
T55	Address hold from SYSCLK rise	0		ns	
T56	SYSCLK rise to LA20 valid		49	ns	
T57	LA20 hold from SYSCLK rise	0		ns	
T58	SYSCLK rise to SA0 valid		40	ns	
T59	SA0 hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T66	SYSCLK rise to $\overline{CSEN}$ fall		32	ns	
T67	SYSCLK rise to $\overline{CSEN}$ rise		33	ns	
T68	IOCHRDY setup to SYSCLK rise	12		ns	
T69	IOCHRDY hold from SYSCLK rise	0		ns	
T70	SYSCLK rise to $\overline{IOR}$ fall		28	ns	
T71	SYSCLK rise to $\overline{IOR}$ rise		35	ns	
T72	SYSCLK rise to $\overline{MEMW}$ fall		47	ns	
T73	SYSCLK rise to $\overline{MEMW}$ rise		35	ns	
T74	SYSCLK rise to $\overline{DEN1}$ fall		32	ns	I/O to memory
T75	SYSCLK rise to $\overline{DEN1}$ rise		42	ns	I/O to memory
T76	SYSCLK rise to $\overline{DEN0}$ fall		32	ns	I/O to memory
T77	SYSCLK rise to $\overline{DEN0}$ rise		42	ns	I/O to memory
T78	SYSCLK rise to $\overline{SDEN}$ fall		21	ns	
T79	SYSCLK rise to $\overline{SDEN}$ rise		37	ns	I/O to memory

TABLE 11-11. DMA CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T80	SYSCLK rise to SDTR rise		30	ns	
T81	SYSCLK rise to SDTR fall		20	ns	
T82	SYSCLK rise to $\overline{IOW}$ fall		53	ns	
T83	SYSCLK rise to $\overline{IOW}$ rise		37	ns	
T84	SYSCLK rise to $\overline{MEMR}$ fall		17	ns	
T85	SYSCLK rise to $\overline{MEMR}$ rise		38	ns	
T86	SYSCLK rise to $\overline{DEN1}$ fall		22	ns	Memory to I/O
T87	SYSCLK rise to $\overline{DEN1}$ rise		116	ns	Memory to I/O
T88	SYSCLK rise to $\overline{DEN0}$ fall		22	ns	Memory to I/O
T89	SYSCLK rise to $\overline{DEN0}$ rise		116	ns	Memory to I/O
T90	SYSCLK rise to $\overline{SDEN}$ rise		116	ns	Memory to I/O
T91	SYSCLK rise to DTR rise		31	ns	
T92	SYSCLK rise to DTR fall		22	ns	
T100	$\overline{MEMW}$ fall to $\overline{RAS}$n fall		27	ns	
T101	$\overline{MEMW}$ rise to $\overline{RAS}$n rise		29	ns	
T102	$\overline{MEMW}$ fall to $\overline{CAS}$n fall		108	ns	
T103	$\overline{MEMW}$ rise to $\overline{CAS}$n rise		30	ns	
T105	$\overline{MEMW}$ fall to RA10 - RA0 valid		100	ns	
T107	$\overline{MEMW}$ fall to W/$\overline{R}$ high		29	ns	
T108	$\overline{MEMW}$ rise to W/$\overline{R}$ low	10		ns	
T120	$\overline{MEMR}$ fall to $\overline{RAS}$n fall		28	ns	
T121	$\overline{MEMR}$ rise to $\overline{RAS}$ rise		29	ns	
T122	$\overline{MEMR}$ fall to $\overline{CAS}$n fall		110	ns	
T123	$\overline{MEMR}$ rise to $\overline{CAS}$ rise		31	ns	
T125	$\overline{MEMR}$ fall to RA10 - RA0 valid		100	ns	
T126	$\overline{MEMR}$ fall to DPH, DPL float		25		
T127	$\overline{MEMR}$ rise to DPH, DPL driven	35			
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T305	D15 - D0 setup to $\overline{MEMR}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{MEMR}$ rise	10		ns	

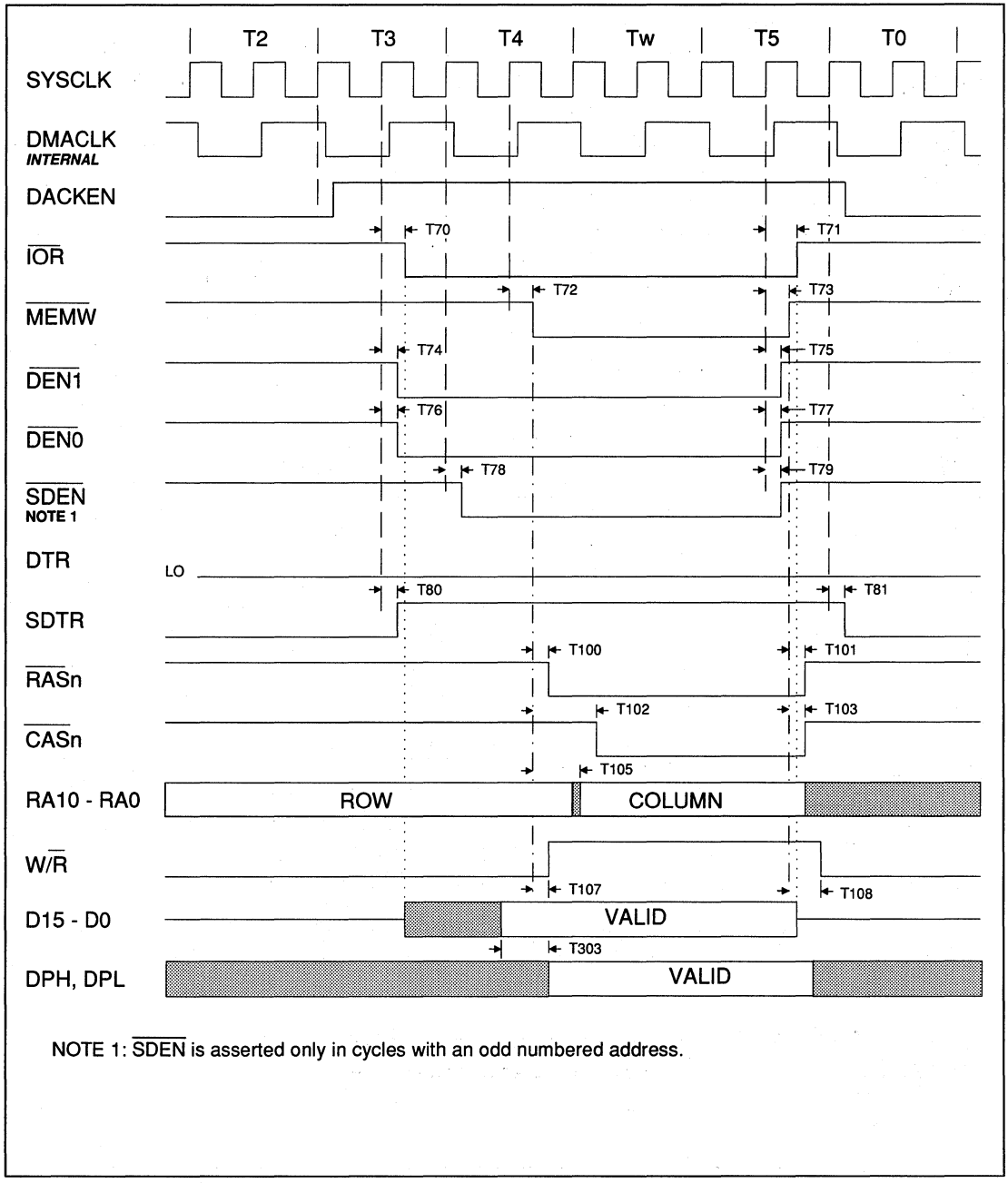
TABLE 11-11. DMA CYCLES cont.



NOTE 1: ALE, BALE and AEN may be asynchronous. Minimum valid time is shown. DMA channels 0, 1, 2, and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

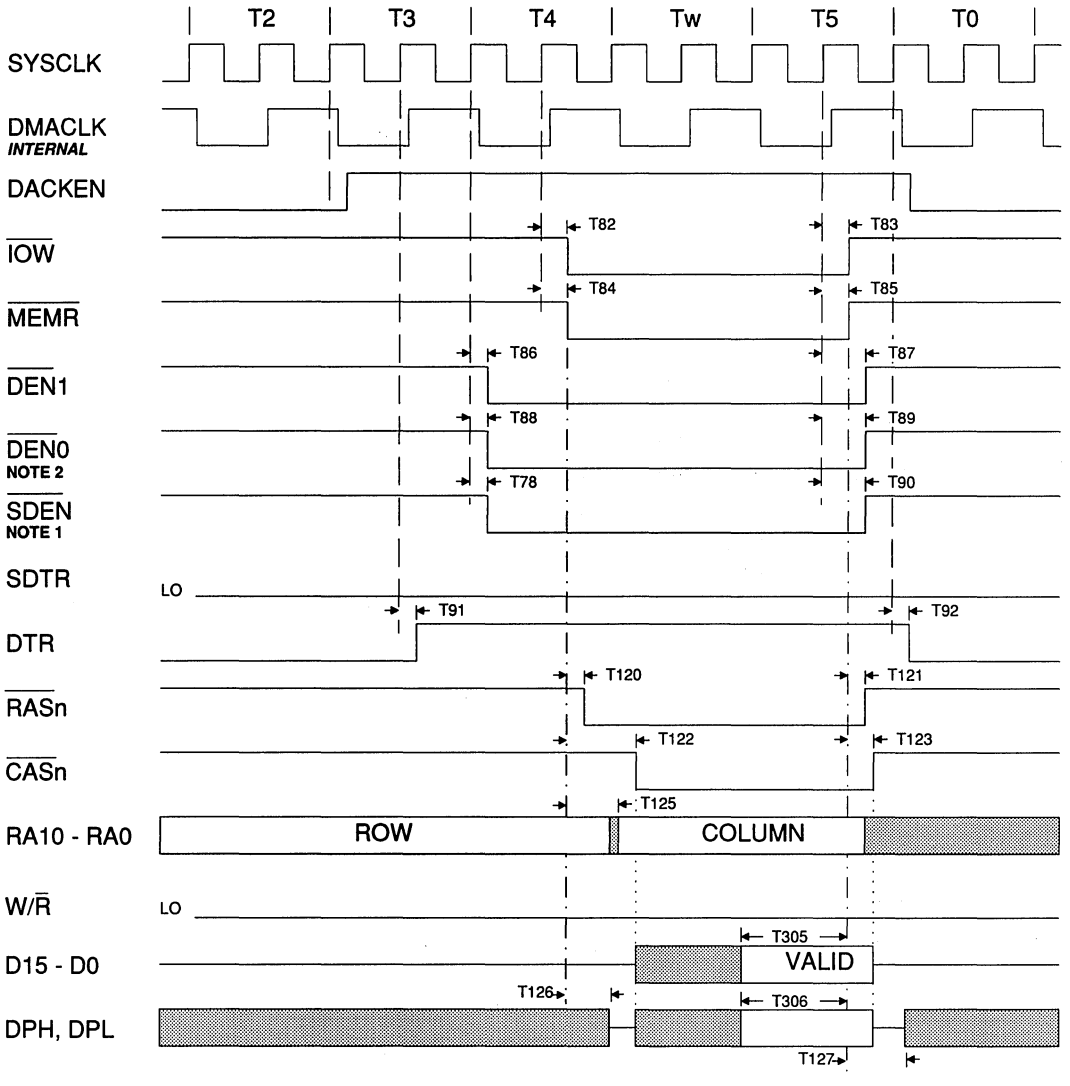
NOTE 2: $\overline{\text{CSEN}}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

FIGURE 11-42. BASIC DMA CYCLE, DEFAULT TIMING



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.

FIGURE 11-43. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.
NOTE 2: $\overline{\text{DEN0}}$ is asserted only in cycles with an even numbered address.

FIGURE 11-44. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O

11.2.5 AT Bus Master

The AT bus master timing is covered in the following sequence:

- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T55	Address hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T150	$\overline{MASTER}$ fall to AEN fall		30	ns	
T151	$\overline{MASTER}$ rise to AEN rise		30	ns	
T152	$\overline{MASTER}$ fall to A23 - A21, A19 - A1 float		30	ns	
T153	$\overline{MASTER}$ rise to A23 - A21, A19 - A1 driven	15		ns	
T154	$\overline{MASTER}$ fall to LA20 float		23	ns	
T155	$\overline{MASTER}$ rise to LA20 driven	10		ns	
T156	$\overline{MASTER}$ fall to SA0 float		24	ns	
T157	$\overline{MASTER}$ rise to SA0 driven	10		ns	
T158	$\overline{MASTER}$ fall to $\overline{BHE}$ float		30	ns	
T159	$\overline{MASTER}$ rise to $\overline{BHE}$ driven	10		ns	
T160	$\overline{MASTER}$ fall to $\overline{CSEN}$ fall		32	ns	
T161	$\overline{MASTER}$ rise to $\overline{CSEN}$ rise		35	ns	
T162	$\overline{MASTER}$ fall to $\overline{MEMR}$ float		24	ns	
T163	$\overline{MASTER}$ rise to $\overline{MEMR}$ driven	10		ns	
T164	$\overline{MASTER}$ fall to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, float		23	ns	
T165	$\overline{MASTER}$ rise to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$ driven	10		ns	

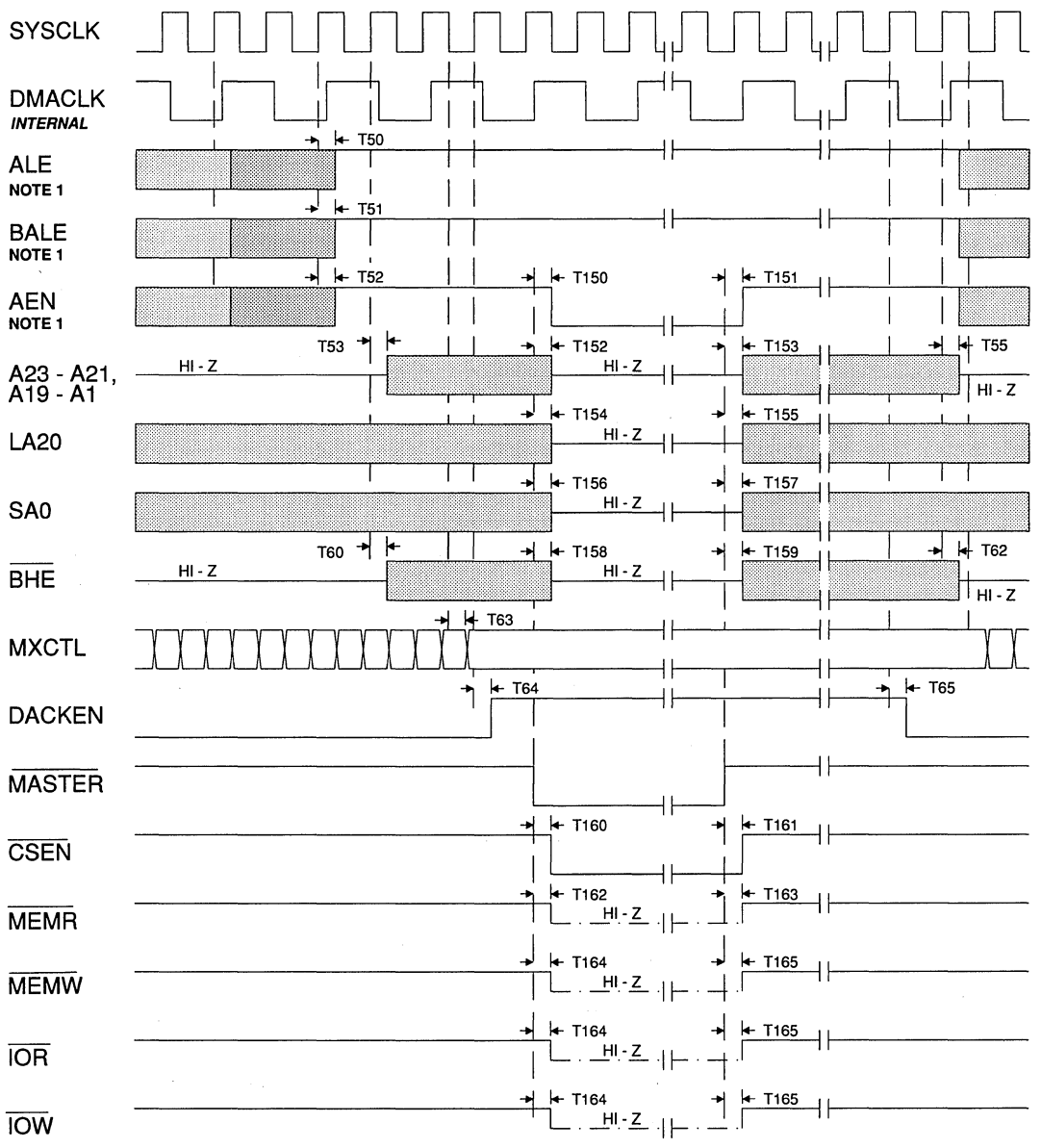
TABLE 11-12. AT BUS MASTER CYCLE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T166	A23 - A21, A19 - A1 setup to MEMR, MEMW	45		ns	
T167	LA20 setup to MEMR, MEMW	50		ns	
T168	BHE setup to MEMR, MEMW	0		ns	
T169	SA0 setup to MEMR, MEMW	0		ns	
T170	A23 - A21, A19 - A1 hold from MEMR, MEMW	15		ns	
T171	LA20 hold from MEMR, MEMW	15		ns	
T172	BHE hold from MEMR, MEMW	15		ns	
T173	SA0 hold from MEMR, MEMW	15		ns	
T174	SA0 in to A0 out delay		45	ns	
T175	MEMW fall to DEN1 fall		30	ns	
T176	MEMW fall to DEN0 fall		30	ns	
T177	MEMW rise to DEN1 rise		83	ns	
T178	MEMW rise to DEN0 rise		83	ns	
T179	MEMR fall to DEN1 fall		85	ns	
T180	MEMR fall to DEN0 fall		85	ns	
T181	MEMR rise to DEN1 rise		32	ns	
T182	MEMR rise to DEN0 rise		32	ns	
T183	MEMR fall to DTR rise		29	ns	
T184	MEMR rise to DTR fall		82	ns	
T190	MEMR, MEMW fall to RASn fall		83	ns	
T191	MEMR, MEMW rise to RASn rise		33	ns	
T192	MEMR, MEMW fall to CASn fall		126	ns	
T193	MEMR, MEMW rise to CASn rise		33	ns	
T194	MEMR, MEMW fall to RA10 - RA0 column address valid		120	ns	
T196	MEMR, MEMW fall to RA10 - RA0 row address valid		42	ns	
T197	RA10 - RA0 column address hold from MEMR, MEMW rise	5		ns	

TABLE 11-12. AT BUS MASTER CYCLE cont.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T300	$\overline{MEMW}$ fall to W/$\overline{R}$ rise		33	ns	
T301	$\overline{MEMW}$ rise to W/$\overline{R}$ fall	10		ns	
T302	$\overline{MEMW}$ fall to DPH, DPL valid		32	ns	
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T304	DPH, DPL hold from $\overline{MEMW}$ rise	5		ns	
T305	D15 - D0 setup to $\overline{MEMR}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{MEMR}$ rise	10		ns	
T307	$\overline{MEMR}$ fall to DPH, DPL float		35	ns	
T308	$\overline{MEMR}$ rise to DPH, DPL driven	58		ns	

TABLE 11-12. AT BUS MASTER CYCLE cont.



NOTE 1: The shaded regions of ALE, BALE and AEN show a possible asynchronous relarionship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

FIGURE 11-45. AT BUS MASTER, BUS ACQUISITION/RELEASE

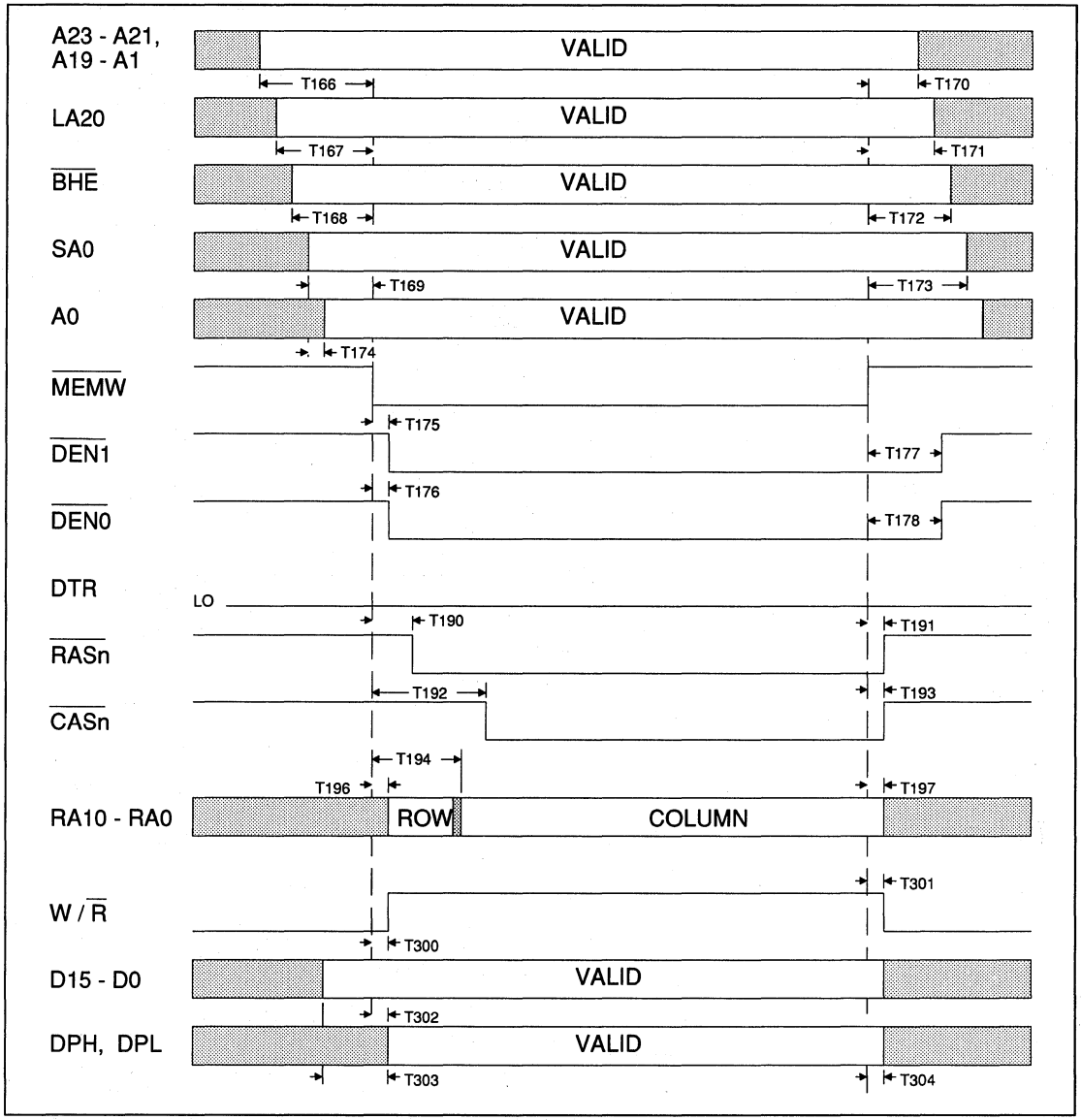


FIGURE 11-46. AT BUS MASTER, WRITE TO ON-BOARD MEMORY

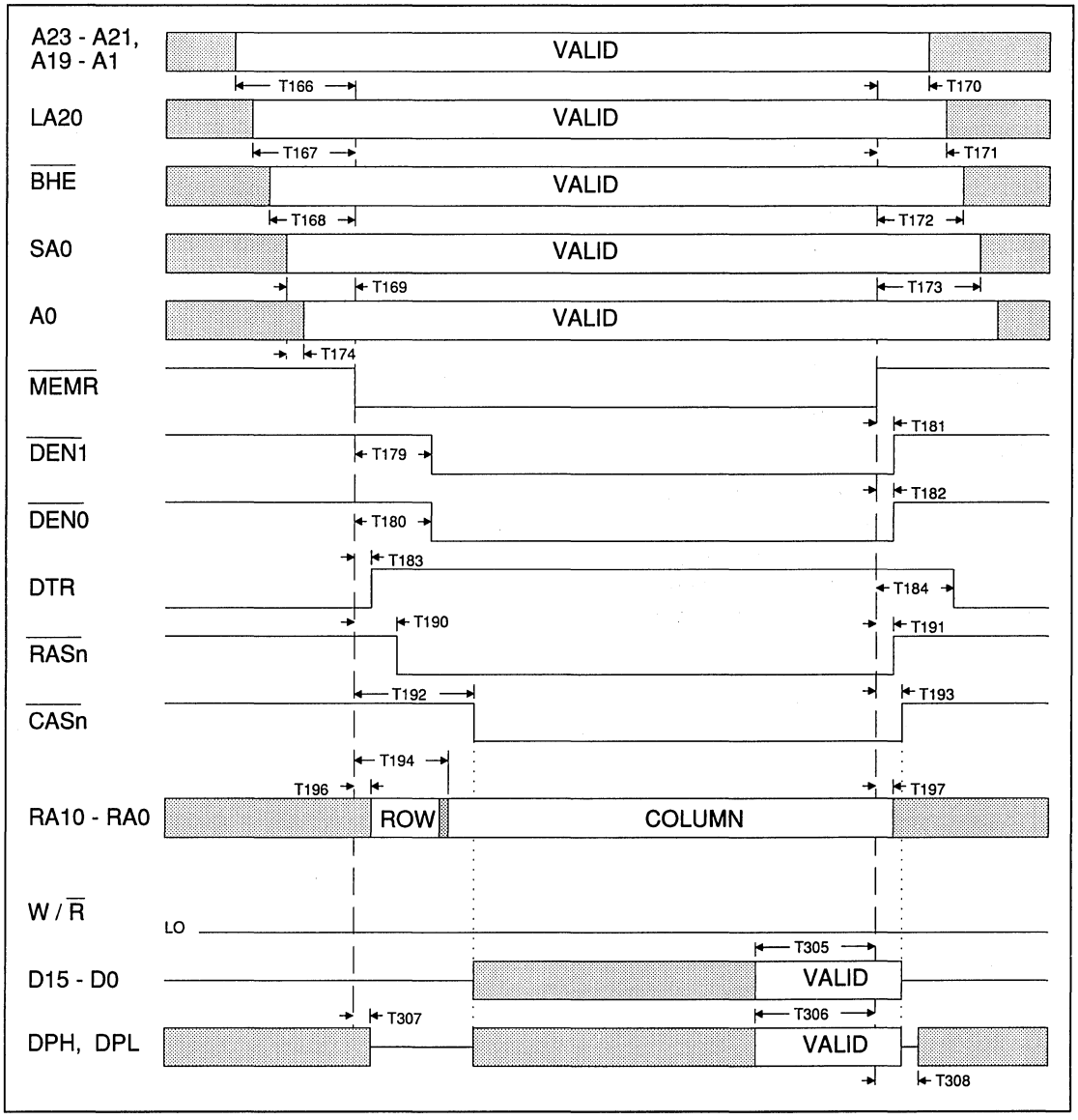
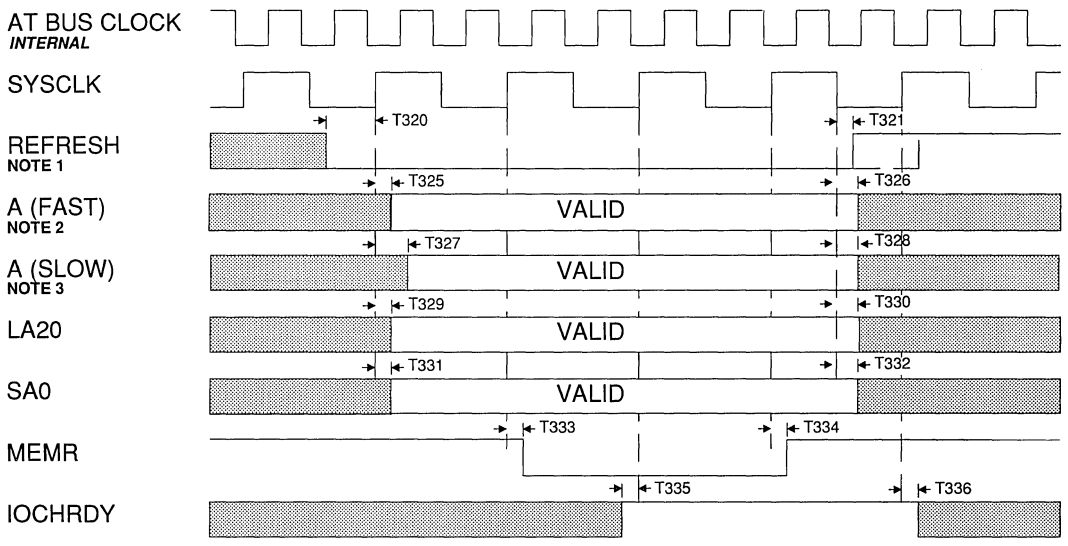


FIGURE 11-47. AT BUS MASTER, READ FROM ON-BOARD MEMORY

11.2.6 AT Bus Refresh

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T320	$\overline{\text{REFRESH}}$ low before SYSCLK rise	4		ns	$\overline{\text{REFRESH}}$ setup is number given plus (T00 × 0.25)
T321	SYSCLK fall to $\overline{\text{REFRESH}}$ rise		16	ns	
T325	SYSCLK rise to A23 - A21, A19 - A16 and A7 - A1 valid		35	ns	
T326	SYSCLK fall to A23 - A21, A19 - A16 and A7 - A1 invalid	2		ns	
T327	SYSCLK rise to A20, A15 - A8 valid		45	ns	
T328	SYSCLK fall to A20, A15 - A8 invalid	2		ns	
T329	SYSCLK rise to LA20 valid		30	ns	
T330	SYSCLK fall to LA20 invalid	2		ns	
T331	SYSCLK rise to SA0 valid		30	ns	
T332	SYSCLK fall to SA0 invalid	2		ns	
T333	SYSCLK rise to $\overline{\text{MEMR}}$ low		8	ns	
T334	SYSCLK rise to $\overline{\text{MEMR}}$ high		7	ns	
T335	IOCHRDY setup to SYSCLK rise	23		ns	
T336	IOCHRDY hold time from SYSCLK rise	0		ns	

TABLE 11-13. AT BUS REFRESH CYCLE, DEFAULT TIMING



NOTE 1: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

NOTE 2: (FAST) is address lines A23 - A21, A19 - A16 and A7 - A1.

NOTE 3: (SLOW) is address lines A20, and A15 - A8

FIGURE 11-48. AT BUS REFRESH CYCLE, DEFAULT TIMING

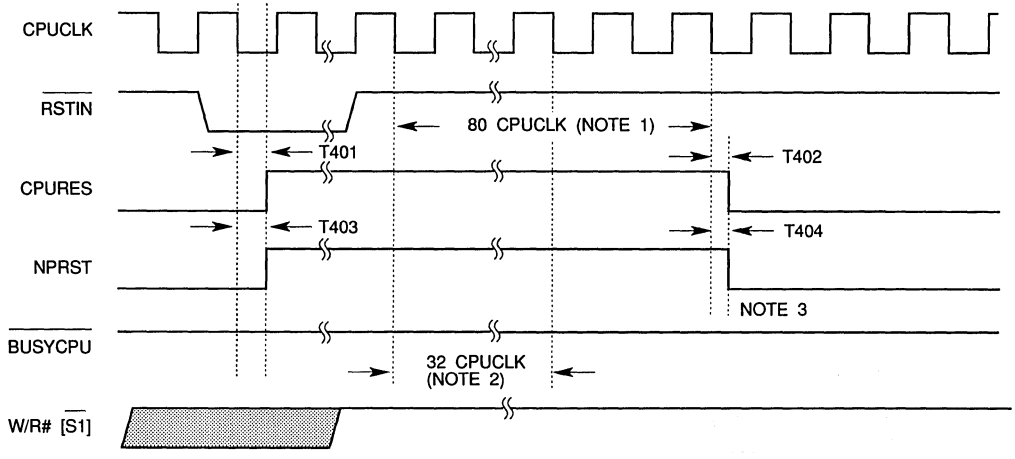
11.3 PROCESSOR TIMING

This section covers the 80286 CPU timing, followed by the 80386SX.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T140	See Table 11-9				
T141	See Table 11-9				
T143	See Table 11-9				
T401	CPUCLK fall to CPURES rise delay		14	ns	
T402	CPUCLK fall to CPURES fall delay		13	ns	
T403	CPUCLK fall to NPRST rise delay		14	ns	
T404	CPUCLK fall to NPRST fall delay		13	ns	
T405	CPUCLK fall to $\overline{\text{BUSYCPU}}$ fall delay		35	ns	①
T406	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35	ns	①
T408	$\overline{\text{SO}}$, $\overline{\text{S1}}$ setup time to CPUCLK	9		ns	
T409	$\overline{\text{SO}}$, $\overline{\text{S1}}$ hold time to CPUCLK	1		ns	
T410	M/$\overline{\text{IO}}$ setup time to CPUCLK	26		ns	
T411	M/$\overline{\text{IO}}$ hold time to CPUCLK	1		ns	
T412	Address setup time to CPUCLK	26		ns	
T413	Address hold time to CPUCLK	1		ns	
T414	$\overline{\text{PEACK}}$ setup time to CPUCLK	7		ns	
T415	$\overline{\text{PEACK}}$ hold time to CPUCLK	1		ns	
T416	DPH, DPL setup time to CPUCLK fall	5		ns	
T417	DPH, DPL hold time from CPUCLK fall	19		ns	
T418	D15 - D0 setup time to CPUCLK fall	5		ns	
T419	D15 - D0 hold time from CPUCLK fall	19		ns	

① T405 and T406 are for reference only since $\overline{\text{BUSYCPU}}$ is an asynchronous signal to the 80286. These two parameters are guaranteed by design and will not be tested.

TABLE 11-14. 80286 CPU TIMING

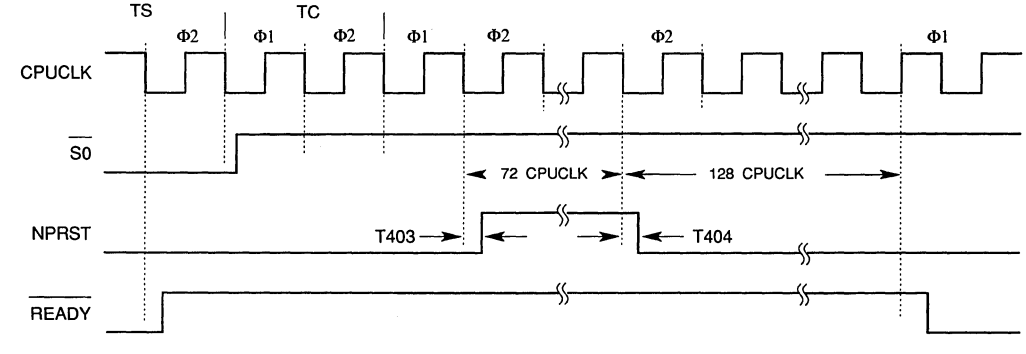


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

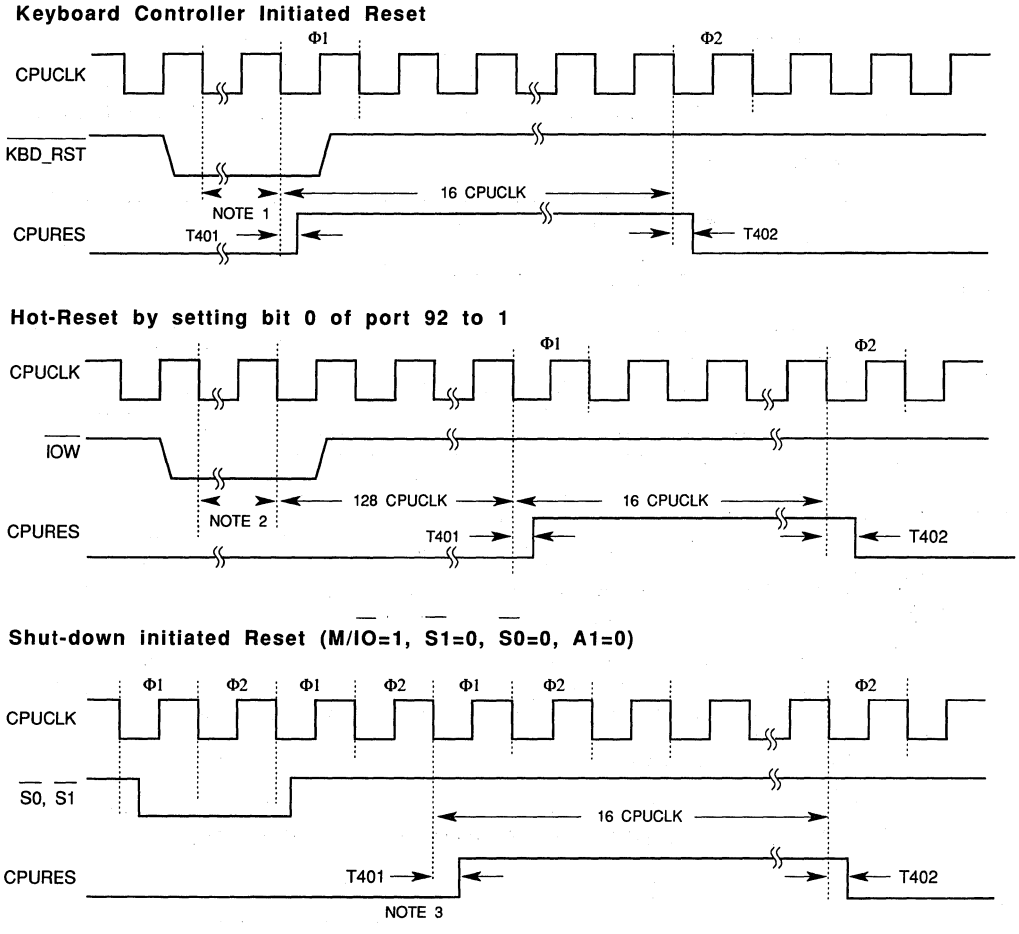
FIGURE 11-49. 80286 - CPURES AND NPRST DURING POWER UP



NOTE 1: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 2: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's C287A.

FIGURE 11-50. 80286 - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1

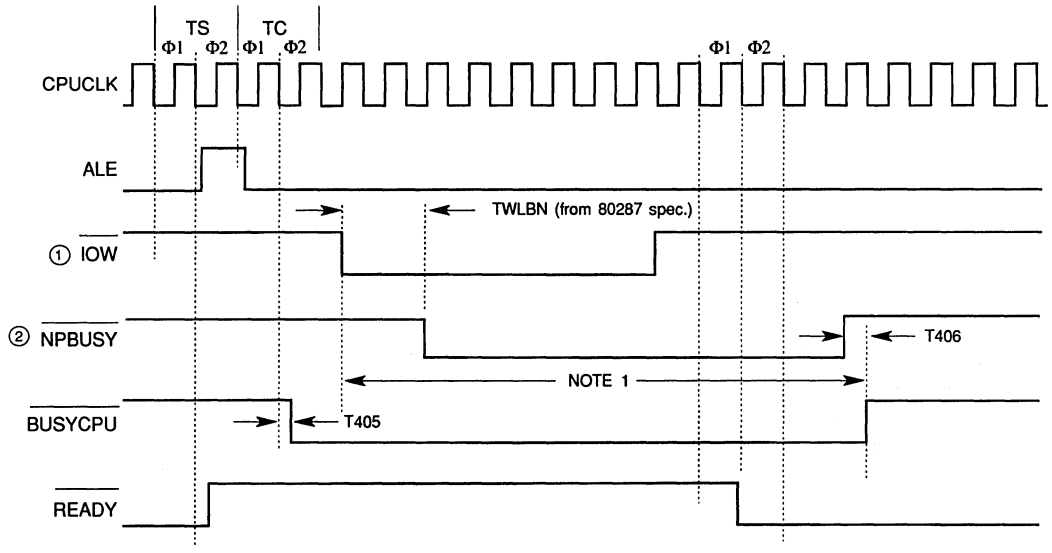


NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is asserted at the beginning of phase 1 to maintain the phase relationship with the 80286.

FIGURE 11-51. 80286 - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

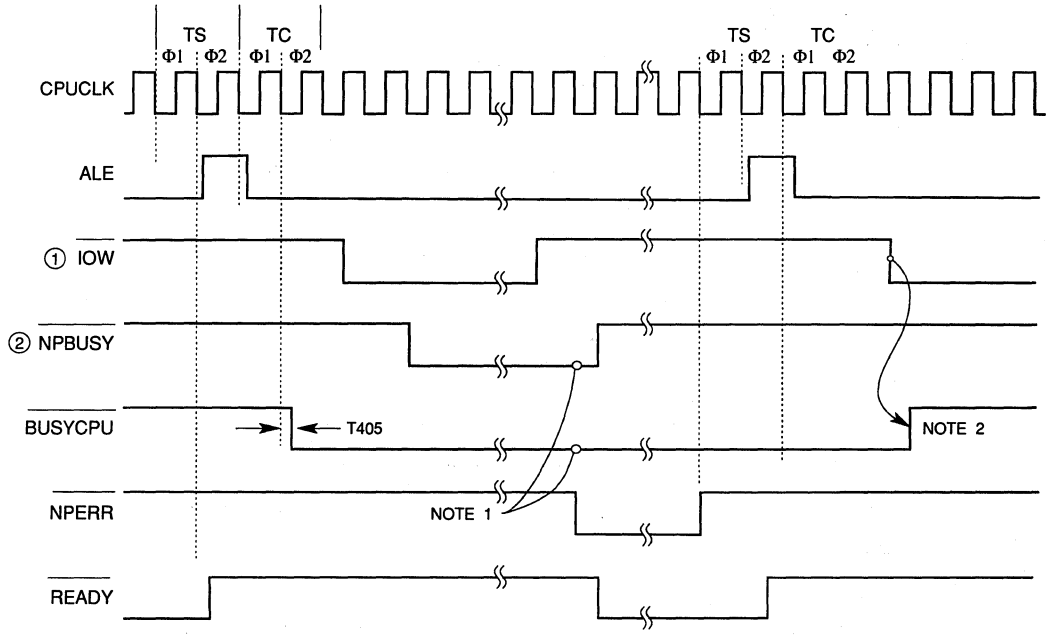


① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: During a write to the 80287, $\overline{\text{BUSYCPU}}$ is asserted at the middle of the first Tc and continues for one SYSCLK plus two CPUCLKs beyond the active edge of $\overline{\text{IOW}}$, then follows the $\overline{\text{NPBUSY}}$ from the 80287. This early assertion of $\overline{\text{BUSYCPU}}$ is required to maintain compatibility with the 80287.

FIGURE 11-52. 80286 - $\overline{\text{BUSYCPU}}$ ASSERTED DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: $\overline{\text{BUSYCPU}}$ is latched by the leading edge of the $\overline{\text{NPERR}}$ signal from the coprocessor while $\overline{\text{NPBUSY}}$ from the coprocessor is still active.

NOTE 2: $\overline{\text{BUSYCPU}}$ is de-asserted by the leading edge of $\overline{\text{IOW}}$, delayed by a low half of SYSCLK, when any data is written to port F0. $\overline{\text{BUSYCPU}}$ can be an asynchronous signal to the processor and is shown for reference only.

FIGURE 11-53. 80286 - LATCHING $\overline{\text{BUSYCPU}}$ WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

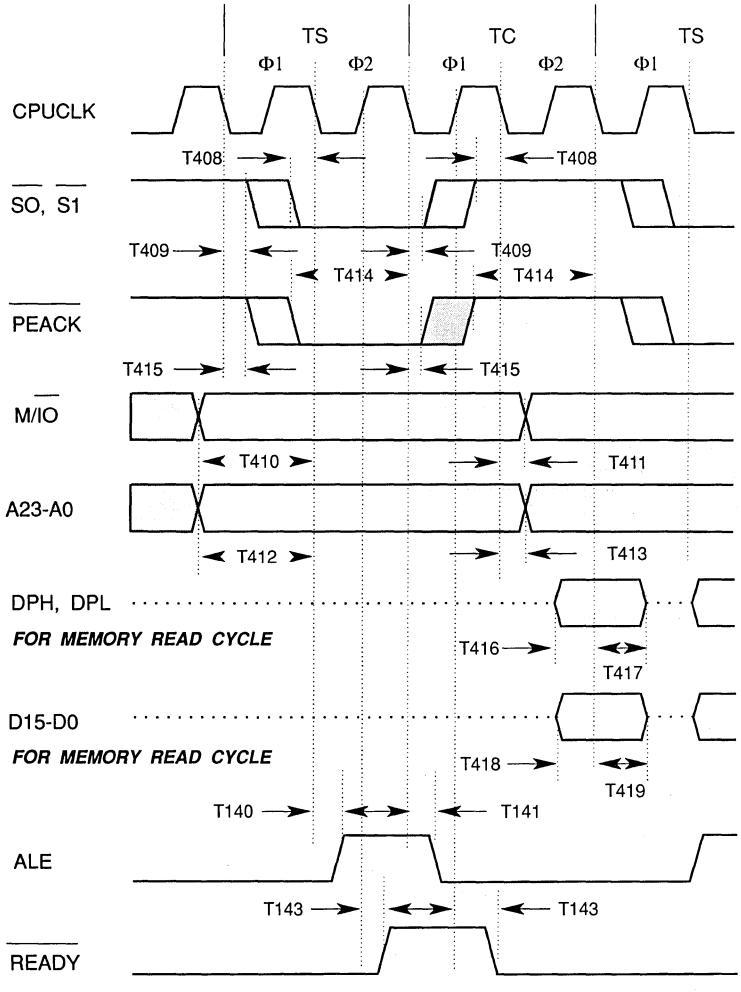


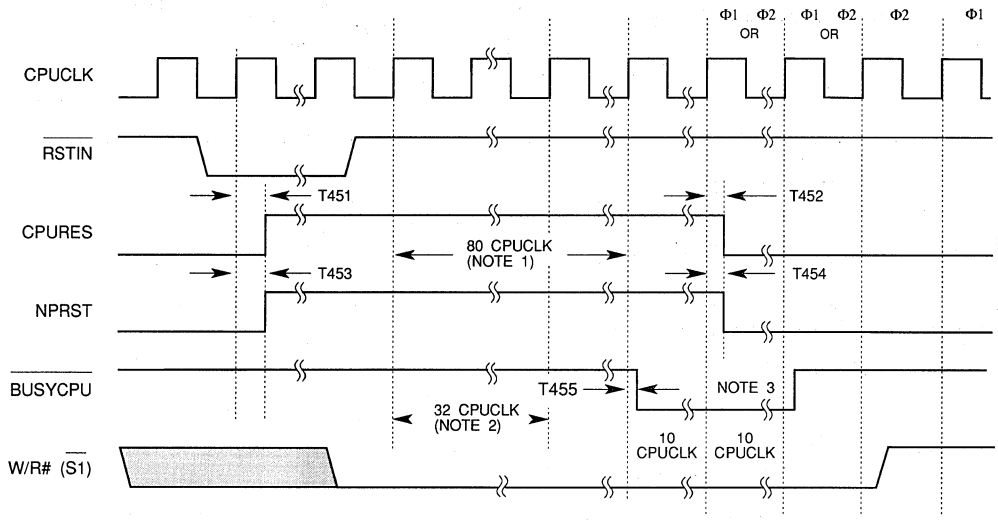
FIGURE 11-54. 80286 - MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	20 MHz		25 MHz		UNITS
		MIN	MAX	MIN	MAX	
T140	See Table 11-9					
T141	See Table 11-9					
T204	See Table 11-6					
T214	See Table 11-6					
T215	See Table 11-6					
T451	CPUCLK rise to CPURES rise delay		14		10	ns
T452	CPUCLK rise to CPURES fall delay		13		10	ns
T453	CPUCLK rise to NPRST rise delay		14		10	ns
T454	CPUCLK rise to NPRST fall delay		13		10	ns
T455	CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay		35		35	ns
T456	CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay		35		30	ns
T457	$\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay		30		30	ns
T458	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35		35	ns
T460	$\overline{\text{NPERR}}$ fall to EPEREQ rise delay		30		30	ns
T462	ADS# setup time to CPUCLK rise *	14		10		ns
T463	ADS# hold time from CPUCLK rise	5		4		ns
T464	W/R# setup time to CPUCLK rise *	14		8		ns
T465	W/R# hold time from CPUCLK rise	5		4		ns
T466	D/C# setup time to CPUCLK rise *	14		6		ns
T467	D/C# hold time from CPUCLK rise	5		4		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise *	17		15		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	5		4		ns
T470	$\overline{\text{BHE}}$ setup time to CPUCLK rise	17		15		ns
T471	$\overline{\text{BHE}}$ hold time from CPUCLK rise	3		4		ns

TABLE 11-15. 80386SX CPU TIMING

SYMBOL	CHARACTERISTIC	20 MHz		25 MHz		UNITS
		MIN	MAX	MIN	MAX	
T472	HLDA setup time to CPUCLK rise *	10		6		ns
T473	HLDA hold time from CPUCLK rise	3		4		ns
T474	HOLD valid delay from CPUCLK rise *		26		20	ns
T475	DPH setup time to CPUCLK rise	5		5		ns
T476	DPH hold time from CPUCLK rise	19		19		ns
T477	D15-D0 setup time to CPUCLK rise	5		5		ns
T478	D15-D0 hold time from CPUCLK rise	19		19		ns
T479	A23-A1, BLE# setup time to CPUCLK rise *	40		38		ns
T480	A23-A1, BLE# hold time from CPUCLK rise	3		4		ns

TABLE 11-15. 80386SX CPU TIMING cont.

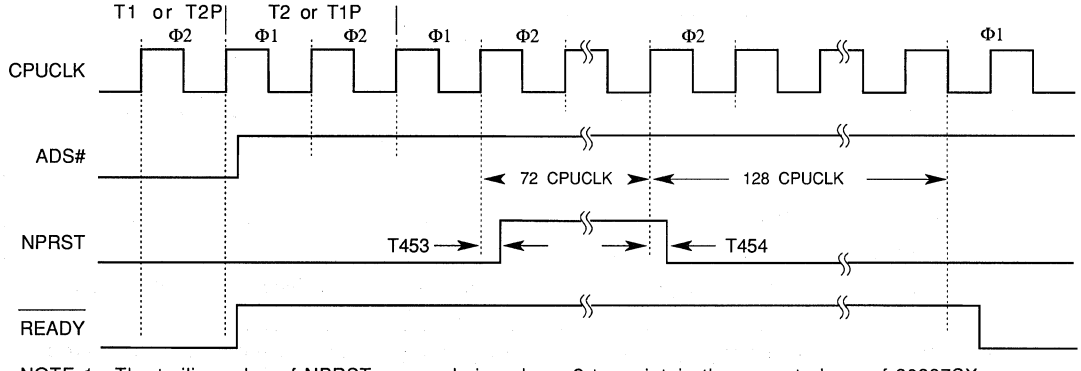


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

FIGURE 11-55. 80386SX - CPURES AND NPRST DURING POWER UP



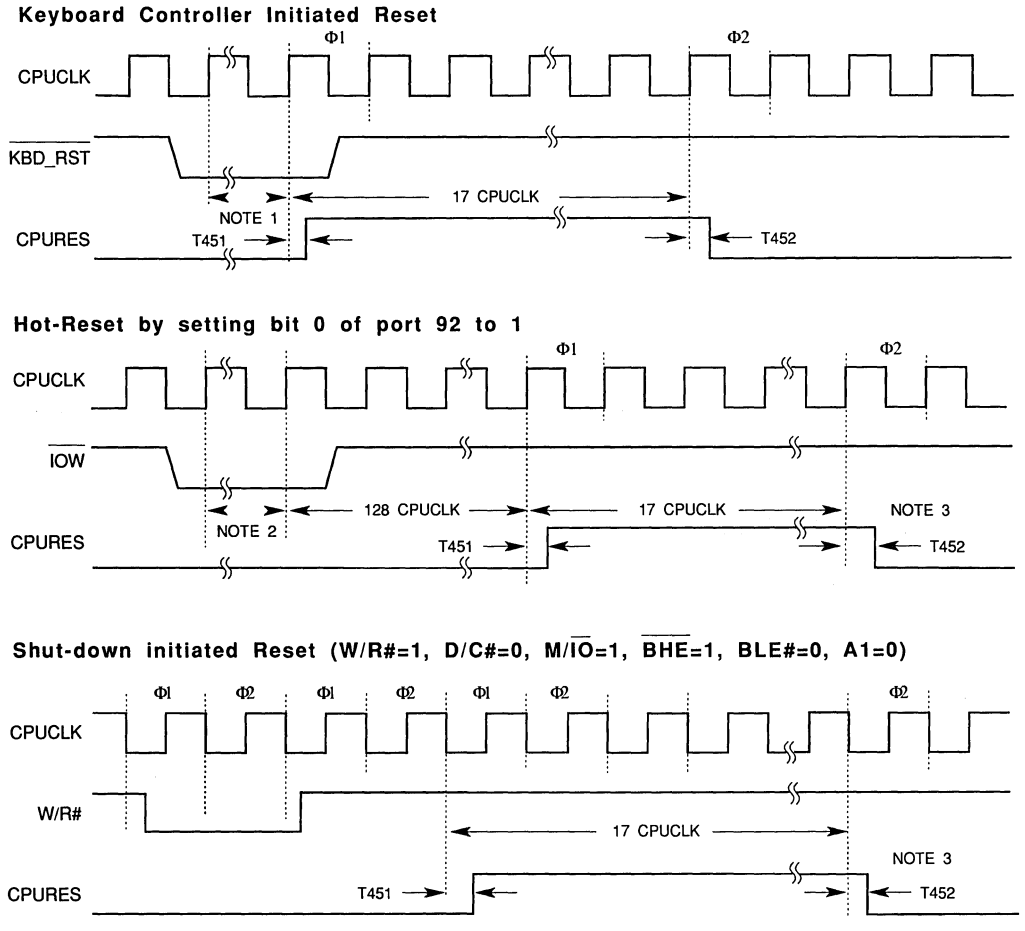
NOTE 1: The trailing edge of NPRST occurs during phase 2 to maintain the correct phase of 80387SX with the 80386SX.

NOTE 2: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 3: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's 80C287A.

NOTE 4: 25 MHz operation requires a minimum of 8 MHz for AT Bus Clock.

FIGURE 11-56. 80386SX - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1



NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

FIGURE 11-57. 80386SX - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

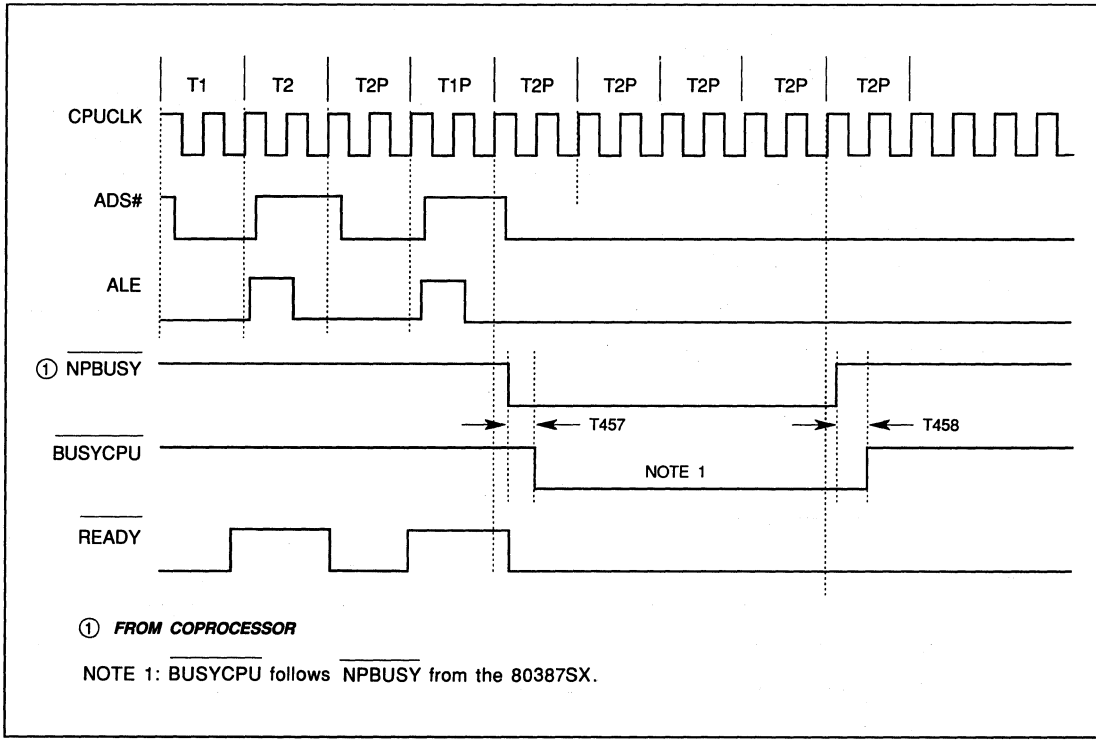
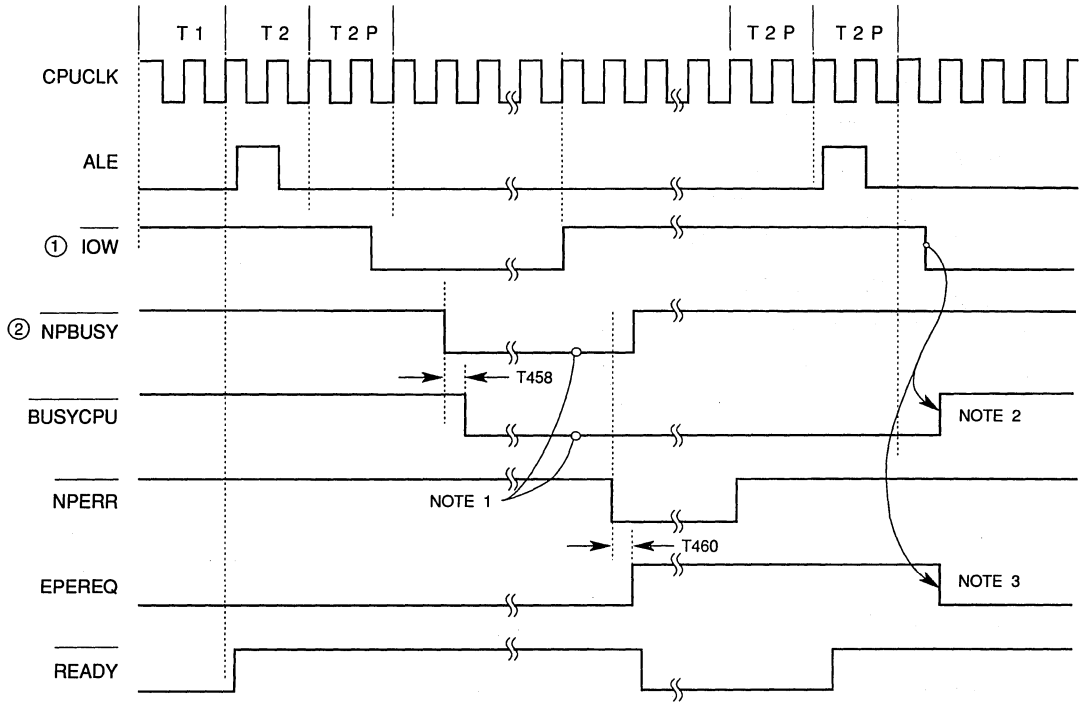


FIGURE 11-58. 80386SX - $\overline{\text{BUSYCPU}}$ ASSERTION DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW delayed by a low half of SYSCLK when any data is written to port F0H. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

NOTE 3: EPEREQ is asserted if NPERR occurs while NPBUSY from the coprocessor is active. EPEREQ is de-asserted by the leading edge of IOW delayed by the low half of SYSCLK when any data is written to port F0H. EPEREQ can be asynchronous to the processor and is shown for reference only.

FIGURE 11-59. 80386SX - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

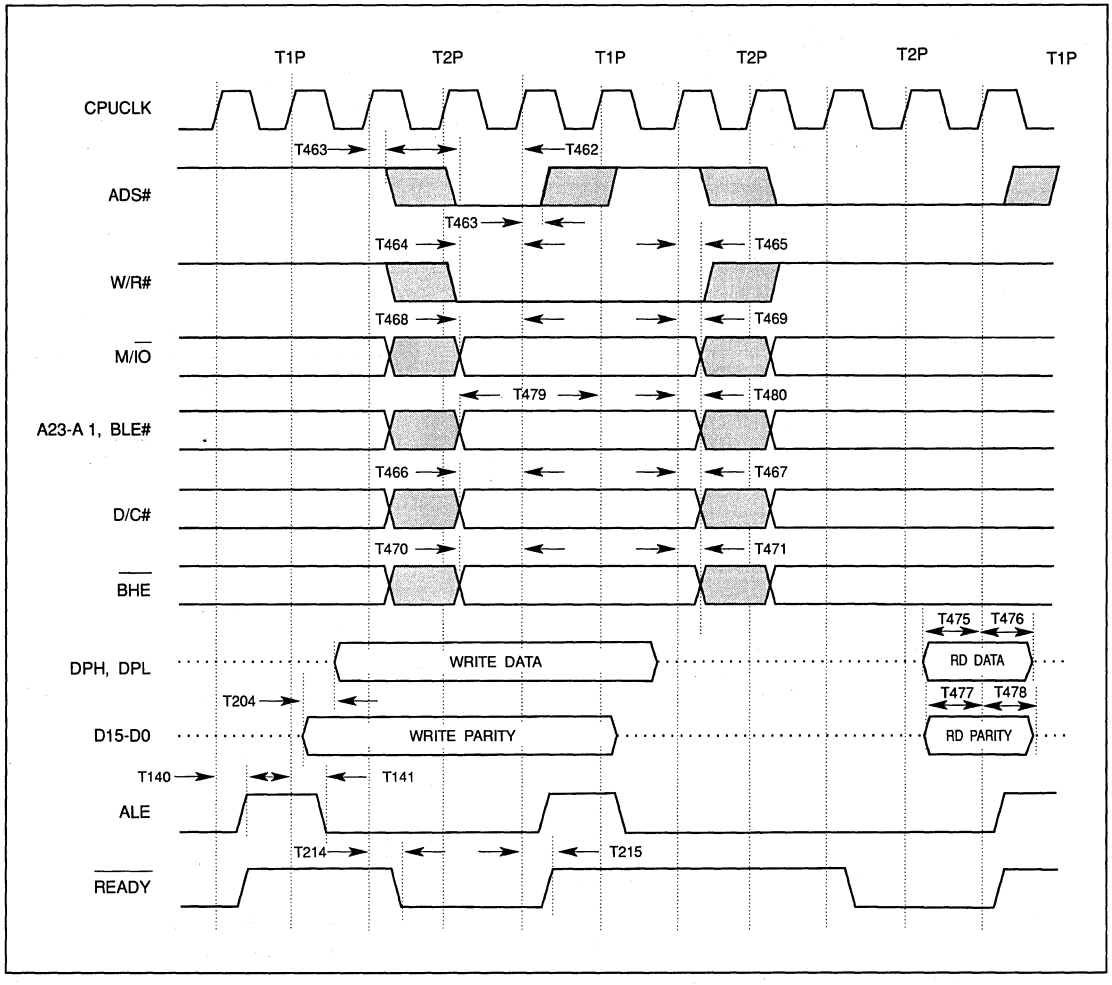


FIGURE 11-60. 80386SX - MISCELLANEOUS TIMING

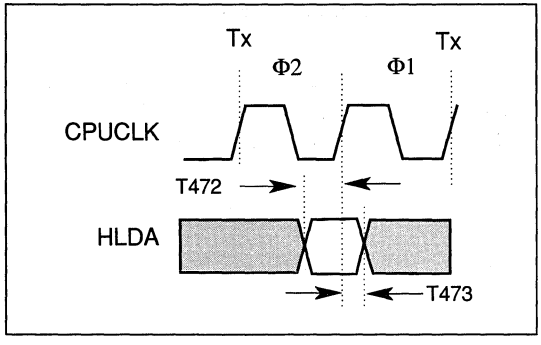


FIGURE 11-61. 80386SX - INPUT SETUP AND HOLD TIMING

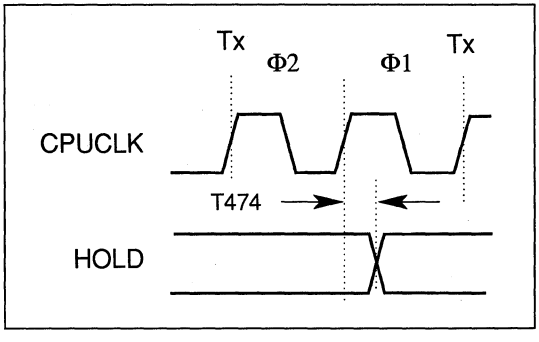


FIGURE 11-62. 80386SX - OUTPUT DELAY TIMING

12.0 PACKAGE DIMENSIONS

Figure 12-1 Illustrates the 132-Pin PQFP package showing the dimensions in inches.

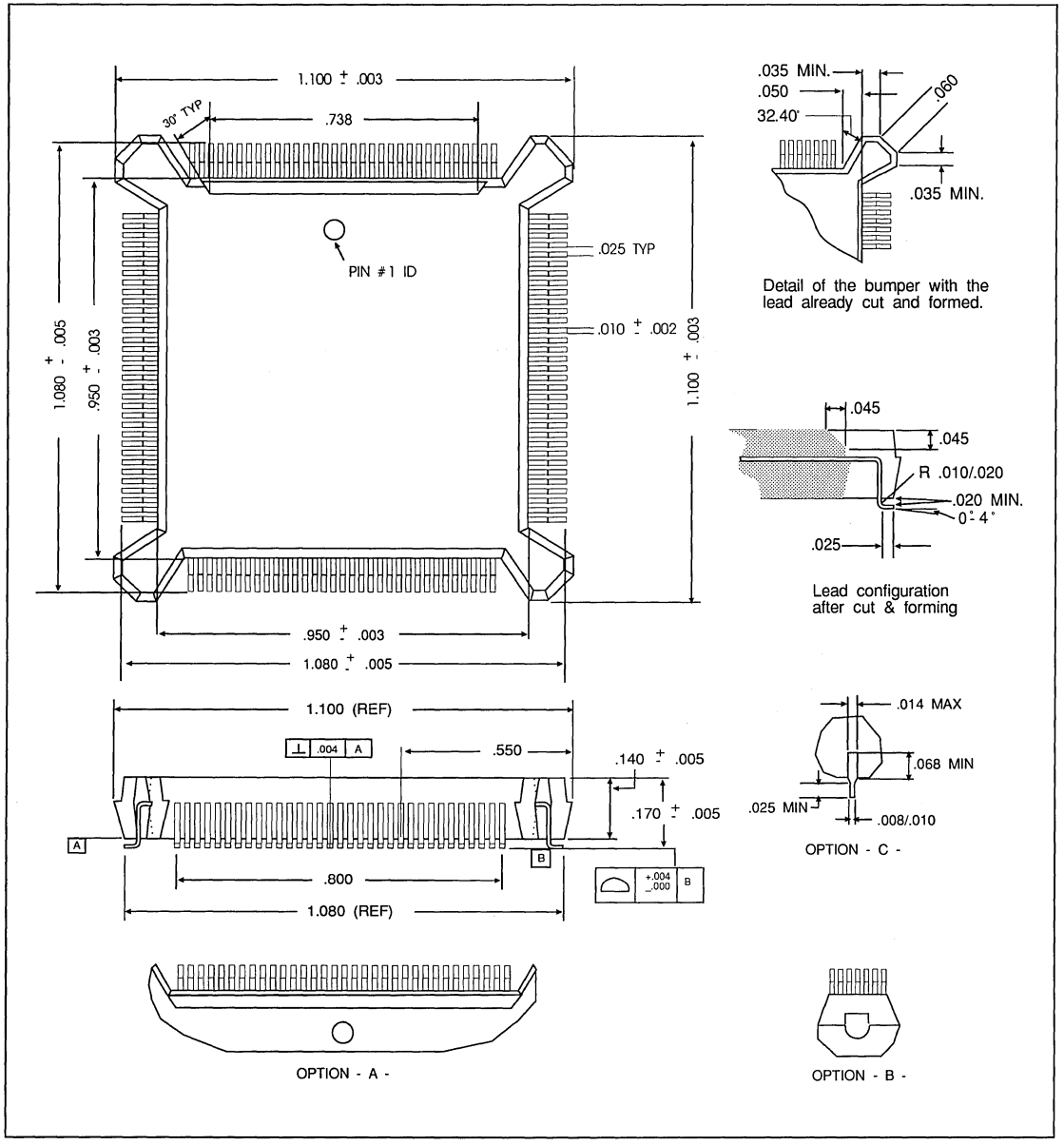


FIGURE 12-1. 132-PIN PQFP PACKAGE

APPENDIX

A.0 DC ELECTRICAL SPECIFICATIONS

This section provides the DC Operating Characteristics for the WD76C10ALV. The parameters that differ from the WD76C10A/LP are marked with an * .

A.1 MAXIMUM RATINGS

Supply Voltage (Vcc) with respect to Vss (ground) . . . . . Vcc - Vss ≤ 7.0 Volts

Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to Vdd +0.3 Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)

Power Dissipation . . . . . 300 mW *

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

A.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
Vcc = +3.3V ±.0.3V for WD76C10ALV *

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tristate And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High *	VCC -0.8		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current *		120 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz

TABLE A-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-27	-40	µA	Not suspend and resume mode

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

M/IO, PEACK, NPERR, NPBUSY, S0, S1, NPRST, CPURES, DPH, DPL

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-27	-90	µA	Not processor down or suspend mode

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

PMCIN, IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, BHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-27	-90	µA	Not suspend mode

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

CASL3, CASL2, CASH3, SDT/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current *	-27	-90	µA	RESET IN = 0

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

FOR PINS WITH INTERNAL PULLDOWNS:

A23-A0, D15-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current *	-27	-90	µA	Processor power down or suspend mode

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage *	Vcc -0.2		V	IOUT = -100 µA
VOH	Output High Voltage *	2.4		V	IOUT = -1 mA
VOL	Output Low Voltage *		.4	V	IOUT = 1.5 mA

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage *	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage *		.4	V	IOUT = 3 mA

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

IOR, IOW, MEMR, MEMW, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage *		.5	V	IOUT = 12 mA

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:

REFRESH

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage *		.4	V	IOUT = 12 mA

TABLE A-1. DC OPERATING CHARACTERISTICS cont.

A.3 AC OPERATING CHARACTERISTICS

This section provides the WD76C10ALV AC Operating Characteristics for the 80386SX Page Mode and 80386SX CPU Mode. The parameters that differ from the WD76C10A/LP are marked with an * .

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
CPURES	50 pF	NPRST	50 pF	$\overline{BHE}$	50 pF
W/$\overline{R}$	50 pF	ALE	50 pF	$\overline{DEN1}$, $\overline{DEN0}$	50 pF
$\overline{SDEN}$	50 pF	DT/$\overline{R}$	50 pF	SDT/$\overline{R}$	50 pF
MXCTL2 - 0	50 pF	DACKEN	50 pF	$\overline{CSEN}$	50 pF
$\overline{LOMEG}$	50 pF	SPKR	50 pF	$\overline{READY}$	50 pF
$\overline{HOLD}$	50 pF	INTRQ	50 pF	NMI	50 pF
$\overline{BUSYCPU}$	50 pF	EPEREQ	50 pF	A23 - A0	60 pF
CPUCLK	70 pF	SYSCLK	75 pF	$\overline{CASH3}$ - $\overline{0}$ *	50 pF
$\overline{CASL3}$ - $\overline{0}$	75 pF	D15 - D0	100 pF	DPH	100 pF
DPL	100 pF	$\overline{RAS3}$ - $\overline{RAS0}$	150 pF	$\overline{IOW}$	200 pF
$\overline{IOR}$	200 pF	$\overline{MEMW}$	200 pF	$\overline{MEMR}$	200 pF
LA20	200 pF	SA0	200 pF	AEN	200 pF
BALE	200 pF	$\overline{REFRESH}$	200 pF	RA10 - RA0 *	220 pF

TABLE A-2. SIGNAL LOADING

A.4 80386SX PAGE MODE TIMING

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T200	Processor ADDRESS to RAM address valid, Page Hit		34	27
T201	CPUCLK rise to CAS fall, 2.5 CLK CAS		31	25
T202	CPUCLK fall to CAS rise		24	21
T203	CPUCLK fall to CAS fall, 2.0 CLK CAS		27	22
T204	Processor data to parity valid		25	20
T205	CPUCLK rise to RAM address valid, Page Miss		48	43
T206	CPUCLK rise to WNRDRAM rise		31	28
T207	CPUCLK fall to RAS fall, first access		27	21
T208	CPUCLK rise to COLUMN address valid		49	33
T209	CPUCLK rise to WNRDRAM fall		31	28
T212	CPUCLK rise to RAS rise, Page Miss		27	24
T213	CPUCLK fall to RAS fall, Page Miss		27	24
T214	CPUCLK rise to READY fall *		25	25
T215	CPUCLK rise to READY rise *		25	25

TABLE A-3. 80386SX - PAGE MODE MEMORY TIMING

SYMBOL	CHARACTERISTIC	20 MHz		25 MHz		UNITS
		MIN	MAX	MIN	MAX	
T140	See Table 11-9					
T141	See Table 11-9					
T204	See Table 11-6					
T214	See Table 11-6					
T215	See Table 11-6					
T451	CPUCLK rise to CPURES rise delay		14		12	ns
T452	CPUCLK rise to CPURES fall delay		13		12	ns
T453	CPUCLK rise to NPRST rise delay		14		10	ns
T454	CPUCLK rise to NPRST fall delay		13		10	ns
T455	CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay		35		35	ns
T456	CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay		35		30	ns
T457	$\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay		30		30	ns
T458	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35		35	ns
T460	$\overline{\text{NPERR}}$ fall to EPEREQ rise delay		30		30	ns
T462	ADS# setup time to CPUCLK rise *	14		14		ns
T463	ADS# hold time from CPUCLK rise	5		4		ns
T464	W/R# setup time to CPUCLK rise *	14		12		ns
T465	W/R# hold time from CPUCLK rise	5		4		ns
T466	D/C# setup time to CPUCLK rise *	14		10		ns
T467	D/C# hold time from CPUCLK rise	5		4		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise *	17		19		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	5		4		ns
T470	$\overline{\text{BHE}}$ setup time to CPUCLK rise	17		15		ns
T471	$\overline{\text{BHE}}$ hold time from CPUCLK rise	3		4		ns

TABLE A-4. 80386SX CPU TIMING

SYMBOL	CHARACTERISTIC	20 MHz		25 MHz		UNITS
		MIN	MAX	MIN	MAX	
T472	HLDA setup time to CPUCLK rise *	10		10		ns
T473	HLDA hold time from CPUCLK rise	3		4		ns
T474	HOLD valid delay from CPUCLK rise *		26		26	ns
T475	DPH setup time to CPUCLK rise	5		5		ns
T476	DPH hold time from CPUCLK rise	19		19		ns
T477	D15-D0 setup time to CPUCLK rise	5		5		ns
T478	D15-D0 hold time from CPUCLK rise	19		19		ns
T479	A23-A1, BLE# setup time to CPUCLK rise *	42		42		ns
T480	A23-A1, BLE# hold time from CPUCLK rise	3		4		ns

TABLE A-4. 80386SX CPU TIMING cont.

WD76C20/LV

Floppy Disk Controller,

Real Time Clock, IDE Interface,

and Support Logic Device

WESTERN DIGITAL

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LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This data sheet applies to both the WD76C20, and WD76C20LV. The WD90C20LV is a low voltage version of the WD76C20 chip. For convenience all references to these two devices will be referred to as the WD76C20.

See Appendix A for the specification differences of the WD76C20LV.

1.2 FEATURES

The WD76C20 includes these features:

- 84-pin PLCC and PQFP packages
- 5V supply requirement (WD76C20)
  3.3V supply requirement (WD76C20LV)
- 3.0V battery backup supply for the RTC and 114 byte SRAM (WD76C20)
  2.4V battery backup supply for the RTC and 114 byte SRAM (WD76C20LV)
- Implemented in a low-power, high-performance, 1.25 micron CMOS technology process
- Floppy Disk Controller (FDC) software transparent power-down mode with low standby ICC current. FDC features:
  - 256 tracks support
  - 100% software compatible with NEC 765A
  - Integrated high-performance DPLL data separator:
    - 125, 250, 300, 500 Kb/sec and 1 Mb/sec data rates
    - Option to select 150 Kb/sec FM and 300 Kb/sec MFM data rates only
  - Automatic Write Precompensation:
    - Defeat option
    - Inner track value of 125 or 187 ns pin selectable
  - On chip clock generation:
    - 2 TTL clock inputs, or
    - Single 16 or 32 MHz crystal circuit and one TTL clock input
  - Power Qualified Reset
    - Enable PQR in WD76C20
    - Disable PQR in WD76C20LV
  - Host interface read/write accesses compatible with 80286 microprocessors at speeds up to 12 MHz with 0 wait states
  - Direct floppy disk drive interface - no buffers needed
    - 48 mA sink output drivers
    - Schmitt Trigger input line receivers
  - FDC direct PC XT/AT interface compatibility
    - Floppy Control and Operations Registers on chip
    - In PC/AT mode, provides required signal qualification to DMA channel
    - IBM BIOS compatible
    - Dual-speed spindle drive support
  - PS/2 type drive support
- Real Time Clock (RTC) features:
  - Software compatible with Motorola MC146818A.
  - Internal time base and oscillator circuitry
  - Counts seconds, minutes, and hours
  - Counts days of the week, date, month, and year
  - Time base input for 32.768 KHz square wave
  - Time base oscillator for parallel resonant crystals
  - Binary or BCD representation of time, calendar, and alarm

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- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight savings time option
- Automatic leap year compensation
- Interfaced with software as 128 RAM locations
- 114 bytes of general purpose RAM
- Status bit indicates data integrity
- Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software maskable and testable:
  - Time-of-day alarm - once-per-second to once-per-day
  - Periodic interrupt rates from 122 us to 500 ms
  - End-of-clock update cycle

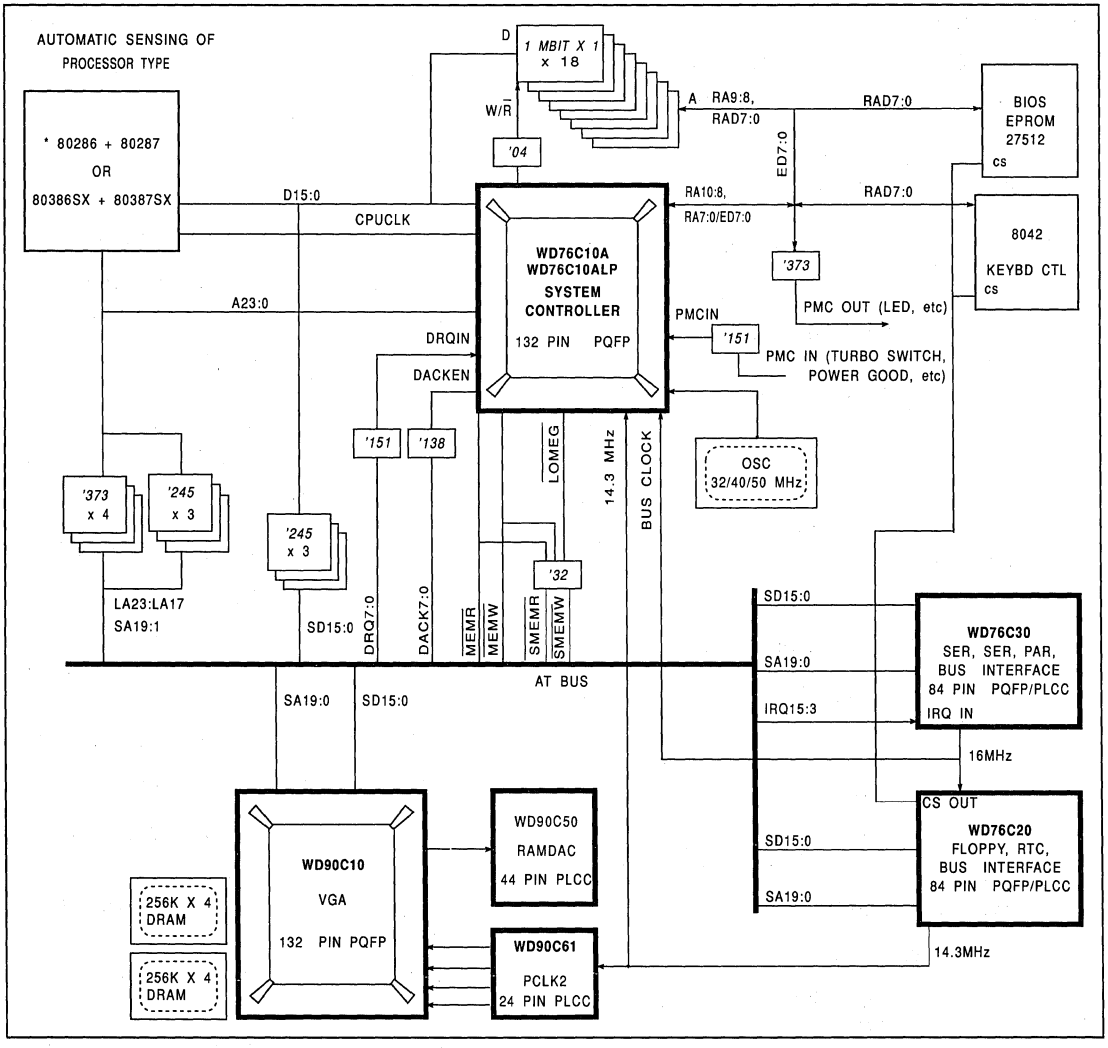

FIGURE 1-1. SYSTEM LEVEL FUNCTIONAL BLOCK DIAGRAM

1.3 GENERAL DESCRIPTION

The WD76C20 is a member of the WD7600 chip set which provides a cost-effective, power-efficient solution to PC systems design, especially those relating to "lap-top" devices. The set includes the WD76C10, the WD76C20, and the WD76C30 as shown in Figure 1-1. Together these chips provide all necessary logic to build a fully integrated system board for several varieties of IBM PC/AT compatibles including systems using 80286, 80386SX, and 80C286 processors.

As part of this chip set, the WD76C20 provides these integral functions:

- Bus Interface Logic
- IDE Interface
- Chip Select Logic
- Floppy Disk Controller
- Real Time Clock
- Suspend/Resume Logic

The Floppy Disk Controller (FDC) component provides necessary timing and signalling between the host processor peripheral bus and a floppy disk drive through a cable connector.

The Real Time Clock component provides calendar and clock information for the system.

The IDE Interface controls buffering between the system's AT Bus and PC/AT compatible IDE drive interface.

The Bus Interface Logic controls buffering of data between the system's AT Bus and the WD76C20.

The Chip Select Logic section provides decoding for selected chip functions both within the WD76C20 and on the PC/AT motherboard.

Suspend/Resume Logic provides support for chip set power-down and resume sequences.

The remainder of this manual contains the following information:

Section 2 discusses the basic system architecture.

Section 3 provides signal descriptions.

Section 4 discusses the Chip Select Logic in more detail.

Section 5 discusses the Floppy Disk Controller in more detail.

Section 6 provides additional information on the IDE Interface.

Section 7 provides information on the Real Time Clock and SRAM.

Section 8 gives more information on the Suspend/Resume Logic.

Section 9 provides DC Operating Characteristics.

Section 10 provides AC Interface Timing.

Section 11 shows two package diagrams.

Appendix A lists the specifications for the WD76C20LV device.

2.0 ARCHITECTURE

The WD76C20 has three principal functions as illustrated in Figure 2-1. First, it exchanges control signals with the WD76C10 System Controller. Second, under control of the WD76C10, it exchanges data and qualified operation/status information with the Host via the system's AT Bus. Third, it provides complete control and data read/write services for one to four floppy disk units.

Internally, the WD76C20 has the following functional components:

- Bus Interface Logic
- Chip Select Logic
- IDE Drive Interface
- Floppy Disk Controller
- Real Time Clock and associated SRAM
- Suspend/Resume Logic

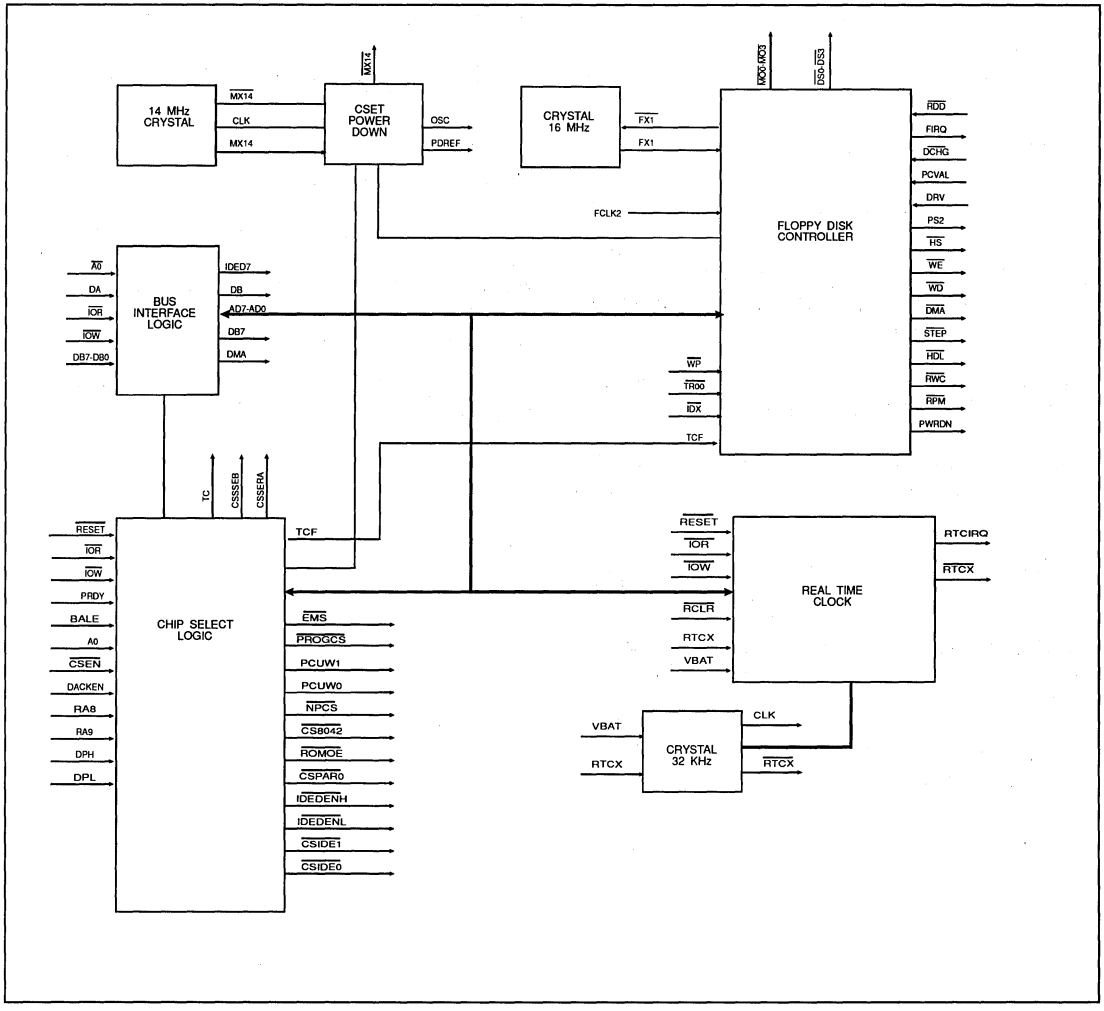

FIGURE 2-1. WD76C20 FUNCTIONAL BLOCK DIAGRAM

These functional components are described briefly in the following sections.

For a more detailed description of Chip Select Logic, IDE Interface Support, Floppy Disk Controller, Real Time Clock, and the Suspend/Resume Logic, refer to Sections 4 through 9. Signals mentioned in the following discussion are listed and described in Section 3.

2.1 BUS INTERFACE LOGIC

The chip's Bus Interface controls the buffering of bits D0-D7 passing between the system's AT Bus and any WD76C20 internal source/destination 8-bit storage cell via the internal bus. The Bus Interface receives the $\overline{IOR}$ and $\overline{IOW}$ signals from the WD76C10, and with the appropriate chip selects from the Chip Select Logic (CSL), it parallel-passes D0-D7 from the AT Bus to an internal WD76C20 cell, or vice versa. The internal cells which the Bus Interface Logic reads/writes to are:

- The Control, Master Status, Status, Data, or Operation Registers in the Floppy Disk Controller
- The 128 registers in the SRAM affiliated with the Real Time Clock.

The Bus Interface Logic also provides a controlled bidirectional path for bit D7 between the AT Bus and the IDE Drive Port.

2.2 CHIP SELECT LOGIC

The Chip Select Logic (CSL) component of the WD76C20 provides the decoding needed both for selecting chip functions within the WD76C20 and on the PC/AT motherboard. It receives the DPL, DPH, and RA8-RA10 signals from the WD76C10 Systems Controller and outputs appropriately decoded chip select signals (detailed in Section 3). Overall control of the decoding processes is accomplished using the $\overline{CSEN}$ and DACKEN signals from the WD76C10. $\overline{CSEN}$ enables the decoded output, while DACKEN causes the CSL to ignore the inputs from the WD76C10.

2.3 FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) portion of the WD76C20 is a VLSI Super Cell that provides all functions required between the host processor peripheral bus and the cable connector to the floppy disk drive. This provides a comprehensive solution to floppy subsystem control. Among its many features, the FDC possesses a software-transparent power-down mode which facilitates the chip's use in lap-top and portable systems. For more information on this component, refer to Section 5.

2.4 REAL TIME CLOCK AND SRAM

The Real Time Clock (RTC) component of the 76C20, in conjunction with the 128-byte register file, provides both calendar (day-of-week, day-of-month, month, and year) and clock (hours, minutes, and seconds) information, along with clocked alarms and a periodic interrupt. This interface gets signals from the 76C20 Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the 76C20 internal bus and the RTC internal bus accessing the SRAM.

2.5 SUSPEND/RESUME LOGIC

This functional block is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10. This can switch to a 32.768 KHz clock during the low-power Suspend mode. This logic supports the WD7600 power-down and resume sequencing required to run the Floppy Disk Controller and other components during low power.

3.0 SIGNAL DESCRIPTION

Figure 3-1 illustrates the signal names and pin locations on the 84-pin PLCC/PQFP WD76C20 package. Table 3-1 lists the signal names by pin number and Table 3-2 lists the signal names alphabetically. Table 3-3 lists the signal names and descriptions grouped by function.

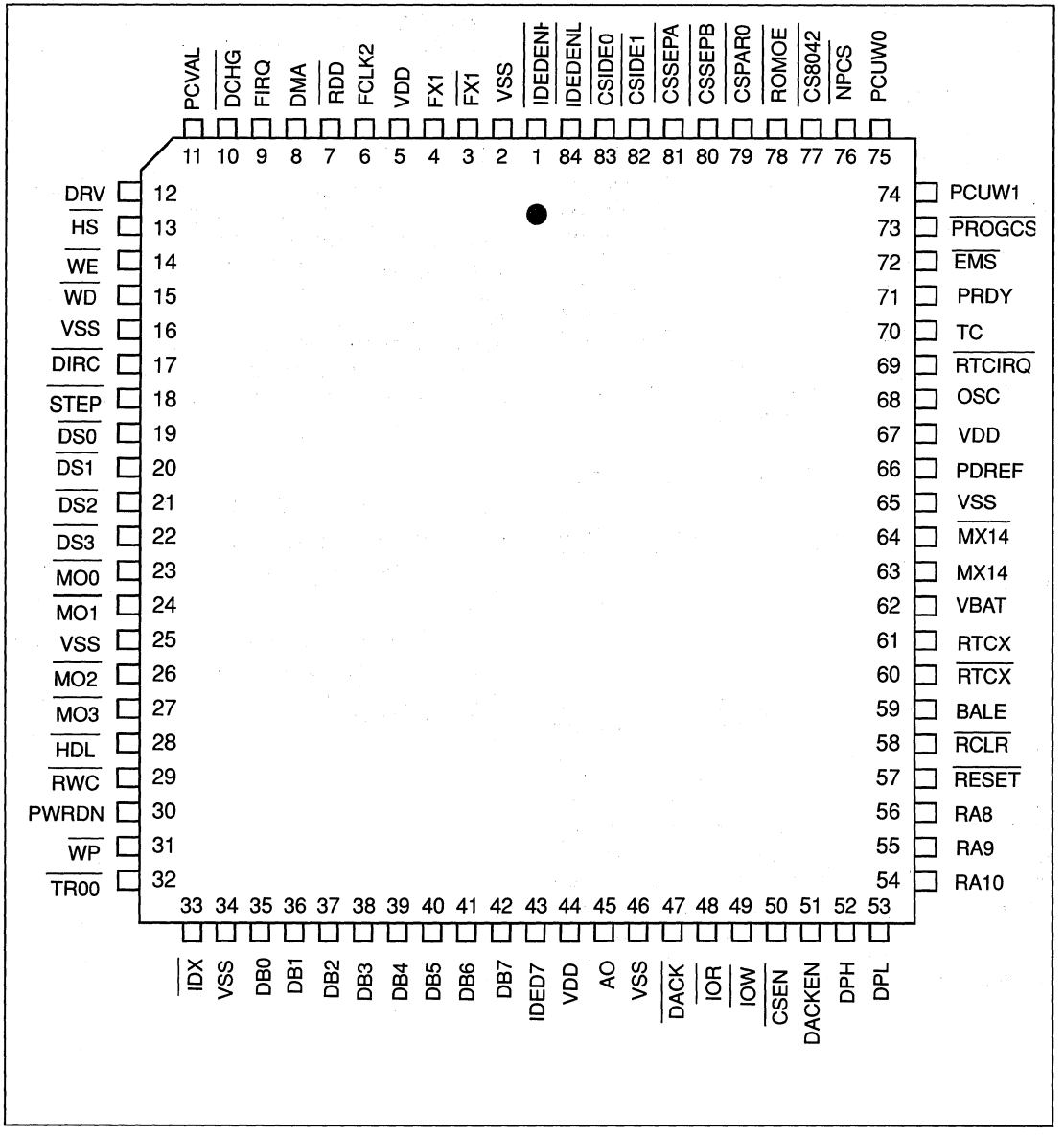

FIGURE 3-1. WD76C20 PIN DIAGRAM

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	45	DS1	20	MO2	26	ROMOE	78
BALE	59	DS2	21	MO3	27	RPM/RWC	29
CSEN	50	DS3	22	MX14	63	RTCIRQ	69
CSIDE0	83	EMS	72	MX14	64	RTCX	60
CSIDE1	82	FIRQ	9	NPCS	76	RTCX	61
CSPAR0	79	FCLK1/FX1	4	OSC	68	RWC/RPM	29
CSSERB	80	FCLK2	6	PCUW1	74	STEP	18
CSSERA	81	FX1	3	PCUW0	75	TC	70
CS8042	77	FX1/FCLK1	4	PCVAL	11	TR00	32
DACK	47	HDL	28	PDREF	66	VBAT	62
DACKEN	51	HS	13	PRDY	71	VDD	5,44,67
DB0-DB7	35-42	IDEDENH	1	PROGCS	73	VSS	2,16,25,34,46,65
DCHG	10	IDEDENL	84	PWRDN	30	WD	15
DIRC	17	IDED7	43	RA8	56	WE	14
DMA	8	IDX	33	RA9	55	WP	31
DPH	52	IOR	48	RA10	54		
DPL	53	IOW	49	RCLR	58		
DRV/PS2	12	MO0	23	RDD	7		
DS0	19	MO1	24	RESET	57		

TABLE 3-1. PIN ASSIGNMENTS (ALPHABETICAL ORDER)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IDEDENH	22	DS3	43	IDED7	64	MX14
2	VSS	23	MO0	44	VDD	65	VSS
3	FX1	24	MO1	45	A0	66	PDREF
4	FX1	25	VSS	46	VSS	67	VDD
5	VDD	26	MO2	47	DACK	68	OSC
6	FCLK2	27	MO3	48	IOR	69	RTCIRQ
7	RDD	28	HDL	49	IOW	70	TC
8	DMA	29	RWC	50	CSEN	71	PRDY
9	FIRQ	30	PWRDN	51	DACKEN	72	EMS
10	DCHG	31	WP	52	DPH	73	PROGCS
11	PCVAL	32	TR00	53	DPL	74	PCUW1
12	DRV/PS2	33	IDX	54	RA10	75	PCUW0
13	HS	34	VSS	55	RA9	76	NPCS
14	WE	35	DB0	56	RA8	77	CS8042
15	WD	36	DB1	57	RESET	78	ROMOE
16	VSS	37	DB2	58	RCLR	79	CSPAR0
17	DIRC	38	DB3	59	BALE	80	CSSEPB
18	STEP	39	DB4	60	RTCX	81	CSSEPA
19	DS0	40	DB5	61	RTCX	82	CSIDE1
20	DS1	41	DB6	62	VBAT	83	CSIDE0
21	DS2	42	DB7	63	MX14	84	IDEDENL

TABLE 3-2. PIN ASSIGNMENTS (NUMERICAL ORDER)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		INTEGRATED DRIVE ELECTRONICS (IDE)		
1	$\overline{\text{IDEDENH}}$	IDE High Byte Drive Enable	O	CMOS level output goes active low to enable the IDE Drive Interface Bus transceivers for the high byte of of the 16-bit interface. The signal is used with the CSIDEO card select output signal to the IDE drive only during 16-bit IDE data transfers.
43	IDED7	IDE Data Bit 7	I/O	TTL level I/O providing a data path for bit 7 between the Host and the IDE drive interface. IDED7 is an output, passing data to the IDE drive from DB7 of the Host data bus whenever an IOW to the IDE drive interface is detected. IDED7 is an input, passing data from the IDE drive to DB7 of the Host data bus whenever an IOR of the IDE drive interface is detected, except when reading from address 3F7H. During an IOR of 3F7H, the floppy DCHG status is output on the Host data bus pin DB7.
82	$\overline{\text{CSIDE1}}$	IDE Card Selected Aux. Registers	O	CMOS level output is used by the Host to address and communicate with the IDE drive auxiliary registers. Host activates the signal through a decode in the CSL logic block, while at the same time asserting IDEDENL.
83	$\overline{\text{CSIDE0}}$	IDE Card Selected Registers 0-7	O	CMOS level output is used by the Host to address and communicate with the IDE drive on the I/O channel. The Host activates the signal through a decode in the CSL logic block, while at the same time asserting IDEDENL or both IDEDENL and IDEDENH.
84	$\overline{\text{IDEDENL}}$	IDE Low Byte Drive Enable	O	CMOS level output goes active low to enable the IDE drive interface bus transceivers for the low byte of the 16-bit Interface. The signal is used with the CSIDE0 card select output signal to the IDE drive only during 16-bit IDE data transfers.
		HOST INTERFACE		
8	DMA	FDC DMA Request	O	DMA request for byte transfers of data. In PC/AT mode, this pin is tri-stated, enabled by DMAEN signal from the Operations Register.
45	AO	BIL Address Line	I	Address line selecting data (= 1) or status (= 0) information for the FDC. A0 = 0 during IOW is illegal except when putting the FDC into sleep mode.
47	$\overline{\text{DACK}}$	FDC DMA Acknowledge	I	Used by DMA controller to transfer data from FDC onto the bus. Logical equivalent to FDCS and A0=1. In PCAT mode, this signal is qualified by DMAEN from the Operations Register.

TABLE 3-3. SIGNAL DESCRIPTIONS

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		HOST INTERFACE (cont.)		
48	$\overline{IOR}$	BIL Input/Output Read	I	Read enable allowing data or status information to be transferred onto data bus by the WD76C20.
49	$\overline{IOW}$	BIL Input/Output Write	I	Write enable latching data from the bus into sub-system buffer registers.
57	$\overline{RESET}$	Chip Reset	I	TTL input resets the WD76C20 with the exception of the normal timekeeping operations which will remain uninterrupted. Resets all device outputs. Resets FDC controller, placing microsequencer in idle PC/AT mode.
		FLOPPY DISK CONTROL		
3	$\overline{FX1}$	FDC XTAL Output #1	O	This pin is an oscillator drive output for a 16 MHz resonant crystal. FX1 should be left floating if a TTL level clock is used at pin FX1.
4	FX1	FDC XTAL Input #1	I	XTAL oscillator input requiring a 16 MHz resonant crystal. This oscillator is used for all standard data rates, and may be driven with a 16 MHz TTL level signal instead of using the 16 MHz crystal.
	FCLK1	FDC CLK Input #1	I	
6	FCLK2	FDC CLK Input #2	I	TTL level input used for non-standard data rates; can be driven with a 9.6 MHz clock for 300 Kb/s MFM data rate and only be selected from the control register.
7	$\overline{RDD}$	FDC Read Disk	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
9	FIRQ	FDC Interrupt Request	O	Interrupt request indicating completion of command execution or data transfer requests (non-DMA mode). In PCAT mode, this pin is tri-stated, enabled by DMAEN signal from the Operations Register.
10	$\overline{DCHG}$	FDC Disk Changed	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low and drive door is open or that the diskette has possibly changed since last drive selection. The pin has an internal pull-up register.
11	PCVAL	FDC Precompensation Value Select	I	This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125 ns, 0 = 187 ns. In the defeat option, the PCVAL input is a don't care, and internally the pre-comp value is disabled.

TABLE 3-3. SIGNAL DESCRIPTIONS (CONTINUED)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		FLOPPY DISK CONTROL (cont.)		
12	DRV PS2	FDC Drive Type FDC PS2 Drive Type	I O	In the input mode, a logic 0 indicates to the FDC that a 2-speed spindle motor is present and that FCLK2 should be grounded because it will not be used. As an option, this pin can be defined as an output to support the floppy drive connector pin 2 for PS/2 style drives, indicating the FDC is set internally for a single spindle motor. The pin has an internal pull-up resistor.
13	$\overline{HS}$	FDC Head Select	O	This high current driver (HCD) output selects the head, i.e., side, of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
14	$\overline{WE}$	FDC Write Enable	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
15	$\overline{WD}$	FDC Write Data	O	This HCD is the write data output. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
17	$\overline{DIRC}$	FDC Stepper Direction	O	This HCD output determines the direction of head stepper motor. Logic 1 = outward motion, logic 0 = inward motion.
18	$\overline{STEP}$	FDC Stepper Step	O	This HCD output issues an active low pulse for each track to track movement of the head.
28	$\overline{HDL}$	FDC Head Load	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
29	$\overline{RWC}$ $\overline{RPM}$	FDC Reduce Write Current Revolutions Per Minute	O O	This HCD output, when active low, causes a reduced write current when bit density is increased toward the inner tracks, becoming active when tracks > 2. In PCAT mode, this signal can be used on 2-speed drives to select 300 RPM, active low, when 250 MFM or 125 FM KBs is selected and DRV = 0.
30	PWRDN	FDC Power Down	O	CMOS output, when active high, indicates the FDC portion of the WD76C20 has gone into power down mode. This signal can be used to power-down the floppy drive if supported.
31	$\overline{WP}$	FDC Write Protected	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low when a diskette is write-protected.

TABLE 3-3.SIGNAL DESCRIPTIONS (CONTINUED)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		FLOPPY DISK CONTROL (cont.)		
32	$\overline{TR00}$	FDC Track Zero	I	This ST input senses status from the drive indicating active low, when the head is positioned over the outermost track, track 00.
33	$\overline{IDX}$	FDC Index Hole	I	This ST input senses status from the drive indicating active low when the head is positioned over the beginning of a track, marked by an index hole.
		CHIP SELECT		
50	$\overline{CSEN}$	CSL Chip Select Enable	I	Chip Select Enable TTL input used to output enable the appropriate CSL control line as decoded from the RA8, RA9, RA10, DPL and DPH inputs. When DACKEN is asserted low, the function of $\overline{CSEN}$ is negated. When used to enable and disable the WD76C30 48 MHz clock, $\overline{CSEN}$ acts as a strobe to a latch. When it and DACKEN are both asserted, the TC output will go high.
51	DACKEN	CSL Dack Enabled	I	TTL input that indicates the host is performing a DMA transfer unrelated to the WD76C20. When active high, it is used to disqualify all CSL input lines.
52	DPH	CSL Address Parity High	I	Decoded chip select TTL input pad, bit CS4.
53	DPL	CSL Address Parity Low	I	Decoded chip select TLL input pad, bit CS3.
54	RA10	CSL Address Line 10	I	Decoded chip select TTL input pad, bit CS2.
55	RA9	CSL Address Line 9	I	Decoded chip select TTL input pad, bit CS1.
56	RA8	CSL Address Line 8	I	Decoded chip select TTL input pad, bit CS0.
58	BALE	CSL Bus ALE	I	TTL input which, when active high, causes latches on the CSL Input Code ($\overline{CSEN}$, DPH, DPL, RA10, RA9, RA8) to become transparent. When BALE is forced low, the data in the transparent latches is latched. This pin has an internal pull-up resistor so the pin can be left unconnected and the latches transparent.
70	TC	CSL Host Terminal Count	O	CMOS level output used to indicate the final count has been reached during a host DMA transfer unrelated to the WD76C20. It is also used internally by the FDC to indicate a DMA transfer to the floppy drive is complete. TC asserts high when both DACKEN and $\overline{CSEN}$ are asserted. (DACKEN=1, $\overline{CSEN}$=0).

TABLE 3-3. SIGNAL DESCRIPTIONS (CONTINUED)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		CHIP SELECT (cont.)		
71	PRDY	CSL Processor Ready	I	ST input senses processor ready status to help latch the CSL inputs correctly during system byte swapping activities. This pin has an internal pull-up resistor so that it can be left unconnected when not needed. The PRDY input should be used in system designs that use the BALE pin.
72	$\overline{\text{EMS}}$	CSL External EMS Access	O	CMOS card select output decoded from CSL input lines and issued to select external EMS.
73	$\overline{\text{PROGCS}}$	CSL Program Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a programmable chip select.
74	PCUW1	CSL Power Control Unit Write Strobe #1	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #1.
75	PCUW0	CSL Power Control Unit Write Strobe #0	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #0.
76	$\overline{\text{NPCS}}$	CSL Numerical Processor Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the numerical processor, the 80287.
77	$\overline{\text{CS8042}}$	CSL 8042 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the 8042.
78	$\overline{\text{ROMOE}}$	CSL ROM Output Enable	O	CMOS chip select output decoded from CSL input lines and issued to output enable the BIOS ROM.
79	$\overline{\text{CSPAR0}}$	CSL Parallel Port #0 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the parallel port #0.
80	$\overline{\text{CSSSEB}}$	CSL Serial Port B Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port B.
81	$\overline{\text{CSSERA}}$	CSL Serial Port A Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port A.
		REAL TIME CLOCK		
58	$\overline{\text{RCLR}}$	RTC RAM Clear	I	A dual function pin. As long as it is held low, all 76C20 outputs are held in a high impedance state to facilitate testing. It is also used as a ST input to clear all 114 bytes of the general purpose RAM. None of the clock or calendar functions are interrupted, and the 14 registers that are used by the RTC are left unchanged. This pin has an internal pull-up so it can be left unconnected.

TABLE 3-3. SIGNAL DESCRIPTIONS (CONTINUED)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		REAL TIME CLOCK (cont.)		
60	$\overline{\text{RTCX}}$	RTC Time Base XTAL Out	O	XTAL oscillator output for parallel resonant AT cut crystal at 32.768 KHz.
61	RTCX	RTC Time Base XTAL In	I	32.768 KHz XTAL oscillator input for use with crystal oscillator circuit.
62	VBAT	RTC Battery Backup	NA	Battery backup power supply VDD pin. A 3-volt battery connector can be attached to maintain the RTC timekeeping functions and SRAM integrity during system power-downs. (See Figure 2-3a)
69	$\overline{\text{RTCIRQ}}$	RTC Interrupt Request	O	Open-drain CMOS output that is set to tri-state unless the RTC needs to interrupt the processor, when the pin goes low and stays low until register C is read, or the part is reset through the RESET pin.
		SUSPEND/RESUME SUPPORT		
63	MX14	S/R 14.318 MHz Crystal In	I	Crystal oscillator input for the 14.318 MHz oscillator.
64	$\overline{\text{MX14}}$	S/R 14.318 MHz Crystal Out	O	Crystal oscillator output for the 14.318 MHz oscillator.
66	PDREF	Suspend/Resume DRAM Refresh	O	External DRAM refresh line used to support the WD76C10 when it goes into Suspend/Resume mode. During Suspend/Resume mode, this pad provides a 1.0 µS ± 0.5 µS pulse once every 15.26 µS a (using a 50% duty cycle) and is used to maintain the DRAM integrity with as little power as possible. The Suspend/Resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
68	OSC	S/R WD76C10 Clock Driver	O	CMOS level clock driver output used to support the WD76C10. When not in the WD76C10's suspend/resume mode, the output waveform is a 14.318 MHz square wave, and when in suspend/resume mode, it becomes a 32.768 KHz square wave. The WD76C10 suspend/resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
		DATA BUS		
35-42	DB(0-7)	BIL Processor Data/Address Bus	I/O	8-bit bi-directional, tri-stateable data bus.

TABLE 3-3. SIGNAL DESCRIPTIONS (CONTINUED)

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MOTOR CONTROL		
23	$\overline{MO0}$	FDC Motor on #0	O	This HCD output, when active low, is motor on enable for disk drive #0, in PCAT mode.
24	$\overline{MO1}$	FDC Motor on #1	O	This HCD output, when active low, is motor on enable for disk drive #1, in PCAT mode.
26	$\overline{MO2}$	FDC Motor on #2	O	Reserved for 4 Mbyte support (density select).
27	$\overline{MO3}$	FDC Motor on #3	O	Reserved for 4 Mbyte support (density select).
		DRIVE SELECT		
19	$\overline{DS0}$	FDC Drive Select #0	O	This HCD output, when active low, is Drive #0 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN0 bit.
20	$\overline{DS1}$	FDC Drive Select #1	O	This HCD output when active low is Drive #1 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN1 bit.
21	$\overline{DS2}$	FDC Drive Select #2	O	This HCD output, when active low, is Drive #2 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN2 bit.
22	$\overline{DS3}$	FDC Drive Select #3	O	This HCD output, when active low, is Drive #3 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN3 bit.
		MISCELLANEOUS		
2, 16, 25, 34, 46, 65		VSS		Ground
5, 44, 67		VDD		+5V Power

TABLE 3-3. SIGNAL DESCRIPTIONS (CONTINUED)

4.0 CHIP SELECT LOGIC

The Chip Select Logic is handled cooperatively by all the chips in the chip set, with each chip contributing its part to the logic. The WD76C10 and WD76C20 are particularly interrelated. Many of the decoding operations begun by the WD76C10 are handed to the WD76C20 for completion, and vice versa. For this reason, it is necessary to read both this section and section 7 of the WD76C10 for the fullest possible understanding of this function.

The Chip Select Logic of the WD76C20 provides decoding of five CSL input lines, DPH, DPL, RA10-8, into 17 output lines.

Figure 4-1 provides a block diagram of the inputs and outputs associated with this component.

Before the decoder can function, it must be enabled by $\overline{\text{CSEN}}$ going active low and remains open until it is disabled by DACKEN going active high. Optionally, the chip select inputs ($\overline{\text{CSEN}}$, DPH, DPL, RA10, RA9, RA8) can be latched by dropping the BALE from 1 to 0. These latches are transparent when BALE is held high or left unconnected.

Once enabled, the Chip Select Logic provides decoding for the following signals, as shown in Table 4-1.

Table 4-2 lists the I/O addresses and chip selects generated for each fixed port. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

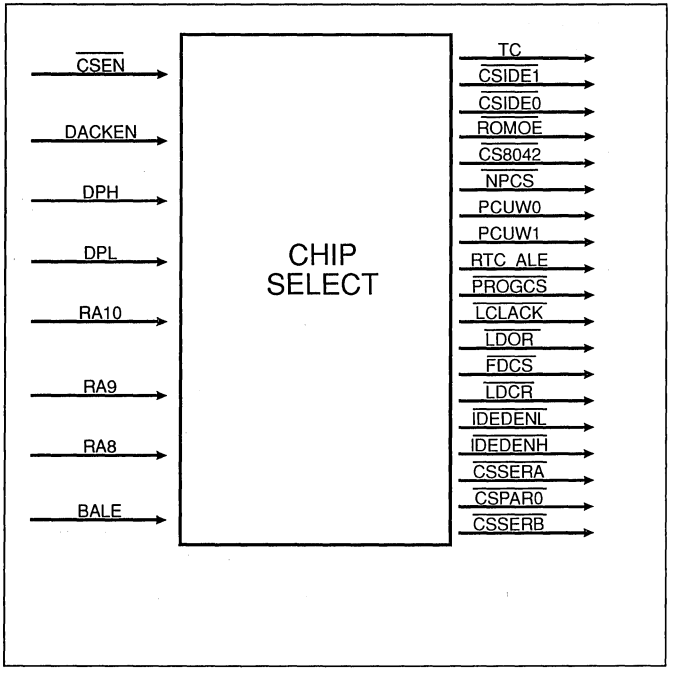

FIGURE 4-1. CHIP SELECT BLOCK DIAGRAM

CS#	CSL INPUT LINES DPH	DPL	RA10	RA9	RA8	FUNCTION
00H	0	0	0	0	0	Assert $\overline{\text{ROMOE}}$ to Output Enable the ROM BIOS[1]
01H	0	0	0	0	1	Assert $\overline{\text{CS8042}}$ to Chip Select the Keyboard Control[1]
02H	0	0	0	1	0	Assert $\overline{\text{NPCS}}$ to Chip Select the Numeric Processor[1]
03H	0	0	0	1	1	Assert PCUW0 to Write Strobe PCU #0
04H	0	0	1	0	0	Assert $\overline{\text{LCLACK}}$ to acknowledge Keyboard Processor[1]
05H	0	0	1	0	1	Assert RTC ALE for RTC I/O[1]
06H	0	0	1	1	0	Assert RTC Write Strobe Gated by $\overline{\text{CSEN}}$ & $\overline{\text{IOW}}$[1]
07H	0	0	1	1	1	Assert RTC Read Stobe Gated by $\overline{\text{CSEN}}$ & $\overline{\text{IOR}}$[1]
08H	0	1	0	0	0	Assert FDC $\overline{\text{LDOR}}$ Register Select Line[1]
09H	0	1	0	0	1	Assert FDC $\overline{\text{FDCS}}$ Chip Select Line[1]
0AH	0	1	0	1	0	Assert FDC $\overline{\text{LDCR}}$ Register (Read/Write) Select Line[1]
0BH	0	1	0	1	1	Assert FDC $\overline{\text{LDCR}}$ Register (Read/Write) Select Line & assert $\overline{\text{IDEDENL}}$ and $\overline{\text{CSIDE1}}$ IDE Card Select Lines[1]
0CH	0	1	1	0	0	Assert $\overline{\text{IDEDENL}}$ and $\overline{\text{CSIDE0}}$ IDE Card Select Line & assert $\overline{\text{IDEDENH}}$ if A0 = 0[1]
0DH	0	1	1	0	1	Assert $\overline{\text{IDEDENL}}$ and $\overline{\text{CSIDE}}$[1] IDE Card Select Line[1]
0EH	0	1	1	1	0	Assert $\overline{\text{CSSERA}}$ to Chip Select Serial Port A[1]
0FH	0	1	1	1	1	Assert $\overline{\text{CSPAR0}}$ to Chip Select Parallel Port 0[1]
10H	1	0	0	0	0	Assert $\overline{\text{CSSERB}}$ to Chip Select Serial Port B[1]
11H	1	0	0	0	1	Assert $\overline{\text{PROGCS}}$[1]
14H	1	0	1	0	0	Assert $\overline{\text{EMS}}$ to signify external EMS memory access[1]
15H	1	0	1	0	1	WD76C30 48 MHz Clk Disable , CSL Latches Code, OSSERA, $\overline{\text{CSSERB}}$ & $\overline{\text{CSPAR0}}$ stay asserted[2]
16H	1	0	1	1	0	48 MHz Clk Enable for WD76C30, CSL unlatches code, so $\overline{\text{CSSERA}}$, $\overline{\text{CSSERB}}$ & $\overline{\text{CSPAR0}}$ deassert[3]
17H	1	0	1	1	1	Assert PCUW1 to Write Strobe PCU #1

TABLE 4-1. CHIP SELECT LINE DECODER

[1] These signals are generated using latched CSL inputs if BALE is used.
[2] Suspend Mode is entered by asserting code 15H on the CSL inputs, while qualifying it by $\overline{\text{CSEN}}$=0, $\overline{\text{IOW}}$=0, and the falling edge of OSC.
[3] Suspend Mode is left by asserting code 16H on the CSL inputs, while qualifying it by an OSC falling edge.

PORT	I/O ADDRESS	CS#	FUNCTION
ROM Chip Select	N/A	00	Chip Select for BIOS ROM
Keyboard Control	060 - 06E Even	01	Chip Select For 8042
80287	00E0 - 00FF	02	Chip Select for Numeric Processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real Time Clock	070	05	RTC ALE
Real Time Clock	071	06	RTC Write Stroke
Real Time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary Address Secondary Address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary Address Secondary Address
Floppy Control Chip Select	3F7 377	0A	Primary Address Secondary Address (Floppy Enabled, HD Disabled)
Floppy And HD Control Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address
Hard Disk Chip Select	3F6, 3F7[1] 376, 377[1]	0D	Primary Address, IDE Mode Only Secondary Address, IDE Mode Only
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E[2]	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10[2]	
Program Chip Select	PROG	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS		14	External EMS
	F072	15	48 MHz Clock Disabled
	F472	16	48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Reserved		1E, 1F	Reserved

TABLE 4-2. I/O ADDRESS AND CHIP SELECT ASSIGNMENTS

[1] IDE Hard Disk enabled, floppy disabled
[2] CS# is the decoded value of CS4-CS0.

5.0 FLOPPY DISK CONTROLLER

This section discusses the Floppy Disk Controller in detail. The Floppy Disk Controller (FDC) consists of several logical and/or physical blocks, as illustrated in Figure 5-2.

These components are:

- The 765A-compatible Core
  - Clock & Timing Generator
- Drive Interface
  - Data Separator
  - Write Precompensator
- Host Interface
  - Control Register
  - Operations Register
  - Master Status Register
  - Disk Interface Control Register
  - Data Register

Each of these topics is discussed in the following sections.

5.1 765A-COMPATIBLE CORE

The WD76C20 maintains the core attributes of the 765A floppy disk controller. The micro-sequencer is functionally equivalent and all commands will execute identically, assuring software compatibility with the 765A standard. The floppy control state machine on the front-end is also functionally equivalent. The micro-sequencer and control state machine operate at 8 times the selected bit data rate in MFM and 16 times the bit data rate in FM.

5.1.1 Clock and Timing Generator

The FDC portion of the WD76C20 provides all clock generation necessary for the floppy disk subsystem including SCLK (Sampling Clock), WCLK (Write Clock) and MCLK (Master Clock).

A 16 MHz crystal oscillator circuit provides the necessary signals for internal timing when external clocks are unavailable. The 16 MHz signal handles all standard data rates (500 and 250 Kb/sec) used in PC/AT designs, and a non-standard data rate (300 Kb/sec.). If neither the board space nor the 16 MHz TTL clock is available, FCLK1/FX1 can be driven with a 16 MHz TTL-level clock, and FCLK2 with a 9.6 MHz TTL clock. This will handle standard data rates (500, 250, and 125 Kb/sec.), and a non-standard data rate (300 Kb/sec.).

5.1.1.1 SCLK

SCLK is the clock which drives the digital phase lock loop data separator during data recovery. This clock frequency is always 32 times the selected data rate, and is exactly the frequency of the signals on FX1 (FCLK1) and FCLK2, whether or not standard data rates are being used (see Table 5-1).

FCLK		SCLK	
FCLK1	**FCLK2**	**Standard**	**Non-Stan.**
16 MHz TTL	9.6 MHz TTL	16 MHz	9.6 MHz
16 MHz TTL	Tied Low	16 MHz	Disabled

TABLE 5-1. FDC SAMPLING (SCLK) CLOCK

If the oscillator is not used, a 16 MHz TTL clock should be applied at FCLK1 (FX1) as shown in Figure 5-1. Data rates for this crystal are shown in Table 5-2.

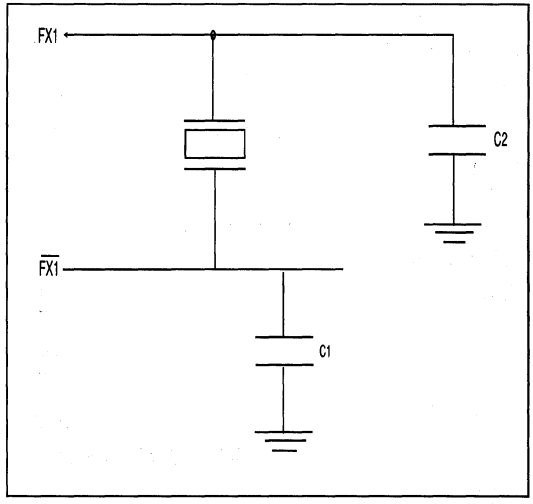

FIGURE 5-1. 16 MHZ CRYSTAL

DATA RATE	CODE	SCLK	MCLK	WCLK
125 Kb/sec	FM	4 MHz	2 MHz	250 KHz
500 Kb/sec	MFM	16 MHz	4 MHz	1 MHz
250 Kb/sec	FM	8 MHz	4 MHz	500 KHz
250 Kb/sec	MFM	8 MHz	2 MHz	500 KHz
300 Kb/sec	MFM	9.6 MHz	2.4 MHz	600 KHz

TABLE 5-2. FDC MCLK & WCLK GENERATION

5.1.1.2 WCLK

WCLK is used by the encoder logic to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency twice the selected data rate. See Table 5-2 for WCLK data rates.

5.1.1.3 MCLK

MCLK is used by the micro-sequencer. Both the MCLK and $\overline{\text{MCLK}}$ clocks latch in a 2-phase scheme. One micro-instruction cycle is 4 MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate. See Table 5-2 for MCLK data rates.

5.1.1.4 Automatic Power-Down Mode

In this mode, the FDC powers down all circuitry except for the Data Register, the Operations Register, the Control Register, the Master Status Register and the I/O path leading to and from the data bus. Since the crystal oscillator controller circuitry and all non-essential linear circuitry is turned off, the controller will draw very low current. The FDC can return from power-down mode by simply polling the Master Status Register, after which the crystal oscillator turns on along with the other circuitry.

To resume on power-up, the FDC turns on the crystal oscillator, which in turn activates all the clock circuitry on the chip.

For more information on the Power-Down Modes, refer to Section 7.

5.2 DRIVE INTERFACE

The FDC's disk drive interface includes data separation and write precompensation in addition to the usual formatting, encoding/decoding, stepper motor control and status sensing functions. All inputs are TTL compatible, and outputs are high-current, open-drain drivers that conform to the ANSI specification of 48 mA.

The FDC no longer supports certain pin functions provided for in the 765 predecessor. The output RW/SEEK is used in the 765-based subsystem as a multiplexer select line to allow a pin to have 2 functions depending on whether a read, write, or seek type command is under execution. This signal is no longer available externally but is used within the WD76C20 to assure that no improper pin functionality occurs.

The LCT function has been renamed $\overline{\text{RWC}}$ and resides on a pin of its own with slightly altered active conditions and in the PC/AT mode is $\overline{\text{RPM}}$. $\overline{\text{DIRC}}$ is the only function on that pin and is enabled only during seeks as a power conservation measure.

$\overline{\text{STEP}}$ is also only enabled during seeks and a fault rest (FR) is no longer needed since FLT, fault detects, are not sensed. FLT status - status register #3, bit 7 - will always be a logic 0 state. Also, track zero status, $\overline{\text{TR00}}$, is only sensed during seeks.

Two-sided drive status, TS, is no longer supported, and Status Register #3, bits 6 and 3 will both now reflect Write Protect status. The FDC device assumes the drive is ready all the time since DRDY signal is set to logic 1 internally. This will still result in an FIRQ. This action is acknowledged as a change in status and demands a Sense Interrupt Status command execution in order to clear the FIRQ. Signals MFM, RDW, WCK and VCO are no longer needed since all logic associated with these is now contained within the FDC.

5.2.1 Data Separator

The FDC incorporates the patented digital phase lock loop used in the WD92C32 product. The sample clock rate, SCLK, must be 32 times the data rate.

5.2.2 Write Precompensation

The FDC maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 16 MHz clock, if this is the frequency on pin FCLK1, and clocked through a shift register, FX1. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle which equals 1/4 of the bit cell period or 1/2 the WCLK period.

When PCVAL is set to 1, all data will be precompensated by ±125 ns regardless of track number and data rate, but only for MFM encoding (no write precomp for FM). If PCVAL is 0, and if a track inside number 28 is accessed, then ±187 ns of precomp will be generated. For frequencies other than 16 MHz on FX1, these precomp values will be 2 and 3 SCLK clock cycles respectively.

When a non-standard data rate using FCLK2 is chosen, the precompensation logic is run from this frequency. In this case, the PCVAL function is disabled. Hence precomp values will always be 2 clock cycles. For 9.6 MHz this value is ±208 ns. The write precomp can be disabled by the use of bit 2 of Control register for PC AT. With no write precomp, the PCVAL input to the chip is ignored.

5.3 HOST INTERFACE

The host access signals are identical to a 765A floppy disk controller, but timings have been enhanced. The host interface has been designed to support up to 12 MHz bus speeds without the use of wait states. Input strobes are Schmitt Triggers. The data bus drive capability is 12 mA IOL, and 5 mA IOH, allowing, in most applications, direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC/AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor architecture; however, in the PC AT these functions are latched into registers addressed within the system's I/O mapping. These registers, Operations and Control, are incorporated into the FDC.

The FDC has 8 internal registers.

- Control Register is a write register that provides support logic for selection of desired data rates and write precompensation logic.
- Disk Interface Control Register provides a read only register for determining the Disk Change status signal.
- Operations Register provides all the control signals required to select the drive and the spindle motor.
- Master Status Register is an 8-bit read/write register comprised of these two parts:
  - MSR is an 8-bit read only register containing FDC status information and may be accessed at any time.
  - MSR1 is an 8-bit write only register containing support for the Power Down Mode and the PS/2 drive type select.
- Status Registers 0-3 are four read only registers under system control providing various status and error information.
- Data Register is an 8-bit read/write register which stores data, commands, parameters, and FDD status information.

Selection of these registers is handled through the decoding of 7 lines as shown in Table 5-3.

ADDRESS MAP	$\overline{CS}$	A0	$\overline{LDCR}$	$\overline{LDOR}$	R/W/RW
MASTER STATUS REGISTER	0	0	–	–	R
MASTER STATUS REGISTER1	0	0	–	–	W
DATA REGISTER	0	1	–	–	R/W
OPERATIONS REGISTER	–	–	–	0	W
CONTROL REGISTER	–	–	0	–	W
DISK INTERFACE REGISTER	–	–	0	–	R

TABLE 5-3. FDC REGISTER MAP

5.3.1 Control Register

The Control Register is a Write register.

Address 3F7, $\overline{LDCR}$ = 0, $\overline{IOW}$ = 0 - Write only

The Control Register is used to set the data transfer rate and disable write precomp. On receiving an $\overline{IOW}$, the WD76C20 latches the three LSB's of the data bus. These bits, along with CR1 and CR0 in the Control Register, are used as shown in Table 5-1 to select the desired data rate which, in turn, controls the internal clock generation. Clock switchover is internally corrected, allowing continuous operation after changing data rates. Switching this clock must be errorless or the device must be reset. For all non-standard transfer data rates, use Table 5-2.

As an option, FDC also supports a 150 Kb/sec FM data transfer rate. The Control Register is used to set the transfer data rate as shown in Table 5-2. FX1 (pin 4) can be driven with a TTL level 9.6 MHz signal. With this setup, only 150 Kb/sec (FM) and 300 Kb/sec (MFM) data transfer rates can be selected. If the Control Register is not used, the data rate is governed by the supplied clock, or crystal, frequency and must be 64 times the desired MFM data rate. This provides a maximum frequency of 16 MHz for the data rate of 250 Kb/sec.

In PC/AT mode, precomp can be disabled by the use of the No Write Precomp (NWP) bit in the Control Register as shown in Figure 5-3.

7	6	5	4	3	2	1	0
					NWP	CR1	CR0

Signal Name	Default At Reset
NWP	0
CR1	0
CR0	0

Bits 7-3 - Reserved, not defined.

Bit 2 - NWP, No Write Precomp
In PC/AT mode, precomp can be disabled. This enables the PCVAL input pin.

NWP = 0 -
Write Precomp enabled.

NWP = 1 -
Write Precomp disabled.

Bit 1 - CR1, Data Rate 1
CR1 = 0 -
Refer to Tables 5-4.

CR2 = 1 -
Refer to Tables 5-4.

Bit 0 - CR0, Data Rate 0

CR0 = 0 -
Refer to Table 5-4.

CR0 = 1 -
Refer to Tables 5-4.

DATA RATE	PC/AT RPM	MODE	CR1	CR0	DRV
16 MHZ					
500 Kb/sec	1	MFM	0	0	X
250 Kb/sec	1	FM	0	0	X
250 Kb/sec	0	MFM	0	1	0
300 Kb/sec	0	MFM (9.6 MHz)	0	1	1
250 Kb/sec	0	MFM (Reset Default)	1	0	X
125 Kb/sec	0	FM (Reset Default)	1	0	X
125 Kb/sec	0	FM	1	1	X
9.6 MHZ					
300 Kb/sec	1	MFM	0	0	X
150 Kb/sec	1	FM	0	0	X

TABLE 5-4. FCLK1 DATA RATE DECODER

5.3.2 Disk Interface Control Register

The Disk Interface Control Register is a Read only register. It shares the same address as the Control Register but is accessed to indicate the state of $\overline{DCHG}$. This signal helps decode Disk Interface Control logic by sensing status from the disk drive. It senses low if the drive door is open or the diskette has changed since the last drive selection.

Address 3F7, $\overline{LDCR}$ = 0 - Read only

During the Read Mode, bit 7 indicates the state of the Disk Change Status signal, $\overline{DCHG}$. Bits 6 through 0 are tri-stated and used by the hard disk during this read.

7	6	5	4	3	2	1	0
DCHG	Tristated						

Signal Name	Default At Reset
Bit 6-0	Tristated
Bit 7	0

Bit 7 - D_CHG, Disk Changed status signal

D_CHG = 0 -

$\overline{DCHG}$ has not changed state.

D_CHG = 1 -

$\overline{DCHG}$ has changed state.

Bits 6-0 - Tri-stated

5.3.3 Operations Register

Address 3F2, $\overline{LDOR}$ = 0, $\overline{IOW}$ = 0, PCAT Mode - Write only

When the Operations Register receives an $\overline{IOW}$, the data on the data bus is latched into the Operations Register. This register replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select desired drive.

7	6	5	4	3	2	1	0
MOEN				DMAEN	$\overline{SRST}$	DSEL	
3	2	1	0			1	0

Signal Name	Default At Reset
MOEN3-0	0
DMAEN	0
$\overline{SRST}$	1
DSEL1-0	0

Bits 7-4 - MOEN3-0, Motor On Enable 3-0

MOEN3 through MOEN0 produce the inverted outputs MO3, MO2, MO1, and MO0.

Bit 3 - DMAEN, DMA Enable

In PC/AT mode, FIRQ and DMA are tri-stated and qualified by DMAEN. The data bus is designed to handle 20 LSTTL loading.

Bit 3 = 0 -
DMA and FIRQ outputs and $\overline{DACK}$ input disabled.

Bit 3 = 1 -
DMA and FIRQ outputs and $\overline{DACK}$ input enabled.

Bit 2 - $\overline{SRST}$, Soft Reset

Bit 2 = 0 -
The Floppy Disk Controller will be reset. After the Soft Reset has occurred, bit 2 is returned to a 1.

Bit 2 = 1 -
Normal or default state.

Bit 1, 0 - DSEL1, 0, Drive Select

The DSEL 1,0 drive select bits are valid only when in the PC/AT Mode.

DS1	DS0	DRIVE SELECT
0	0	$\overline{DS0}$ Active
0	1	$\overline{DS1}$ Active
1	0	$\overline{DS2}$ Active

TABLE 5-5. DRIVE SELECT DECODE

5.3.4 Master Status Registers

The Master Status Register (MSR) is a Read/Write register. The Write Mode and Read Mode of the Master Status Register provide different functions and are discussed separately in this section.

The Write Mode MSR, called MSR1, sets the conditions for drive select and motor enable signals. It also checks for correct polarity on the DRV/PS2 pin for PS/2 drive types.

Table 5-6 shows the sequence to select the PS/2 type of drives and the polarity on DRV/PS2 pin which is tied to pin 2 on the floppy disk drive connector. If this register is not programmed for PS/2 configuration, the $\overline{RWC}$ output from FDC should go to pin 2 of the floppy disk drive connector. The default is AT mode which means that the $\overline{RWC}$ output from the FDC should be tied to Pin 2 of the FDC connector.

A0	$\overline{IOR}$	IOW	Function
0	0	1	Read from Main Status Register (MSR)
0	1	0	Write into Main Status Register (MSR1)
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

TABLE 5-6. MSR/DDR DECODE

The WD76C20 decodes for both the Master Status Register and the Data Register based on five signals: A0, $\overline{RD}$, $\overline{WR}$, $\overline{RD}$, and $\overline{WR}$ as shown in Table 5-5.

5

5.3.4.1 MSR1: Power-Down and PS/2 Support

Address 3F4, A0 = 0, $\overline{IOW}$ = 0 - Write only

In the Write Mode, the MSR1 register contains support for the Power Down Mode and the PS/2 drive type select. You may write to this register to enable the Power Down Mode (option 1), to disable user transparent Power-Down Mode (option 2), and set up the PS/2 type drive configuration. The Power Down-Mode is discussed in more detail in section 7.

7	6	5	4	3	2	1	0
CTST		PSSEL				PD2ENAB	PDM
1	0	3	2	1	0		

Signal Name	Default At Reset
CTST1,0	0
PSSEL3-0	0
PD2ENAB	1
PDM1	0

The storage element for all bits is FF and the clock qualifier is MSRCK.

Bits 7,6 - CTS1-0, reserved

CTS1 and CTS0 should always be zero.

Bit 5 - PSSEL3

PSSEL3 = 1 -
PS2 drive 3 is selected.

Bit 4 - PSSEL2

PSSEL2 = 1 -
PS2 drive 2 is selected.

Bit 3 - PSSEL1

PSSEL1 = 1 -
PS2 drive 1 is selected.

Bit 2 - PSSEL0

PSSEL0 = 1 -
PS2 drive 0 is selected.

Bit 1 - PD2_ENAB, FDC Power Down Option 2

PD2_ENAB = 0 -
User-transparent Power Down Mode option 2 is disabled.

PD2_ENAB = 1 -
User-transparent Power Down Mode option 2 is enabled. A hard reset also enables the PDM option 2. Refer to section 7 for more details.

Bit 0 - PDM, FDC Power Down Mode Option 1

PDM = 0 - Disabled
PDM is set to 0 by a hard or soft reset.

PDM = 1 -
The FDC immediately enters the user-initiated Power Down Mode. Refer to section 7 for more details.

5.3.4.2 MSR: FDC Status Information

Address 3F4, A0 = 0, $\overline{IOR}$= 0 - Read only

In the Read Mode, MSR contains FDC status information and can be accessed at any time.

7	6	5	4	3	2	1	0
RQM	DI/O	EXM	CB	D3B	D2B	D1B	D0B

Signal Name	Default At Reset
Bits 7-0	0

Bit 7 - RQM, Request For Master

RQM = 0 -
The FDC is busy.

RQM = 1 -
The Data Register is ready to send to or receive data from the processor. RQM and DI/O should be used to perform handshaking functions specifying the ready status and signal direction to the processor.

STEP	CODE	REGISTER VALUE	DESCRIPTION	RWC	DRV
1.	3F4	00	Disable FDC Sleep Mode	–	–
2.	3F7	00	Select 500 Kb/sec data rate and 3.5" 1.44 MB in AT Mode	1	1
3.	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$, and DMAEN bits of Operations Register	1	1
4.	3F4	04	Enable bit 2 of MSR and select PS2 drive 0 (1.44 MB)	1	1
5.	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$, and DMAEN bits of Operations Register	1	0
6.	3F4	08	Enable bit 3 of MSR and select	–	–
7.	3F7	02	Select 250 Kb/sec data rate and 3.5" 720 KB	0	0
8.	3F2	2D	Disable $\overline{SRST}$, enable $\overline{DS1}$, $\overline{MO1}$ and DMAEN bit of the Operations Register PSSEL1 (3.5" 720 KB)	0	1

TABLE 5-7. PS/2 SUPPORT SEQUENCE

Bit 6 - DI/O, Data Input

DI/O indicates the direction of the data transfer between the FDC and the processor.

DI/O = 0 -
Transfer is from the processor to the Data Register.

DI/O = 1 -
Transfer is from the Data Register to the processor.

Bit 5 - EXM

EXM operates only during the Execution phase in non-DMA mode.

EXM = 0 -
Execution Phase has ended and the Results Phase has started.

EXM = 1 -
Performing Execution Phase in non-DMA mode.

Bit 4 - CD, Floppy Disk Controller Busy

CB = 0 -
The FDC is not busy.

CB = 1 -
A Read or Write Command is in progress. The FDC will not accept any other command.

Bit 3 - D3B, Floppy Disk Drive 3 Busy

D3B = 0 -
Floppy Drive 3 is not in Seek Mode.

D3B = 1 -
Floppy Drive 3 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 2 - D2B, Floppy Disk Drive 2 Busy

D2B = 0 -
Floppy Drive 2 is not in Seek Mode.

D2B = 1 -
Floppy Drive 2 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 1 - D1B, Floppy Disk Drive 1 Busy

D1B = 0 -
Floppy Drive 1 is not in Seek Mode.

D1B = 1 -
Floppy Drive 1 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 0 - D0B, Floppy Disk Drive 0 Busy

D0B = 0 -
Floppy Drive 0 is not in Seek Mode.

D0B = 1 -
Floppy Drive 0 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

5

5.3.4.3 Overrun Error Status Reporting

The WD76C20 has the capability to detect and flag data overruns during DMA operations. This situation may occur, for example, when a floppy operation, DRAM refresh, and DMA channel 2 transfer occur simultaneously. Should a data overrun occur, D4 (OR) in Status Register 1 (SR1) will be set.

Versions of the WD76C20 which contain this feature can be distinguished easily by reading RTC RAM location 66H after reset. If the device contains the overrun flag feature, the LSB location 66H is 1. In these devices, 66H is read only.

Address 66 - Read only

7	6	5	4	3	2	1	0
							Flag

Signal Name	Default At Reset
Bit 0	1

Bits 7-1 - Not defined

Bit 0 - Flag, Overrun Flag

Flag = 0 -
There is no overrun flag feature supported by this version of the WD76C20 device.

Flag = 1 -
The overrun flag feature is supported by this version of the WD76C20 device.

5.3.5 Status Registers

Address 3F4, A0 = 1, $\overline{CS}$ = 0, $\overline{IOR}$ = 0

There are four read only status registers that are part of the Floppy result phase and contain a variety of status information. They can only be accessed after the execution phase and must be read sequentially, starting with SR0 and going through SR3.

These four status registers are explained on the following pages.

5.3.5.1 Status Register 0

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HS	US1	US0

Signal Name	Default At Reset
All signals	0

Bits 7 - 6 - IC, Interrupt Code

IC 7	IC 6	
0	0	Normal termination of command was completed and properly executed
0	1	Abnormal termination of the command (AT). Execution was started but was not successfully completed
1	0	Invalid command issue (IC). Issued command was never started
1	1	Not defined

Bit 5 - SE, Seek End

SE = 0 -
The FDC has not completed the SEEK command.

SE = 1 -
The FDC has completed the SEEK command.

Bit 4 - EC, Equipment Check

EC = 0 -
Track 0 signal occurred within 77 step pulses per Recalibrate Command.

EC = 1 -
Track 0 signal failed to occur after 77 step pulses per Recalibrate Command and set this flag.

Bit 3 - NR, Not Ready

NR = 0 -
Drive is ready. This is always assumed to be logic 0.

Bit 2 - HS, Head Select

This flag is used to indicate the state of the head at interrupt.

Bit 1 - US1, Unit Select 1

This flag is used to indicate a Drive Unit Number at interrupt.

Bit 0 - US0, Unit Select 0

This flag is used to indicate a Drive Unit Number at interrupt.

5.3.5.2 Status Register 1

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

Signal Name	Default At Reset
All signals	0

Bit 7 - EN, End of Cylinder

EN = 1 -
When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.

Bit 6 - Not used. This bit is always low.

Bit 5 - DE, Data Error

DE = 1 -
The FDC has detected a Cyclic Redundancy Check (CRC) error in either the ID field or the data field and set this flag.

Bit 4 - OR, Overrun

OR = 0 -

The FDC was serviced by the Host during data transfers within a specified time interval.

OR = 1 -
The FDC was not serviced by the Host during data transfers within a specified time interval and this flag was set.

Bit 3 - Not used. This bit is always low.

Bit 2 - ND, No Data

When this bit is high, it can indicate one of several problems with FDC tracking or reading.

ND = 0 -
This flag is not set.

ND = 1 -
During execution of READ DATA, WRITE DELTED DATA, or SCAN, the FDC could not find the section specified in the Internal Data Register (IDR) and this flag was set.

During execution of the READ ID command, the FDC could not read the ID field without an error and this flag was set.

During execution of the READ A TRACK command, the starting sector could not be found and this flag was set.

Bit 1 - NW, Not Writeable

NW = 0 -
This flag is not set.

NW = 1 -
During execution of WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK, the FDC detected a WP from the Floppy Disk Drive and this flag was set.

Bit 0 - MA, Missing Address Mark

MA = 0 -
This flag is not set.

MA = 1 -
If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.

If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time, the Missing Address Mark in the data field (MD) of Status Register 2 is set.

5.3.5.3 Status Register 2

7	6	5	4	3	2	1	0
0	CM	DD	WC	SH	SN	BC	MD

Signal Name	Default At Reset
All signals	0

Bit 7 - Not used. This bit is always low.

Bit 6 - CM, Control Mark

CM = 0 -
This flag is not set.

CM = 1 -
During execution of the READ DATA or SCAN command, the FDC encountered a section that contained a Deleted Data Address Mark and this flag was set.

Bit 5 - DD, Data Error

DD = 0 -
FDC detected no CRC error in the data field.

DD = 1 -
FDC detected a CRC error in the data field and set this flag.

Bit 4 - WC, Wrong Cylinder

This bit is related to the ND bit.

WC = 0 -
This flag is not set.

WC = 1 -
When the contents of Cylinder (C) on the medium is different from that stored in the IDR, this flag is set.

Bit 3 - SH, Scan Equal

SH = 0 -
During execution of the SCAN command, the condition of equal is not satisfied.

SH = 1 -
During execution of the SCAN command, the condition of equal is satisfied and this flag is set.

Bit 2 - SN, Scan Not

SN = 0 -
This flag is not set.

SN = 1 -
The FDC cannot find a sector on the cylinder meeting the condition of SCAN and this flag is set.

Bit 1 - BC, Bad Cylinder

This bit is related to the ND bit.

BC = 0 -
This flag is not set.

BC = 1 -
When the contents of C on the medium does not agree with the IDR and the contents of C is FF, this flag is set.

Bit 0 - MD, Missing Address Mark In Data Field

MD = 0 -
This flag is not set.

MA = 1 -
When data is read from the medium, if the FDC cannot detect a Data Address Mark or Deleted Data Address Mark, then this flag is set.

5.3.5.4 Status Register 3

7	6	5	4	3	2	1	0
0	$\overline{WP}$	RY	T0	$\overline{WP}$	HS	US1	US0

Signal Name	Default At Reset
Bit 7	0
$\overline{WP}$	1
RY	1
T0	0
$\overline{WP}$	1
HS	0
US1	0
US0	0

Bit 7 - Not used. This bit is always low.

This differs from the NEC765.

Bit 6 - $\overline{WP}$, $\overline{WRITE\ PROTECTED}$

This bit is used to indicate the status of the $\overline{WP}$ signal from the Floppy Disk Drive.

$\overline{WP}$ = 0 -
$\overline{WP}$ is asserted.

$\overline{WP}$ = 1 -
$\overline{WP}$ is not asserted.

Bit 5 - RY, Ready

This differs from the 765 standard.

RY = 1 -
This bit is always set to this value because the drive is presumed to be ready.

Bit 4 - T0, Track 0

This bit is used to indicate the status of the Track 0 signal from the FDD.

T0 = 0 -
T0 is not asserted.

T0 = 1 -
T0 is asserted.

Bit 3 - $\overline{WP}$, $\overline{WRITE\ PROTECTED}$

This bit is used by the WD76C20 to indicate the status of the $\overline{WRITE\ PROTECTED}$ signal from the FDD.

$\overline{WP}$ = 0 -
$\overline{WP}$ is asserted.

$\overline{WP}$ = 1 -
$\overline{WP}$ is not asserted.

Bit 2 - HS, Head Select

This bit is used to indicate the status of the Side Select signal to the FDD.

HS = 0 -
Side Select signal is not asserted.

HS = 1 -
Side Select signal asserted.

Bit 1 - US1, Unit Select 1

This bit is used to indicate the status of the Unit Select 1 signal to the FDD.

US1 = 0 -
Unit Select 1 signal is not asserted.

US1 = 1 -
Unit Select 1 signal is asserted.

Bit 0 - US2, Unit Select 2

This bit is used to indicate the status of the Unit Select 2 signal to the FDD.

US0 = 0 -
Unit Select 2 signal is not asserted.

US0 = 1 -
Unit Select 2 signal is asserted.

5.3.6 Data Register

The eight-bit Data Register is a Read/Write register controlling the flow of data that stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain results after a particular command.

The Data Register is selectively decoded by four signals – A0, $\overline{RD}$, $\overline{WR}$, and $\overline{FDCS}$ (CSL code 09) – as shown below.

A0	$\overline{RD}$	$\overline{WR}$	FDCS	FUNCTION
1	0	1	0	Read Data Register
1	1	0	0	Wrote to Data Register

TABLE 5-8. DATA REGISTER DECODE

Address 3F5 - Read and Write

Two bits within the MSR (address 3F4), RQM (bit 7) and DIO (bit 6) are used to perform the handshaking function and transfer data between the Data Register and the processor. All disk data transfer goes through this register. Once the FDC enters the command execution phase, it clears the Data Register of all data to ensure that no invalid data is transferred.

7	6	5	4	3	2	1	0
Register Data							

6.0 IDE DRIVE INTERFACE

This section discusses the components of the WD76C20 that control and oversee the function of the Integrated Drive Electronics (IDE) interface logic. While most of the traditional hard disk controller functions reside on the drive itself, the chip set must still interact at several points with the drive in order to coordinate the transmission of data and address information across the bus.

6.1 IDE DRIVE SIGNAL LOGIC

The WD76C20 provides multiplexing and data path buffering for IDE drive data. Internally, these functions are achieved using pads DB7 and IDED7.

6.2 CHIP SELECT

IDE drive support is handled by the WD76C10 and WD76C20 cooperatively, utilizing chip select logic. Table 6-1 provides a table of the chip select assignments integral to the IDE support. For more information on Chip Select Logic, refer to Section 4.

6.3 IDE/FDD DRIVE SELECTION

The WD76C20 determines whether the IDE drive or the FDD is using the bus. When the CSL decodes for 0A, any reads or writes to address 3F7 or 377 indicate that the Floppy Disk Drive is chosen. When the CSL decodes for 0B, reads to 3F7 indicate the FDD and writes specify the IDE drive. When the CSL decodes for 0C, reads and writes are always selected for a hard disk drive at addresses 1F0 through 1F7 and 170 through 177. When the CSL decodes for 0D, reads and writes are always selected for the hard disk (IDE drive only), at addresses 3F6 - 3F7 and 376 - 377.

6.4 IDE READ/WRITE

The read or write status of the IDE drive is determined by the IDED7 signal which provides a data path for bit 7 between the host and the IDE drive interface. IDED7 becomes an output, writing data from the host to the drive, when $\overline{IOW}$ is driven low. IDED7 is an input signal, reading data from the drive to the host, when $\overline{IOR}$ is low.

The exception to this rule is when the chip is reading from address 3F7. As previously explained, when $\overline{IOR}$ is detected at this location, the floppy DCHG status is output on the host data bus pin DB7.

6.5 IDE DRIVE SELECT

The WD76C20 can support a maximum of two drives. Drive selection is determined by the $\overline{CSIDE0}$ and $\overline{CSIDE1}$ signals. Normally, when $\overline{CSIDE0}$ is driven low, it indicates that drive 0 is on the bus; when $\overline{CSIDE1}$ is driven low, this indicates that drive 1 is on the bus. Both of these signals are activated through a decode in the CSL and are asserted in conjunction with either $\overline{IDEDENL}$ or both $\overline{IDEDENH}$ and $\overline{IDEDENL}$. CSL 0B decodes for $\overline{CSIDE1}$ and 0C decodes for $\overline{CSIDE0}$.

6.6 DATA PATH SELECT

The IDE data path can either be 8- or 16-bits wide. Recognition of this width is made possible using the $\overline{IDEDENL}$ and $\overline{IDEDENH}$ signals. When asserted low, $\overline{IDEDENL}$ and $\overline{IDEDENH}$ indicate a 16-bit path exists. $\overline{IDEDENH}$ is asserted only when A0 is driven low and the CSL has decoded for 0C. $\overline{IDEDENL}$ is asserted when CSL is decoded for 0C or 0D.

PORT	I/O ADDRESS	CS#	FUNCTION
Floppy/Hard Disk Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address
IDE Hard Disk Chip Select	3F6, 3F7[1] 376, 377[1]	0D	Primary Address, IDE Mode Only Seconary Address, IDE Mode Only

TABLE 6-1. IDE CHIP SELECT ASSIGNMENTS

[1] IDE Hard Disk enabled, floppy disabled.

7.0 REAL TIME CLOCK

This section describes the Real Time Clock and its associated registers. A block diagram of the RTC is shown in Figure 7-1.

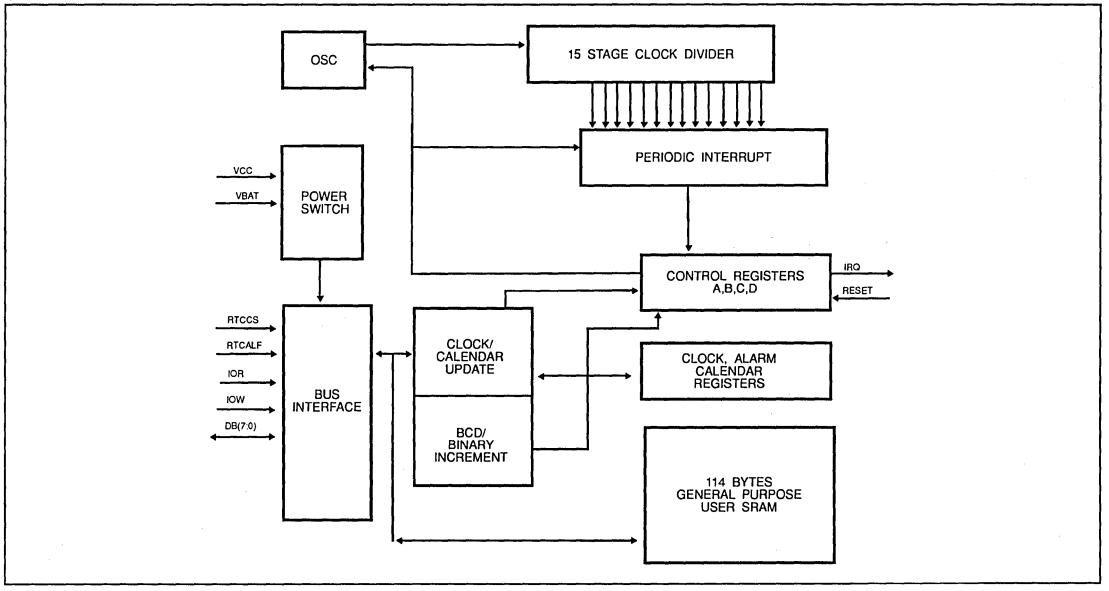

FIGURE 7-1. RTC BLOCK DIAGRAM

Ten SRAM data registers (Registers 00-09) contain all the calendar/clock/alarm information with the RTC crystal-controlled oscillator and frequency divider providing the appropriate timing updates to keep them accurate. Control and status information for the RTC is contained in Registers A-D of the SRAM. Remaining SRAM registers, with a total capacity of 114 bytes, are available to the user.

Read and/or write access to the SRAM (control/status, calendar/clock/alarm, and general purpose registers) is through the RTC bus interface. This interface gets signals from the 76C20 Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the 76C20 internal bus and the RTC internal bus accessing the SRAM.

Calendar/clock/alarm information is processed through Update Logic that:

- Increments calendar/clock counts based on "ticks" received from the Frequency Divider,
- Attends to Daylight/Standard Time and Leap Year adjustments, and
- Formats/deformats the information as straight binary or binary coded decimal data, as selected.

Input power to the RTC component is from the VBAT pin. Switching from System VDD to battery power is accomplished through two diodes as shown in Figure 7-1.

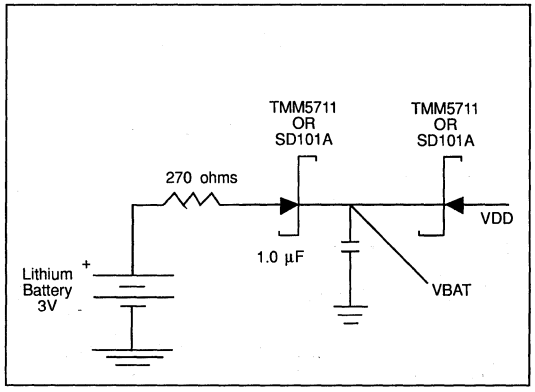

FIGURE 7-2. VBAT EXTERNAL SUPPORT

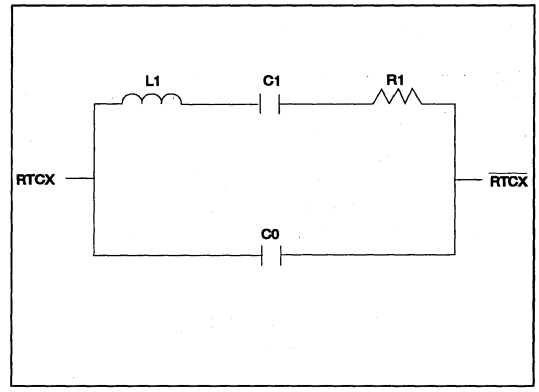

FIGURE 7-4. RTC CRYSTAL PARAMETERS

7.1 TIME BASE OSCILLATOR CIRCUIT

The oscillator that provides the time base for the RTC requires the external circuit shown in Figure 7-2 and the values listed in Table 7-1. The crystal used in parallel with the on-chip oscillator should be an AT-cut crystal with a 32.768 KHz resonant frequency as shown in Figure 7-3, using signals listed in Table 7-2. When in battery backup mode, this circuit is still active, providing the rest of the RTC with a valid time base.

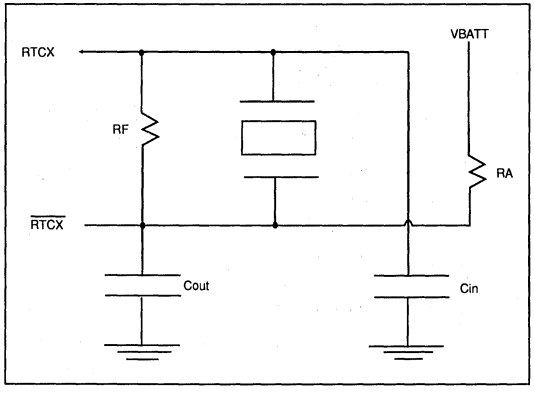

FIGURE 7-3. RTC CRYSTAL EXTERNAL CIRCUITRY

7.2 POWER SWITCH

This functional block is used to detect when the system power is shutting down and the RTC needs to go into battery backup mode. In the event of a full chip power-down without a battery backup, the VRT bit of register D will be reset to zero, indicating that the contents of the SRAM and RTC operational registers are not guaranteed. In order to reset the bit, register D must be read after a full power-up.

7.3 BUS INTERFACE

The RTC Bus Interface block is used to access the internal bus for the WD76C20. Protocol is maintained between the BIL block (Bus Interface Logic) and the RTC Bus Interface. The BIL block generates the $\overline{RD}$ and $\overline{WR}$ strobes, and the $\overline{CS}$ signals are decoded from the external bus by the Chip Select Logic.

7.4 CLOCK DIVIDER

This functional block uses clock divider logic to split the 32.768 KHz time base down to a 1 Hz signal that can be used by the timekeeping blocks. It also provides the periodic interrupt block with access to all stages of the division.

7.5 PERIODIC INTERRUPT

This functional block has access to the various stages of the Clock Divider. Using these signals under the direction of register A, an RTCIRQ pulse can be generated periodically for the processor, varying from once every 122 µS to once every 500 ms. The Periodic Interrupt function is enabled by the PIE bit in register B.

7.6 BCD/BINARY INCREMENT & CLOCK/CALENDAR UPDATE

This dual purpose logic block is used to increment and update the 10 timing registers and to check for the existence of an alarm condition. Several register bits are used to control this block, preventing contention between a processor seeking access to the information registers and the occurrence of an update cycle.

7.7 OPERATIONAL REGISTERS

Shown in Figure 7-2 is a memory map of the RTC, SRAM and operational registers. Under normal conditions all these registers are Read/Write except:

- Registers C and D are Read Only.
- Bit 7 of register A is Read Only.
- The high order bit of the seconds byte is Read Only.

7.7.1 Setting Correct Time

Writing the correct time to the RTC is done using this sequence:

1. Program the SET bit in register B to 1 and the Data Mode bit (DM) of Register B to the appropriate level.
2. Load the 10 bytes representing the current time and alarm status from the host into the RTC by addressing the appropriate memory locations and performing a normal I/O Write operation.
3. After all 10 timing bytes and the DM bit have been written to the RTC, the SET bit should be cleared.

After this, the DM bit cannot be changed without reinitializing all 10 registers.

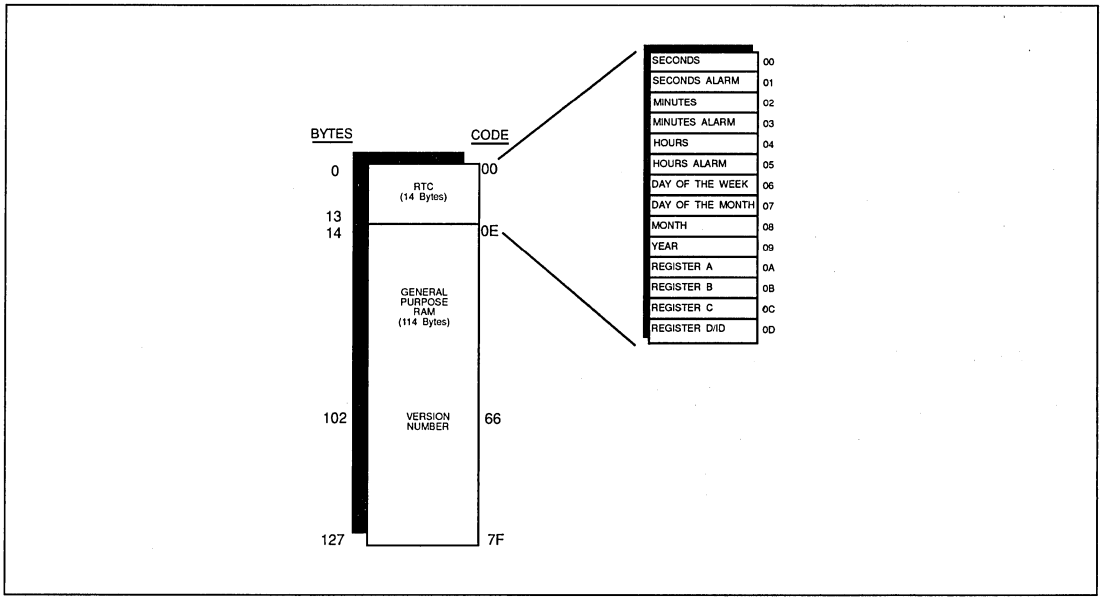

FIGURE 7-5. RTC ADDRESS MAP

ADDRESS	FUNCTION	RANGE		
		DECIMAL	BINARY	BCD DATA
00	SECONDS	0 - 59	00 - 3B	00 - 59
01	SECONDS ALARM	0 - 59	00 - 3B	00 - 59
02	MINUTES	0 - 59	00 - 3B	00 - 59
03	MINUTES ALARM	0 - 59	00 - 3B	00 - 59
04	HOURS - 12 HOUR MODE HOURS - 24 HOUR MODE	1 - 12 0 - 23	01-0C am,81-8C pm 00 - 17	01-12, 81-92 00 - 23
05	HOURS ALARM - 12 HOUR MODE HOURS ALARM - 24 HOUR MODE	1 - 12 0 - 23	01-0C am,81-8C pm 00 - 17	01-12, 81-92 00 - 23
06	DAY OF THE WEEK (SUNDAY = 1 etc.)	1 - 7	01 - 17	01 - 17
07	DATE	1 - 31	01 - 1F	01 - 31
08	MONTH	1 - 12	01 - 0C	01 - 12
09	YEAR	0 - 99	00 - 63	00 - 99

TABLE 7-1. RTC DATA MODES

Table 7-1 shows the Binary and BCD formats of the time, calendar and alarm locations. When the 12-hour format is selected, the high order bit of the hours byte represents AM when it is 0, and PM when it is 1. Once a second, the 10 bytes are updated and checked for alarm conditions. If a Host Read of the time occurs during an update, the hours, minutes, and seconds may not agree. Methods to avoid this possibility are covered later.

7.7.2 Setting Alarm Intervals

Alarms can be set to interrupt the Host in a variety of ways, designating intervals ranging from once a second to once a day. To set periodicity: write don't care bytes (any value from C0 to FF) into the appropriate alarm registers. In this way, an alarm scheduled to interrupt the Host only once a day would have all alarm registers programmed to the proper values. An alarm scheduled to go off once an hour would have a don't care value in the hour register. One scheduled to go off every minute would have don't care values programmed into hours and minutes. An alarm will go off every second if all three registers are programmed to don't cares.

7.7.3 RTC Register A

Address 0A - Bit 7 Read only, Bits 6-0 Read/Write

7	6	5	4	3	2	1	0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Signal Name	Default At Reset
UIP	None
DV2-0	None
RS3-0	None

Bit 7 - UIP, Update In Progress

Used by the Host to determine when updates are not going to occur.

UIP = 0 -

The Host can assume that a transfer is not going to happen for at least another 244 µs, during which time registers 9 through 0 are fully available. Writing 1 to the SET bit (Register B, bit 7) inhibits any further updates and clears the UIP bit.

UIP = 1 -

An update is in progress during which time registers 9 through 0 are not available.

Bits 6-4 - DV2-0, Oscillator Control 2-0

DV2, DV1 and DV0 enable and disable the oscillator for use during product shipping. The code 010 will turn the oscillator on and start dividing.

Bits 6-4 - DV2-0, Oscillator Control 2-0

RS3, RS2, RS1 and RS0 are used to select the periodic interrupt rate as shown in Table 7-2. Once the rate is selected, use the PIE bit (Register B, bit 6) to enable the interrupt. Functionally, these pins are decoded to select which spot on the divider chain should be tapped in order to generate interrupts.

REGISTER A BITS				PERIODIC
RS3	RS2	RS1	RS0	INTERRUPT RATE
0	0	0	0	None
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 µs
0	1	0	0	244.141 µs
0	1	0	1	488.281 µs
0	1	1	0	976.5625 µs
0	1	1	1	1.953125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	125 ms
1	1	0	1	250 ms
1	1	1	0	500 ms
1	1	1	1	

TABLE 7-2. RTC PERIODIC INTERRUPT RATE DECODER

7.7.4 RTC Register B

Address 0B - Read and Write

7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	0	DM	24/12	DSE

Signal Name	Default At Reset
SET	0
PIE	0
AIE	0
UIE	0
Bit 3	0
DM	None
24/12	None
DSE	None

Bit 7 - SET, Write to registers 9-0 in progress

SET = 0 -
Normal operation.

SET = 1 -
A Write to registers 9 through 0 can proceed without the possibility of an update cycle occurring part way through.

Bit 6 - PIE, Period Interrupt Enable

PIE = 0 -
Normal operation.

PIE = 1 -
The Host is interrupted whenever the Periodic Interrupt Flag (PIF at Register C, bit 6) is set to 1.

Bit 5 - AIE, Alarm Interrupt Enable

AIE = 0 -
The Host is not interrupted as a result of the AF.

AIE = 1 -
The Host is interrupted whenever the Alarm Flag (AF at Register C, bit 5) is set to 1.

Bit 4 - UIE, Update Interrupt Enable

UIE = 0 -
The Host is not interrupted as a result of the UF.

UIE = 1 -
The Host is interrupted whenever the Update Flag (UF at Register C, bit 4) is set to 1.

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Bit 3 - Reserved, should be set to zero (default state at reset)

DM, Data Mode

The DATA Mode control bit sets and indicates whether the time is stored in binary or BCD format.

DM = 0 -
Binary coded decimal data.

DM = 1 -
Binary data.

Bit 1 - 24/12, 24- or 12-hour format

24/12 = 0 -
The time is set to a 12-hour AM, PM format.

24/12 = 1 -
The time is set to a 24-hour format.

Bit 0 - DSE, Daylight Savings Enable

The Daylight Savings Enable bit allows the RTC to perform adjustments required to maintain daylight savings: on the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM, and on the last Sunday in October at 1:59:59 AM, it changes to 1:00:00 AM

DSE = 0 -
Daylight savings time is not enabled.

DSE = 1 -
Daylight savings time is enabled.

7.7.5 RTC Register C

Address 0C - Read only

7	6	5	4	3	2	1	0
IRQF	PIF	AIF	UP	Reserved			

Signal Name	Default At Reset
IRQF	0
PIF	0
AIF	0
UF	0
Bits3-0	0

Bit 7 - IRQF, Interrupt Request Flag

IRQF = 0 -
The RTC is not issuing a Host service interrupt request.

SET = 1 -
The RTC is issuing a Host service interrupt request. The Boolean equation for the flag is:

$$IRQ = PF\ PIE + AF\ AIE + UF\ UIE$$

Bit 6 - PIF, Period Interrupt Flag

The PIF bit is independent of the PIE bit, but the PIE bit still controls whether or not an $\overline{\text{RTCIRQ}}$ pulse is generated.

PIF = 0 -
The divider tap determined by the decoded RSX lines did not change state.

PIF = 1 -
The divider tap determined by the decoded RSX lines changed state. The bit is cleared by reading Register C or resetting the WD76C20.

Bit 5 - AIF, Alarm Interrupt Flag

AIF = 0 -
An alarm condition has not occurred.

AIF = 1 -
An alarm condition has occurred, either because of a timing match or "don't care" conditions. AIF is cleared by reading Register C or resetting the WD76C20.

Bit 4 - UF, Update Ended Interrupt Flag

UIE = 0 -
UF is reset during each update cycle.

UIE = 1 -
UF is set after each update cycle.

Bit 3-0 - Reserved, 0 default at reset

7.7.6 RTC Register D

Address 0D - Read only

7	6	5	4	3	2	1	0
IRQF	PIF	AIF	UP	Reserved			
				ID3	ID2	ID1	ID0

Signal Name	Default At Reset
VRT	None
Bits6-4	0
ID3-0	None

Bit 7 - VRT, Valid RAM and Time

The RTC uses Valid RAM and Time to indicate the possibility of corruption in the SRAM memory locations.

VRT = 0 -

The time and calendar are not valid. An interrupt in the power occurred during which neither VBAT or VDD provided sufficient voltage.

VRT = 1 -

The time and calendar are valid. An interrupt in power either did not occur, or VBAT or VDD provided sufficient voltage.

Bits 6-4 - Not used, state is ignored

Bit 3-0 - ID3-0, Revision ID Code

ID3, ID2, ID1, and ID0 are used to indicate the device ID code. This code identifies the chip during board-level testing.

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8.0 POWER MANAGEMENT: SUSPEND/RESUME LOGIC

Suspend/Resume Logic is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10. This can switch to a 32.768 KHz clock during the Suspend mode. While in Suspend mode, the WD76C20 typically draws less than 2 mA.

The Suspend/Resume Logic also provides the external DRAM refresh signal, PDREF, that pulses active low once every 15.26 µS. This logic also supports a latched signal that causes $\overline{\text{CSSERA}}$, $\overline{\text{CSSERB}}$ and $\overline{\text{CSPAR0}}$ to remain low during Suspend mode, signaling the WD76C30 to disable the 48 MHz crystal.

Like several other functions discussed in this databook, the Suspend/Resume function is supported by the entire chip set, especially the WD76C20 and WD76C30. In the discussion that follows, much of the material can also apply to other members of the chip set. To see the interconnection of chips during this process, refer to Figure 8-x.

8.1 OVERVIEW

The WD7600's power management saves power whenever possible without degrading the system's performance. Whenever the system perceives itself as not doing anything "useful," it powers down. This both slows the clock speed and cuts down on power consumption. The full power-down sequence is called system Suspend. The power-up sequence from system Suspend is called Resume.

8.1.1 Suspending the System

Suspend is initiated by a change in the state of certain Power Management Control (PMC) input(s). This change can either be programmed to generate a NMI or a Local Attention. If a PMC input is programmed to cause a Local Attention, the Local Attention signal has to be tied to an IRQ level. Once tied to interrupts, it can be determined when a system is performing an "idle" task. When it is known that the system is performing such a task, the processor can be safely powered down. The processor is then awakened on the next unmasked DRQ, IRQ, or NMI.

Once the processor is halted, it is awakened by an IRQ, which means that it will come out of power down on every IRQ0 once every 55 µs.

Several conditions are used by the processor to confirm an "idle" state. These are:

- Low battery condition
- External switch tied to a PMC interrupt enable that generates an IRQ
- Software-initiated suspend corresponding to a hardware interrupt (for example, an INT77H for IRQ15H)
- Watchdog timer generates a PMC interrupt to the WD76C10 (which in turn generates an IRQ) whenever it recognizes it is not being used.

Any of the preceding reasons are valid for ascertaining that the system is idle. The following is a general description of the Suspend sequence:

1. Any change in PMC input signals the WD76C10 to generate a Local Attention which is tied to an IRQ leading to the processor.

   The processor vectors to the power-down routine and the processor saves its internal states and the states of all peripherals attached to it that are to power down.

   The processor saves the states into a protected area of the system DRAM (similar to the shadowed BIOS). If the entire AT bus is to be powered down, the processor writes to the BUS POWER DOWN ENABLE bit in the WD76C10.
2. The power down routine (in a loadable driver) writes to the full-power-down bit in the WD76C10 which enables the power-down sequence. The WD76C10 switches to sampling of the PMC inputs with the 14.318 MHz clock instead of the AT BUS clock.
3. The processor then writes to an I/O register in the WD76C10 that switches a PMC output connected to the PWRDN input pin of the WD90C20. On assertion of the PWRDN signal, the VGA controller enters the Power Down mode which refreshes the video DRAM via the AT BUS REFRESH signal. This is done so that the PIXCLK clock generator can later be powered down and the VGA controller can continue refresh. CAS before RAS refresh is the preferred way of refreshing the DRAMs because it allows lower power operation

without the generation of a DRAM refresh address.

4. The processor then writes to the KILL 48 MHz register which sends a CSL address code of 15H to the WD7600 encoded Chip Select Bus (ENCSBUS). The WD76C20 decodes the 15H (qualified by an IOW) and disables its 16 MHz oscillator, errorlessly switches the 14.318 MHz oscillator signal to a 32 KHz, 50% duty cycle signal, then disables the 14.318 MHz oscillator. The WD76C20 also asserts the CSSERA, CSSERB, and CSPAR signals simultaneously which signals the WD76C30 to disable its 48 MHz oscillator. When this oscillator is disabled, the AT BUS CLOCK, KEYBOARD CLOCK, and 80287 CLOCK are disabled. The processor executes a halt instruction and the WD76C10 detects the halt status from the processor and switches from the AT compatible refresh to the PDREF controlled refresh. The WD76C10 then switches the AT bus compatible REFRESH output signal to mimic the PDREF input signal.

   The PDREF input is a CMOS level clock signal that has a 124 µs period and a low going pulse of 200 ns to 1 µs. This signal is always active and should be adequate for refreshing low power DRAMs. This signal is generated by the WD76C20.
5. On detecting that the 14.318 MHz clock has been changed to 32 KHz, the WD76C10 tri-states all outputs except the PMC controls, DRAM controls, RAD bus, and AT bus REFRESH signal. The CPURES signal is asserted and then tri-stated and is pulled high through a 200K pull-up resistor. All inputs except RSTIN, CLK14, and the PMC are ignored, and all circuitry except the PMC and refresh logic is stopped.

The power is now turned off to the CPU, PIXCLK, BUS, etc. by the assertion of a PMC output from the WD76C10.

Figure 8-1 illustrates the interconnected concepts of Suspend, Resume, and Sleep Mode cycles.

8.1.2 Resuming the System

Resume is initiated by changes to PMC input(s) similar to the Suspend mode.

1. The WD76C10 samples the PMC inputs at 32 KHz. When it detects a change of any enabled PMC inputs, PMC outputs switch and power up the processor, bus, and so on. After 1 ms (timed by the 32 KHz clock input), the WD76C10 samples the processor-power-good PMC input. When this is active, the CPURES is driven high and the rest of the WD76C10 control outputs are driven to their correct states. If the BUS POWER DOWN bit is enabled, a BUS RESET is issued also.
2. Once the chip detects the power-good signal, the WD76C10 performs a write to the ENABLE 48 HMz register which sends a CSL address code of 16H on the ENCSBUS.
3. The WD76C20 receives the 16H address code, enables the 16 MHz and 14.318 MHz oscillators, and deasserts the CSSERA, CSSERB, and CSPAR signals. After approximately 20 ms (stabilizing time for the oscillators), the WD76C20 switches the OSC 32 KHz signal to 14.318 MHz.
4. The WD76C30 enables its 48 MHz oscillator on the deassertion of its CSSERA, CSSERB, and CSPAR input signals.
5. When the WD76C10 detects that the 32 KHz has been switched to 14.318 MHz, it switches the PMC sampling to the AT BUS CLOCK. The WD76C10 then switches from PDREF- controlled refresh to the AT-compatible refresh. The WD76C10 also switches the AT bus REFRESH sign from PDREF input to AT-compatible refresh rate. The WD76C10 deasserts the CPURESET signal and the processor comes out of reset and checks the shutdown status in the RTC RAM on the WD76C20. This tells the processor that it is coming out of full power-down mode as opposed to a warm or cold boot. The processor then restores the states of the machine.
6. The processor writes to the WD76C10 register that causes the WD76C10 to deassert its PMC output. This output is connected to the PWRDN input of the WD90C20 signallng the WD90C20 to come out of the power down mode.

Figure 8-2 illustrates how the WD7600 chip set shares the Suspend/Resume/Sleep Mode duties.

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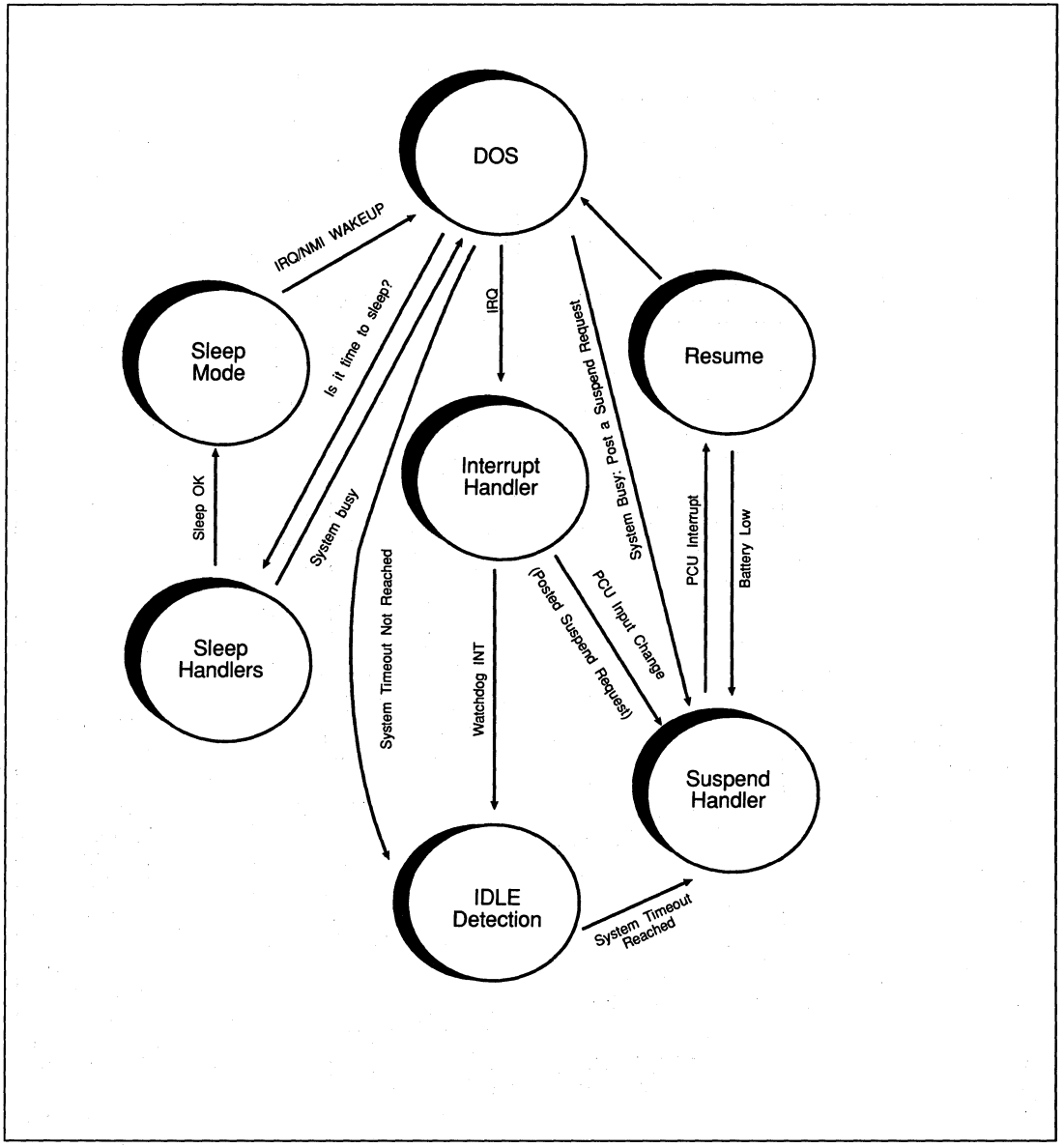

FIGURE 8-1. SUSPEND/RESUME/SLEEP MODE CYCLE

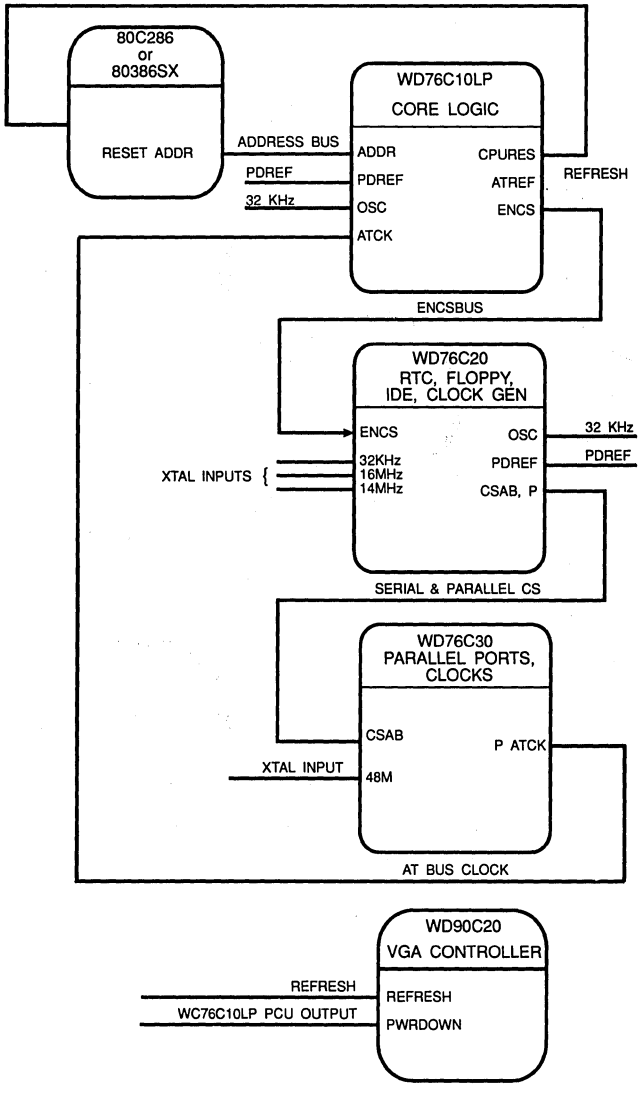

FIGURE 8-2. FULL POWER-DOWN MODE SYSTEM BLOCK DIAGRAM

8.2 PDREF

The PDREF is an external DRAM refresh line used to support the WD76C10 when it goes into Suspend/Resume mode. During Suspend/Resume mode, this pad provides a 1.0 µs pulse once every 15.26 µs (during a 50% duty cycle). This pulse is used to maintain the DRAM integrity with as little power as possible.

8.3 14 MHZ CRYSTAL SPECIFICATIONS

The 14.318 MHz crystal oscillator associated with the Suspend/Resume Logic is shown in Figure 8-3. This timing is maintained through the MX14 and $\overline{MX14}$ pins. MX14 is the input pin for the 14.318 oscillator and $\overline{MX14}$ is the output pin for the oscillator.

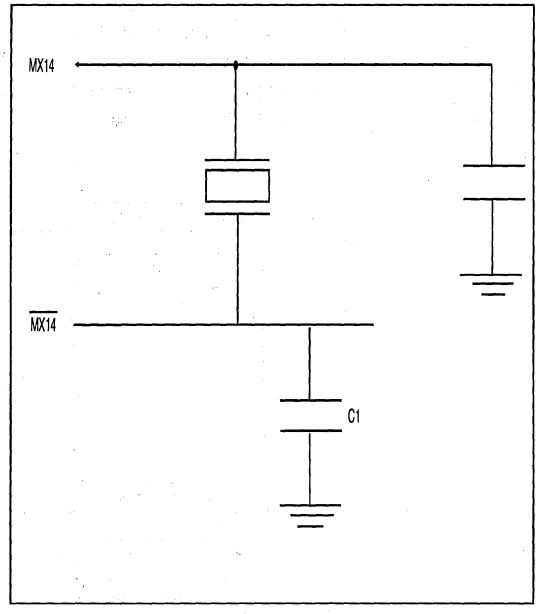

FIGURE 8-3. 14 MHZ CLOCK GENERATION

8.4 PIN STATES DURING POWER DOWN

Table 8-1 shows what happens to the pins during power-down.

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND MODE IN	SUSPEND MODE OUT
1	$\overline{\text{IDEDENH}}$	OUTPUT		O		O		Z
2	VSS	VSS						
3	$\overline{\text{FX1}}$	OUTPUT		Z		Z		Z
4	FX1	INPUT	IH		IH		IH	
5	VDD	VDD						
6	FCLK2	INPUT	IH		IH		IH	
7	$\overline{\text{RDD}}$	SCH INPUT	IH		IH		IH	
8	DMA	BIDIRECT (input unused)	IH	Z***	IH	Z***	IH	Z
9	FIRQ	BIDIRECT	IH	Z***	IH	Z***	IH	Z
10	$\overline{\text{DCHG}}$	SCH W/PULLUP	IH		IH		IH	
11	PCVAL	SCH INPUT	IH		IH		IH	
12	DRV	BIDIRECT SCH (W/PULLUP)	IH	Z	IH	Z	IH	Z
13	$\overline{\text{HS}}$	OUTPUT		Z		Z		Z
14	$\overline{\text{WE}}$	OUTPUT		Z		Z		Z
15	$\overline{\text{WD}}$	OUTPUT		Z		Z		Z
16	VSS	VSS						
17	$\overline{\text{DIRC}}$	OUTPUT		Z		Z		Z
18	$\overline{\text{STEP}}$	OUTPUT		Z		Z		Z
19	$\overline{\text{DS0}}$	OUTPUT		Z		Z		Z
20	$\overline{\text{DS1}}$	OUTPUT		Z		Z		Z
21	$\overline{\text{DS2}}$	OUTPUT		Z		Z		Z
22	$\overline{\text{DS3}}$	OUTPUT		Z		Z		Z
23	$\overline{\text{MO0}}$	OUTPUT		Z		Z		Z
24	$\overline{\text{MO1}}$	OUTPUT		Z		Z		Z
25	VSS	VSS						
26	$\overline{\text{MO2}}$	OUTPUT		Z		Z		Z
27	$\overline{\text{MO3}}$	OUTPUT		Z		Z		Z
28	$\overline{\text{HDL}}$	OUTPUT		Z		Z		Z
29	$\overline{\text{RWC}}$	OUTPUT		Z		Z		Z
30	PWRDN	OUTPUT		OH		OH		OH
31	$\overline{\text{WP}}$	INPUT	IH		IH		IH	

TABLE 8-1. PIN STATES DURING POWER-DOWN

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1		PD OPT2		SUSPEND MODE	
			IN	OUT	IN	OUT	IN	OUT
32	$\overline{TR00}$	INPUT	IH		IH		IH	
33	$\overline{IDX}$	INPUT	IH		IH		IH	
34	VSS	VSS						
35	*DB0	BIDIRECT	I	O	I	O	IH	Z
36	*DB1	BIDIRECT	I	O	I	O	IH	Z
37	*DB2	BIDIRECT	I	O	I	O	IH	Z
38	*DB3	BIDIRECT	I	O	I	O	IH	Z
39	*DB4	BIDIRECT	I	O	I	O	IH	Z
40	*DB5	BIDIRECT	I	O	I	O	IH	Z
41	*DB6	BIDIRECT	I	O	I	O	IH	Z
42	*DB7	BIDIRECT	I	O	I	O	IH	Z
43	IDED7	BIDIRECT	I	O	I	O	IH	Z
44	VDD	VDD						
45	A0	INPUT	I		I		IH	
46	VSS	VSS						
47	$\overline{DACK}$	INPUT	I		I		IH	
48	$\overline{IOR}$	INPUT	I		I		IH	
49	$\overline{IOW}$	INPUT	I		I		IH	
50	$\overline{CSEN}$	INPUT	I		I		I	
51	DACKEN	INPUT	I		I		I	
52	DPH	INPUT	I		I		I	
53	DPL	INPUT	I		I		I	
54	RA10	INPUT	I		I		I	
55	RA9	INPUT	I		I		I	
56	RA8	INPUT	I		I		I	
57	RESET	INPUT	I		I		I	
58	$\overline{RCLR}$	INPUT	I		I		IH	
59	BALE	INPUT (W/ PULLUP)	I		I		IH	
60	$\overline{RTCX}$	OUTPUT		O		O		O
61	RTCX	INPUT	I		I		I	
62	VBAT	VDD						
63	MX14	INPUT	I		I		IH	
64	$\overline{MX14}$	OUTPUT		O		O		Z
65	VSS	VSS						

TABLE 8-1. PIN STATES DURING POWER-DOWN (CONTINUED)

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND MODE IN	SUSPEND MODE OUT
66	PDREF	OUTPUT		O		O		O
67	VDD	VDD						
68	OSC	OUTPUT		O		O		O
69	RTCIRQ	OUTPUT		O		O		O
70	TC	OUTPUT		O		O		O
71	PRDY	INPUT	I		I		IH	
72	$\overline{\text{EMS}}$	OUTPUT		O		O		Z
73	$\overline{\text{PROGCS}}$	OUTPUT		O		O		Z
74	PCUW1	OUTPUT		O		O		O
75	PCUW0	OUTPUT		O		O		O
76	$\overline{\text{NPCS}}$	OUTPUT		O		O		Z
77	$\overline{\text{CS8042}}$	OUTPUT		O		O		Z
78	$\overline{\text{ROMOE}}$	OUTPUT		O		O		Z
79	$\overline{\text{CSPAR0}}$	OUTPUT		O		O		O
80	$\overline{\text{CSSERB}}$	OUTPUT		O		O		O
81	$\overline{\text{CSSERA}}$	OUTPUT		O		O		O
82	$\overline{\text{CSIDE1}}$	OUTPUT		O		O		Z
83	$\overline{\text{CSIDE0}}$	OUTPUT		O		O		Z
84	$\overline{\text{IDEDENL}}$	OUTPUT		O		O		Z

TABLE 8-1. PIN STATES DURING POWER-DOWN (CONTINUED)

9.0 SPECIFICATIONS

9.1 MAXIMUM RATINGS

Absolute Maximum Ratings - All voltages referenced to VSS

VCC .....7.0 Vol

Voltage at any pin ..... + 0.3 Volts

Storage Temperature ..... -55°C to +70°C

9.1 DC OPERATING CHARACTERISTICS

TA=0°C (32°F) to 70°C (158°F)

VCC = 5V ±5%

CL =100 pf; C_{an} =10 pf; C_{inclk} = 20 pf

VIL/VOL referenced to 0.8V

VIH/VOH referenced to 2.0V

CY specifies FX1 period

MCY specifies MCLK period, dependent on selected data rate

WCY specifies MCLK period, dependent on selected data rate

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
VCC	+5V Supply	4.75	5.25	V
VBAT	Battery Backup Voltage	2.6	VDD	V
VIL	Input Low Voltage - Data Bus & XTOCS		0.8	V
VIH	Input High Voltage - Data Bus & XTOCS	2.0		V
VILT	Input Low Threshold - Schmitt Trigger	0.8		V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysteresis	0.5		$V_{typical}$
VOLAT	Output Low - DBus, FIRQ, DMA; IO=12.0 mA		0.4	V
VOHAT	Output High - DBus, FIRQ, DMA; IO= -5.0 mA	2.8		V
VOLHC	Output Low - Drive Interface IO=48 mA		0.4	V
VOL	Output Low - All Others; IO=4.0 mA		0.4	V
VOH	Output High - All Others; IO=400 uA	2.8		V
ILUL	Latch Up Current Low	40		mA
ILUH	Latch Up Current High	-40		mA
ILL	Leakage Current Low		10	uA
ILH	Leakage Current High		-10	uA
ICC	Supply Current - 100 uA source loads		70	mA
ICC	Supply Current - 5 mA source loads		140	mA
ICCPDM1	Supply current in power down mode[1] (Option 1)		200	$uA_{typical}$
ICCPDM2	Supply current in power down mode[1] (Option 2)		2	$mA_{typical}$
ICCPDM3	Supply current in chip set power down mode		2	mA
ICCBAT	Supply current in battery backup mode[1]		50	uA
PD	Power Dissipation - ICC max[3]		700	mW
PDHL	Power Dissipation - ICCHL max[2 3]		850	mW

TABLE 9-1. DC CHARACTERISTICS

[1] Vin = VCC or GND, IO=0 mA
[2] Includes DBx; IO=-5.0 mA source loads
[3] Includes open drain high current drivers at Vol=0.4V

9.3 CRYSTAL CAPACITANCE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
	RTC CRYSTAL			
R1	Crystal Motional Resistance		40	K Ohm
C0	Crystal Shunt Capacitance		1.7	pF
C1	Crystal Motional Capacitance		0.0035	pF
Q	Crystal Quality Factor	50		K
CI_{in}	Crystal Circuit Input Capacitance	15	± 5%	pF
C_{out}	Crystal Circuit Output Capacitance	15	± 5%	pF
RA	Crystal Circuit Drive Level Resistor	422	± 1%	K Ohm
Rf	Crystal Circuit Feedback Resistor	15	22	M Ohm
	16 MHZ CRYSTAL			
R_{series}	Crystal Circuit Resistors	30		Ohm
C_{shunt}	Crystal Output	10		pF
C_1	Crystal Input Capacitance	47	± 5%	pF
C_2	Crystal Output Capacitance	15	± 5%	pF
	14 MHZ CRYSTAL			
Rseries	Crystal Circuit Resistors	30		Ohm
C_{shunt}	Crystal Output	10	± 5%	pF
C_1	Crystal Input Capacitance	22	± 5%	pF
C_2	Crystal Output Capacitance	22		pF

TABLE 9-2. CRYSTAL CAPACITANCE

10.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into four main categories:

- Floppy Disk Controller Specification
- Real Time Clock Specifications
- IDE Interface Timing
- Suspend/Resume Support Timing
- Chip Select Logic Decode Timing

Each table provides timing specifications which are followed by a figure displaying a timing diagram.

10.1 FLOPPY DISK CONTROLLER SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1MCY + 150	ns

TABLE 10-1. FDC READ TIMING SPECIFICATION

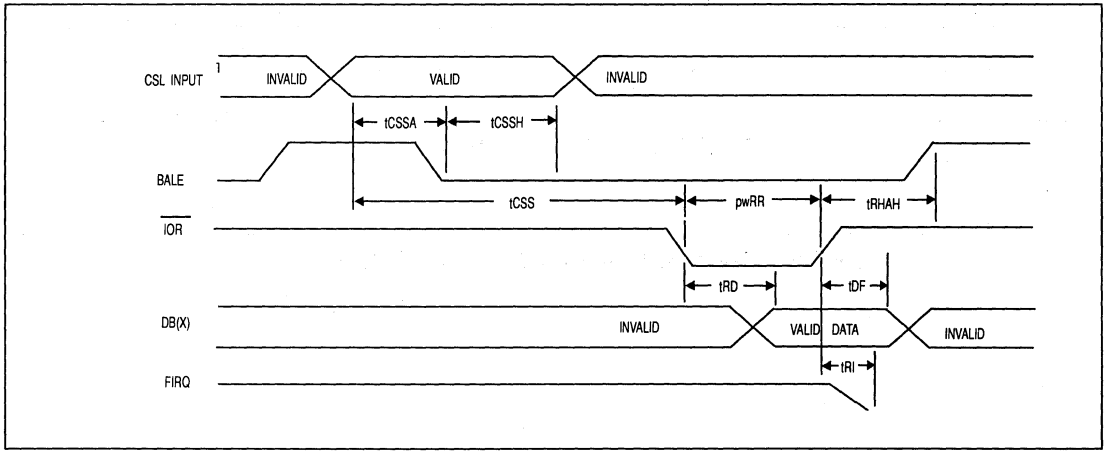

FIGURE 10-1. FDC READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1 MCY +150	ns

TABLE 10-2. FDC READ W/BALE TIMING SPECIFICATION

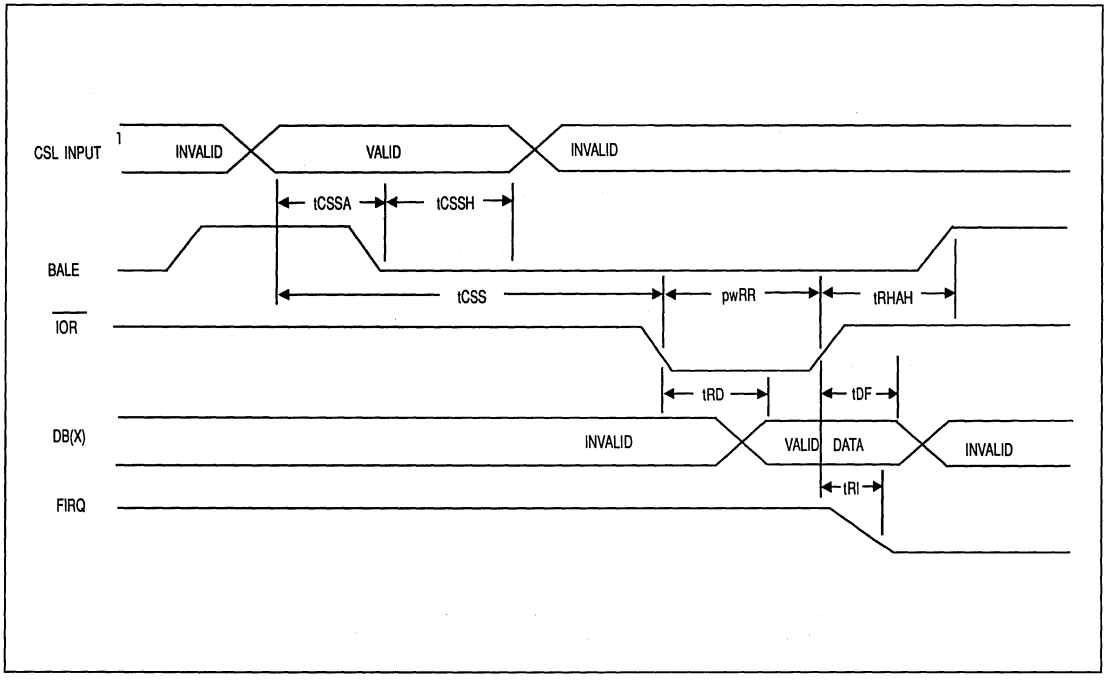

FIGURE 10-2. FDC READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1MCY + 150	ns

TABLE 10-3. FDC WRITE TIMING SPECIFICATION

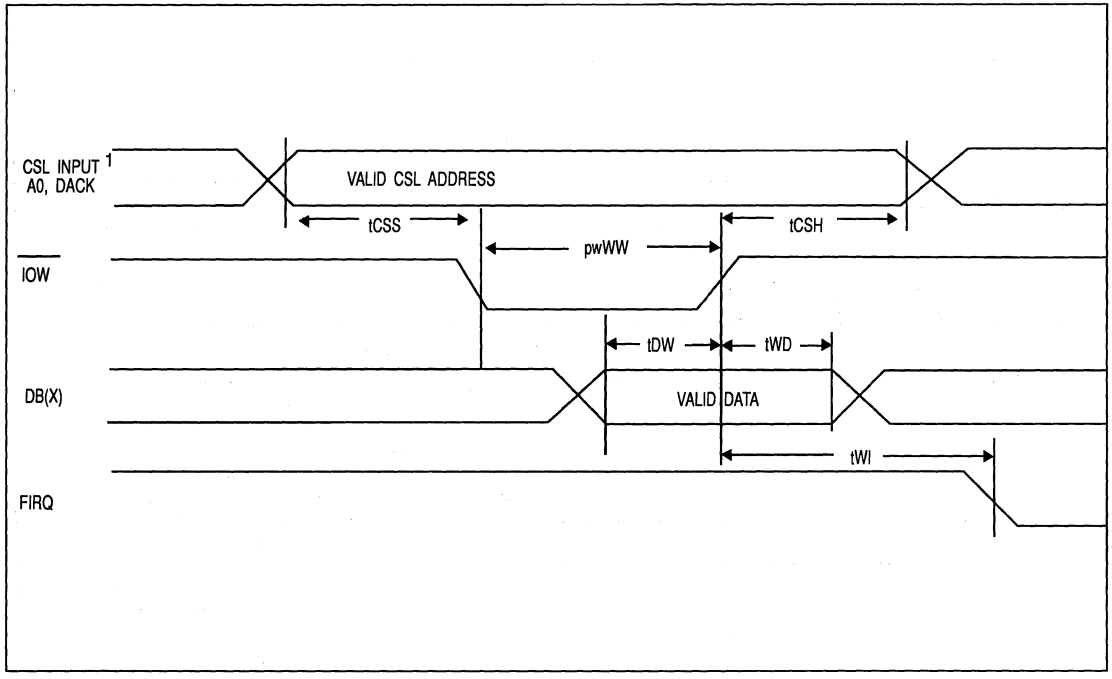

FIGURE 10-3. FDC WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1 MCY +150	ns

TABLE 10-4. FDC WRITE W/BALE TIMING SPECIFICATION

5

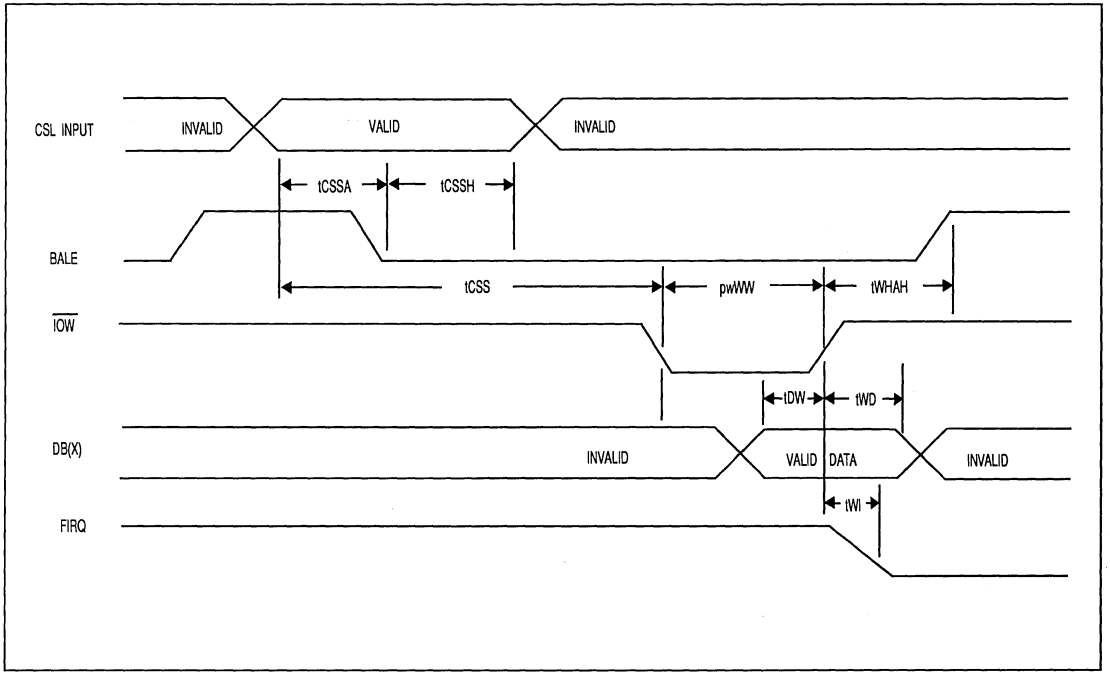

FIGURE 10-4. FDC WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tMCY	DMA Cycle Time	52		MCY
tMA	$\overline{DACK}$ Delay Time from DMA High	0		ns
tAM	DMA Reset Delay Time from $\overline{DACK}$ Low		140	ns
tAA	$\overline{DACK}$ Width	125		ns
tMRW	$\overline{IOR}$ or $\overline{IOW}$ Response from DMA High		48	MCY
tMtMR	$\overline{IOR}$ Delay from DMA	0		ns
tMW	$\overline{IOW}$ Delay from DMA	0		ns
tRD	Data Access Time from $\overline{IOR}$ Low		120	ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-5. FDC DMA TIMING SPECIFICATION

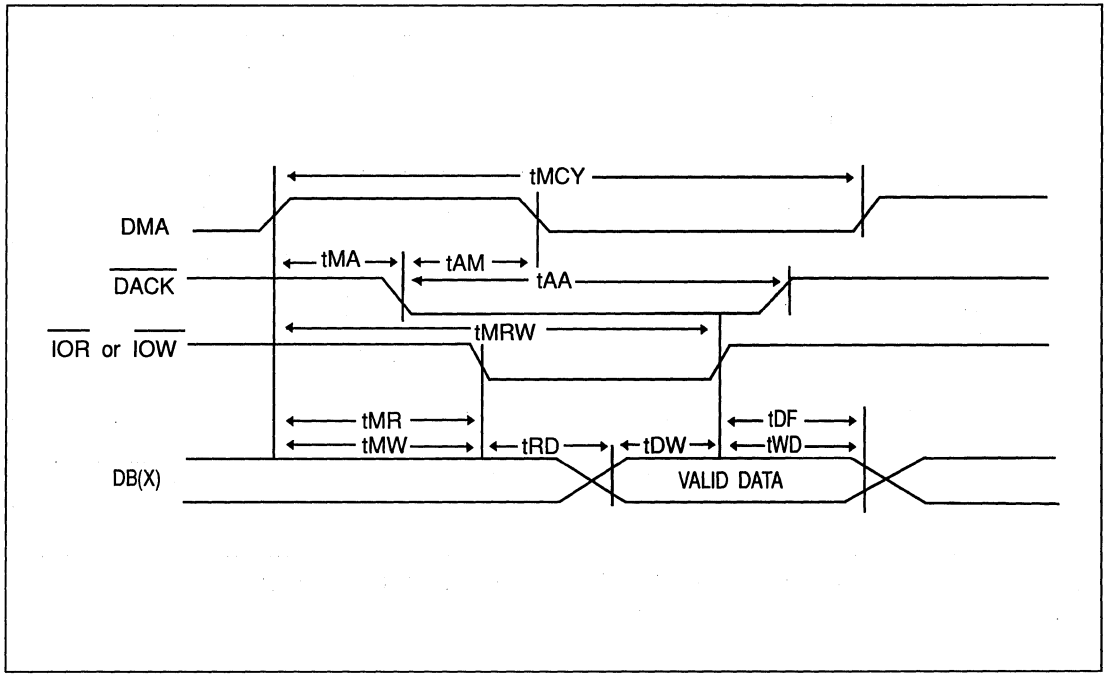

FIGURE 10-5. FDC DMA TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tTCR	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOR}$	0	192	MCY
tTCW	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOW}$	0	384	MCY
tTC	DACKEN High, $\overline{CSEN}$ Low Pulse Width	60		ns
tTCA	DACKEN High, $\overline{CSEN}$ Low to TC Asserted	0	30	ns
tTCD	DACKEN Low, $\overline{CSEN}$ High to TC De-Asserted	0	30	ns

TABLE 10-6. FDC TERMINAL COUNT TIMING SPECIFICATION

5

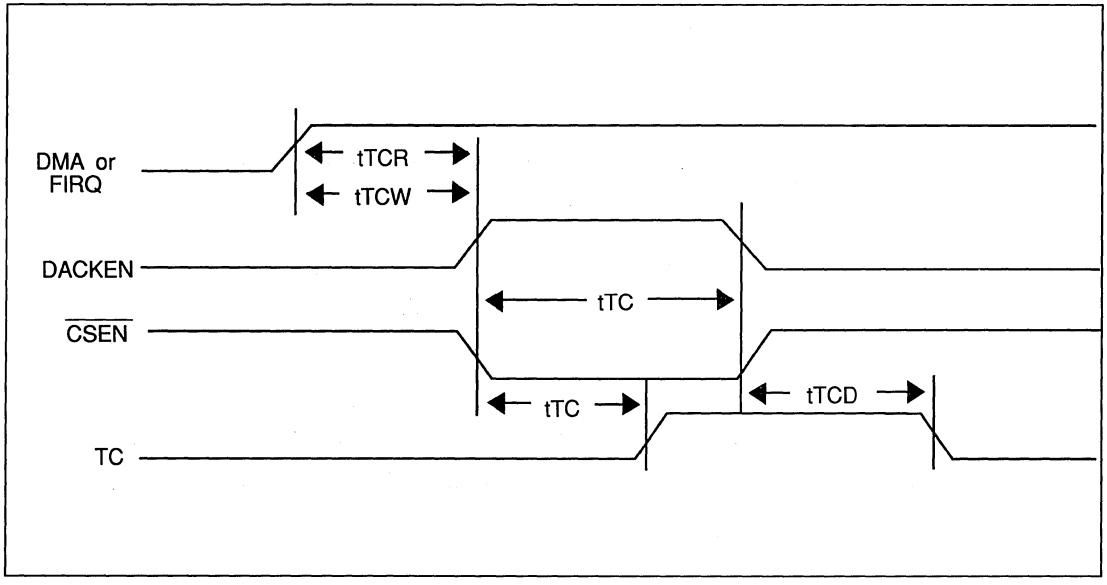

FIGURE 10-6. FDC TERMINAL COUNT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCY	Clock Period	60		ns
tR	Clock Rise Time		5	ns
tF	Clock Fall Time		5	ns
tPH	Clock Active (High or Low)	25		ns

TABLE 10-7. FDC 16 MHZ CLOCK TIMING SPECIFICATION

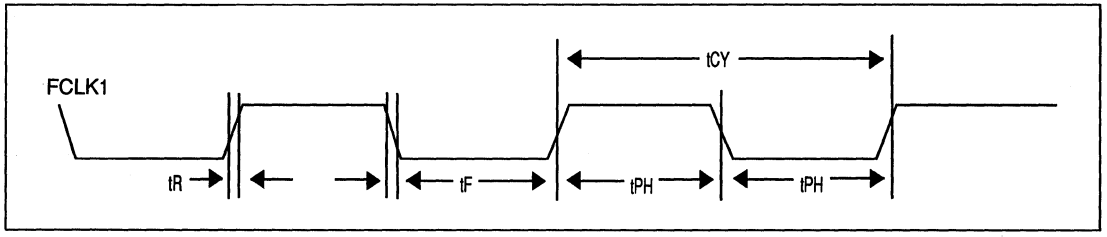

FIGURE 10-7. FDC 16 MHZ CLOCK TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tDST	$\overline{\text{DIRC}}$ Set Up to $\overline{\text{STEP}}$ Low	4		MCY
tSTP	STEP Active Time Low	24		MCY
tSTD	DIRC Hold Time from STEP High	96		MCY
tSC	STEP Cycle Time	132		MCY
tSTU	DS(x) Hold Time from STEP Low	20		MCY
tIDX	IDX Index Pulse Width	1		MCY
tRDD	RDD Active Time Low	40		ns
tWDD	WD Write Data Width Low	1/2		WCY

TABLE 10-8. FDC DISK DRIVE TIMING SPECIFICATION

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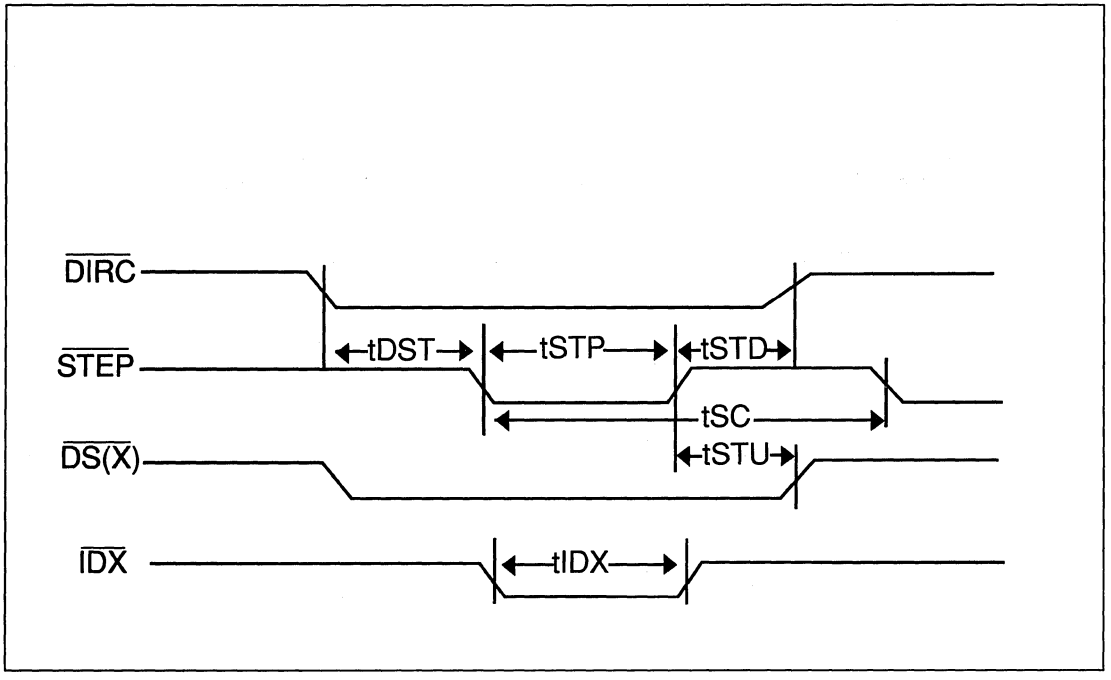

FIGURE 10-8. FDC DISK DRIVE TIMING DIAGRAM

10.2 REAL TIME CLOCK SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle IOW Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle IOW or IOR Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-9. RTC AND RAM READ TIMING SPECIFICATION

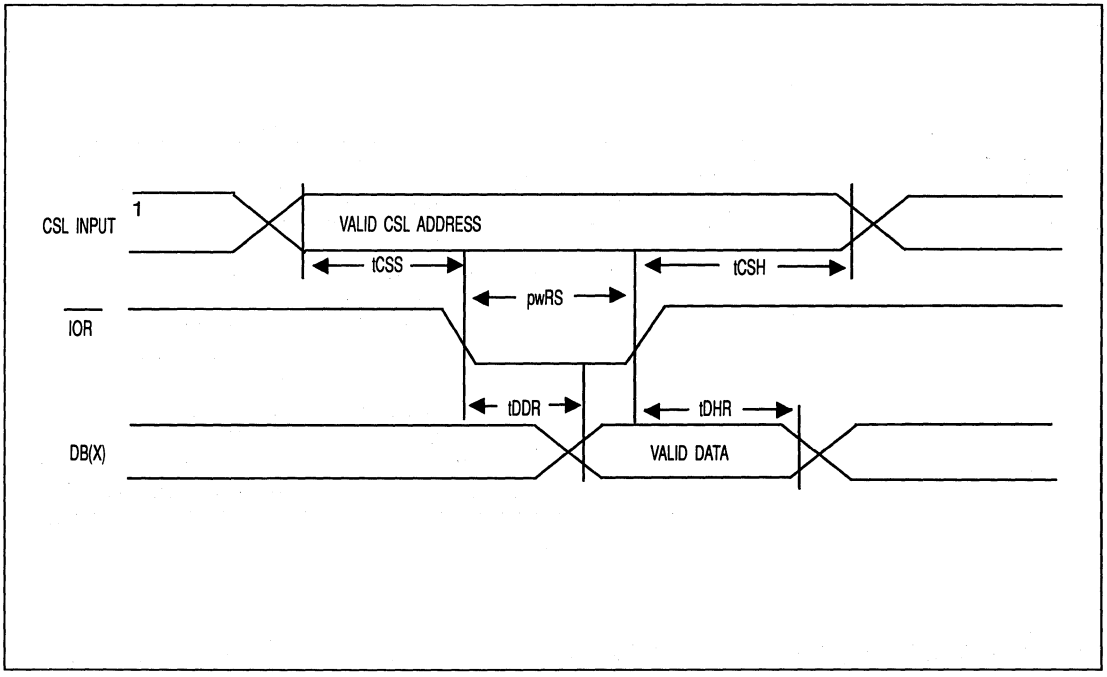

FIGURE 10-9. RTC AND RAM READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDSW	Address or Data Setup Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-10. RTC AND RAM WRITE W/BALE TIMING SPECIFICATION

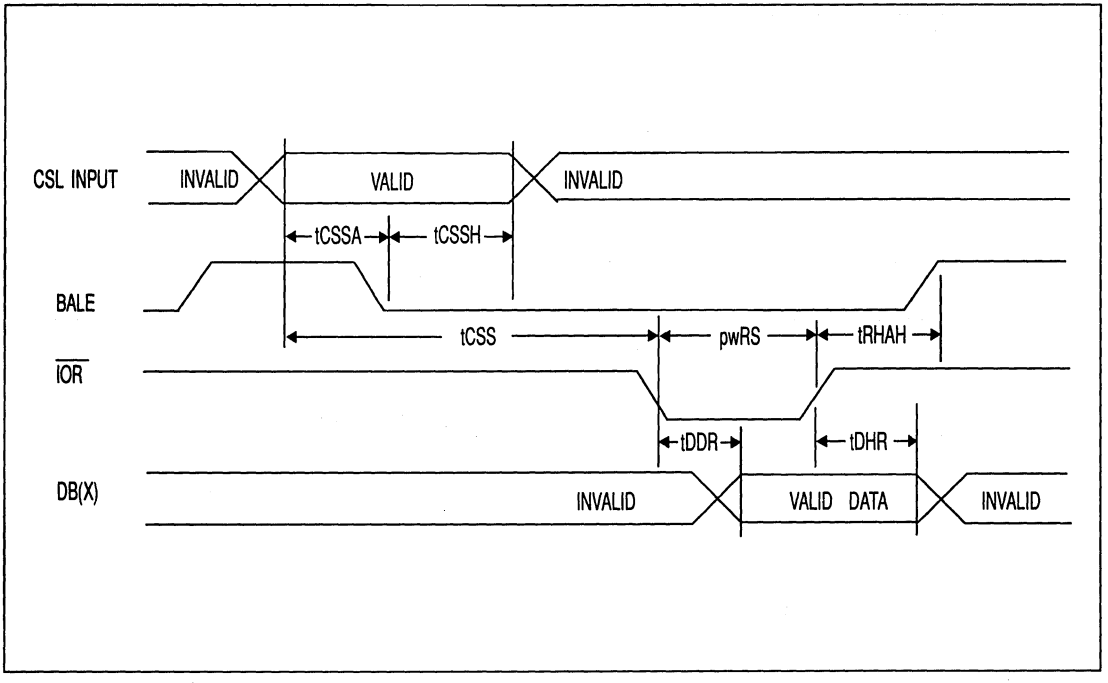

FIGURE 10-10. RTC AND RAM READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDSW	Address or Data Set Up Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-11. RTC AND RAM WRITE TIMING SPECIFICATION

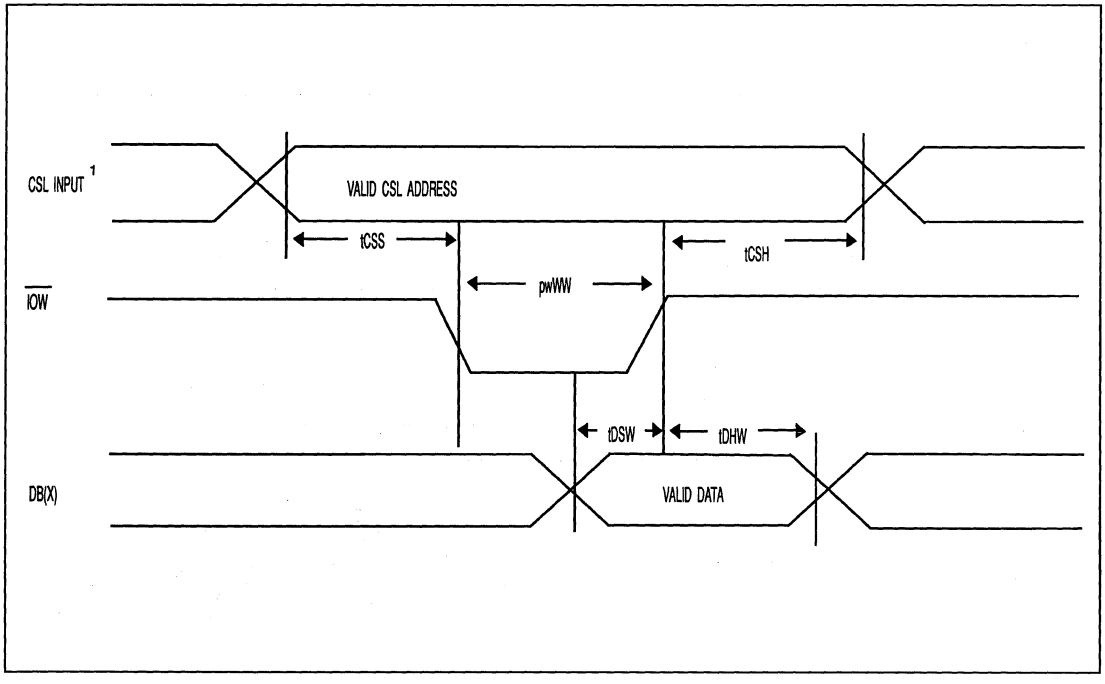

FIGURE 10-11. RTC AND RAM WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-12. RTC AND RAM READ W/BALE TIMING SPECIFICATION

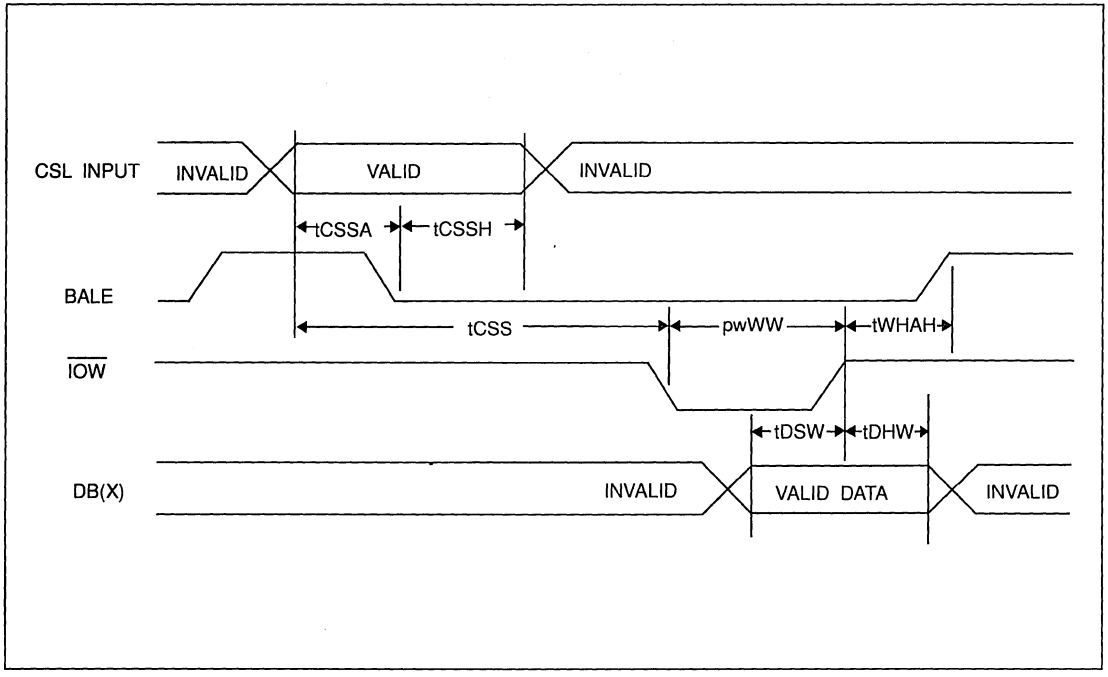

FIGURE 10-12. RTC AND RAM WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tRLIQ	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{IOR}}$ (Qualified by RECS)		2	µS
tRLIH	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{RESET}}$		2	µS

TABLE 10-13. RTC IRQ RELEASE TIMING SPECIFICATION

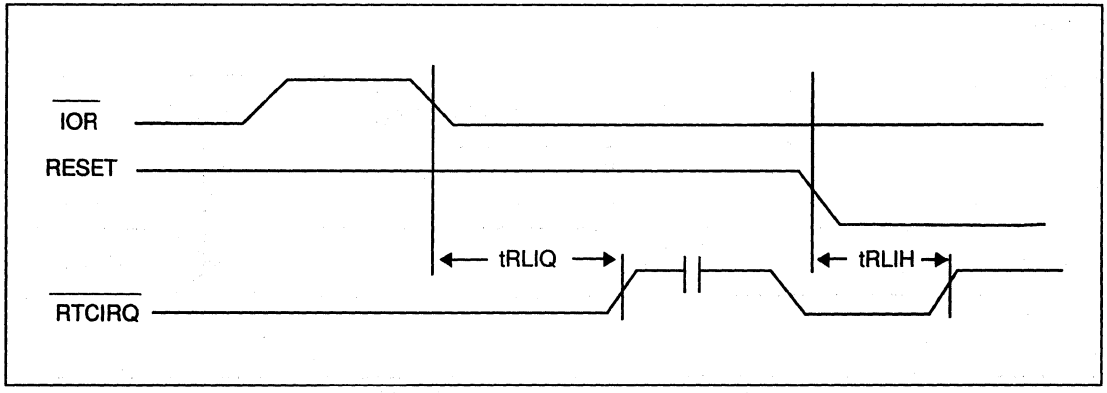

FIGURE 10-13. RTC IRQ RELEASE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tPRST	Power on Reset Width	200		ns
tRST	Reset Width	5		µS
tCA	Chip Access Delay from $\overline{\text{RESET}}$ High	32		MCY

TABLE 10-14. RESET TIMING SPECIFICATION

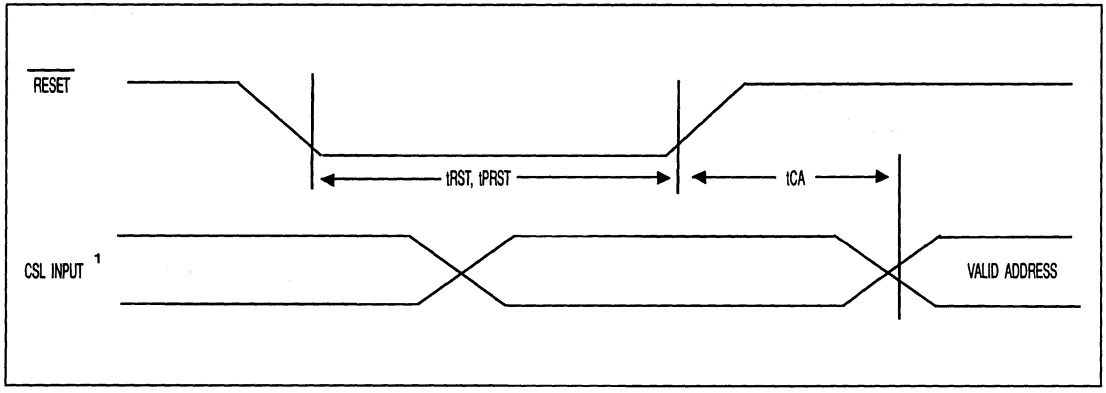

FIGURE 10-14. RESET TIMING DIAGRAM

10.3 IDE INTERFACE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tD7D	Propagation Delay from IDED7 to DB7		20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-15. IDE INTERFACE TIMING (IDED7 TO DB7)

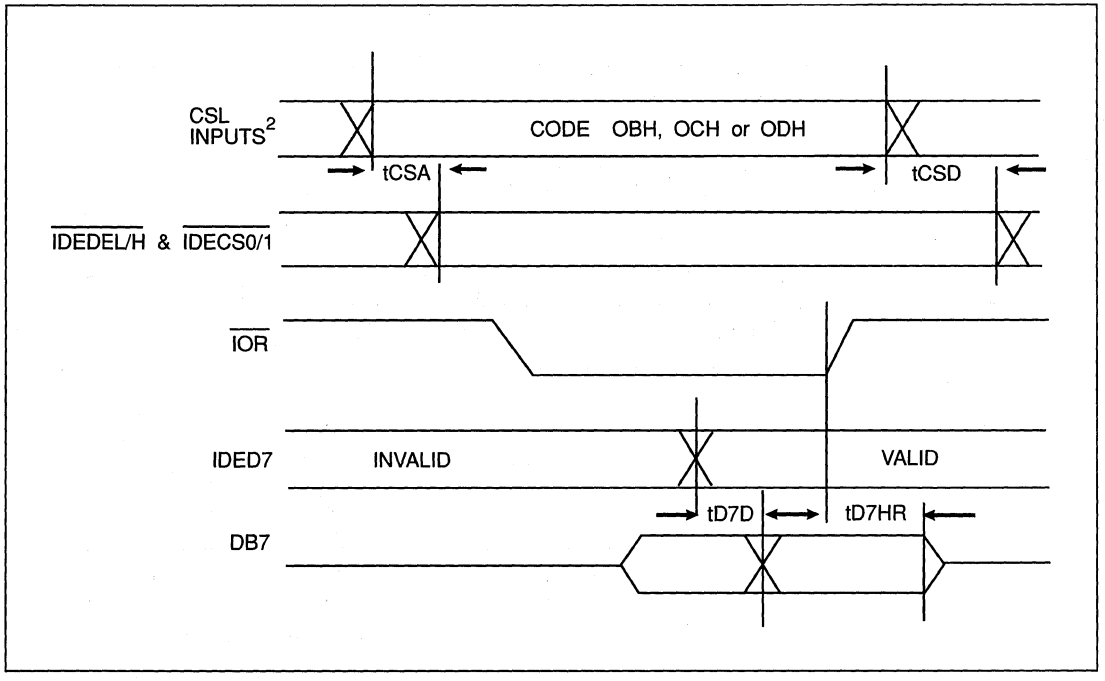

FIGURE 10-15. IDE INTERFACE TIMING DIAGRAM (IDED7 TO DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tD7D	Propagation Delay from IDED7 to DB7		20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-16. IDE INTERFACE W/BALE TIMING (IDED7 TO DB7)

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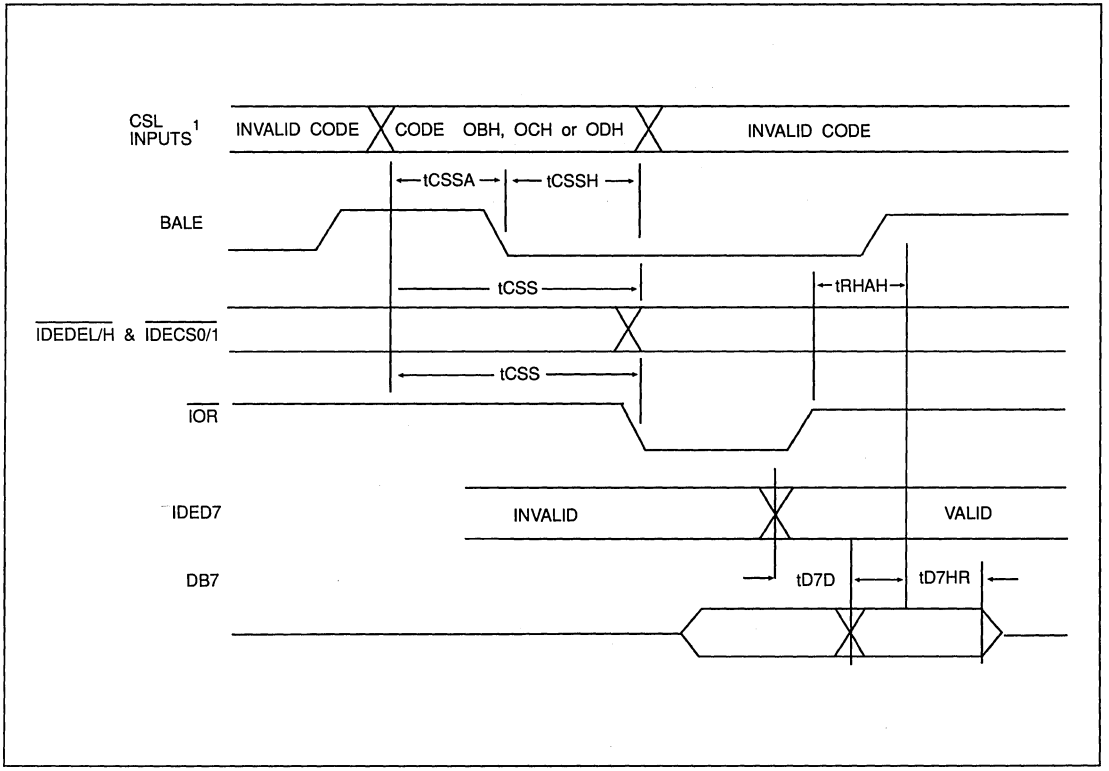

FIGURE 10-16. IDE INTERFACE W/BALE TIMING (IDED7 to DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tIDDR	IDED7 Enable time from $\overline{IOW}$ low		60	ns
tIDD	Propagation Delay from DB7 to IDED7		60	ns
tIDHR	IDED7 to Float Delay to $\overline{IOW}$ high	20	160	ns

TABLE 10-17. IDE INTERFACE TIMING (DB7 TO IDED7)

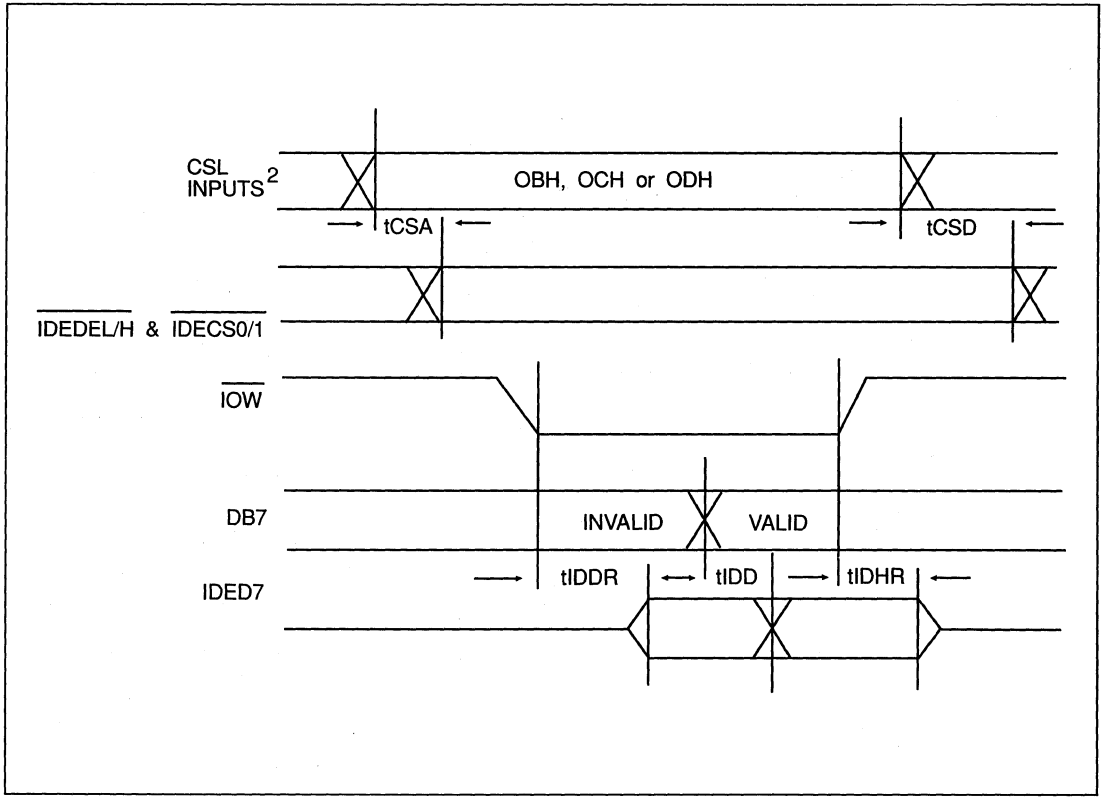

FIGURE 10-17. IDE INTERFACE TIMING (DB7 TO IDED7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time From BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tIDDR	IDED7 Enable time from $\overline{IOW}$ Low		60	ns
tIDHR	IDED7 to Float Delay from $\overline{IOW}$ High	20	160	ns

TABLE 10-18. IDE INTERFACE W/BALE TIMING (DB7 TO IDED7)

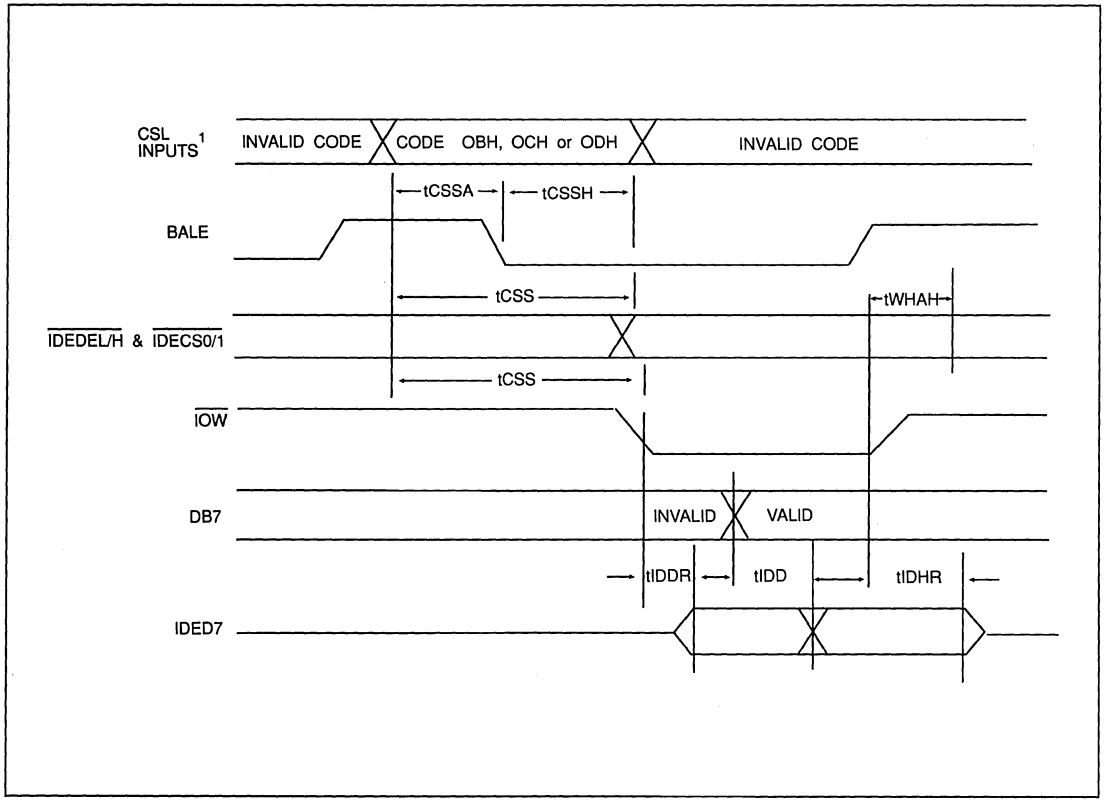

FIGURE 10-18. IDE INTERFACE W/BALE TIMING (DB7 to IDED7)

10.4 SUSPEND/RESUME TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCWSS	CSL Input Valid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tCWSR	CSL Input Invalid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tOSD	OSC Suspend Initiated to OSC Low Gap	60		µS
tOSL	OSC Low Gap	60		µS

TABLE 10-19. RESUME TO SUSPEND SUPPORT TIMING*

*Note: Code 15 can also be latched in with BALE.

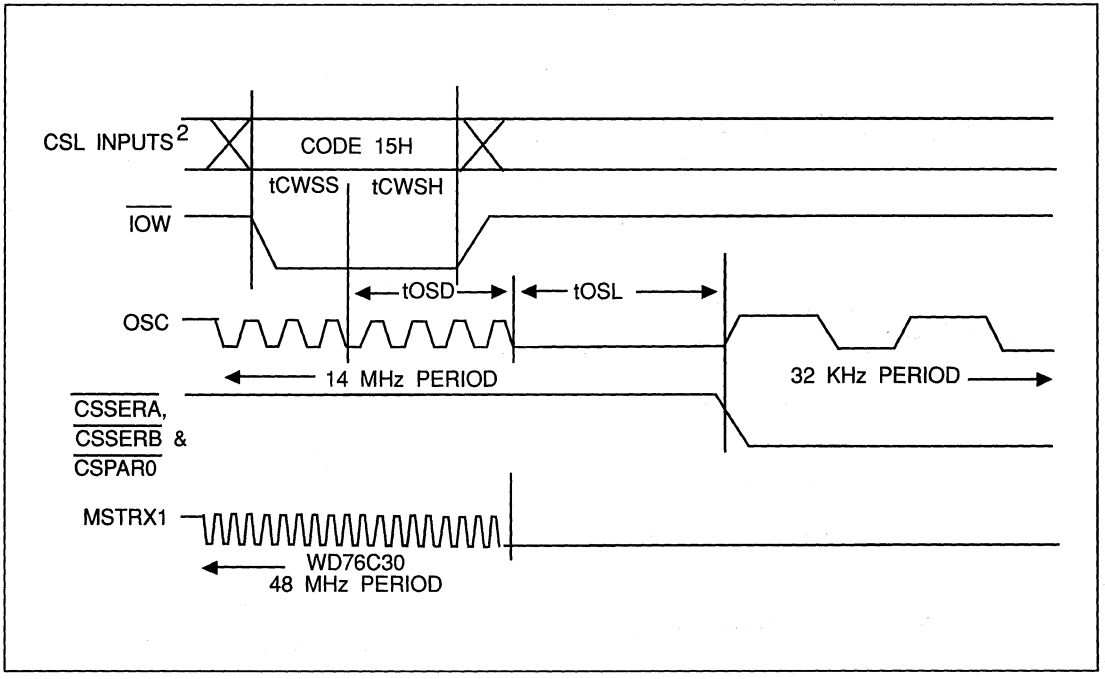

FIGURE 10-19. RESUME TO SUSPEND SUPPORT TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCRS	CSL Input Valid to OSC Transition to Low	30		ns
tCRH	CSL Input Invalid to OSC Transition to Low	30		ns
tCOR	CSL Output De-Assert to Resume WD76C30*	60	91	µS
tOTD	OSC Transition Delay (for XTAL warmup)*	500	501	ms

* CSL Code 16H is latched on the falling edge of OSC.

TABLE 10-20. SUSPEND TO RESUME SUPPORT TIMING

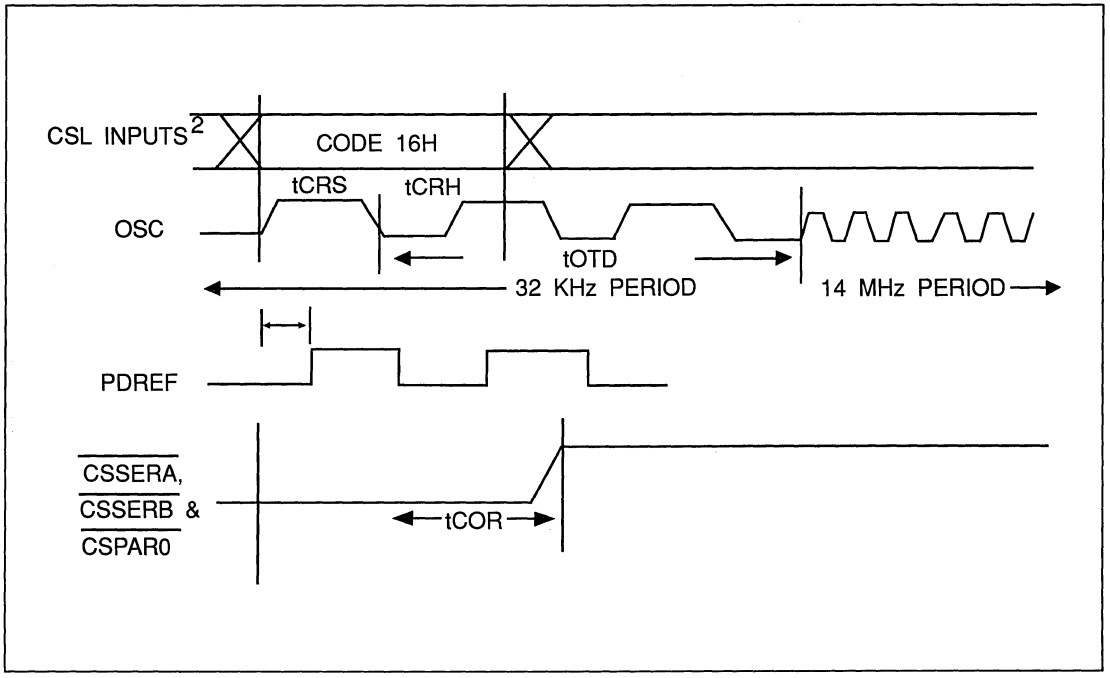

FIGURE 10-20. SUSPEND TO RESUME SUPPORT LOGIC

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input[2] Valid to CSL Asserted		35	ns
tCSD	CSL Input[2] Invalid to CSL Output De-Asserted		35	ns
tCSH	CSL Input Address[2] Hold Time from $\overline{IOW}$ High	10		ns
tWLPH	$\overline{IOW}$ Low to PCUW0/1 High		35	ns
tWHPH	$\overline{IOW}$ High to PCUW0/1 Low		35	ns

TABLE 10-21. CHIP SELECT LOGIC DECODE TIMING SPECIFICATION

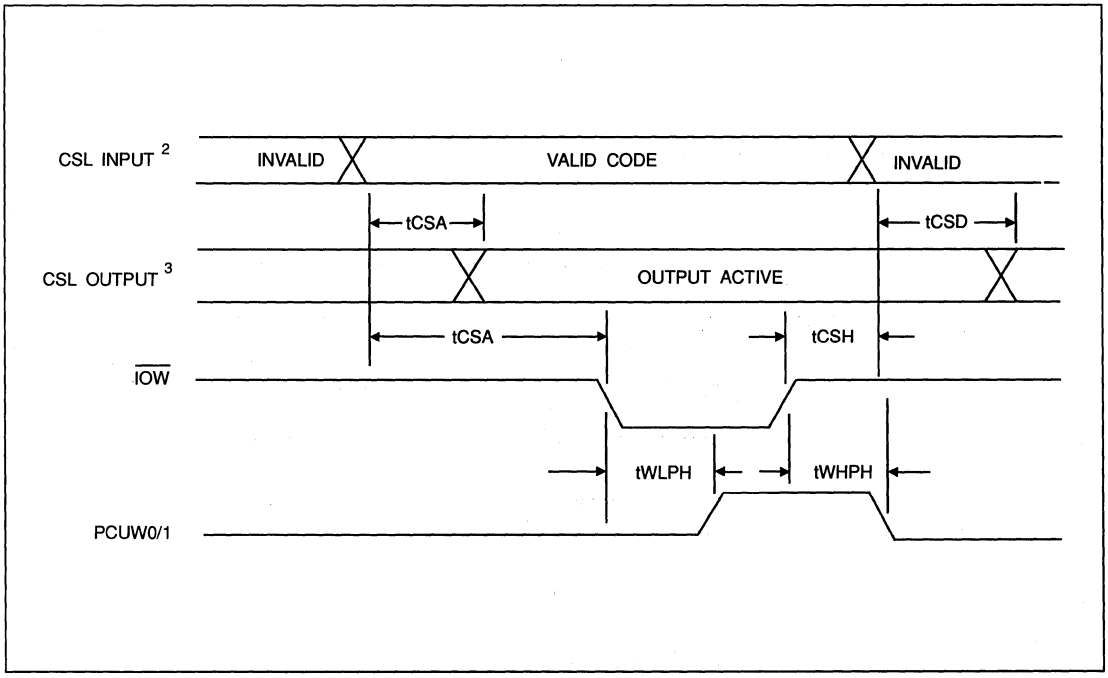

FIGURE 10-21. CHIP SELECT LOGIC DECODE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[2] Set Up to BALE Low	10		ns
tCSSH	CSL Inpu Addresst[2] Hold Time from BALE Low	5		ns
tCSA	CSL Input Valid to Output[3]Asserted	35		ns

TABLE 10-22. CSL DECODE W/BALE TIMING SPECIFICATION

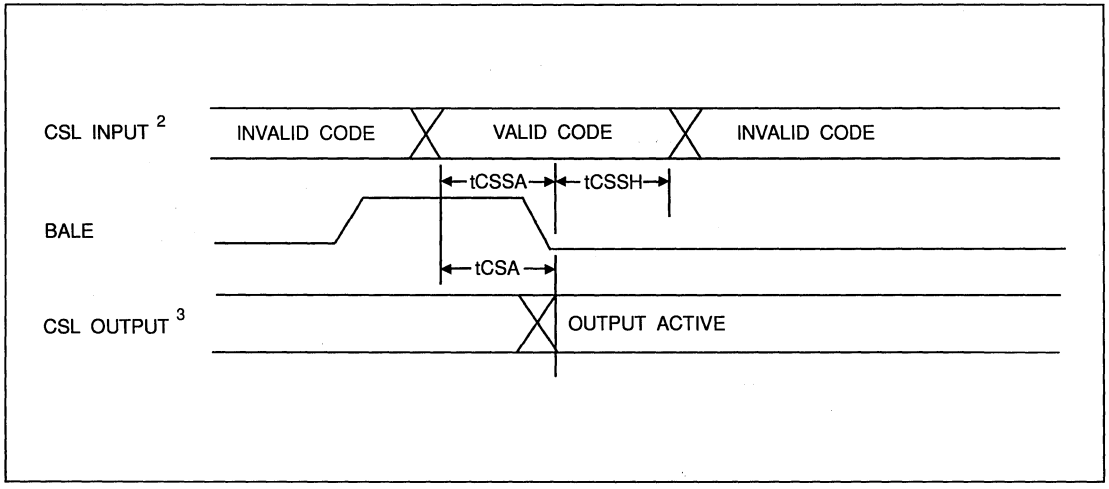

FIGURE 10-22. CHIP SELECT LOGIC DECODE W/BALE TIMING DIAGRAM

Notes

[1] The RTCALE and RTCCS are internal to the WD76C20 and are used by the RTC during I/O operations. The CS, LDCR, and LDOR are also internal to the WD76C20 and used by the FDC during I/O operations. CSL Inputs decoded in Table 4-1 are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal. The general specification for generating the internal and external signals is presented in Tables 10-21 and 10-22.

[2] CSL Inputs are decoded in Table 4-1 and are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal as shown in Figure 10-21 and 10-22. Also included in this group is DACKEN which must be deasserted (logic=0) in order to allow the decoder to activate any signal other than TC, which is asserted (logic=1) when both DACKEN and CSEN are active.

[3] CSL outputs are control lines used both internally by the WD76C20 (FDCCS, FDC LDCR, FDC LDOR, RTC CS, and RTC AEN) and externally by other chips (IDEDENL, IDEDENH, CSIDE0, CSIDE1, CSSERA, CSSERB, CSPAR0, ROMOE, 8042CS, NPCS, PCUW0, PCUW1, PROGCS, EMS and TC). For all but one case, only a single, decoded output is asserted at any given time and is unique as decoded in Table 4-1. Although not mentioned in Table 4-1, TC is asserted when both DACKEN and CSEN are active, as specified in Table 10-6.

11.0 PACKAGE DIMENSIONS

Figure 11-1 shows the 84-pin PLCC package dimension in inches and millimeters.

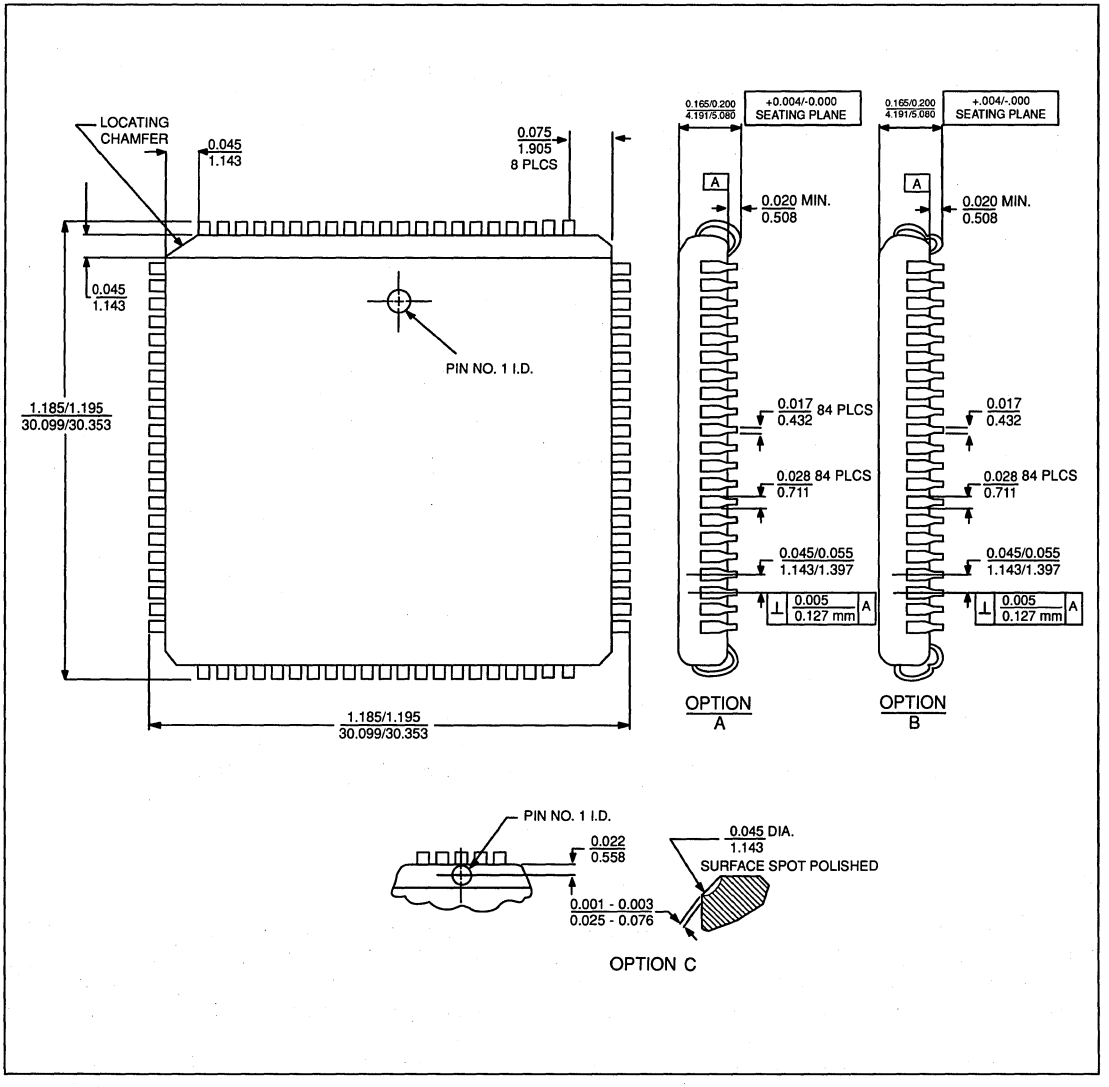

FIGURE 11-1. WD76C20 PACKAGE DIAGRAM (84-PIN PLCC)

Figure 11-2 shows the 84-pin PQFP package dimension in inches and millimeters.

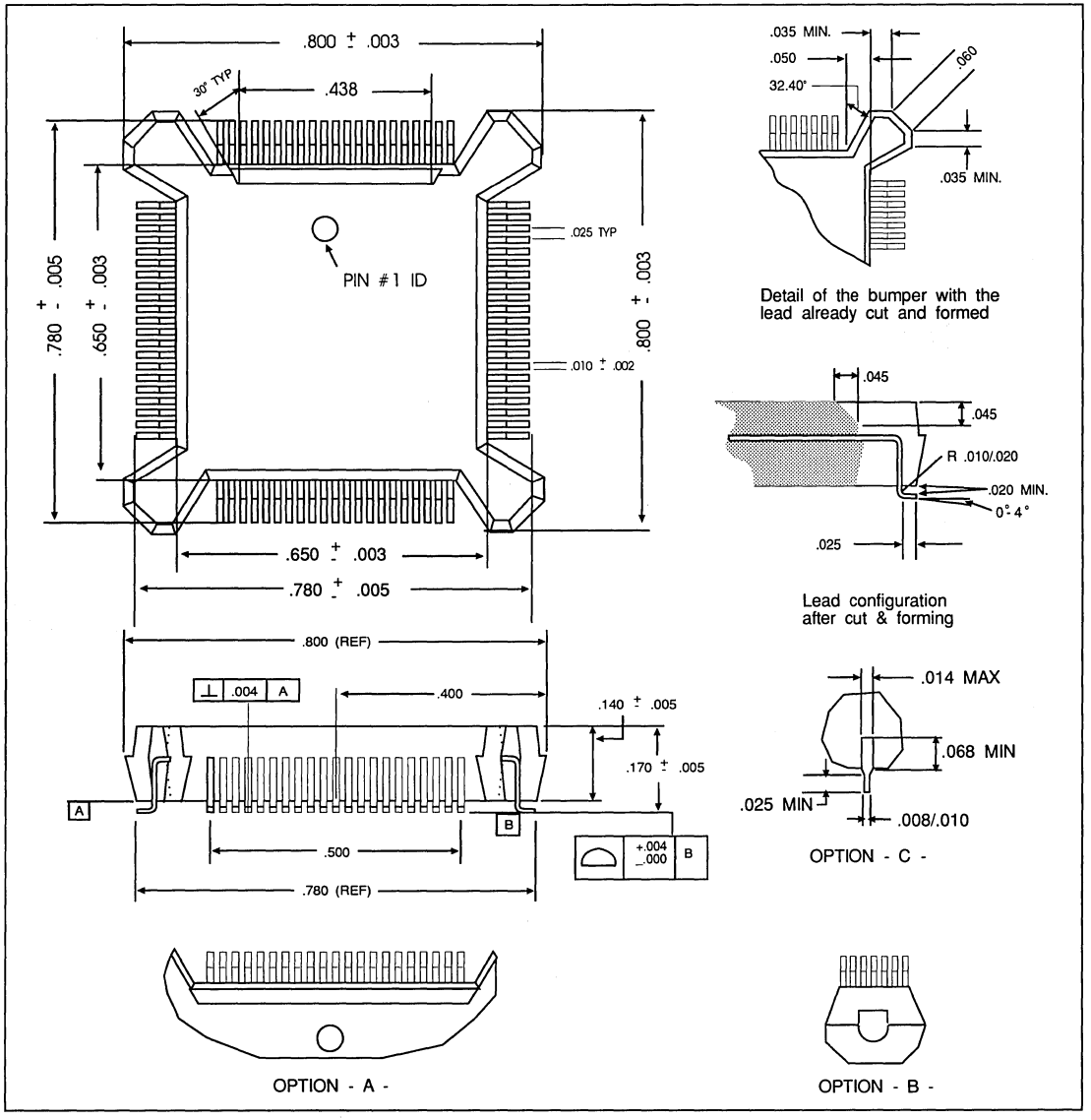

FIGURE 11-2. WD76C20 PACKAGE DIAGRAM (84-PIN PQFP)

A.0 WD76C20LV DEVICE SPECIFICATIONS

A.1 INTRODUCTION

This appendix lists the specifications and describes the operation of the WD76C20LV. This appendix is only preliminary and may later be expanded into a separate document.

A.2 MAXIMUM RATINGS

Absolute maximum ratings; all voltages referenced to Vss.

Storage Temperature	-65°C (-85°F)to 150°C (302°F)
V_{CC}	4.5 volts
Voltage at any pin	-0.1 to 4.50 volts
Lithium Battery	2.4 volts (nominal)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
VCC	+ 3 V Supply	3.0	3.6	V
VBAT	Battery Backup Voltage	2.4	VDD	V
VIL	Input Low Voltage - Data Bus and XTOCS	-0.3	0.8	V
VIH	Input High Voltage - Data Bus and XTOCS	2.0	VCC+.3	V
VILT	Input Low Threshold - Schmitt Trigger	0.8		$V_{typical}$
VIHT	Input High Threshold - Schmitt Trigger		2.0	$V_{typical}$
VHYS	Schmitt Trigger Hysteresis	0.5		$V_{typical}$
VOLAT	Output Low - DBus, FIRQ, DMA: IO=12mA		0.4	V
VOHAT	Output High - DBus, FIRQ, DMA: IO=-5.0mA	2.4		V
VOLHC	Output Low - Drive Interface: IO=48mA		0.4	V
VOL	Output Low - All Others: IO=4mA		0.4	V
VOH	Output High - All Others: IO=400µA	2.4		V
ILUL	Latch Up Current Low	40		mA
ILUH	Latch Up Current High	-40		mA
ILL	Leakage Current Low		10	µA
ILH	Leakage Current High		-10	µA
ICC	Supply Current - 100µA source loads		50	mA
ICC	Supply Current - 5mA source loads		100	mA
ICCPDM1	Supply Current in Power-Down Mode (Option 1)		100	$\mu A_{typical}$
ICCPDM2	Supply Current in Power-Down Mode (Option 2)		1	$mA_{typical}$
ICCPDM3	Supply Current in Chip Set Power-Down Mode		1	mA
ICCBAT	Supply Current in Battery Backup Mode		25	µA
PD	Power Dissipation - ICC max[1]		300	mW
PDHL	Power Dissipation - ICC max[2, 3]		350	mW

TABLE A-1. D.C. CHARACTERISTICS (WD76C20LV)

1 VIN = VCC or GND, IO = 0mA
2 Includes DBx: IO=-5.0 mA source loads
3 Includes open drain high current drivers at VOL = 0.3V

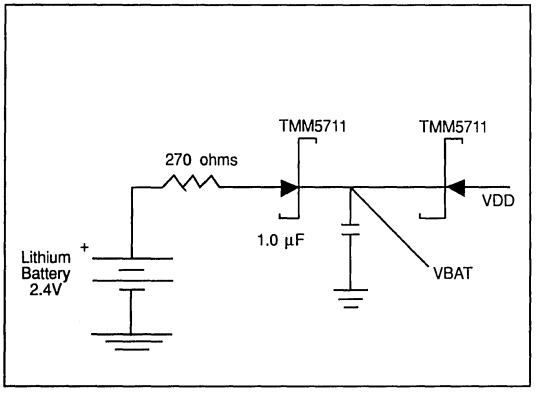

FIGURE A-1. VBAT EXTERNAL SUPPORT

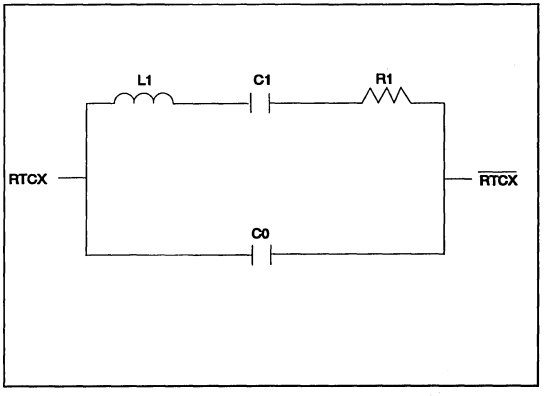

FIGURE A-3. RTC CRYSTAL PARAMETERS

5

A.3 TIME BASE OSCILLATOR CIRCUIT

The oscillator that provides the time base for the RTC requires the external circuit shown in Figure A-1 and the values listed in Table A-2. The crystal used in parallel with the on-chip oscillator should be an AT-cut crystal with a 32.768 KHz resonant frequency as shown in Figure A-2, using signals listed in Table A-2. When in battery backup mode, this circuit is still active, providing the rest of the RTC with a valid time base.

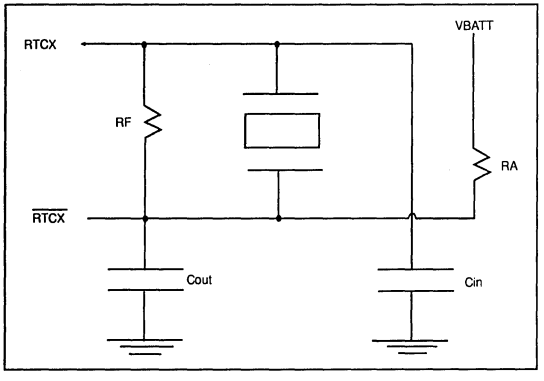

FIGURE A-2. RTC CRYSTAL EXTERNAL CIRCUITRY

A.4 POWER SWITCH

This functional block is used to detect when the system power is shutting down and the RTC needs to go into battery backup mode. In the event of a full chip power-down without a battery backup, the VRT bit of register D will be reset to zero, indicating that the contents of the SRAM and RTC operational registers are not guaranteed. In order to reset the bit, register D must be read after a full power-up.

A.5 BUS INTERFACE

The RTC Bus Interface block is used to access the internal bus for the WD76C20LV. Protocol is maintained between the BIL block (Bus Interface Logic) and the RTC Bus Interface. The BIL block generates the $\overline{RD}$ and $\overline{WR}$ strobes, and the $\overline{CS}$ signals are decoded from the external bus by the Chip Select Logic.

A.6 CLOCK DIVIDER

This functional block uses clock divider logic to split the 32.768 KHz time base down to a 1 Hz signal that can be used by the timekeeping blocks. It also provides the periodic interrupt block with access to all stages of the division.

A.7 CRYSTAL CAPACITANCE

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS
	*RTC CRYSTAL**			
R1	Crystal Motional Resistance		40	K ohm
C0	Crystal Shunt Capacitance		1.7	pF
C1	Crystal Motional Capacitance		0.0035	pF
Q	Crystal Quality Factor	50		K
CI_{IN}	Crystal Circuit Input Capacitance	30	±5%	pF
C_{OUT}	Crystal Output Capacitance	30	±5%	pF
RA	Crystal Circuit Drive Level Resistor	330	±1%	K ohm
RF	Crystal Circuit Feedback Resistor	15	22	M ohm
	16 MHZ CRYSTAL			
Rseries	Crystal Circuit Resistors	30		ohm
Cshunt	Crystal Output	10		pF
C1	Crystal Input Capacitance	47	±5%	pF
C2	Crystal Output Capacitance	15	±5%	pF
	14MHZ CRYSTAL			
Rseries	Crystal Circuit Resistors	30		ohm
Cshunt	Crystal Output	10	±5%	pF
C1	Crystal Input Capacitance	22	±5%	pF
C2	Crystal Output Capacitance	22		pF

TABLE A-2. CRYSTAL CAPACITANCE FOR WD76C20LV

* RTC crystal components specified are valid for crystals with A(CL) load capacitance of 18 pF typical. (CL = 18 pF).

WD76C30/LV

Peripheral Controller, Interrupt Multiplexer, and Clock Generator Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION

1.1 WD76C30/LV FEATURES

- Two fully programmable and independent serial I/O ports configurable as PC/AT compatible (WD16C452) or PS/2 compatible (WD16C552)
  - ° Loopback controls for communications link fault isolation for each ACE
  - ° Line break generation and detection for each ACE
  - ° Complete status reporting capabilities
  - ° Generation and stripping of serial asynchronous data control bits (start, stop, parity)
  - ° Programmable baud rate generator and MODEM control signals for each port
  - ° Programmable baud rate generator input clock
  - ° Optional 16 byte FIFO buffers on both transmit and receive of each port for CPU relief during high speed data transfer
  - ° Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each port
- Parallel port configurable as a fully Centronics or PS/2 compatible, bidirectional parallel port
- Independently programmable parallel port
- Interrupt multiplexing logic
  - ° Selectable multiplexing logic for connecting PC/AT interrupt request lines to the WD76C10 single chip AT controller
- Clock generation circuitry
  - ° 80287 coprocessor clock generation
  - ° WD76C10 and floppy controller clock generation
  - ° 8042 keyboard clock generation
- Built-in testability features
- Hardware or software controllable sleep mode
- CMOS implementation for high speed and low power requirements
- Pulse extension on IRQ inputs
- 84-pin PLCC and PQFP packages

1.2 GENERAL

The WD76C30/LV device provides three functional groups. It is a Peripheral Controller, Interrupt Multiplexer, and Clock Generator.

The low power CMOS WD76C30/LV is a single device solution which provides interrupt multiplexing logic, clock generation, two serial ports, and one bidirectional parallel port.

Interrupt multiplexing logic interfaces the PC/AT interrupt request lines with the WD76C10 Single Chip AT Controller.

Integrated clock generation circuitry uses the 48 MHz input signal to generate the 1.8462, 3.072, and 8.0 MHz clocks used internally for the two serial ports, a 9.6 MHz signal used for the keyboard controller and floppy controller, a programmable duty/frequency clock for the 80287 coprocessor, and a 16 MHz clock for driving the WD76C10 Single Chip AT Controller, and floppy controller.

For low power implementations such as laptops, oscillator disable and sleep modes are available to power down unused logic.

The bidirectional parallel port is software configurable as either a PC/AT or a PS/2 compatible port. The parallel port data lines and open drain printer signals have high current drive capabilities.

Each ACE is programmable as either a WD16C550 or WD16C450 compatible device. Each WD16C550 configured ACE is capable of buffering up to 16 bytes of data upon reception, relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing which is vital in a multitasking environment. Each ACE has a maximum recommended data rate of 512 Kbaud.

1.3 WD76C30/LV DIFFERENCES

Both the WD76C30 and WD76C30LV operate with two power supplies. The WD76C30 logic is powered by a 5.0 volt supply, while the WD76C30LV logic is powered by a 3.3 volt supply. The parallel and serial port interfaces are only supported by the WD76C30.

1.4 PERIPHERAL CONTROLLER

The peripheral controller is functionally equivalent to the WD16C452/552. The mode of operation of the serial ports and parallel port is selectable via the Mode Select Register. Each serial port is configurable as either a FIFO enhanced ACE (WD16C550 compatible) or a standard ACE (WD16C450). The parallel port is configurable as either a PS/2 bidirectional parallel port or a PC/AT compatible parallel port. A detailed description of the Mode Selection Register is described in the parallel port section.

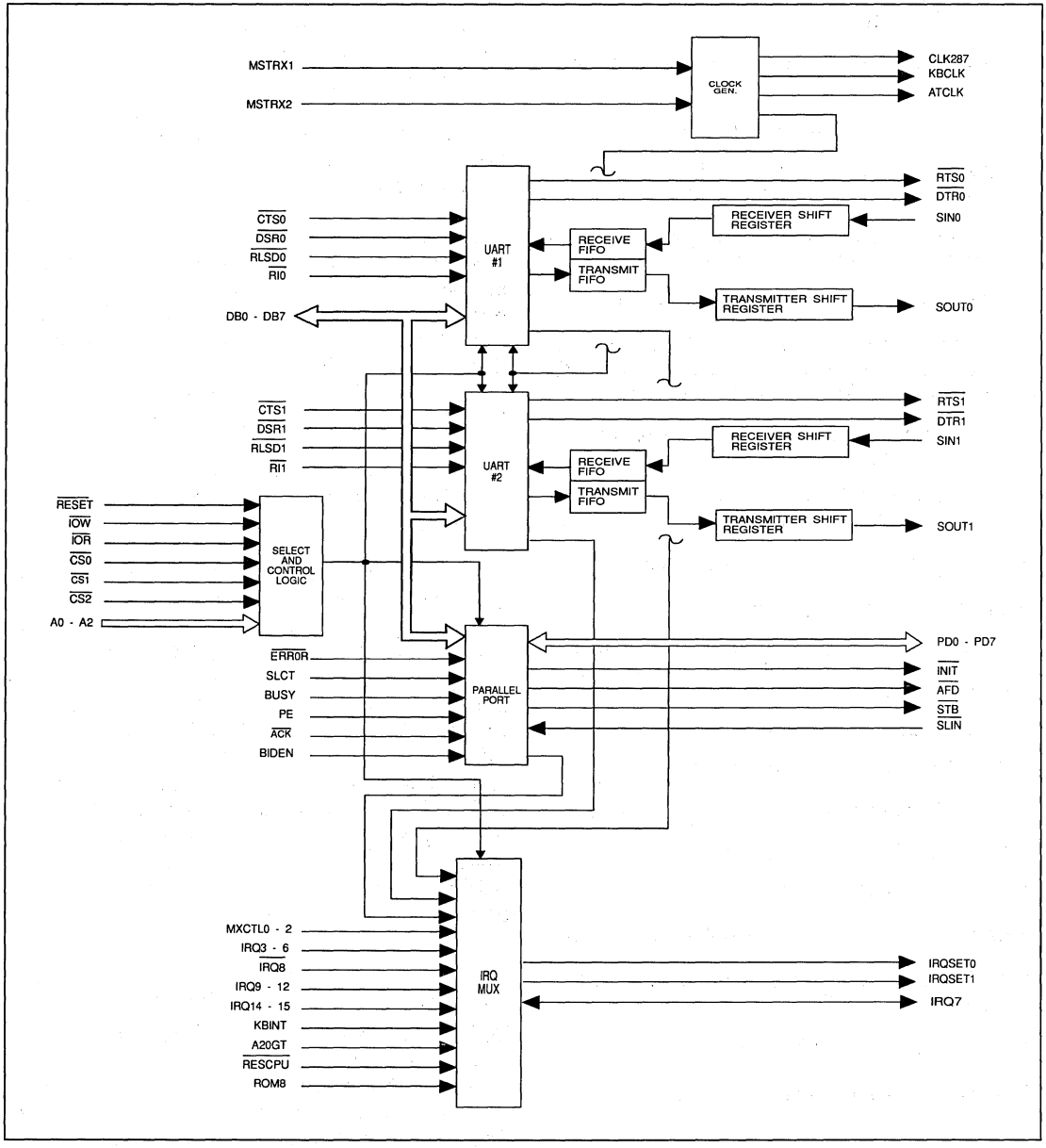

FIGURE 1-1. WD76C30/LV BLOCK DIAGRAM

2.0 PIN DESCRIPTION

Table 2-1 provides a description of the signals serviced by the WD76C30/LV. A drawing of the 84-pin QUAD package, showing the pin and signal locations, is provided in Figure 2-1. The DC operating characteristics and timing are presented in section 6. The DC Operating Charactersitics for the WD76C30LV are presented in the Appendix.

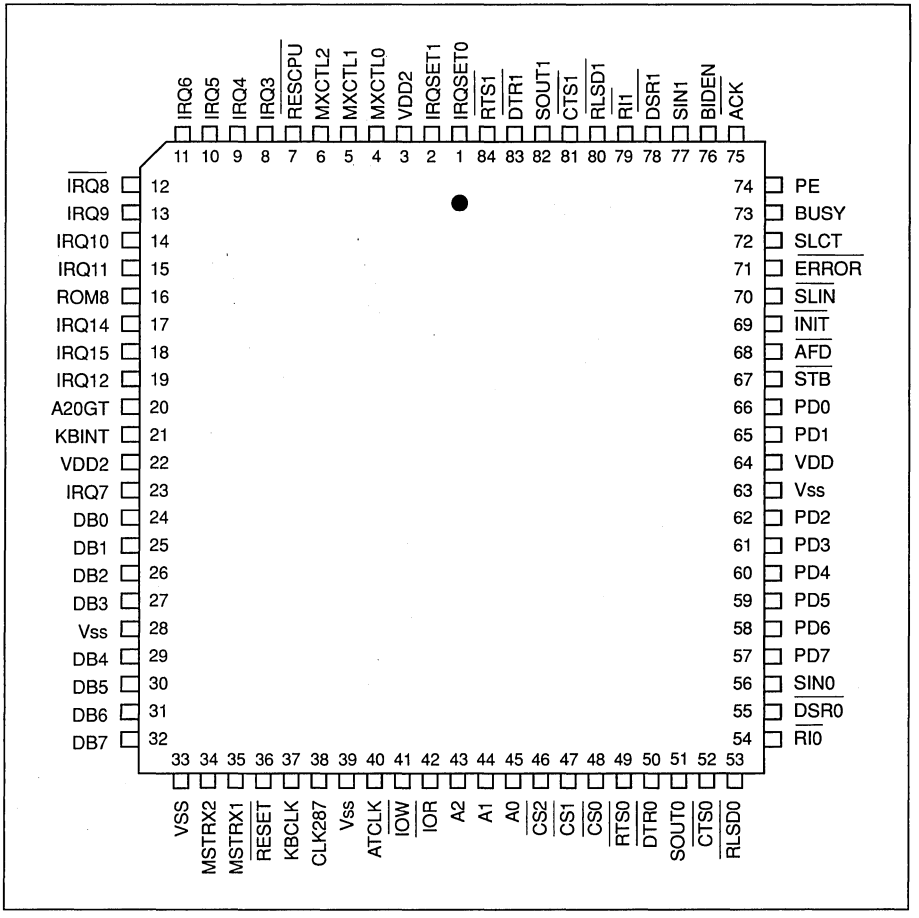

FIGURE 2-1. 84-PIN PLCC - SIGNAL/PIN ASSIGNMENT

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
76	BIDEN	Bidirectional Enable	I	When de-asserted, the BIDEN enables the parallel port data lines as outputs. When asserted, BIDEN works in conjunction with the DIR bit (see Table 4-3) to control the direction of the parallel port data bit.
78, 55	$\overline{DSR1}$, $\overline{DSR0}$	Data Set Ready	I	The communication link asserts these signals to indicate that it is ready to exchange data with the associated Asynchronous Communications Element (ACE). Bit 5 of the associated MODEM Status Register reflects the logical state of $\overline{DSR}$.
79, 54	$\overline{RI1}$, $\overline{RI0}$	Ring Indicator	I	When asserted, these signals indicate that a ringing signal for the associated ACE is being received by the MODEM or data set. This logical value is reflected in bit 6 of the associated MODEM Status Register.
80 53	$\overline{RLSD1}$ $\overline{RLSD0}$	Received Line Signal Detect	I	The Data Circuit-terminating Equipment (DCE) asserts these signals when the associated ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the associated MODEM Status Register reflects this value.
82 51	SOUT1 SOUT0	Serial Data Output	O	SOUT1 is the transmitted Serial Data Output from ACE#1 to the communication link. SOUT0 is the transmitted Serial Data Output from ACE#0 to the communication link. The SOUT signals are set to a marking condition (logical 1) upon a Master Reset.
77, 56	SIN1, SIN0	Serial Data Inputs	I	SIN1 is the received Serial Data Input from the communication link to ACE#1. SIN0 is the received Serial Data Input from the communication link to ACE#0. Data on the serial data inputs are disabled when exercising loop back mode and internally connected to their respective SOUT lines.
83, 50	$\overline{DTR1}$, $\overline{DTR0}$	Data Terminal Ready	O	When asserted, the Data Terminal Ready informs the MODEM or data set that the associated ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
84, 49	$\overline{RTS1}$, $\overline{RTS0}$	Request To Send	O	When asserted, the $\overline{Request\ To\ Send}$ informs the MODEM or data set that the associated ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.

TABLE 2-1. PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
81, 52	CTS1, CTS0	Clear to Send	I	The DCE asserts the Clear To Send to signal the associated ACE that a remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
32 - 29, 27 - 24	DB7 - DB0	Data Bits	I/O	The Data Bits are tri-state, bidirectional communication lines between the WD76C30/LV and Data Bus. DB0 is the least significant bit and the first serial bit to be transmitted or received.
43 - 45	A2, A1, A0	Address lines A2-A0	I	Address Lines A2 - A0 are used to select the registers internal to the WD76C30/LV.
41	IOW	Input/Output Write Strobe	I	When Input/Output Write Strobe is asserted, data is written to the Port's addressed register from the Data Bus (DB7 - DB0). The register is addressed by Address Lines A2 - A0. ACE#0, ACE#1, or the Parallel Port is selected by CS0, CS1, or CS2 respectively.
42	IOR	Input/Output Read Strobe	I	When Input/Output Read Strobe is asserted, data is read from the Port's addressed register and placed on the Data Bus (DB7 - DB0). The register is addressed by Address Lines A2 - A0. ACE#0, ACE#1, or the Parallel Port is selected by CS0, CS1, or CS2 respectively.
48	CS0	Chip Select 0	I	Chip Select 0 when asserted, selects serial port 0.
47	CS1	Chip Select 1	I	Chip Select 1 when asserted, selects serial port 1.
46	CS2	Chip Select 2	I	Chip Select 2 when asserted, enables the parallel port.
36	RESET	Reset	I	When asserted, RESET forces the WD76C30/LV into an idle mode in which all serial data activities are terminated. The IRQ MUX is forced into a non-compatible mode. The WD76C30/LV remains in the idle state until programmed to begin data activities.
57 - 62, 65 - 66	PD7 - PD0	Parallel Data Bits	I/O	Bidirectional data port, providing parallel input and output to the parallel port.

TABLE 2-1. PIN DESCRIPTIONS Cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
67	$\overline{\text{STB}}$ ①	Line Printer Strobe	O	When asserted, the Line Printer Strobe signals the line printer to latch the data currently on the parallel port (PD7 - PD0).
68	$\overline{\text{AFD}}$ ①	Line Printer Autofeed	O	When asserted, the Line Printer Autofeed signals the line printer to autofeed continuous form paper.
69	$\overline{\text{INIT}}$ ①	Line Printer Initialize	O	When asserted, Line Printer Initialize signals the line printer to begin an initialization routine.
70	$\overline{\text{SLIN}}$ ①	Line Printer Select	O	When asserted, Line Printer Select selects the printer.
23	IRQ7/$\overline{\text{IRQ7}}$	Interrupt Request 7	I/O	IRQ7/$\overline{\text{IRQ7}}$ is an input to the IRQ MUX when the WD76C30/LV is not in the Stand Alone Mode. IRQ7/$\overline{\text{IRQ7}}$ is output as the Parallel Port Interrupt when the WD76C30/LV is in the Stand Alone Mode (refer to section 5.6, 5.7). When operating as the Parallel Port Interrupt, IRQ7/$\overline{\text{IRQ7}}$ is a tristate signal and must be enabled by bit 4 in the Write Control Register (refer to section 4.0). When the Parallel Port Interrupt is PC/AT compatible, this signal is IRQ7 and is asserted at the rising edge of $\overline{\text{ACK}}$ and de-asserted at the falling edge of $\overline{\text{ACK}}$. When the Parallel Port is PS/2 compatible, this signal is $\overline{\text{IRQ7}}$ and is asserted at the rising edge of $\overline{\text{ACK}}$ and de-asserted at the rising edge of $\overline{\text{IOR}}$, when reading the Parallel Port Status Register.
71	$\overline{\text{ERROR}}$	Line Printer Error	I	The printer asserts this signal to inform the parallel port of a deselect condition, PE, or other error condition.
72	SLCT	Line Printer Select	I	The line printer asserts the Line Printer Select signal when it has been selected.
73	BUSY	Line Printer Busy	I	The line printer asserts the Line Printer Busy signal when it has an operation in progress.
74	PE	Line Printer Paper Empty	I	The line printer asserts the Line Printer Paper Empty signal when it is out of paper.

① These outputs are open drain with internal pull-ups.

TABLE 2-1. PIN DECSRIPTION Cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
75	$\overline{\text{ACK}}$	$\overline{\text{Line Printer}}$ Acknowledge	I	The line printer asserts the $\overline{\text{Line}}$ $\overline{\text{Printer}}$ $\overline{\text{Ac-}}$ knowledge signal to confirm that the data transfer from the WD76C30/LV to the printer was successful.
4 - 6	MXCTL0 - MXCTL2	IRQ MUX Control	I	MXCTL0 - MXCTL2 are encoded select signals generated by the WD76C10 for sampling the IRQ inputs.
8 - 15, 17-19	$\overline{\text{IRQ3}}$ - 6 $\overline{\text{IRQ8}}$ IRQ9-11 IRQ14, 15, 12	IRQ MUX Inputs	I	These 11 interrupt signals, along with $\overline{\text{IRQ7}}$, $\overline{\text{RESCPU}}$, ROM8, KBINT, and A20GT are multiplexed into IRQSET0 and IRQSET1 at a period rate defined by MXCTL0 - MXCTL2.
7	$\overline{\text{RESCPU}}$	$\overline{\text{Reset}}$ $\overline{\text{CPU}}$	I	The keyboard controller asserts $\overline{\text{Reset}}$ $\overline{\text{CPU}}$ when the CPU should be reset.
16	ROM8	8-bit ROM	I	ROM8 is multiplexed into the IRQSET1 signal and, when asserted, indicates to the WD76C10 that the system ROM is eight bits, when de-asserted it is 16 bits.
21	KBINT	Keyboard Interrupt	I	KBINT is multiplexed into the IRQSET1 signal and indicates to the WD76C10 that a keyboard interrupt is pending.
20	A20GT	Address 20 Signal	I	A20GT is multiplexed into the IRQSET1 signal and reflects the state of the address 20 signal. This allows compatibility with the 8086 and 80286 processors when addressing memory in the 64 Kbyte boundary above 1 Mbyte.
35	MSTRX1 ①	Master Clock 1	I	The Master Clock 1 signal can be driven by either a 16 MHz crystal or 48 MHz TTL oscillator.
34	MSTRX2 ①	Master Clock 2	O	Master Clock 2 is connected to the 16 MHz crystal to generate Master Clock 1 for the clock generation circuitry. This pin is left disconnected if Master Clock 1 is being driven by a 48 MHz TTL oscillator.
38	CLK287	80287 Clock	O	CLK287 clock drives the 80287 coprocessor. CLK287 is programmable via the Clock Selection Register. A variety of clock frequencies and duty cycles provide compatibility with a variety of 80287 or 80287 compatible coprocessors.

① Third overtone of 16 MHz crystal is used to generate the 48 MHz clock.

TABLE 2-1. PIN DESCRIPTION Cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
37	KBCLK	Keyboard Clock	O	Keyboard Clock is a 9.6 MHz clock used to drive the keyboard controller. This signal can be used to drive the WD37C65 Floppy Disk Controller for systems not using the WD76C20 Storage Controller.
40	ATCLK	AT Clock	O	AT Clock is a 16 MHz clock used to drive the ATCLK input to the WD76C10. AT Clock provides a fixed reference that allows the PC/AT bus state machine to run with 8 MHz compatible timing. This signal can be used to drive the Floppy Disk Controller in the WD76C20 Storage Controller.
1 2	IRQSET0 IRQSET1	Interrupt Request Set 0, 1	O	These signals are outputs of the IRQ multiplexing logic. When in the Stand Alone Mode IRQSET0 and IRQSET1 become the tristate interrupt outputs from Serial Port 0 and 1 respectively. (Refer to section 5.6)
64	V_{DD}	Power Supply		WD76C30, +5V power supply to the serial and parallel port logic. This supply can be turned off. WD76C30LV, +3.3 power supply to the serial and parallel port logic. This supply can be turned off.
3, 22	$V_{DD}2$	Power Supply		+5V power supply to the WD76C30, excluding the serial and parallel ports. +3.3V power supply to the WD76C30LV, excluding the serial and parallel ports.
28, 39, 63, 33	Vss	Ground		System signal ground.

TABLE 2-1. PIN DESCRIPTION Cont.

3.0 SERIAL PORT REGISTERS

The WD76C30/LV contains two serial ports, therefore, the following registers exist in duplicate, one per port.

3.1 SERIAL PORT REGISTER ADDRESSING

3.1.1 Chip Select ($\overline{CS0}$, $\overline{CS1}$)

When $\overline{CS0}$ is low, registers for serial port 0 can be accessed, and when $\overline{CS1}$ is low, registers for serial port 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$, or $\overline{CS2}$) should ever be low at any time, unless all three are low for Sleep Mode.

Power Down Reset:
In the Parallel Port, asserting Mode Selection Register bit 3 (PUD) described in section 5.5, causes the ACE to reset to the condition listed in Table 3-2.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an idle mode. Registers are not reset by this operation. Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data, returning them to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

3.1.2 Register Select (A0, A1, A2)

To select a register for read or write operation, see Table 3-1.

NOTE
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read)
0	0	0	0	Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read)
X	0	1	0	FIFO Control Register (write)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING

3.2 ACE OPERATIONAL DESCRIPTION

3.2.1 Master Reset

Asserting $\overline{\text{RESET}}$ on pin 36 causes the ACE to reset to the condition listed in Table 3-2.

3.2.2 ACE Accessible Registers

The system programmer has access to any of the registers as summarized in Table 3-3. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset or PUD = 1	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset or PUD = 1	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset or PUD = 1	All Bits Low
MODEM Control Register	Master Reset or PUD = 1	All Bits Low
Line Status Register	Master Reset or PUD = 1	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset or PUD = 1 MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
$\overline{\text{SOUT}}$	Master Reset or PUD = 1	High
$\overline{\text{RTS}}$	Master Reset or PUD = 1	High
$\overline{\text{DTR}}$	Master Reset or PUD = 1	High
RCVR FIFO Counter	MR or FCR1• FCR0 or ΔFCR0 or PUD = 1	All Bits Low
XMIT FIFO Counter	MR or FCR2 • FCR0 or ΔFCR0 or PUD = 1	All Bits Low
FIFO CONTROL	Master Reset or PUD = 1	All Bits Low
D7 - D0 Data Bus Lines	In Tristate Mode, Unless $\overline{\text{IOR}}$ = Low	Tri-State Data (ACE to CPU)
Address Selection Register	Master Reset	All Bits Low
Clock Selection Register	Master Reset	All Bits Low
CLK Disable Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Parallel Port Interrupt Selection Register	Master Reset	All Bits Low
Mode Selection Register	Master Reset	All Bits Low
Parallel Port Control	Master Reset or PUD = 1	Bits 7 - 6 High, Bits 5 - 0 Low
Parallel Port Data	Master Reset or PUD = 1	All Bits Low
Parallel Port Status	None	
$\overline{\text{SLIN}}$, $\overline{\text{INIT}}$, $\overline{\text{AFD}}$, $\overline{\text{STB}}$,	Master Reset or PUD = 1	High, Low, High, High

* Reset disables the Stand Alone Mode *
PUD is bit 3 of the Mode Selection Register

TABLE 3-2. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

	REGISTER ADDRESS ②					
	DLAB = 0 A2-A0 = 0 Read Only	DLAB = 0 A2-A0 = 0 Write Only	DLAB = 0 A2-A0 = 1	DLAB = X A2-A0 = 2 Read Only	DLAB = X A2 - A0 = 2 Write Only	DLAB = X A2 - A0 = 3
	REGISTER TITLE					
Bit No.	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Identification Register	FIFO Control Register	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IID)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IID)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IID) ①	Not Used	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (LSB)(RFTL)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (MSB) (RFTL)	Divisor Latch Access Bit (DLAB)

① These bits are 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30 SERIAL PORT REGISTERS

	REGISTER ADDRESS ②					
	DLAB = X A2-A0 = 4	DLAB = X A2-A0 = 5	DLAB = X A2-A0 = 6	DLAB = X A2-A0 = 7	DLAB = 1 A2-A0 = 0	DLAB = 1 A2-A0 = 1
	REGISTER TITLE					
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO ① (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

① Thls bit is 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30 SERIAL PORT REGISTERS (Cont.)

3.3 LINE CONTROL REGISTER

The Line Control Register provides control over the word length, number of Stop Bits, Parity, Break Control and selection of the Receiver Buffer, Transmitter Holding Register and Interrupt Enable Register.

Address A2-A0 = 3, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
DLAB	SBR	STP	EPS	PEN	STB	WLS1	WLS0

Signal Name	Default After Master Reset
All signals	0

Bit 7 - DLAB, Divisor Latch Access

DLAB = 0 -
Access the Receiver Buffer, Transmitter Holding Register or Interrupt Enable Register.

DLAB = 1 -
Access the Divisor Latches of the Baud Rate Generator during a Read or Write operation.

Bit 6 - SBR, Set Break Control

The SBR feature enables the CPU to alert a terminal in a computer communications system.

SBR = 0 -
Serial Output (SOUT) follows the output of the transmitter.

SBR = 1 -
The Serial Output (SOUT) is forced to the Spacing (logic 0) State and remains there (until reset by a low-level SBR), regardless of other transmitter activity.

Bit 5 - STP, Stick Parity

STP = 0 -
When parity is enabled by PEN (bit 3), it is represented as indicated by the state of EPS (bit 4).

STP = 1 -
When parity is enabled by PEN, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by EPS.

Bit 4 - EPS, Even Parity Select

EPS = 0 -
When PEN (bit 3) equals 1 and STP equals 0, an odd number of logic 1's are transmitted or checked in the data word bits and Parity bit.

EPS = 1 -
When PEN equals 1 and STP equals 0, an even number of bits are transmitted or checked.

Bit 3 - PEN, Parity Enable

PEN = 0 -
No parity is generated or checked.

PEN = 1 -
Parity is generated on transmitted data or checked on received data between the last data word bit and Stop bit of the serial data. The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.

Bit 2 - STB, Number Of Stop Bits

This bit specifies the number of Stop Bits in each transmitted serial character.

STB = 0 -
One Stop Bit is generated in the transmit data.

STB = 1 -
When WLS1 and WLS0 (bits 1 and 0) select a 5-bit word length, 1-1/2 Stop bits are generated.

When WLS1 and WLS0 select a 6, 7 or 8-bit word length, two Stop bits are generated.

Bits 1, 0 - WLS1, WLS0, Word Length Select

WLS1 and WLS0 specify the number of bits in each transmitted or received serial character.

WLS1	WLS0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator with a programmable input clock of 1.843 MHz, 3.0 MHz or 8 MHz clocks, as well as a 48 MHz input for test purposes. The output frequency of the Baud Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load. Loading of either divisor Latch forces the Transmitter and Receiver into the Idle Mode. The transmitter does not enter the Idle Mode until after the character in the shift register has been transmitted.

Tables 3-3, 3-4 and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock, another is a 3.072 MHz clock and the third is an 8.0 MHz clock.

NOTE

The maximum operating frequency of the Baud Rate Generator is 8.0 MHz.

The data rate should never be greater than 512 Kbaud.

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

TABLE 3-4. BAUD RATES USING 1.8432 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—

TABLE 3-5. BAUD RATES USING 3.072 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 3-6. BAUD RATE USING 8.0 MHz CLOCK

3.5 LINE STATUS REGISTER

The Line Status Register provides status information to the CPU concerning the data transfer.

Address A2-A0 = 5, DLAB = X - Read

7	6	5	4	3	2	1	0
EIRF	TEMT	THRE	BI	FE	PE	OE	DR

Signal Name	Default After Master Reset
EIRF	0
TEMT	1
THRE	1
BI	0
FE	0
PE	0
OE	0
DR	0

Bit 7 - EIRF, Error in RCVR FIFO

EIRF = 0 -
When in Character Mode, EIRF is always 0.

When in FIFO Mode, a 0 indicates no error in the RCVR.

EIRF = 1 -
There is at least one parity error, framing error or break indication in the FIFO. EIRF is set to 0 when the Line Status Register is read and there are no additional errors in the FIFO.

Bit 6 - TEMT, Transmitter Empty

TEMT = 0 -
When in the Character Mode, at least one byte has been written into the Transmitter Holding Register.

When in the FIFO Mode, at least one byte has been written into the XMIT FIFO.

TEMT = 1 -
When in the Character Mode, the Transmitter Holding Register and Transmitter Shift Register are idle (empty).

In the FIFO Mode, the XMIT FIFO and XMIT Shift Registers are empty.

Bit 5 - THRE, Transmitter Holding Register Empty

Character Mode:

THRE indicates that the ACE is ready to accept a new character for transmission. THRE also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty interrupt enable is set high.

THRE = 0 -
The CPU has loaded the Transmitter Holding Register.

THRE = 1 -
A character has been transferred from the Transmitter Holding Register into the Transmitter Shift Register.

FIFO Mode:

Normally

THRE responds immediately when the XMIT FIFO is emptied or when the first character is written into the XMIT FIFO.

The first transmitter interrupt after changing the first bit of FIFO Control Register will be immediate if the Transmit Holding Register Interrupt is enabled.

Exception

The Transmitter FIFO empty indications are delayed one character time, minus the last Stop Bit time, whenever the Transmitter FIFO is empty and there have not been at least two characters in Transmitter FIFO at the same time since the last time that Transmitter FIFO was empty.

THRE = 0 -
At least one character has been written into the XMIT FIFO.

THRE = 1 -
The XMIT FIFO is empty.

Bit 4 - BI, Break Interrupt

BI indicates that the received character is a Break.

BI = 0 -
The CPU read the contents of the Line Status Register. Restarting after a break is received requires the SIN pin to be high for at least one half bit time.

BI = 1 -

When in the Character Mode, the received data input has been held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and is set when the associated character is in the top of the FIFO.

Bit 3 - FE, Framing Error

FE indicates that the received character did not have a valid Stop Bit.

FE = 0 -

The CPU read the contents of the Line Status Register.

FE = 1 -

In the Character Mode, the Stop Bit following the last data bit or parity bit was detected as a zero bit (Spacing Level).

In the FIFO Mode, an FE is associated with a particular character in the FIFO and is set when the associated character is at the top of the FIFO.

Bit 2 - PE, Parity Error

PE indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit.

PE = 0 -

The CPU read the contents of the Line Status Register.

PE = 1 -

In the Character Mode, a parity error has been detected.

In the FIFO Mode, a parity error is associated with a particular character in the FIFO, and PE is set when the associated character is at the top of the FIFO.

Bit 1 - OE, Overrun Error

OE indicates that an Overrun Error occurred.

OE = 0 -

The CPU read the contents of the Line Status Register.

OE = 1 -

In the Character Mode, the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register. This destroyed the previous character.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the Receiver Shift Register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over but nothing will be transferred to the FIFO.

Bit 0 - DR, Receiver Data Ready

DR = 0 -

In the Character Mode, the CPU read the data in the Receiver Buffer Register.

In the FIFO Mode, the receiver FIFO is empty.

DR = 1 -

In the Character Mode, a complete incoming character has been received and transferred into the Receiver Buffer Register.

In the FIFO Mode, a complete incoming character has been received and transferred into the RCVR FIFO.

NOTE

Bits 4 through 1 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits of the Line Status Register, except bit 7, can be set or reset by writing to the register.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing with all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. Listed according to their priority the four levels of interrupt conditions are:

Receiver Line Status
Received Data Ready
Transmitter Holding Register Empty
MODEM Status

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (IIR).

The IIR, when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Bits 3-0 are further described in Table 3-7.

Address A2-A0 = 2, DLAB = X - Read only

7	6	5	4	3	2	1	0
FERO		0	0	IID			$\overline{IP}$

Signal Name	Default After Master Reset
FERO	00
IID	000
$\overline{IP}$	1

Bits 7, 6 - FERO, FIFO Enable

The FERO bits identify whether the FIFO Control Register bit 0, has placed the device in the Character Mode or FIFO Mode.

FERO = 0 0 -
The device is in the Character Mode

FERO = 1 1 -
The device is in the FIFO Mode.

Bits 5, 4 - These bits are always logic 0.

Bits 3-1 - IID, Interrupt ID

The IID bits identify the highest priority interrupt pending (see Table 3-7).

Bit 0 - $\overline{IP}$, Interrupt Pending

The $\overline{IP}$ bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending.

$\overline{IP}$ = 0 -
An interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

$\overline{IP}$ = 1 -
No interrupt is pending and polling (if used) continues.

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
IID Bit 3	IID Bit 2	IID Bit 1	$\overline{IP}$ Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register or FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 3-7. INTERRUPT CONTROL FUNCTIONS

3.7 INTERRUPT ENABLE REGISTER

When INT (bit 3 of Modem Control Register) is a logic 1, the Interrupt Enable Register controls the selection of the four interrupt sources of the ACE, making it possible to separately activate the device's internal Interrupt signals.

It is possible to disable the entire interrupt system, or selected interrupts by configuring bits three though zero of the Interrupt Enable Register.

Disabling the interrupt system inhibits the Interrupt Identification Register and the active internal interrupt signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Address A2-A0 = 1, DLAB = 0 - Read and Write

7	6	5	4	3	2	1	0
0	0	0	0	EDSSI	ERLSI	ETBEI	ERBFI

Signal Name	Default After Master Reset
All signals	0

Bits 7-4 - These four bits are always set to 0 by the hardware.

Bit 3 - EDSSI, Enable MODEM Status Interrupt

EDSSI = 0 -
Disables the MODEM Status Interrupt.

EDSSI = 1 -
Enables the MODEM Status Interrupt.

Bit 2 - ERLSI, Enable Receiver Line Status Interrupt

ERLSI = 0 -
Disables the Receiver Line Status Interrupt.

ERLSI = 1 -
Enables the Receiver Line Status Interrupt.

Bit 1 - ETBEI, Enable Transmitter Holding Register Empty Interrupt

ETBEI = 0 -
Disables the Transmitter Holding Register Empty Interrupt.

ETBEI = 1 -
Enables the Transmitter Holding Register Empty Interrupt.

Bit 0 - ERBFI, Enable Received Data Available Interrupt

ERBFI = 0 -
Disables the Received Data Available Interrupt.

ERBFI = 1 -
Enables the Received Data Available Interrupt.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It can be used by the programmer as a general purpose register.

Address A2-A0 = 7, DLAB = X - Read and Write

7	6	5	4	3	2	1	0

Signal Name	Default After Master Reset
All signals	None

3.9 FIFO CONTROL REGISTER

The FIFO Control Register is used to enable the FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels and select the mode of DMA signaling.

Address A2-A0 = 2, DLAB = X, Write only

7	6	5	4	3	2	1	0
RFTL		Reserved		Not Used	TFR	RFR	FEWO

Signal Name	Default After Master Reset
All signals	0

Bits 7, 6 - RFTL, RCVR FIFO Trigger Level

RFTL controls the trigger level of the Received Data Available Interrupt.

RFTL

7	6	Trigger Level (bytes)
0	0	- 01
0	1	- 04
1	0	- 08
1	1	- 14

Bits 5, 4 - Reserved for future use and should be programmed to zeros.

Bit 3 - Not Used

In the WD16C550 this is the DMS bit.

Bit 2 - TFR, Transmitter FIFO Reset

Writing a one to TFR clears all characters from the XMIT Error FIFO and resets its counters and this bit to 0. The shift register and XMIT FIFO are not cleared.

Bit 1 - RFR, Reciver FIFO Reset

Writing a one to RFR clears all characters from the RCVR Error FIFO and resets its counters and this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 0 - FEWO, FIFO Enable

FEWO = 0 -
XMIT and RCVR FIFOs are disabled

FEWO = 1 -
XMIT and RCVR FIFOs are enabled. When changing from Character Mode to FIFO Mode, data in the FIFOs does not automatically clear. Setting or resetting FEWO clears all characters from the RCVR Error FIFO and resets the XMIT and RCVR FIFO counters to 0. FEWO must be set to 1 before setting TFR and RFR or they will not be programmed. As illustrated by the following boolean equation, FEWO along with SP_FIFO in the Mode Selection Register determine whether the Character Mode or FIFO Mode is selected.

Character Mode = $\overline{FEWO} + \overline{SP\_FIFO}$
FIFO Mode = FEWO • SP_FIFO

3.10 MODEM CONTROL REGISTER

The MODEM Control Register controls the interface with the MODEM, data set or a peripheral device emulating a MODEM.

Address A2-A0 = 4, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
0	0	0	LOOP	INT	NC	RTS	DTR

Signal Name	Default After Master Reset
All signals	0

Bits 7-5 - These three bits are always set to 0 by the hardware.

Bit 4 - LOOP, Loopback Mode

This bit provides a loopback feature for diagnostic testing of the ACE. Selecting the Loopback Mode results in the following setup (Refer to Figure 3-1):

- The transmitter Serial Output (SOUT) is set to a logic 1 (high) state.
- The receiver Serial Input (SIN) is disconnected.
- The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.

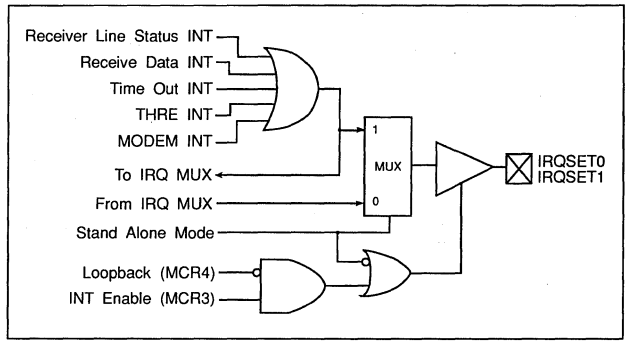

FIGURE 3-1. INTERRUPT SIGNAL LOGIC

- The four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$ and $\overline{RI}$) are disconnected, and the MODEM Control Register bits 3-0 are internally connected to the four MODEM Control inputs.

While in the Stand Alone and Loopback Mode, the IRQSET outputs are tristated (see Figure 3-1). In the Loopback Mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the ACE.

In the Loopback Mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register.

To return to normal operation, the registers must be reprogrammed for normal operation and then LOOP (bit 4) reset to a logic 0.

LOOP = 0 -
Normal Mode.

LOOP = 1 -
Loopback Mode.

Bit 3 - INT, Interrupt

INT enables the IRQSET output when in the Stand Alone Mode. In Loopback Mode this bit is connected internally to bit 7 of the MODEM Status Register (Refer to Figure 3-1).

INT = 0 -
The IRQSET output is tri-stated.

INT = 1 -
The IRQSET output is enabled in the Stand Alone Mode.

Bit 2 - NC, No external connection.

In the Loopback Mode, this bit is connected internally to bit 6 of the MODEM Status Register.

Bit 1 - RTS, Request To Send

Bit 1 controls the $\overline{RTS}$ signal. In the Loopback Mode, this bit is connected internally to bit 4 of the MODEM Status Register.

RTS = 0 -
$\overline{RTS}$ is set to a logic one.

RTS = 1 -
$\overline{RTS}$ is set to a logic zero.

Bit 0 - DTR, Data Terminal Ready

Bit 0 controls the $\overline{DTR}$ signal. In the Loopback Mode, this bit is connected internally to bit 5 of the MODEM Status Register.

DTR = 0 -
$\overline{DTR}$ is set to a logic one.

DTR = 1 -
$\overline{DTR}$ is set to a logic zero.

NOTE

The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

3.11 MODEM STATUS REGISTER

The MODEM Status Register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, bits 3 through 0 of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Address A2-A0 = 6, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
RLSD	RI	DSR	CTS	DRLSD	TERI	DDSR	DCTS

Signal Name	Default After Master Reset
RLSD	X
RI	X
DSR	X
CTS	X
DRLSD	0
TERI	0
DDSR	0
DCTS	0

Bit 7 - RLSD, Received Line Signal Detect

RLSD is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 3 of the MODEM Control Register (INT).

Bit 6 - RI, Ring Indicator

RI is the complement of the Ring Indicator ($\overline{RI}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 2 of the MODEM Control Register.

Bit 5 - DSR, Data Set Ready

DSR is the complement of the Data Set Ready ($\overline{DSR}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 0 of the MODEM Control Register (DTR).

Bit 4 - CTS, Clear To Send

CTS is the complement of the Clear to Send ($\overline{CTS}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 1 of the MODEM Control Register (RTS).

Bit 3 - DRLSD, Delta Received Line Signal Detector

DRLSD is the Delta Received Line Signal Detector (DRLSD) indicator.

DRLSD = 0 -
The $\overline{RLSD}$ input to the WD76C30/LV has not changed state since the last time it was read by the CPU.

DRLSD = 1 -
The $\overline{RLSD}$ input to the WD76C30/LV has changed state since the last time it was read by the CPU.

Bit 2 - TERI, Trailing Edge of Ring Indicator

TERI is the Trailing Edge of Ring Indicator (TERI) detector.

TERI = 0 -
The $\overline{RI}$ input to the WD76C30/LV has not changed from an On (logic 1) to an Off (logic 0) condition.

TERI = 1 -
The $\overline{RI}$ input to the WD76C30/LV has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 1 - DDSR, Delta Data Set Ready

DDSR is the Delta Data Set Ready (DDSR) indicator.

DDSR = 0 -
The $\overline{DSR}$ input to the WD76C30/LV has not changed state since the last time it was read by the CPU.

DDSR = 1 -
The $\overline{DSR}$ input to the WD76C30/LV has changed state since the last time it was read by the CPU.

Bit 0 - DCTS, Delta Clear to Send

DCTS is the Delta Clear to Send (DCTS) indicator.

DCTS = 0 -
The CTS input to the WD76C30/LV has not changed state since the last time it was read by the CPU.

DCTS = 1 -
The CTS input to the WD76C30/LV has changed state since the last time it was read by the CPU.

NOTE

Setting bits 3, 2, 1, or 0 to a logic 1 generates a MODEM Status Interrupt.

3.12 FIFO OPERATION NOTES

3.12.1 FIFO Interrupt Mode Operation

When FEWO and ERBFI are 1 (bit 0 of the FIFO Control Register and bit 1 of the Interrupt Enable Register), the following RCVR interrupts will occur.

1. A FIFO timeout interrupt occurs when the following is true:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in four continuous character times (if two stop bits are being used, the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded four continuous character times.

   The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level, the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

3. When the XMIT FIFO is empty, the THRE interrupt is set and is reset when one character is written to the XMIT FIFO.

3.12.2 FIFO Polling Mode Operation

The FIFO Polling Mode is initialized when FEWO is 1 and EDSSI, ERLSI, ETBEI and ERBFI are 0 (bit 1 of the FIFO Control Register and bits 3 through 0 of the Interrupt Enable Register). In polling mode, the user can poll the LSR directly to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately, either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated on the interrupt pin in the FIFO Polling Mode. However, the RCVR and XMIT FIFOs are still fully capable of holding characters.

3.12.3 FIFO Pointer

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte and associated Status byte to be read. Reading the RCVR Data byte increments the internal counter, while reading the Status byte does not, therefore, the Status byte should always be read prior to reading the Data byte associated with it.

4.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics type printers. When $\overline{CS2}$ is asserted, the parallel port is selected, allowing access to all parallel port control and status registers. (Refer to Tables 4-1 and 4-2.)

A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
X	0	0	1	0	Data - Write
X	0	0	0	1	Data - Read
X	0	1	0	1	Status - Read
X	1	0	1	0	Control - Write
X	1	0	0	1	Control - Read
0	1	1	1	0	Address Select Register - Write
0	1	1	0	1	Address Select Register - Read
1	1	1	1	0	Data Access Register - Write ①
1	1	1	0	1	Data Access Register - Read ①
X	0	1	1	0	Invalid

① A2-A0, $\overline{IOR}$ and $\overline{IOW}$, in conjunction with bits 2-0 of the Address Selection Register, select one of six registers. See section 5.1.

TABLE 4-1. PARALLEL PORT ($\overline{CS2}$ = 0) REGISTER ADDRESS

BIT NO.	READ DATA 0	WRITE DATA 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2
0	Data Bit 0	Data Bit 0	1	STB	STB
1	Data Bit 1	Data Bit 1	1	AFD	AFD
2	Data Bit 2	Data Bit 2	$\overline{INT}$ ①	$\overline{INIT}$	$\overline{INIT}$
3	Data Bit 3	Data Bit 3	$\overline{ERROR}$	SLIN	SLIN
4	Data Bit 4	Data Bit 4	SLCT	IRQ ENB	IRQ ENB
5	Data Bit 5	Data Bit 5	PE	1	DIR ②
6	Data Bit 6	Data Bit 6	$\overline{ACK}$	1	NC
7	Data Bit 7	Data Bit 7	$\overline{BUSY}$	1	NC

① This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 is a 1), Otherwise the bit is always a 1.

② This bit is only available when the parallel port bus is PS/2 compatible (Mode Selection Register bit 1 is a 1).

TABLE 4-2. ACCESSIBLE PARALLEL PORT REGISTERS

4.1 DATA REGISTER

This read/write register is used to write to or read data from the Parallel Port Data Bus.

Register select - Write:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A1-A0 = 0

Register select - Read:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 0

7	6	5	4	3	2	1	0
Parallel Bus Data							

Signal Name	Default After Master Reset
All signals	0

Bits 7-0

These bits represent the data being written to or read from the Parallel Port Data Bus.

4.2 STATUS REGISTER - READ

The contents of this read only register represents the status of the corresponding Parallel Port pins (refer to Tables 2-1, 4-2 and Figure 2-1).

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 1

7	6	5	4	3	2	1	0
$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	$\overline{INT}$	1	1

Signal Name	Default After Master Reset
$\overline{BUSY}$	X
$\overline{ACK}$	X
PE	X
SLCT	X
$\overline{ERROR}$	X
$\overline{INT}$	0
Bits 1, 0	1

Bit 7 - $\overline{BUSY}$

Bit 6 - $\overline{ACK}$, Acknowledge

Bit 5 - PE, Parity Error

Bit 4 - SLCT, Select

Bit 3 - $\overline{ERROR}$

Bit 2 - $\overline{INT}$, Interrupt

$\overline{INT}$ represents the status of the Parallel Port's internal interrupt signal. This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 equals 1) otherwise it is a 1.

Bits 1, 0

These bits are set to one by the hardware.

4.3 CONTROL REGISTER - WRITE

The Control Register is used to write to the associated lines and, with the exception of bits 7 through 5, may be read by a Control Register - Read operation. See section 4.4.

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A1-A0 = 2

7	6	5	4	3	2	1	0
NC	NC	DIR	IRQ_ ENB	SLIN	$\overline{INIT}$	AFD	STB

Signal Name	Default After Master Reset
Bits 7, 6	X
DIR	0
IRQ_ENB	0
SLIN	0
INIT	0
AFD	0
STB	0

Bits 7, 6 - Not connected

Bit 5 - DIR, Direction

DIR works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus (refer to Table 4-3). DIR only functions when the parallel port bus is PS/2 compatible as indicated by the Mode Selection Register bit 1 = 1.

Port Mode	Biden Pin 76	Direction Bit - 5	Port Direction	Compatability
Extended	1	0	Write *	PS/2
Extended	0	X	Write *	PS/2
Extended	1	1	Read *	PS/2
Compatible	1	N/A	Read *	PC/AT
Compatible	0	N/A	Write *	PC/AT

* Read and write refer to internal WD76C30/LV reading and writing the Parallel Port.

TABLE 4-3. PARALLEL PORT OPERATION MODES

Bit 4 - IRQ_ENB, Interrupt Enable

IRQ_ENB = 0 -
Parallel Port Interrupt is not enabled.

IRQ_ENB = 1 -
Parallel Port Interrupt is enabled.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

4.4 CONTROL REGISTER - READ

Bits 4 through 0 are read/write bits and represent the state as set by a Control Register - Write operation. Bit 5 (DIR) is a write only bit, and, along with bits 7 and 6, are always represented with a 1. See section 4.3

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 2

7	6	5	4	3	2	1	0
1	1	1	IRQ_ ENB	SLIN	$\overline{INIT}$	AFD	STB

Signal Name	Default After Master Reset
Bits 7-5	1
IRQ_ENB	0
SLIN	0
INIT	0
AFD	0
STB	0

Bits 7-5

These bits are set to one by the hardware.

Bit 4 - IRQ_ENB, Interrupt Enable

IRQ_ENB = 0 -
Parallel Port Interrupt is not enabled.

IRQ_ENB = 1 -
Parallel Port Interrupt is enabled.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

5.0 INTERRUPT, CLOCK AND MODE SELECTION REGISTERS

The internal registers used for the interrupt multiplexing, clock selection and mode selection are accessed in a two step process, using two address locations in the Parallel Port Register. First, the address for the desired register to be accessed is written into the Address Select Register located at address three of the Parallel Port. Then the data to be read from or written to the selected register is accessed through the Data Access Register (see Table 4-1), located at address seven in the Parallel Port. It is not necessary for these write operations to follow each other.

5.1 ADDRESS SELECTION REGISTER

Register select - Read:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2-A0 = 3

Register select - Write:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2-A0 = 3

7	6	5	4	3	2	1	0
TEST BIT	SER_PRT_1 CLK		SER_PRT_0 CLK		DAT_ACC_REG		

Signal Name	Default After Master Reset
All signals	0

Bit 7 - Testbit

The Testbit replaces the Serial 1, Serial 0 and Parallel Port interrupt signals to the internal interrupt multiplexer with the SLCT, BUSY and PE signals, respectively.

Bits 6, 5 - SER_PRT_1 CLK, Serial Port 1 Clock

These bits select the input clock used by serial port 1.

SER_PRT_1 CLK

6	5	Serial Port 1 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits 4, 3 - SER_PRT_0 CLK, Serial Port 0 Clock

These bits select the input clock used for serial port 0.

SER_PRT_0 CLK

4	3	Serial Port 0 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits 2-0 - DAT_ACC_REG, Data access register name

These bits, in conjunction with address A2-A0 = 7, select one of the six registers listed below. See Table 4-1.

When all accesses are completed, this field should be set to the Parking Value (7). This prevents inadvertent accesses to the Data Access Register from disturbing the setup during normal operation.

DAT_ACC_REG

2	1	0	Data Access Register Name	Reset Mode
0	0	0	Clock Select Reg.	00H
0	0	1	Clock Disable Reg.	00H
0	1	0	Serial Port 0 Int. Selection Reg.	00H
0	1	1	Serial Port 1 Int. Selection Reg.	00H
1	0	0	Parallel Port Int. Selection Reg.	00H
1	0	1	Mode Selection Reg.	00H
1	1	0	Version Register	
1	1	1	Parking Value	

B2	B1	B0	CLK287 FREQUENCY	COPROCESSOR SUPPORTED
0	0	0	8 MHz, 33% Duty Cycle	8 MHz Intel 80287 8 MHz AMD 80C287
0	0	1	9.6 MHz, 33% Duty Cycle	10 MHz Intel 80287 10 MHz AMD 80C287 10 MHz AMD 80EC287
0	1	0	12 MHz, 33% Duty Cycle	12 MHz AMD 80C287 12 MHz AMD 80EC287
0	1	1	12 MHz, 50% Duty Cycle	12 MHz Intel 80C287A
1	0	0	16 MHz, 33% Duty Cycle	16 MHz AMD 80C287 16 MHz AMD 80EC287
1	0	1	16 MHz, 50% Duty Cycle	Future Expansion
1	1	0	Logic Low	CLK287 Stopped low
1	1	1	Logic High	CLK287 Stopped high

TABLE 5-1. CLOCK SELECTION REGISTER

6

5.2 CLOCK SELECTION REGISTER

The Clock Selection Register is addressed by the Address Selection Register bits 2-0 = 0 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
RESERVED					CLOCK CO-CPU		

Signal Name	Default After Master Reset
All signals	0

Bits 7-3 - Reserved for future use and should be programmed to 0.

Bits 2-0 - CLOCK CO-CPU

These bits are used to select the desired frequency and duty cycle for supporting the 80287 coprocessor. Refer to Table 5-1 for the bit configurations.

5.3 SLEEP MODE

For low power consumption, the internal oscillators may be individually disabled via the Clock Disable Register described in section 5.4. For minimum power consumption, a sleep mode is offered which disables the 48 MHz clock, KBCLK, CLK287, ATCLK, Parallel Port (PD0 - 7), Data Bus (D0-7), all outputs, all pullups and, except for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{RESET}$, all inputs. Although KBCLK, CLK287, and ATCLK are disabled during sleep mode, their outputs are held low with small pulldown transistors.

Sleep Mode is activated by hardware asserting all three Chip Selects ($\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$) simultaneously. All registers are preserved in the sleep mode. Sleep Mode is deactivated when one or more of the Select signals are de-asserted.

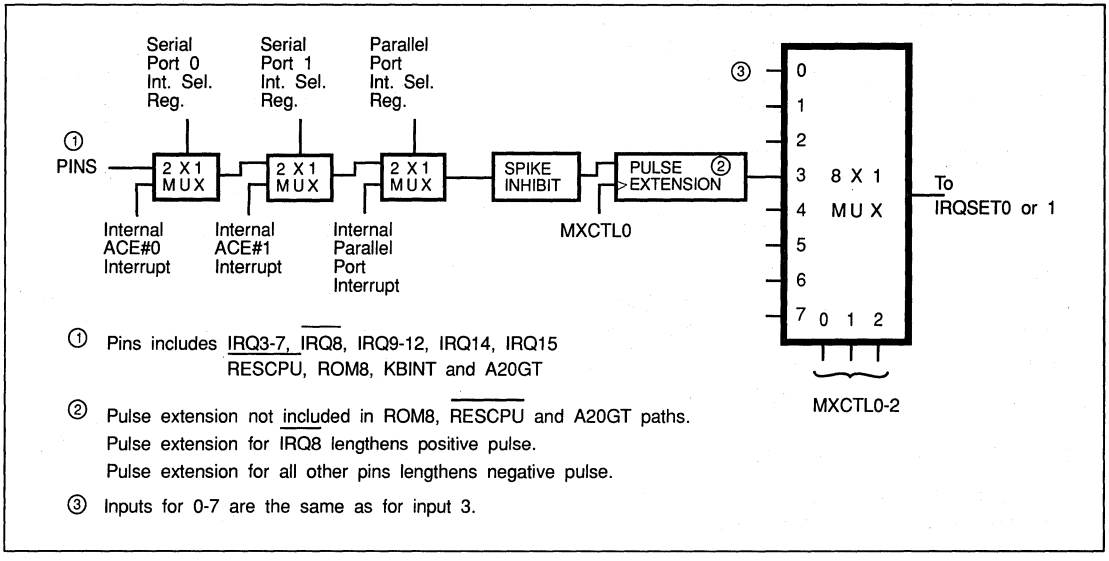

FIGURE 5-1. INTERRUPT MUX BLOCK DIAGRAM

5.4 CLOCK DISABLE REGISTER

The Clock Disable Register is addressed by the Address Selection Register bits 2-0 = 1 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
ISP1 CLK	ISP0 CLK			AT_ CLK	KB_ CLK	OSC_ DIS	

Signal Name	Default After Master Reset
All signals	0

Bit 7 - ISP1_CLK, Internal Serial Port 1 Clock

ISP1_CLK = 0 -
Internal Serial Port 1 clock is not disabled.

ISP1_CLK = 1 -
Internal Serial Port 1 clock is disabled.

Bit 6 - ISP0_CLK, Internal Serial Port 0 Clock

ISP0_CLK = 0 -
Internal Serial Port 0 clock is not disabled.

ISP0_CLK = 1 -
Internal Serial Port 0 clock is disabled.

Bit 5, 4 - Reserved and should be programmed to 0.

Bit 3 - ATCLK

ATCLK = 0 -
ATCLK is not disabled.

ATCLK = 1 -
ATCLK signal is held at a logic low.

Bit 2 - KBCLK

KBCLK = 0 -
KBCLK is not disabled.

KBCLK = 1 -
KBCLK signal is held at a logic low.

Bit 1 - OSC_DIS, Oscillator Disable

OSC_DIS = 0 -
The 48 MHz oscillator is not disabled and, KBCLK, CLK287 and ATCLK are not frozen.

OSC_DIS = 1 -
The 48 MHz oscillator is disabled and, KBCLK, CLK287 and ATCLK are frozen.

Bit 0 - Reserved and should be programmed to 0.

NOTE

Asserting $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ simultaneously disables the 48 MHz oscillator. Upon removing the disabling of the 48 MHz oscillator, it restarts itself within 30 ms. Logic prevents the internal OSC Clock from starting again until the 48 MHz oscillator is running at full amplitude.

5.5 MODE SELECTION REGISTER

The Mode Selection Register is addressed by the Address Selection Register bits 2-0 = 5 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				PUD	ATPS2 INT	ATPS2 PP	SP FIFO

Signal Name	Default After Master Reset
All signals	0

Bits 7-4 - Reserved and should be programmed to 0.

Bit 3 - PUD, Power-up Power-down

PUD must always be high when powering down the ports by turning off V_{DD}.

PUD = 0 -
The serial and parallel ports are in the power-up mode.

PUD = 1 -
The serial and parallel ports are in the power-down mode (see Tables 3-2 and 6-11).

With the exception of addresses 011 and 111 of the parallel port, all registers are reset. Also, the following signals are disabled: $\overline{DTR0}$, $\overline{DTR1}$, $\overline{RST0}$, $\overline{RST1}$, SOUT0, SOUT1, PD0-7, BIDEN, $\overline{ERROR}$, $\overline{SLCT}$, $\overline{PE}$, $\overline{ACK}$, BUSY, $\overline{INIT}$, $\overline{SLIN}$, $\overline{STB}$ AND $\overline{AFD}$.

Bit 2 - ATPS2_INT, PC/AT PS/2 Parallel Port Interrupt

ATPS2_INT = 0 -
The Parallel Port Interrupt signal is PC/AT compatible.

ATPS2_INT = 1 -
The Parallel Port interrupt signal is PS/2 compatible.

Bit 1 - ATPS2_PP, PC/AT PS/2 Parallel Port

ATPS2_PP = 0 -
The Parallel Port Bus is configured as a PC/AT compatible Parallel Port.

ATPS2_PP = 1 -
The Parallel Port Bus is configured as a PS/2 extended Parallel Port.

Bit 0 - SP_FIFO, Serial Port FIFO

SP_FIFO = 0 -
Both Serial Ports are configured to operate in non-FIFO mode (Character Mode).

SP_FIFO = 1 -
Both Serial Ports can operate in the FIFO mode if the applicable FEWO is set to 1. The FEWO bit is located in the FIFO Control Register described in section 3.9. The following boolean equation illustrates how to select the Character Mode or FIFO Mode.

Character Mode = $\overline{FEWO} + \overline{SP\_FIFO}$
FIFO Mode = FEWO • SP_FIFO

5.6 INTERRUPT MULTIPLEXER

The WD76C30/LV provides the logic required to interface the PC/AT interrupt request lines with the WD7XC10 Single Chip AT Controller. The WD7XC10 generates input signals MXCTL2 - 0 and the WD76C30/LV uses these signals to select the IRQ inputs. Table 5-3 identifies the multiplexing sequence for the IRQSET0 and IRQSET1 signals. The output of the sampled IRQ inputs are provided on the IRQSET0 and IRQSET1 outputs (see Figure 5-2 IRQSET).

Negative pulse extension logic widens negative pulses on twelve of the sixteen MUX inputs. They are IRQ3-7, IRQ9-12, IRQ14,15 and KBINT. Positive pulse extension logic widens a positive pulse on IRQ8. The pulse width is extended by five positive going edges on MXCTL0 from the leading edge of the pulse or three positive going edges on MXCTL0 from the trailing edge of the pulse, whichever lasts longer. Note that pulses in the opposite direction that don't include three rising MXCTL0 edges are never seen on IRQSET0 or IRQSET1. None of this pulse extension logic applies to RESCPU, ROM8 or A20GT (see Figure 5-1 Interrupt Mux Block Diagram).

When the appropriate bits in the Serial Port 0 Interrupt Selection Register (see section 5.7) are set to the Stand Alone Mode, the interrupt multiplexing logic is disabled. IRQSET0 and IRQSET1 are defined in Table 5-2. The Serial Port 0 Interrupt Selection Register and Serial Port 1 Interrupt Selection Register are used to assign Serial Port Interrupts to IRQ MUX inputs. The Parallel Port Interrupt Selection Register is used to assign the Parallel Port Interrupt to one IRQ MUX input.

IRQSET0 = Serial Port 0 Interrupt (tri-state enabled by bit 3 of the Modem Control Register)

IRQSET1 = Serial Port 1 Interrupt (tri-state enabled by bit 3 of the Modem Control Register)

IRQ7 = Parallel Port Interrupt (tri-state enabled by bit 4 of the parallel port Write Control Register)

TABLE 5-2. STAND ALONE MODE

MXCTL 2	1	0	IRQSET0
0	0	0	$\overline{\text{IRQ8}}$
0	0	1	IRQ9
0	1	0	IRQ10
0	1	1	IRQ11
1	0	0	ROM8
1	0	1	$\overline{\text{RESCPU}}$
1	1	0	IRQ14
1	1	1	IRQ15
MXCTL 2	**1**	**0**	**IRQSET1**
0	0	0	IRQ12
0	0	1	KBINT
0	1	0	A20GT
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

TABLE 5-3. MXCTL2 - 0 IRQSET0 - 1 MULTIPLEXING

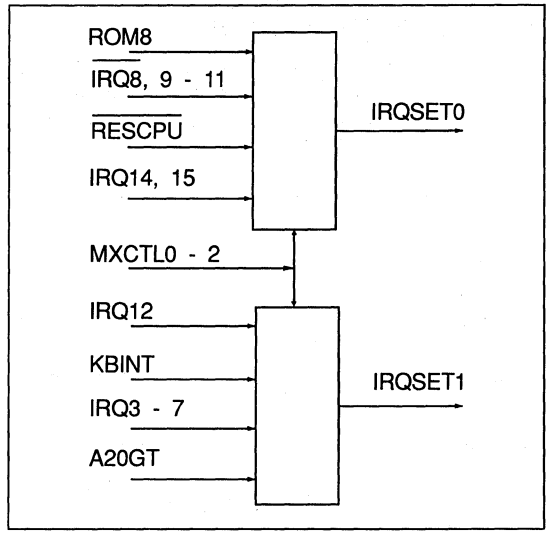

FIGURE 5-2. IRQSET - WHEN NOT IN STAND ALONE MODE

5.7 SERIAL PORT 0 INTERRUPT SELECTION REGISTER

The Serial Port 0 Interrupt Selection Register is addressed by the Address Selection Register bits 2-0 = 2 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				SP0_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - SP0_INT_SEL, Serial Port 0 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 0 Interrupt. The Stand Alone Mode may also be selected by these bits and applies to all ports.

Bits 4 and 3 of the Modem Control Register (refer to section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 0 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15
X	1	1	1	1	Stand Alone Mode

All other combinations are reserved.

5.8 SERIAL PORT 1 INTERRUPT SELECTION REGISTER

The Serial Port 1 Interrupt Selection Register is addressed by the Address Selection Register bits 2-0 = 3 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				SP1_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - SP1_INT_SEL, Serial Port 1 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 1 Interrupt.

Bits 4 and 3 of the Modem Control Register (refer to section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 1 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Serial Port 1 Interrupt Selection Register has priority over the Serial Port 0 Interrupt Selection Register. That is, Serial Port 1 interrupt replaces the Serial Port 0 interrupt when both registers select the same interrupt. The interrupts are not ORed.

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5.9 PARALLEL PORT INTERRUPT SELECTION REGISTER

The Parallel Port Interrupt Selection Register is addressed by the Address Selection Register bits 2-0 = 4 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				PP_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - PP_INT_SEL, Parallel Port Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Parallel Port Interrupt.

IRQ_ENB is bit 4 of the Parallel Port Control Register (refer to section 4.3) and must be set to 1.

IRQ EN	B3	B2	B1	B0	Parallel Port Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Parallel Port Interrupt Selection Register has priority over both of the Serial Port Interrupt Selection Registers. That is, the Parallel Port interrupt replaces the Serial Port 0 or 1 interrupt when the registers select the same interrupt. The interrupts are not ORed.

5.10 VERSION REGISTER

The Version Register is a read only register and contains the ones-compliment of the version of the WD76C30/LV. FF hex represents Revision A, B and C. FE hex is revision D.

The Version Register is addressed by the Address Selection Register bits 2-0 = 6 and address bits A2-A0 = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
			Version Number				

Signal Name	Default After Master Reset
All signals	X

6.0 ELECTRICAL SPECIFICATIONS

This section provides the AC Timing Characteristics for both the WD76C30 and WD76C30LV, and the DC Operating Characteristics for the WD76C30. Refer to the appendix for the DC Operating Characteristics for the WD76C30LV.

6.1 MAXIMUM RATINGS - WD76C30

Temperature Under Bias .....0°C (32°F) to 70°C (158°F)

Storage Temperature .....-65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages with respect to Vss .....-0.5V to +7.0V

Power Dissipation .....300 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

6.2 CAPACITANCE - WD76C30

Ta = 25°C (77°F), f = 1.0 MHz, VccA = 5.0V, VccB = 5.0V, Vss = 0V

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

TABLE 6-1 CAPACITANCE

6.3 DC OPERATING CHARACTERISTICS - WD76C30

Ta = 0°C (32°F) to +70°C (158°F), V_{DD} = +5V ±5%, V_{DD2} = +5V ±5%
Vss = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0 2.3	Vcc Vcc	V V	Except MXCTL2-0 MXCTL2-0
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB ,SLIN, AFD ① Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB0-DB7. Ioh = -15.0 mA on PD0-PD7. Ioh = -0.55 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, $\overline{SLIN}$. Ioh = -0.2 mA on other outputs.
Icc	Power Supply Current		80	mA	Vcc = 5.5V MSTRX1 = 48 MHz All other inputs = 5.5V. All outputs floating Baud Rate = 512K. Serial Port CLK = 8 MHz.
Iil ②	Input Leakage		±15	µA	Vcc = 5.5V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage				Vin = 0.0V, 5.5V.
Idl	Data Bus Leakage (DB and PD)		±10	µA	Vout = 0.4V, Vout = 4.5V Data Bus in High Impedance State.
Ioz	Tristate Leakage		± 20	µA	Vcc = 5.5V, GND = 0V, Vout = 0.0V, 5.5V.
Vil (RES)	$\overline{Reset}$ Schmitt Vil		0.8	V	
Vih (RES)	$\overline{Reset}$ Schmitt Vih	2.3		V	

TABLE 6-2. DC OPERATING CHARACTERISTICS

① The $\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{INIT}$ outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. In PS/2 mode $\overline{IRQ7}$ is also an open collector. When in Vol state, each input sinks a minimum of 10 mA.

② $\overline{RESCPU}$, IRQ3 - 7, $\overline{IRQ8}$, IRQ9 - 12, IRQ14 - 15, ROM8, A20GT, KBINT, AND $\overline{CS1}$ have nominally 300 µA pullups. These pullups, along with all others, are disabled when the 48 MHz oscillator is disabled by asserting $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ simultaneously. The pulldowns on KBCLK, ATCLK, and CLK287 are enabled when the three chip selects are low and sink 40 mA min.

6.4 AC OPERATING CHARACTERISTICS AND TIMING WD76C30/LV

Ta = 0°C (32°F) to +70°C (158°F), V_{DD} = +5V ± 5%, $V_{DD}2$ = +5V ± 5% WD76C30
Vss = 0V, V_{DD} = $V_{DD}2$ = 3.3V ±10% WD76C30LV

Table 6-1 lists the timing categories and their Figure and Table number.

FIGURE NUMBER	TABLE NUMBER	FIGURE TITLE
6-1	6-4	Receiver Timing
6-2	6-5	Transmitter Timing
6-3	6-6	MODEM Control Timing
6-4	6-7	Read Cycle Timing
6-5	6-7	Write Cycle Timing
6-6	6-4	RCVR FIFO Signaling Timing for First Byte
6-7	6-4	RCVR FIFO Signaling Timing after First Byte (RBR already set)
6-8	6-8	Parallel Port Timing
6-9	6-8	Parallel Port Interrupt Timing
6-10	6-9	Clock Generation Timing
6-11	6-10	Interrupt MUX Timing (A)
6-12	6-10	Interrupt MUX Timing (B)

TABLE 6-3. TIMING FIGURE/TABLE NUMBERS

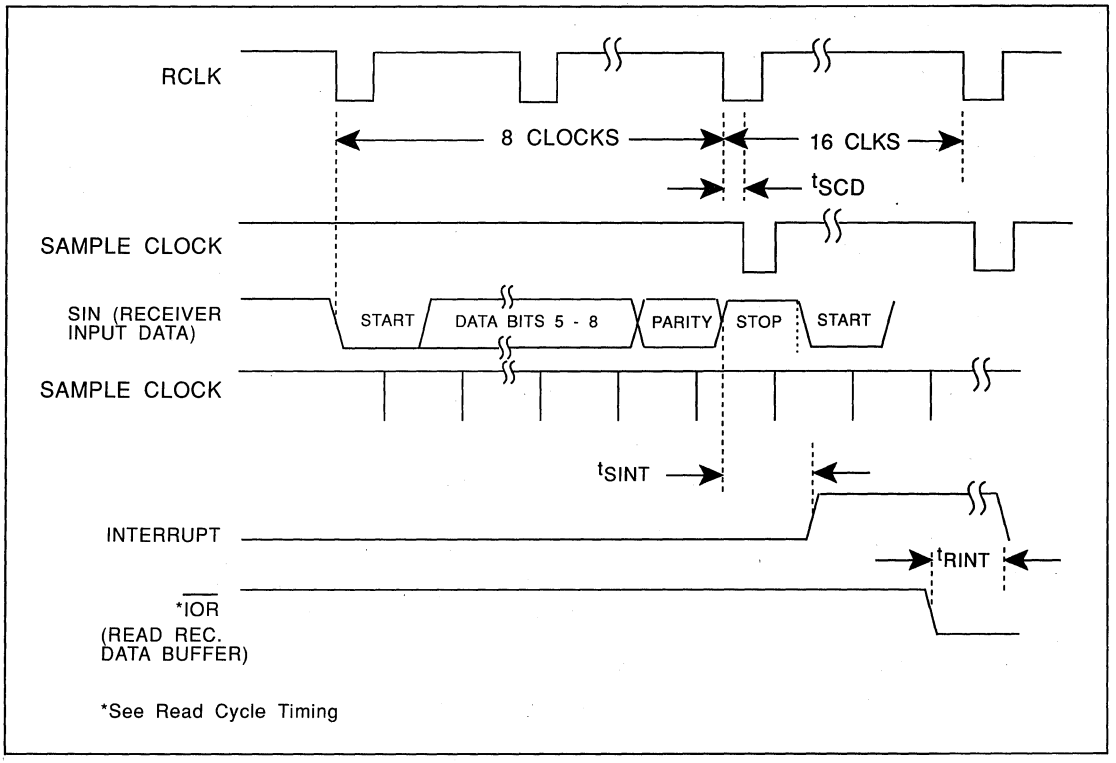


FIGURE 6-1. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK ② to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		17 ①	RCLK ② Cycles	100 pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt		250	ns	100 pF Load

TABLE 6-4. RECEIVER TIMING

① When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

② RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

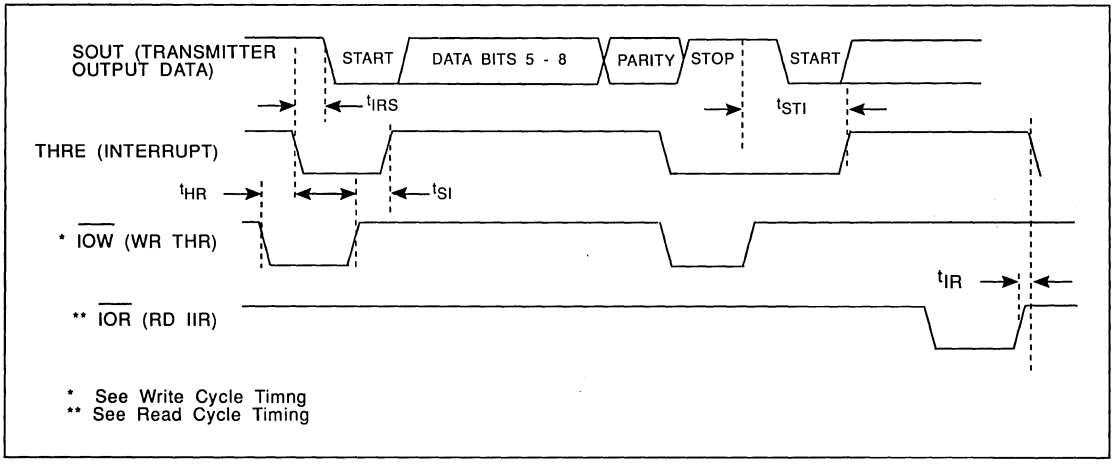


FIGURE 6-2. TRANSMITTER TIMING

6

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tHR	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from initial INTR Reset to Transmit start	8	24	TCLK ① Clock Cycles	
tSI ②	Delay from Initial Write to Interrupt	16	24	TCLK ① Clock Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	TCLK ① Clock Cycles	
tIR	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load

TABLE 6-5. TRANSMITTER TIMING

① TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.

② In FIFO mode tSI might extend to beginning of Stop Bit. See Line Status Register for details.

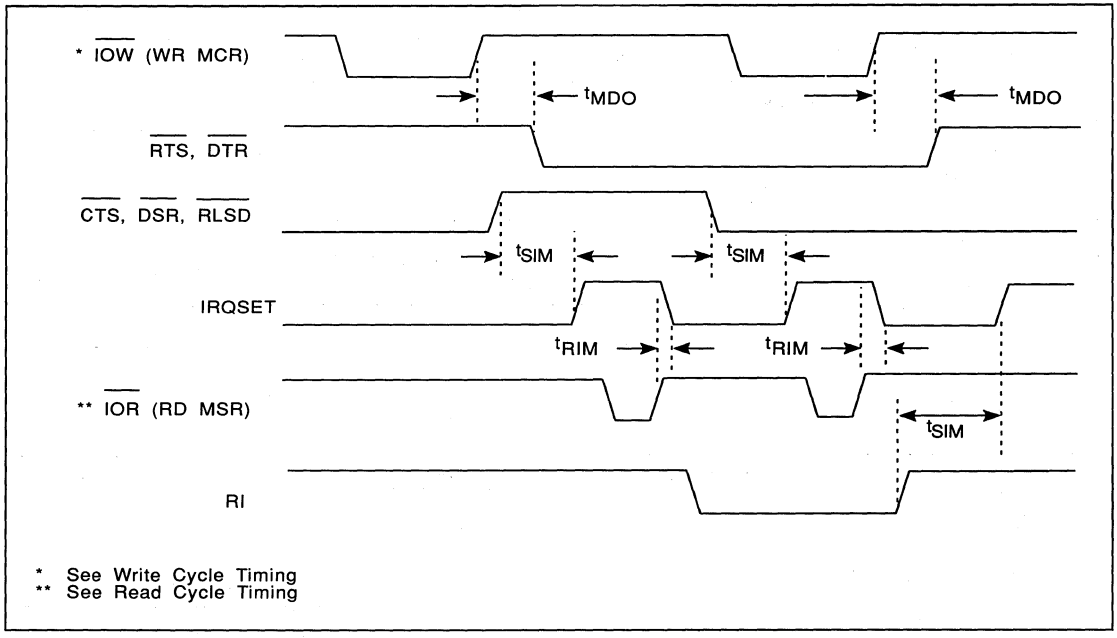


FIGURE 6-3. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		250	ns	100 pF Load

TABLE 6-6. MODEM CONTROL TIMING

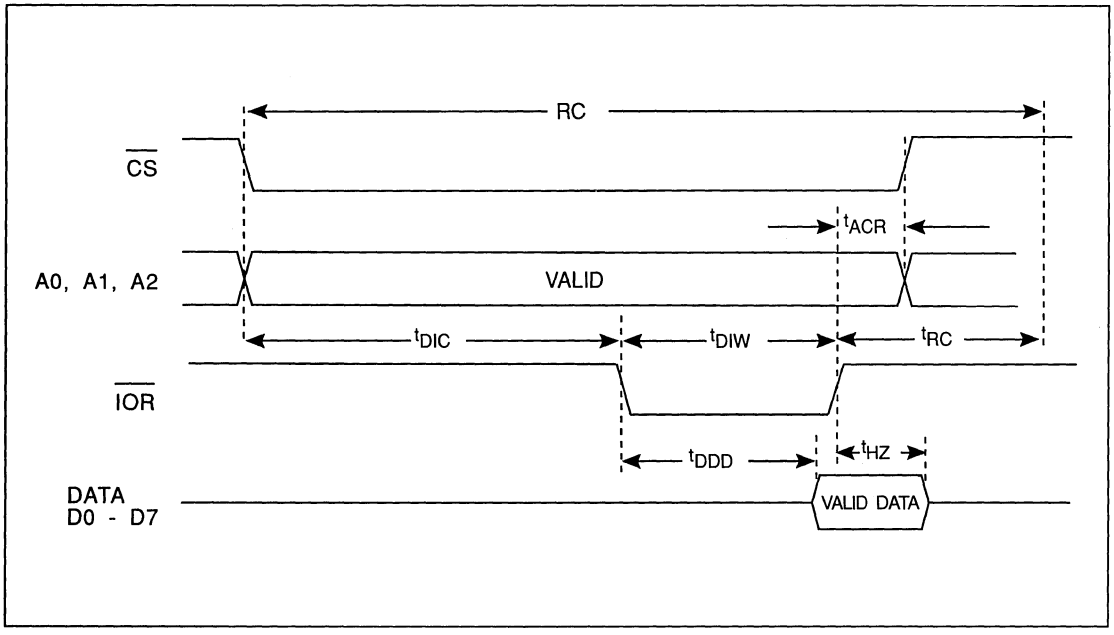


FIGURE 6-4. READ CYCLE TIMING

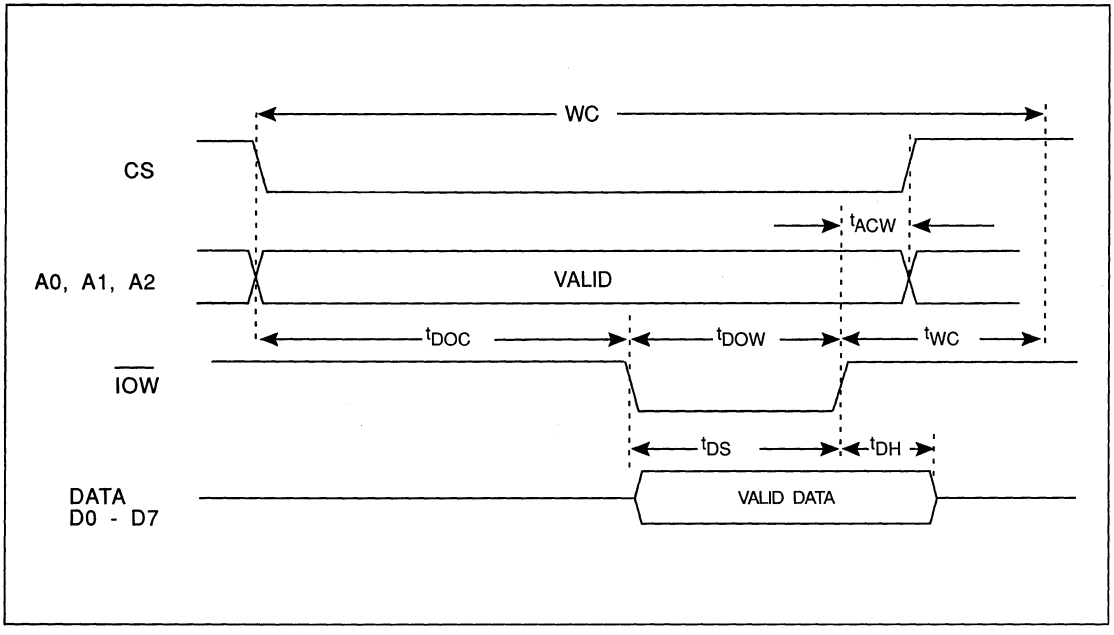


FIGURE 6-5. WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
t_{RC}	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = $t_{DIC} + t_{DIW} + t_{RC}$ + 20 ns	300		ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 ns	300		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOW}$	20		ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to data		100	ns	1 TTL Load
t_{MR}	Master Reset Pulse Width	1.0		µs	1 TTL Load
t_{PWRUP}	Delay from TTL Clock in to internal clock on power up.		50	µs	
t_{OSCUP}	Delay from OSC clock in to internal clock on power up.		30	ms	

TABLE 6-7. READ/WRITE CYCLE TIMING

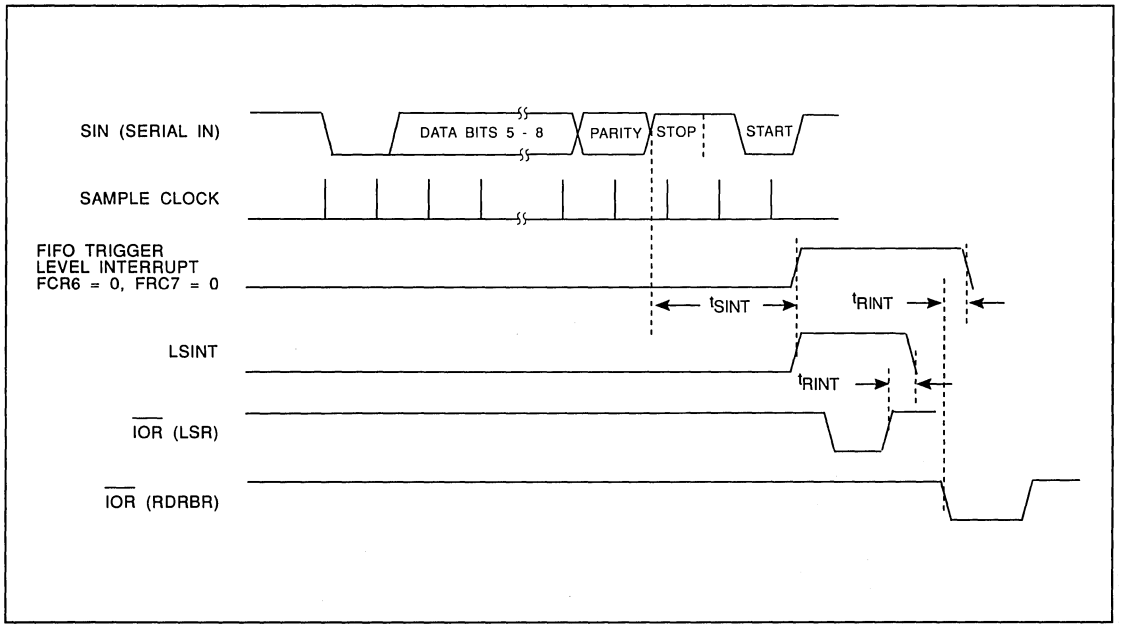


FIGURE 6-6. RCVR FIFO SIGNAL TIMING FOR FIRST BYTE

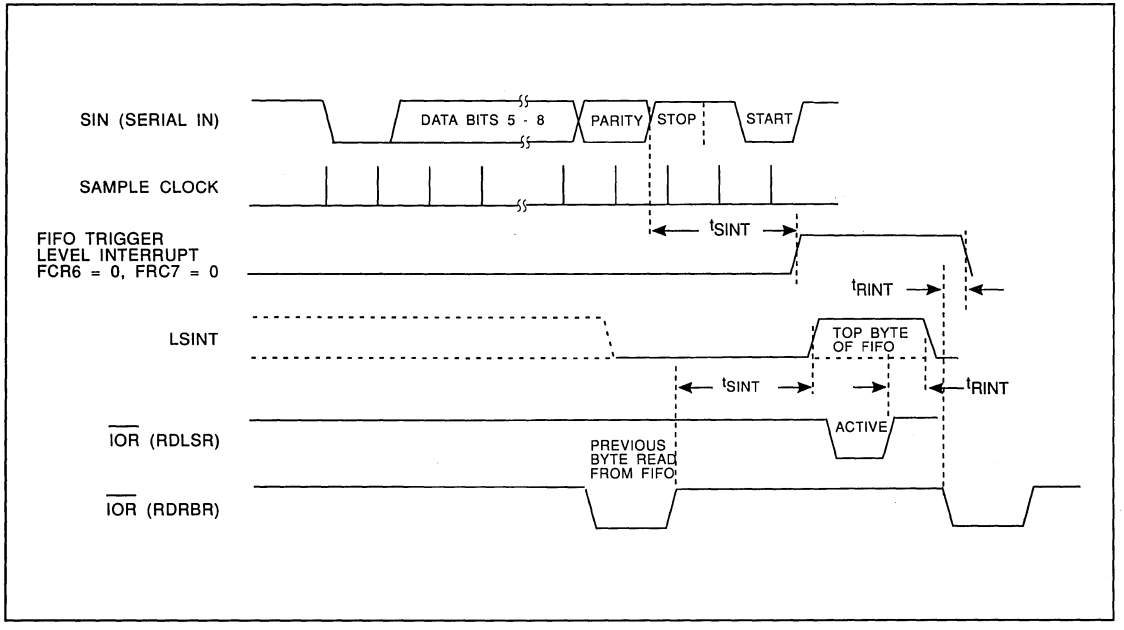


FIGURE 6-7. RCVR FIFO SIGNAL TIMING AFTER FIRST BYTE (RBR ALREADY SET)

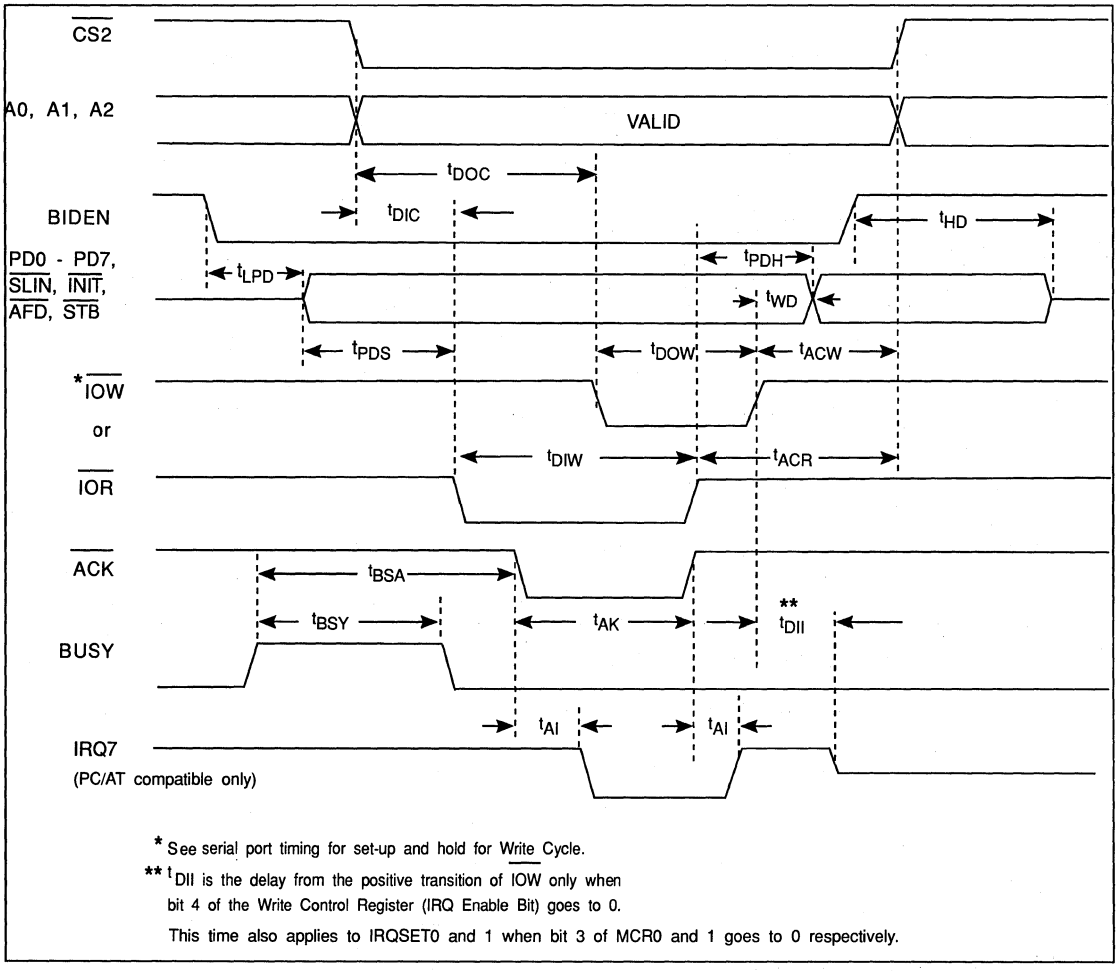


FIGURE 6-8. PARALLEL PORT TIMING

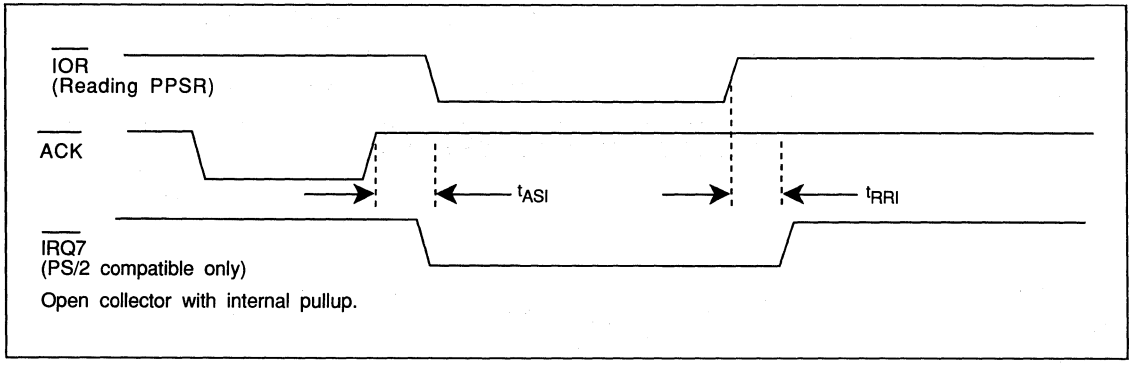


FIGURE 6-9. PARALLEL PORT INTERRUPT TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, $\overline{SLIN}$, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF Load
t_{HD}	BIDEN High to PD0-PD7 Tri-State		120	ns	50 pF Load
t_{LPD}	BIDEN Low to PD0-PD7 Delay		100	ns	50 pF Load
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$	0		ns	
t_{BSY}	BUSY Width	100		ns	
t_{AK}	$\overline{ACK}$ Width	100		ns	
t_{AI}	IRQ7 Delay from $\overline{ACK}$		60	ns	50 pF Load
tASI	$\overline{ACK}$ to set interrupt		60	ns	50 pF Load
t_{RRI}	Read Parallel Port Status Register (PPSR)		60	ns	50 pF Load
t_{DII}	$\overline{IOW}$ to TriState	0	100	ns	50 pF Load

TABLE 6-8. PARALLEL PORT TIMING

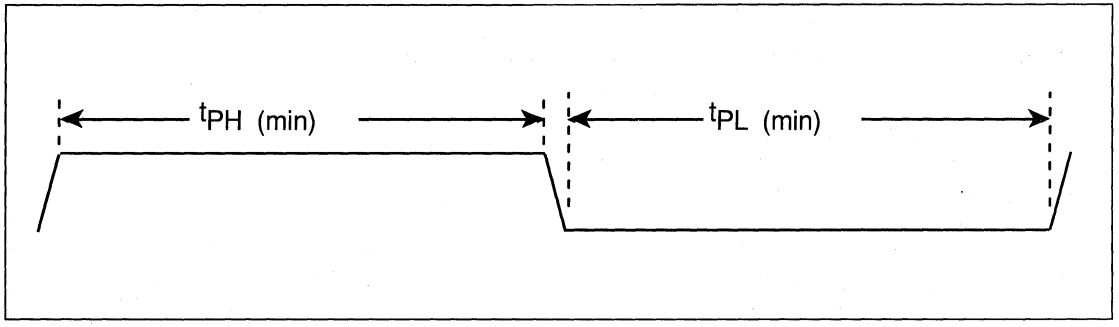
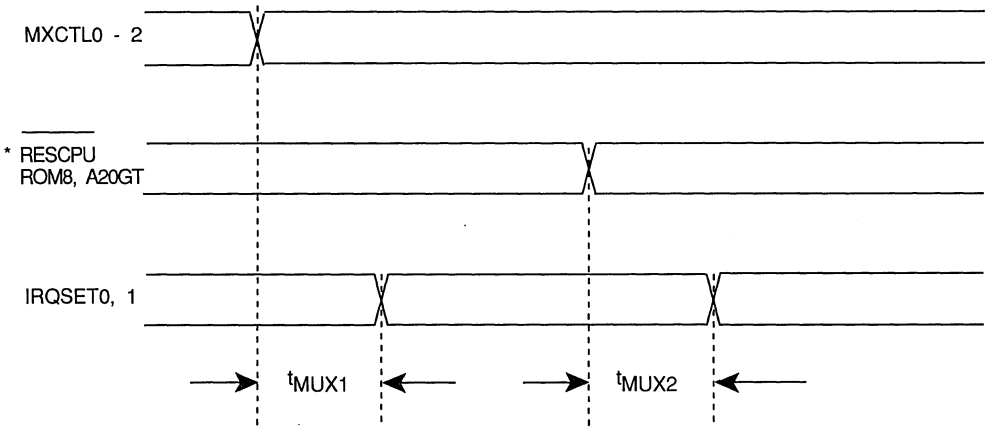


FIGURE 6-10. CLOCK GENERATION TIMING

CLOCK TYPE	t_{PH} min. ns.	t_{PL} min. ns.	FREQUENCY MHz	MAX. EDGE DELAY ① FROM MSTRX1 EDGE
CLK287 SEL				
0	40	68	8	100 ns
1	28	60	9.6	100 ns
2	20	50	12	100 ns
3	35	35	12	100 ns
4	14	35	16	100 ns
5	25	25	16	100 ns
KBCLK	50	33	9.6	100 ns
ATCLK	27	25	16	100 ns
MSTRX1	8	8	48	N/A

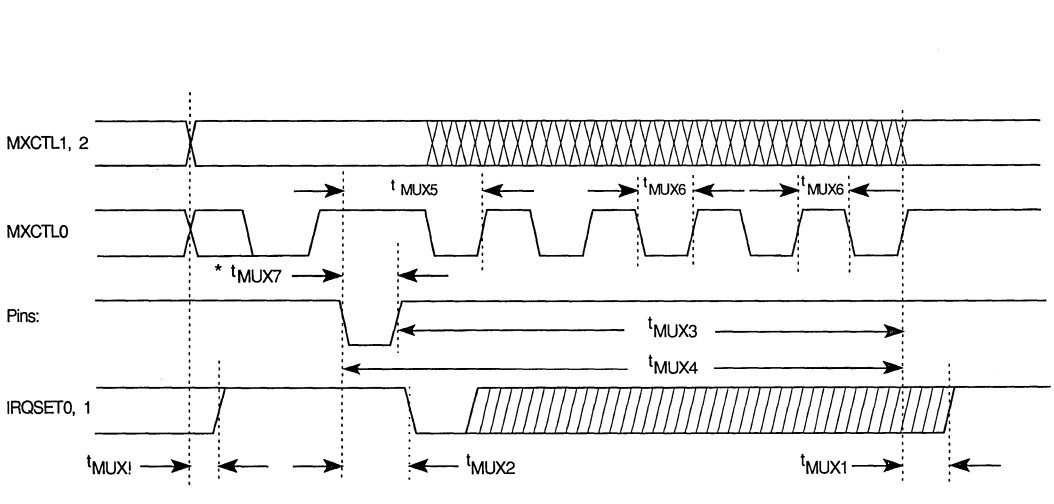
TABLE 6-9. CLOCK GENERATION TIMING

① All 50 pF loads



* Spikes of 10 ns or less on inputs are suppressed.

FIGURE 6-11. INTERRUPT MUX TIMING - A



Pins: IRQ3-7, IRQ9-12, IRQ14, IRQ15, KBINT, IRQ8 (IRQ8 PIN INVERTED)
* Spikes of 10 ns or less are suppressed

FIGURE 6-12. INTERRUPT MUX TIMING - B

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
^{t}MUX1	Delay from MUX control change		25	ns	50 pF load
^{t}MUX2	Delay from MUX input going low		125	ns	50 pF load
^{t}MUX3	Rising MXCTL0 clock edges required	3	5		
^{t}MUX4	Rising MXCTL0 clock edges required	5			
^{t}MUX5	MUX input setup time	100		ns	
^{t}MUX6	MXCTL0-2 pulse width	40		ns	
^{t}MUX7	Pins pulse width	75		ns	

TABLE 6-10. INTERRUPT MUX TIMING

PIN NUMBER	SIGNAL NAME	① INPUT/ OUTPUT	② SERIAL ③ PARALLEL POWER DOWN	② FULL ③ POWER DOWN
50	$\overline{DTR0}$	O	OZ	OZ
83	$\overline{DTR1}$	O	OZ	OZ
49	$\overline{RTS0}$	O	OZ	OZ
84	$\overline{RTS1}$	O	OZ	OZ
82, 51	SOUT1, 0	O	OZ	OZ
40	ATCLK ⑤⑦	O, P	O, PZ	OZ, PL
38	CLK287 ⑥⑦	O, P	O, PZ	OZ, PL
37	KBCLK ⑤⑦	O, P	O, PZ	OZ, PL
2, 1	IRQSET1, 0	O	O	OZ
23	IRQ7	I, O, P	I, O, PH	IX, OZ, PZ
57-62, 65, 66	PD7-0	I, O	IX, OZ	IX, OZ
76	BIDEN ⑧	I, P	IX, PZ	IX, PZ
71	$\overline{ERROR}$	I	IX	IX
72	SLCT	I	IX	IX
74	$\overline{PE}$	I	IX	IX
75	$\overline{ACK}$	I	IX	IX
73	BUSY	I	IX	IX
69	$\overline{INIT}$	I, O,P	IX, OZ, OZ	IX, OZ, OZ
70	$\overline{SLIN}$	I, O,P	IX, OZ, PZ	IX, OZ, PZ
67	$\overline{STB}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
68	$\overline{AFD}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
48	$\overline{CS0}$	I	I	I
46	$\overline{CS2}$	I	I	I
47	$\overline{CS1}$	I, P	I, PH	I, PZ
53	$\overline{RLSD0}$	I	IX	
52	$\overline{CTS0}$	I	IX	IX
54	$\overline{RI0}$	I	IX	IX
55	$\overline{DSR0}$	I	IX	IX
81	$\overline{CTS1}$	I	IX	IX
80	$\overline{RLSD1}$	I	IX	IX
79	$\overline{RI1}$	I	IX	IX
78	$\overline{DSR1}$	I	IX	IX
77, 56	SIN1, 0	I	IX	IX
6-4	MXCTL2-0	I	I	IX
8-11	IRQ3-6	I, P	I, PH	IX, PZ
12	IRQ8	I, P	I, PH	IX, PZ
13-15, 19	IRQ9-12	I, P	I, PH	IX, PZ
17, 18	IRQ14, 15	I, P	I, PH	IX, PZ
16	ROM8	I, P	I, PH	IX, PZ
20	A20GT	I, P	I, PH	IX, PZ

TABLE 6-11. STATE OF PINS AT POWER DOWN

PIN NUMBER	SIGNAL NAME	① INPUT/ OUTPUT BUFFER	② SERIAL ③ PARALLEL POWER DOWN	② FULL ③ POWER DOWN
21	$\overline{\text{KBINT}}$	I, P	I, PH	IX, PZ
7	$\overline{\text{RESCPU}}$	I, P	I, PH	IX, PZ
32-24	D7-0	I, O	I, O	IX, OZ
41	$\overline{\text{IOW}}$	I	I	IX
42	$\overline{\text{IOR}}$	I	I	IX
43-45	A2-A0	I	I	IX
36	$\overline{\text{RESET}}$	I	I	I
35	MSTRX1 ④	I, O	I, OB	I, OH
34	MSTRX2	O	O	OL

①

BUFFER TYPE

I = Input buffer
O = Output buffer
P = Pullup or pulldown

② **POWER DOWN STATE**

OZ = Tri-state output
O = Driven output
OH = Output driven high
OL = Output driven low
OB = Output driven to oscillator BIAS point

I = Input enabled
IX = Input disabled, consumes no power, input between 0V and 5V
PH = Pullup enabled
PL = Pulldown enabled
PZ = Pullup or pulldown disabled

③ Serial/Parallel Power Down: PUD = 1 (bit 3 of the Mode Selection Register described in section 5.5). Full Power Down: $\overline{\text{CS2}}$, $\overline{\text{CS1}}$ and $\overline{\text{CS0}}$ on pins 46, 47 and 48 are low simultaneously. This has priority over PUD.

④ When driven by a TTL oscillator, MSTRX1 requires an input low current (I_{IL}) of approximately 1 mA. To eliminate this in full power down mode, the TTL oscillator driving MSTRX1 must be disabled or driven to +5 volts.

⑤ KBCLK and ATCLK can be programmed to stop with their outputs remaining low. Stopping is not synchronous and is separate from what happens during a full power down.

⑥ CLK287 can be programmed to stop with its output remaining high or low. Stopping is synchronous and is separate from what happens in full power down.

⑦ When entering full power down, the drivers for KBCLK, ATCLK and CLK287 are tri-stated and are driven low by a pulldown FET that is only enabled during a full power down. This FET sinks a minimum of 45 µA, and drives the output low when connected to a CMOS input. Stopping is not synchronous.

⑧ BIDEN has an external pullup so that applications requiring a high can leave it floating.

TABLE 6-11. STATE OF PINS AT POWER DOWN Cont.

7.0 PACKAGE DIMENSIONS

Figure 7-1. Illustrates the 84-Pin PLCC package showing the dimensions in inches.
Figure 7-2. Illustrates the 84-Pin PQFP package showing the dimensions in inches.

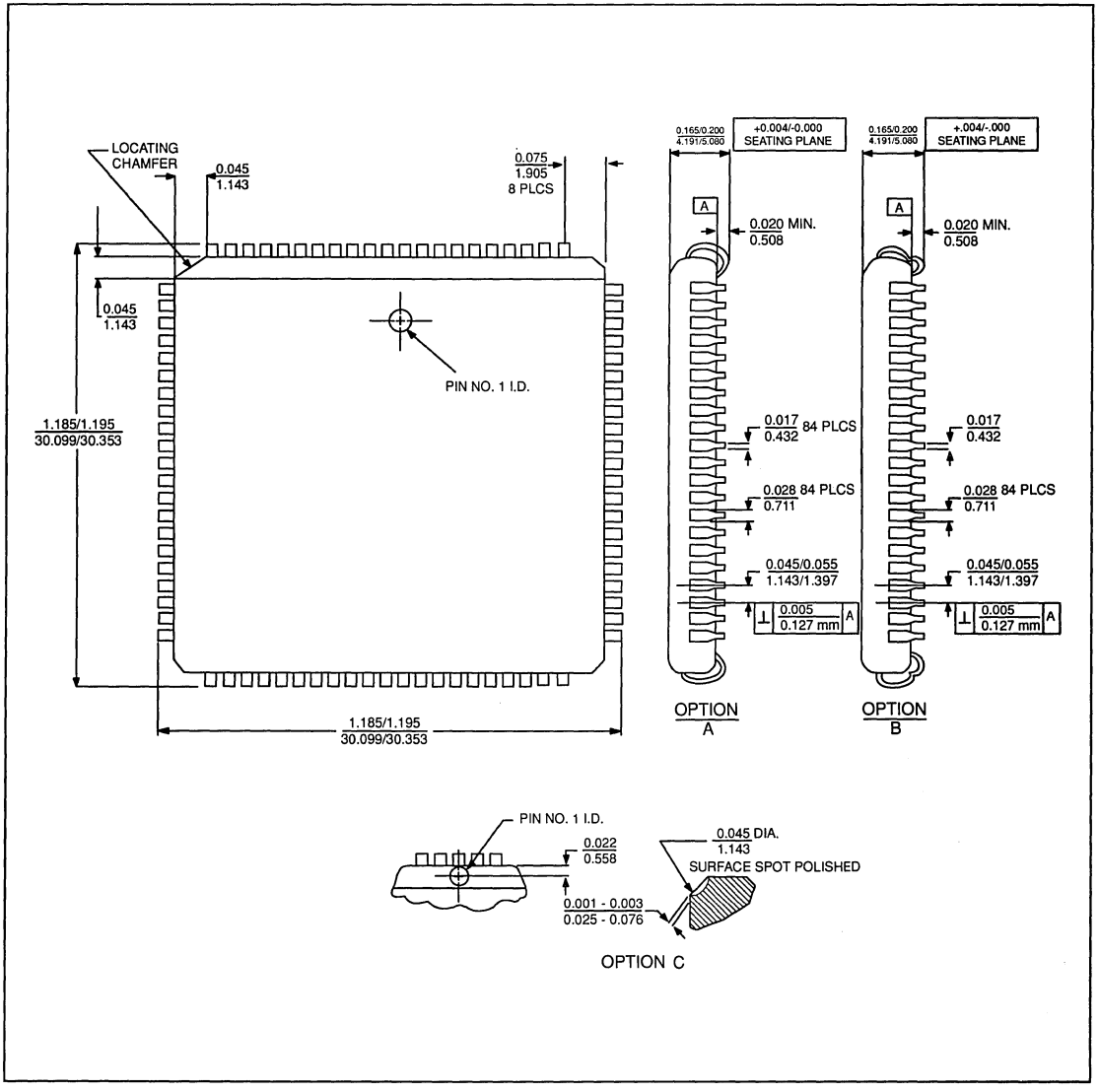


FIGURE 7-1. 84-PIN PLCC PACKAGE

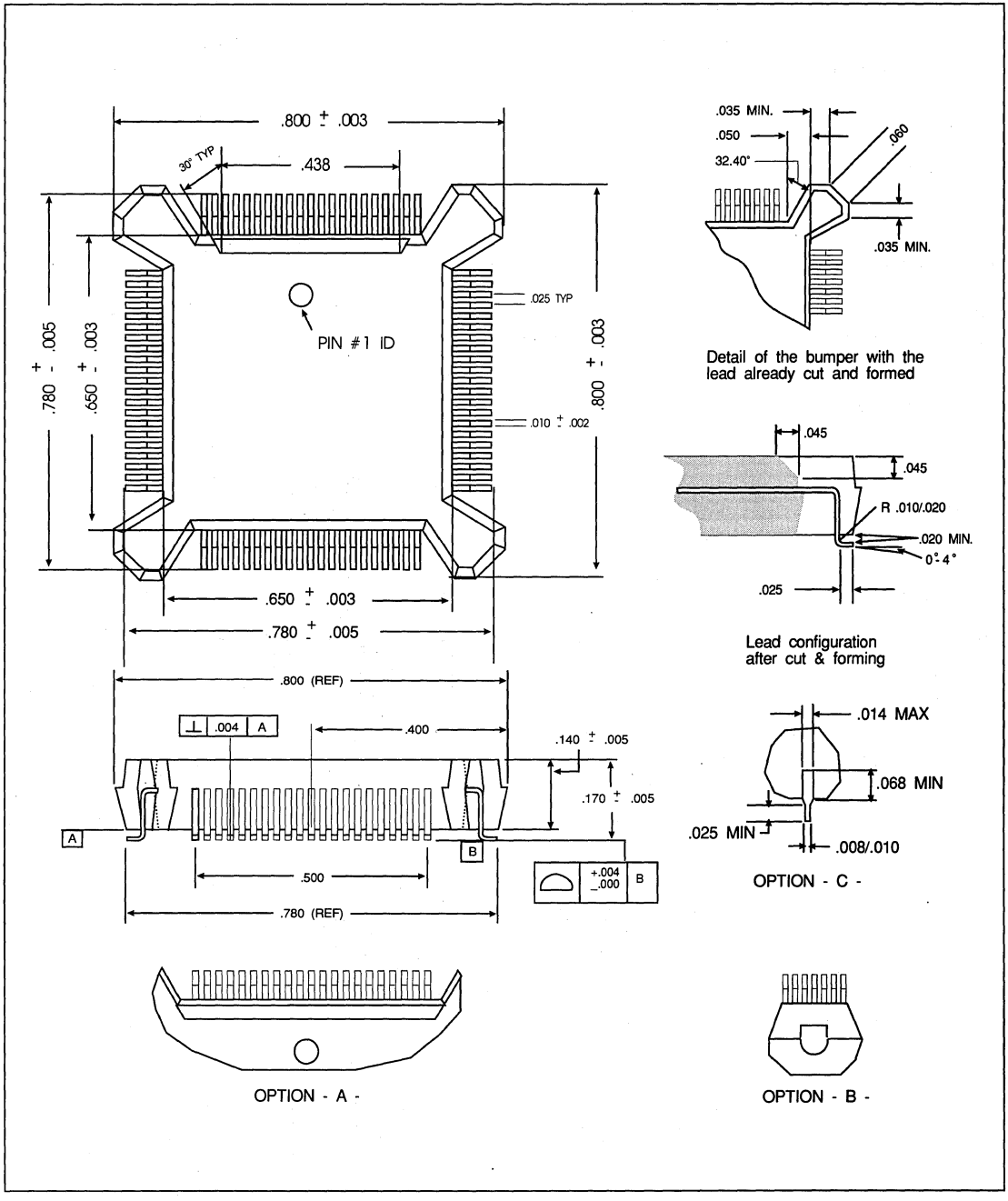


FIGURE 7-2. 84-PIN PQFP PACKAGE

8.0 CRYSTAL MANUFACTURES (Partial List)

American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Eire, Pennsylvania 16508

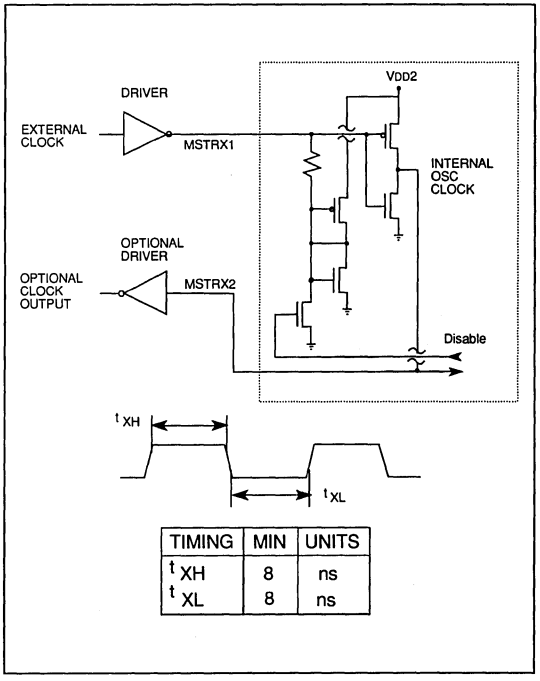
Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626

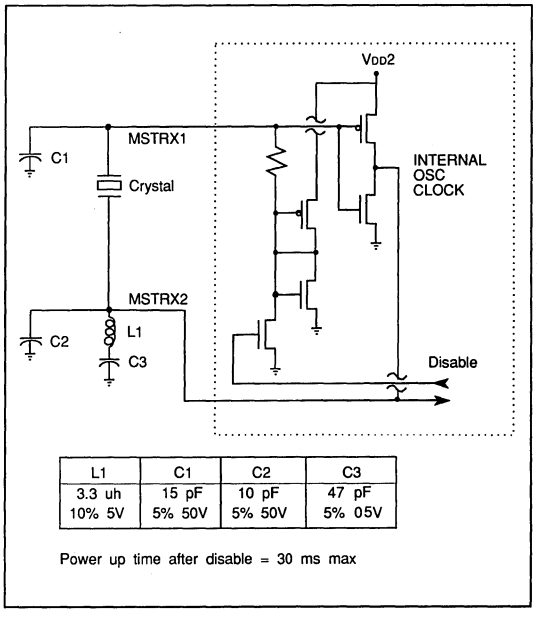
8.1 CRYSTAL SPECIFICATIONS

Series resonant frequency tolerance at 25° C	48.0 MHz ± 50 PPM
Series resonant frequency tolerance at 0° C TO 70° C	48.0 MHz ± 100 PPM
Mode of oscillation	Third over-tone
Adjacent spurious frequency	20 db down, min.
Effective series resistance	80 ohms, max.
Shunt capacitance	5 pf max.
Drive level at room temperature	2000 microwatts
Operating temperature	0° C to 70° C
Insulation resistance	500M ohms/DC100V



TIMING	MIN	UNITS
tXH	8	ns
tXL	8	ns

FIGURE 8-1. EXTERNAL CLOCK INPUT (48 MHz MAX.)



L1	C1	C2	C3
3.3 uh 10% 5V	15 pF 5% 50V	10 pF 5% 50V	47 pF 5% 05V

Power up time after disable = 30 ms max

FIGURE 8-2. TYPICAL CRYSTAL OSCILLATOR NETWORK

APPENDIX - A

A.O WD76C30LV DC ELECTRICAL SPECIFICATIONS

A.1 WD76C30LV MAXIMUM RATINGS

Temperature Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages with respect to Vss ..... -0.1V to +4.5v except for parallel/serial port
-0.5V to +7.0V for parallel/serial port

Power Dissipation ..... 180 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

A.2 CAPACITANCE

Ta = 25°C (77°F), f = 1.0 MHz, VccA = 3.3V, VccB = 3.3V, Vss = 0V

$V_{CC}A$ and $V_{CC}B$ are tied to $V_{DD}2$.

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

TABLE A-1 CAPACITANCE

A.3 DC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to +70°C (158°F), V_{DD} = $V_{DD}2$ = +3.3V ±10%
Vss = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.3	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc +.3	V	
Vil	Input Low Voltage	-0.3	0.8	V	
Vih	Input High Voltage IRQ Mux control	2.0	Vcc +.3	V V	Except MXCTL2-0 MXCTL2-0
Vol	Output Low Voltage		0.4	V	Iol = 2.0 mA on DB0-DB7. Iol = 12 mA on PD0-PD7. Iol = 12 mA on INIT, STB ,SLIN, AFD ① Iol = 2.0 mA on other outputs.
Voh	Output High Voltage Parallel Port Printer Interface	2.4		V	Ioh = -0.4 mA on DB0-DB7. Ioh = 0.5 mA on PD0-PD7. Ioh = -0.55 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, $\overline{SLIN}$. Ioh = -0.2 mA on other outputs.
Icc	Power Supply Current		50	mA	V_{DD} = 5.0V, $V_{DD}2$ = 3.3V MSTRX1 = 48 MHz All other inputs = 3.3V All outputs floating Baud Rate = 512K Serial Port CLK = 8 MHz.
Iil ②	Input Leakage		±15	µA	Vcc = 3.3V, Vss = 0.0V All other pins float.
Icl	Clock Leakage				Vin = 0.0V, 3.3V
Idl	Data Bus Leakage (DB and PD)		±10	µA	Vout = 0.1V, Vout = 3.0V Data Bus in High Impedance State.
Ioz	Tristate Leakage		± 20	µA	Vcc = 3.3V, GND = 0V, Vout = 0.0V, 3.3V
Vil (RES)	$\overline{Reset}$ Schmitt Vil		0.8	V	
Vih (RES)	$\overline{Reset}$ Schmitt Vih	2.0		V	

TABLE A-2. DC OPERATING CHARACTERISTICS

① The $\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{INIT}$ outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. In PS/2 mode $\overline{IRQ7}$ is also an open collector. When in Vol state, each input sinks a minimum of 10 mA.

② $\overline{RESCPU}$, IRQ3 - 7, $\overline{IRQ8}$, IRQ9 - 12, IRQ14 - 15, ROM8, A20GT, KBINT, AND $\overline{CS1}$ have nominally 300 µA pullups. These pullups, along with all others, are disabled when the 48 MHz oscillator is disabled by asserting $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ simultaneously. The pulldowns on KBCLK, ATCLK, and CLK287 are enabled when the three chip selects are low and sink 40 mA min.

WD7910/LP

ISA-Based System Controller with Cache for 80386SX and 80286 Desktop and Portable Compatibles

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The WD7710 is the second generation single chip AT solution based on the WD76C10A core. It is fabricated in 0.9 micron CMOS. The WD7710 provides 8 Kbytes of direct-mapped or two-way set associative lookaside caching, a page-interleaved memory controller, and enhanced power management features. Figure 1-1 shows the block diagram of the WD7710-based system.

The standard version of the WD7710 operates from 5 VDC (±10%) supplies. An extended low-power version, the WD7710LP, can operate with 3.3 VDC (±0.3V) or 5 VDC (±0.5V).

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD7710 and WD7710LP System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD7710 and WD7710LP operate similarly and are referred to in this document as the System Controller. Where there are differences, the devices are identified specifically.

1.2 FEATURES

- Software and pin compatible with WD76C10A
- 8Kbyte on-chip cache for 80386SX
  - Direct map or 2 way set-associative
  - Self timed Integrated RAM arrays
  - Programmable non-cacheable regions
  - Diagnostic mode to test Tag and Data Ram
  - Flush command
  - 25 Mhz zero wait state cache hit
- ROM may be shadowed and/or cached
- Supports Static CPU for power savings in sleep mode
- Supports extra wait state for page mode
- Operates at speeds of 16 MHz, 20 MHz and 25 MHz.
- Interfaces with 80286, or 80386SX CPUs.
- Supports memory in four banks with 64 Kbits, 256 Kbits, 1 Mbits or 4 Mbits DRAMs. Also supports new 512k x 8, 1M x 16 and 2M x 8 DRAM configurations.
- Page mode zero wait state access at 25 MHz with 70 ns DRAM.
- Supports up to 16 Mbyte of real memory, or 32 Mbyte of EMS memory.
- Maintains controlled propagation delay for 80386SX reset.
- Employs an internal self-tuning delay line for DRAM control.
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise.
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and VGA BIOS may be mapped into one physical PROM.
- Advanced 64 Kbyte and 128 Kbyte ROM shadowing allows main BIOS and video BIOS shadowing along with 320 Kbyte and 256 Kbyte remap to extended or expanded memory.
- Offers additional power saving modes:
  - Slow Refresh
  - Stop DMA Clock
- Parity generation and checking.
- 132-pin PQFP package
- 3.3V low power operation
- I/O Pin mapping for testability
- Low power 0.9 micron CMOS technology.

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Additional features of WD7710LP only:

- Provides System Activity Monitor (SAM).
- Provides power control with suspend and resume.
- Provides processor stop clock.
- Features CAS before RAS slow refresh for portable applications.
- Offers automatic processor clock speed switching.
- 3V Suspend to hard disk

1.3 GENERAL DESCRIPTION

The WD7710 is designed for use in a high performance desktop AT computer using an 80286 or 80386SX processor up to 25 MHz. The WD7710LP has the features of the WD7710 and is designed to operate in a high-performance notebook/laptop AT compatible computer using an 80286 or 80386SX processor.

1.3.1 WD7710

The WD7710 contains a high-performance memory controller with programmable modes of operation. It supports non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, 1 Mbit, 4 Mbit or 16 Mbit DRAM may be controlled, allowing up to 16 Mbytes of real or 32 Mbytes EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used. In addition, the WD7710 controls page mode DRAM or static column DRAM with page mode operation.

The on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line information is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

The WD7710 interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power-up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.2 WD7710LP

In addition to supporting all the features of the WD7710, the WD7710LP also supports portable notebook/laptop computers. To provide this support, the WD7710LP makes use of Power Management Control (PMC) for powering down peripherals or the processor, which includes processor stop clock, slow clock, automatic processor clock speed switching modes and CAS before RAS slow refresh. Suspend and resume is supported when low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 5 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

The System Activity Monitor (SAM) provided by WD7710LP is a transparent feature that replaces the functions previously performed by software. It determines when the system has been idle for a previously programmed period of time and determines a clean break point in which to perform powerdown activities such as suspend.

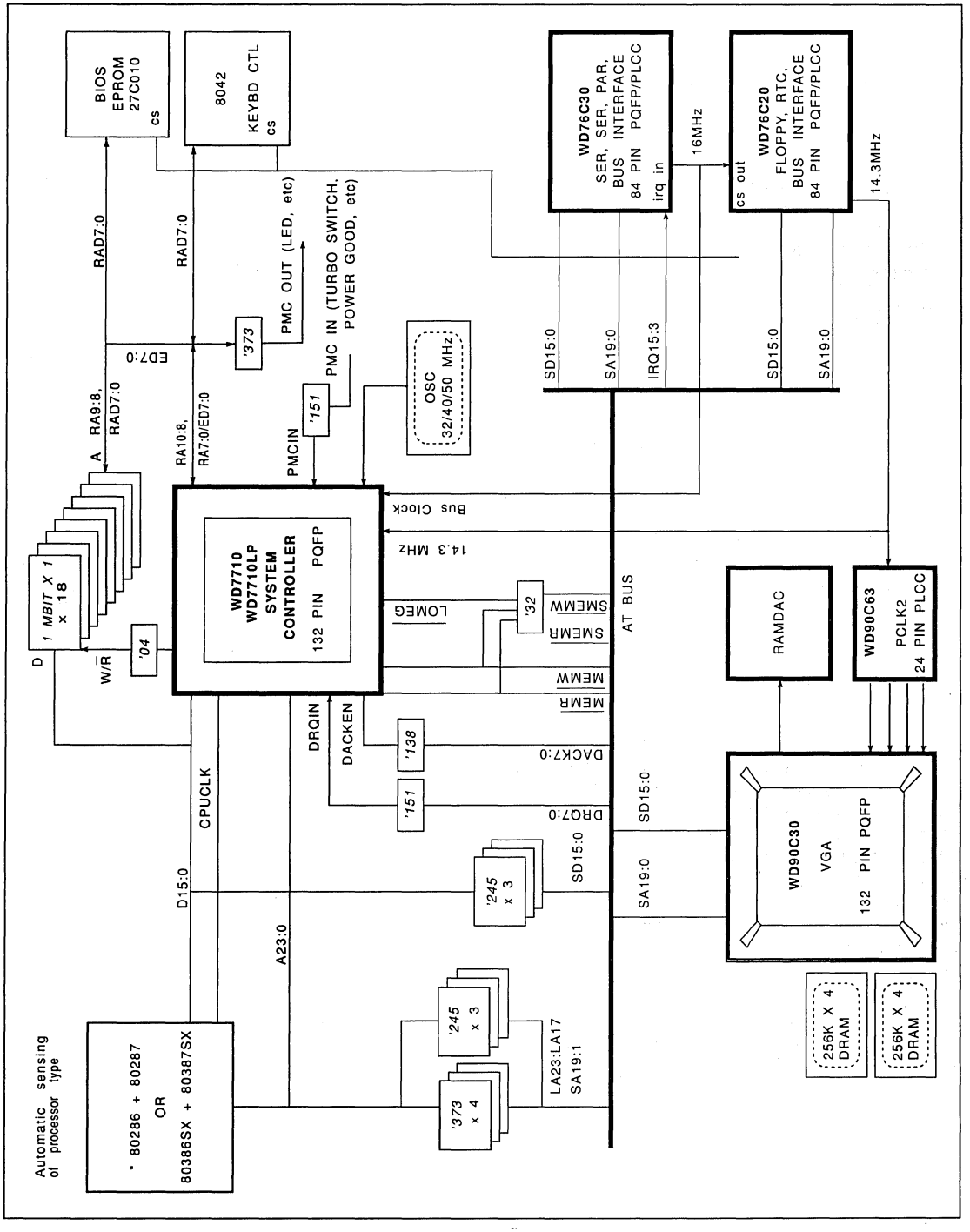

FIGURE 1-1. SYSTEM BLOCK DIAGRAM FOR DESKTOP

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control (WD7710LP only)
- Register File
- Cache control

Sections 2.1 through 2.10 provide an overview of these blocks and are described in more detail in sections 4 through 10.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal, which it uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal. It is at this time that the type of processor in use (80286, 80287 or 80386SX, 80387SX) is determined by examining the S1[W/R#] signal.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the S1[W/R#] signal. This block also controls whether the CPUCLK is to be an input or output. While both devices have the ability to reduce the processor clock rate, only the WD7710LP has the ability to stop the clock to the processor. The WD7710LP also has the ability to power down the processor, at which time it tristates the CPUCLK, READY, HOLD, INTRQ and NMI signals.

2.4 NUMERIC PROCESSOR CONTROL

Both System Controllers support an 80287 or 80387SX processor.

2.5 DATA BUS

The Data Bus is a 16-bit (two bytes) bidirectional bus that connects to the processor's, System Controller, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory. Both versions of the System Controller supports non-page mode memory and independent two-way interleave page mode access to the DRAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD7710LP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD7710LP tristates the CPUCLK, READY, HOLD, INTRQ and NMI output signals to the main processor. Also contained within this functional block are the SMI and SAM logic.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port 1872H, serve more than one area. In this instance the register description appears only in one section but is referred to in all appropriate sections.

The registers, and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15. through A00. Within the text, when the address is expressed as a three digit number, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072H and E872H and Port 70H Shadow Register at E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72H - Read only

Bits 11 through 03 are particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
T	Not Used			DMA #2			
				CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1				P4	Not Used		
CH3	CH2	CH1	CH0				

Signal Name — **Default At RSTIN**

All signals . . . . . None

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bit 03 - P, Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, section 4.3

Bits 02-00 - Not used, state is ignored

2.8.2 Lock/Unlock Register

Port Address F073H - Write only

15	14	13	12	11	10	09	08
Not Used							

07	06	-5	04	03	02	01	00
L/UL = DA-							

Signal Name	Default At RSTIN
All signals	None

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -
11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -
Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

2.9 Cache Control

This functional block contains the 8Kbyte integrated cache (both tag and data RAM) as well as cache control logic.

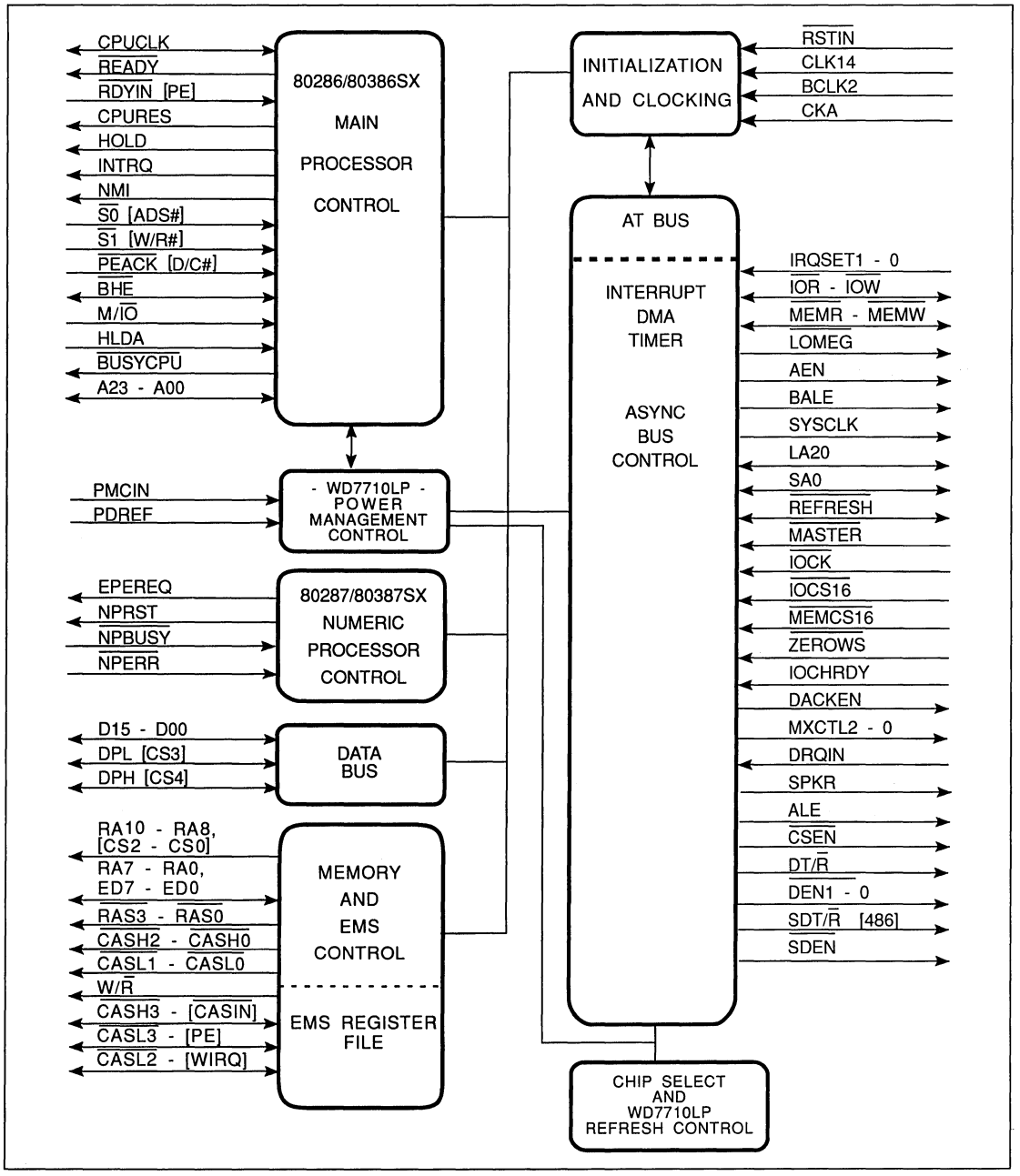

FIGURE 2-1. WD7710 AND WD7710LP BLOCK DIAGRAM

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	8.5, Table 8-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real-Time Clock Address Register	No	5.8.1
071 - 07F odd	Real-Time Clock Data Register	No	5.8.2
080 - 09F	(except 092H) DMA Page Registers	No	5.6.4
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	Clear 287 Busy	No	5.3.2
00F1	Reset 287/387SX	No	5.3.3
1072	CPU Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	8.1
2872	Chip Selects	Yes	8.2
3072	Programmable Chip Select Address	Yes	8.3
3872	Memory Control	Yes	6.2.1
3C72	DMA Shadow Register 1	Yes	9.14
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4472	DMA Shadow Register 2	Yes	9.14
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
4C72	DMA Shadow Register 3	Yes	9.14
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
5C72	Reserved		
6072	RAM Shadow And Write Protect	Yes	6.2.4
6472	Reserved		
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
6C72	Reserved		
7072	PMC Output Control 7:0	Yes	9.3
7472	Reserved		
7872	PMC Output Control 15:8	Yes	9.3
7C72	Reserved		
8072	PMC Timers	Yes	9.4
8872	PMC Inputs 7:0	Yes	9.5
8C72	Reserved		
9072	NMI Status	Yes	9.7
9472	Reserved		
9872	Diagnostic	Yes	10.1
9C72	Reserved		
A072	Delay Line	Yes	10.2

TABLE 2-1. REGISTER INDEX

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
A472	Reserved		
A872	Test Enable	Yes	10.3
AC72	Reserved		
B072	Activity Monitor Control	Yes	9.11
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	9.6
D072	Serial/Parallel Shadow Register	Yes	9.8
D472	Interrupt Controller Shadow	Yes	9.9
D872	Activity Monitor Mask	Yes	9.12
DC72	Test Status	Yes	10.4
E072	EMS Page Register Pointer	No	6.4.2
E472	Port 70H Shadow	No	9.10
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	8.5, Table 8-1
F472	48 MHz Oscillator Enable	Yes	8.5, Table 8-1
F872	Cache Flush	Yes	8.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	No	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX (cont.)

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3.0 SIGNAL DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	RA5/ED5	34	EPEREQ	67	VSS	100	A10
2	VCC	35	NPRST	68	D11	101	VCC
3	RA4/ED4	36	LOMEG	69	VCC	102	A9
4	RA3/ED3	37	MEMW	70	D12	103	A8
5	VSS	38	MEMR	71	D13	104	A7
6	RA2/ED2	39	IOW	72	D14	105	A6
7	RA1/ED1	40	IOR	73	D15	106	A5
8	RA0/ED0	41	BHE	74	DT/R	107	A4
9	CASH2	42	NPERR	75	DEN1	108	A3
10	CASL2 [WIRQ]	43	PEACK [D/C]	76	DEN0	109	A2
11	RAS2	44	M/IO	77	SYSCLK	110	IRQSET1
12	CASH3 [CASIN]	45	S0 [ADS#]	78	CPURES	111	IRQSET0
13	CASL3 [PE]	46	S1 [W/R#]	79	BALE	112	MXCTL0
14	RAS3	47	READY	80	A23	113	MXCTL1
15	DPH [CS4]	48	HLDA	81	A22	114	MXCTL2
16	DPL [CS3]	49	HOLD	82	A21	115	CSEN
17	RSTIN	50	BCLK2	83	IOCK	116	DACKEN
18	DRQIN	51	RDYIN [CKA] [PE]	84	CLK14	117	PDREF
19	IOCHRDY	52	CPUCLK	85	NPBUSY	118	PMCIN
20	ZEROWS	53	BUSYCPU	86	A0 [BLE#]	119	W/R
21	IOCS16	54	NMI	87	A1	120	CASH0
22	MEMCS16	55	INTRQ	88	A20	121	CASL0
23	SPKR	56	D0	89	A19	122	RAS0
24	SA0	57	D1	90	A18	123	CASH1
25	LA20	58	D2	91	A17	124	CASL1
26	MASTER	59	D3	92	A16	125	RAS1
27	ALE	60	D4	93	A15	126	RA10 [CS2]
28	AEN	61	D5	94	A14	127	RA9 [CS1]
29	SDEN	62	D6	95	A13	128	RA8 [CS0]
30	SDT/R [486]	63	D7	96	A12	129	VSS
31	VCC	64	D8	97	A11	130	RA7/ED7
32	REFRESH	65	D9	98	VSS	131	RA6/ED6
33	VSS	66	D10	99	VSS	132	VSS

Note: Some pins are multi-functional depending upon the mode of operation. The alternate signal for these pins is enclosed in brackets.

TABLE 3-1. PIN ASSIGNMENTS

PIN	MNEMONIC	I/O	DESCRIPTION
			INITIALIZATION AND CLOCKING
84	CLK14	I	**Clock 14** CLK14 is derived from a 14.318 MHz crystal and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
17	$\overline{\text{RSTIN}}$	I	**System Reset In** $\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at powerup. For a detailed description, see Section 4, Initialization and Clocking.
50	BCLK2	I	**Bus Clock** BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock.
			AT BUS
110	IRQSET1	I	**Interrupt Request Set 1** IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
111	IRQSET0	I	**Interrupt Request Set 0** IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, $\overline{\text{RESCPU}}$, IRQ8, IRQ9 - IRQ11, IRQ14 and IRQ15. Refer to Table 5-1 and Figure 5-1.
114-112	MXCTL2:0	O	**Multiplexer Control 2-0** MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0 and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and $\overline{\text{RESCPU}}$. Refer to Table 5-1 and Figure 5-1.
115	$\overline{\text{CSEN}}$	O	**Chip Select Enable** When $\overline{\text{CSEN}}$ is asserted, DPH, DPL, and RA10-RA8 are used to generate one of 28 different chip selects. Refer to Table 8-1.
116	DACKEN	O	**DACK Enable** When DACKEN is asserted, MXCTL2-0 are used to generate DACK7-5, 3-0 and BUS_RST. Refer to Table 5-1 and Figure 5-1.
18	DRQIN	I	**Multiplexed DRQ Inputs** DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1
19	IOCHRDY	I/O	**I/O Channel Ready** Indicates extra wait states are required for the AT bus cycles.

TABLE 3-2. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
20	$\overline{\text{ZEROWS}}$	I	**Zero Wait States** Indicates the current AT bus cycle can be finished in zero wait state.
21	$\overline{\text{IOCS16}}$	I	**16-Bit I/O Cycle** Inicates the I/O device on the AT bus is a 16-bit slave.
22	$\overline{\text{MEMCS16}}$	I	**16-Bit Memory Cycle** Indicates that the memory device on the AT bus is a 16-bit slave.
23	SPKR	O	**Speaker** SPKR drives the speaker transistor.
24	SA0	I/O	**System Address 0** When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line.When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.
25	LA20	I/O	**Early Address 20** When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
26	$\overline{\text{MASTER}}$	I	**Master** $\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to be selected as input signals.
27	ALE	O	**Address Latch Enable** ALE is used to clock the SA1 - SA19 address latches.
28	AEN	O	**Address Enable** AEN is asserted by the System Controller while performing DMA and Refresh cycles.
29	$\overline{\text{SDEN}}$	O	**Swap Data Enable** $\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.

TABLE 3-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
30	SDT/$\overline{R}$	I/O	**Swap Data Transmit/Receive [80486]** SDT/$\overline{R}$ controls the direction of the buffer between the low byte and high byte of the AT bus. SDT/$\overline{R}$ is tristated by a 50K pullup resistor internal to the WD7910 when $\overline{RSTIN}$ at pin 80 is low. **SDT/$\overline{R}$ Mode - Output** When SDT/$\overline{R}$ is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{R}$ is low, it directs data from the high byte of the AT bus to the low byte. Forcing SDT/$\overline{R}$ high while $\overline{RSTIN}$ is low selects the SDT/$\overline{R}$ mode. Holding SDT/$\overline{R}$ high as $\overline{RSTIN}$ goes high maintains the SDT/$\overline{R}$ mode. **80486 Mode - Input** Selecting 80486 mode sets the SRC bit in Port 1072H to 1. This causes $\overline{RDYIN}$ at Pin 51 to be the default processor clock source input. Forcing SDT/$\overline{R}$ low while $\overline{RSTIN}$ is low selects the 80486 mode. holding SDT/$\overline{R}$ low as $\overline{RSTIN}$ goes high, maintains the 80486 mode. SDT/$\overline{R}$ pin may be forced low at reset with a 5K pulldown resistor or an open collector or tristate driver driven by $\overline{RSTIN}$.
32	$\overline{REFRESH}$	I/O	**Refresh** As an output, $\overline{REFRESH}$ is asserted by the System Controller to refresh memory on the AT Bus. As an input, $\overline{REFRESH}$ is asserted by the Bus Master in conjunction with $\overline{MEMR}$ to refresh memory on the AT Bus and DRAM controlled by the System Controller.
36	$\overline{LOMEG}$	O	**First Megabyte** $\overline{LOMEG}$ is asserted when the AT bus address is below 1 Mbyte.
37	$\overline{MEMW}$	I/O	**Memory Write** $\overline{MEMW}$ is an output and it is asserted by the System Controller when a memory write access to the AT bus is to take place. It is an input during Master mode.
38	$\overline{MEMR}$	I/O	**Memory Read** $\overline{MEMR}$ is an output and it is asserted by the System Controller when a memory read access to the AT bus is to take place. It is an input during Master mode.
39	$\overline{IOW}$	I/O	**I/O Write** $\overline{IOW}$ is an output and it is asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. $\overline{IOW}$ is an input during Master Mode.
40	$\overline{IOR}$	I/O	**I/O Read** $\overline{IOR}$ is an output and iit s asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. $\overline{IOR}$ is an input during Master Mode.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
74	DT/$\overline{R}$	O	**Data Transmit/Receive** DT/$\overline{R}$ controls the direction of the AT Data Bus D00 through D15. When DT/$\overline{R}$ is high, data is directed to the AT Bus. When DT/$\overline{R}$ is low, data is transferred from the AT bus.
75	$\overline{DEN1}$	O	**Data Bus Enable 1** When asserted, $\overline{DEN1}$ enables the high order byte data buffer.
76	$\overline{DEN0}$	O	**Data Bus Enable 0** When asserted, $\overline{DEN0}$ enables the low order byte data buffer.
77	SYSCLK	O	**System Clock** In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.
79	BALE	O	**AT Bus Address Latch Enable** Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
83	$\overline{IOCK}$	I	**I/O Channel Check** When asserted, $\overline{IOCK}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
			MAIN PROCESSOR CONTROL
4	$\overline{BHE}$	I/O	**Bus High Enable** As an input, $\overline{BHE}$ indicates a transfer of the high byte on the processor data bus. $\overline{BHE}$ is an output during DMA transfers.
43	PEACK [D/C#]	I	**Processor Extension Acknowledge [Data Control]** In the 80286 mode, pin 43 is PEACK. in the 80386SX mode, pin 43 is D/C#.
44	M/IO	I	**Memory or I/O** Processor Memory cycle or $\overline{I/O}$ Status cycle.
45	$\overline{S0}$ [ADS#]	I	**Processor Status 0 [Address Status]** In the 80286 mode pin 45 is $\overline{S0}$. in the 80386SX mode, this pin 45 is ADS#.
46	$\overline{S1}$ [W/R#]	I	**Processor Status 1 [Write/Read]** In the 80286 mode, pin 46 is S1. In the 80386SX mode, pin 46 is W/R#.
47	$\overline{READY}$	O	**Processor Ready** $\overline{READY}$ is an output to the processor
48	HLDA	I	**Hold Acknowledge** Processor hold acknowledge.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
49	HOLD	O	**Hold Request** Processor hold cycle request.
51	RDYIN/CKA/PE	I	**Processor Ready In / Alternate Clock / Parity Error** The Memory Control Register at port address 3872H determines whether pin 51 is to be used as $\overline{\text{RDYIN}}$, CKA or PE. $\overline{\text{RDYIN}}$ is used in a discrete cache system to indicate a hit or miss. CKA is used as a source for the CPU clock. PE indicates a parity error from an external memory controller
52	CPUCLK	I/O	**Processor Clock** CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at Port Address 1072H. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.
54	NMI	O	**Non-maskable Interrupt** Processor non-maskable interrupt cycle request.
55	INTRQ	O	**Interrupt Request** Processor interrupt cycle request.
78	CPURES	O	**Main Processor Reset** CPURES is a synchronous processor reset signal.
80 - 82 88 - 97 100 102 - 109 87 86	A23:A21 A20:A11 A10 A9:A2 A1 A0 [BLE#]	I/O	**Processor Address A23-A00 [Bus Low Enable]** A23 through A1 are address lines from the 80286 or 80386SX. A0 is address bit A0 for the 80286, BLE# for the 80386SX. A0 is controlled by SA0 (AT bus pin 24) during Master Mode operations. A21, A19 through A1 are outputs during refresh and DMA cycles; they are inputs in other modes. A20 and A0 are outputs during refresh, DMA and Master Mode cycles; they are inputs in other modes.
NUMERIC PROCESSOR CONTROL			
85	$\overline{\text{NPBUSY}}$	I	**Numeric Processor Busy** Busy signal from the numeric processor 80287 or 80387SX.
34	EPERQ	O	**Extend PERQ** PERQ extend signal to the 80386SX for IRQ13 handling. Used only for the 80386SX.
35	NPRST	O	**Numeric Processor Reset** Reset to the numeric processor 80287 or 80387SX.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
42	$\overline{\text{NPERR}}$	I	**Numeric Processor Error** Error signal from the numeric processor 80287 or 80387SX.
53	$\overline{\text{BUSYCPU}}$	O	**Coprocessor Busy** Coprocessor Busy signal to the processor.
			DATA BUS
15	DPH[CS4]	I/O	**Data Parity High Byte [Chip Select 4]** For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.
16	DPL[CS3]	I/O	**Data Parity Low Byte [Chip Select 3]** For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.
73 - 70 68 66 - 56	D15 - D12 D11, D10 - D0	I/O	**Data Bits 15 through 0** The Data Bits are connected directly to the Local and Numeric processors, DRAM data and AT Bus data transceivers.
			MEMORY AND EMS CONTROL
119	W/$\overline{\text{R}}$	O	**Write /Read** W/$\overline{\text{R}}$ is high when writing to memory and low when reading from memory. W/$\overline{\text{R}}$ should be buffred before use.
126 127 128	RA10/CS2 RA9/CS1 RA8/CS0	O	**DRAM Address Bits 11 through 8** **Chip Select Bits 2 through 0** The DRAM Address Bus is multi-functional. During DRAM cycles, RA11 through RA0 select the DRAM row and column.
130 131 1 3 4 6 7 8	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	I/O	**DRAM Address Bits 7 through 0** **EDATA Bits 7 through 0** During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.
14 11 125 122	$\overline{\text{RAS3}}$ thru $\overline{\text{RAS0}}$	O	**Row Address Select Bits 3 through 0** $\overline{\text{RAS3}}$ through $\overline{\text{RAS0}}$ are designed to access the DRAM without the use of external drivers.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
12	CASH3 [CASIN]	I/O	**Column Address Select High 3 through 0** CASH3 [CASIN] is tristated by a 50K pullup resistor internal to the WD7710 when RSTIN at pin 17 is low.
9	CASH2	O	
123	CASH1	O	**CAS Output Mode** CASH3 through CASH0 operate as output signals and are designed to access the DRAM without the use of external drivers. Forcing CASH3[CASIN] high while RSTIN is low, selects the CASH3 Output Mode. Holding CASH3[CASIN] high as RSTIN goes high, maintains the CASH3 Output Mode.
120	CASH0	O	**CAS Input Mode** In this mode, pins 12, 13 and 10 function as input pins controlled by CASIN, PE and WIRQ. CASH2, CASH1, and CASH0 remain output signals. Forcing CASH3 [CASIN] low while RSTIN is low, selects the CAS Input Mode. Holding CASH3 [CASIN] low as RSTIN goes high, maintains the CAS Input Mode. The CASH3 [CASIN] pin may be forced low at reset with a 5K pulldown resistor or an open collector or tristate driver driven by RSTIN.
13	CASL3 [PE]	I/O	**Column Address Select Low 3 [Parity Error}**
10	CASL2 [WIRQ]	I/O	**Column Address Select Low 2 [Weitek Interrupt]**
124	CASL1	O	**Column Address Select Low 1 and 0**
121	CASL0	O	**CAS Output Mode** CASL3 through CASL0 are designed to access the DRAM without the use of external drivers. **CAS Input Mode - PE** When CAS Input Mode is selected by [CASIN] on pin 12, and bits 13 and 12 of Port 3872H are both 1, pin 13 becomes an input and represents a parity error. A parity error is indicated by the low to high transition of the PE signal. **CAS Input Mode - WIRQ** When CAS Input Mode is selected by [CASIN] on pin 12, pin 10 becomes an interrupt signal which is typically connected to IRQ13, the error signal of a Weitek coprocessor. When WIRQ goes from low to high, an IRQ 13 is generated to the system.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
			POWER MANAGEMENT CONTROL
117	NPDREF	I	**Power-down Refresh** NPDREF is a 64 KHz signal from the WD7710. During power-down, NPDREF is passed internally to pin 98 (REFRESH).
118	PMCIN	I	**Power Management Control Input** PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
			MISCELLANEOUS
5, 33, 67, 98, 99, 129, 132	VSS	I	**Ground**
2, 31, 69, 101	VCC	I	**+5 Volts**

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, NRSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor. At this time the System Controller also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which are decoded externally as BUS_RST (DACK4), see sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the System Controller enters the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD7710 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds higher than 50 MHz, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872H. The PMC control output 0 tristates the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by SCHH or SCH (CPU Clock Control Register - bits 01 or 00, at Port Address 1072H) or divided down by CLK_SPD (bits 14-12). Only the WD7710LP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle. The other method can be used when the CPUCLK is an

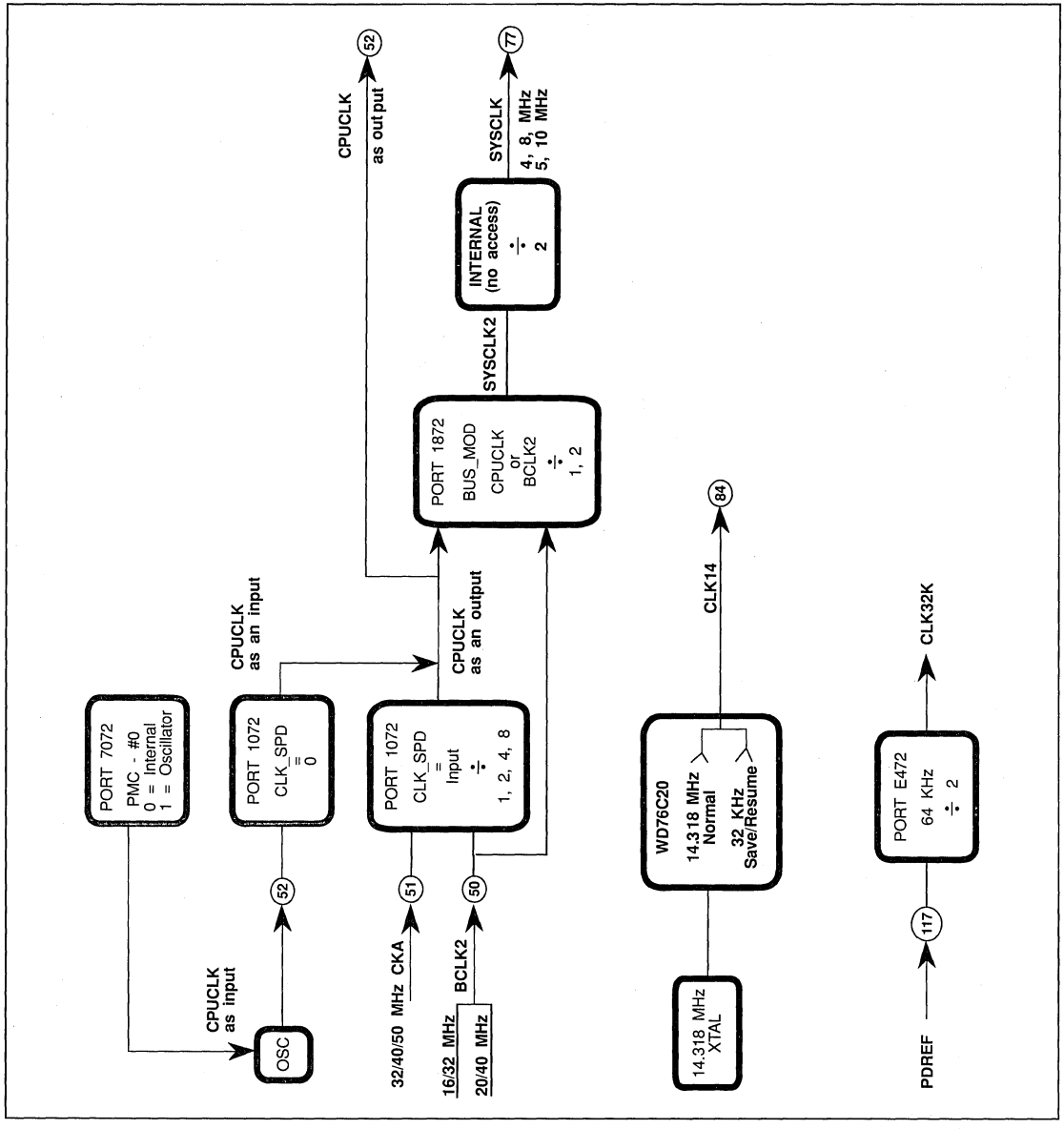

FIGURE 4-1. CLOCK CONTROL

output or input and generated by an external oscillator. In this case, EXT_HOLD is used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is determined by SRC (CPU Clock Control Register bit 15 at Port Address 1072H). SRC is set automatically at power up reset, if a clock source is present at pin 51 (CKA).

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072H - Read and Write

15	14	13	12	11	10	09	08
SRC	CLK_SPD			AUT_ FST	ALT_CLK_SPD		

07	06	05	04	03	02	01	00
EXT_HOLD						SCHH	SCH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	000/001
AUT FST †	0
ALT CLK SPD †	000
EXTEND HOLD	0000
Bits 03, 02	None
SCH †	0
SCHH †	0

† Featured only in the WD7710LP

Bit 15 - SRC, CPUCLK Clock Source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

Default Value

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state within 64 clocks after $\overline{RSTIN}$ is de-asserted.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after $\overline{RSTIN}$ is de-asserted, or when operating in the 80486 Mode. The 80486 Mode is selected by holding SDT/$\overline{R}$ low during $\overline{RSTIN}$ transition from low to high.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK Clock Speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD *defaults to 000 or 001 at power up. Changing the CPUCLK from an input (CLK_SPD = 000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One millesecond later, CPUCLK becomes active as an output. One millesecond and 16 CPUCLK clocks (or one millesecond) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated due to the clock driver not being able to synchronously switch the clock. The one millesecond and 16 clocks or one millesecond selection is made through the Diagnostic Register at Port 9872H.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source (* Default value).
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (* Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

* Based upon the value of CLOCK_DIR_IN at power up (refer to Table 5-1, Figure 5-1 and section 5.1.2).

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Bit 11 - AUT_FST, Automatic Processor Clock Speed Switching
Featured only in the WD7710LP

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-2. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-2 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-1 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-1. The EXT_HOLD field must be 0000 when AUT_FST = 1.

TURBO	AUTO_FST	CPU CLOCK SPEED
0	0	CLK_SPD
0	1	CLK_SPD
1	0	ALT_CLK_SPD
1	1	CLK_SPD or ALT_CLK_SPD

TABLE 4-1. CLOCK SWITCH SELECTION

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access or processor reset	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-2. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate Clock Speed
Featured only in the WD7710LP

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value).

0 0 1 - Equals source.

0 1 0 - Equals source div by 2.

0 1 1 - Equals source div by 4, 25% duty cycle.

1 0 0 - Equals source div by 4, 75% duty cycle.

1 0 1 - Equals source div by 8, 12% duty cycle.

1 1 0 - Equals source div by 8, 88% duty cycle.

Bits 07-04 - EXT_HOLD, Extend Processor Hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external TURBO signal is asserted, EXT_HOLD is forced to 0000. When the external TURBO signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value).

0 0 0 1 - 1 µs hold after refresh.

0 0 1 0 - 2 µs hold after refresh.

0 0 1 1 - 3 µs hold after refresh.

0 1 0 0 - 4 µs hold after refresh.

↕

1 1 0 1 - 13 µs hold after refresh.

1 1 1 0 - 14 µs hold after refresh.

1 1 1 1 - 15 µs hold after refresh.

Bits 03-02 - Reserved for future use, must be set to zero

Bit 01 - SCHH, Stop CPUCLK at next Halt and Hold.
Featured only in the WD7710LP

SCHH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7710LP rather than an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate selected by the Refresh Control Register at Port 2072H.

SCHH = 0 -
Normal processor clock (default value).

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

Bit 00 - SCH, Stop CPUCLK at next Hold
Featured only in the WD7710LP

SCH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7910LP instead of an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate as selected by the Refresh Control Register at Port 2072H.

SCH = 0 -
Normal processor clock (Default value).

SCH = 1 -
Stop processor clock at next processor hold cycle.

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5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8) and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external 74F138, 3 to 8 Decoder for desktop systems, or 74ACT138, 3 to 8 Decoder for laptop systems, uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 74F151, 8 to 1 Multiplexer for desktop systems, or 74ACT151, 8 to 1 Multiplexer for laptop systems, to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1. This controls the default value of CLK_SPD in the CPU Clock (CPUCLK) Control Register at Port 1072H. See section 4.2.4.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA, DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{NRSTIN}$ to determine ROM data width (ROM8). The $\overline{RESCPU}$ and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus And Terminal Count (TC) Signal

The AT Address Bus SA19-00 and $\overline{NBLE}$ are generated from A19-00 with external latches and tristate buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and $\overline{CSEN}$ are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD7910, the $\overline{TURBO}$ signal may be connected directly to PMCIN. In the WD7710LP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{\text{IRQ8}}$	IRQ12	$\overline{\text{TURBO}}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	$\overline{\text{RESCPU}}$	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

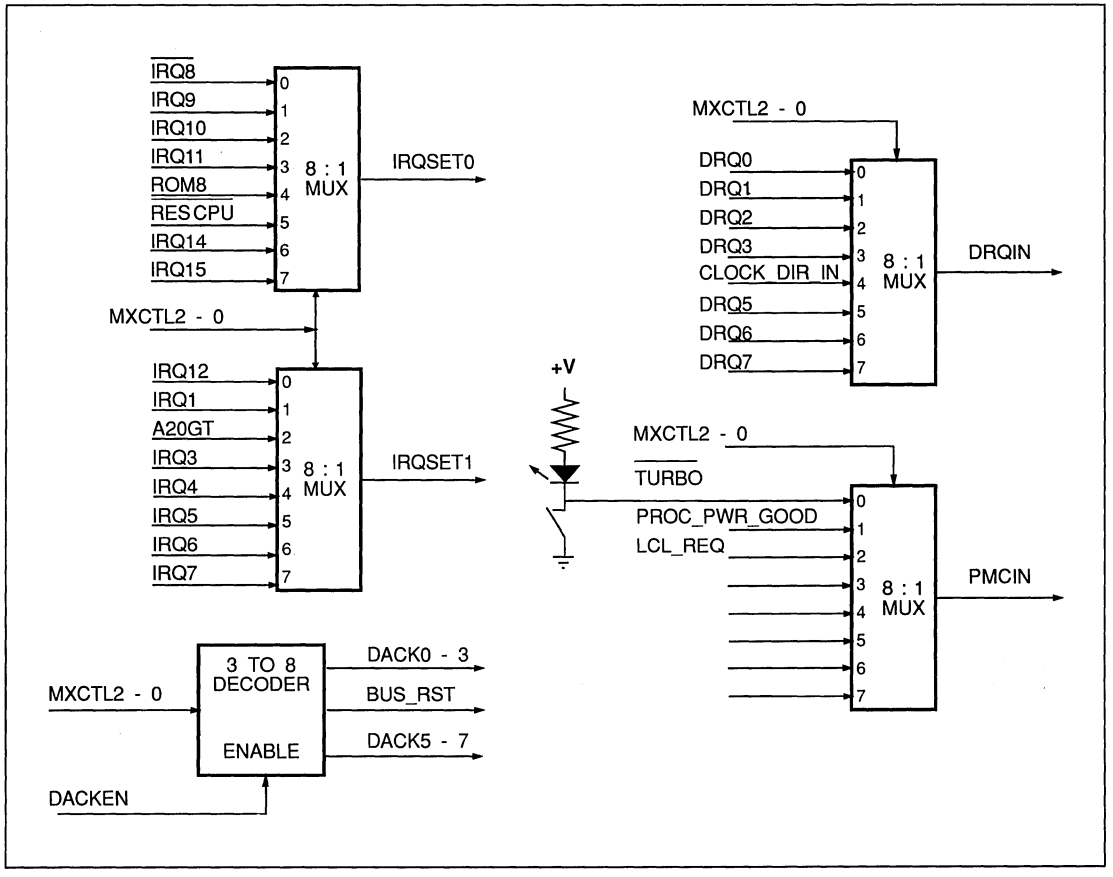


FIGURE 5-1. MXCTL2-0 MULTIPLEXING

5.3 NUMERIC PROCESSOR

5.3.1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872H - Read and Write

15	14	13	12	11	10	09	08
NP_ BSY	PRO_ PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI 16	WSM_ 16	WSI8		WSM8	

Signal Name	Default At RSTIN
NP_BSY	0
PRO_PD †	0
Bit 12	None
FPD †	0
BUS_MOD	00
BRQ_DEL	00
BAK_DEL	11
WSI_16	0
WSM_16	0
WS18	10
WSM8	10

† Featured only in the WD7710LP

Bit 15 - NP_BSY, Numeric Processor Busy

NP_BSY must be set for systems using an 80286 CPU where the CPU runs faster than the AT bus. The causes BUSYCPU to be asserted early during any CPU write to I/O ports F8H through FFH. BUSYCPU is de-asserted at the end of the I/O write if the coprocessor has not asserted its own NPBUSY by this time. Early assertion of BUSYCPU is necessary to prevent a loss of synchronization between the 80286 and 80287. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Force an early BUSYCPU for I/O writes to coprocessor addresses F8H through FFH. (Default value).

NP_BSY = 1 -
Normal BUSYCPU assertion.

Bit 14 - PRO_PD, Processor Power Down
Featured only in the WD7710LP

When PRO_PD has been changed from zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated at the next Halt State and the expansion bus will continue to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD7710LP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power (Default value).

PRO_PD = 1 -
Start processor power down sequence.

Bit 13 - FPD, Full Powerdown
Featured only in the WD7710LP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except NRSTIN, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Powerdown) from Port 7072H is set. This enables the powering down of all chips except DRAM, WD7710LP, WD76C20, WD76C30 and WD90C20. The WD76C20 provides NPDREF

(a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the REFRESH signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at Port 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port 8872H input is high. The tristated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus Mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

- 0 0 - Bus logic uses BCLK2 divided by 2 (Default value).
- 0 1 - Bus logic uses BCLK2 divided by 1.
- 1 0 - Bus logic uses CPUCLK divided by 2.
- 1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

- 0 0 - 1 Bus clock delay (Default value).
- 0 1 - .5 Bus clock delay.
- 1 0 - No clock delay.
- 1 1 - Reserved.

Bits 07, 06 - BAK_DEL, Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

- 0 0 - No delay.
- 0 1 - -.5 Bus clock delay.
- 1 0 - -1 Bus clock delay.
- 1 1 - +.5 Bus clock delay (Default value)

Bit 05 - WSI16, Wait State for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state (Default value).

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait State for 16 bit Memory

WSM16 = 0 -
1 Bus clock wait state (Default value).

WSM16 = 1 -
2 Bus clock wait state.

Bits 03, 02 - WSI8, Wait State for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

Bits 01, 00 - WSM8, Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

5.3.2 Numeric Processor Busy (NPBUSY) Reset

Port Address 0F0H - Write only

Writing any data to this port resets the 80287 busy signal (de-asserts NPBUSY). The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H - Write only

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	8 MHz	ASYNC	0X	01	01
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	00
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA Controller 1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA Controller 2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA Controller 2 is used to cascade DMA controller #1. Table 5-4 indentifies the Controller/-Channel location and function.

AT BUS DMA CHANNEL	DMA CONTROLLER	TRANSFER TYPE
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

Single Transfer Mode - 01

In single transfer mode, the channel makes one transfer for each request. The word count is decremented, and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the $\overline{MASTER}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or MEMW signals.

Write - 01

A write transfers data from an I/O device to memory.

Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address Hex	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
080-09F			DMA Page Register
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008H, 0D0H - Write only

The Command Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

Signal Name	Default At RSTIN
All signals	0

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008H, 0D0H - Read only

Bits 3-0 are reset by $\overline{\text{NRSTIN}}$, writing any data to Port Address 00DH or 0DAH (see section 5.4.14) or when read by a Status Read Command.

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0 TC

Signal Name	Default At RSTIN
CH3_DRQ - CH0_DRQ	None
CH3_TC - CH0_TC	0

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009H, 0D2H - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
					CRQ	CH#	

Signal Name	Default At RSTIN
All signals	0

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	0 - Channel 0
0	1	1 - Channel 1
1	0	0 - Channel 2
1	1	1 - Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a $\overline{\text{RSTIN}}$, or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H - Write only

7	6	5	4	3	2	1	0
					SE_ MA	CH#	

Signal Name	Default At RSTIN
All signals	1

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH - Write only

Writing any data to this register resets all Masks. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH - Write only

7	6	5	4	3	2	1	0
				CH3_ MA	CH2_ MA	CH1_ MA	CH0_ MA

Signal Name	Default At RSTIN
All signals	1

Bits 7-4 - Not used, state is ignored

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00BH, 0D6H - Write only

This register selects the mode and type of transfer for each channel. Refer to sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_ MOD		AD_ DEC	AUTO	TRA_ TYP		CHA# SEL	

Signal Name	Default At RSTIN
All signals	None

Bits 7, 6 - TRA_MOD, Transfer Mode

TRA_MOD 7	6	
0	0	- Demand
0	1	- Single
1	0	- Block
1	1	- Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP 3	2	
0	0	0 - Verify
0	1	1 - Write
1	0	0 - Read
1	1	1 - Not used

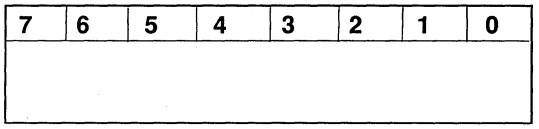
Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL 1	0	
0	0	0 - Channel 0
0	1	1 - Channel 1
1	0	0 - Channel 2
1	1	1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H - Write only

Each DMA controller has a pointer flip-flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip-flop is reset, bits 7-0 are accessed, and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see section 5.4.14). In either case, the data is ignored.



Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

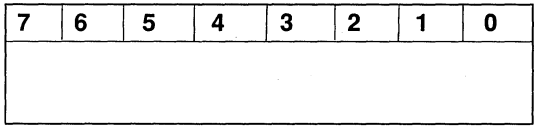
5.4.14 Master Clear Rgister

Port Addresses 00DH, 0DAH - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.



Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.15 DMA Mode Shadow Register

Port Address B872H - Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt Controller 1 is in the I/O space of 020H to 021H and Interrupt Controller 2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of Interrupt Controller 1 is used to cascade Interrupt Controller 2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	RTC
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

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6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

Interrupt Controller	Address Hex	Function	Read/write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Signal Name	Default At RSTIN
All signals	None

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1

Bit 3 - L_T, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bit 2 - I2 H_L, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

Port Addresses 0A1H - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H - Write only

A Slave does not have ICW4.

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Not Special Fully Nested Mode

S F N M = 1 -
Special Fully Nested Mode

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT 7	6	5	
0	0	0	- Clear Rotate On Automatic EOI
0	0	1	- Non-specific EOI
0	1	0	- Not used
0	1	1	- Specific EOI
1	0	0	- Set Rotate on Automatic EOI
1	0	1	- Rotate on Non-Specific EOI
1	1	0	- Set Priority
1	1	1	- Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV 2	1	0	
0	0	0	- Interrupt Level 0
	↕		
1	1	1	- Interrupt Level 7

5.5.3.3 OCW3

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ISR	

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM 6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 -
No Poll Command

P_C = 1 -
Poll Command

Bits 1-0 - IRR_ISR, Interrupt Request Register and Interrupt Service Register

IRR_ISR 1	0	
0	0	- Not used
0	1	- Not used
1	0	- Read Interrupt Request Register
1	1	- Read Interrupt Service Register

5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O ADDRESS	USE	READ/ WRITE
040H	Timer 0 Count/Status	Read/Write
041H	Timer 1 Count/Status	Read/Write
042H	Timer 2 Count/Status	Read/Write
043H	Control Word	Write

TIMER CHANNEL	USE
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

ADDRESS 9	8	7	6	5	4	3	2	1	0	DECODES	HEX
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PIO)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real-Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real-Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092H)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087H	DMA Channel 0
0083H	DMA Channel 1
0081H	DMA Channel 2
0082H	DMA Channel 3
008BH	DMA Channel 5
0089H	DMA Channel 6
008AH	DMA Channel 7
008FH	Refresh

TABLE 5-9. PAGE REGISTER DECODES

NOTE

Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

5.8 NMI AND REAL TIME CLOCK

5.8.1 Real Time Clock Address Register

Port Address 070H-07EH even - Write only

There is only one RTC Address Register. All even number addresses from 070H through 07EH access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
RTC6 - RTC0	None

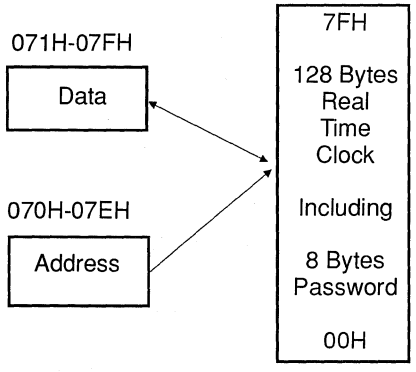
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real-Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real-Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071H-07FH.



5.8.2 Real-Time Clock Data Register

Port Address 071H-07FH odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071H through 07FH access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to section 7.2).

7	6	5	4	3	2	1	0
Real-Time Clock Data							

5.8.3 Lock Pass, Alternate A20G And Hot Reset

Port Address 092H - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
Bits 7-4, 2	None
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by NRSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

Bit 0 - HOT_RST, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Port Address 061H- 06FH odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

Odd numbered Port Addresses 061H through 06FH provide access to parity error and I/O Channel Check of the expansion bus.

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity Error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O Channel Check from the expansion bus (read only)

IOCK = 0 -
No I/O Channel Check Error

IOCK = 1 -
I/O Channel Check Error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O Channel Check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable Parity Error Check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by Port Address register 6072H, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled

Bit 1 - ENSPK, Enable Speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA11 through RA0. During I/O cycles, RA11 through RA08 (CS3-CS0)are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA10 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM, plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{MEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128 Kbyte to 640 Kbyte, 256 Kbyte to 640 Kbyte and 512 Kbyte to 640 Kbyte.

When disabling any on-board DRAM, the register at Port Address 6872H must not be programmed to enable the on-board Lower EMS Page Frame.

The WD7710 and WD7710LP provide support for DRAM banks to be independent or two-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size.

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872H - Read and Write

15	14	13	12	11	10	09	08
PG_CAS		CA		PG	ILV		

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS	0
CA	00
PG	0
ILV	00
SIZE_BNK3	00
SIZE_BNK2	00
SIZE_BNK1	00
SIZE_BNK0	00

Bit 15 - PG_CAS, Page Mode CAS Width

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks. This is required for 80386SX Pipeline mode.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache Mode

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the RDYIN signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the RDYIN (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)

0 1 - Cache Mode enabled.

1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the external memory controller.

1 1 - Pin 51 may be used as the alternate clock CKA. When CAS Input Mode is enabled, PE on pin 111 becomes an input and represents an error. (See pin 12 description in Table 3-2 on selecting CAS Mode.)

Bit 11 - PG, Page Mode

PG = 0 - Non-page mode (Default value)
Word interleaving is employed when bank interleaving is enabled by ILV. Non-page mode *is not supported* in 1Mbit x 16 chips and 2Mbits x 16 configurations.

PG = 1 - Page mode
Page mode interleaving is performed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In Non-page Mode (PG = 0), word interleaving is employed. In Page Mode (PG = 1), Page Mode interleaving is used. Four-way interleave is only supported in Page Mode when four banks are installed using one of the following DRAM configurations: 4 Mbits x 16; 512Kbits x 16; 1Mbit x 16 chips; or 2Mbits x 16. Interleave of 64 Kbits x 16 DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size and assigned the same starting address when they are interleaved together.

ILV 10 09 08

- 0 0 0 - No interleaving performed
- 0 0 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are not interleaved
  Banks 0 and 1 must be the same size
- 0 1 0 - Banks 0 and 1 are not interleaved
  Banks 2 and 3 are interleaved
- 0 1 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are interleaved
  (Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.)
- 1 0 0 - Page Mode four-way interleave (Banks 0, 1, 2 and 3 must have one of the following DRAM configurations installed: 4 Mbits x 16; 512 Kbits x 16; 2Mbits x 16; or 1 Mbit x 16 chips.)

DRAM Banks 3 through 0

The WD7710 and WD7710LP support all DRAM sizes. The DRAM sizes may be mixed.

Bits 07, 06 - SIZE_BNK3, Size of Bank 3

PORT 7472	PORT 3872		BANK 3 SIZE
BIT 15	BIT 7	BIT 6	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 05, 04 - SIZE_BNK2, Size of Bank 2

PORT 7472	PORT 3872		BANK 2 SIZE
BIT 14	BIT 5	BIT 4	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 03, 02 - SIZE_BNK1, Size of Bank 1

PORT 7472	PORT 3872		BANK 1 SIZE
BIT 13	BIT 3	BIT 2	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 01, 00 - SIZE_BNK0, Size of Bank 0

PORT 7472	PORT 3872		BANK 0 SIZE
BIT 12	BIT 1	BIT 0	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 1 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 0 start address					

Port Address 5072H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 3 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 2 start address					

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes. For three banks of the same size, in which two are interleaved, the two interleaved banks must be placed at a lower starting address than the third bank.

RAM SIZE	PAGE SIZE	BANK SIZE
64Kbits x 16	512 Bytes	128 Kbytes
256 Kbits x 16	1024 Bytes	512 Kbytes
1 Mbits x 16	2048 Bytes	2048 Kbytes
4 Mbits x 16	4096 Bytes	8192 Kbytes
512 Kbits x 16	1024 Bytes	1024 Kbytes
1 Mbit x 16 chips	512 Bytes	2048 Kbytes
2 Mbits x 16	1024 Bytes	4096 Kbytes

6.2.3 Split Starting Address

Port Address 5872H - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At RSTIN
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	00
SPLIT_SIZE	00
Bits 01, 00	None

Bit 15 - EN_BK3, Enable Bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value)

EN_BK3 = 1 -
Bank 3 is enabled

Bit 14 - EN_BK2, Enable Bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value)

EN_BK2 = 1 -
Bank 2 is enabled

Bit 13 - EN_BK1, Enable Bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value)

EN_BK1 = 1 -
Bank 1 is enabled

Bit 12 - EN_BK0, Enable Bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value)

EN_BK0 = 1 -
Bank 0 is enabled

Bits 11, 10 - DRAM_DRV, DRAM Driver Strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

DRAM_DRV
11 10

0 0 - Full strength DRAM address drive, up to 350 pF (Default value)

0 1 - Low strength DRAM address drive, up to 100 pF

1 0 - Medium strength DRAM address drive, up to 180 pF

1 1 - High strength DRAM address drive, up to 260 pF

Bits 09, 08 - SP SIZE, Split Size

The split is implemented by moving the block of memory between 0A0000H through 0FFFFFH to another area. The destination area must start on a 512 Kbyte boundary. If BIOS is to be shadowed, the split size must be 320 Kbyte for a 64 Kbyte shadow or 256 Kbyte for a 128 Kbyte shadow, and the RAM Shadow And Write Protect Register (Port 6072H) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000H (640 Kbyte) to 100000H (1024 Kbyte) is available for remapping. The remapping may start at 100000H, providing 384 Kbyte of extended memory, or may start at 0F0000H to allow BIOS shadowing, with 320 Kbyte of extended memory. Only a single bank may be split. The bank to be split must be at least 512 Kbyte or larger.

SPLIT SIZE
09 08

0 0 - No split (Default value)
0 1 - 256 Kbyte split, memory moved from 0A0000H to 0DFFFFH
1 0 - 320 Kbyte split, memory moved from 0A0000H to 0EFFFFH
1 1 - 384 Kbyte split, memory moved from 0A0000H to 0FFFFFH

Bits 07-02 - A24-A19, Split Starting Address

Bits 01, 00 - Not used, state is ignored

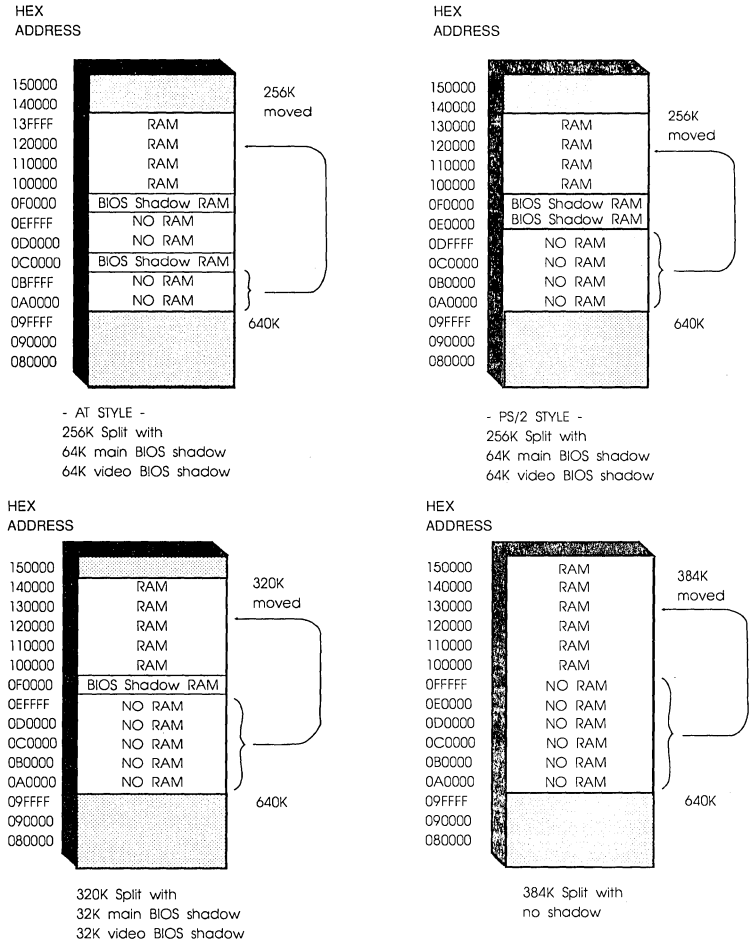


FIGURE 6-1. SPLIT SIZE

6.2.4 RAM Shadow And Write Protect

Port Address 6072H - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
X_ MEM		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	00
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	00
X_MEM	0
Bit 06	None
VB_SIZ	00
ROM_TYP	00
BL_MOU †	00

† Featured only in the WD7710LP

Bit 15, 14 - DIS_MEM, Disable On-board Memory

DIS_MEM
15 14

0 0 - On-board memory from 128 KB to 640 KB not disabled (Default value).

0 1 - On-board memory from 512 KB to 640 KB disabled.

1 0 - On-board memory from 256 KB to 640 KB disabled.

1 1 - On-board memory from 128 KB to 640 KB disabled.

Bit 13 - HM_WP, High Memory Write Protect Enable

This bit enables the write protection for the memory boundary established by the register at Port C072H.

HM_WP = 0 -
High memory write protect not enabled (Default value).

HM_WP = 1 -
High memory write protect enabled.

Bit 12 - WP, Shadowed BIOS Write Protect Enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value).

WP = 1 -
Write protect for shadowed BIOS enabled.

Bit 11 - INV_PAR, Invert Parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value).

INV_PAR = 1 -
Invert parity when writing to on-board DRAM.

Bit 10 - PAR_DIS, Parity Checking Disabled

Parity checking is normally enabled or disabled by Port 061H. Setting PAR_DIS overrides the Port 061H setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by Port 061H (Default value).

PAR_DIS = 1 -
Parity checking disabled.

Bits 09, 08 - SHD, Shadow BIOS

Before the BIOS can be shadowed, the SPLIT_SIZE field in the Split Starting Address Register at Port 5872H must be programmed to non-zero.

ROM at FE0000H through FFFFFFH, the top of 16 MByte address space is never shadowed.

Option SHD 11 should be used when Video Remap Function is desired (i.e. Video BIOS in the lower half of EPROM shows up at C0000H).

64 Kbyte of system BIOS at 0F0000H through 0FFFFFH, and up to 64 Kbyte of video BIOS at 0C0000H through 0CFFFFH, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000H through 0FFFFFH. When SHD is set to 11, the video BIOS appears at 0C0000H through 0CFFFFH rather than 0E0000H through 0EFFFFH.

The video shadow size at 0C0000H - 0CFFFFH is determined by VB_SIZ, the video BIOS size field.

SHD
09 08

† 0 0 - No BIOS shadowing, allows 384 KB remap (Default value).

0 1 - 64 KB system BIOS shadow, 0F0000H - 0FFFFFH, allows 320 KB remap.

1 0 - 128 KB system BIOS shadow, 0E0000H - 0FFFFFH, allows 256 KB remap.

† 1 1 - 64 KB system BIOS shadow, 0F0000 - 0FFFFF and video BIOS shadow, allows 256 KB remap.

† See note following bits 01, 00.

Bit 07 - X_MEM, Shadow BIOS for Read/Write Memory

When SHD (bits 09 and 08) equals 11, X_MEM provides the means of using RAM from E8000H through EFFFFH not being used for video BIOS shadowing, to be used as read/write memory.

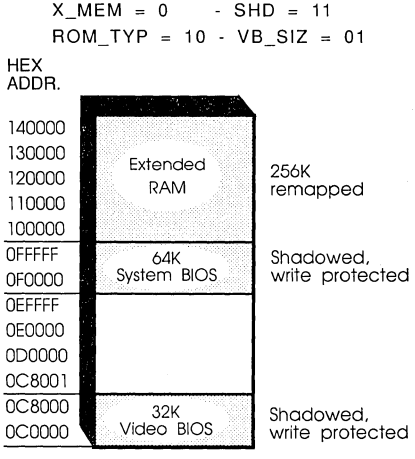


FIGURE 6-2. X_MEM = 0

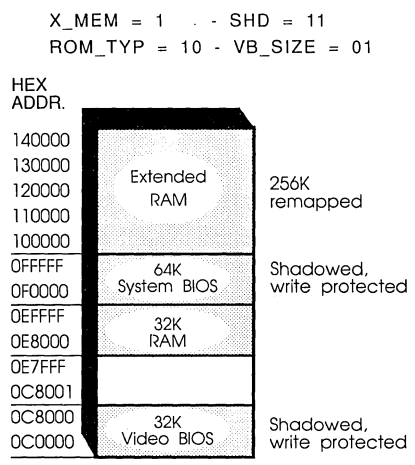


FIGURE 6-3. X_MEM = 1

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS Size

VB_SIZ †
05 04

0 0 - 16 KB video BIOS (Default value)

0 1 - 32 KB video BIOS

1 0 - 48 KB video BIOS

1 1 - 64 KB video BIOS

† See note following bits 01, 00.

Bits 03, 02 - ROM_TYP, ROM Type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000H - 0FFFFFH or FE0000H - FFFFFFH.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000H - 0FFFFFH or FF0000H - FFFFFFH.

For ROM type 10, CSPROM is asserted when the address is 0F0000H - 0FFFFFH, FF0000H - FFFFFFH or 0C0000H - 0CXFFFH where X is determined by VB_SIZ. This allows either a 128 Kbyte BIOS with a 64 Kbyte system BIOS and a 64 Kbyte video BIOS, or a 64 Kbyte BIOS with a 32 Kbyte system BIOS and a 32 Kbyte video BIOS. The 32 Kbyte video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000H - CX000H and F0000H - FX000H. A

64 Kbyte EPROM needs addresses SA15 - SA0. A 128 Kbyte EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128 KB system BIOS, located at E0000H - FFFFFH
- 0 1 - 64 KB system BIOS, located at F0000H - FFFFFH (Default value)
- † 1 0 - 64 KB or 128 KB shared BIOS System BIOS located at F0000H - FFFFFH, video BIOS located at C0000H - CX000H
- 1 1 - Reserved

† See note following bits 01, 00.

Bits 01, 00 - BL_MOU, Backlight Mouse Control
Featured only in the WD7710LP

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port 1072H bit 11. Enabling the Backlight Mouse Control also affects the Back/light and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00

- 0 0 - No mouse control (Default value)
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

† NOTE

When SHD = 11 and X_MEM = 0, or SHD = 00 and ROM_TYP = 10, the portion of 0E0000H DRAM memory that is not mapped to 0C0000H (as determined by VB_SIZ) is not accessible. Once a portion of 0E0000H segment is mapped to 0C0000H, all 0E0000H accesses go to the expansion bus without generation of $\overline{\text{CSPROM}}$. This allows AT bus plug-in boards and/or drivers to access the E0000H segment.

6.2.5 High Memory Write Protect Boundary

Port Address C072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At RSTIN
Bits 15-08	None
A24 - A17	00

Bits 15-08 - Not used, state is ignored

Bits 07-00 - A24-A17, Boundary Address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at Port 6072H. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at Port 4072H, the memory timing mode changes immediately. The code that programs this register should be in ROM and not shadowed in RAM.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072H - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_ RAW	NP_WCAS		_NP_RCAS	

07	06	05	04	03	02	01	00
	NP_RAS_ HLD		NP_PWE			NP_WS	

Signal Name	Default At RSTIN
Bits 15, 07	None
NP_MODE	00
NP_RAW	0
NP_WCAS	00
NP_RCAS	00
NP_RAS_HLD	00
NP_PWE	000
NP_WS	00

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-Page Mode

There are two non-page modes available, Mode-00 and Mode-01. Mode-00 provides one processor clock of row address hold time and is used for 1, 2 or 3 wait state memory cycles. Mode-01 provides a half processor clock of row address hold time and is used for 0 wait state memory cycles. Because the memory timing may be adjusted in increments of half a processor clock, Mode-00 is suited for all DRAM and processor speeds.

Mode-01 provides a half processor clock row address hold time, which is usually sufficient for system speeds of 12.5 MHz and slower. This compressed timing allows zero wait state operation.

Table 6-1A shows typically required DRAM speeds and register programming values for various processor speeds. Because DRAM timing varies among manufacturers, the required DRAM speed may differ from those listed in the table.

NP_MODE
14 13

0 0 - Minimum 1 wait state.

0 1 - Minimum 0 wait state.

PROCESSOR SPEED	NP_ MODE	DRAM SPEED	WAIT STATES	REGISTER 4072H
12.5 MHz	01	80 ns	0	3560H
16 MHz	01	53 ns	0	3560H
16 MHz	00	80 ns	1	1025H
20 MHz	00	80 ns	1	1025H
20 MHz	00	100 ns	2	107AH

TABLE 6-1A. TYPICAL DRAM SPEEDS

Bit 12 - NP_RAW, Non-page disable Read After Write

EMS accesses and interleave miss cycles (I/O cycle to device on RAD) may add one additional wait state.

NP_RAW = 0 -
Memory read cycles immediately following a write cycle causes an automatic wait state to be added before initiating the read cycle.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bit 11, 10 - NP_WCAS, Non-page Write CAS Delay

NP_WCAS
11 10

0 0 - CAS write delay 1.0 CLK2
0 1 - CAS write delay 1.5 CLK2
1 0 - CAS write delay 2.0 CLK2
1 1 - CAS write delay 2.5 CLK2

Bit 09, 08 - NP_RCAS, Non-page Read CAS Delay

NP_RCAS
11 10

0 0 - CAS read delay 1.0 CLK2
0 1 - CAS read delay 1.5 CLK2
1 0 - CAS read delay 2.0 CLK2
1 1 - CAS read delay 2.5 CLK2

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS Hold Time

The RAS active delay is reduced by half a clock during writes if NP_WCAS is set to 1X, or during reads if NP_RCAS is set to 1X.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS.

0 1 - RAS active until 1.5 clock after CAS.

1 0 - RAS active until 2.0 clock after CAS.

1 1 - RAS active until 2.5 clock after CAS.

Bits 04-02 - NP_PWE, Non-page CAS Pulse Width Extension

The pulse width is reduced by half a clock during writes if NP_WCAS is set to X1, or during reads if NP_RCAS is set to 1X.

NP_PWE
04 03 02

0 0 0 - No extension (2 CLK2 normal)
0 0 1 - Extended by 0.5 CLK2
0 1 0 - Extended by 1.0 CLK2
0 1 1 - Extended by 1.5 CLK2
1 0 0 - Extended by 2.0 CLK2
1 0 1 - Extended by 2.5 CLK2
1 1 0 - Extended by 3.0 CLK2
1 1 1 - Extended by 3.5 CLK2

Bits 01, 00 - NP_WS, Non-page Wait States

NP_WS makes it possible to unconditionally add wait states to all DRAM cycles. Condional wait states may be added to read after write cycles, EMS accesses and interleave miss cycles, with NP_RAW (bit 12).

NP_WS
01 00

0 0 - No wait states added
0 1 - 1 Wait state added
1 0 - 2 Wait states added
1 1 - 3 Wait states added

TIMING	NUMBER OF CLK2'S	
	MODE-00	MODE-01
Row address to RAS	2	2
RAS width	3 + NPH + NPHB / 2	1 + NPH + NPHB / 2
Row address hold	1	0.5
Column address setup (read)	1 + NPRF / 2	0.5 + NPRF / 2
Column address setup (write)	1 + NPWF / 2	1 + NPWF / 2
RAS hold (read from CAS)	1 + NPHB / 2 - NPRF / 2 + NPH	0.5 - NPRF / 2 + NPH
RAS hold (write)	1 + NPHB / 2 - NPWF / 2 + NPH	0.5 - NPWF / 2 + NPH
CAS width (read)	① + NPCAS + NPCB / 2 - NPRF / 2	① + NPCAS + NPCB / 2 - NPRF / 2
CAS width (write)	① + NPCAS + NPCB / 2 - NPWF / 2	① + NPCAS + NPCB / 2 - NPWF / 2
RAS precharge	2 × (2 + NP_WS) - RAS width	2 × (2 + NP_WS) - RAS width
Column address hold	1 - NPCB / 2	1 - NPCB / 2

① 2 if NPCAS = 0 or 1
1 if NPCAS = 2 or 3

NPWF = Bit 10 NPRF = Bit 08 NPH = Bit 06 NPHB = Bit 05
NPCAS = Bits 04, 03 NPCB = Bit 02 NP_WS = Bits 01, 00

TABLE 6-1B. NON-PAGE MODE TIMING

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6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access †	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access, pipline mode †	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit, pipeline mode †	1
	Read page first access non-pipeline mode †	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4

† Equal Bank sizes, non-EMS cycle

First access is a page mode memory cycle which immediately follows a refresh, DMA or master cycle. It is not necessary for the DRAMs to be precharged for a first access cycle, since all RAS signals have been high in the previous cycle. This shortens a first access page mode cycle by one wait state. For example, a read page miss, non-pipeline mode in 80386SX mode is four wait states. A read page miss, non-pipeline mode, first access in 80386SX mode is three wait states. All installed DRAMs must be the same size and configuration and the memory cycle cannot be an EMS cycle for a first access to occur.

TABLE 6-2. PAGE MODE WAIT STATES

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64 Kbyte, 256 Kbyte, 1 Mbyte or 4 Mbyte SIMM memory modules.

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	64 KBITS NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 4-WAY INTERLEAVE, 256K 2-WAY INTERLEAVE, 1MBITS NON-INTERLEAVE OR 512 KBITS X 8 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	256 KBITS 4-WAY INTERLEAVE, 1 MBITS 2-WAY INTERLEAVE, 4 MBITS NON-INTERLEAVE OR 512 KBITS X 8 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1 MBITS 4-WAY OR 4 MBITS 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	4 MBITS 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	512K X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A22	A19	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: NON-INTERLEAVE											
ROW	A13	A9	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A10	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A22	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	2M X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A23	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	REFRESH ADDRESS											
ROW		A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER (Continued)

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

An external latch is required to generate RA11 for 1M x 16 and 2M x 16 type DRAMs. It latches A13 from the processor address bus with the inverted READY signal from the WD7710.

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872H - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_ RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	00
Bits 12, 09, 08	None
EMS_EN	00
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS Pointer

The INC bit controls whether or not the EMS Pointer at Port E072H is to be incremented after each read or write of the EMS Page Register at Port E872H.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper Page Frame Location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000H (Default value)

0 1 - Upper page frame starts at C8000H

1 0 - Upper page frame starts at CC000H

1 1 - Upper page frame starts at D0000H

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS Enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming without having to enable a Page Frame. This is useful for initializing the lower Page Frame.

1 0 - Enable upper Page Frame assignments and EMS register programming.

1 1 - Enable upper and lower Page Frame assignments and EMS register programming.

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable Lower Boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17,
LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128 Kbyte below the actual start address. For example, to start EMS at the 1 Mbyte boundary, this field should be set to 07H.

6.4.2 EMS Page Register Pointer

Port Address E072H - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
DLT							
16	15	15	13	12	11	10	9

07	06	05	04	03	02	01	00
DLT		POINTER					
8	7						

Signal Name	Default At RSTIN
DLT	0-0
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in Port 6872H, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at Port E872H. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

Bits 15-06 - DLT, Delay Line Test

In the Delay Line Test Mode, these bits represent the state of internal Delay Line signals.

The Delay Line Test is initiated by bit 8 (TDL) in the Test Enable Register at Port Address A872H.

Bits 05-00 - POINTER, EMS Page Register Number

Decimal number, 00 through 39. When programming this field, the hex equivalent 00 through 27H should be used.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF

EMS registers 32 through 39 (decimal) can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See Port E872H description.

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 (decimal) are enabled or disabled as a block. If the EMS_EN field of Port 6872H is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See Port E872H description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872H - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

There are 40 EMS Page Registers accessible through Port E872H. Only EMS registers 32 through 39 are initialized to zero. EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at Port E072H provides the offset location for Port E872H.

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
Bits 14-12	0
P11-P0	0

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at Port 6872H. When EMS_EN equals 11, the EN bit in this register is treated as a one for the lower Page Frame.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MBytes of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16 Kbytes, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128 Kbytes of memory and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MBytes, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using MEMR, MEMW, MEMCS16 and IOCHRDY to make the transfer.

NOTE

When using external EMS memory with P11 = 1, EN (bit 15) must be 0.

7.0 CACHE CONTROLLER

The Cache Controller provides an effective way to increase the memory bandwidth by storing the most frequently used data in the internal Cache DATA RAM. The WD7710 provides both software and hardware mechanisms to assure coherency of the data between CPU, DMA and Bus Master cycles. During DMA/Master write cycles, the controller will compare the system address and the tag contents. If the address matches, the data will be written into the data RAM. The cache can also be flushed by writing to the flush register.

7.1 CACHE ARCHITECTURE

The cache controller contains of eight functional blocks.

- Processor Interface
- TAG RAM
- DATA RAM
- SNOOP Interface
- Non-cacheable Control
- Diagnostic Control Logic
- LRU
- Flush

Figure 7-1 shows a block diagram of the cache.

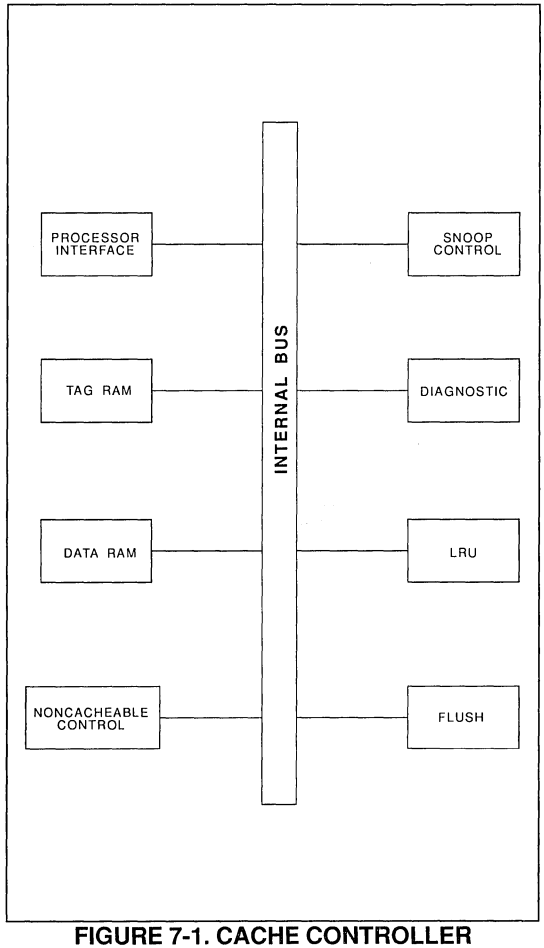

FIGURE 7-1. CACHE CONTROLLER FUNCTIONAL DIAGRAM

7.1.1 Processor Interface

The processor interface supports the 80386SX in both pipeline and non-pipeline mode. It keeps track of the 80386SX processor states a generates READY for read hit cycles. It ignores all the I/O and co-processor cycles.

7.1.2 TAG RAM

BIST (Built-In-Self-Test)logic is included in the TAG RAM to reduce test time.

The internal TAG RAM is organized as two sets of 256 x 21 self-timed synchronous static RAM. Twelve bits are used to store A12:23 from the processor; 8 bits are used to store the demultiplexed A1:3 as line valid, and 1 bit is used as block valid. The block valid bit can be cleared by the FLUSH function which flushes the cache contents and causes block miss for all the subsequent cycles.

A4 through A11 from the 80386SX selects one of the entries from each set. The output from the TAG RAM is compared against the address (A12:23,A1:A3) from the processor. If the address is the same and the corresponding line valid and block valid bits are set, a cache hit cycle is activated. If an address match occurs when the block valid bit is set, and the line valid is clear, it is a line miss. On the other hand, if the address does not compare or the block valid bit is clear, it is a block miss cycle.

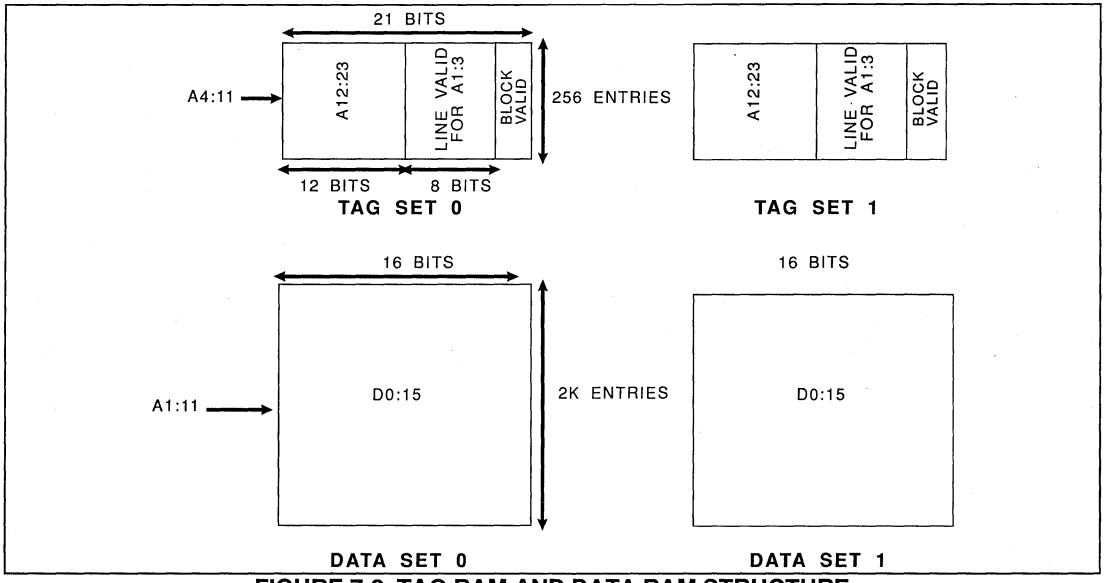

FIGURE 7-2. TAG RAM AND DATA RAM STRUCTURE

During the read block miss cycle, the address is written into the TAG RAM, the block valid bit is set, and the corresponding line valid bit is set.

During the read line miss cycle, the corresponding line valid bit is set, and all other bits are not altered.

Address Compare	Line Valid	Block Valid	
X	X	0	Block Miss
0	X	1	Block Miss
1	0	1	Line Miss
1	1	1	Hit

During a memory write cycle, the contents of the TAG RAM is not affected. The Block size of the TAG RAM is eight lines and each line is 2 bytes. The TAG RAM enters low power mode during Full Power Down to conserve power.

7.1.3 Data RAM

The internal DATA RAM is organized as 2 sets of 2K x 16. During a read hit cycle, the data is provided by one of the sets of DATA RAM to the processor. During a read miss cycle, the data is provided by the DRAM to the processor and is written into the DATA RAM. If the read cycle is a page hit, it will be a one wait state cycle. If it is a page miss, it will be a four wait states cycle. See Section 12.4, Cache Controller Timing.

During a write hit cycle, the data from the processor is written into the DATA RAM to maintain data coherency. In a write miss cycle, either block miss or line miss, no action is taken and DATA RAM contents are not affected. See Section 12.4, Cache Controller Timing.

The DATA RAM enters low power mode during Full Power Down to conserve power. BIST logic is included in the DATA RAM to reduce test time.

7.1.4 Snoop Interface

The Snoop interface maintains the data coherency when DMA or Master cycles take place. When a DMA or Bus Master write cycle occurs, the Snoop logic will update the data in the DATA RAM if the address from DMA or the Bus Master is the same as the corresponding TAG address(Hit cycle). If no match is indicated (Miss cycle), the DATA RAM will not be updated. See Section 12.4, Cache Controller Timing.

7.1.5 Non-cacheable Control

Two user definable and twelve standard non-cacheable regions are provided. Ten of the twelve standard regions are 16KB increments from C8000H - EFFFFH. These regions can be used as EMS memory or for DOS 5.0 Upper Memory Blocks and can be enabled or disabled individually. The other two standard non-cacheable regions are the video BIOS area (C0000-CXFFF or E0000-EFFFF) and the system BIOS area (F0000-FFFFF). The Non-cacheable control logic allows cacheing of these regions to be enabled or disabled individually.

The two user definable non-cacheable regions can also be enabled individually. The non-cacheable regions are set by the upper and lower limit registers. These regions are assigned on 4Kbyte boundaries anywhere in the 16MB physical address space of the 80386SX.

The typical applications of these user defined noncacheable areas are the memory between 512KB and 640KB, and the memory accessed on the AT bus. When powered up, the WD7910 assumes all the memory from 0KB to 640KB and 1M to 16MB are cacheable. It is necessary to have the BIOS to program the noncacheable region registers.

7.1.6 Diagnostic Control Logic

The function of the diagnostic control logic, when enabled, is to map the internal TAG RAM and LRU RAM to address 20000H and DATA RAM to address 40000H. In this mode, memory accesses to these address ranges are diverted to the internal TAG RAM and DATA RAM. This permits the system BIOS to test the internal DATA RAM and TAG RAM.

During Diagnostic Access, the 21-bit TAG RAM (D20:0) and the 2-bit LRU RAM (L1:0) are concatenated to 23 bits and mapped into the Address Space by using A1 to determine whether the data presented is TAG RAM bits D20-D9 (A1 Low) or TAG RAM bits {L1:0,D8:0} (A1 high). Since the LRU RAM has 128 entries (See Section 3.1.7) whereas the TAG RAM has 256 entries, so address A4 has no effect on the selection of the LRU RAM.

7.1.7 LRU

The LRU section has 128 entries and each entry has 2 bits. Addresses 11:5 are used to select one of the entries and Address 4 is used to select one of the two bits. In the event of a read miss, either group can be updated with new data. The LRU bit of the corresponding entry flags the candidate for replacement. Once the replacement is done, LRU bit of the corresponding entry is changed and pointed to the other set. In the event of read hit, the LRU bit of the corresponding entry points to the other set. During a write hit cycle, the corresponding LRU bit is changed and pointed to the other set. The LRU bit is not changed for write miss cycles. All the entries are reset to zero by NRESIN.

7.1.8 Flush

Flush is used to clear all the block valid bits in the TAG RAM and to clear all the LRU bits. This force the cache controller to rebuild the cache contents and force all the subsequent fetch to the DRAM. This is used after an EMS page change.

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7.2 CACHE CONTROL REGISTER

Port Address C472 Read / Write

15	14	13	12	11	10	09	08
C_ ENBL	C_ SSB	C_ DIAG	C_ SVB	MFR	C_M	HI_ME M9	HI_ME M8

07	06	05	04	03	02	01	00
HI_ME M7	HI_ME M6	HI_ME M5	HI_ME M4	HI_ME M3	HI_ME M2	HI_ME M1	HI_ME M0

Bit 15 - C_ENBL, Cache Enable

This bit is used to enable the cache controller. Before writing to this bit, the memory controller must be programmed to support the cache mode. This can be done by writing (01) to bit 13 and 12 of register 3872. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_ENBL= 1 Cache Enable
C_ENBL= 0 Cache Disable (Default)

Bit 14 - C_SSB, Cache Shadowed System BIOS at F0000H through FFFFFH

When the System BIOS is shadowed, it can also be cached to increase the system BIOS performance. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SSB = 1 Enable caching of shadow RAM. When Custom mode is enabled, the address from 0F0000H - 0F0FFFH is not cached.

C_SSB = 0 Disable caching of shadow RAM (Default)

Bit 13 - C_DIAG, Cache Diagnostic Mode

Enabling the cache and this bit puts the cache into diagnostic mode as described in section 7.1.6. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_DIAG = 1 Cache is in diagnostic mode

C_DIAG = 0 Standard cache mode (Default)

Bit 12 - C_SVB, Cache Shadowed Video BIOS at E0000H through EFFFFH or C0000H through CXXXXH

When the Video BIOS is shadowed, it can also be cached to increase the Video BIOS performance.When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SVB = 1 Enable Cacheing Video BIOS

C_SVB = 0 Disable Cacheing Video BIOS (Default)

Bit 11 - C_MFR, Manufacturing Test Bit

Bit 10 - C, Cache Mode

C = 1 2-way set associative
C = 0 Direct-mapped (Default)

Bits 9:0 - HI-MEM, High memory region caching control. Setting these bits enables the caching of the HI-MEM region. Default after reset is 0.

BIT 9 EC000H - EFFFFH
BIT 8 E8000H - EBFFFH
BIT 7 E4000H - E7FFFH
BIT 6 E0000H - E3FFFH
BIT 5 DC000H - DFFFFH
BIT 4 D8000H - DBFFFH
BIT 3 D4000H - D7FFFH
BIT 2 D0000H - D3FFFH
BIT 1 CC000H - CFFFFH
BIT 0 C8000H - CBFFFH

Bits 9:0 = 1, Enable caching
Bits 9:0 = 0, Disable caching

7.2.1 Noncacheable Region 1 Upper Boundary

Port Address BC72. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S_REF	INT_DIS	INT_ST	S_IO RDY

This register determines the upper address boundary of the user defineable noncacheable region 1. Default after reset is zero.

Bits 15:4, = A23: 12 of the upper address boundary

Bit 3, Slow Refresh

When this bit is set, the DRAM refresh rate is slowed down to 120µs. This bit does not affect the refresh toggle bit in Port 61.

Bit 3 = 1, Enable Slow Refresh

Bit 3 = 0, Disable Slow Refresh (Default)

Bit 2, Interrupt Disable

When this bit is set, the interrupt from the interrupt controller is disabled. The command will not take effect immediately if the interrupt request signal from the interrupt controller is active. The command will take effect immediately if the interrupt request signal is inactive. This allows control of the interrupt regardless of the Operating system privilege level.

Bit 2 = 1, Disable the hardware interrupt from the interrupt Controller

Bit 2 = 0, Enable hardware interrupt.

Bit 1, Interrupt Disable Status (Read Only)

This enables reading of Interrupt Status regardless of Operating System privilege level.

Bit 1 = 1, Indicates the Interrupt Disable command is pending

Bit 1= 0, Indicates the Interrupt Disable command is processed

Bit 0, SNOOP with IOCHRDY active

During periods when the CPU Clock is slower than the AT BUS clock (slowed for power savings), the Snoop Logic may be unable to properly track the memory cycle during DMA or BUS Master Cycles. Setting this bit enables the WD7710 to use the IOCHRDY signal to lengthen the cycle.

Bit 0 = 1, Enable IOCHRDY for DMA/Master cycle

Bit 0 = 0, Disable IOCHRDY for DMA/Master cycle (Default)

7.2.2 Noncacheable Region 1 Lower Boundary

Port Address B472. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S DMA_ CLK	X_ WS	S_ BIST	BIST _S

This register determines the lower address boundary of the user defineable noncacheable region 1. Noncacheable region 1 is disabled when the upper boundary is set below the lower boundary. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary.

Bit 3, Stop DMA Clock

Setting this bit causes the DMA clock to stop while there is no DMA activity. Upon any DMA request (DRQn), the DMA clock starts up again and continues to run until 16 DMA clocks after the end of the DMA Acknowledge (DACKn).

Bit 3 = 1, Enable Stop DMA Clock

Bit 3 = 0, Disable Stop DMA Clock (Default)

Bit 2, Extra Wait State for Page Mode

If this bit is active, it adds an extra wait state to all the memory cycles. With this featury system manufacturer can use slower DRAM for WD7710 system without loss of huge performance and achieve saving since the majority of the memory access are directly to the internal cache.

Bits 1, Start BIST

Setting bit 1 forces the BIST to check the TAG RAM and DATA RAM. The result can be checked by reading BIT 0. Bit 0 is a read only register.

Bit 0, BIST Status

Bit 0 = 1, RAM error.

Bit 0 = 0, No error found.

7.2.3 Noncacheable Region 2 Lower Boundary

Port Address CC72 Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12				NR 2C

This is used to determine the lower address boundary of the user defineable noncacheable region 2. Any address above or equal to this address is considered non-cacheable. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary

Bits 3:1, Test Register

For Factory use only.

Bit 0, Non-cacheable Region 2

Bit 0 = 1, enables non-cacheable Region 2
Bit 0 = 0, disables non-cacheable Region 2 (default)

7.2.4 Flush

Port Address F872H Write Only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00

Signal Name	Default At RSTIN
All signals	None

Writing to this I/O port with any data will clear all the valid bits in the TAG RAM. This is ordinarily used to clear the cache when there is a change to the EMS page register and also causes the WD7710 to output Chip Select number 13H.

8.0 PORT CHIP SELECT AND WD7710LP REFRESH

This section describes refresh control logic peculiar to the WD7710LP and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 8-1 identifies the ports, their Chip Select number, I/O address and function.

8.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H - Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF †	0
V_REF †	0
CBR_REF †	0
CBR_SR	0
SCSI	0
PAR	00
PAR_L	0
SER_A	000
SER_AL	0
SER_B	000
SER_BL	0

† Featured only in the WD7710LP

Bit 15 - M_REF, Memory Refresh Power Down Mode
Featured only in the WD7710LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and M_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value).

M_REF = 1 -
Slow refresh main on-board memory.

Bit 14 - V_REF, Video Refresh Power Down Mode
Featured only in the WD7710LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and V_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS Before RAS Refresh For On-board DRAM
Featured only in the WD7710LP

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not.

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 8-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353XH

Bits 10, 09 - PAR, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 8-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BCH - 3BFH

1 0 - PAR chip select at I/O port 378H - 37FH

1 1 - PAR chip select at I/O port 278H - 27FH

Bit 08 - PAR_L, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, Serial Port A Chip Select

The serial port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port A chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port A chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port A chip select at I/O port 2E8H - 2EFH

Bit 04 - SER_AL, Serial A Port Bus Location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B Serial Port B Chip Select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port B chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port B chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port B chip select at I/O port 2E8H - 2EFH

Bit 00 - SER_BL, Serial B Port Bus Location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_BL = 1 -
Serial port B is located on the expansion data bus

8.2 RTC, PVGA, 80287 TIMING, AND DISK CHIP SELECTS

Port Address 2872H - Read and Write

Bits 12 through 07 and Port Address 3072H control the use and location of the Programmable Chip Select.

15	14	13	12	11	10	09	08
RTC_ L	FST_ VGA	FST_ SCSI	EN_ PCS1	U_ MSK1	L_MSK1		

07	06	05	04	03	02	01	00
PRG_ L	HS_ HD		P/S	HS_ 287	LK_ PSW	DS_ HD	DS FLP

Signal Name	Default At RSTIN
RTC_L	0
FST_VGA	0
FST_SCSI	0
EN_PCS	0
U_MSK1	00
L_MSK1	00
PRG L	0
HS HD	000
P/S	000
HS 287	0
LK PSW	0
DS HD	0
DS FLP	0

Bit 15 - RTC_L, Real-Time Clock

The Real-Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

Bit 14 - FST_VGA, Fast VGA Video

The performance of Western Digital Imaging PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital Imaging PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
One wait state I/O cycle to PVGA

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 SCSI Contoller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS1, Enable Programmable Chip Select 1

The Programmable Chip Select logic is selected with chip select 11 and may be disabled or enabled. See Table 8-1.

EN_PCS = 0 -
Disable Programmable Chip Select (Default value)

EN_PCS = 1 -
Enable Programmable Chip Select

Bit 11 - U_MSK1, Upper Address Bits Masked

U_MSKI determines whether or not the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

U_MSKI = 0 -
A15 through A10 are ignored (Default value).

U_MSKI = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK1, Lower Address Bits Masked

L_MSK1 determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

L_MSK1
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value).

0 0 1 - A00 is ignored.

0 1 0 - A00, A01 are ignored.

0 1 1 - A00, A01, A02 are ignored.

1 0 0 - A00, A02, A03 are ignored, A01 is not ignored, ver. A-F. A00, A01, A02 A03 are ignored, WD76C10A and newer.

Bit 07 - PRG_L, Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable Chip Select is on the expansion bus.

Bit 06 - HS_HD, High Speed Hard Disk Data Transfer Rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with IOCS16 ignored and the WD76C20 hard disk chip select remaining stable.

NOTE

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives WD-AC280, WD-AC140, WD-AC160, WD-AC2120, WD-AP4200, WD-AB130 and WD-AH260.

HS_HD = 0 -
Compatible bus timing enabled (Default value).

HS_HD = 1 -
High speed hard disk accesses enabled.

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 8-1, chip select numbers 08H through 0BH.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value).

P/S = 1 -
Secondary hard disk and Floppy address selected.

Bit 03 - HS_287, Co-processor 80287 High Speed Timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_287 results in 16-bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value).

HS_287 = 1 -
Fast 80287 timing.

Bit 02 - LK_PSW, Prevent Locking Password

Port 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092H bit 3, Lock_Pass can be set (Default value).

LK_PSW = 1 -
Port 092H bit 3, Lock_Pass can not be set.

Bit 01 - DS_HD, Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

8.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072H - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

Signal Name	Default At RSTIN
All signals	None

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8.4 I/O PORT ADDRESSES

Table 8-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
ROM Chip Select	N/A	00	Chip select for BIOS ROM
Keyboard Control	060 - 06E even	01	Chip select for 8042
80287	00E0 - 00FF	02	Chip select for numeric processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real-time Clock	070	05	RTC ALE
Real-time Clock	071	06	RTC Write Strobe
Real-time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary address Secondary address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary address Secondary address
Floppy Control Chip Select	3F7 377	0A	Primary address Secondary address (Floppy enabled, HD disabled)
Floppy and HD Control Chip Select	3F7 377	0B	Primary address Secondary address (Floppy enabled, HD enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary address Secondary address
Hard Disk Chip Select	3F6 3F7 † 376 377 †	0D	Primary Address Secondary address
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ††	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	

TABLE 8-1. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ††	
Program Chip Select 1	PROG 1	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Floppy Chip Select	3F0 - 3F1 370 - 371	18	Primary address Secondary address
Floppy Chip Select	3F3 373	19	Primary address Secondary address
Program Chip Select2	PROG 2	1A	
Program Chip Select 3	PROG 3	1B	
Reserved		1E	Reserved
Reserved		1F	Reserved

† IDE Hard disk enabled, floppy disabled

†† The Chip Select Number is the decoded value of CS4 - CS0. If the Programmed Chip Select corresponds to any other decode, the Programmed Chip Select is suppressed. If Serial Port A and B are programmed for the same address, Serial Port B Chip Select is suppressed.

TABLE 8-1. I/O PORT ADDRESSES (Continued)

9.0 POWER MANAGEMENT CONTROL

The WD7710LP supports all PMC inputs, output and interrupt functions.

9.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD7710LP is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2 and VCPI.

With the WD7710LP a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approch to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

System Activity
System activity denotes periods of time in which the system performs useful tasks. The sources Of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ 0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ 8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A progammable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

Using SAM for System Power Management:

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period, SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation, and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order to do this, control to the CPU must be relin-

quished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds, and establish a clean breakpoint for Suspending the system.

Advantages of SAM:

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

- Detection of system activity for extended periods of time, for the purposes of system timeout.
- Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program.

7. SAM also carries information on DMA activity state. This is used for determining whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at powerup time on Resume.

NOTE

SAM cannot be used for determining when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2.

9.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control Register is used to control the power converter from the processor. The WD7710LP holds CPUCLK, READY, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, READY, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT273 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD7710LP's internal registers by way of the PMC logic. The keyboard processor starts a local ac-

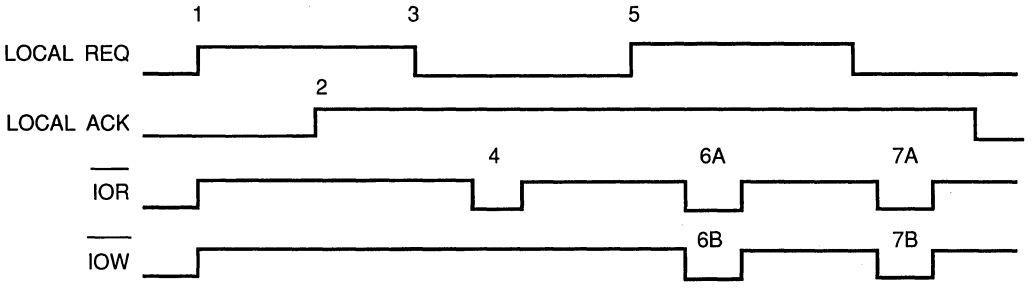
cess by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1 and Table 9-2). The WD7710LP arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD7710LP asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD7710LP on the data bus and drops the LCL_REQ. The WD7710LP responds by de-asserting LCL_ACK.

If the opcode specified a register write, data high (D15 through D08) and data low (D07 through D00), bytes are passed to the WD7710LP. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD7710LP to the keyboard processor.

All special operation registers within the WD7710LP may be accessed in this manner without first unlocking the register. See section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 9-1 shows the handshake procedure, followed by the keyboard controller and the WD7710LP.

Figures 9-2 and 9-3 represents the powerdown and powerup sequence and control.



1 8042 Requests local data transfer

2 WD7710LP returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD7710LP reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD7710LP Reads high byte

7A WD7710LP Read low byte, writes to internal register

FOR READ CYCLE OF WD7710LP INTERNAL REGISTER:

6B WD7710LP Writes high byte to 8042

7B WD7710LP writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	RSV	A15	A14	A13	A12	A11	A10

DIR = 1 - Read register (generates IOW to 8042)

DIR = 0 - Write register (generates IOR to 8042)

FIGURE 9-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

9.3 PMC OUTPUT CONTROL REGISTERS

Port Address 7072H - Bits 07-00 are Read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 7:0

Featured only in the WD7710LP

Port Address 7872H - Bits 07-00 are Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 15:08

Featured only in the WD7710LP

PMC	PMC OUTPUT SIGNAL PORT 7072H	PMC	PMC OUTPUT SIGNAL PORT 7872H
0H	CPU Clock Driver Enable	8H	User Defined
1H	LCD Enable	9H	User Defined
2H	Backlight Enabled	AH	User Defined
3H	LCL_ACK	BH	User Defined
4H	LCL_ATN	CH	User Defined
5H	Processor powerdown	DH	User Defined
6H	Gate A20	EH	User Defined
7H	Full Powerdown	FH	User Defined

TABLE 9-1. PMC OUTPUT SIGNALS

9.4 PMC TIMERS

Port Address 8072H - Read and Write

When no keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 9-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 01 and 00 (BL_MOU) in the RAM Shadow And Write Protect Register at Port Address 6072H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default RSTIN
BL_TIMEOUT †	0
LCD_TIMEOUT †	0

† Featured only in the WD7710LP

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds
↕
FEH - enabled for 254 x 5 seconds
FFH - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds
↕
FEH - enabled for 254 x 5 seconds
FFH - LCD enabled

9.5 PMC INPUTS

Port Address 8872H - Read and Write

15	14	13	12	11	10	09	08
PMC_UPD	EN_LCL	AF7	AF6	AF5	AF4	AF3	AF2

07	06	05	04	03	02	01	00
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Signal Name	Default At RSTIN
PMC_UPD	0
EN_LCL †	0
AF7-AF2 †	0
IN7-IN0	None

† Featured only in the WD7710LP

Bit 15 - PMC_UPD, Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (Port Address 7072H) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

Bit 14 - EN_LCL, Enable Local Request - Featured only in the WD7710LP

EN_LCL enables the PMCIN 2 to initiate a local access of the WD7710LP internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

Bits 13-08 - AF7-AF2, Local Attention Flags Featured only in the WD7710LP

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

Bits 07-00 - IN7-IN0, PMC Inputs 7-0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7 through IN0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 9-2.

9.6 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
Non-maskable Interrupt Enable							

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
Local Attention Enable							

Signal Name	Default At RSTIN
EI7-EI2 †	0
EA7-EA2 †	0

† Featured only in the WD7710LP

Bits 15-10 - EI7-EI2, Non-maskable Interrupt Enable 7 through 2 - Featured only in the WD7710LP

EI7 through EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7 through IN_2 in Port 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Non-maskable Interrupt not enabled

EI7-EI2 = 1 -
Non-maskable Interrupt is enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Local Attention Enable Featured only in the WD7710LP

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled

Bits 01, 00 - Not used, state is ignored

9.7 NMI STATUS

Port Address 9072H - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
	Non-maskable Interrupt Flags						

Signal Name	Default At RSTIN
IF7-IF2 †	0-0

† Featured only in the WD7710LP

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Non-maskable Interrupt Flags 7 through 2 - Featured only in the WD7710LP

NMI interrupt flags IF7 through IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

Bits 01, 00 - Not used, must be 0

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PMC INPUT NUMBER[1]	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER[2]
00H	$\overline{\text{TURBO}}$		
01H	PROC_PWR_GOOD		
02H	LCL_REQ or User Defined	Transistion	IF2 or AF2
03H	User Defined	Transistion	IF3 or AF3
04H	User Defined	Transistion	IF4 or AF4
05H	User Defined	Transistion	IF5 or AF5
06H	User Defined	Transistion	IF6 or AF6
07H	User Defined	Active Edge	IF7 or AF7

1 Port Address 8872H, section 9.5
2 Port Address 9072H, section 9.7
Port Address 8872H, section 9.5

TABLE 9-2. PMCIN INPUTS

9.8 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN
All signals	None

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

9.9 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the WD7710. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

15	14	13	12	11	10	09	08
AMT OUT	DEV		TM7	TS7	S F N M	AUT_ EOI	RA_ EOI

07	06	05	04	03	02	01	00
PLM2 PLM1 PLM0 Priority Level Master			PLS2 PLS1 PLS0 Priority Level Slave			SMM M	SMM S

Signal Name	Default At RSTIN
Bits 15, 12-00	None
Bits 14, 13	00

Bit 15 - AMTOUT, Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

Bit 14, 13 - DEV, Device

DEV identifies the device as WD7910 or WD7710 and is used in conjunction with VER at Port Address 9872H and SVER at Port Address A872H. DEV, VER and SVER are defined in Table 10.1.

Bit 12 - TM7, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 11 - TS7, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 10 - SFNM, Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD7710 does not require SFNM for the slave interrupt controller and ignores its state.

Bit 09 - AUT_EOI, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD7710 does not require AUT_EOI for the slave interrupt controller and ignores its state.

Bit 08 - RA_EOI, Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7 through 5 of OCW2). The WD7710 does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

Bits 07-05 - PLM2-PLM0, Priority Level Master

PLM2-PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bits 04-02 - PLS2-PLS0, Priority Level Slave

PLS2-PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bit 01 - SMMM, Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

Bit 00 - SMMS, Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

7

9.10 PORT 70 SHADOW REGISTER

Port Address E472

15	14	13	12	11	10	09	08
CLK 32K	REF DET	INTR	NOD MA	TOD UN	RSVD	RSVD	RSVD

07	06	05	04	03	02	01	00
NMI MSK	RTC IR6	RTC IR5	RTC IR4	RTC IR3	RTC IR2	RTC IR1	RTC IR0

This register provides read-only information on the status of interrupts and DMA which is useful for determining when the processor may be put to sleep. Two bits are also provided for generating software delays without incurring the operating system traps that would result from accessing I/O port 0061 in virtual 86 mode. This register also contains a shadow of the real time clock address register, a write only I/O port. It is necessary to access the real-time clock CMOS RAM during Suspend/Resume operations. This shadow of Port 0070 allows it to be restored to the same state it was in at suspend time.

This register can be read without first unlocking the WD7710. This is important since the CLK32K, REFDET, and TODUN bits may need to be read frequently.

Bit 15 - CLK32K

This read-only bit is a divide by 2 of the PDREF input. It can be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 microsecond period with a 50% duty cycle.

Bit 14 - REFDET

This read-only bit is a copy of the REFDET bit available from I/O Port 0061, Bit 4.

Bit 13 - INTR

This read-only bit gives the state of the INTR output pin to the CPU.

Bit 12 - NODMA, No DMA

This read-only bit is set whenever it has been at least 30.5 microseconds since the last DMA or bus master cycle occurred.

Bit 11 - TODUN, Time of Day Update Needed (R/W)

This is a general purpose storage bit which can be written and read but has no effect on internal logic. Its purpose is to allow an SMI handler to signal the operating system that the time of day has been corrupted. This bit is checked by the Timer 0 Interrupt Handler. Note that although this bit is readable without unlocking the WD7710, it cannot be written unless the WD7710 is unlocked.

Bits 10:8 - RSVD

These read-only bits are reserved for future use. They currently are read back as a 0.

Bit 7 - NMIMSK, NMI Mask

This read-only bit gives the state of the NMI mask bit as it was set the last time I/O port 0070 was written.

Bits 6:0 - RTCIR6-0

These read-only bits give the state of the real time clock address register as it was set the last time I/O port 0070 was written.

9.11 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13-11, 08-00 Read and Write Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in section 9.12.

15	14	13	12	11	10	09	08
IRR AE	CB12	AM TM	ACT LCH	IND ET	ACT AFT	ACT BEF	AM EN

07	06	05	04	03	02	01	00
Coarse Timeout Count AMC7 AMC6 AMC5 AMC4				Fine Timeout Count AMC3 AMC2 AMC1 AMC0			

Signal Name	Default At RSTIN
IRRAE	0
CB12	None
AMTM	0
ACTLCH	None
INDET	None
ACTAFT	None
ACTBEF	None
AMEN	0
AMC7-AMC0	0-0

Bit 15 - IRRAE, Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

Bit 14 - CB12, Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

Bit 13 - AMTM, Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

Bit 12 - ACTLCH, Activity Latch

This latch is always enabled, regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

Bit 11 - INDET, Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07-00) to be reached.

NOTE

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

Bit 10 - ACTAFT, Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -
Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

Bit 09 - ACTBEF, Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -
Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC7-AMC0 (bits 07-00). It would be necessary for the routine to clear the software counter if ACTBEF were set, since there would have been no activity only for the period of time programmed in AMC7-AMC0.

Bit 08 - AMEN, Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -
Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -
Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected, the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM7 through ACM0, INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

Bits 07-04 - AMC7-AMC4, Activity Monitor Counter Coarse

AMC7-AMC4 establish the timeout values from 64 seconds to 16 minutes in 64-second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC7	AMC6	AMC5	AMC4	
0	0	0	0	0 seconds
0	0	0	1	1 min., 4s
0	0	1	0	2 min., 8s
0	0	1	1	3 min., 12s
0	1	0	0	4 min., 16s
0	1	0	1	5 min., 20s
0	1	1	0	6 min., 24s
0	1	1	1	7 min., 28s
1	0	0	0	8 min., 32s
1	0	0	1	9 min., 36s
1	0	1	0	10 min., 40s
1	0	1	1	11 min., 44s
1	1	0	0	12 min., 48s
1	1	0	1	13 min., 52s
1	1	1	0	14 min., 56s
1	1	1	1	16 min., 0s

Bits 03-00 - AMC3-AMC0, Activity Monitor Counter Fine

AMC3-AMC0 establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC3	AMC2	AMC1	AMC0	
0	0	0	0	0 ms
0	0	0	1	7.8 ms
0	0	1	0	15.6 ms
0	0	1	1	23.4 ms
0	1	0	0	31.3 ms
0	1	0	1	39.1 ms
0	1	1	0	46.9 ms
0	1	1	1	54.7 ms
1	0	0	0	62.5 ms
1	0	0	1	70.3 ms
1	0	1	0	78.1 ms
1	0	1	1	85.9 ms
1	1	0	0	93.8 ms
1	1	0	1	101.6 ms
1	1	1	0	109.4 ms
1	1	1	1	117.2 ms

NOTE

The fine timeout delay (AMC3 through AMC0) is added to the coarse timeout delay (AMC7 through AMC4) to obtain the total timeout delay.

9.12 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

15	14	13	12	11	10	09	08
PCSM	PMCILS	PMCIS2	PMCIS1	PMCIS0	NMIM	HDDM	COPM

07	06	05	04	03	02	01	00
IMS1	IMS0	IRR8M	IRR7M	IRR0M	ISR8M	ISR7M	ISR0M

Signal Name	Default RSTIN
All signals	0

Bit 15 - PCSM, Programmable Chip Select Mask

PCSM = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7710LP are considered activity.

PCSM = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7710LP are ignored.

Bit 14 - PMCILS, Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13-11, PMCIS2-0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

Bits 13-11 - PMCIS2-PMCIS0, Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

NOTE

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

PMCIS 2 1 0
0 0 0 - PMC input 2 selected
0 0 1 - PMC input 3 selected
0 1 0 - PMC input 4 selected
0 1 1 - PMC input 5 selected
1 0 0 - PMC input 6 selected
1 0 1 - PMC input 7 selected
1 1 0 - Reserved
1 1 1 - Disabled, no PMC inputs checked

Bit 10 - NMIM, Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

Bit 9 - HDDM, Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

Bit 8 - COPM, Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. For an 80286 system, this is I/O address range 00F8H through 00FFH. For an 80386SX system, this is when A23 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

Bits 07, 06 - IMS1-0, Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS1 through 0 provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

IMS 1 0
0 0 - IRQ5 masked
0 1 - IRQ10 masked
1 0 - IRQ11 masked
1 1 - IRQ15 masked

Bit 05 - IRR8M, Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register

at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

NOTE
See Test Enable Register (A872), Section 11.3 for information about IRQ9 enable control.

Bit 04 - IRR7M, Interrupt Request Register 7 Mask

IRR7M = 0 -
Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -
Parallel Port or Spurious Interrupt (IRR7) is ignored.

Bit 03 - IRR0M, Interrupt Request Register 0 Mask

IRR0M = 0 -
Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -
Time Of Day Interrupt (IRR0) is ignored.

Bit 02 - ISR8M, Interrupt Service Register 8 Mask

ISR8M = 0 -
Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -
Real-Time Clock Interrupt (ISR8) is ignored.

Bit 01 - ISR7M, Interrupt Service Register 7 Mask

ISR7M = 0 -
Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -
Parallel Port or Spurious Interrupt (ISR7) is ignored.

Bit 00 - ISR0M, Interrupt Service Register 0 Mask

ISR0M = 0 -
Time of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -
Time Of Day Interrupt (ISR0) is ignored.

9.13 3V Suspend Shadow Registers

The 3V suspend mode provides maximum power savings for the system. The contents of the DRAM, chip set registers, CPU registers and video RAM are all written to the hard disk and then all voltages are shut down, including the power supply. The only logic left on in this mode is the real-time clock and a 3V suspend controller. The real-time clock and the 3V suspend controller run off of the real-time clock battery. When the resume request is sampled by the suspend controller, the suspend controller enables the power supply and resumes the system.

To maintain compatibility with the IBM AT, the timer and DMA registers cannot be read back. To overcome this, these registers are shadowed and read back through other registers. (See descriptions for registers 3C72, 4472 and 4C72.)

9.13.1 DMA Shadow Register 1

Port Address 3C72H (R)

15	14	13	12	11	10	09	08
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

07	06	05	04	03	02	01	00
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

Bit 15, the AD_DEC bit of register 0B for DMA channel 2.

Bit 14, the AUTO bit of register 0B for DMA channel 2.

Bits 13:12, the TRA_TYP bits of registers 0B for DMA channel 1.

Bits 11:10, the TRA_MOD bits of register 0B for DMA channel 1.

Bit 9, the AD_DEC bit of register 0B for DMA channel 1.

Bit 8, the AUTO bit of register 0B for DMA channel 1.

Bits 7:6, the TRA_TYP bits of register 0B for DMA channel 1.

Bits 5:4, the TRA_MOD bits of register 0B for DMA channel 0.

Bit 3, the AD_DEC bit or register 0B for DMA channel 0.

Bit 2, the AUTO bit of register 0B for DMA channel 0.

Bits 1:0, the TRA_TYP bits of register 0B for DMA channel 0.

9.13.2 DMA Shadow Register 2

Port Address 4472H (R)

15	14	13	12	11	10	09	08
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

07	06	05	04	03	02	01	00
TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD

Bits 15:14, the TR_TYP bits of register 0D6 for channel 6.

Bits 13:12, the TRA_MOD bits of register 0D6 for channel 5.

Bit 11, the AD_DEC bit of register 0D6 for channel 5.

Bit 10, the AUTO bit of register 0D6 for channel 5.

Bits 9:8, the TRA_TYP bits of register 0D6 for channel 5.

Bits 7:6, the TRA_MOD bits of register 0B for channel 3.

Bit 5, the AD_DEC bit of register 0B for channel 3.

Bit 4, the AUTO bit of register 0B for channel 3.

Bit 3:2, the TRA_TYP bits of register 0B for channel 3.

Bits 1:0, the TRA_MOD bits of register 0B for channel 2.

9.13.3 DMA Shadow Register 3

Port Address 4C72H (Read only for bits 14:0)

15	14	13	12	11	10	09	08
SCB		EX_ WR	RO_ PRI		CO_ DIS	TRA_ MOD	TRA_ MOD

07	06	05	04	03	02	01	00
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

Bit 15, Shadow Control BIT (SCB)

Bit 14, Reserved

Bit 13, When SCB is low, this bit represents the EX_WR bit of register 08. When SCB is high, this bit represents the EX_WR bit of register of register 0D0.

Bit 12, When SCB is low, this bit represents the RO_PRI bit of register 08. When SCB is high, this bit represents the RO_PRI bit of register 0D0.

Bit 11, Reserved.

Bit 10, When SCB is low, this bit represents the CO_DIS bit of register 08. When SCB is high, this bit represents the CO_DIS bit of register 0D0.

Bits 9:8, These bits represent the TRA_MOD bits of register 0D6 for channel 7.

Bit 7, AD_DEC bit of register 0D6 for channel 7.

Bit 6, AUTO bit of register 0D6 for channel 7.

Bits 5:4, the TRA_TYP bits of register 0D6 for channel 7.

Bits 3:2, the TRA_MOD bits of register 0D6 for channel 6.

Bit 1, the AD_DEC bit of register 0D6 for channel 6.

Bit 0, the AUTO bit of register 0D6 for channel 6

9.13.4 DMA Base Address and Count Register

When the SCB is high, the DMA base aaddress and base count can be read back from register 0 to 7. When SCB is low, register 0 to 7 represents the current address and current count.

9.13.5 Timer Count

When SCB is high, the timer base count can be read back from register 40:43. When SCB is low, the register 40:43 represents the timer current count.

9.14 SAVE AND RESUME

When the WD7710LP is in the Save And Resume Mode, it typically draws less than 500 µA. Figures 9-2 and 9-3 illustrate the steps that the WD7710LP goes through during power down and power up.

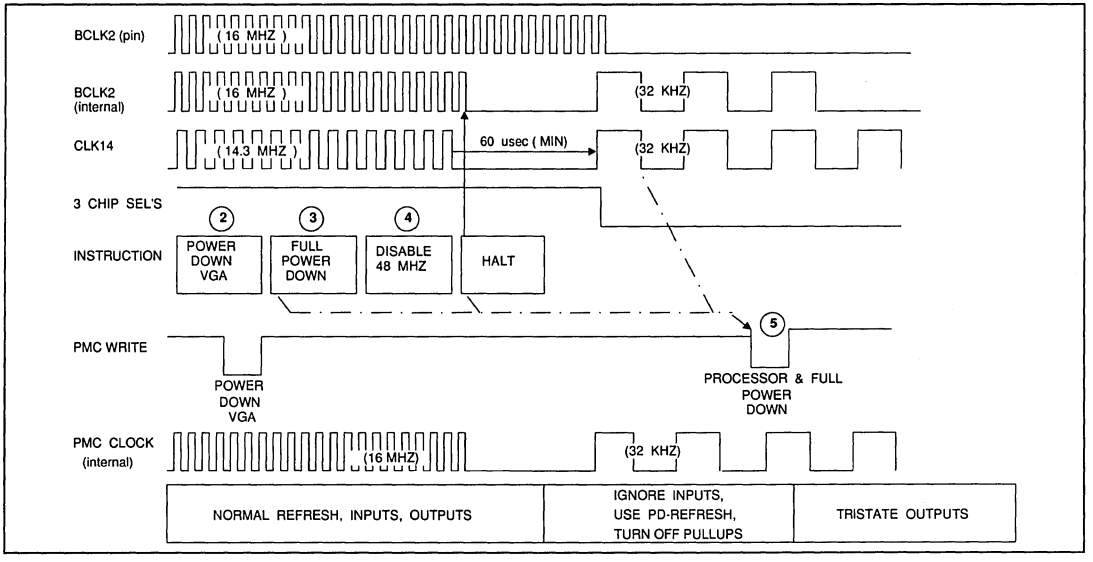

FIGURE 9-2. POWER DOWN

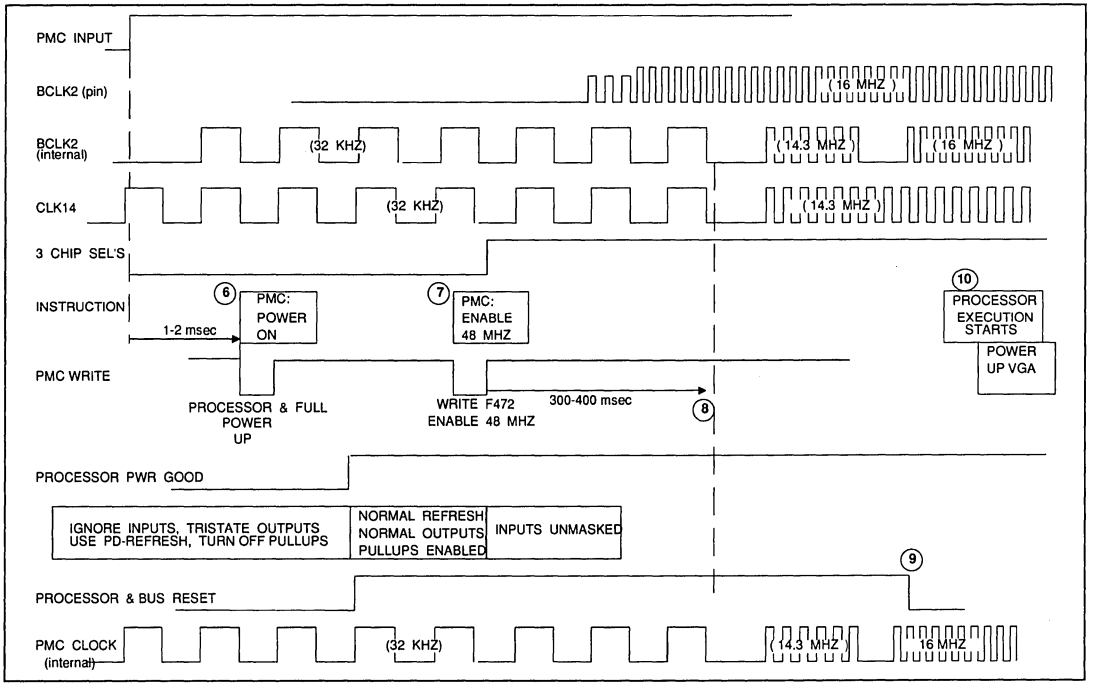

FIGURE 9-3. POWER UP

10.0 DIAGNOSTIC MODE

Simultaneously asserting MASTER, MEMR and MEMW while RSTIN is asserted, causes all output pins to become tristated. The outputs remain tristated if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted and any of the MASTER, MEMR or MEMW are not asserted. The output tristate mode allows an in-circuit board tester to drive the WD7710's output pins.

I/O Pin Mapping Mode

The I/O Pin Mapping Mode provides the in-circuit tester for evaluating the connectivity of the WD7710 to the printed circuit board. Simultaneously asserting MASTER, MEMR, MEMW when A1 is high, A2 is low, and RSTIN is asserted, causes the WD7710 to switch to I/O Mapping Mode. The WD7710 stays in this mode if RSTIN is deasserted while MASTER, MEMR, and MEMW are asserted.

Full Tristate Mode

Simultaneously asserting MASTER, MEMR, and MEMW with A1 low and A2 high while RSTIN is asserted, causes all the output pins of the WD7710 to tristate and disablesall the pullup and pulldown register. The WD7710 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test for leakage current of the device.

Pullup and Pulldown Test Mode

Simultaneously asserting MASTER, MEMR, MEMW with A1 and A2 high while RSTIN is asserted, causes all the output pins of the WD7710 to become tristated and enables all the pullup and pulldown resistors. The WD7710 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test the pullup and pulldown resistors of the device.

10.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

15	14	13	12	11	10	09	08
RSVD			CLK_TST	REF_MAS	AUT_A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
AUT_A20	0
Bit 09	None
CLK_SW	0
SX	None
DS	0
DIAG	0-0

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - AUT_A20, Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 9-1).

AUT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

AUT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX Processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, Diagnostic Function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 10-1. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

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DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	Reserved
00010	Reserved	10010	Reserved
00011	Reserved	10011	Reserved
00100	Reserved	10100	Reserved
00101	Reserved	10101	Reserved
00110	Reserved	10110	Reserved
00111	Reserved	10111	Reserved
01000	Reserved	11000	Reserved
01001	Reserved	11001	Reserved
01010	Reserved	11010	Reserved
01011	Reserved	11011	Reserved
01100	Reserved	11100	Reserved
01101	Reserved	11101	Reserved
01110	Reserved	11110	Reserved
01111	Reserved	11111	Reserved

TABLE 10-1. DIAGNOSTIC TESTS

10.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default RSTIN
Bits 15-08	None
LAT	0
DL	0
DELAY	None

Bit 07 - LAT, Latch Output Strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

10.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15-10 Read only
Bits 09-00 Read and Write

The test function bits 07-03 are for factory use only.

15	14	13	12	11	10	09	08
SVER				BF40	BC40	IRQ9 EN	TDL

07	06	05	04	03	02	01	00
OLD IHLD	BFC 3	BIST 3	BFC 40	BIST 40	EN_ PLD	DISFA	EN_ LVL

Signal Name	Default At RSTIN
All signals	0-0

Bits 15-12 - SVER, Secondary Version Number.

See VER at Port Address 9872H.

PORT ADDRESS D472H DEVICE - Bits 14, 13			PORT ADDRESS A872H SECONDARY VERSION - Bits 15-12				
14	13	Device	15	14	13	12	Rev
0	0	WD76C10	0	0	0	0	A
0	1	WD7710/7910	0	0	0	1	B
1	0	Reserved	0	0	1	0	C
1	1	Reserved	-	-	-	-	-
			1	1	1	1	P

Bit 11 - BF40, EMS Register Self Test Status

Bit 10 - BC40, EMS Register Self Test Status

Bit 09 - IRQ9EN = 0, Masks IRR9 and ISR9 so that the System Activity Monitor does not detect these signals. This prevents vertical retrace from being a source of activity for SAM.

IRQ9EN = 0 ,
Masking of IRR9 and ISR9 enabled

IRQ9EN = 1,
Masking disabled

Bit 08 - TDL, Test Delay Line.

Bit 07 - OLD_IHLD,

OLD_IHLD = 0 -
SX test not enabled

OLD_IHLD = 1 -
SX test enabled

Bit 06 - BFC3,

BFC3 = 0 -
DMA register file test

BFC3 = 1 -
DMA register file test

Bit 05 - BIST3,

BIST3 = 0 -
DMA register file test

BIST3 = 1 -
DMA register file test

Bit 04 - BFC40,

BFC40 = 0 -EMS mapping RAM

BFC40 = 1 -EMS mapping RAM

Bit 03 - BIST40,

BIST40 = 0 -
EMS mapping RAM

BIST40 = 1 -
EMS mapping RAM

Bit 02 - EN_PLD, Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23 through A00, and on processor data lines D15 through D00.

Bit 01 - DISFA, Disable First Access

DISFA = 0 -
First access Page Mode cycles are not disabled.

DISFA = 1 -
First access Page Mode cycles are disabled. Page Miss cycles occur instead.

Bit 00 - EN_LVL, Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of edge-sensed or level-sensed interrupts.

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10.4 TEST STATUS REGISTER

Port Address DC72H - Read only

For factory use only.

15	14	13	12	11	10	09	08
Delay Line Status CAL	MED	SLOW	DLT6	DLT5	DLT4	DLT3	DLT2

07	06	05	04	03	02	01	00
DLT1	DLT0	BF34	BF33	BF32	BF31	BF30	BC

Signal Name	Default RSTIN
All signals	None

Bit 15 - CAL, Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

Bits 14, 13 - MED, SLOW, Medium and Slow

These bits provide information regarding the output buffer strength.

MEDIUM	SLOW	
0	0	Output buffers are set to low strength (fast WD7710/7710LP).
0	1	Invalid
1	0	Output buffers are set to medium strength (medium speed WD7710/7710LP).
1	1	Output buffers are set to full strength (slow WD7710/7710LP).

Bits 12-06 - DLT6-DLT0,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7710/7710LP.

Bits 05-01 - BF34-BF30,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7710/7710LP.

Bit 00 - BC

This bit provides information about internal nodes and are for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD7710/7710LP.

11.0 DC ELECTRICAL SPECIFICATIONS

11.1 MAXIMUM RATINGS

Supply Voltage (Vcc) with respect to Vss (ground) . . . . . Vcc - Vss ≤ 7.0 Volts

Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to Vdd +0.3 Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)

Power Dissipation . . . . . 600 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

11.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
Vcc = +5V ±.25V (5%) for WD7910 and WD7910LP

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SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tristate And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD7910LP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 11-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend and resume mode

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

M/IO, PEACK, NPERR, NPBUSY, S0, S1, NPRST, CPURES, DPH, DPL

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not processor down or suspend mode

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

PMCIN, IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, BHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend mode

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

CASL3, CASL2, CASH3, SDT/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	RESET IN = 0

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

FOR PINS WITH INTERNAL PULLDOWNS:

A23-A0, D15-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current	-30	-110	µA	Processor power down or suspend mode

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage		.4	V	IOUT = 2 mA

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage		.4	V	IOUT = 4 mA

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

IOR, IOW, MEMR, MEMW, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:

REFRESH

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 11-1. DC OPERATING CHARACTERISTICS cont.

12.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into three major categories: Memory Timing Section 12.1, AT Bus Timing Section 12.2, Processor Timing Section 12.3, and Cache Controller Timing (Section 12.4).

Table 12-1 lists the timing tables and figures, and their section location.

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
12-3		80286 - Page Mode Memory Timing	12.1.1
	12-1	80286 - Page Mode First Access Read/Write	12.1.1
	↕		
	12-6	80286 - Page Mode Read Hit Followed By Write Hit	12.1.1
12-4		80286 - Non-Page Mode 00 Memory Timing	12.1.2
	12-7	80286 - Non-Page Mode 00 1 Wait State Write	12.1.2
	12-8	80286 - Non-Page Mode 00 1 Wait State Read	12.1.2
	12-9	80286 - Non-Page Mode 00 2 Wait States Read After Write	12.1.2
12-5		80286 - Non-Page Mode 01 Memory Timing	12.1.3
	12-10	80286 - Non-Page Mode 01 0 Wait State Write	12.1.3
	12-11	80286 - Non-Page Mode 01 0 Wait State Read	12.1.3
12-6		80386SX - Page Mode Memory Timing	12.1.4
	12-12	80386SX - Page Mode, First Access Read/Write	12.1.4
	↕		
	12-17	80386SX - Page Mode, Write Miss Following A Write	12.1.4
12-7		80386SX - Non-Page Mode 00 And Mode 01	12.1.5
	12-18	80386SX - Non-Page Mode 00 1 Wait State Read	12.1.5
	↕		
	12-21	80386SX - Non-Page Mode 00 1 Wait State Read	12.1.5
12-8		CPU Initiated AT Bus Cycles	12.2.1
	12-22	AT Bus I/O Or Memory Read: 8-Bit, Default Timing	12.2.1
	↕		
	12-31	AT Bus I/O Or Memory Write: 16-Bit, Default Timing	12.2.1
12-9		Entering The AT Bus	12.2.2
	12-32	80286 CPU - Asysnchronous CPUCLK To SYSCLK, BREQ Delay = 1/2 Clock	12.2.2
	↕		
	12-37	80386SX CPU - Synchronous CPUCLK To SYSCLK	12.2.2
12-10		Exiting The AT Bus	12.2.3
	12-38	Synchronous AT Bus Cycle Completion, AT Bus Clock = 1/2 CPUCLK	12.2.3
	↕		
	12-41	Asynchronous AT Bus Cycle Completion, BAK_DEL = 0 Or +0.5 AT Bus Cycles	12.2.3
12-11		DMA Entering And Exiting The AT Bus	12.2.4
	12-42	Basic DMA Cycle, Default Timing	12.2.4
	12-43	DMA Cycle, 8-Bit I/O To On-board Memory	12.2.4
	12-44	DMA Cycle, On-board Memory To 8-Bit I/O	12.2.4
12-12		AT Bus Master Cycle	12.2.5
	12-45	AT Bus Master, Bus Acquisition/Release	12.2.5
	12-46	AT Bus Master, Write To On-board Memory	12.2.5
	12-47	AT Bus Master, Read From On-board Memory	12.2.5
12-13		AT Bus Refresh Cycle, Default Timing	12.2.5
	12-48	AT Bus Refresh Cycle, Default Timing	12.2.5

TABLE 12-1. TIMING FIGURE/TABLE NUMBERS

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
12-14		80286 CPU TIMING	12.3
	12-49	80286 - CPURES AND NPRST DURING POWER UP	12.3
	↕		
	12-54	80286 - MISCELLANEOUS TIMING	12.3
12-15		80386SX CPU TIMING	12.3
	12-55	80386SX - CPURES AND NPRST DURING POWER UP	12.3
	↕		
	12-62	80386SX - OUTPUT DELAY TIMING	12.3

TABLE 12-1. TIMING FIGURE/TABLE NUMBERS cont.

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
CPURES	50 pF	NPRST	50 pF	$\overline{BHE}$	50 pF
W/$\overline{R}$	50 pF	ALE	50 pF	$\overline{DEN1}$, $\overline{DEN0}$	50 pF
$\overline{SDEN}$	50 pF	DT/$\overline{R}$	50 pF	SDT/$\overline{R}$	50 pF
$\overline{MXCTL2 - 0}$	50 pF	DACKEN	50 pF	$\overline{CSEN}$	50 pF
$\overline{LOMEG}$	50 pF	SPKR	50 pF	$\overline{READY}$	50 pF
$\overline{HOLD}$	50 pF	INTRQ	50 pF	NMI	50 pF
$\overline{BUSYCPU}$	50 pF	EPEREQ	50 pF	$\overline{A23 - A0}$	60 pF
$\overline{CPUCLK}$	70 pF	SYSCLK	75 pF	$\overline{CASH3 - 0}$	75 pF
$\overline{CASL3 - 0}$	75 pF	$\overline{D15 - D0}$	100 pF	$\overline{DPH}$	100 pF
$\overline{DPL}$	100 pF	$\overline{RAS3 - RAS0}$	150 pF	$\overline{IOW}$	200 pF
$\overline{IOR}$	200 pF	$\overline{MEMW}$	200 pF	$\overline{MEMR}$	200 pF
LA20	200 pF	$\overline{SA0}$	200 pF	AEN	200 pF
BALE	200 pF	$\overline{REFRESH}$	200 pF	RA10 - RA0	350 pF

TABLE 12-2. SIGNAL LOADING

12.1 MEMORY TIMING

Sections 12.1.1 through 12.1.5 present the memory timing for Page Mode and Non-Page Mode, for the 80286 and 80386SX processors.

Categories are grouped as follows:

80286
- Page Mode
- Non-Page Mode 00
- Non-Page Mode 01

80386SX
- Page Mode
- Non-Page Mode 00 and 01

Mnemonics used in the timing diagrams and tables are defined as:

TC - Command Cycle
TW - Wait State Cycle
TS - Status Cycle
WNRDRAM - Write Not Read DRAM (W/$\overline{R}$ pin 119).

12.1.1 80286 Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T220	Processor address to RAM address valid, Page Hit	32	30
T221	CPUCLK fall to $\overline{CAS}$ fall, 2.5 CLK CAS	36	34
T222	CPUCLK rise to $\overline{CAS}$ rise	29	27
T223	CPUCLK rise to $\overline{CAS}$ fall, 2.0 CLK CAS	30	26
T224	Processor data to parity valid	25	22
T225	CPUCLK fall to RAM address valid, Page Miss	39	36
T226	CPUCLK fall to WNRDRAM rise	34	31
T227	CPUCLK rise to $\overline{RAS}$ fall, first access	28	26
T228	CPUCLK fall to column address valid	44	41
T229	CPUCLK fall to WNRDRAM fall	34	31
T232	CPUCLK fall to $\overline{RAS}$ rise, Page Miss	29	27
T233	CPUCLK rise to $\overline{RAS}$ fall, Page Miss	28	26
T234	CPUCLK rise to READY rise	24	22
T235	CPUCLK rise to READY fall	24	22

TABLE 12-3. 80286 - PAGE MODE MEMORY TIMING

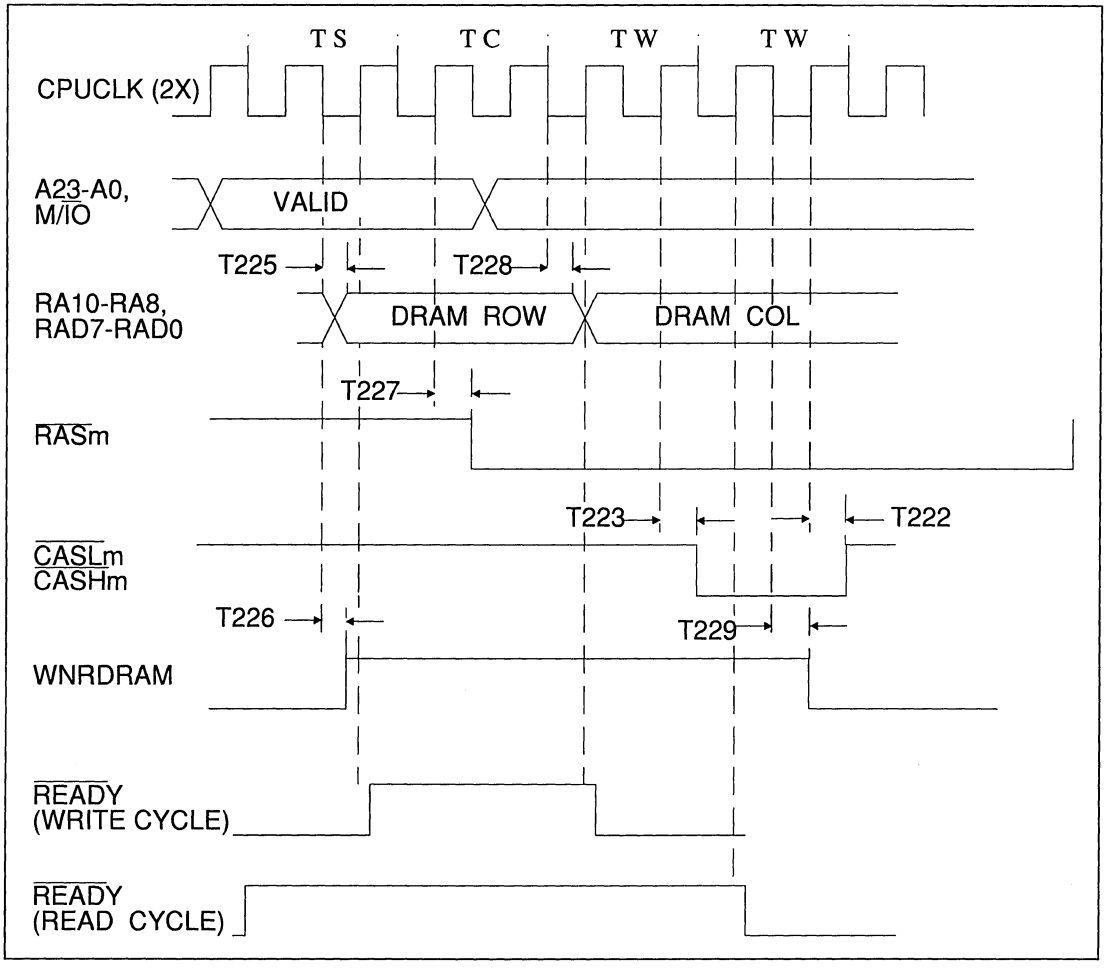

FIGURE 12-1. 80286 - PAGE MODE FIRST ACCESS READ/WRITE

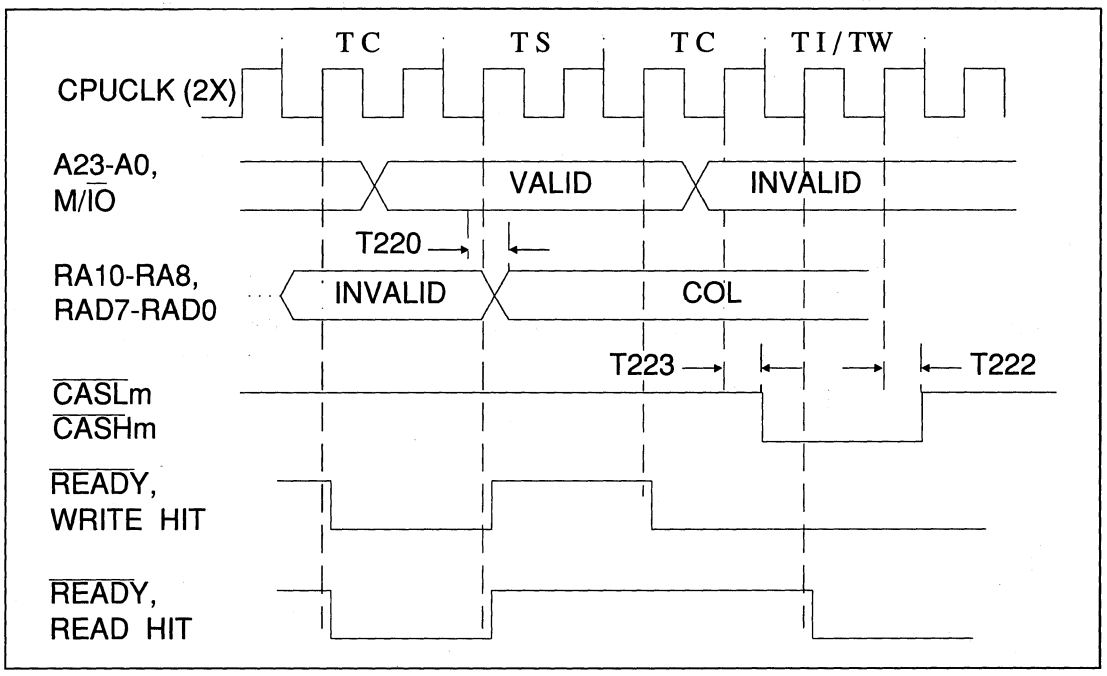

FIGURE 12-2. 80286 - PAGE MODE READ CYCLE AND PAGE HIT

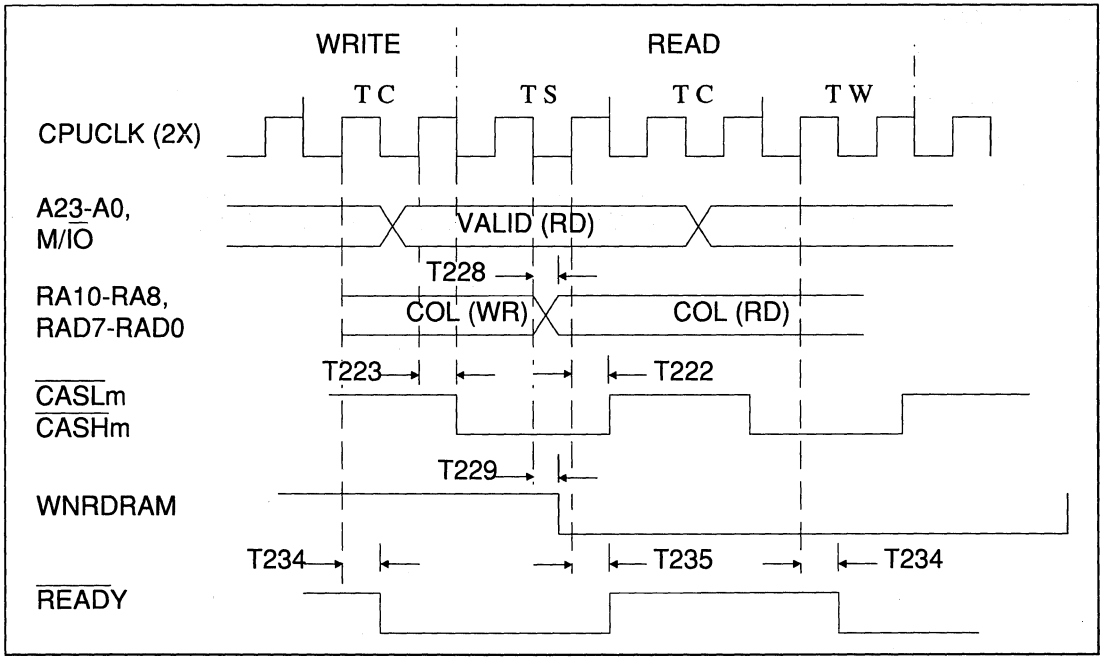

FIGURE 12-3. 80286 - PAGE MODE READ AFTER WRITE

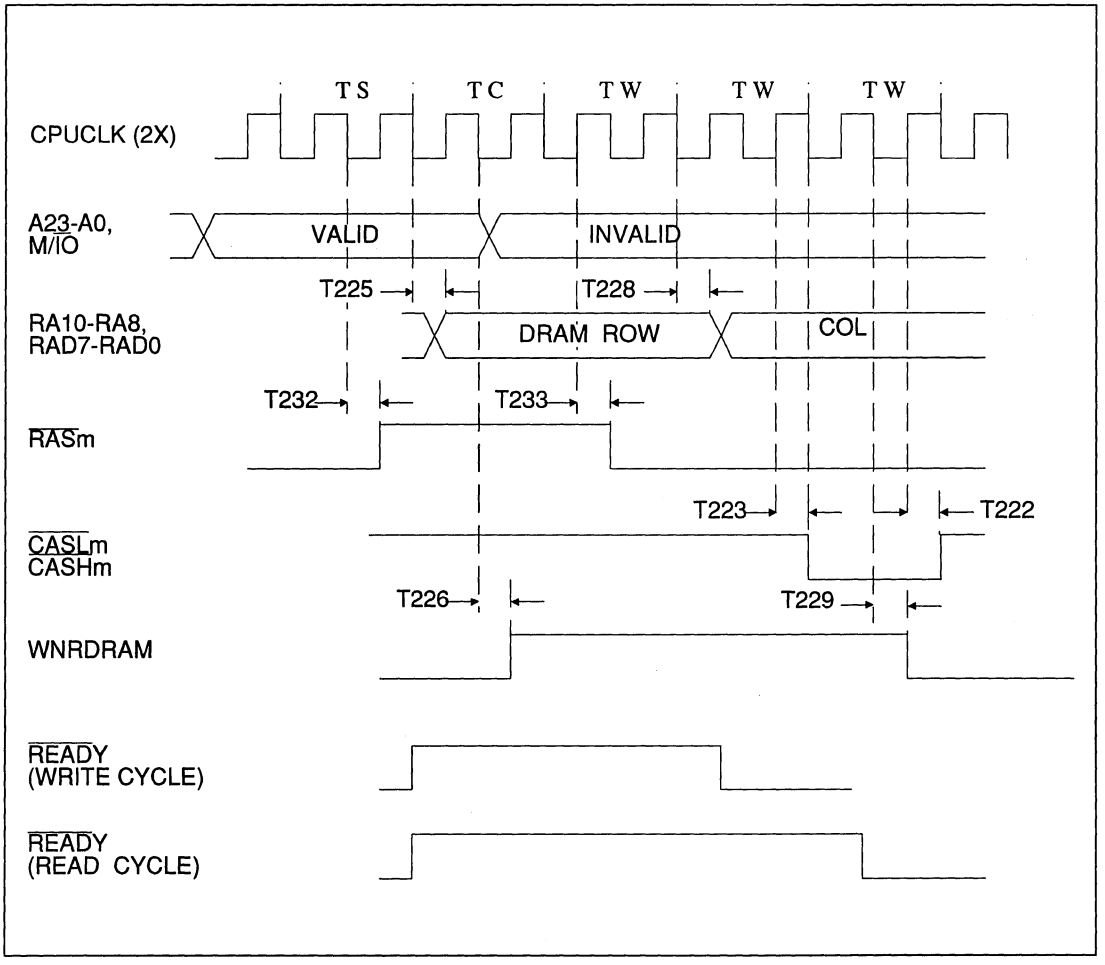

FIGURE 12-4. 80286 - PAGE MODE, PAGE MISS READ/WRITE

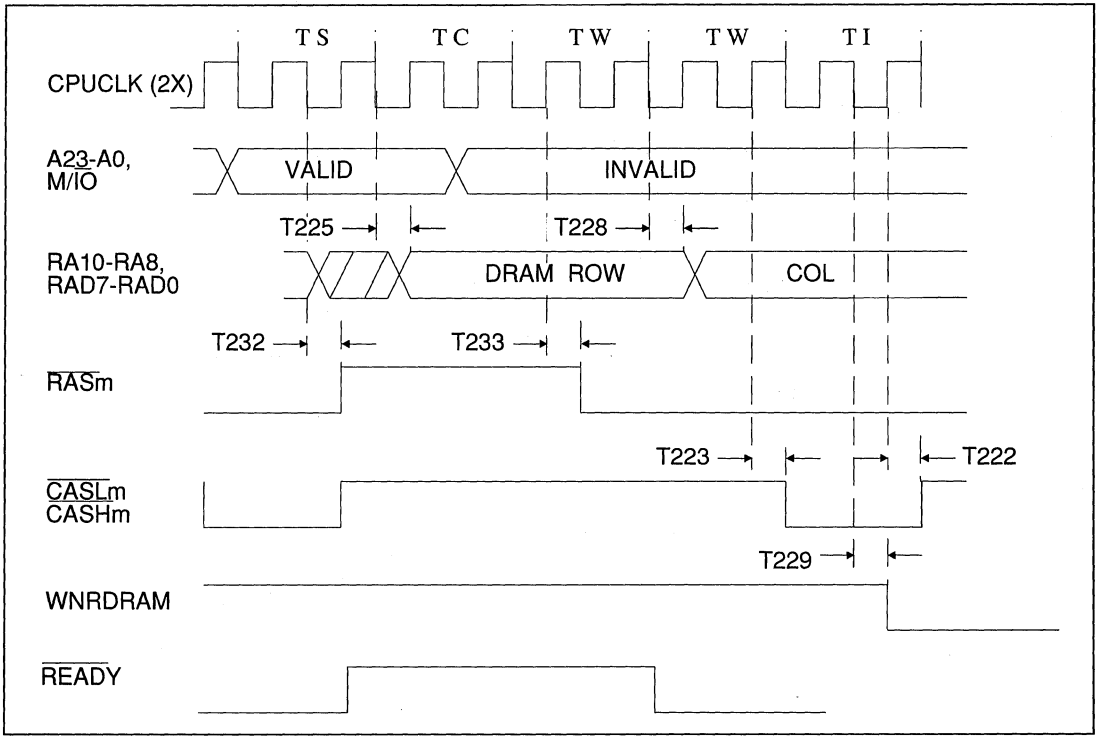

FIGURE 12-5. 80286 - PAGE MODE, WRITE MISS AFTER WRITE

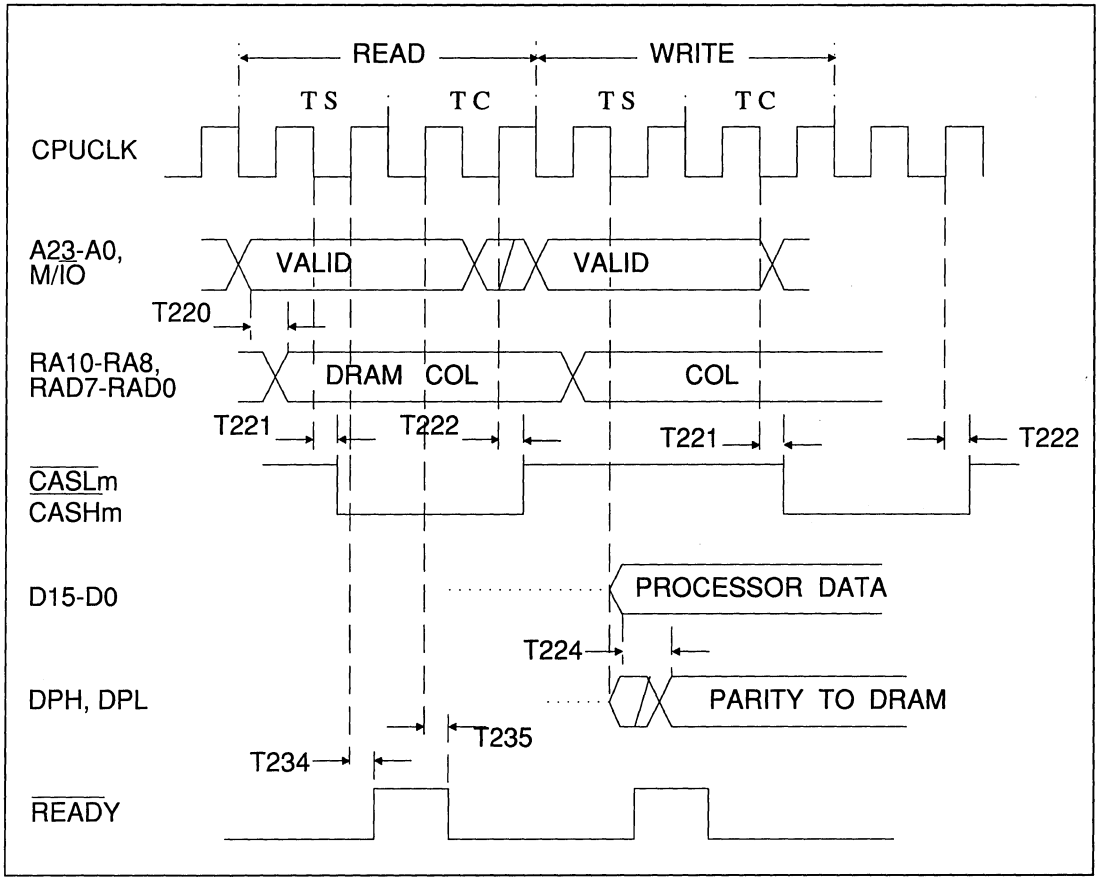

FIGURE 12-6. 80286 - PAGE MODE READ HIT AND WRITE HIT

12.1.2 80286 Non-Page Mode 00 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T234	See Table 13-3		
T235	See Table 13-3		
T252	CPUCLK fall to $\overline{CAS}$ rise	33	30
T255	CPUCLK fall to $\overline{RAS}$ fall	35	32
T270	CPUCLK fall to ROW address	46	42
T271	CPUCLK fall to $\overline{CAS}$ fall	37	34
T273	CPUCLK fall to WNRDRAM fall	33	31
T274	CPUCLK fall to WNRDRAM rise	33	31
T275	Data holding tristate. ①	12	12
T276	Clock fall to parity valid	30	27
T277	CPUCLK fall to RAS rise	30	28
T278	CPUCLK fall to COLUMN address valid	41	38
T279	Processor address to ROW address	32	30

① Tristate times are not tested. Timing specifications are derived from simulation.

TABLE 12-4. 80286 - NON-PAGE MODE 00 MEMORY TIMING

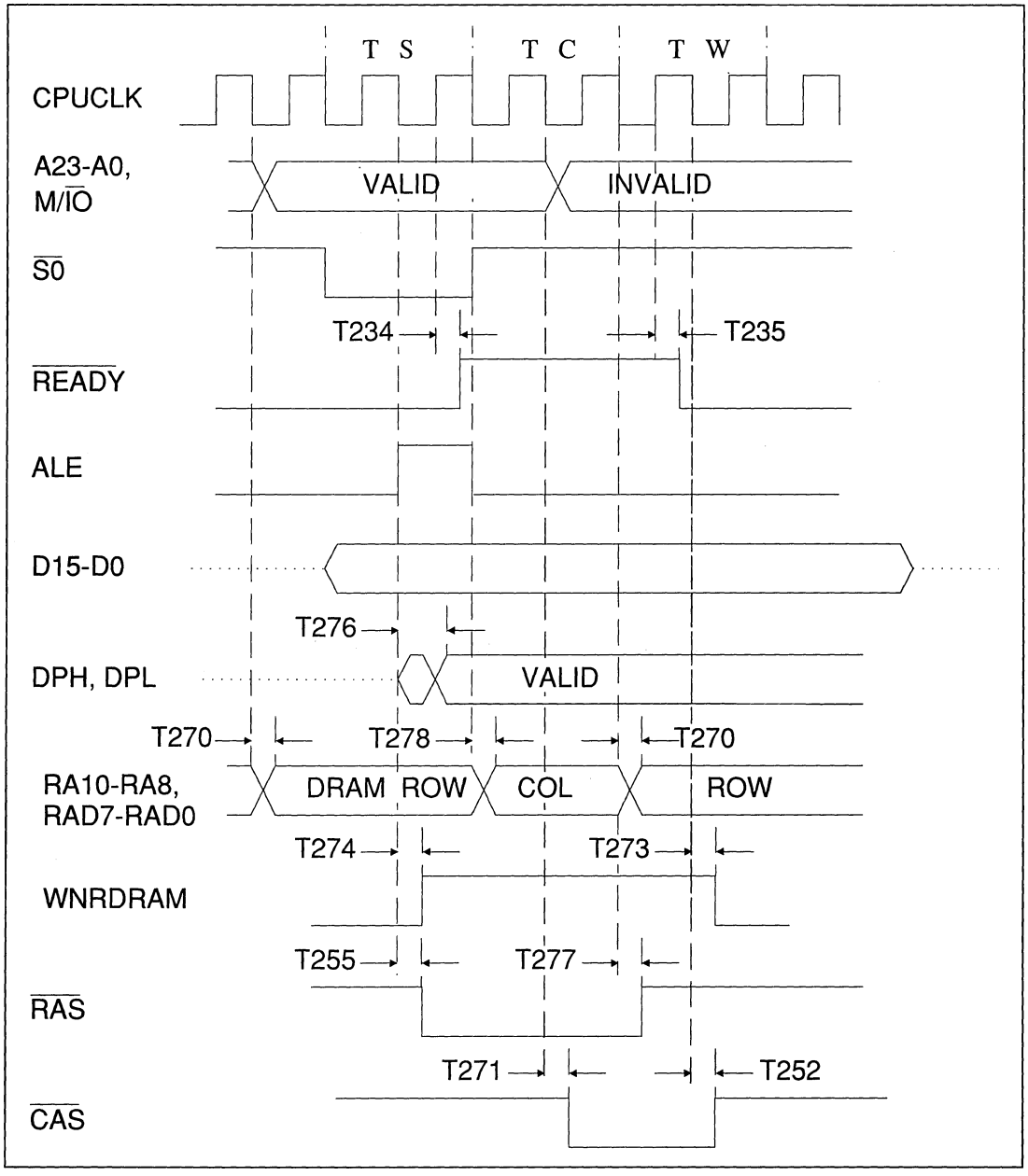

FIGURE 12-7. 80286 - NON-PAGE MODE 00, 1 WAIT STATE WRITE (4072H = 0001)

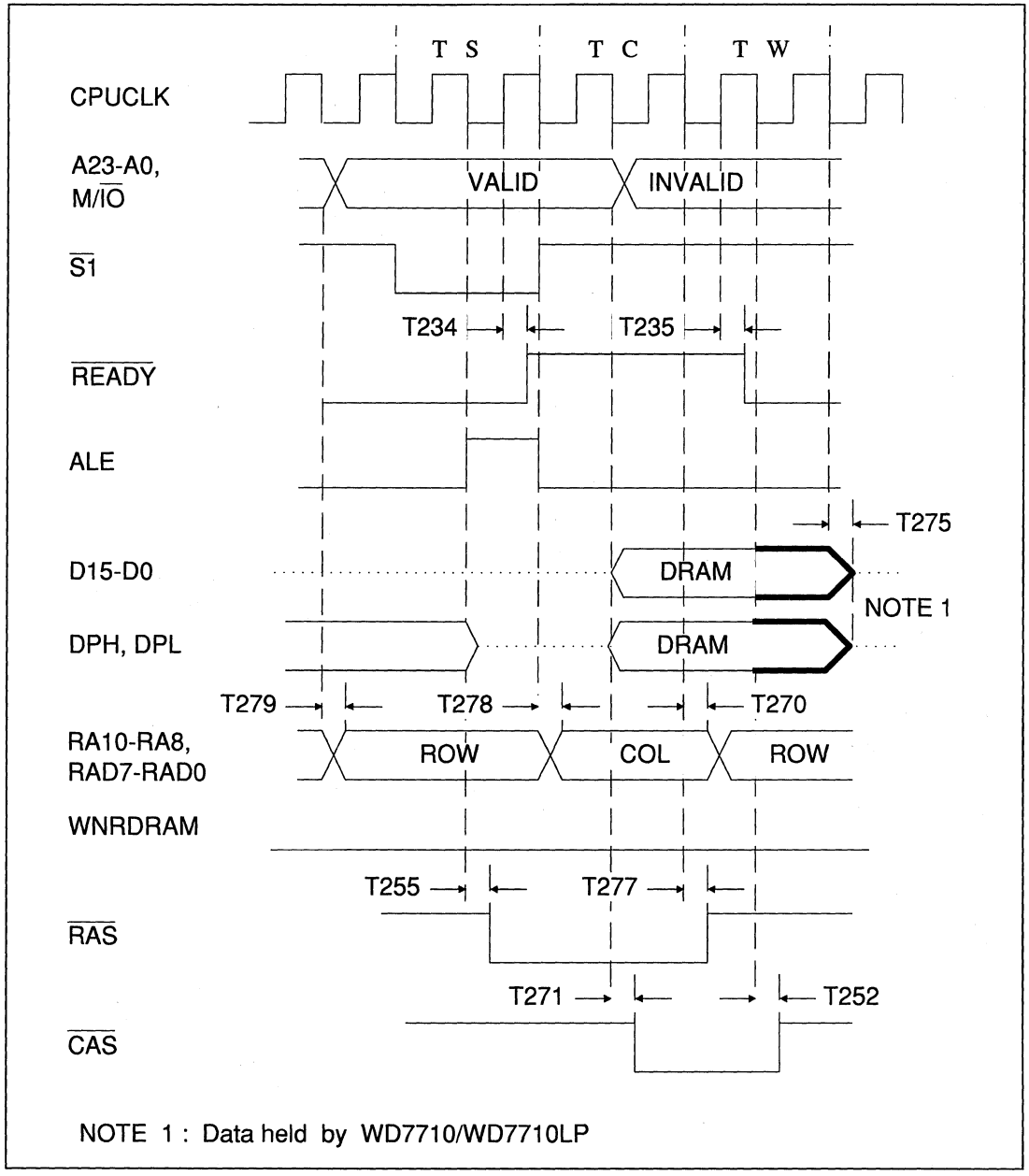

FIGURE 12-8. 80286 - NON-PAGE MODE 00, 1 WAIT STATE READ (4072H = 0001)

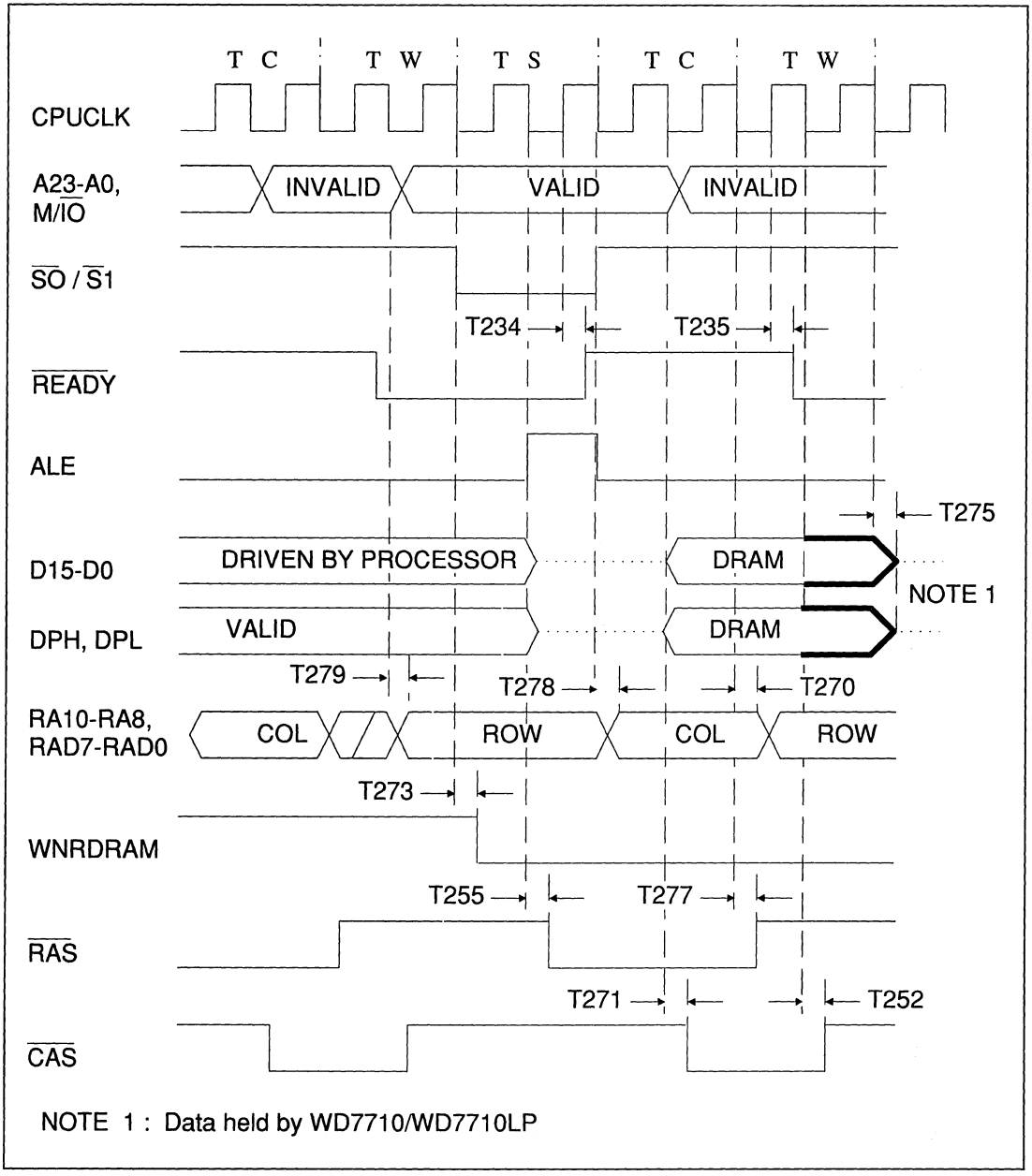

FIGURE 12-9. 80286 - NON-PAGE MODE MODE 00, 2 WAIT STATES READ AFTER WRITE (4072H = 0001)

12.1.3 80286 Non-Page Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T224	See Table 12-3		
T234	See Table 12-3		
T235	See Table 12-3		
T252	See Table 12-4		
T253	CPUCLK fall to WNRDRAM fall	34	31
T254	CPUCLK fall to WNRDRAM rise	34	31
T255	See Table 12-4		
T257	CPUCLK rise to $\overline{RAS}$ rise	35	32
T258	CPUCLK rise to COLUMN address valid	44	40
T276	See Table 12-4		

TABLE 12-5. 80286 - NON-PAGE MODE 01 MEMORY TIMING

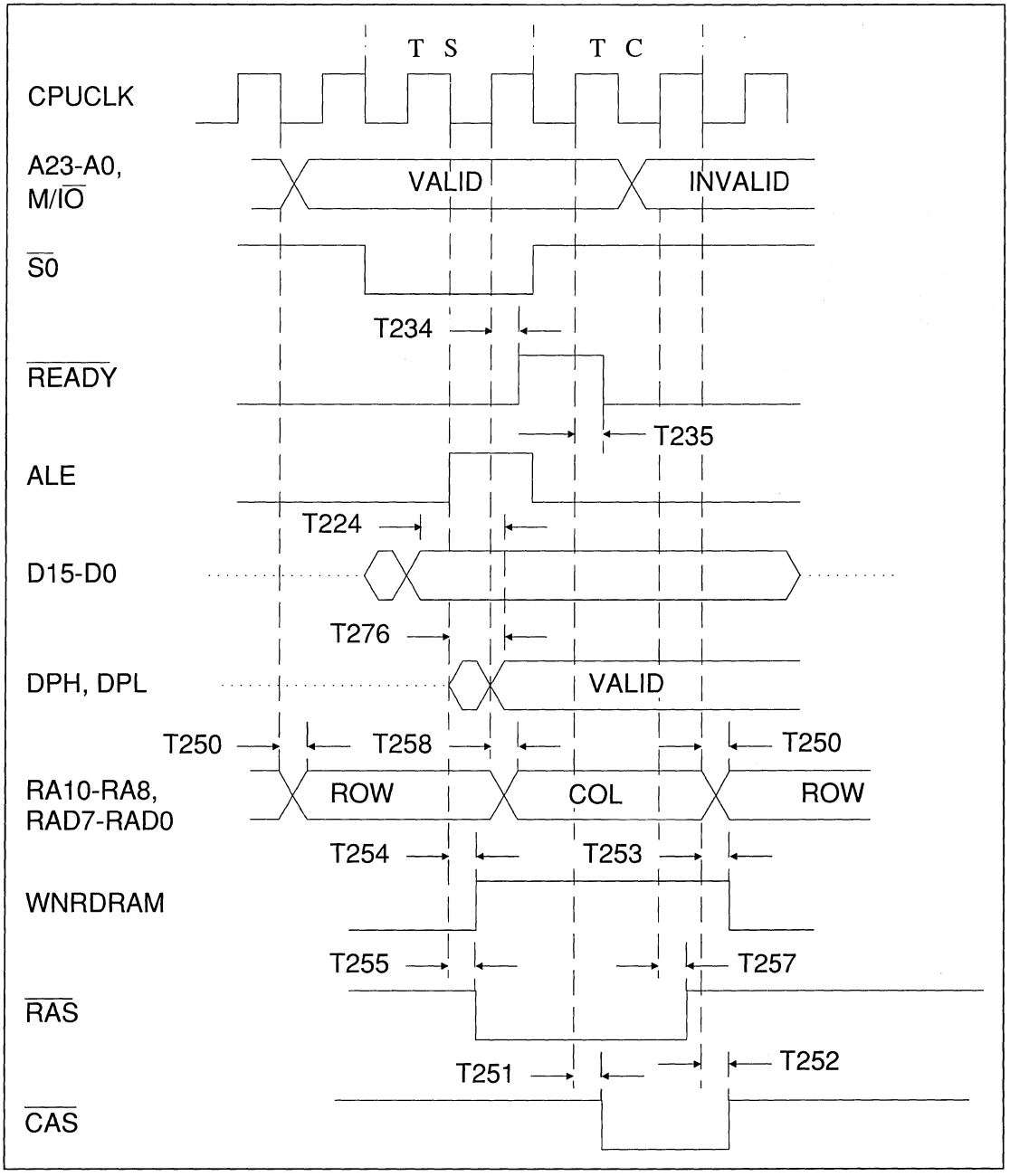

FIGURE 12-10. 80286 - NON-PAGE MODE 01, 0 WAIT STATE WRITE (4072H = 3560H)

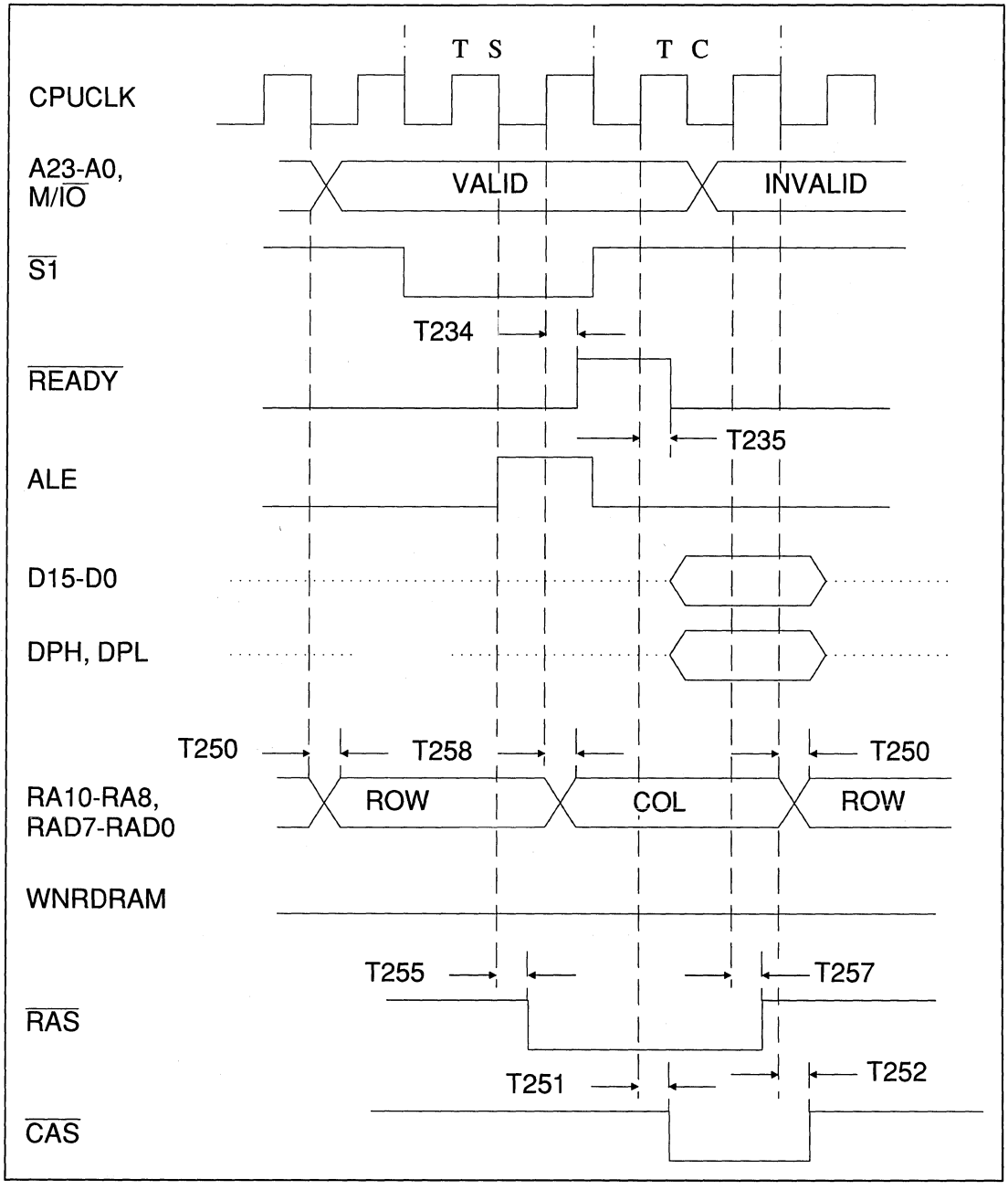

FIGURE 12-11. 80286 - NON-PAGE MODE 01, 0 WAIT STATE READ (4072H = 3560H)

12.1.4 80386SX Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T200	Processor ADDRESS to RAM address valid, Page Hit		34	27
T201	CPUCLK rise to CAS fall, 2.5 CLK CAS		31	25
T202	CPUCLK fall to CAS rise		24	21
T203	CPUCLK fall to CAS fall, 2.0 CLK CAS		27	22
T204	Processor data to parity valid		25	20
T205	CPUCLK rise to RAM address valid, Page Miss		48	43
T206	CPUCLK rise to WNRDRAM rise		31	28
T207	CPUCLK fall to RAS fall, first access		27	21
T208	CPUCLK rise to COLUMN address valid		49	33
T209	CPUCLK rise to WNRDRAM fall		31	28
T212	CPUCLK rise to RAS rise, Page Miss		27	24
T213	CPUCLK fall to RAS fall, Page Miss		27	24
T214	CPUCLK rise to READY fall		19	18
T215	CPUCLK rise to READY rise		19	18

TABLE 12-6. 80386SX - PAGE MODE MEMORY TIMING

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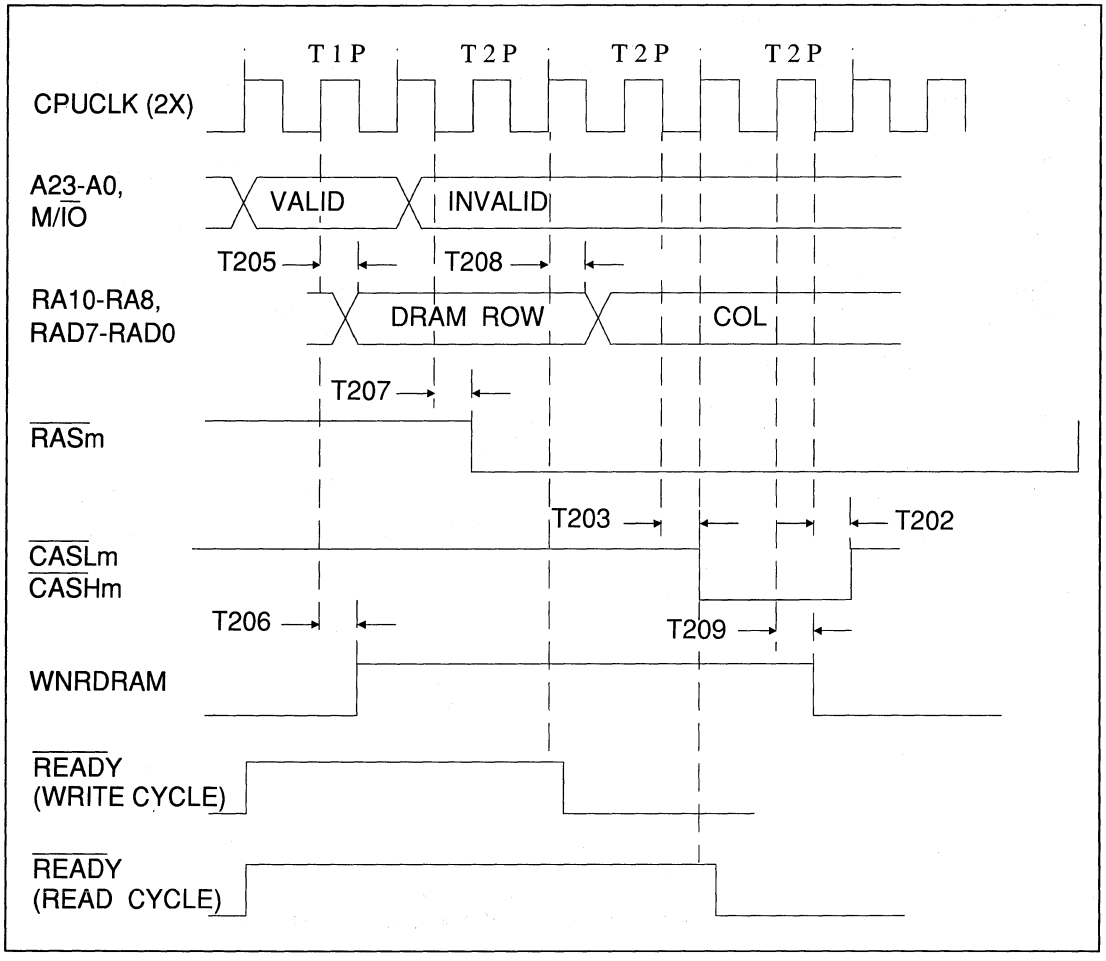


FIGURE 12-12. 80386SX - PAGE MODE, FIRST ACCESS READ/WRITE

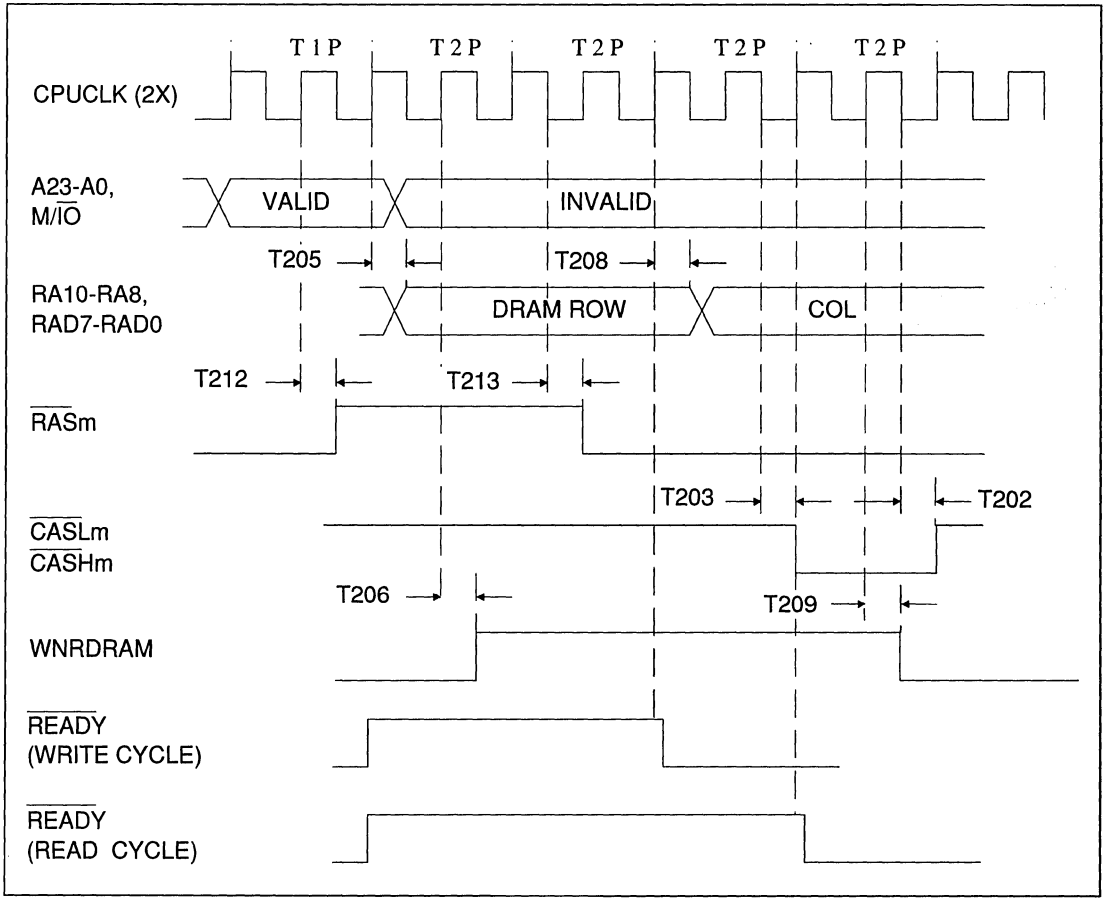


FIGURE 12-13. 80386SX - PAGE MODE, PAGE MISS READ/WRITE

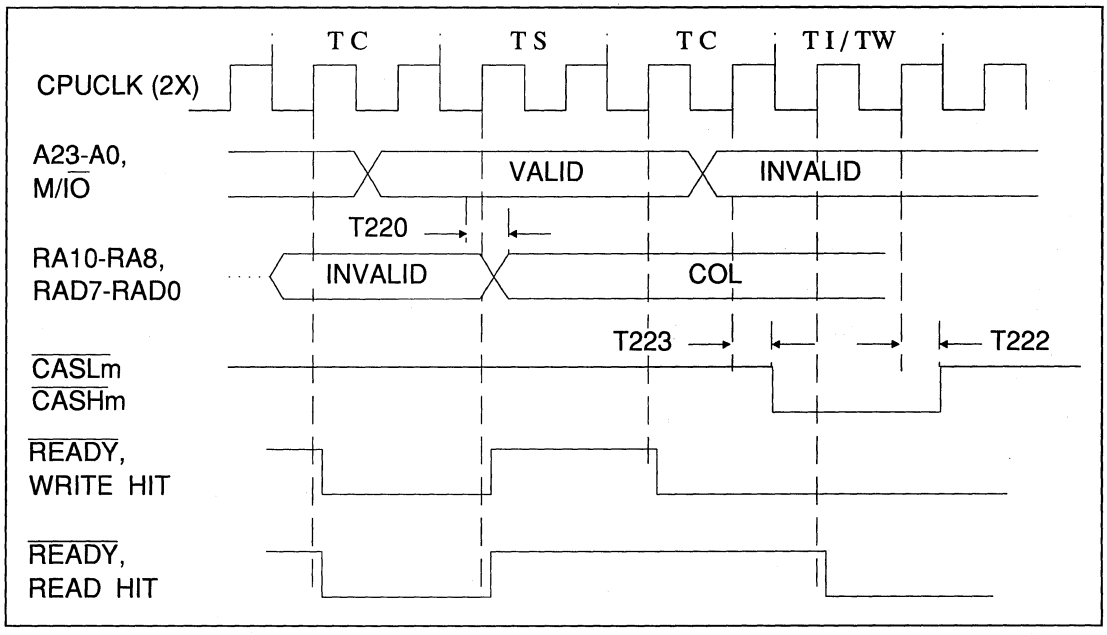


FIGURE 12-14. 80386SX - PAGE MODE, RAD CYCLE FOLLOWED BY A PAGE HIT

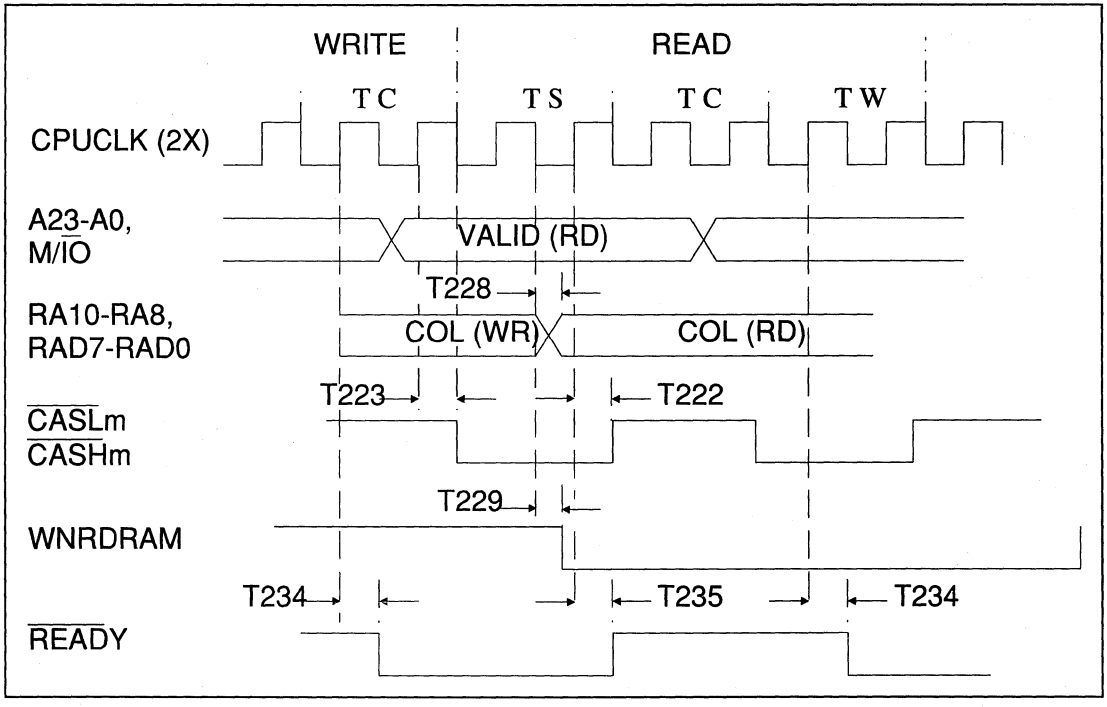


FIGURE 12-15. 80386SX - PAGE MODE, READ AFTER WRITE

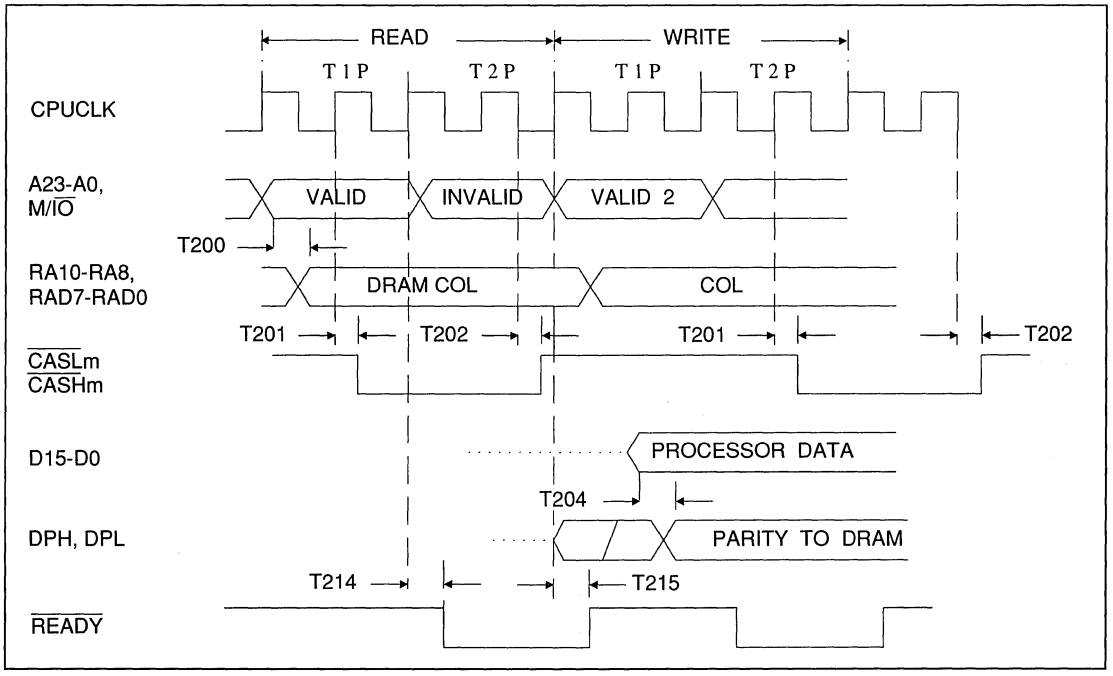


FIGURE 12-16. 80386SX - PAGE MODE, READ HIT FOLLOWED BY A WRITE HIT

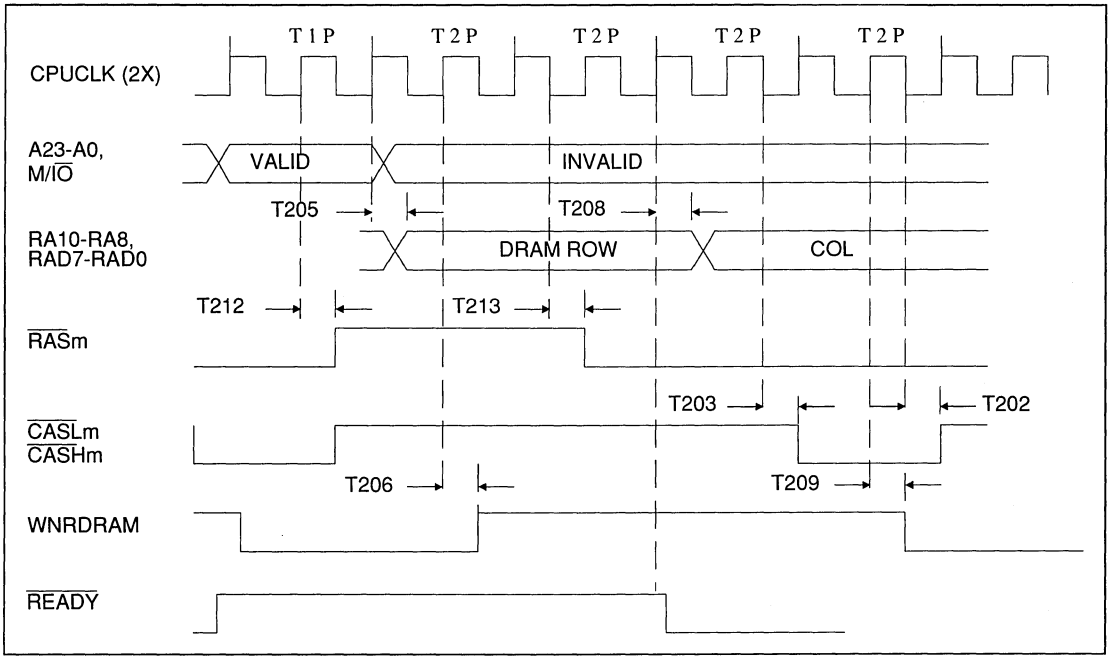


FIGURE 12-17. 80386SX - PAGE MODE, WRITE MISS CYCLE FOLLOWING A WRITE CYCLE

12.1.5 80386SX Non-Page Mode 00 and Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T204	See Table 12-6			
T214	See Table 12-6			
T215	See Table 12-6			
T240	CPUCLK rise to ROW address valid		42	42
T241	CPUCLK fall to CAS fall		27	27
T242	CPUCLK rise to CAS rise		28	24
T243	CPUCLK rise to WNRDRAM fall		28	28
T244	CPUCLK rise to WNRDRAM rise		28	28
T245	CPUCLK rise to RAS fall		25	23
T246	CPUCLK rise to RAS rise		25	23
T247	CPUCLK fall to RAS rise		29	29
T248	CPUCLK fall to COLUMN address valid		44	44
T249	CPUCLK rise to CAS fall		29	29
T260	CPUCLK rise to COLUMN address		43	41

TABLE 12-7. 80386SX - NON-PAGE MODE 00 & 01 MEMORY TIMING

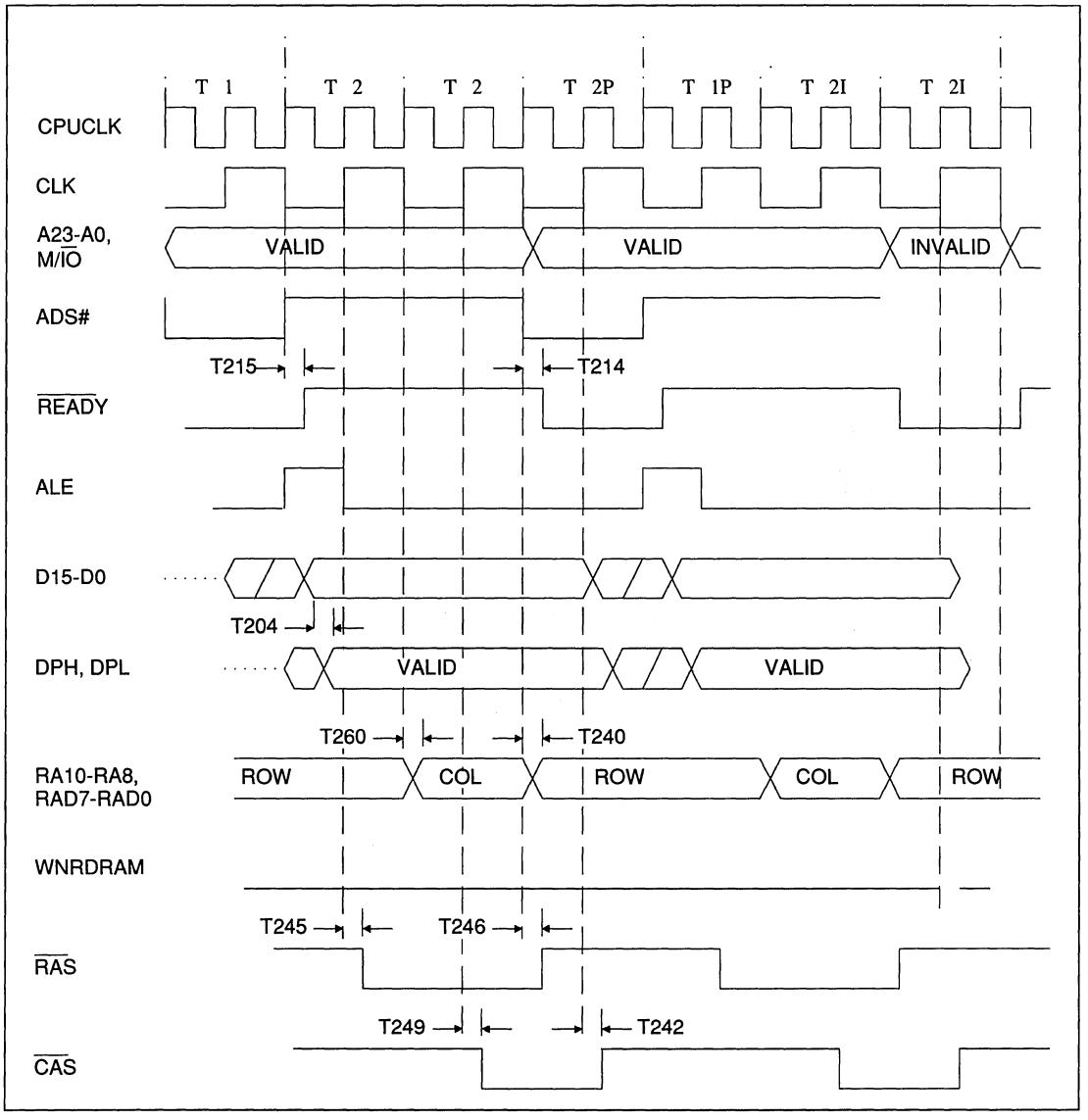


FIGURE 12-18. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE READ (PIPELINE) (4072H = 0001)

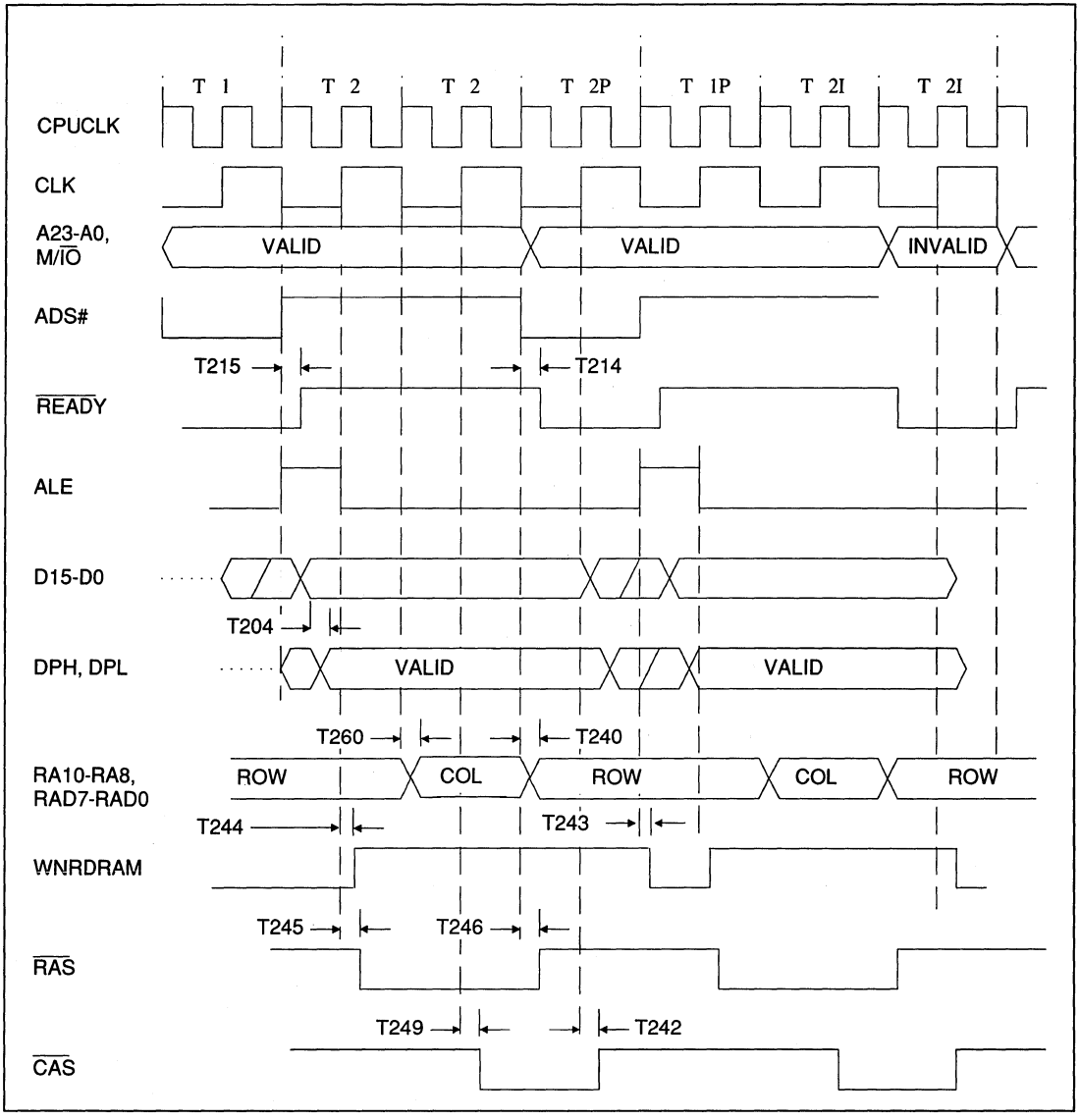


FIGURE 12-19. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE WRITE (PIPELINE) (4072H = 0001)

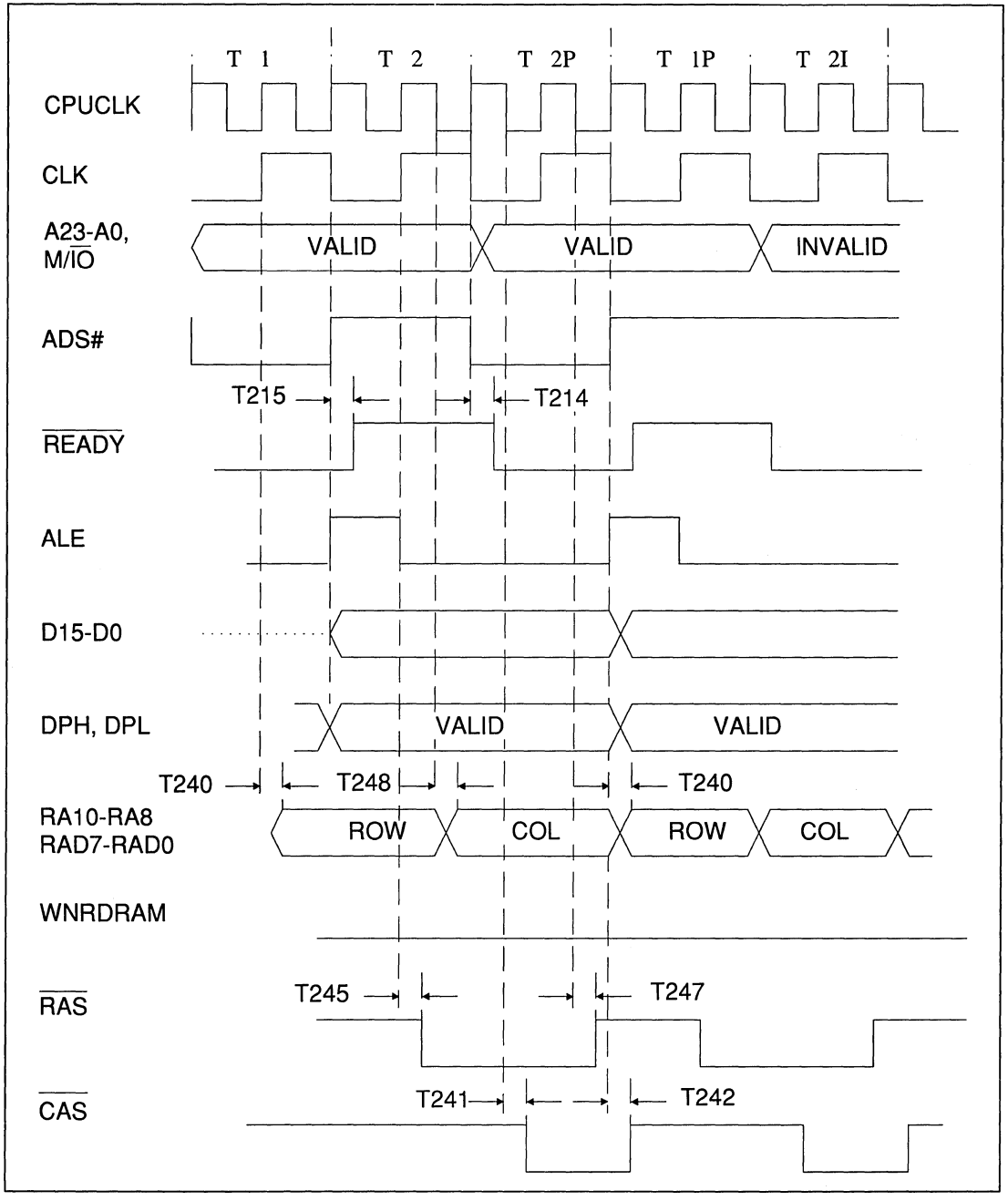


FIGURE 12-20. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

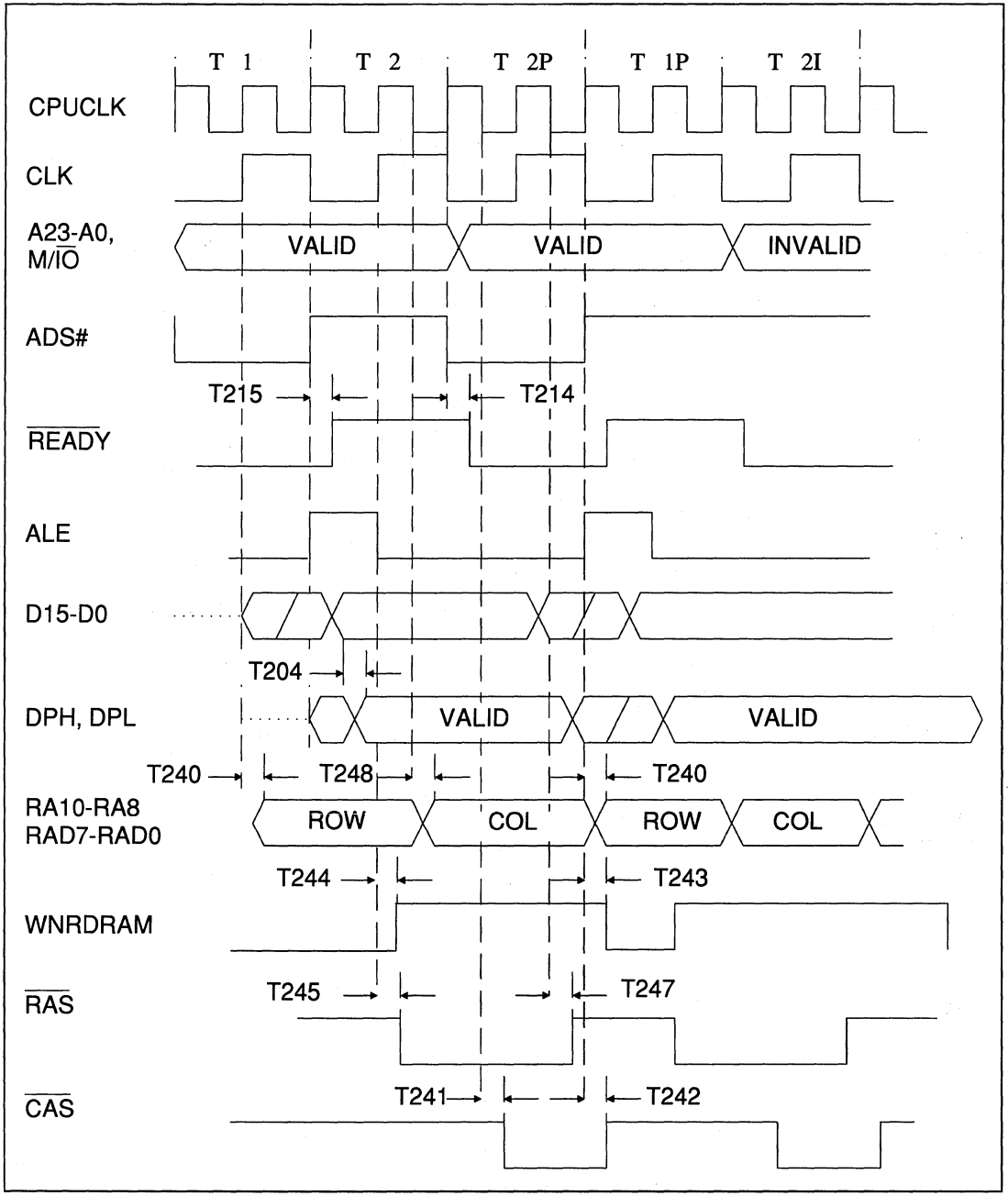


FIGURE 12-21. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

12.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus refresh cycle

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

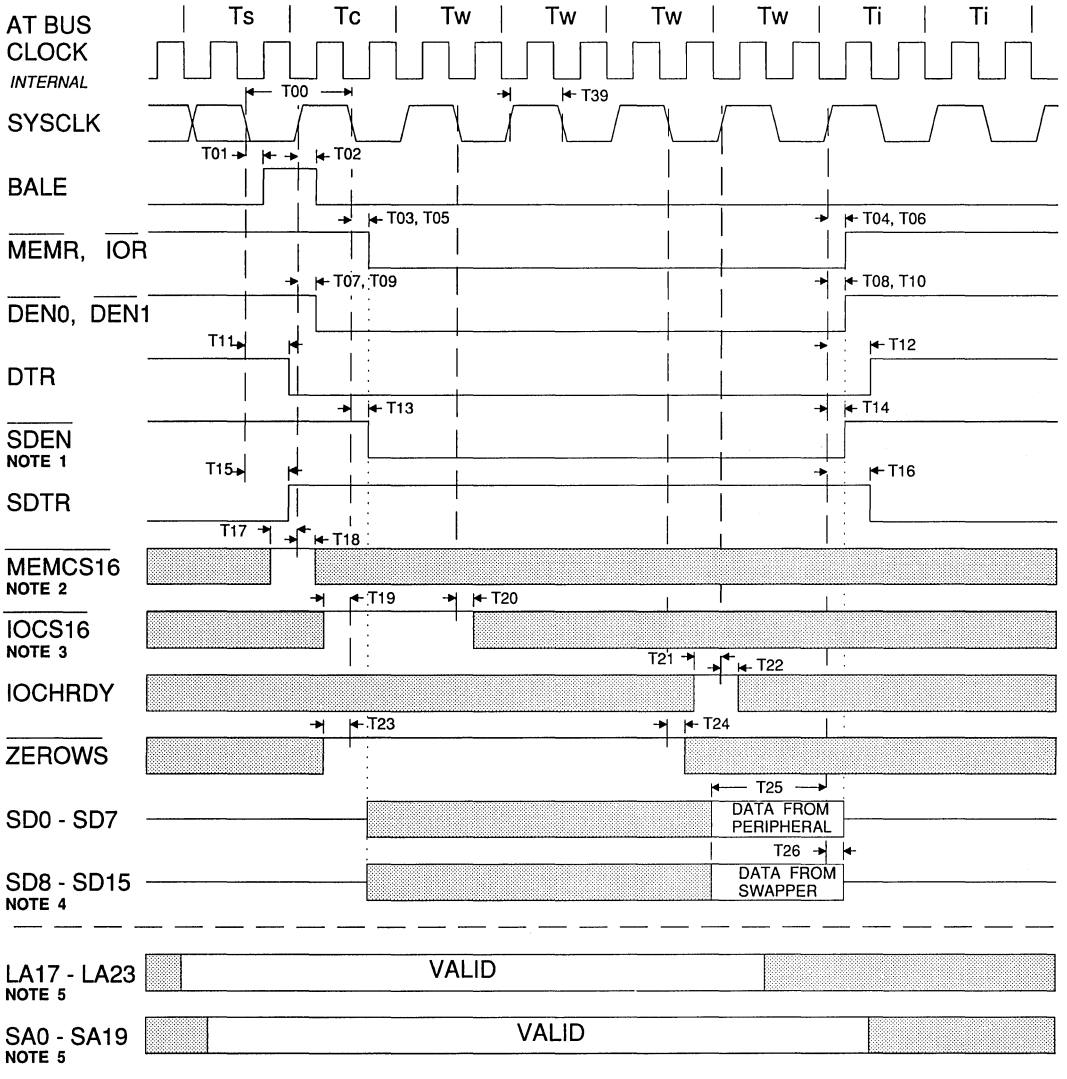
12.2.1 CPU Initiated AT Bus Cycles

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T00	SYSCLK Cycle Time	100		ns	
T01	SYSCLK fall to BALE rise		12	ns	
T02	SYSCLK rise to BALE fall		9	ns	
T03	SYSCLK fall to $\overline{\text{MEMR}}$ fall		9	ns	8-bit cycle
T04	SYSCLK rise to $\overline{\text{MEMR}}$ rise		6	ns	
T05	SYSCLK fall to $\overline{\text{IOR}}$ fall		10	ns	
T06	SYSCLK rise to $\overline{\text{IOR}}$ rise		7	ns	
T07	SYSCLK rise to $\overline{\text{DEN0}}$ fall		7	ns	Read Cycle
T08	SYSCLK rise to $\overline{\text{DEN0}}$ rise		11	ns	Read Cycle
T09	SYSCLK rise to $\overline{\text{DEN1}}$ fall		7	ns	Read Cycle
T10	SYSCLK rise to $\overline{\text{DEN1}}$ rise		9	ns	Read Cycle
T11	SYSCLK fall to DTR fall		19	ns	Delay is number given plus (T00 × 0.25)
T12	SYSCLK rise to DTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T13	SYSCLK fall to $\overline{\text{SDEN}}$ fall		10	ns	
T14	SYSCLK rise to $\overline{\text{SDEN}}$ rise		8	ns	
T15	SYSCLK fall to SDTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T16	SYSCLK rise to SDTR fall		11	ns	Delay is number given plus (T00 × 0.25)
T17	$\overline{\text{MEMCS16}}$ setup time to SYSCLK rise	25		ns	
T18	$\overline{\text{MEMCS16}}$ hold time from SYSCLK rise	0		ns	
T19	$\overline{\text{IOCS16}}$ setup time to SYSCLK fall	23		ns	
T20	$\overline{\text{IOCS16}}$ hold time from SYSCLK fall	0		ns	8-bit cycle

TABLE 12-8. CPU INITIATED AT BUS CYCLES

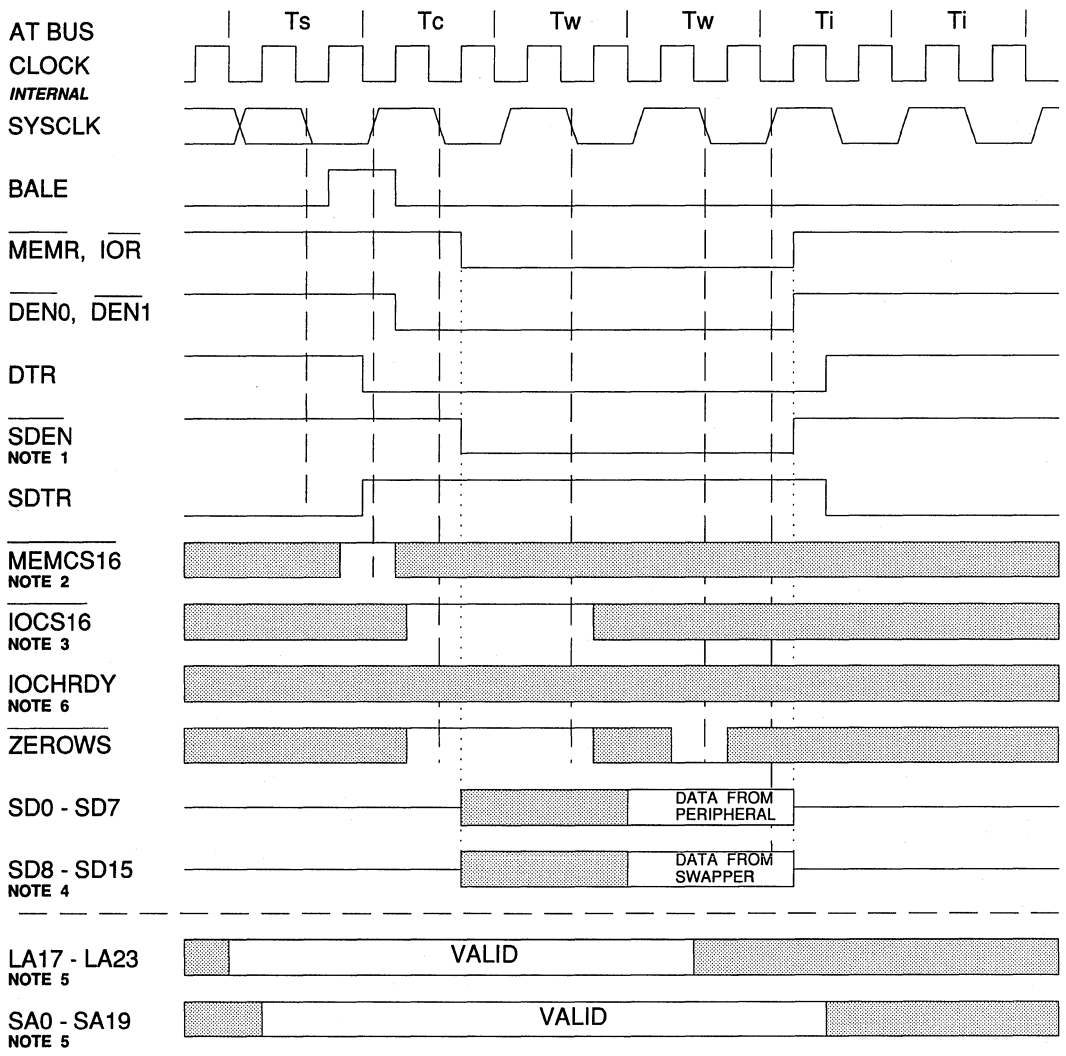
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T21	IOCHRDY setup time to SYSCLK rise	22		ns	
T22	IOCHRDY hold time from SYSCLK rise	0		ns	
T23	$\overline{\text{ZEROWS}}$ setup time to SYSCLK fall	24		ns	
T24	$\overline{\text{ZEROWS}}$ hold time from SYSCLK fall	0		ns	
T25	AT Bus data setup time to SYSCLK rise	22		ns	Total setup time is number given plus delay through AT Bus data buffers.
T26	AT Bus data hold time from SYSCLK rise	0		ns	
T27	SYSCLK fall to $\overline{\text{MEMW}}$ fall		9	ns	
T28	SYSCLK rise to $\overline{\text{MEMW}}$ rise		5	ns	
T29	SYSCLK fall to $\overline{\text{IOW}}$ fall		10	ns	
T30	SYSCLK rise to $\overline{\text{IOW}}$ rise		8	ns	
T31	SYSCLK fall to $\overline{\text{DEN0}}$ fall		10	ns	Write cycle
T32	SYSCLK fall to $\overline{\text{DEN0}}$ rise		9	ns	Write cycle
T33	SYSCLK fall to $\overline{\text{DEN1}}$ fall		10	ns	Write cycle
T34	SYSCLK fall to $\overline{\text{DEN1}}$ rise		9	ns	Write cycle
T35	SYSCLK fall to $\overline{\text{SDEN}}$ rise		11	ns	
T36	SYSCLK fall to SA0 rise		16	ns	Word to byte conversion cycle
T37	SYSCLK rise to $\overline{\text{MEMR}}$ fall		6	ns	16-bit cycle
T38	$\overline{\text{IOCS16}}$ hold time from SYSCLK rise	0		ns	16-bit cycle
T39	SYSCLK high time	-4	0	ns	(T00 ÷ 2) plus number given

TABLE 12-8. CPU INITIATED BUS CYCLES cont.



NOTE 1: SDEN is asserted only when SA0 is high.
NOTE 2: MEMCS16 is sampled only during memory cycles.
NOTE 3: IOCS16 is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-22. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING



NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.

NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

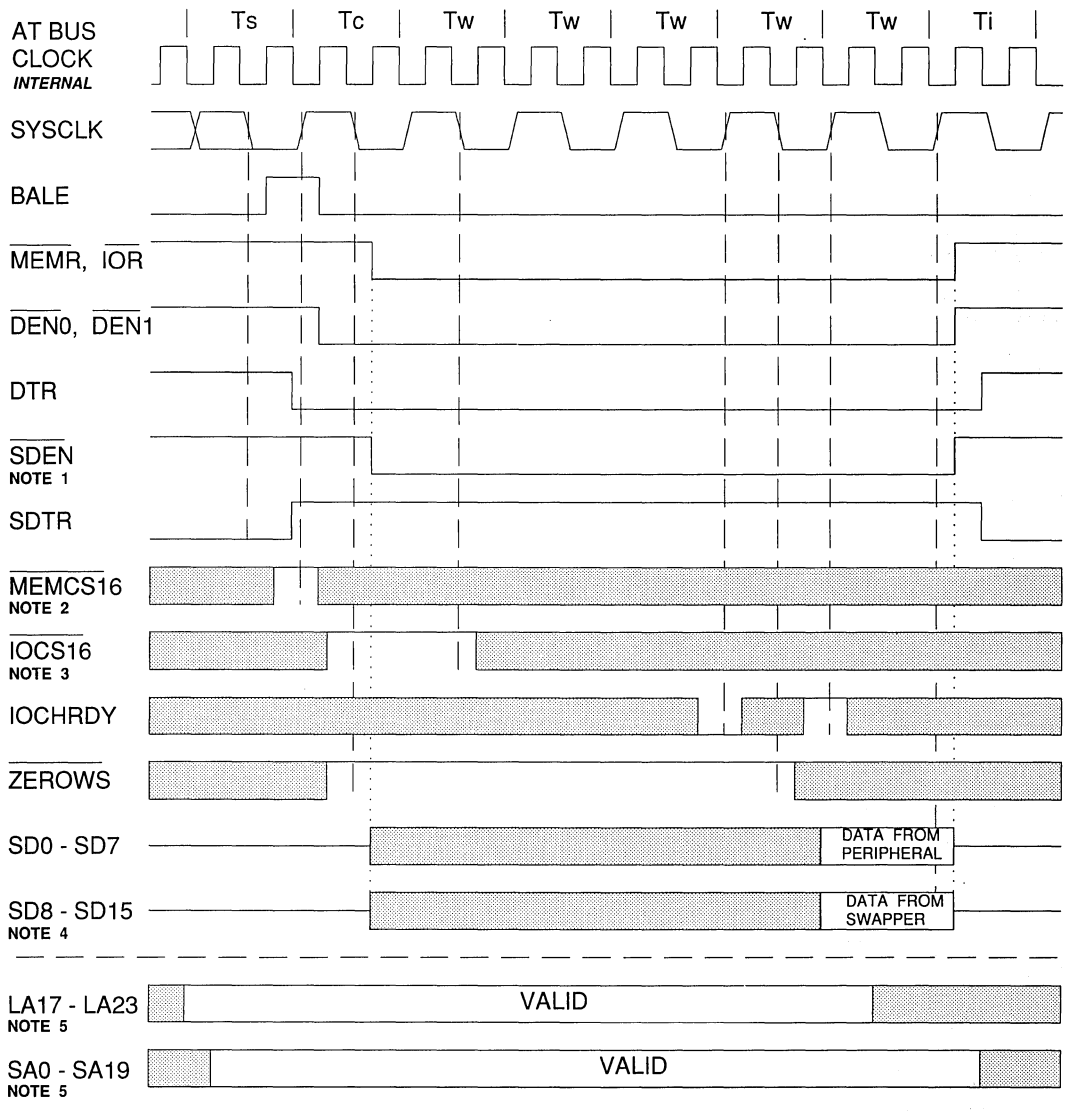
NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

NOTE 6: IOCHRDY overrides $\overline{\text{ZEROWS}}$ only during the first cycle of a word to byte conversion.

FIGURE 12-23. AT BUS I/O OR MEMORY READ: 8-BIT, $\overline{\text{ZEROWS}}$ ASSERTED



NOTE 1: SDEN is asserted only when SA0 is high.

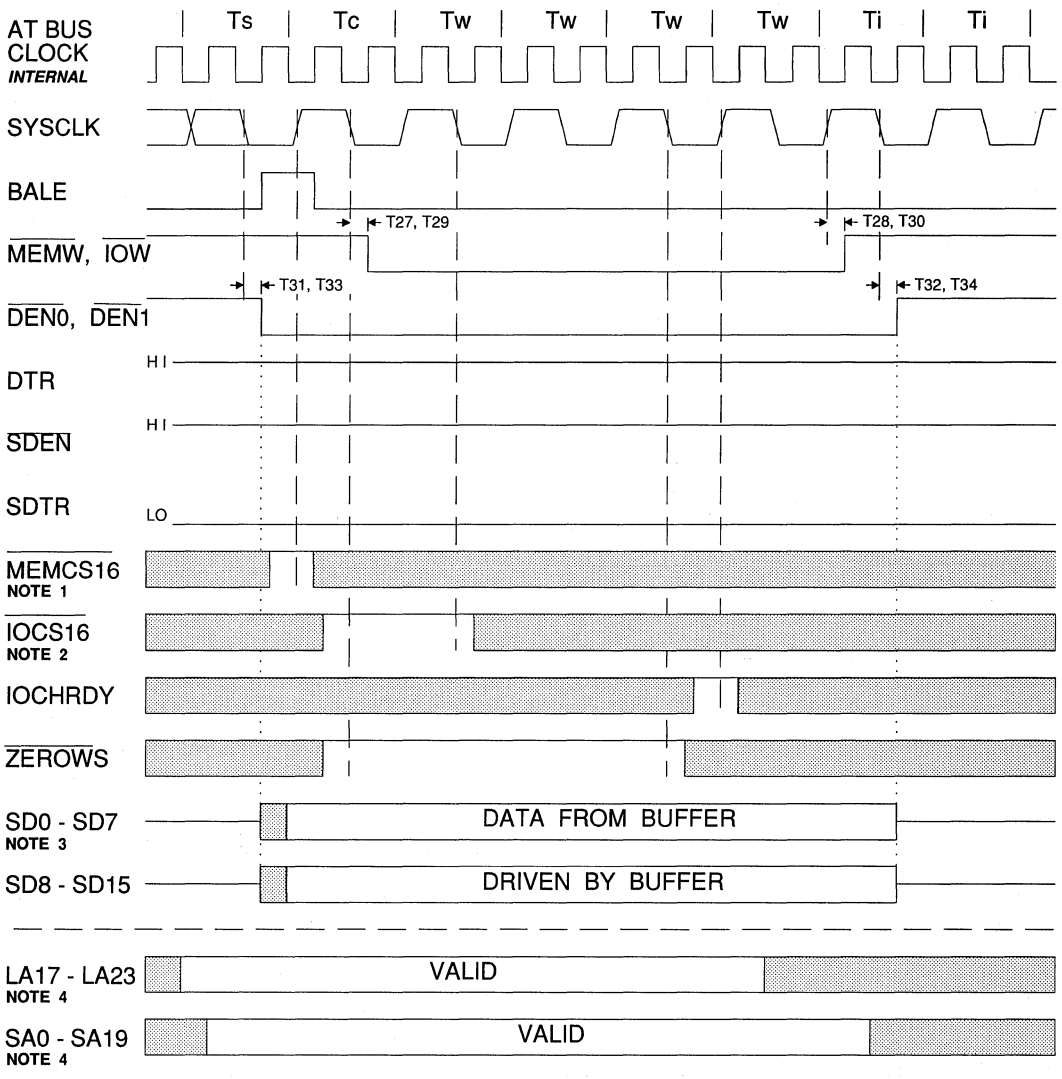
NOTE 2: MEMCS16 is sampled only during memory cycles.

NOTE 3: IOCS16 is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-24. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED



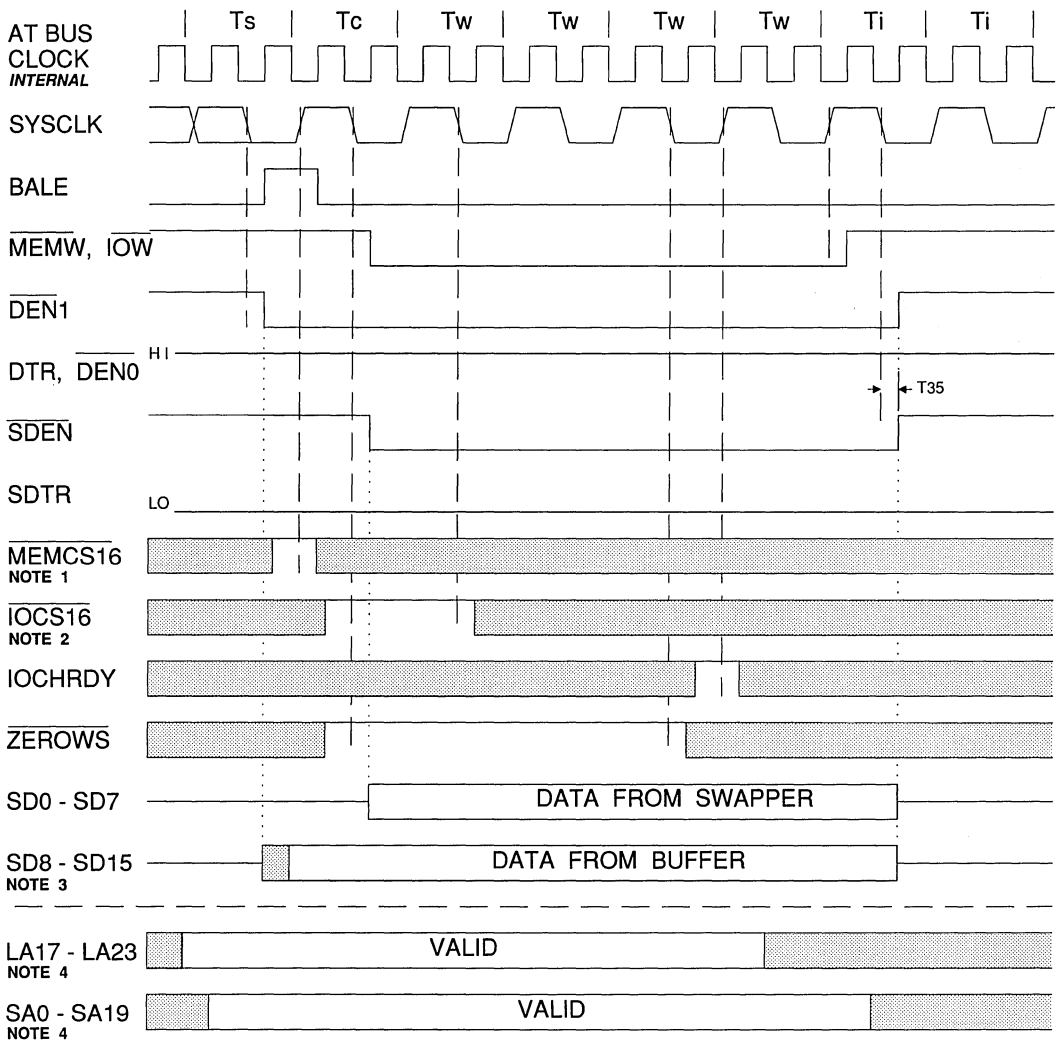
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when $\overline{\text{DEN0}}$ is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-25. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING



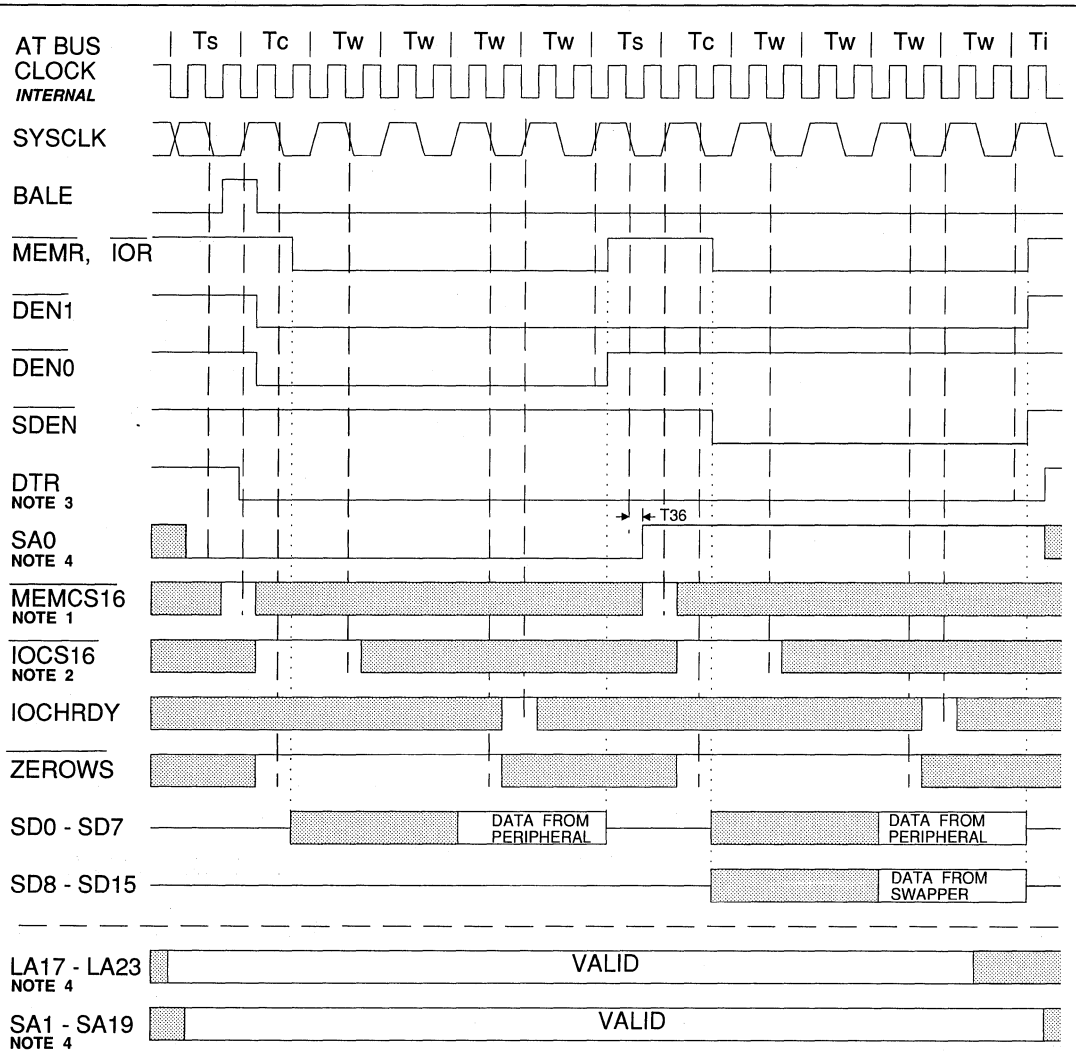
NOTE 1: MEMCS16 is sampled only during memory cycles.

NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD8 - 15 when DEN1 is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-26. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING



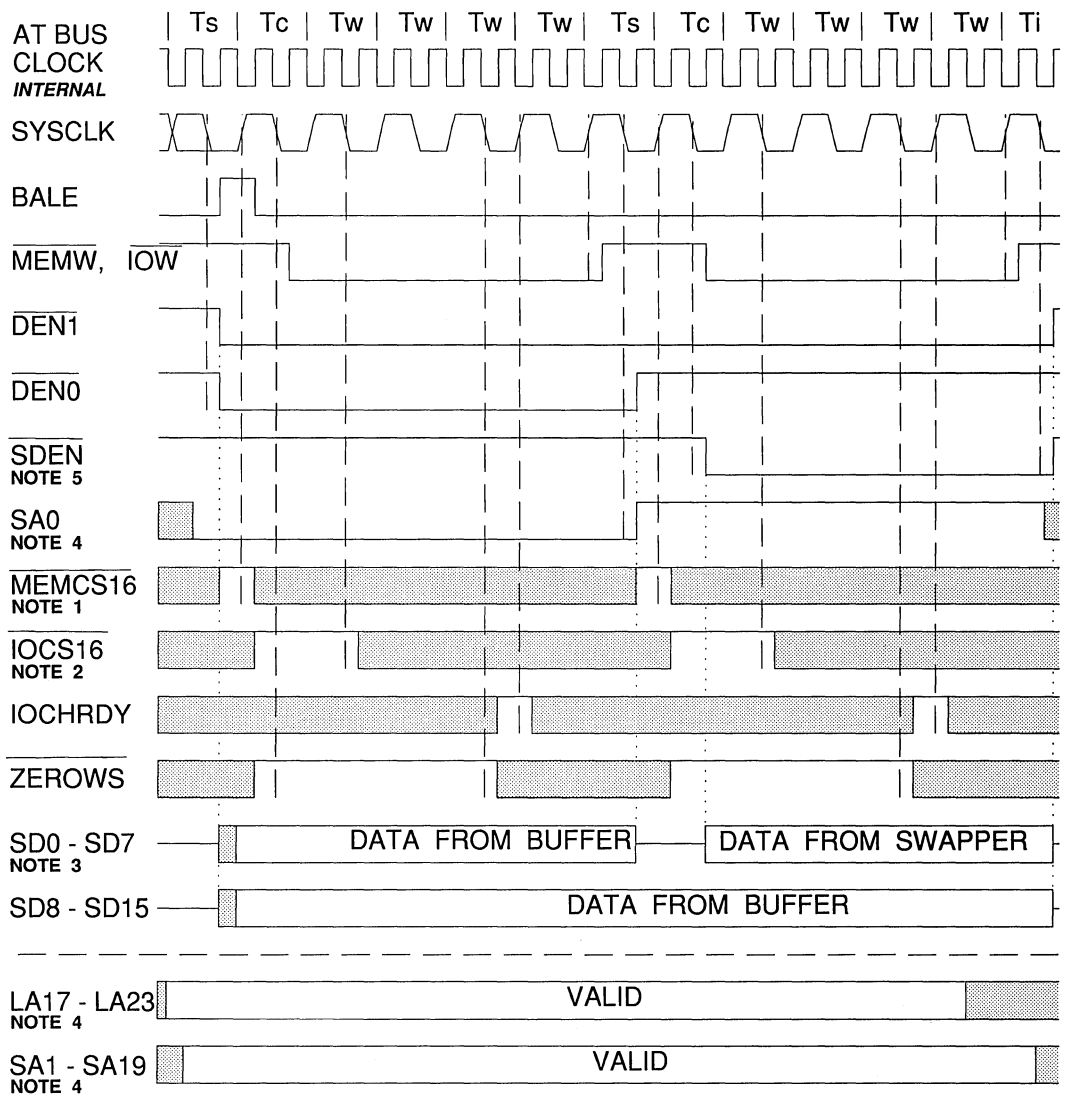
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: SDTR is the inversion of DTR during CPU transfer cycles.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-27. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: MEMCS16 is sampled only during memory cycles.

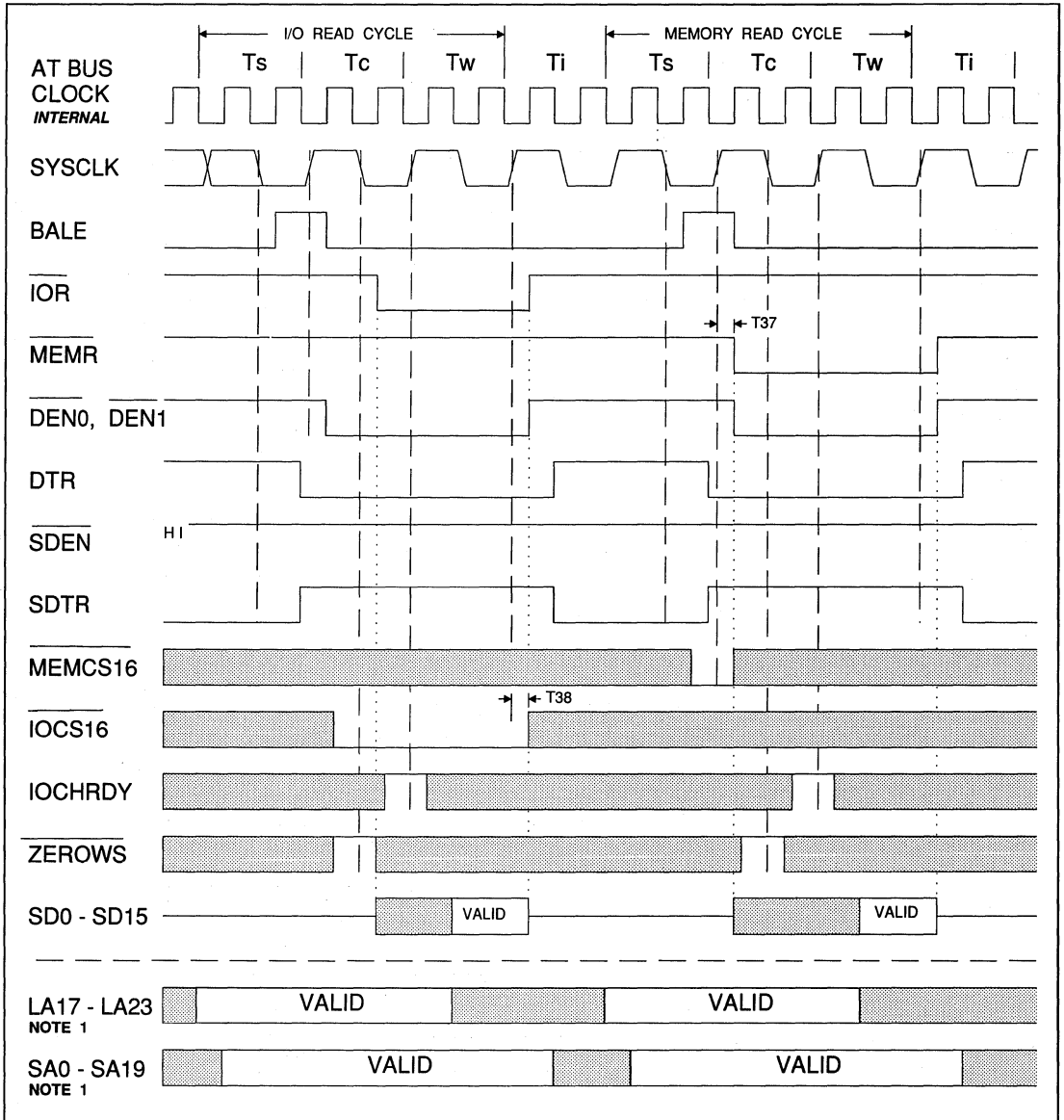
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when DEN0 is asserted is dependent on register settings and may be synchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

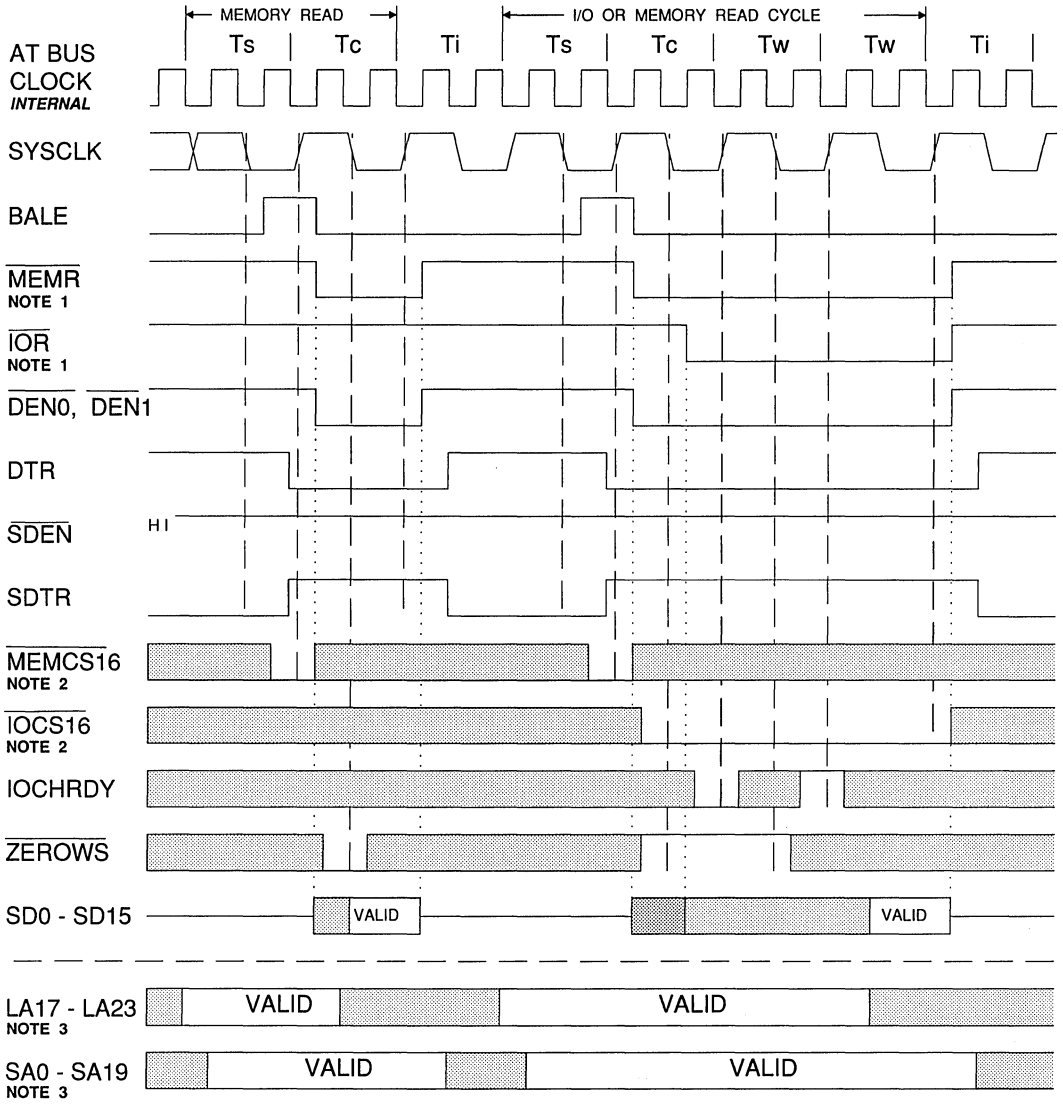
NOTE 5: SDTR remains low and DTR remains high for this cycle.

FIGURE 12-28. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-29. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING

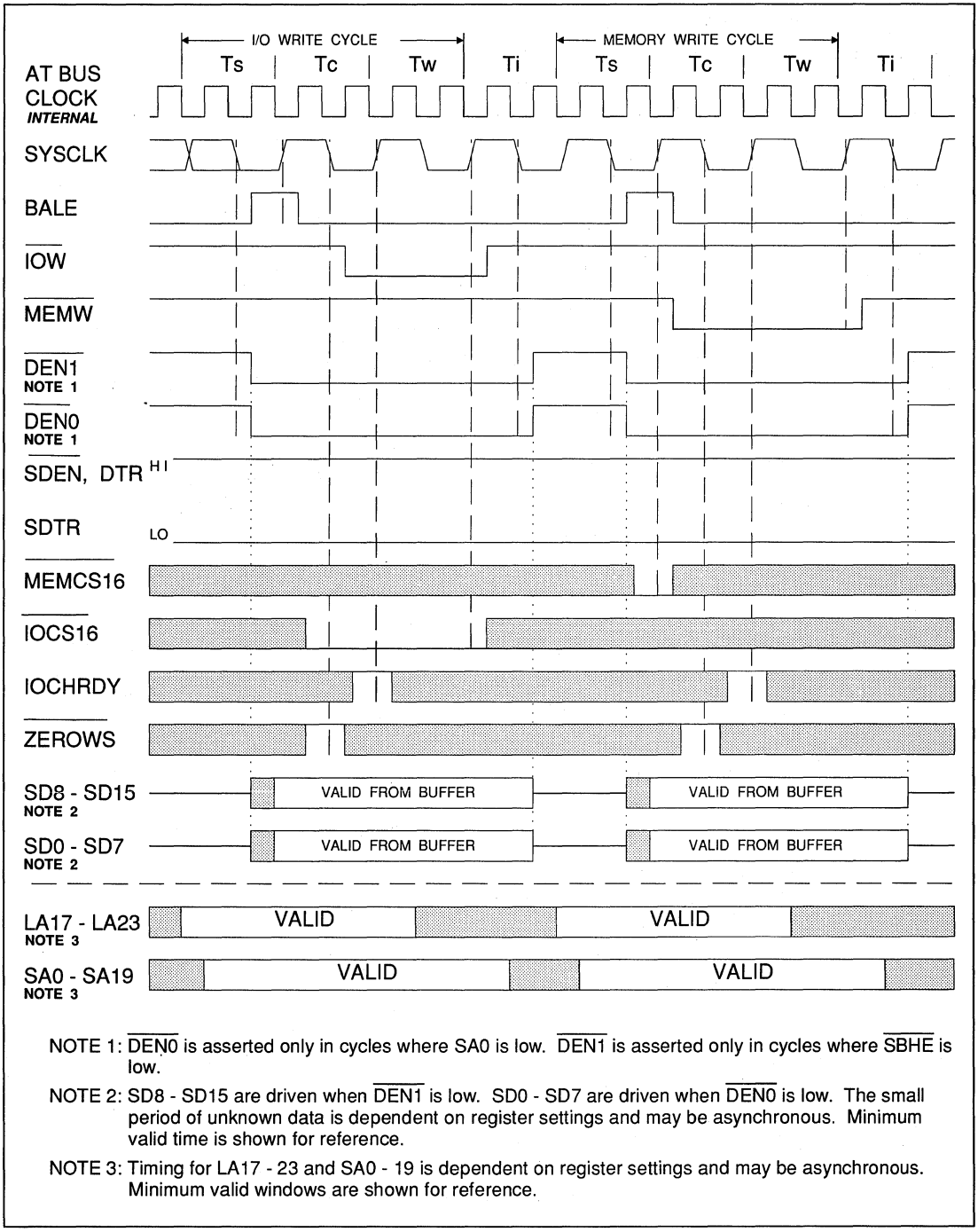


NOTE 1: MEMR and IOR will not be asserted simultaneously. The first cycle must be to memory, as zero wait state I/O cycles are not supported.

NOTE 2: MEMCS16 is sampled only during memory cycles. IOCS16 is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-30. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED



NOTE 1: $\overline{DEN0}$ is asserted only in cycles where SA0 is low. $\overline{DEN1}$ is asserted only in cycles where $\overline{SBHE}$ is low.

NOTE 2: SD8 - SD15 are driven when $\overline{DEN1}$ is low. SD0 - SD7 are driven when $\overline{DEN0}$ is low. The small period of unknown data is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 12-31. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING

12.2.2 Entering the AT Bus

The timing in this section is presented in the following sequence:

80286 CPU

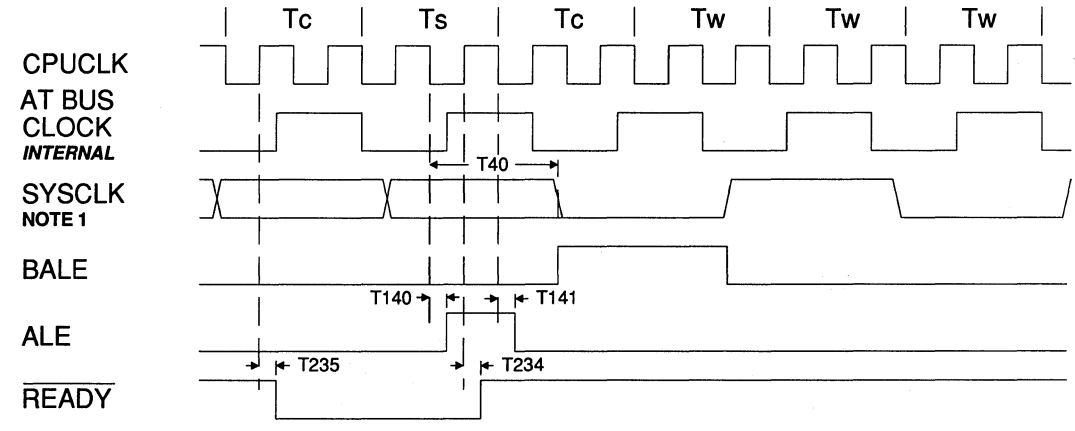
Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

80386SX CPU

Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T40	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	4		ns	Register 1872H: BRQ_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T41	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	9		ns	Register 1872H: BRQ_DEL = 00 BUS_MOD = 0X Delay is number given plus (T00 × 0.5)
T42	CPUCLK fall to SYSCLK fall 80386SX CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T43	CPUCLK rise to SYSCLK fall 80386SX CPU mode.		35	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T44	CPUCLK rise to SYSCLK fall 80286 CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T45	CPUCLK fall to SYSCLK fall 80286 CPU mode.		36	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T140	CPUCLK fall to ALE rise 80286 CPU mode. CPUCLK rise to ALE rise 80386SX CPU mode.		20	ns	
T141	CPUCLK fall to ALE fall 80286 CPU mode. CPUCLK rise to ALE fall 80386SX CPU mode.		20	ns	
T214	See TABLE 13-6				
T215	See TABLE 13-6				
T234	See TABLE 13-3				
T235	See TABLE 13-3				

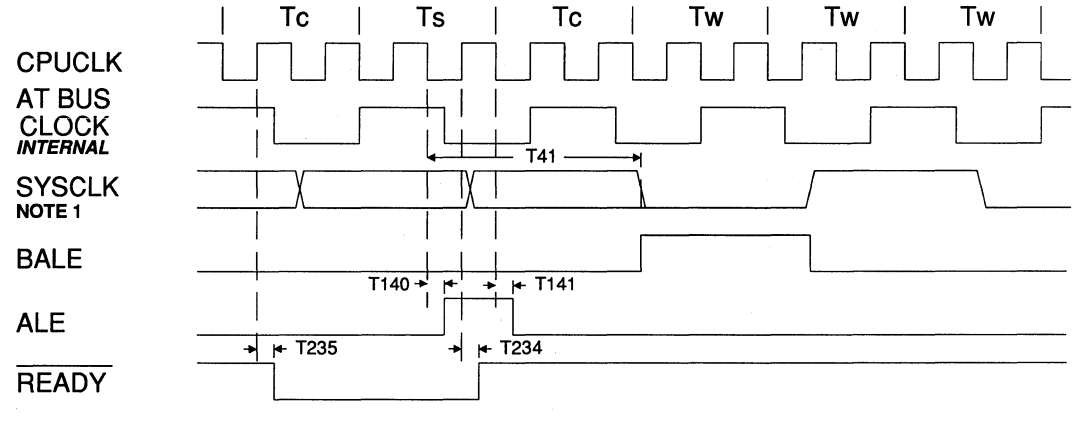
TABLE 12-9. ENTERING THE AT BUS



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

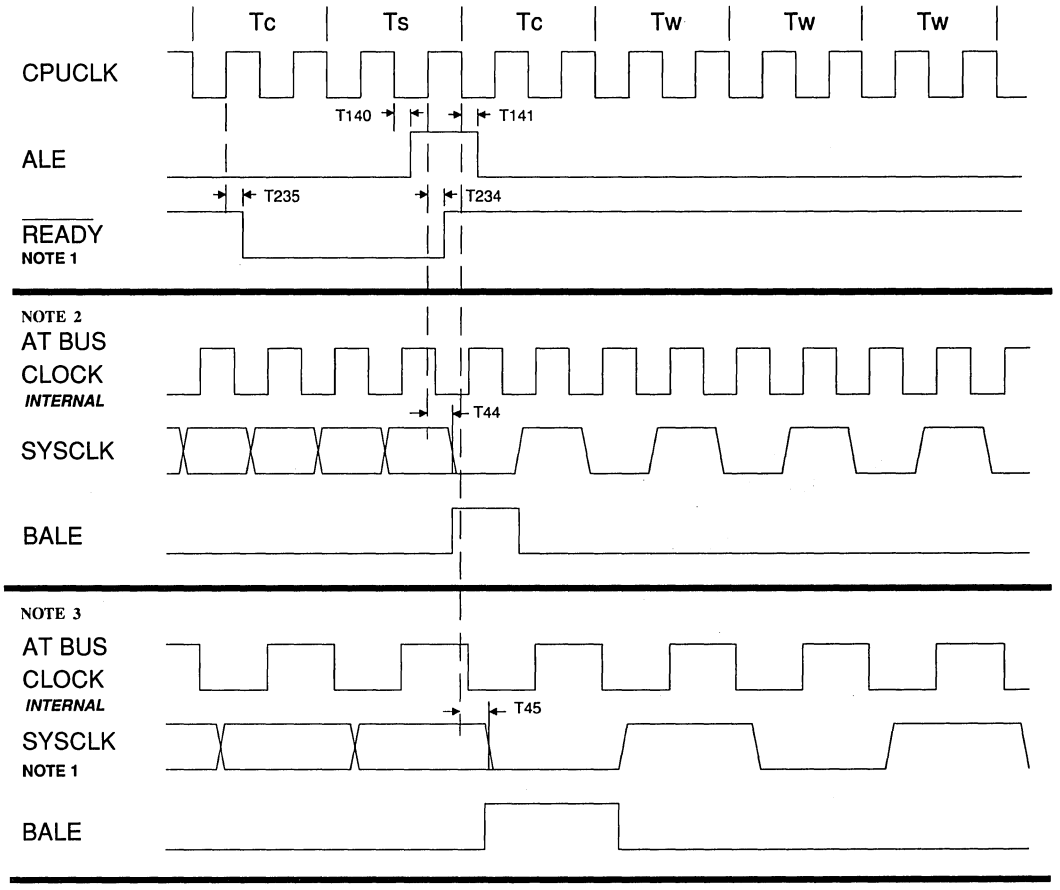
FIGURE 12-32. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1/2 CLOCK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

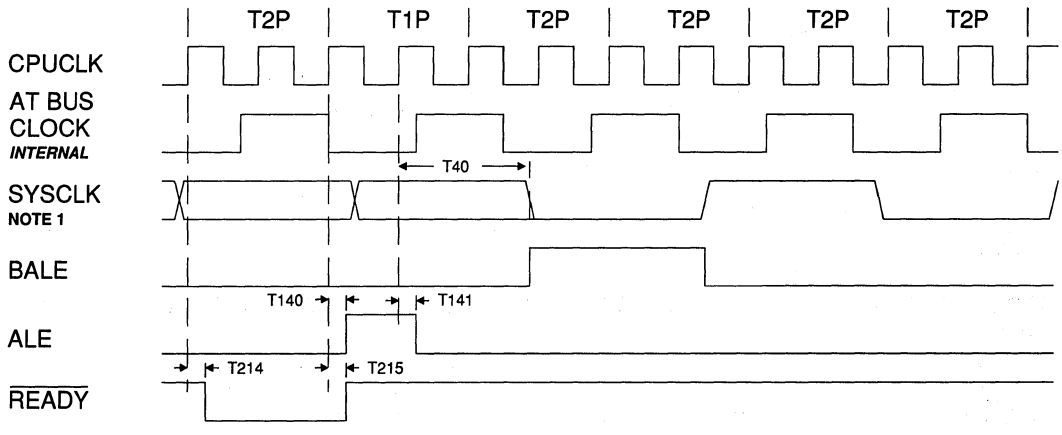
NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 12-33. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1 CLOCK



NOTE 1: READY timing is shown for when the previous cycle was not an AT bus cycle.
NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.
NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

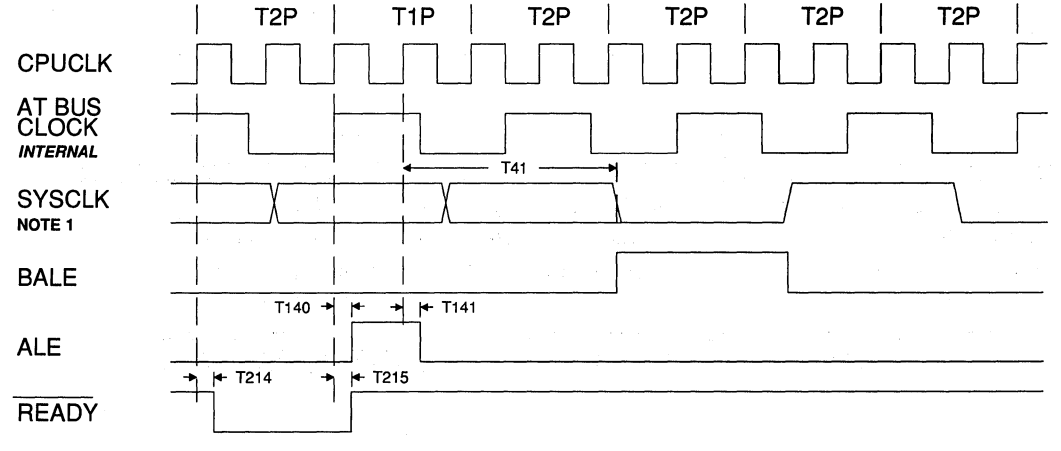
FIGURE 12-34. 80286 CPU - SYCNHRONOUS CPUCLK TO SYSCLK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

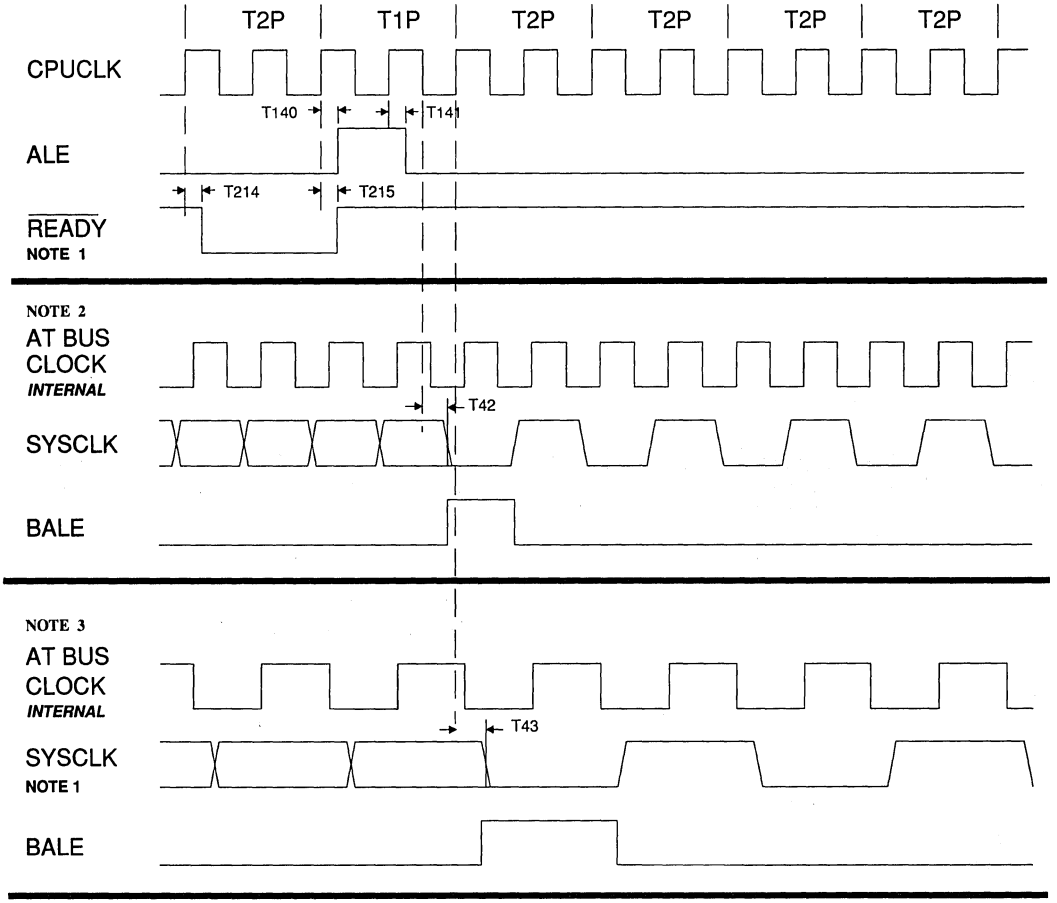
FIGURE 12-35. 80386SX CPU - BREQ DELAY = 1/2 CLOCK



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 12-36. 80386SX - BREQ DELAY = 1 CLOCK



NOTE 1: If this AT bus cycle is immediatly preceded by another bus cycle and the BUS_MOD field in register 1872 = 11, READY will fall 1 CPUCLK later than shown.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

FIGURE 12-37. 80386SX CPU - SYCNHRONOUS CPUCLK TO SYSCLK

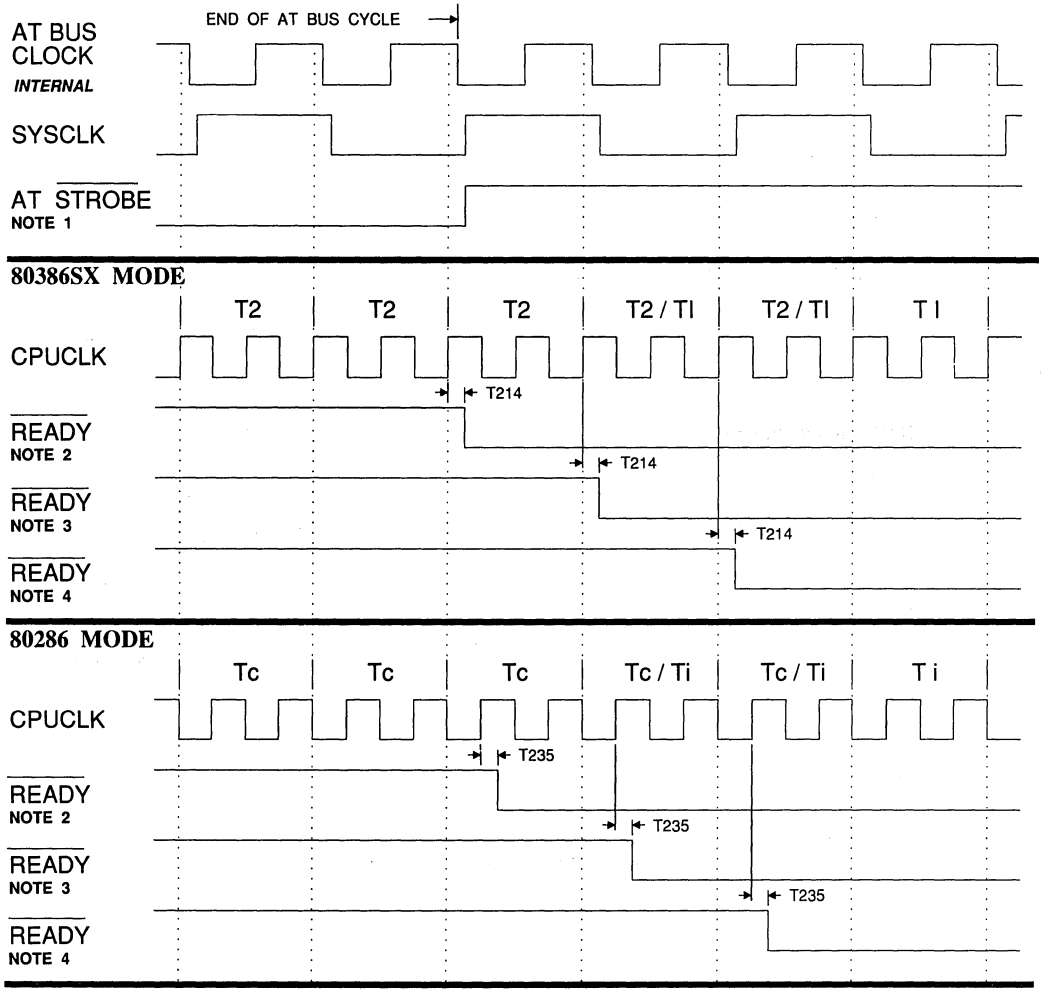
7

12.2.3 Exiting The AT Bus

Exiting a synchronous AT bus is covered first, followed by the asynchronous bus.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T46	SYSCLK fall to CPUCLK	-5		ns	Register 1872H: BAK_DEL = 10 BUS_MOD = 0X
T47	SYSCLK fall to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T48	SYSCLK rise to CPUCLK	-10		ns	Register 1872H: BAK_DEL = 00 BUS_MOD = 0X
T49	SYSCLK rise to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 11 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T144	CPUCLK fall to $\overline{\text{READY}}$ fall, 80286 CPU mode.		24	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T145	CPUCLK fall to $\overline{\text{READY}}$ rise, 80286 CPU mode.		26	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T214	See TABLE 12-6				
T215	See TABLE 12-6				
T234	See TABLE 12-3				
T235	See TABLE 12-3				

TABLE 12-10. EXITING THE AT BUS



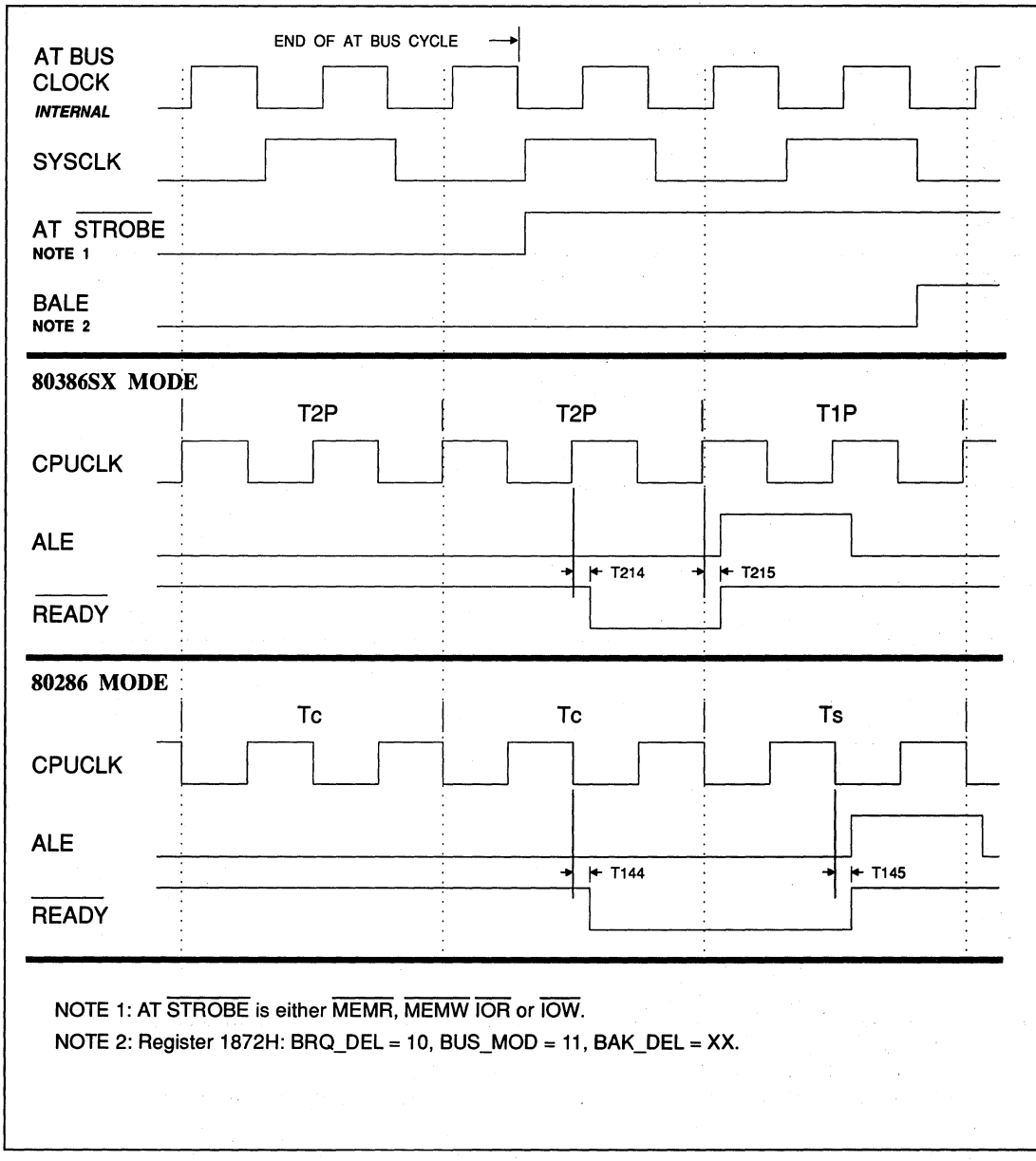
NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BUS_MOD = 10, BAK_DEL = 10 (-1 AT bus clock).

NOTE 3: Register 1872H: BUS_MOD = 10, BAK_DEL = 01 or 00 (-0.5 AT bus clock or no delay).

NOTE 4: Register 1872H: BUS_MOD = 10, BAK_DEL = 11 (+0.5 AT bus clock).

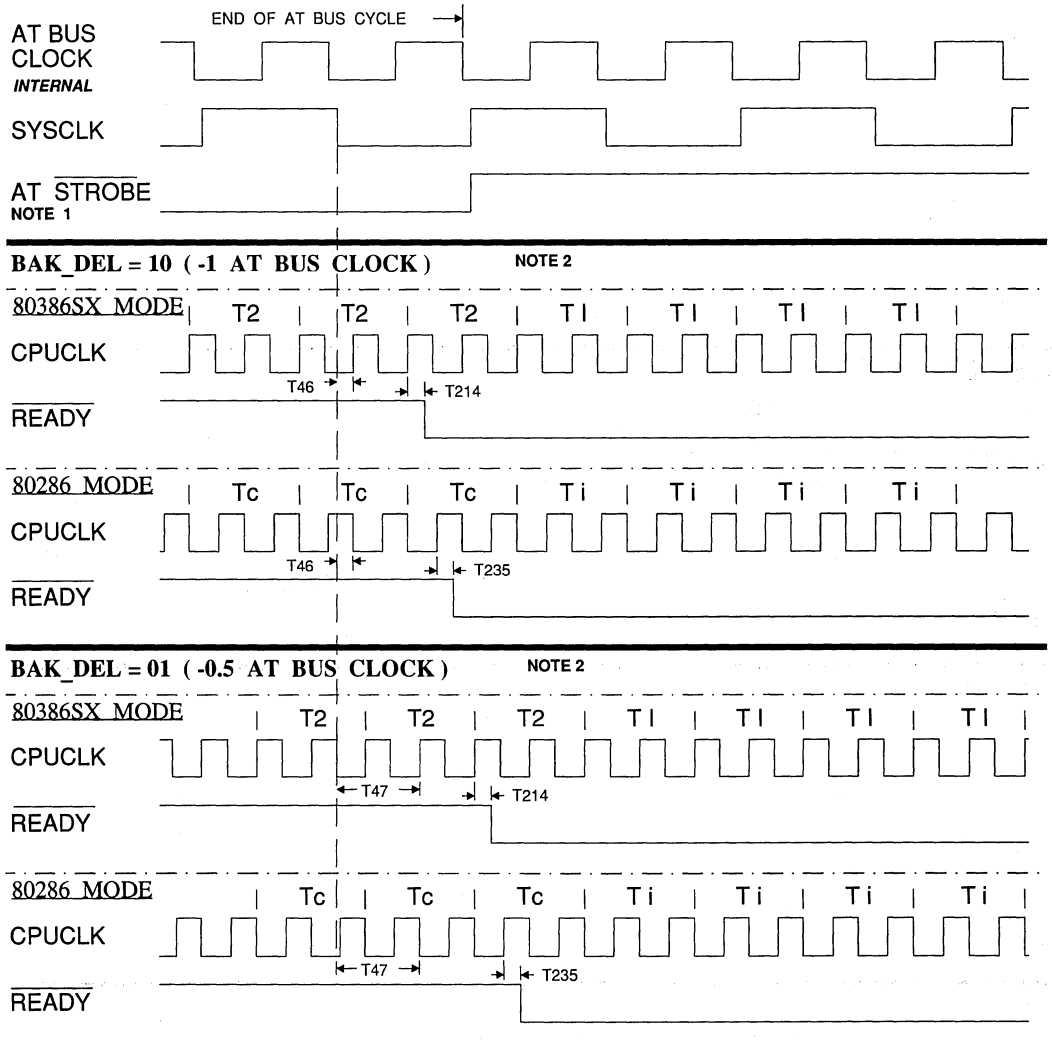
FIGURE 12-38. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 2



NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BRQ_DEL = 10, BUS_MOD = 11, BAK_DEL = XX.

FIGURE 12-39. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 1

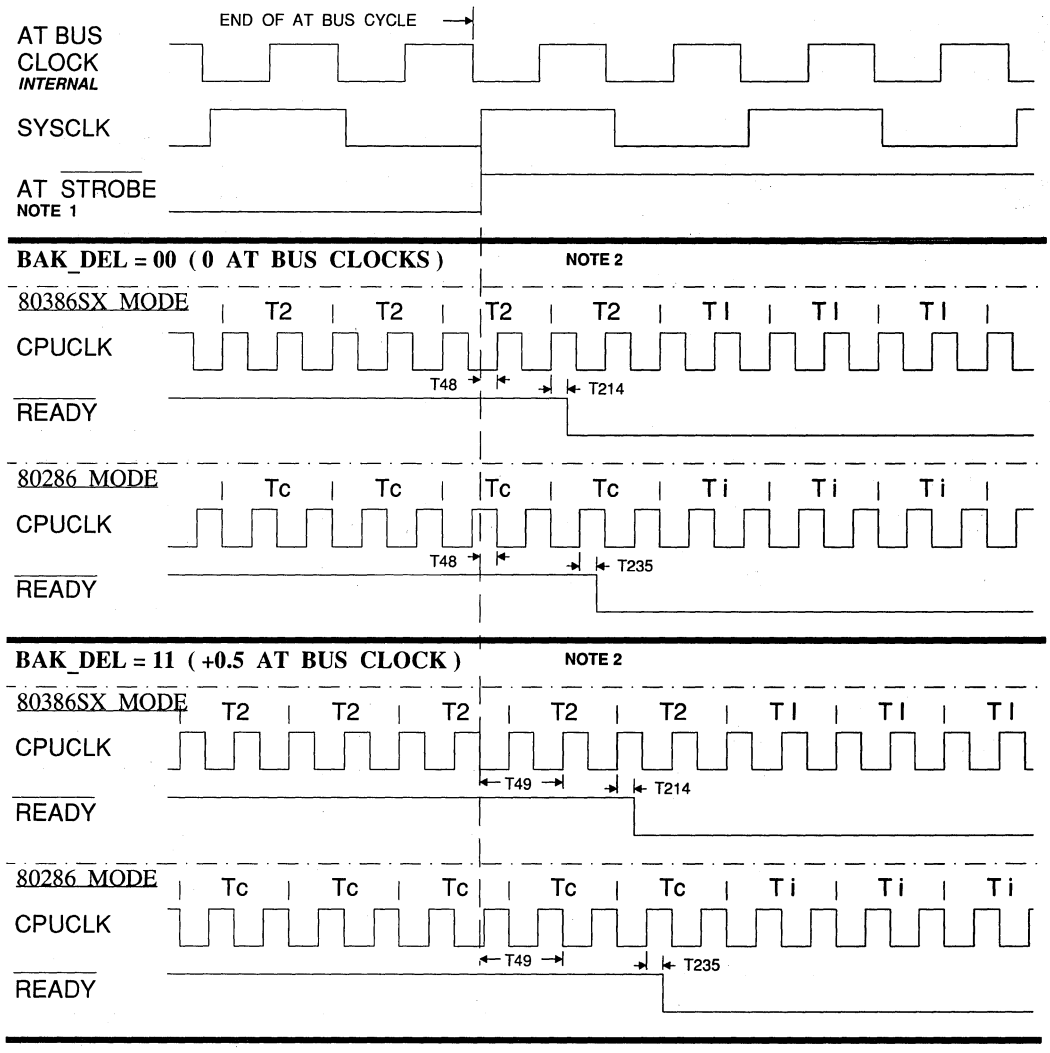


NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 12-40. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = -1 OR -0.5 AT BUS CLOCKS



NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 12-41. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = 0 OR +0.5 AT BUS CLOCKS

12.2.4 DMA Cycles

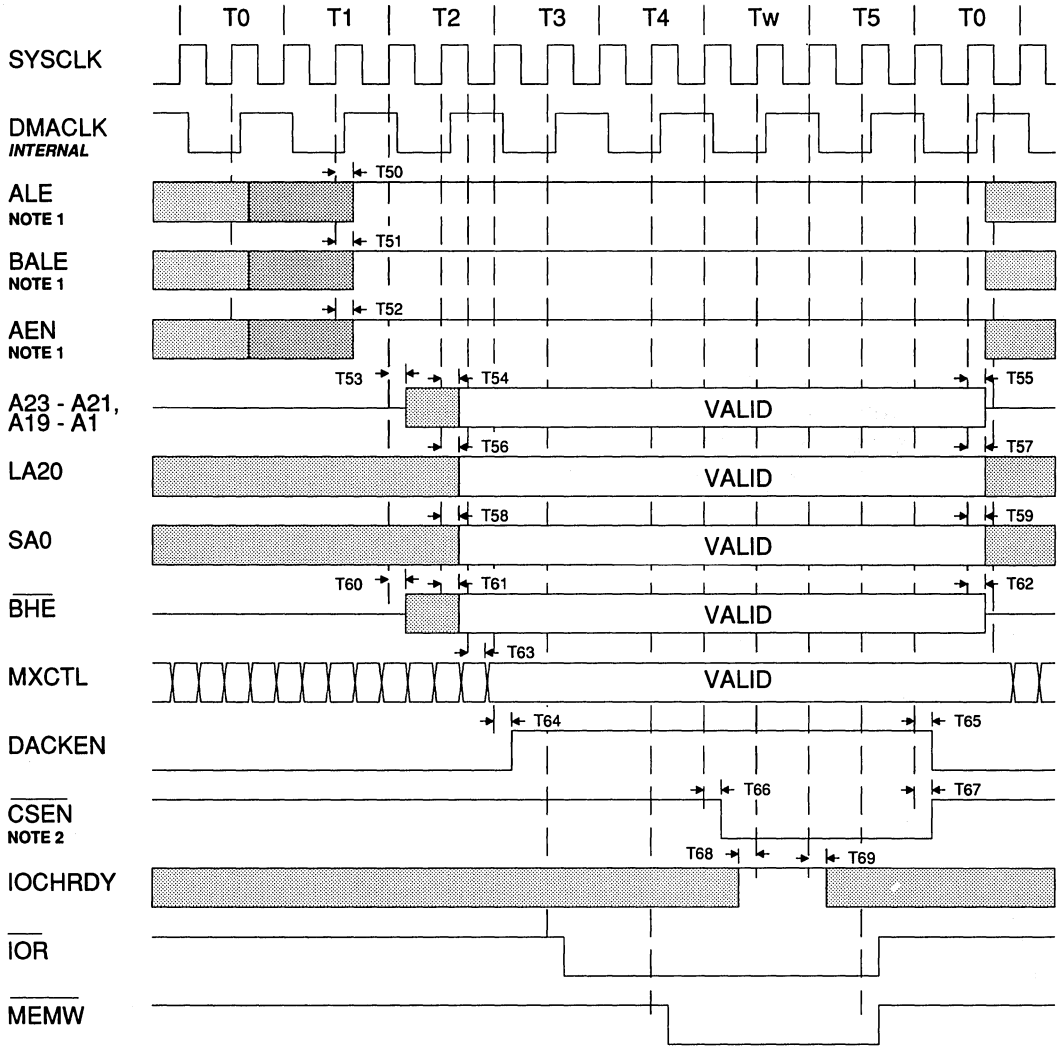
Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T54	SYSCLK rise to Address valid		60	ns	
T55	Address hold from SYSCLK rise	0		ns	
T56	SYSCLK rise to LA20 valid		49	ns	
T57	LA20 hold from SYSCLK rise	0		ns	
T58	SYSCLK rise to SA0 valid		40	ns	
T59	SA0 hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T66	SYSCLK rise to $\overline{CSEN}$ fall		32	ns	
T67	SYSCLK rise to $\overline{CSEN}$ rise		33	ns	
T68	IOCHRDY setup to SYSCLK rise	12		ns	
T69	IOCHRDY hold from SYSCLK rise	0		ns	
T70	SYSCLK rise to $\overline{IOR}$ fall		28	ns	
T71	SYSCLK rise to $\overline{IOR}$ rise		35	ns	
T72	SYSCLK rise to $\overline{MEMW}$ fall		47	ns	
T73	SYSCLK rise to $\overline{MEMW}$ rise		35	ns	
T74	SYSCLK rise to $\overline{DEN1}$ fall		32	ns	I/O to memory
T75	SYSCLK rise to $\overline{DEN1}$ rise		42	ns	I/O to memory
T76	SYSCLK rise to $\overline{DEN0}$ fall		32	ns	I/O to memory
T77	SYSCLK rise to $\overline{DEN0}$ rise		42	ns	I/O to memory
T78	SYSCLK rise to $\overline{SDEN}$ fall		21	ns	
T79	SYSCLK rise to $\overline{SDEN}$ rise		37	ns	I/O to memory

TABLE 12-11. DMA CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T80	SYSCLK rise to SDTR rise		30	ns	
T81	SYSCLK rise to SDTR fall		20	ns	
T82	SYSCLK rise to $\overline{IOW}$ fall		53	ns	
T83	SYSCLK rise to $\overline{IOW}$ rise		37	ns	
T84	SYSCLK rise to $\overline{MEMR}$ fall		17	ns	
T85	SYSCLK rise to $\overline{MEMR}$ rise		38	ns	
T86	SYSCLK rise to $\overline{DEN1}$ fall		22	ns	Memory to I/O
T87	SYSCLK rise to $\overline{DEN1}$ rise		116	ns	Memory to I/O
T88	SYSCLK rise to $\overline{DEN0}$ fall		22	ns	Memory to I/O
T89	SYSCLK rise to $\overline{DEN0}$ rise		116	ns	Memory to I/O
T90	SYSCLK rise to $\overline{SDEN}$ rise		116	ns	Memory to I/O
T91	SYSCLK rise to DTR rise		31	ns	
T92	SYSCLK rise to DTR fall		22	ns	
T100	$\overline{MEMW}$ fall to $\overline{RASn}$ fall		27	ns	
T101	$\overline{MEMW}$ rise to $\overline{RASn}$ rise		29	ns	
T102	$\overline{MEMW}$ fall to $\overline{CASn}$ fall		108	ns	
T103	$\overline{MEMW}$ rise to $\overline{CASn}$ rise		30	ns	
T105	$\overline{MEMW}$ fall to RA10 - RA0 valid		100	ns	
T107	$\overline{MEMW}$ fall to W/$\overline{R}$ high		29	ns	
T108	$\overline{MEMW}$ rise to W/$\overline{R}$ low	10		ns	
T120	$\overline{MEMR}$ fall to $\overline{RASn}$ fall		28	ns	
T121	$\overline{MEMR}$ rise to $\overline{RAS}$ rise		29	ns	
T122	$\overline{MEMR}$ fall to $\overline{CASn}$ fall		110	ns	
T123	$\overline{MEMR}$ rise to $\overline{CAS}$ rise		31	ns	
T125	$\overline{MEMR}$ fall to RA10 - RA0 valid		100	ns	
T126	$\overline{MEMR}$ fall to DPH, DPL float		25		
T127	$\overline{MEMR}$ rise to DPH, DPL driven	35			
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T305	D15 - D0 setup to $\overline{MEMR}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{MEMR}$ rise	10		ns	

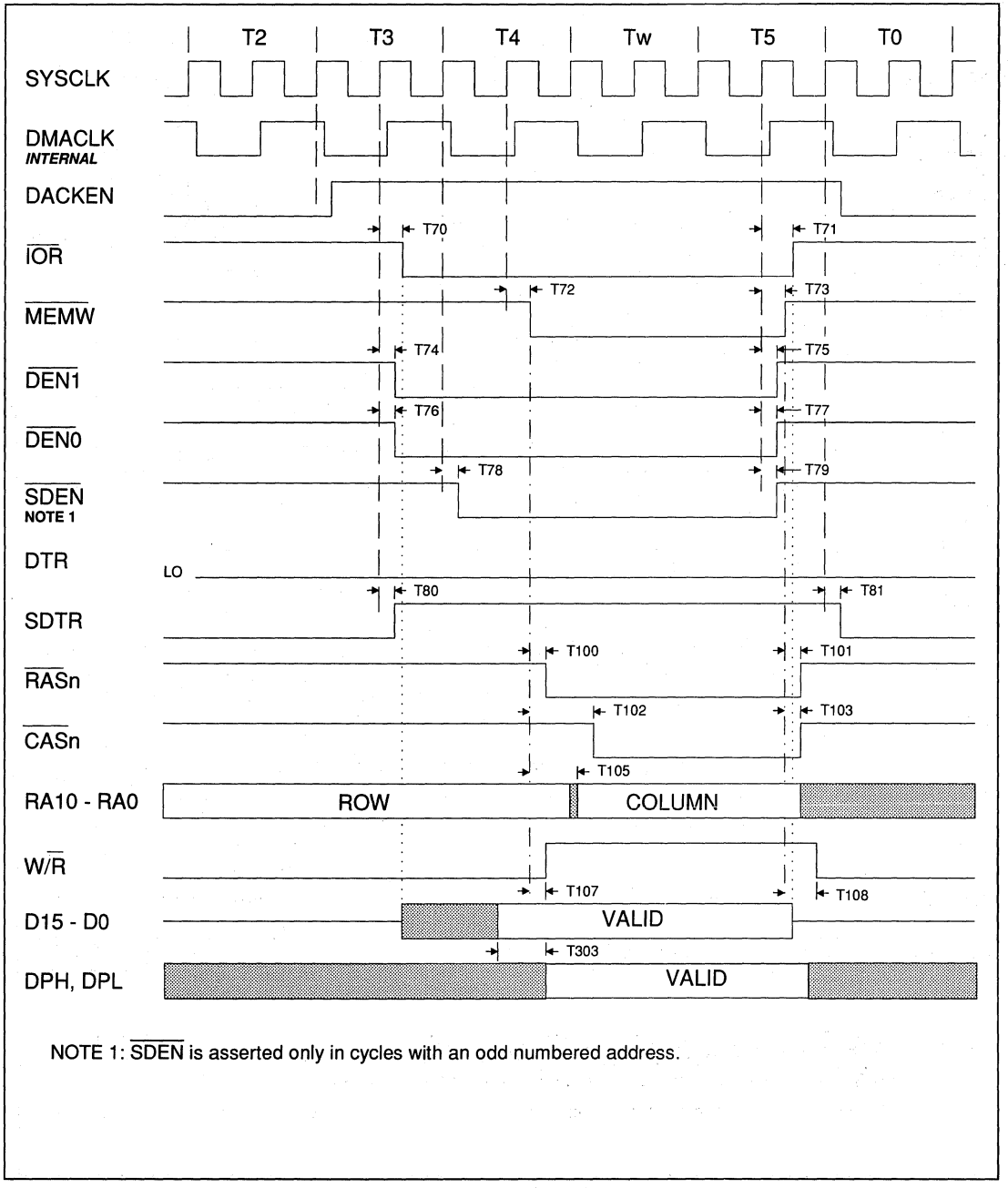
TABLE 12-11. DMA CYCLES cont.



NOTE 1: ALE, BALE and AEN may be asynchronous. Minimum valid time is shown. DMA channels 0, 1, 2, and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

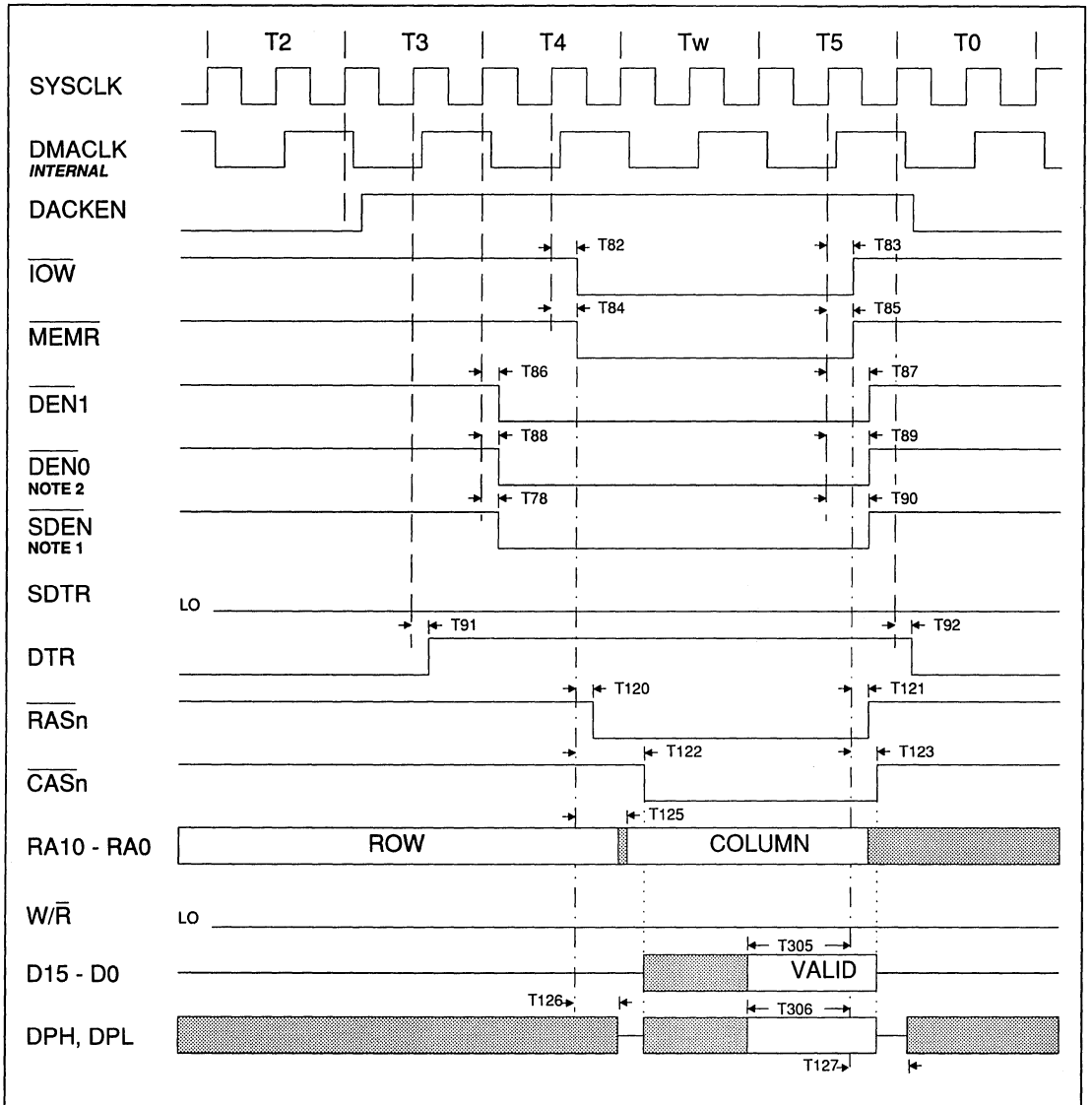
NOTE 2: $\overline{\text{CSEN}}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

FIGURE 12-42. BASIC DMA CYCLE, DEFAULT TIMING



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.

FIGURE 12-43. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.
NOTE 2: $\overline{\text{DEN0}}$ is asserted only in cycles with an even numbered address.

FIGURE 12-44. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O

12.2.5 AT Bus Master

The AT bus master timing is covered in the following sequence:

- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T55	Address hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T150	$\overline{MASTER}$ fall to AEN fall		30	ns	
T151	$\overline{MASTER}$ rise to AEN rise		30	ns	
T152	$\overline{MASTER}$ fall to A23 - A21, A19 - A1 float		30	ns	
T153	$\overline{MASTER}$ rise to A23 - A21, A19 - A1 driven	15		ns	
T154	$\overline{MASTER}$ fall to LA20 float		23	ns	
T155	$\overline{MASTER}$ rise to LA20 driven	10		ns	
T156	$\overline{MASTER}$ fall to SA0 float		24	ns	
T157	$\overline{MASTER}$ rise to SA0 driven	10		ns	
T158	$\overline{MASTER}$ fall to $\overline{BHE}$ float		30	ns	
T159	$\overline{MASTER}$ rise to $\overline{BHE}$ driven	10		ns	
T160	$\overline{MASTER}$ fall to $\overline{CSEN}$ fall		32	ns	
T161	$\overline{MASTER}$ rise to $\overline{CSEN}$ rise		35	ns	
T162	$\overline{MASTER}$ fall to $\overline{MEMR}$ float		24	ns	
T163	$\overline{MASTER}$ rise to $\overline{MEMR}$ driven	10		ns	
T164	$\overline{MASTER}$ fall to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, float		23	ns	
T165	$\overline{MASTER}$ rise to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$ driven	10		ns	

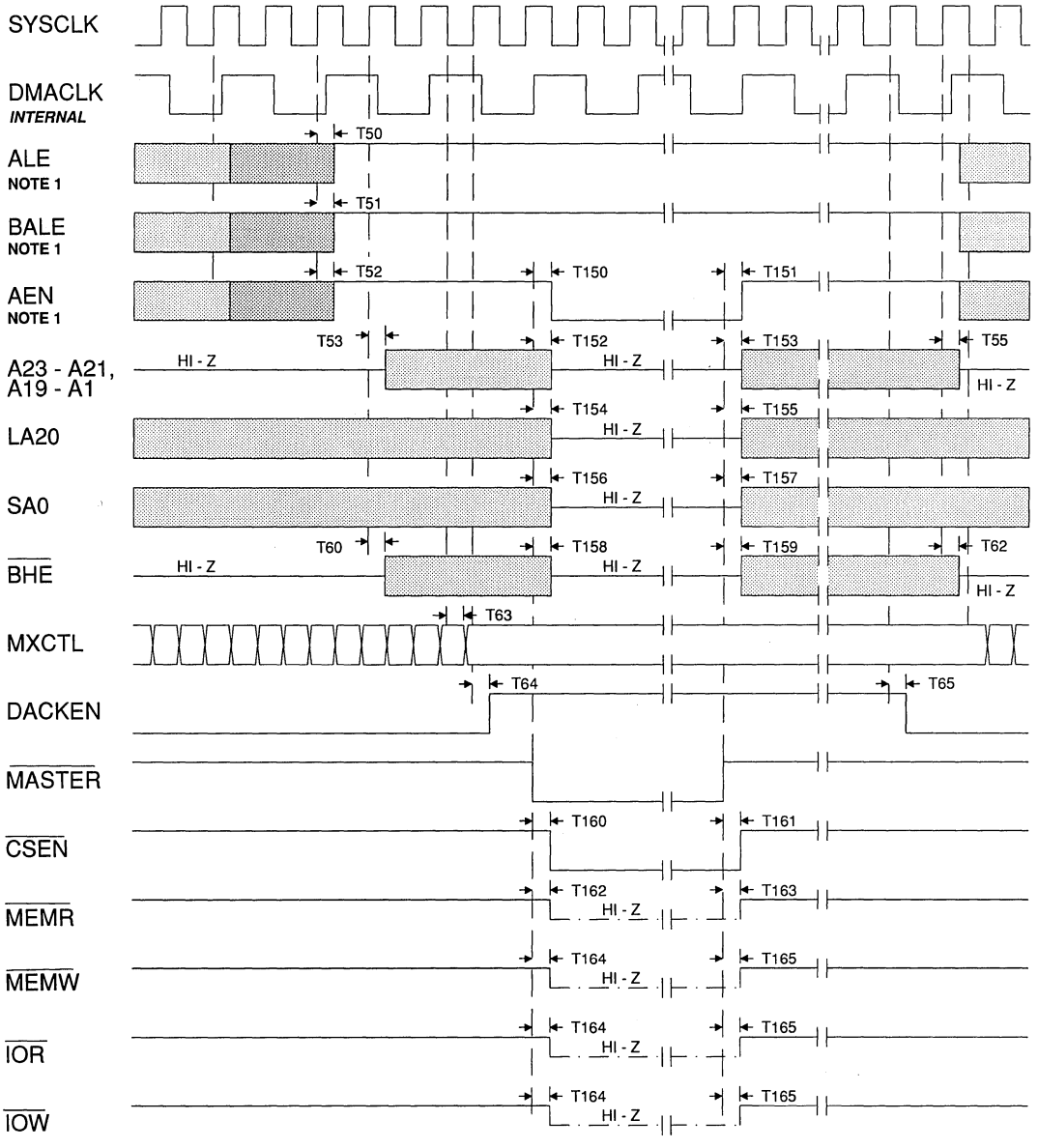
TABLE 12-12. AT BUS MASTER CYCLE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T166	A23 - A21, A19 - A1 setup to MEMR, MEMW	45		ns	
T167	LA20 setup to MEMR, MEMW	50		ns	
T168	BHE setup to MEMR, MEMW	0		ns	
T169	SA0 setup to MEMR, MEMW	0		ns	
T170	A23 - A21, A19 - A1 hold from MEMR, MEMW	15		ns	
T171	LA20 hold from MEMR, MEMW	15		ns	
T172	BHE hold from MEMR, MEMW	15		ns	
T173	SA0 hold from MEMR, MEMW	15		ns	
T174	SA0 in to A0 out delay		45	ns	
T175	MEMW fall to DEN1 fall		30	ns	
T176	MEMW fall to DEN0 fall		30	ns	
T177	MEMW rise to DEN1 rise		83	ns	
T178	MEMW rise to DEN0 rise		83	ns	
T179	MEMR fall to DEN1 fall		85	ns	
T180	MEMR fall to DEN0 fall		85	ns	
T181	MEMR rise to DEN1 rise		32	ns	
T182	MEMR rise to DEN0 rise		32	ns	
T183	MEMR fall to DTR rise		29	ns	
T184	MEMR rise to DTR fall		82	ns	
T190	MEMR, MEMW fall to RASn fall		83	ns	
T191	MEMR, MEMW rise to RASn rise		33	ns	
T192	MEMR, MEMW fall to CASn fall		126	ns	
T193	MEMR, MEMW rise to CASn rise		33	ns	
T194	MEMR, MEMW fall to RA10 - RA0 column address valid		120	ns	
T196	MEMR, MEMW fall to RA10 - RA0 row address valid		42	ns	
T197	RA10 - RA0 column address hold from MEMR, MEMW rise	5		ns	

TABLE 12-12. AT BUS MASTER CYCLE cont.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T300	$\overline{\text{MEMW}}$ fall to W/$\overline{\text{R}}$ rise		33	ns	
T301	$\overline{\text{MEMW}}$ rise to W/$\overline{\text{R}}$ fall	10		ns	
T302	$\overline{\text{MEMW}}$ fall to DPH, DPL valid		32	ns	
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T304	DPH, DPL hold from $\overline{\text{MEMW}}$ rise	5		ns	
T305	D15 - D0 setup to $\overline{\text{MEMR}}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{\text{MEMR}}$ rise	10		ns	
T307	$\overline{\text{MEMR}}$ fall to DPH, DPL float		35	ns	
T308	$\overline{\text{MEMR}}$ rise to DPH, DPL driven	58		ns	

TABLE 12-12. AT BUS MASTER CYCLE cont.



NOTE 1: The shaded regions of ALE, BALE and AEN show a possible asynchronous relarionship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

FIGURE 12-45. AT BUS MASTER, BUS ACQUISITION/RELEASE

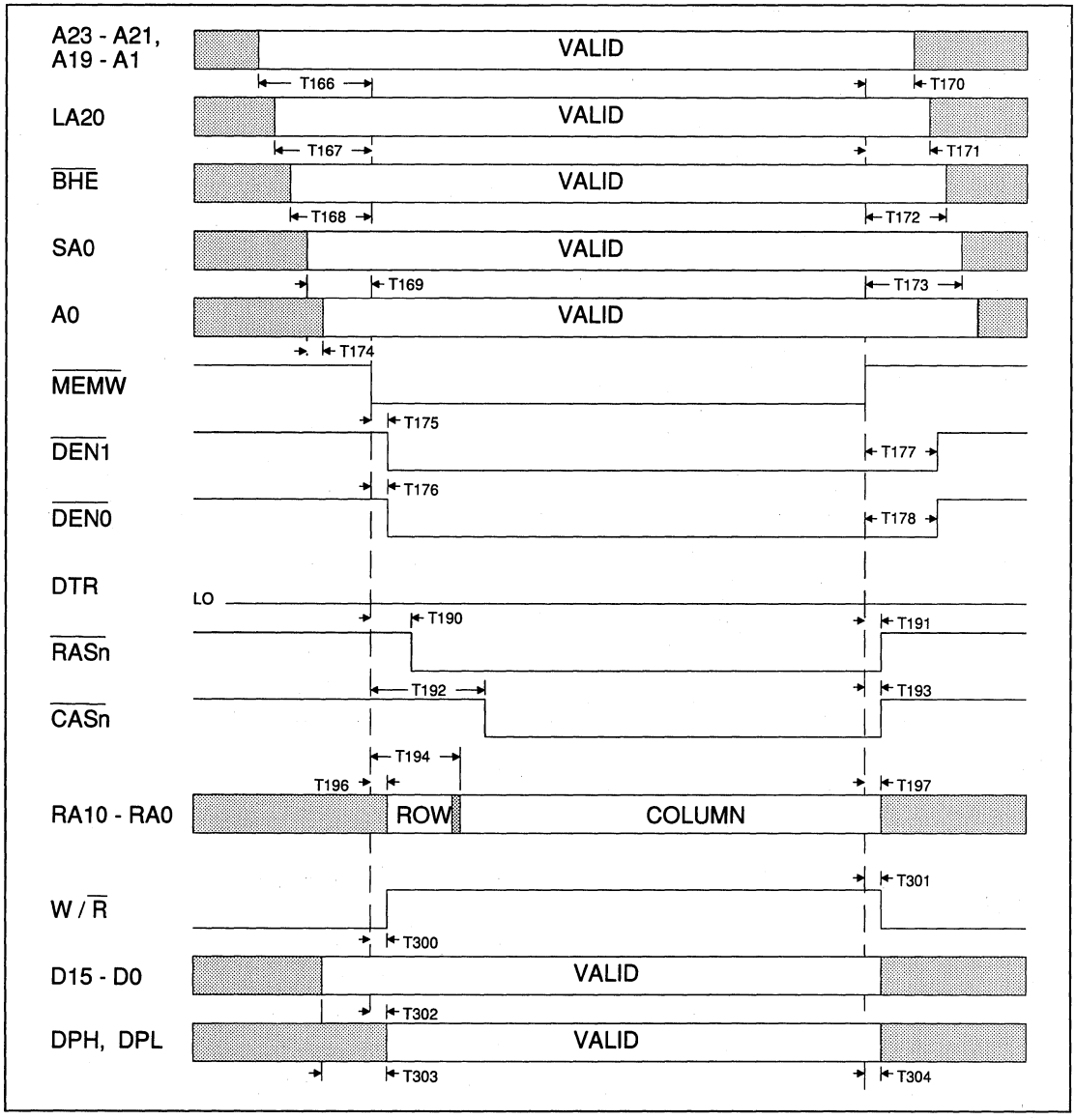


FIGURE 12-46. AT BUS MASTER, WRITE TO ON-BOARD MEMORY

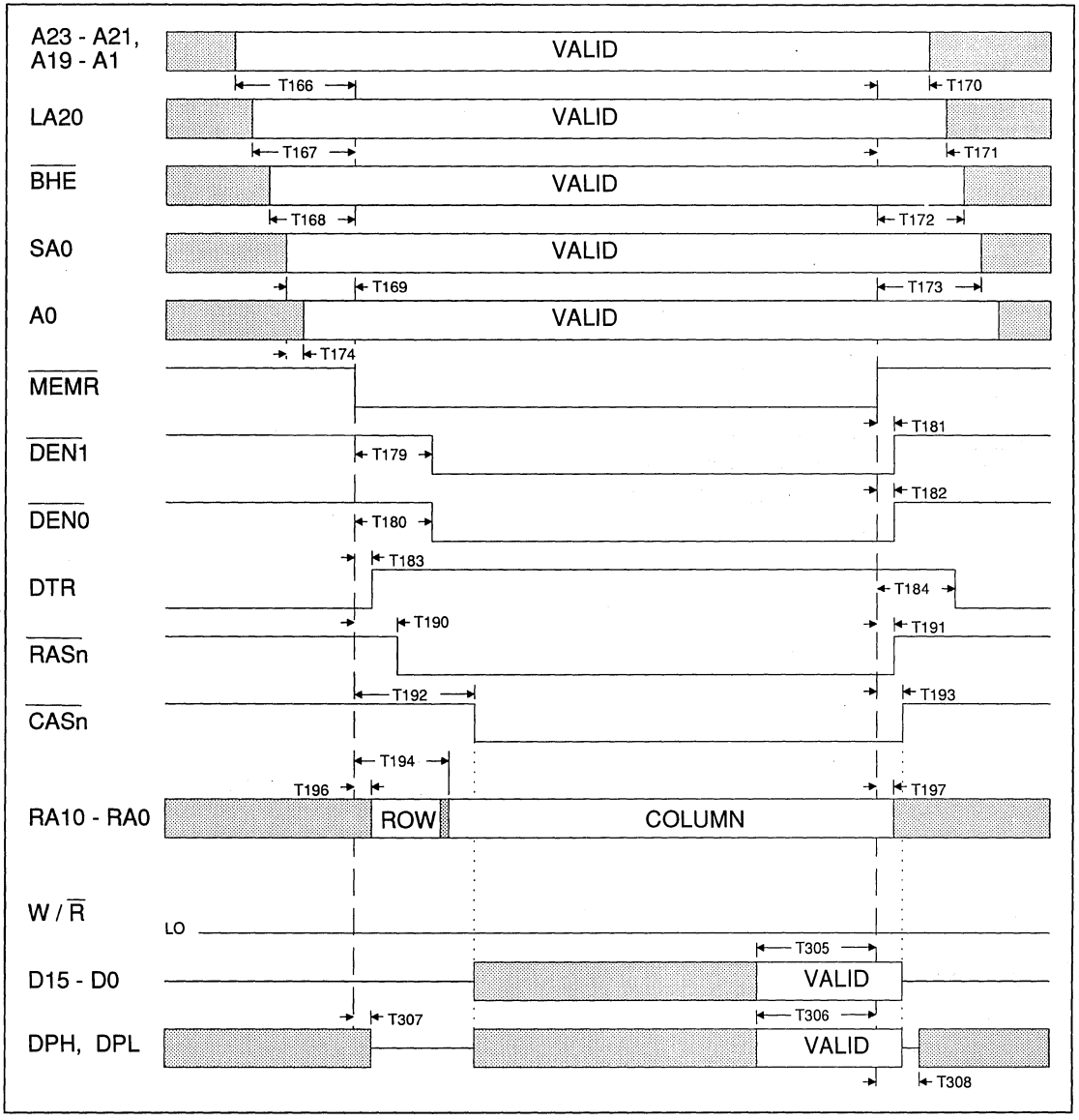


FIGURE 12-47. AT BUS MASTER, READ FROM ON-BOARD MEMORY

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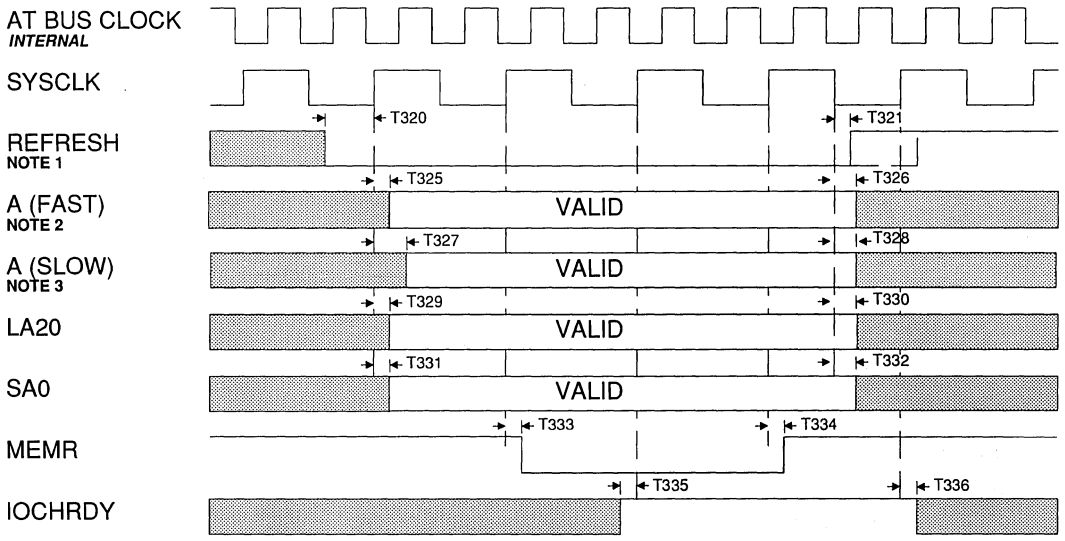
12.2.6 AT Bus Refresh

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T320	$\overline{\text{REFRESH}}$ low before SYSCLK rise	4		ns	$\overline{\text{REFRESH}}$ setup is number given plus (T00 x 0.25)
T321	SYSCLK fall to $\overline{\text{REFRESH}}$ rise		16	ns	
T325	SYSCLK rise to A23 - A21, A19 - A16 and A7 - A1 valid		35	ns	
T326	SYSCLK fall to A23 - A21, A19 - A16 and A7 - A1 invalid	2		ns	
T327	SYSCLK rise to A20, A15 - A8 valid		45	ns	
T328	SYSCLK fall to A20, A15 - A8 invalid	2		ns	
T329	SYSCLK rise to LA20 valid		30	ns	
T330	SYSCLK fall to LA20 invalid	2		ns	
T331	SYSCLK rise to SA0 valid		30	ns	
T332	SYSCLK fall to SA0 invalid	2		ns	
T333	SYSCLK rise to $\overline{\text{MEMR}}$ low		8	ns	
T334	SYSCLK rise to $\overline{\text{MEMR}}$ high		7	ns	
T335	IOCHRDY setup to SYSCLK rise	23		ns	
T336	IOCHRDY hold time from SYSCLK rise	0		ns	

TABLE 12-13. AT BUS REFRESH CYCLE, DEFAULT TIMING



NOTE 1: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

NOTE 2: (FAST) is address lines A23 - A21, A19 - A16 and A7 - A1.

NOTE 3: (SLOW) is address lines A20, and A15 - A8

FIGURE 12-48. AT BUS REFRESH CYCLE, DEFAULT TIMING

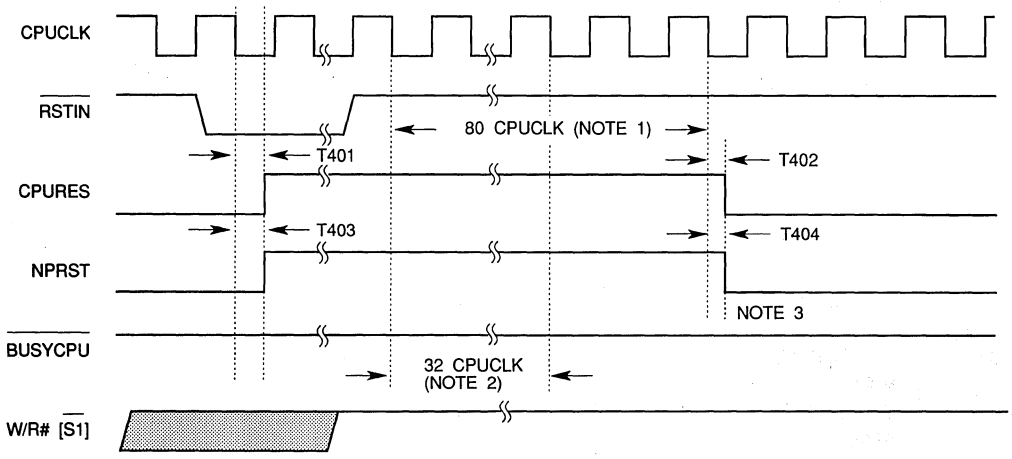
12.3 PROCESSOR TIMING

This section covers the 80286 CPU timing, followed by the 80386SX.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T140	See Table 12-9				
T141	See Table 12-9				
T143	See Table 12-9				
T401	CPUCLK fall to CPURES rise delay		14	ns	
T402	CPUCLK fall to CPURES fall delay		13	ns	
T403	CPUCLK fall to NPRST rise delay		14	ns	
T404	CPUCLK fall to NPRST fall delay		13	ns	
T405	CPUCLK fall to $\overline{\text{BUSYCPU}}$ fall delay		35	ns	①
T406	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35	ns	①
T408	$\overline{\text{SO}}$, $\overline{\text{S1}}$ setup time to CPUCLK	9		ns	
T409	$\overline{\text{SO}}$, $\overline{\text{S1}}$ hold time to CPUCLK	1		ns	
T410	M/$\overline{\text{IO}}$ setup time to CPUCLK	26		ns	
T411	M/$\overline{\text{IO}}$ hold time to CPUCLK	1		ns	
T412	Address setup time to CPUCLK	26		ns	
T413	Address hold time to CPUCLK	1		ns	
T414	$\overline{\text{PEACK}}$ setup time to CPUCLK	7		ns	
T415	$\overline{\text{PEACK}}$ hold time to CPUCLK	1		ns	
T416	DPH, DPL setup time to CPUCLK fall	5		ns	
T417	DPH, DPL hold time from CPUCLK fall	19		ns	
T418	D15 - D0 setup time to CPUCLK fall	5		ns	
T419	D15 - D0 hold time from CPUCLK fall	19		ns	

① T405 and T406 are for reference only since $\overline{\text{BUSYCPU}}$ is an asynchronous signal to the 80286. These two parameters are guaranteed by design and will not be tested.

TABLE 12-14. 80286 CPU TIMING

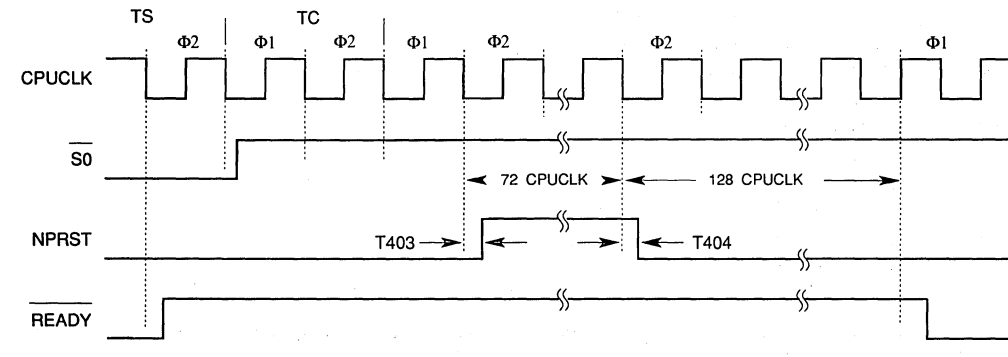


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

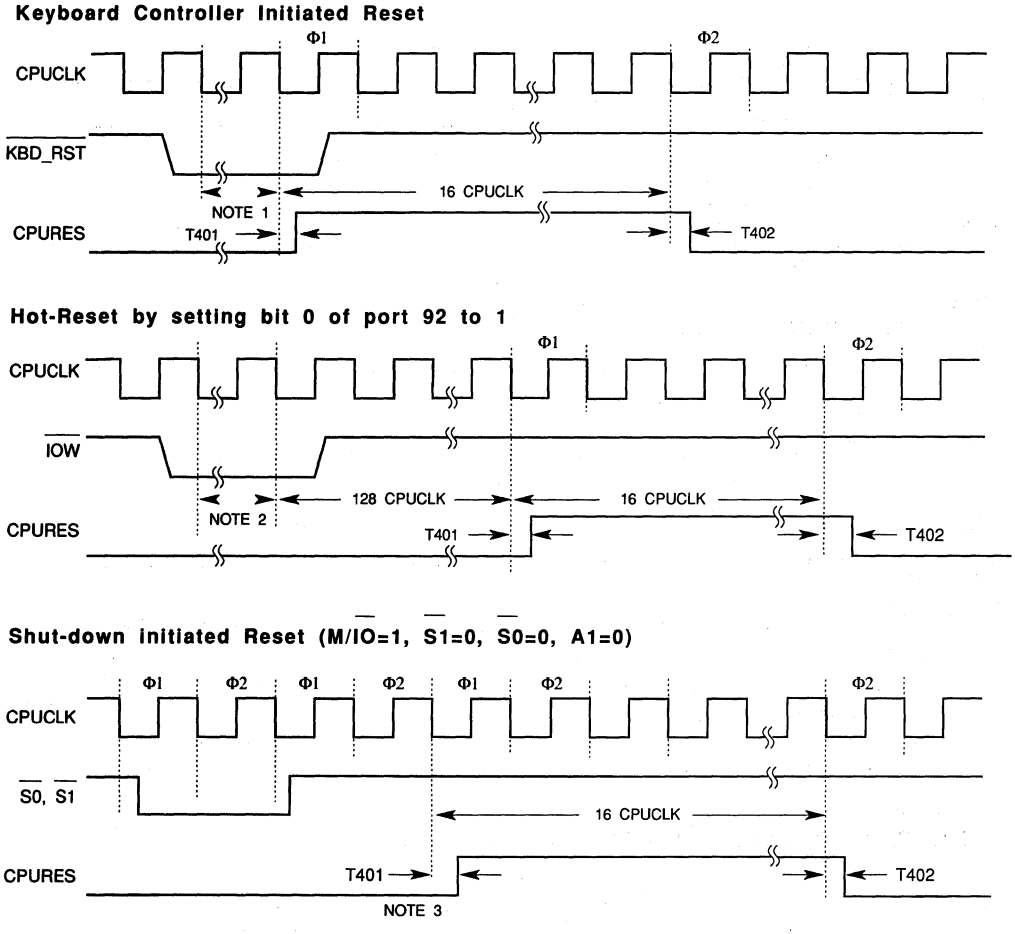
FIGURE 12-49. 80286 - CPURES AND NPRST DURING POWER UP



NOTE 1: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 2: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's C287A.

FIGURE 12-50. 80286 - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1

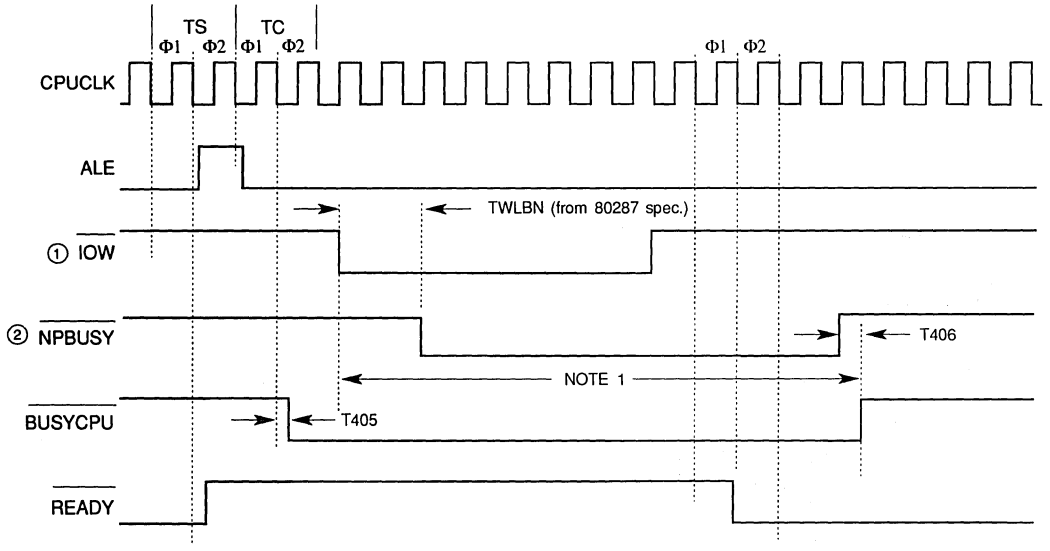


NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is asserted at the beginning of phase 1 to maintain the phase relationship with the 80286.

FIGURE 12-51. 80286 - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET



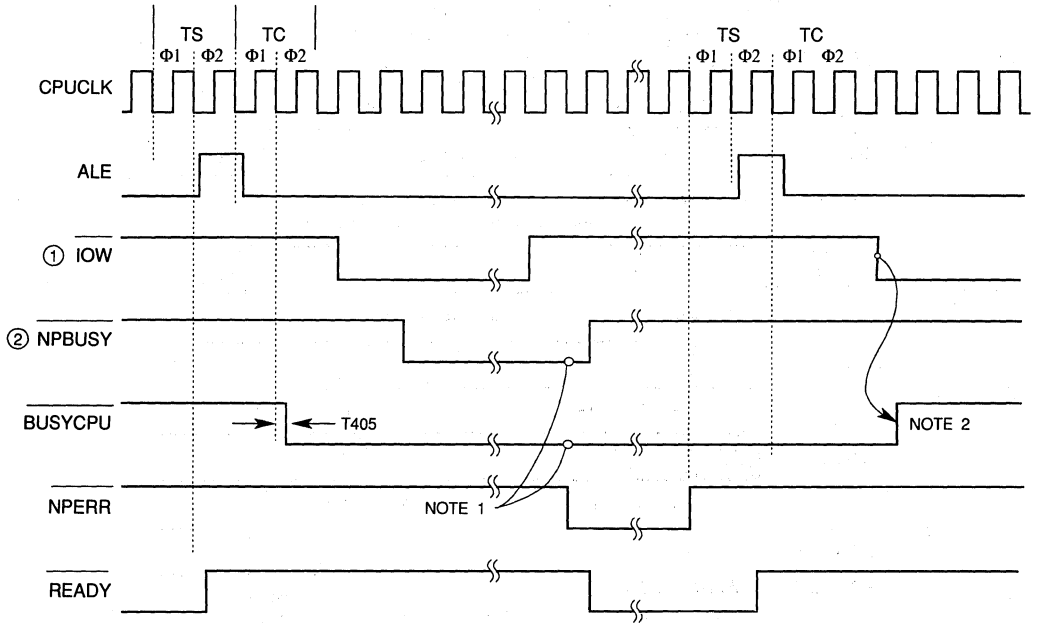
① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: During a write to the 80287, $\overline{\text{BUSYCPU}}$ is asserted at the middle of the first Tc and continues for one SYSCLK plus two CPUCLKs beyond the active edge of $\overline{\text{IOW}}$, then follows the NPBUSY from the 80287. This early assertion of BUSYCPU is required to maintain compatibility with the 80287.

FIGURE 12-52. 80286 - $\overline{\text{BUSYCPU}}$ ASSERTED DURING COPROCESSOR ACCESS

7



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: $\overline{\text{BUSYCPU}}$ is latched by the leading edge of the $\overline{\text{NPERR}}$ signal from the coprocessor while $\overline{\text{NPBUSY}}$ from the coprocessor is still active.

NOTE 2: $\overline{\text{BUSYCPU}}$ is de-asserted by the leading edge of $\overline{\text{IOW}}$, delayed by a low half of SYSCLK, when any data is written to port F0. $\overline{\text{BUSYCPU}}$ can be an asynchronous signal to the processor and is shown for reference only.

FIGURE 12-53. 80286 - LATCHING $\overline{\text{BUSYCPU}}$ WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

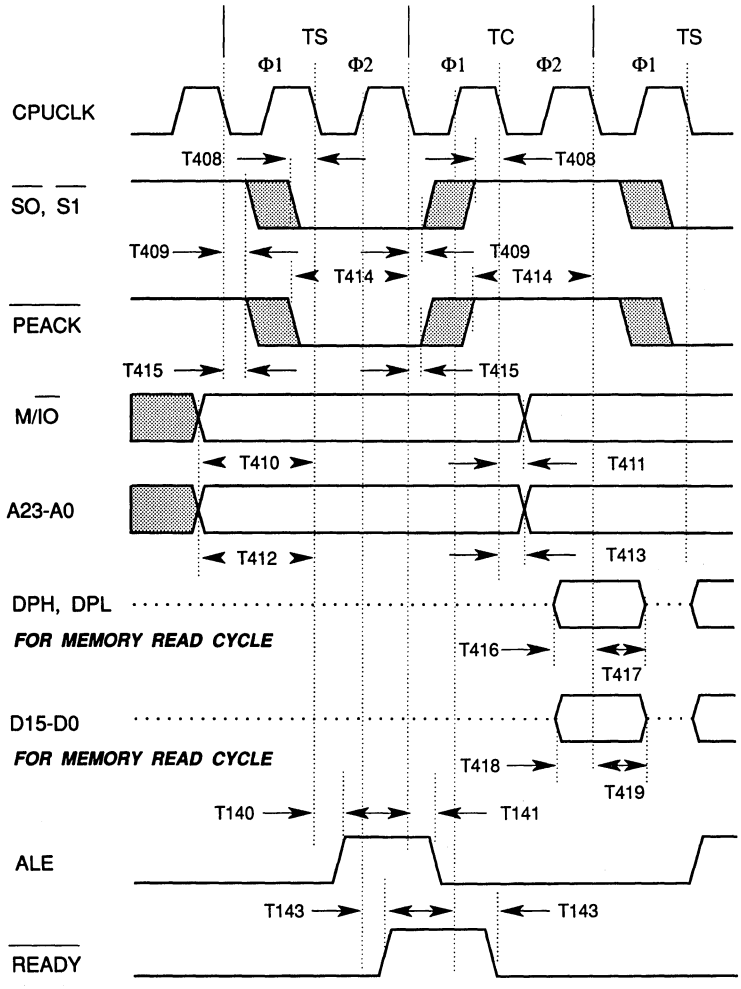


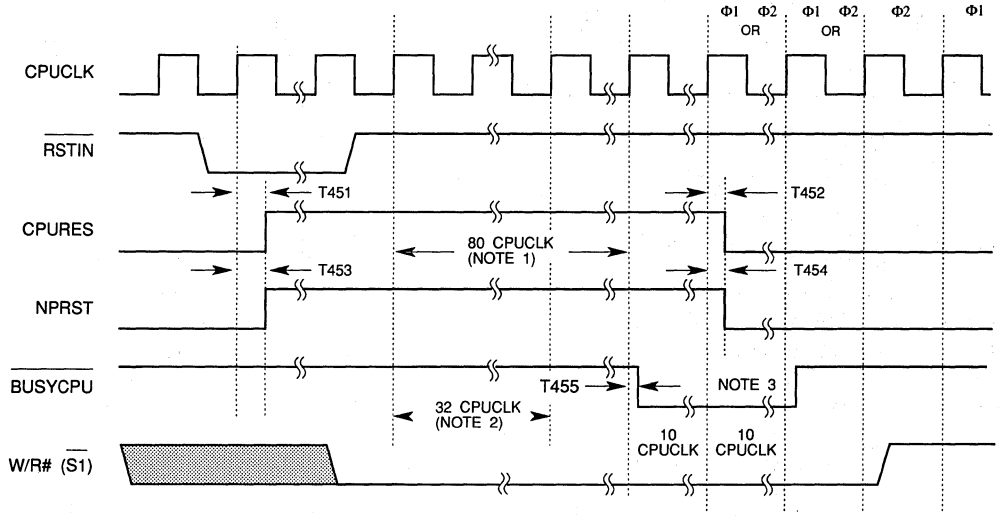
FIGURE 12-54. 80286 - MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T140	See Table 12-9					
T141	See Table 12-9					
T204	See Table 12-6					
T214	See Table 12-6					
T215	See Table 12-6					
T451	CPUCLK rise to CPURES rise delay		14		10	ns
T452	CPUCLK rise to CPURES fall delay		13		10	ns
T453	CPUCLK rise to NPRST rise delay		14		10	ns
T454	CPUCLK rise to NPRST fall delay		13		10	ns
T455	CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay		35		35	ns
T456	CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay		35		30	ns
T457	$\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay		30		30	ns
T458	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35		35	ns
T460	$\overline{\text{NPERR}}$ fall to EPEREQ rise delay		30		30	ns
T462	ADS# setup time to CPUCLK rise	14		10		ns
T463	ADS# hold time from CPUCLK rise	5		4		ns
T464	W/R# setup time to CPUCLK rise	14		8		ns
T465	W/R# hold time from CPUCLK rise	5		4		ns
T466	D/C# setup time to CPUCLK rise	14		6		ns
T467	D/C# hold time from CPUCLK rise	5		4		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise	17		15		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	5		4		ns
T470	$\overline{\text{BHE}}$ setup time to CPUCLK rise	17		15		ns
T471	$\overline{\text{BHE}}$ hold time from CPUCLK rise	3		4		ns

TABLE 12-15. 80386SX CPU TIMING

SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T472	HLDA setup time to CPUCLK rise	10		6		ns
T473	HLDA hold time from CPUCLK rise	3		4		ns
T474	HOLD valid delay from CPUCLK rise		26		20	ns
T475	DPH setup time to CPUCLK rise	5		5		ns
T476	DPH hold time from CPUCLK rise	19		19		ns
T477	D15-D0 setup time to CPUCLK rise	5		5		ns
T478	D15-D0 hold time from CPUCLK rise	19		19		ns
T479	A23-A1, BLE# setup time to CPUCLK rise	40		38		ns
T480	A23-A1, BLE# hold time from CPUCLK rise	3		4		ns

TABLE 12-15. 80386SX CPU TIMING cont.

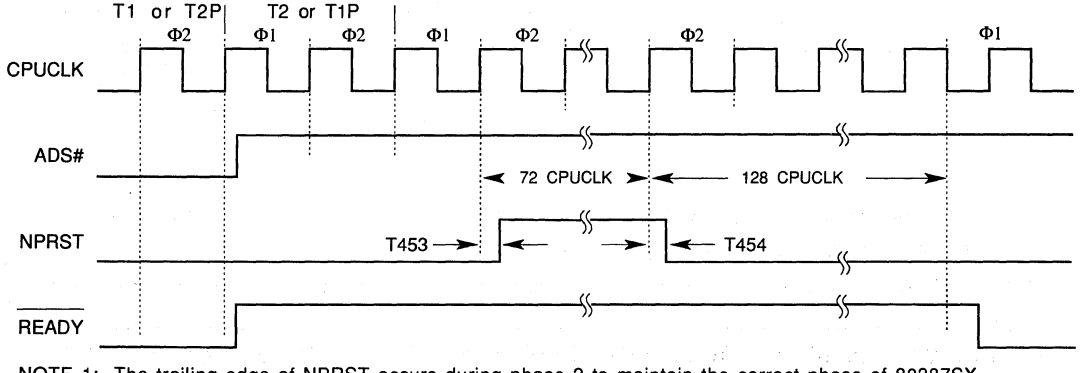


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

FIGURE 12-55. 80386SX - CPURES AND NPRST DURING POWER UP



NOTE 1: The trailing edge of NPRST occurs during phase 2 to maintain the correct phase of 80387SX with the 80386SX.

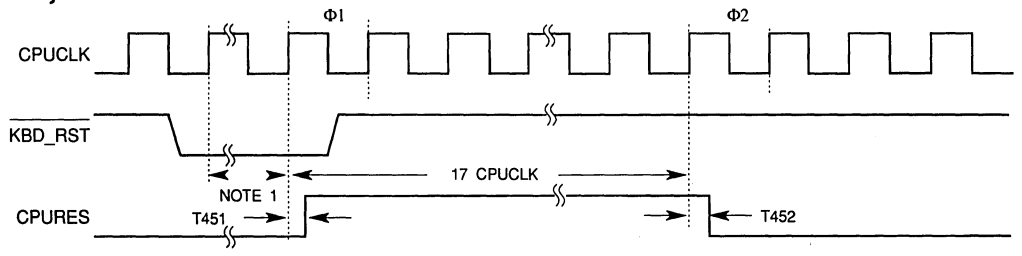
NOTE 2: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 3: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's 80C287A.

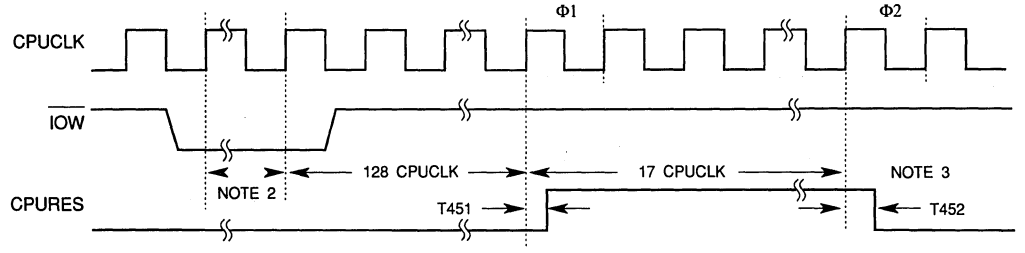
NOTE 4: 25 MHz operation requires a minimum of 8 MHz for AT Bus Clock.

FIGURE 12-56. 80386SX - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1

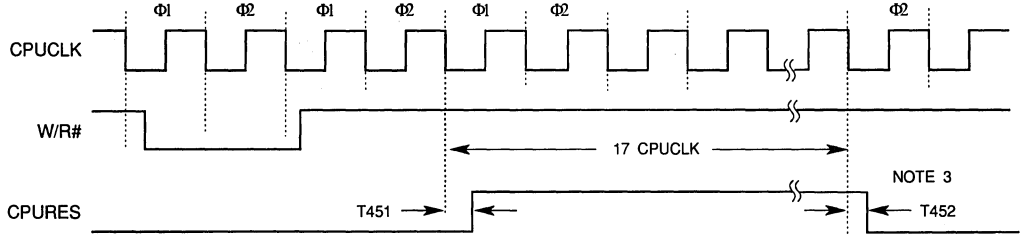
Keyboard Controller Initiated Reset



Hot-Reset by setting bit 0 of port 92 to 1



Shut-down initiated Reset (W/R#=1, D/C#=0, M/$\overline{IO}$=1, $\overline{BHE}$=1, BLE#=0, A1=0)



NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

FIGURE 12-57. 80386SX - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

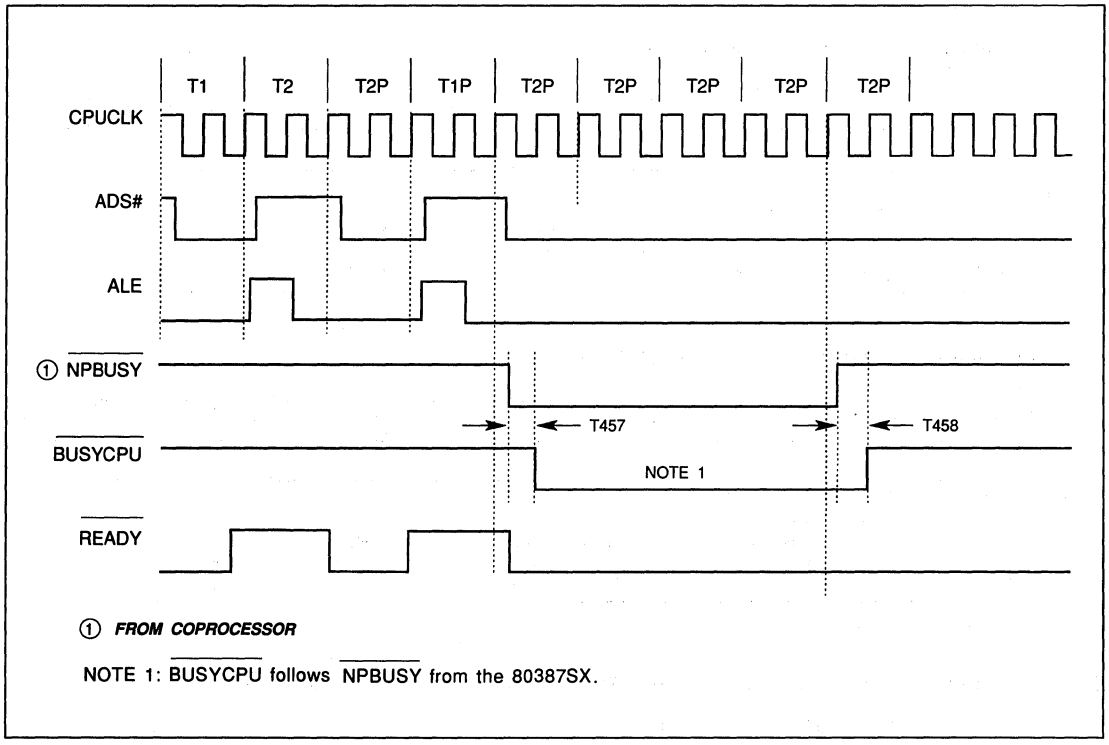
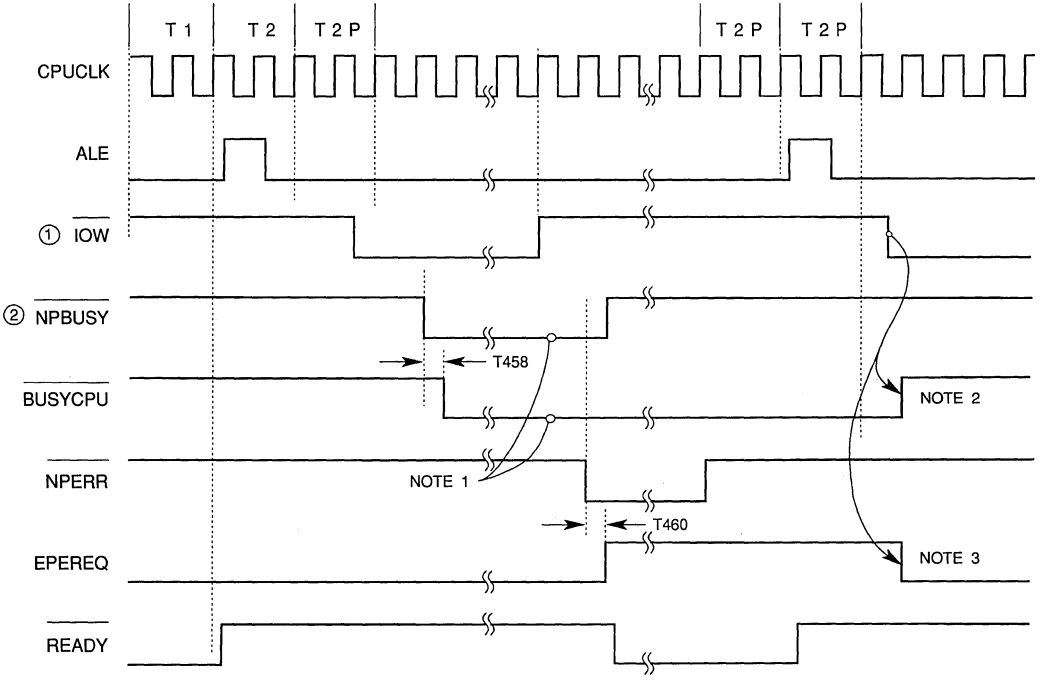


FIGURE 12-58. BUSYCPU ASSERTION DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW delayed by a low half of SYSCLK when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

NOTE 3: EPEREQ is asserted if NPERR occurs while NPBUSY from the coprocessor is active. EPEREQ is de-asserted by the leading edge of IOW delayed by the low half of SYSCLK when any data is written to port F0. EPEREQ can be asynchronous to the processor and is shown for reference only.

FIGURE 12-59. 80386SX - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

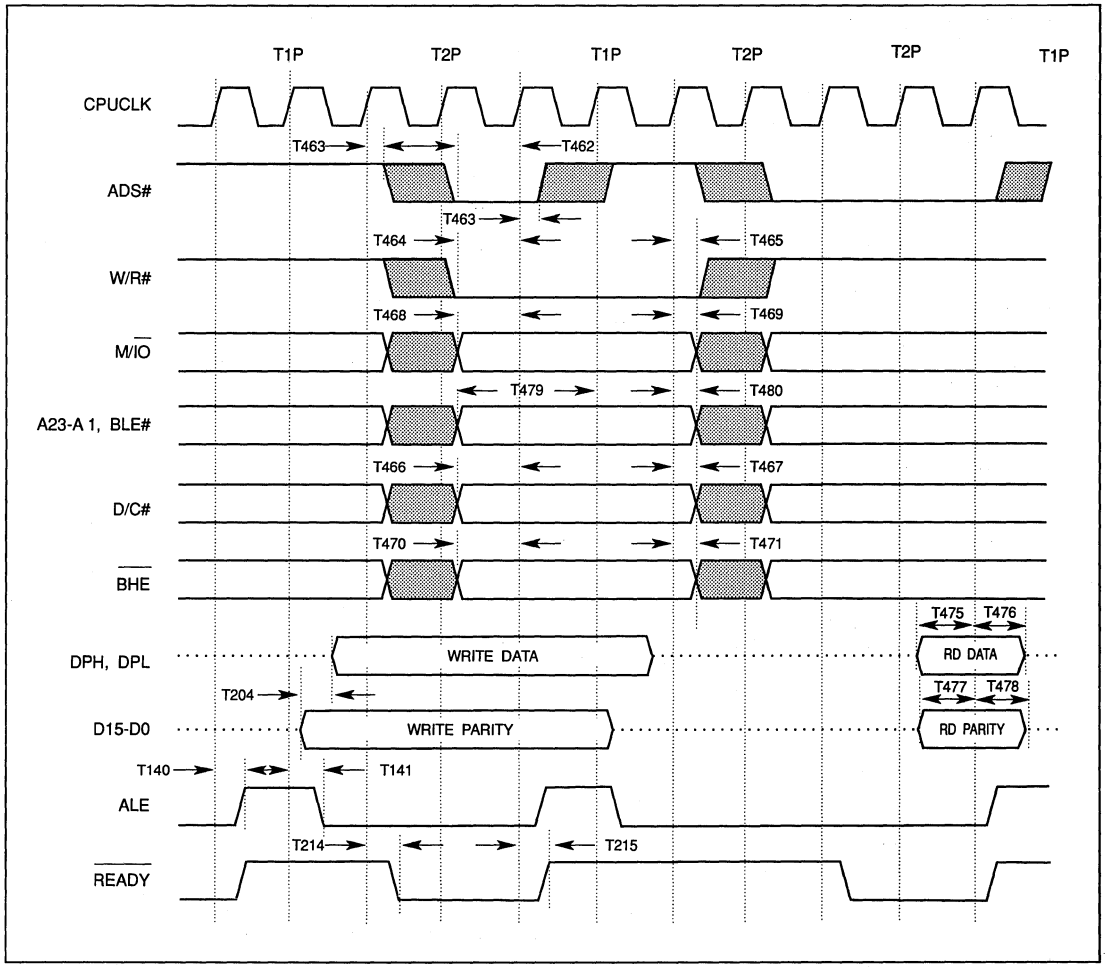


FIGURE 12-60. 80386SX - MISCELLANEOUS TIMING

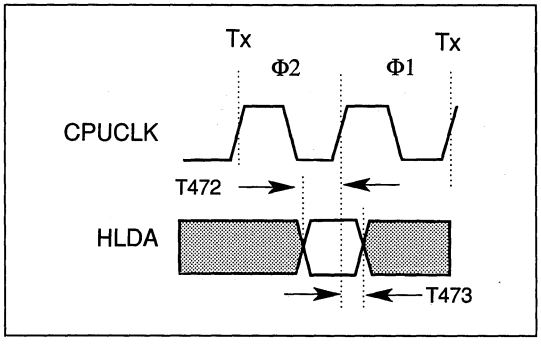


FIGURE 12-61. 80386SX - INPUT SETUP AND HOLD TIMING

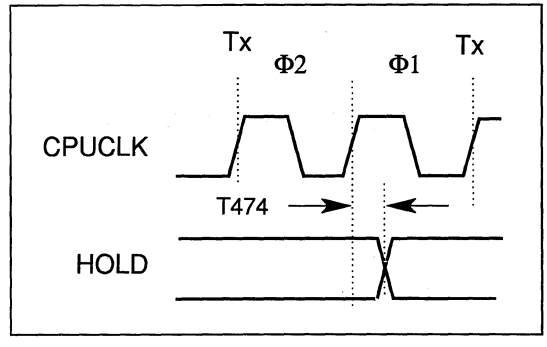


FIGURE 12-62. 80386SX - OUTPUT DELAY TIMING

12.4 CACHE CONTROLLER TIMING

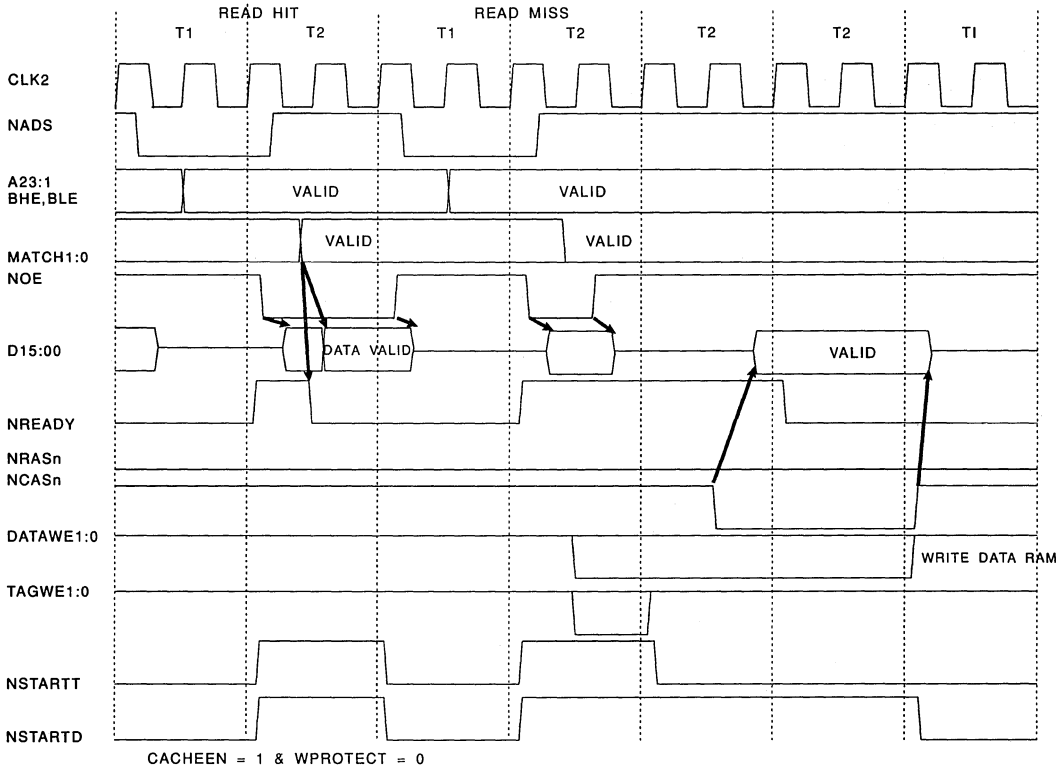


FIGURE 12-63. READ HIT/READ MISS CYCLE

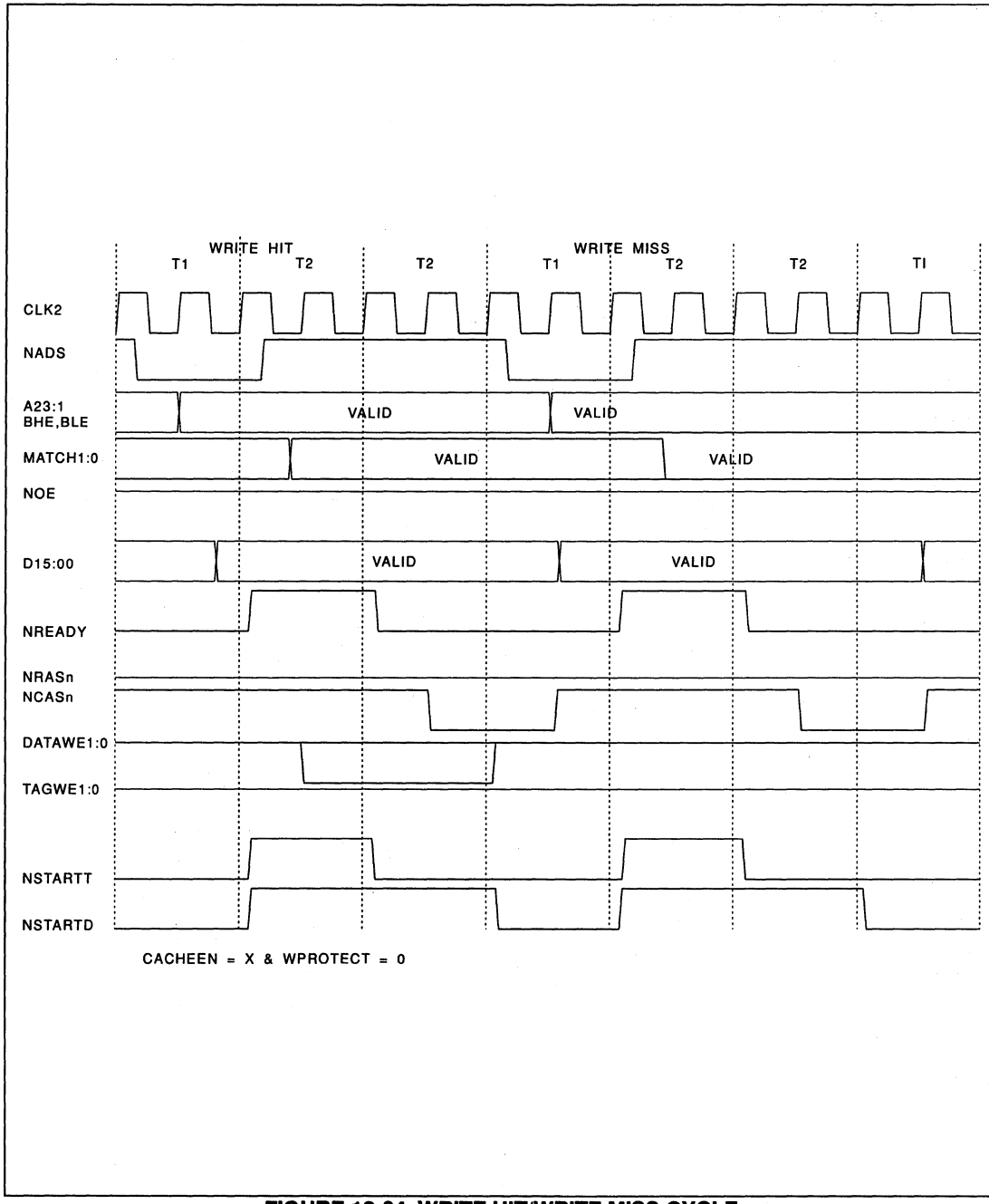


FIGURE 12-64. WRITE HIT/WRITE MISS CYCLE

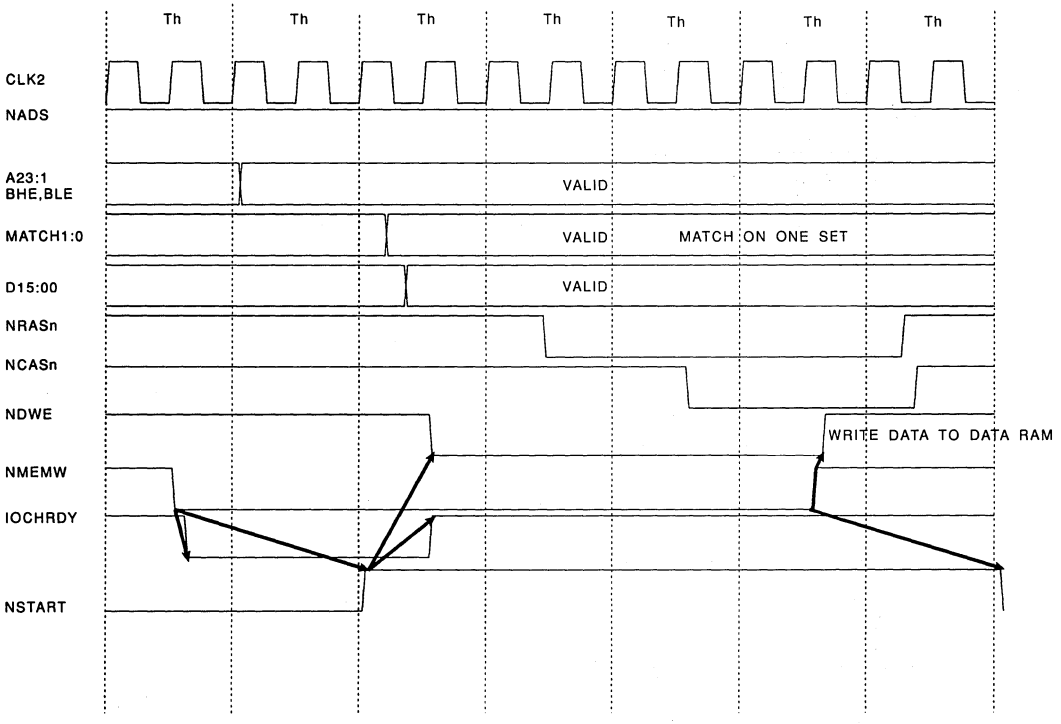


FIGURE 12-65. DMA/MASTERMEMORY WRITE HIT CYCLE

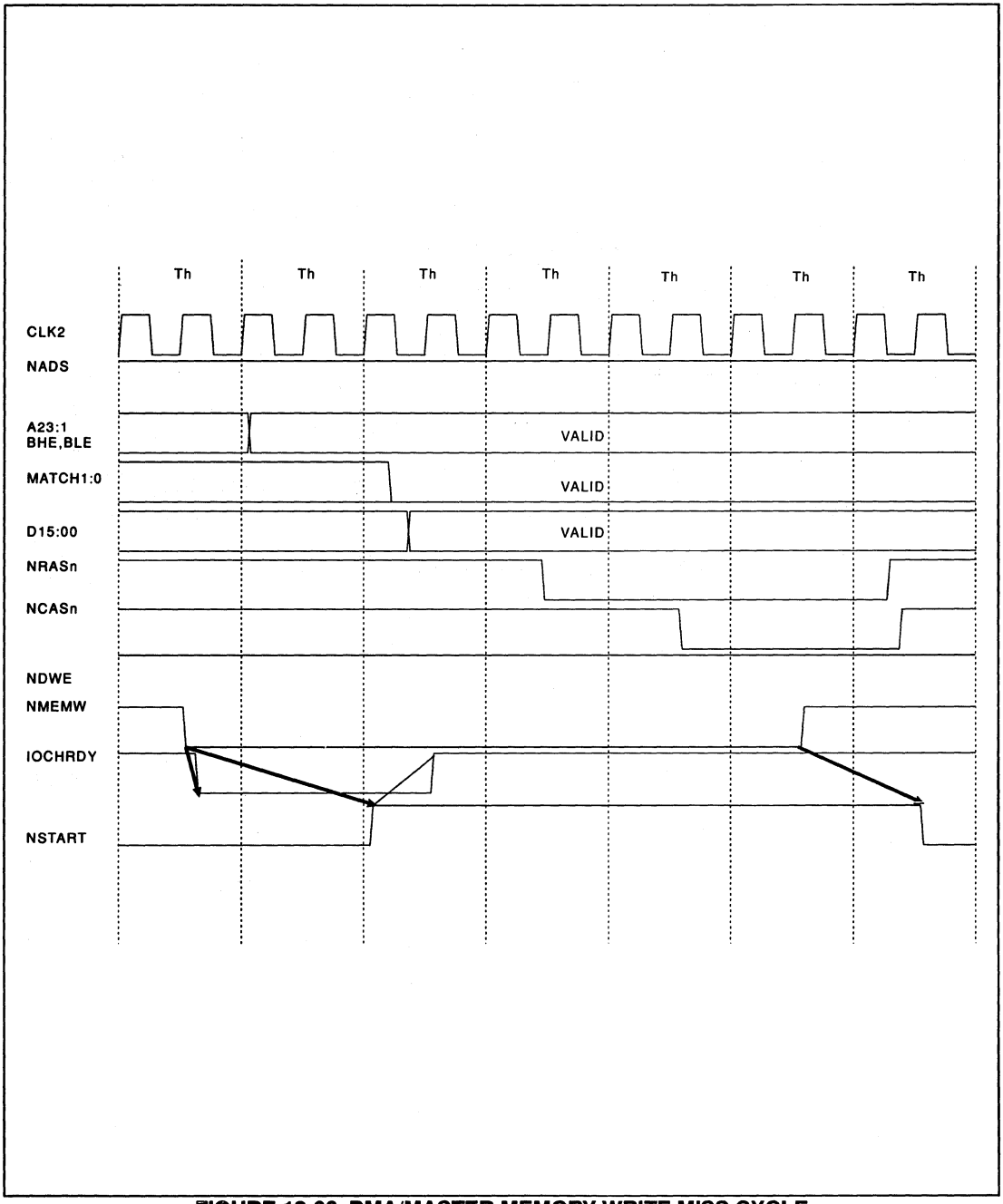


FIGURE 12-66. DMA/MASTER MEMORY WRITE MISS CYCLE

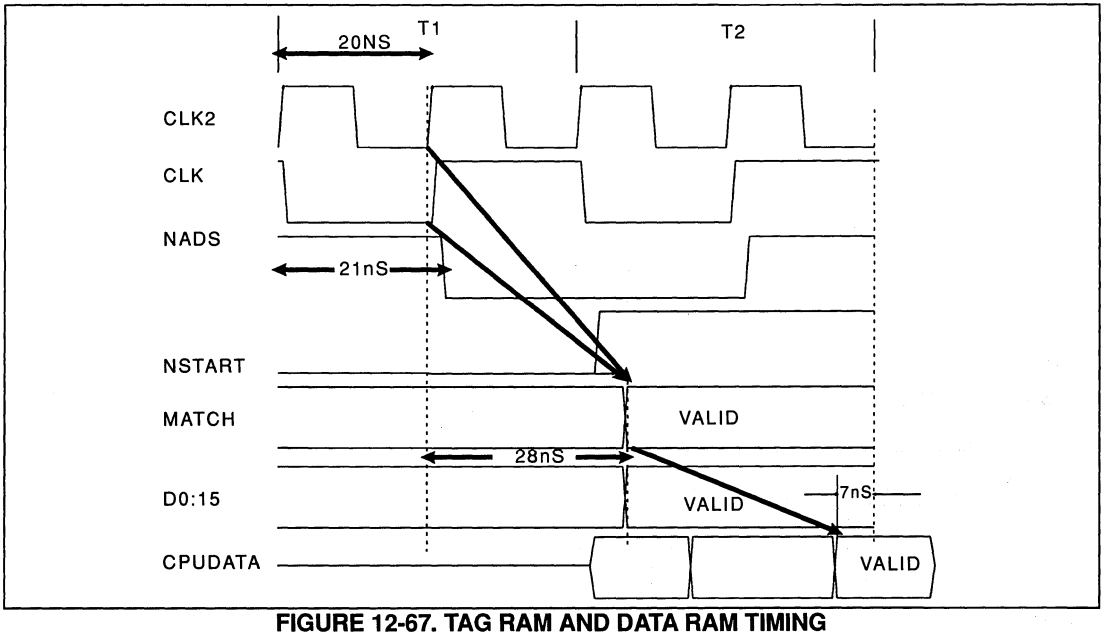


FIGURE 12-67. TAG RAM AND DATA RAM TIMING

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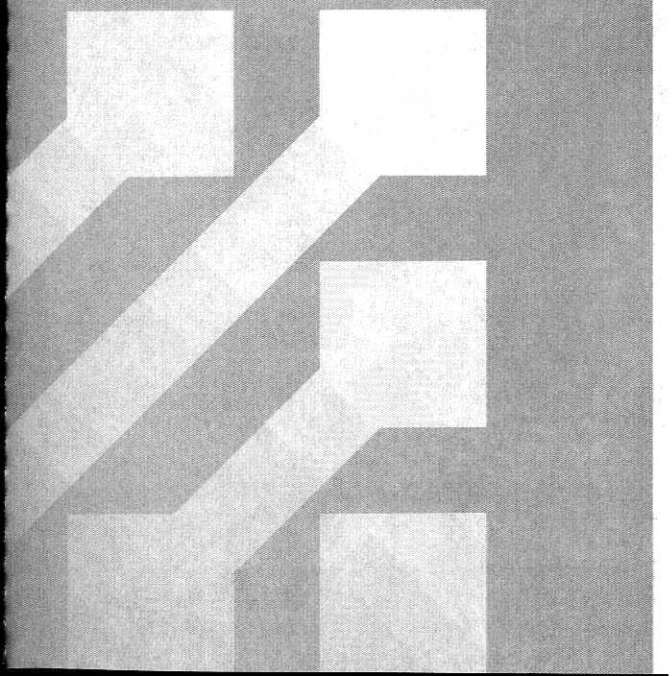
WD7910/LP

ISA-Based System Controller

with Cache for 80386SX and 80286

Desktop and Portable Compatibles



WESTERN DIGITAL

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8

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The WD7910 is the second generation single chip AT solution based on the WD76C10A core. It is fabricated in 0.9 micron CMOS. The WD7910 provides 8 Kbytes of direct-mapped or two-way set associative lookaside caching, a page-interleaved memory controller, and enhanced power management features. Figure 1-1 shows the block diagram of the WD7910-based system.

The standard version of the WD7910 operates from 5 VDC (±10%) supplies. An extended low-power version, the WD7910LP, can operate with 3.3 VDC (±0.3V) or 5 VDC (±0.5V).

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD7910 and WD7910LP System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD7910 and WD7910LP operate similarly and are referred to in this document as the System Controller. Where there are differences, the devices are identified specifically.

1.2 FEATURES

- Software compatible with WD76C10A
- 8Kbyte on-chip cache for 80386SX
  - Direct map or 2 way set-associative
  - Self timed Integrated RAM arrays
  - Programmable non-cacheable regions
  - Diagnostic mode to test Tag and Data Ram
  - Flush command
  - 25 Mhz zero wait state cache hit
- ROM may be shadowed and/or cached
- Supports Static CPU for power savings in sleep mode
- Supports extra wait state for page mode
- Supports VLBI for high-speed video access
- Operates at speeds of 16 MHz, 20 MHz and 25 MHz.
- Interfaces with 80286, or 80386SX CPUs.
- Supports memory in four banks with 64 Kbits, 256 Kbits, 1 Mbits or 4 Mbits DRAMs. Also supports new 512k x 8, 1M x 16 and 2M x 8 DRAM configurations.
- Page mode zero wait state access at 25 MHz with 70 ns DRAM.
- Supports up to 16 Mbyte of real memory, or 32 Mbyte of EMS memory.
- Maintains controlled propagation delay for 80386SX reset.
- Employs an internal self-tuning delay line for DRAM control.
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise.
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and VGA BIOS may be mapped into one physical PROM.
- Advanced 64 Kbyte and 128 Kbyte ROM shadowing allows main BIOS and video BIOS shadowing along with 320 Kbyte and 256 Kbyte remap to extended or expanded memory.
- Offers additional power saving modes:
  - Slow Refresh
  - Stop DMA Clock
- Parity generation and checking.
- 160-pin PQFP package
- 3.3V low power operation
- I/O Pin mapping for testability
- Low power 0.9 micron CMOS technology.

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Additional features of WD7910LP only:

- Supports System Management Interrupt (SMI)
- Provides I/O trapping
- Provides System Activity Monitor (SAM).
- Provides power control with suspend and resume.
- Provides processor stop clock.
- Features CAS before RAS slow refresh for portable applications.
- Offers automatic processor clock speed switching.
- 3V Suspend to hard disk

1.3 GENERAL DESCRIPTION

The WD7910 is designed for use in a high performance desktop AT computer using an 80286 or 80386SX processor up to 25 MHz. The WD7910LP has the features of the WD7910 and is designed to operate in a high-performance notebook/laptop AT compatible computer using an 80286 or 80386SX processor.

1.3.1 WD7910

The WD7910 contains a high performance memory controller with programmable modes of operation. It supports non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, 1 Mbit, 4 Mbit or 16 Mbit DRAM may be controlled, allowing up to 16 Mbytes of real or 32 Mbytes EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used. In addition, the WD7910 controls page mode DRAM or static column DRAM with page mode operation.

The on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line information is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

The WD7910 interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power-up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.2 WD7910LP

In addition to supporting all the features of the WD7910, the WD7910LP also supports portable notebook/laptop computers. To provide this support, the WD7910LP makes use of Power Management Control (PMC) for powering down peripherals or the processor, which includes processor stop clock, slow clock, automatic processor clock speed switching modes and CAS before RAS slow refresh. Suspend and resume is supported when low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 5 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

The System Activity Monitor (SAM) provided by WD7910LP is a transparent feature that replaces the functions previously performed by software. It determines when the system has been idle for a previously programmed period of time and determines a clean break point in which to perform powerdown activities such as suspend.

The WD7910LP also supports System Management Interrupt (SMI) with complete I/O trapping of up to six separate I/O ranges.

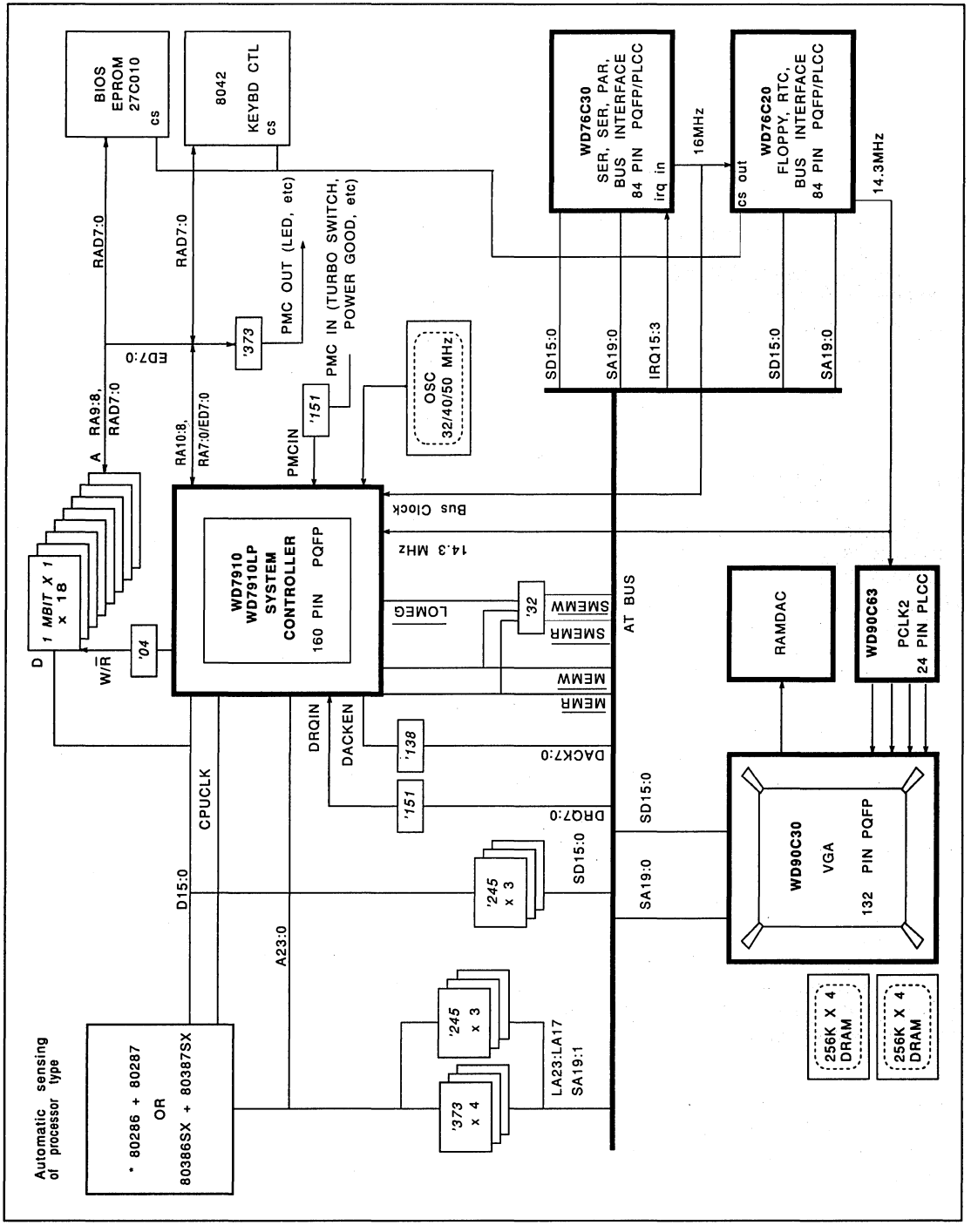

FIGURE 1-1. SYSTEM BLOCK DIAGRAM FOR DESKTOP

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control (WD7910LP only)
- Register File
- Video Local Bus Interface (VLBI) control
- Cache control

Sections 2.1 through 2.10 provide an overview of these blocks and are described in more detail in sections 4 through 11.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal, which it uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal. It is at this time that the type of processor in use (80286, 80287 or 80386SX, 80387SX) is determined by examining the S1[W/R#] signal.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the S1[W/R#] signal. This block also controls whether the CPUCLK is to be an input or output. While both devices have the ability to reduce the processor clock rate, only the WD7910LP has the ability to stop the clock to the processor. The WD7910LP also has the ability to power down the processor, at which time it tristates the CPUCLK, READY, HOLD, INTRQ and NMI signals.

2.4 NUMERIC PROCESSOR CONTROL

Both System Controllers support an 80287 or 80387SX processor.

2.5 DATA BUS

The Data Bus is a 16-bit (two bytes) bidirectional bus that connects to the processor's, System Controller, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory. Both versions of the System Controller supports non-page mode memory and independent two-way interleave page mode access to the DRAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD7910LP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD7910LP tristates the CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI output signals to the main processor. Also contained within this functional block are the SMI and SAM logic.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port 1872H, serve more than one area. In this instance the register description appears only in one section but is referred to in all appropriate sections.

The registers, and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072H and E872H and Port 70H Shadow Register at E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72H - Read only

Bits 11 through 03 are particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
T	Not Used			DMA #2			
				CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1				P4	Not Used		
CH3	CH2	CH1	CH0				

Signal Name — **Default At RSTIN**

All signals . . . . . None

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bit 03 - P, Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, section 4.3

Bits 02-00 - Not used, state is ignored

2.8.2 Lock/Unlock Register

Port Address F073H - Write only

15	14	13	12	11	10	09	08
Not Used							

07	06	-5	04	03	02	01	00
L/UL = DA-							

Signal Name	Default At RSTIN
All signals	None

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -
11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -
Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

2.9 VLBI Control

The Video Local Bus Interface (VLBI) control is internal logic which interfaces with the WD90C56 VLBI controller. It has the ability to determine whether the current CPU cycle should be processed by the WD90C56 or the WD7910LP.

2.10 Cache Control

This functional block contains the 8Kbyte integrated cache (both tag and data RAM) as well as cache control logic.

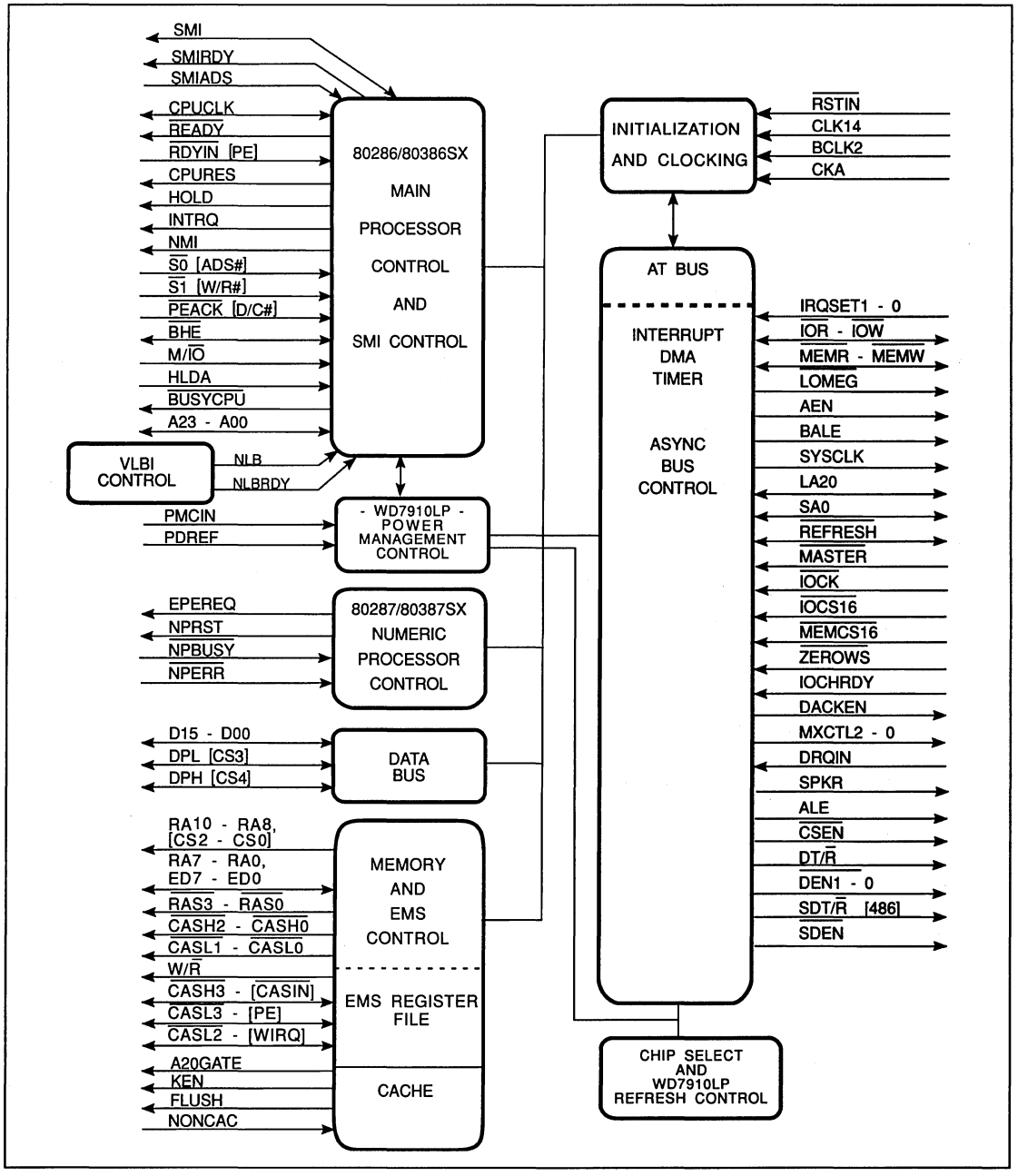

FIGURE 2-1. WD7910 AND WD7910LP BLOCK DIAGRAM

8

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	8.5, Table 8-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real-Time Clock Address Register	No	5.8.1
071 - 07F odd	Real-Time Clock Data Register	No	5.8.2
080 - 09F	(except 092H) DMA Page Registers	No	5.6.4
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	Clear 287 Busy	No	5.3.2
00F1	Reset 287/387SX	No	5.3.3
1072	CPU Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	8.1
2872	Chip Selects	Yes	8.2
3072	Programmable Chip Select Address	Yes	8.3
3872	Memory Control	Yes	6.2.1
3C72	DMA Shadow Register 1	Yes	9.14
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4472	DMA Shadow Register 2	Yes	9.14
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
4C72	DMA Shadow Register 3	Yes	9.14
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
5C72	Programmable CS2 and CS3 Control Register	Yes	10.11
6072	RAM Shadow And Write Protect	Yes	6.2.4
6472	Programmable CS2 Address Register	Yes	10.11
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
6C72	Programmable CS3 Address Register	Yes	10.13
7072	PMC Output Control 7:0	Yes	9.3
7472	DRAM Size and SMI RAM Register	Yes	10.14
7872	PMC Output Control 15:8	Yes	9.3
7C72	SMI I/O Trap Control Register	Yes	10.2
8072	PMC Timers	Yes	9.4
8872	PMC Inputs 7:0	Yes	9.5
8C72	I/O Data/Memory Address Capture Register Low	Yes	10.4
9072	NMI Status	Yes	9.7
9472	I/O Data/Memory Address Capture Register High	Yes	10.7
9872	Diagnostic	Yes	11.1
9C72	SMI I/O Timeout Control Register	Yes	10.5
A072	Delay Line	Yes	11.2

TABLE 2-1. REGISTER INDEX

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
A472	SMI I/O Timeout Count Register 1	Yes	10.8
A872	Test Enable	Yes	11.3
AC72	SMI I/O Timeout Count Register 2	Yes	10.9
B072	Activity Monitor Control	Yes	9.11
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	9.6
D072	Serial/Parallel Shadow Register	Yes	9.8
D472	Interrupt Controller Shadow	Yes	9.9
D872	Activity Monitor Mask	Yes	9.12
DC72	Test Status	Yes	11.4
E072	EMS Page Register Pointer	No	6.4.2
E472	Port 70H Shadow	No	9.10
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	8.5, Table 8-1
F472	48 MHz Oscillator Enable	Yes	8.5, Table 8-1
F872	Cache Flush	Yes	8.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	No	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

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TABLE 2-1. REGISTER INDEX (cont.)

3.0 SIGNAL DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	CLK14	41	PDREF	81	DRQIN	121	CLKA
2	NPBUSY	42	PMCIN	82	IOCHRDY	122	CPUCLK
3	BLE	43	WNRDRAM	83	ZEROWS	123	BUSYCPU
4	A1	44	CASH0	84	IOCS16	124	NMI
5	NC	45	NC	85	A20GATE	125	NA
6	A20	46	CASLO	86	MEMCS16	126	INTRQ
7	A19	47	RAS0	87	SPKR	127	D0
8	A18	48	CASH1	88	SA0	128	D1
9	A17	49	CASL1	89	LA20	129	D2
10	NC	50	NC	90	KEN	130	VSS
11	A16	51	RAS1	91	MASTER	131	D3
12	A15	52	RA10	92	ALE	132	D4
13	A14	53	RA9	93	AEN	133	D5
14	A13	54	RA8	94	SDEN	134	D6
15	NC	55	NC	95	LBRDY	135	VSS
16	A12	56	VSS	96	SDTR	136	D7
17	A11	57	RA7	97	VCC	137	D8
18	VSS	58	RA6	98	REFRESH	138	D9
19	VSS	59	VSS	99	VSS	139	D10
20	RA11	60	NC	100	LB	140	NC
21	A10	61	RA5	101	EPEREQ	141	VSS
22	VCC	62	VCC	102	PRST	142	D11
23	A9	63	RA4	103	LOMEG	143	VCC
24	A8	64	RA3	104	MEMW	144	D12
25	NONCAC	65	NC	105	SMI	145	NC
26	A7	66	VSS	106	MEMR	146	D13
27	A6	67	RA2	107	IOW	147	D14
28	A5	68	RA1	108	IOR	148	D15
29	A4	69	RA0	109	BHE	149	DTR
30	FLUSH	70	NC	110	SMIRDY	150	VSS
31	A3	71	CASH2	111	NPERR	151	DEN1
32	A2	72	CASL2	112	DNC	152	DEN0
33	IRQSET1	73	RAS2	113	MIO	153	SYSCLK
34	IRQSET0	74	CASH3	114	ADS	154	CPURES
35	MXCTLO	75	CASL3	115	SMIADS	155	BALE
36	NC	76	NC	116	WNR	156	NC
37	MXCTL1	77	RAS3	117	READY	157	A23
38	MXCTL2	78	DPH	118	HLDA	158	A22
39	CSEN	79	DPL	119	HOLD	159	A21
40	DACKEN	80	RSTIN	120	BCLK2	160	IOCK

TABLE 3-1. PIN ASSIGNMENTS

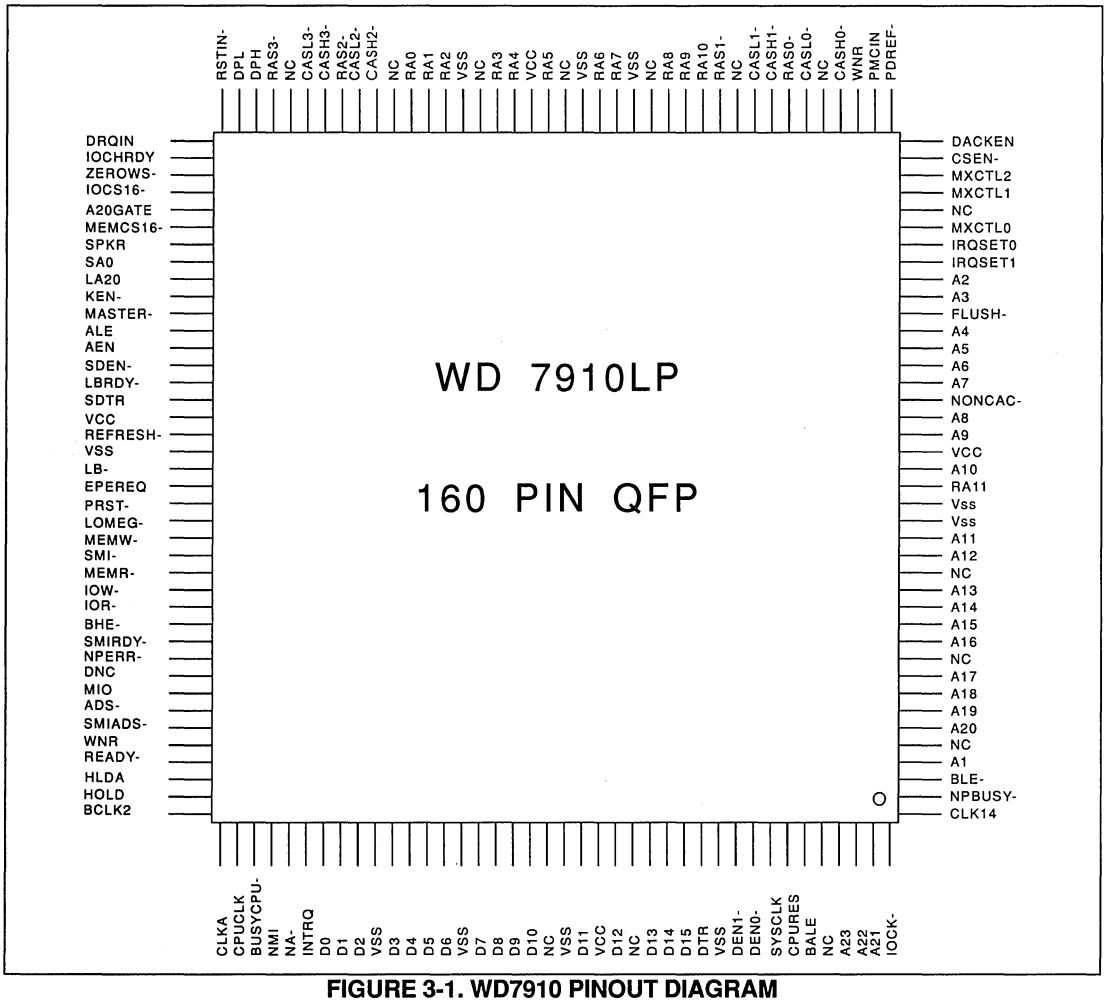

FIGURE 3-1. WD7910 PINOUT DIAGRAM

8

PIN	MNEMONIC	I/O	DESCRIPTION
			INITIALIZATION AND CLOCKING
1	CLK14	I	**Clock 14** CLK14 is derived from a 14.318 MHz crystal and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
80	$\overline{\text{RSTIN}}$	I	**System Reset In** $\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at powerup. For a detailed description, see Section 4, Initialization and Clocking.
120	BCLK2	I	**Bus Clock** BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock.
121	CLKA	I	**Clock A** Source for CPU clock.
			AT BUS
33	IRQSET1	I	**Interrupt Request Set 1** IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
34	IRQSET0	I	**Interrupt Request Set 0** IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, $\overline{\text{RESCPU}}$, $\overline{\text{IRQ8}}$, IRQ9 - IRQ11, IRQ14 and IRQ15. Refer to Table 5-1 and Figure 5-1.
35, 37, 38	MXCTL2:0	O	**Multiplexer Control 2-0** MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0 and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and $\overline{\text{RESCPU}}$. Refer to Table 5-1 and Figure 5-1.
39	$\overline{\text{CSEN}}$	O	**Chip Select Enable** When $\overline{\text{CSEN}}$ is asserted, DPH, DPL, and RA10-RA8 are used to generate one of 28 different chip selects. Refer to Table 8-1.
40	DACKEN	O	**DACK Enable** When DACKEN is asserted, MXCTL2-0 are used to generate DACK7-5, 3-0 and BUS_RST. Refer to Table 5-1 and Figure 5-1.
81	DRQIN	I	**Multiplexed DRQ Inputs** DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1
82	IOCHRDY	I/O	**I/O Channel Ready** Indicates extra wait states are required for the AT bus cycles.

TABLE 3-2. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
83	$\overline{\text{ZEROWS}}$	I	**Zero Wait States** Indicates the current AT bus cycle can be finished in zero wait state.
84	$\overline{\text{IOCS16}}$	I	**16-Bit I/O Cycle** Inicates the I/O device on the AT bus is a 16-bit slave.
86	$\overline{\text{MEMCS16}}$	I	**16-Bit Memory Cycle** Indicates that the memory device on the AT bus is a 16-bit slave.
87	SPKR	O	**Speaker** SPKR drives the speaker transistor.
88	SA0	I/O	**System Address 0** When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line.When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.
89	LA20	I/O	**Early Address 20** When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
91	$\overline{\text{MASTER}}$	I	**Master** $\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to be selected as input signals.
92	ALE	O	**Address Latch Enable** ALE is used to clock the SA1 - SA19 address latches.
93	AEN	O	**Address Enable** AEN is asserted by the System Controller while performing DMA and Refresh cycles.
94	$\overline{\text{SDEN}}$	O	**Swap Data Enable** $\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.
96	SDT/$\overline{\text{R}}$	I/O	**Swap Data Transmit/Receive** SDT/$\overline{\text{R}}$ controls the direction of the buffer between the low byte and high byte of the AT bus. SDT/$\overline{\text{R}}$ is tristated by a 50K pullup resistor internal to the WD7910 when $\overline{\text{RSTIN}}$ at pin 80 is low. **SDT/$\overline{\text{R}}$ Mode - Output** When SDT/$\overline{\text{R}}$ is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{\text{R}}$ is low, it directs data from the high byte of the AT bus to the low byte. Forcing SDT/$\overline{\text{R}}$ high while $\overline{\text{RSTIN}}$ is low selects the SDT/$\overline{\text{R}}$ mode. Holding SDT/$\overline{\text{R}}$ high as $\overline{\text{RSTIN}}$ goes high maintains the SDT/$\overline{\text{R}}$ mode.

TABLE 3-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
98	REFRESH	I/O	**Refresh** As an output, REFRESH is asserted by the System Controller to refresh memory on the AT Bus. As an input, REFRESH is asserted by the Bus Master in conjunction with MEMR to refresh memory on the AT Bus and DRAM controlled by the System Controller.
103	LOMEG	O	**First Megabyte** LOMEG is asserted when the AT bus address is below 1 Mbyte.
104	MEMW	I/O	**Memory Write** MEMW is an output and it is asserted by the System Controller when a memory write access to the AT bus is to take place. It is an input during Master mode.
106	MEMR	I/O	**Memory Read** MEMR is an output and it is asserted by the System Controller when a memory read access to the AT bus is to take place. It is an input during Master mode.
107	IOW	I/O	**I/O Write** IOW is an output and it is asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. IOW is an input during Master Mode.
108	IOR	I/O	**I/O Read** IOR is an output and iit s asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. IOR is an input during Master Mode.
149	DT/R	O	**Data Transmit/Receive** DT/R controls the direction of the AT Data Bus D00 through D15. When DT/R is high, data is directed to the AT Bus. When DT/R is low, data is transferred from the AT bus.
151	DEN1	O	**Data Bus Enable 1** When asserted, DEN1 enables the high order byte data buffer.
152	DEN0	O	**Data Bus Enable 0** When asserted, DEN0 enables the low order byte data buffer.
153	SYSCLK	O	**System Clock** In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
155	BALE	O	**AT Bus Address Latch Enable** Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
160	$\overline{\text{IOCK}}$	I	**I/O Channel Check** When asserted, $\overline{\text{IOCK}}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
			MAIN PROCESSOR CONTROL
95	LBRDY	I	**Local Bus Ready** Local bus cycle ready signal
100	$\overline{\text{LB}}$	I	**Local Bus** Local bus cycle request signal
105	$\overline{\text{SMI}}$	I/O	**SMI Request** SMI request to the processor.
109	$\overline{\text{BHE}}$	I/O	**Bus High Enable** As an input, $\overline{\text{BHE}}$ indicates a transfer of the high byte on the processor data bus. $\overline{\text{BHE}}$ is an output during DMA transfers.
110	$\overline{\text{SMIRDY}}$	O	**SMI Ready** SMI Ready signal to the processor
112	DNC	I	Processor DNC signal.
113	M/IO	I	**Memory or I/O** Processor Memory cycle or $\overline{\text{I/O}}$ Status cycle.
114	$\overline{\text{ADS}}$	I	$\overline{\text{ADS}}$ signal from the processor.
115	$\overline{\text{SMIADS}}$	I	**SMI Address** $\overline{\text{SMIADS}}$ signal from the processor.
116	W/$\overline{\text{NR}}$	I	When W/$\overline{\text{NR}}$ is high, a write to memory occurs; when low, a read from memory occurs.
117	$\overline{\text{READY}}$	O	**Processor Ready** $\overline{\text{READY}}$ is an output to the processor
118	HLDA	I	**Hold Acknowledge** Processor hold acknowledge.
119	HOLD	O	**Hold Request** Processor hold cycle request.
122	CPUCLK	I/O	**Processor Clock** CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at Port Address 1072H. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

8

PIN	MNEMONIC	I/O	DESCRIPTION
124	NMI	O	**Non-maskable Interrupt** Processor non-maskable interrupt cycle request.
125	$\overline{NA}$	O	**Next Address** Next address request to the processor.
126	INTRQ	O	**Interrupt Request** Processor interrupt cycle request.
154	CPURES	O	**Main Processor Reset** CPURES is a synchronous processor reset signal.
157-159, 6-9, 11-14, 16, 17, 21, 23, 24, 26-29, 31, 32, 4, 3	A23:1, $\overline{BLE}$	I/O	**Processor Address A23-A00[$\overline{BLE}$]** A23 through A1 are address lines from the 80286 or 80386SX.
NUMERIC PROCESSOR CONTROL			
2	$\overline{NPBUSY}$	I	**Numeric Processor Busy** Busy signal from the numeric processor 80287 or 80387SX.
101	EPERQ	O	**Extend PERQ** PERQ extend signal to the 80386SX for IRQ13 handling. Used only for the 80386SX.
102	NPRST	O	**Numeric Processor Reset** Reset to the numeric processor 80287 or 80387SX.
111	$\overline{NPERR}$	I	**Numeric Processor Error** Error signal from the numeric processor 80287 or 80387SX.
123	$\overline{BUSYCPU}$	O	**Coprocessor Busy** Coprocessor Busy signal to the processor.
DATA BUS			
78	DPH[CS4]	I/O	**Data Parity High Byte [Chip Select 4]** For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.
79	DPL[CS3]	I/O	**Data Parity Low Byte [Chip Select 3]** For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
148-146, 144, 142, 139-136, 134-131, 129-127	D15-D13 D12, D11, D10-D7 D6-D3 D2-D0	I/O	**Data Bits 15 through 0** The Data Bits are connected directly to the Local and Numeric processors, DRAM data and AT Bus data transceivers.
			MEMORY AND EMS CONTROL
25	$\overline{\text{NONCAC}}$	I	**Noncacheable** External noncacheable signal.
30	$\overline{\text{FLUSH}}$	O	**Flush** Flush signal to external cache controller.
43	NWR	O	**Write Not Read** Write Not Read signal to DRAM.
20 52 53 54	RA11 RA10/CS2 RA9/CS1 RA8/CS0	O	**DRAM Address Bits 11 through 8** **Chip Select Bits 2 through 0** The DRAM Address Bus is multi-functional. During DRAM cycles, RA11 through RA0 select the DRAM row and column.
57 58 61 63 64 67 68 69	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	I/O	**DRAM Address Bits 7 through 0** **EDATA Bits 7 through 0** During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.
77 73 51 47	$\overline{\text{RAS3}}$ thru $\overline{\text{RAS0}}$	O	**Row Address Select Bits 3 through 0** $\overline{\text{RAS3}}$ through $\overline{\text{RAS0}}$ are designed to access the DRAM without the use of external drivers.
74	$\overline{\text{CASH3}}$ [CASIN]	I/O	$\overline{\text{CASH3}}$ [CASIN] is tristated by a 50K pullup resistor internal to the WD76C10A when $\overline{\text{RSTIN}}$ at pin 17 is low.
71 48 44	$\overline{\text{CASH2}}$ $\overline{\text{CASH1}}$ $\overline{\text{CASH0}}$	O O O	**CAS Output Mode** $\overline{\text{CASH3}}$ through $\overline{\text{CASH0}}$ operate as output signals and are designed to accessthe DRAM without the use of external drivers. Forcing CASH3[CASIN] high while RSTIN is low, selects the CASH3 Output Mode. Holding CASH3[CASIN] high as RSTIN goes high, maintains the CASH3 Output Mode.
75 72 49 46	$\overline{\text{CASL3}}$ thru $\overline{\text{CASL0}}$	O	**Column Address Select Low 3 through 0** $\overline{\text{CASL3}}$ through $\overline{\text{CASL0}}$ are designed to access the DRAM without the use of external drivers.
85	A20GATE	O	**A20 Gate** A20 Gate signal to external cache controller

TABL 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
90	$\overline{\text{KEN}}$	O	**Cache Enable** Noncacheable signal to external cache controller.
			POWER MANAGEMENT CONTROL
41	NPDREF	I	**Power-down Refresh** NPDREF is a 64 KHz signal from the WD7910. During power-down, NPDREF is passed internally to pin 98 ($\overline{\text{REFRESH}}$).
42	PMCIN	I	**Power Management Control Input** PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
			MISCELLANEOUS
18, 19, 56, 59, 66, 99, 141	VSS	I	**Ground**
22, 62, 97, 143	VCC	I	**+5 Volts**

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, NRSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor. At this time the System Controller also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which are decoded externally as BUS_RST (DACK4), see sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the System Controller enters the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD7910 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds higher than 50 MHz, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872H. The PMC control output 0 tristates the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by SCHH or SCH (CPU Clock Control Register - bits 01 or 00, at Port Address 1072H) or divided down by CLK_SPD (bits 14-12). Only the WD7910LP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle. The other method can be used when the CPUCLK is an

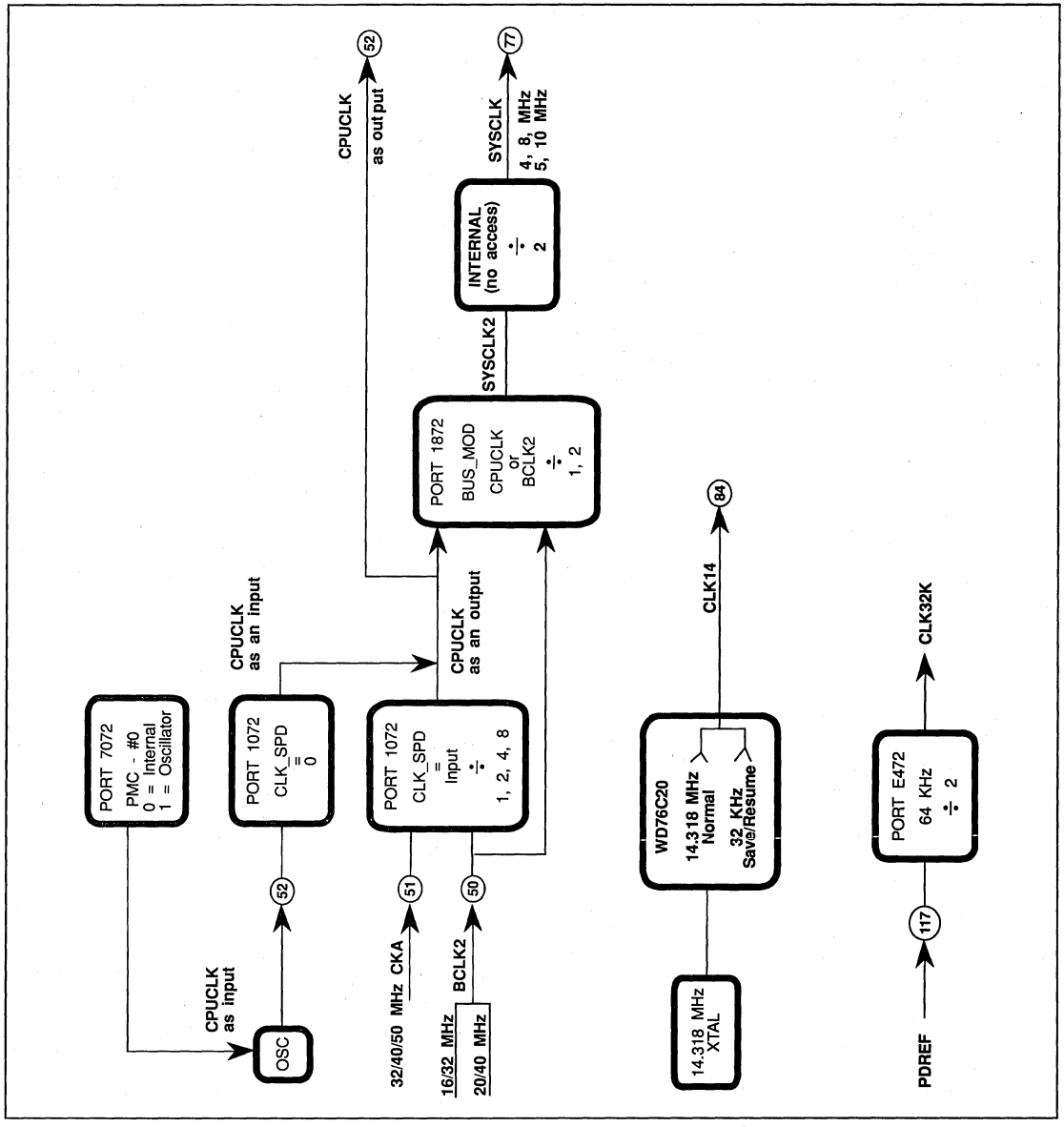

FIGURE 4-1. CLOCK CONTROL

output or input and generated by an external oscillator. In this case, EXT_HOLD is used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is determined by SRC (CPU Clock Control Register bit 15 at Port Address 1072H). SRC is set automatically at power up reset, if a clock source is present at pin 51 (CKA).

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072H - Read and Write

15	14	13	12	11	10	09	08
SRC	CLK_SPD			AUT_ FST	ALT_CLK_SPD		

07	06	05	04	03	02	01	00
EXT_HOLD						SCHH	SCH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	000/001
AUT FST †	0
ALT CLK SPD †	000
EXTEND HOLD	0000
Bits 03, 02	None
SCH †	0
SCHH †	0

† Featured only in the WD7910LP

Bit 15 - SRC, CPUCLK Clock Source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

Default Value

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted, or when operating in the 80486 Mode. The 80486 Mode is selected by holding SDT/$\overline{\text{R}}$ low during $\overline{\text{RSTIN}}$ transition from low to high.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK Clock Speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD *defaults to 000 or 001 at power up. Changing the CPUCLK from an input (CLK_SPD = 000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One millesecond later, CPUCLK becomes active as an output. One millesecond and 16 CPUCLK clocks (or one millesecond) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated due to the clock driver not being able to synchronously switch the clock. The one millesecond and 16 clocks or one millesecond selection is made through the Diagnostic Register at Port 9872H.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source (* Default value).
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (* Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

* Based upon the value of CLOCK_DIR_IN at power up (refer to Table 5-1, Figure 5-1 and section 5.1.2).

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Bit 11 - AUT_FST, Automatic Processor Clock Speed Switching
Featured only in the WD7910LP

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-2. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-2 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-1 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-1. The EXT_HOLD field must be 0000 when AUT_FST = 1.

TURBO	AUTO_FST	CPU CLOCK SPEED
0	0	CLK_SPD
0	1	CLK_SPD
1	0	ALT_CLK_SPD
1	1	CLK_SPD or ALT_CLK_SPD

TABLE 4-1. CLOCK SWITCH SELECTION

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access or processor reset	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-2. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate Clock Speed
Featured only in the WD76C10ALP

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value).

0 0 1 - Equals source.

0 1 0 - Equals source div by 2.

0 1 1 - Equals source div by 4, 25% duty cycle.

1 0 0 - Equals source div by 4, 75% duty cycle.

1 0 1 - Equals source div by 8, 12% duty cycle.

1 1 0 - Equals source div by 8, 88% duty cycle.

Bits 07-04 - EXT_HOLD, Extend Processor Hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external TURBO signal is asserted, EXT_HOLD is forced to 0000. When the external TURBO signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value).

0 0 0 1 - 1 µs hold after refresh.

0 0 1 0 - 2 µs hold after refresh.

0 0 1 1 - 3 µs hold after refresh.

0 1 0 0 - 4 µs hold after refresh.

↕

1 1 0 1 - 13 µs hold after refresh.

1 1 1 0 - 14 µs hold after refresh.

1 1 1 1 - 15 µs hold after refresh.

Bits 03-02 - Reserved for future use, must be set to zero

Bit 01 - SCHH, Stop CPUCLK at next Halt and Hold.
Featured only in the WD76C10ALP

SCHH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7910LP rather than an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate selected by the Refresh Control Register at Port 2072H.

SCHH = 0 -
Normal processor clock (default value).

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

Bit 00 - SCH, Stop CPUCLK at next Hold
Featured only in the WD7910LP

SCH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7910LP instead of an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate as selected by the Refresh Control Register at Port 2072H.

SCH = 0 -
Normal processor clock (Default value).

SCH = 1 -
Stop processor clock at next processor hold cycle.

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5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8) and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external 74F138, 3 to 8 Decoder for desktop systems, or 74ACT138, 3 to 8 Decoder for laptop systems, uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 74F151, 8 to 1 Multiplexer for desktop systems, or 74ACT151, 8 to 1 Multiplexer for laptop systems, to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1. This controls the default value of CLK_SPD in the CPU Clock (CPUCLK) Control Register at Port 1072H. See section 4.2.4.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA, DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{NRSTIN}$ to determine ROM data width (ROM8). The $\overline{RESCPU}$ and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus and Terminal Count (TC) Signal

The AT Address Bus SA19-00 and $\overline{NBLE}$ are generated from A19-00 with external latches and tristate buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and $\overline{CSEN}$ are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD7910, the $\overline{TURBO}$ signal may be connected directly to PMCIN. In the WD7910LP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{IRQ8}$	IRQ12	$\overline{TURBO}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	$\overline{RESCPU}$	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

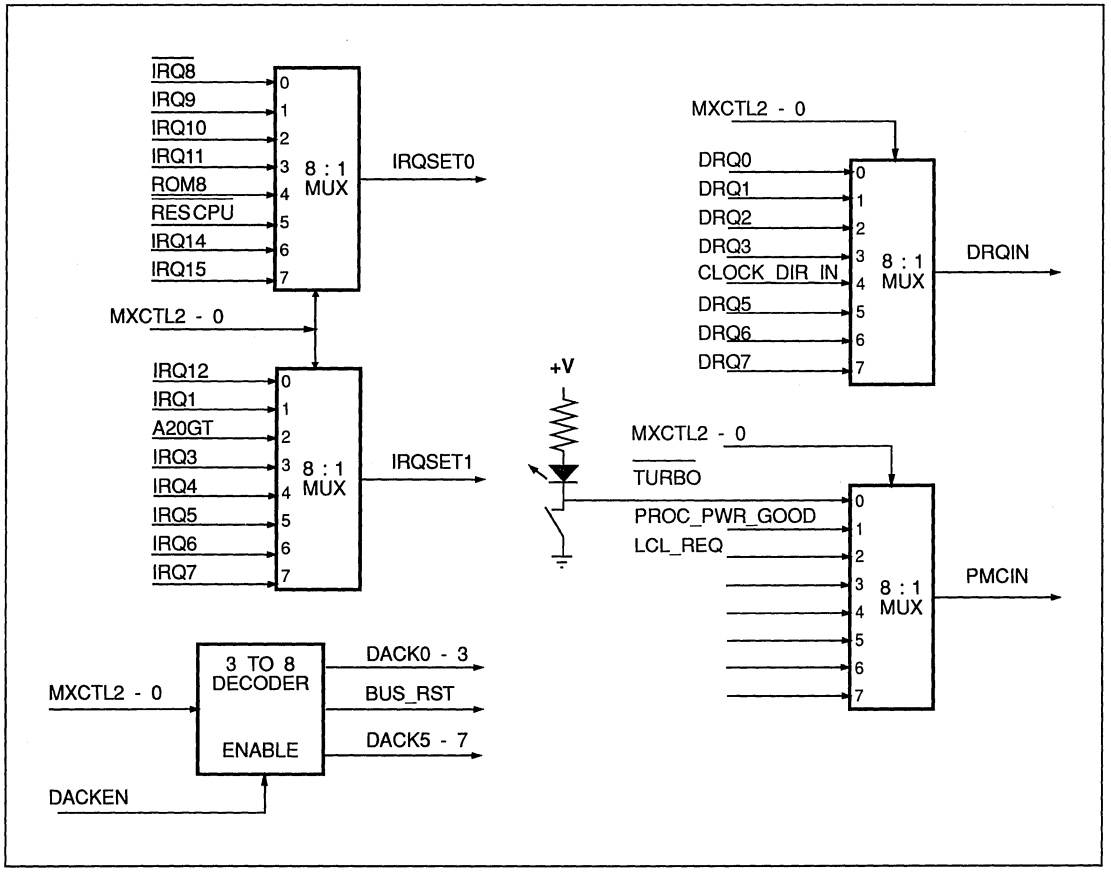

FIGURE 5-1. MXCTL2-0 MULTIPLEXING

5.3 NUMERIC PROCESSOR

5.3.1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872H - Read and Write

15	14	13	12	11	10	09	08
NP_ BSY	PRO_ PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI 16	WSM_ 16	WSI8		WSM8	

Signal Name	Default At NRSTIN
NP_BSY	0
PRO_PD †	0
Bit 12	None
FPD †	0
BUS_MOD	00
BRQ_DEL	00
BAK_DEL	11
WSI_16	0
WSM_16	0
WS18	10
WSM8	10

† Featured only in the WD7910LP

Bit 15 - NP_BSY, Numeric Processor Busy

NP_BSY must be set for systems using an 80286 CPU where the CPU runs faster than the AT bus. The causes $\overline{\text{BUSYCPU}}$ to be asserted early during any CPU write to I/O ports F8H through FFH. $\overline{\text{BUSYCPU}}$ is de-asserted at the end of the I/O write if the coprocessor has not asserted its own $\overline{\text{NPBUSY}}$ by this time. Early assertion of $\overline{\text{BUSYCPU}}$ is necessary to prevent a loss of synchronization between the 80286 and 80287. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Force an early $\overline{\text{BUSYCPU}}$ for I/O writes to coprocessor addresses F8H through FFH. (Default value).

NP_BSY = 1 -
Normal $\overline{\text{BUSYCPU}}$ assertion.

Bit 14 - PRO_PD, Processor Power Down
Featured only in the WD7910LP

When PRO_PD has been changed from zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated at the next Halt State and the expansion bus will continue to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD7910LP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power (Default value).

PRO_PD = 1 -
Start processor power down sequence.

Bit 13 - FPD, Full Powerdown
Featured only in the WD7910LP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except $\overline{\text{NRSTIN}}$, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Powerdown) from Port 7072H is set. This enables the powering down of all chips except DRAM, WD7910LP, WD76C20, WD76C30 and WD90C20. The WD76C20 provides NPDREF

(a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the NREFRESH signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at Port 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port 8872H input is high. The tristated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus Mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

- 0 0 - Bus logic uses BCLK2 divided by 2 (Default value).
- 0 1 - Bus logic uses BCLK2 divided by 1.
- 1 0 - Bus logic uses CPUCLK divided by 2.
- 1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

- 0 0 - 1 Bus clock delay (Default value).
- 0 1 - .5 Bus clock delay.
- 1 0 - No clock delay.
- 1 1 - Reserved.

Bits 07, 06 - BAK_DEL, Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

- 0 0 - No delay.
- 0 1 - -.5 Bus clock delay.
- 1 0 - -1 Bus clock delay.
- 1 1 - +.5 Bus clock delay (Default value)

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Bit 05 - WSI16, Wait State for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state (Default value).

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait State for 16 bit Memory

WSM16 = 0 -
1 Bus clock wait state (Default value).

WSM16 = 1 -
2 Bus clock wait state.

Bits 03, 02 - WSI8, Wait State for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

Bits 01, 00 - WSM8, Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

5.3.2 Numeric Processor Busy ($\overline{\text{NPBUSY}}$) Reset

Port Address 0F0H - Write only

Writing any data to this port resets the 80287 busy signal (de-asserts $\overline{\text{NPBUSY}}$). The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H - Write only

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	8 MHz	ASYNC	0X	01	01
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	00
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA Controller 1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA Controller 2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA Controller 2 is used to cascade DMA controller #1. Table 5-4 indentifies the Controller/-Channel location and function.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

Single Transfer Mode - 01

In single transfer mode, the channel makes one transfer for each request. The word count is decremented, and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the $\overline{MASTER}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or MEMW signals.

Write - 01

A write transfers data from an I/O device to memory.

Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the MEMW or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address Hex	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
080-09F			DMA Page Register
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008H, 0D0H - Write only

The Command Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
		EX_WR	RO_PRI	0	CO_DIS		

Signal Name	Default At RSTIN
All signals	0

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008H, 0D0H - Read only

Bits 3-0 are reset by $\overline{\text{NRSTIN}}$, writing any data to Port Address 00DH or 0DAH (see section 5.4.14) or when read by a Status Read Command.

7	6	5	4	3	2	1	0
CH3_DRQ	CH2_DRQ	CH1_DRQ	CH0_DRQ	CH3_TC	CH2_TC	CH1_TC	CH0 TC

Signal Name	Default At RSTIN
CH3_DRQ - CH0_DRQ	None
CH3_TC - CH0_TC	0

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009H, 0D2H - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by $\overline{\text{RSTIN}}$ or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
					CRQ	CH#	

Signal Name	Default At RSTIN
All signals	0

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a $\overline{\text{RSTIN}}$, or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H - Write only

7	6	5	4	3	2	1	0
					SE_MA	CH#	

Signal Name	Default At RSTIN
All signals	1

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH - Write only

Writing any data to this register resets all Masks. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH - Write only

7	6	5	4	3	2	1	0
				CH3_MA	CH2_MA	CH1_MA	CH0_MA

Signal Name	Default At RSTIN
All signals	1

Bits 7-4 - Not used, state is ignored

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00BH, 0D6H - Write only

This register selects the mode and type of transfer for each channel. Refer to sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_MOD		AD_DEC	AUTO	TRA_TYP		CHA# SEL	

Signal Name	Default At RSTIN
All signals	None

Bits 7, 6 - TRA_MOD, Transfer Mode

TRA_MOD 7	6	
0	0	- Demand
0	1	- Single
1	0	- Block
1	1	- Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP 3	2	
0	0	- Verify
0	1	- Write
1	0	- Read
1	1	- Not used

Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H - Write only

Each DMA controller has a pointer flip-flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip-flop is reset, bits 7-0 are accessed, and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see section 5.4.14). In either case, the data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.14 Master Clear Rgister

Port Addresses 00DH, 0DAH - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.15 DMA Mode Shadow Register

Port Address B872H - Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt Controller 1 is in the I/O space of 020H to 021H and Interrupt Controller 2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of Interrupt Controller 1 is used to cascade Interrupt Controller 2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	RTC
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

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6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

Interrupt Controller	Address Hex	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Signal Name	Default At RSTIN
All signals	None

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1

Bit 3 - L_T, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bit 2 - I2 H_L, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

Port Addresses 0A1H - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H - Write only

A Slave does not have ICW4.

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Not Special Fully Nested Mode

S F N M = 1 -
Special Fully Nested Mode

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT 7	6	5	
0	0	0	- Clear Rotate On Automatic EOI
0	0	1	- Non-specific EOI
0	1	0	- Not used
0	1	1	- Specific EOI
1	0	0	- Set Rotate on Automatic EOI
1	0	1	- Rotate on Non-Specific EOI
1	1	0	- Set Priority
1	1	1	- Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV 2	1	0	
0	0	0	- Interrupt Level 0
	↕		
1	1	1	- Interrupt Level 7

5.5.3.3 OCW3

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ISR	

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM 6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 - No Poll Command

P_C = 1 - Poll Command

Bits 1-0 - IRR_ISR, Interrupt Request Register and Interrupt Service Register

IRR_ISR 1	0	
0	0	- Not used
0	1	- Not used
1	0	- Read Interrupt Request Register
1	1	- Read Interrupt Service Register

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5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040H	Timer 0 Count/Status	Read/Write
041H	Timer 1 Count/Status	Read/Write
042H	Timer 2 Count/Status	Read/Write
043H	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

Address 9	8	7	6	5	4	3	2	1	0	Decodes	Hex
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PIO)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real-Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real-Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092H)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087H	DMA Channel 0
0083H	DMA Channel 1
0081H	DMA Channel 2
0082H	DMA Channel 3
008BH	DMA Channel 5
0089H	DMA Channel 6
008AH	DMA Channel 7
008FH	Refresh

TABLE 5-9. PAGE REGISTER DECODES

NOTE

Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

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5.8 NMI AND REAL TIME CLOCK

5.8.1 Real Time Clock Address Register

Port Address 070H-07EH even - Write only

There is only one RTC Address Register. All even number addresses from 070H through 07EH access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
RTC6 - RTC0	None

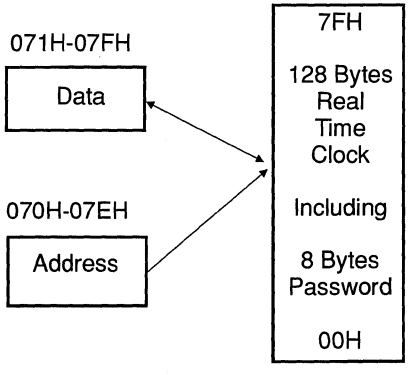
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real-Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real-Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071H-07FH.



5.8.2 Real-Time Clock Data Register

Port Address 071H-07FH odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071H through 07FH access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to section 7.2).

7	6	5	4	3	2	1	0
Real-Time Clock Data							

5.8.3 Lock Pass, Alternate A20G And Hot Reset

Port Address 092H - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
Bits 7-4, 2	None
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by NRSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

Bit 0 - HOT_RST, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Port Address 061H- 06FH odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

Odd numbered Port Addresses 061H through 06FH provide access to parity error and I/O Channel Check of the expansion bus.

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity Error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O Channel Check from the expansion bus (read only)

IOCK = 0 -
No I/O Channel Check Error

IOCK = 1 -
I/O Channel Check Error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O Channel Check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable Parity Error Check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by Port Address register 6072H, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled

Bit 1 - ENSPK, Enable Speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

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6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA11 through RA0. During I/O cycles, RA11 through RA08 (CS3-CS0)are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA11 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM, plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{NMEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128 Kbyte to 640 Kbyte, 256 Kbyte to 640 Kbyte and 512 Kbyte to 640 Kbyte.

When disabling any on-board DRAM, the register at Port Address 6872H must not be programmed to enable the on-board Lower EMS Page Frame.

The WD7910 and WD7910LP provide support for DRAM banks to be independent or two-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size.

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872H - Read and Write

15	14	13	12	11	10	09	08
PG_ CAS		CA		PG	ILV		

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS	0
CA	00
PG	0
ILV	00
SIZE_BNK3	00
SIZE_BNK2	00
SIZE_BNK1	00
SIZE_BNK0	00

Bit 15 - PG_CAS, Page Mode CAS Width

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks. This is required for 80386SX Pipeline mode.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache Mode

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the RDYIN signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the RDYIN (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)

0 1 - Cache Mode enabled.

1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the external memory controller.

1 1 - Pin 51 may be used as the alternate clock CKA. When CAS Input Mode is enabled, PE on pin 111 becomes an input and represents an error. (See pin 12 description in Table 3-2 on selecting CAS Mode.)

Bit 11 - PG, Page Mode

PG = 0 - Non-page mode (Default value)
Word interleaving is employed when bank interleaving is enabled by ILV. Non-page mode *is not supported* in 1Mbit x 16 chips and 2Mbits x 16 configurations.

PG = 1 - Page mode
Page mode interleaving is performed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In Non-page Mode (PG = 0), word interleaving is employed. In Page Mode (PG = 1), Page Mode interleaving is used. Four-way interleave is only supported in Page Mode when four banks are installed using one of the following DRAM configurations: 4 Mbits x 16; 512Kbits x 16; 1Mbit x 16 chips; or 2Mbits x 16. Interleave of 64 Kbits x 16 DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size and assigned the same starting address when they are interleaved together.

8

ILV 10 09 08

- 0 0 0 - No interleaving performed
- 0 0 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are not interleaved
  Banks 0 and 1 must be the same size
- 0 1 0 - Banks 0 and 1 are not interleaved
  Banks 2 and 3 are interleaved
- 0 1 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are interleaved
  (Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.)
- 1 0 0 - Page Mode four-way interleave (Banks 0, 1, 2 and 3 must have one of the following DRAM configurations installed: 4 Mbits x 16; 512 Kbits x 16; 2Mbits x 16; or 1 Mbit x 16 chips.)

DRAM Banks 3 through 0

The WD7910 and WD76910LP support all DRAM sizes. The DRAM sizes may be mixed. See section 10.14, DRAM Size and SMI RAM Register.

Bits 07, 06 - SIZE_BNK3, Size of Bank 3

PORT 7472	PORT 3872		BANK 3 SIZE
BIT 15	BIT 7	BIT 6	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 05, 04 - SIZE_BNK2, Size of Bank 2

PORT 7472	PORT 3872		BANK 2 SIZE
BIT 14	BIT 5	BIT 4	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 03, 02 - SIZE_BNK1, Size of Bank 1

PORT 7472	PORT 3872		BANK 1 SIZE
BIT 13	BIT 3	BIT 2	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 01, 00 - SIZE_BNK0, Size of Bank 0

PORT 7472	PORT 3872		BANK 0 SIZE
BIT 12	BIT 1	BIT 0	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 1 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 0 start address					

Port Address 5072H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 3 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 2 start address					

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes. For three banks of the same size, in which two are interleaved, the two interleaved banks must be placed at a lower starting address than the third bank.

RAM SIZE	PAGE SIZE	BANK SIZE
64Kbits x 16	512 Bytes	128 Kbytes
256 Kbits x 16	1024 Bytes	512 Kbytes
1 Mbits x 16	2048 Bytes	2048 Kbytes
4 Mbits x 16	4096 Bytes	8192 Kbytes
512 Kbits x 16	1024 Bytes	1024 Kbytes
1 Mbit x 16 chips	512 Bytes	2048 Kbytes
2 Mbits x 16	1024 Bytes	4096 Kbytes

6.2.3 Split Starting Address

Port Address 5872H - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At RSTIN
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	00
SPLIT_SIZE	00
Bits 01, 00	None

Bit 15 - EN_BK3, Enable Bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value)

EN_BK3 = 1 -
Bank 3 is enabled

Bit 14 - EN_BK2, Enable Bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value)

EN_BK2 = 1 -
Bank 2 is enabled

Bit 13 - EN_BK1, Enable Bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value)

EN_BK1 = 1 -
Bank 1 is enabled

Bit 12 - EN_BK0, Enable Bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value)

EN_BK0 = 1 -
Bank 0 is enabled

Bits 11, 10 - DRAM_DRV, DRAM Driver Strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

DRAM_DRV

11 10

- 0 0 - Full strength DRAM address drive, up to 350 pF (Default value)
- 0 1 - Low strength DRAM address drive, up to 100 pF
- 1 0 - Medium strength DRAM address drive, up to 180 pF
- 1 1 - High strength DRAM address drive, up to 260 pF

Bits 09, 08 - SP SIZE, Split Size

The split is implemented by moving the block of memory between 0A0000H through 0FFFFFH to another area. The destination area must start on a 512 Kbyte boundary. If BIOS is to be shadowed, the split size must be 320 Kbyte for a 64 Kbyte shadow or 256 Kbyte for a 128 Kbyte shadow, and the RAM Shadow And Write Protect Register (Port 6072H) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000H (640 Kbyte) to 100000H (1024 Kbyte) is available for remapping. The remapping may start at 100000H, providing 384 Kbyte of extended memory, or may start at 0F0000H to allow BIOS shadowing, with 320 Kbyte of extended memory. Only a single bank may be split. The bank to be split must be at least 512 Kbyte or larger.

SPLIT SIZE

09 08

- 0 0 - No split (Default value)
- 0 1 - 256 Kbyte split, memory moved from 0A0000H to 0DFFFFH
- 1 0 - 320 Kbyte split, memory moved from 0A0000H to 0EFFFFH
- 1 1 - 384 Kbyte split, memory moved from 0A0000H to 0FFFFFH

Bits 07-02 - A24-A19, Split Starting Address

Bits 01, 00 - Not used, state is ignored

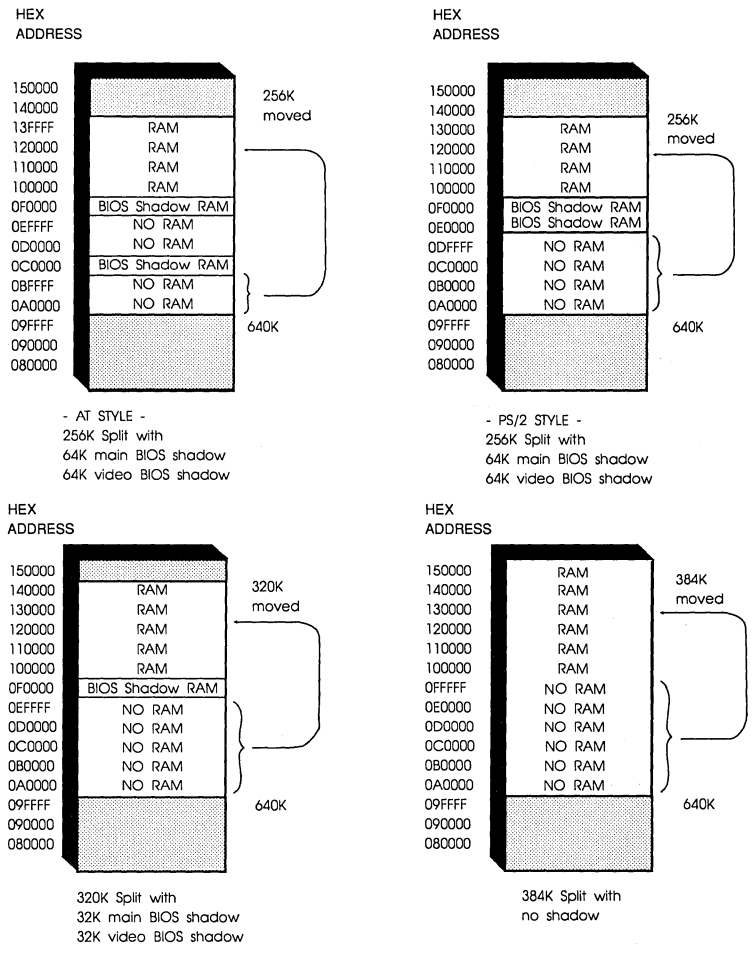

FIGURE 6-1. SPLIT SIZE

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6.2.4 RAM Shadow And Write Protect

Port Address 6072H - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
X_ MEM		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	00
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	00
X_MEM	0
Bit 06	None
VB_SIZ	00
ROM_TYP	00
BL_MOU †	00

† Featured only in the WD7910LP

Bit 15, 14 - DIS_MEM, Disable On-board Memory

DIS_MEM
15 14

0 0 - On-board memory from 128 KB to 640 KB not disabled (Default value).

0 1 - On-board memory from 512 KB to 640 KB disabled.

1 0 - On-board memory from 256 KB to 640 KB disabled.

1 1 - On-board memory from 128 KB to 640 KB disabled.

Bit 13 - HM_WP, High Memory Write Protect Enable

This bit enables the write protection for the memory boundary established by the register at Port C072H.

HM_WP = 0 -
High memory write protect not enabled (Default value).

HM_WP = 1 -
High memory write protect enabled.

Bit 12 - WP, Shadowed BIOS Write Protect Enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value).

WP = 1 -
Write protect for shadowed BIOS enabled.

Bit 11 - INV_PAR, Invert Parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value).

INV_PAR = 1 -
Invert parity when writing to on-board DRAM.

Bit 10 - PAR_DIS, Parity Checking Disabled

Parity checking is normally enabled or disabled by Port 061H. Setting PAR_DIS overrides the Port 061H setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by Port 061H (Default value).

PAR_DIS = 1 -
Parity checking disabled.

Bits 09, 08 - SHD, Shadow BIOS

Before the BIOS can be shadowed, the SPLIT_SIZE field in the Split Starting Address Register at Port 5872H must be programmed to non-zero.

ROM at FE0000H - FFFFFFH, the top of 16 MByte address space is never shadowed.

Option SHD 11 should be used when Video Remap Function is desired (i.e. Video BIOS in the lower half of EPROM shows up at C0000H).

64 Kbyte of system BIOS at 0F0000H - 0FFFFFH, and up to 64 Kbyte of video BIOS at 0C0000H - 0CFFFFH, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000H - 0FFFFFH. When SHD is set to 11, the video BIOS appears at 0C0000H - 0CFFFFH rather than 0E0000H - 0EFFFFH.

The video shadow size at 0C0000H - 0CFFFFH is determined by VB_SIZ, the video BIOS size field.

SHD
09 08

† 0 0 - No BIOS shadowing, allows 384 KB remap (Default value).

0 1 - 64 KB system BIOS shadow, 0F0000H - 0FFFFFH, allows 320 KB remap.

1 0 - 128 KB system BIOS shadow, 0E0000H - 0FFFFFH, allows 256 KB remap.

† 1 1 - 64 KB system BIOS shadow, 0F0000 - 0FFFFF and video BIOS shadow, allows 256 KB remap.

† See note following bits 01, 00.

Bit 07 - X_MEM, Shadow BIOS for Read/Write Memory

When SHD (bits 09 and 08) equals 11, X_MEM provides the means of using RAM from E8000H through EFFFFH not being used for video BIOS shadowing, to be used as read/write memory.

X_MEM = 0 - SHD = 11
ROM_TYP = 10 - VB_SIZ = 01

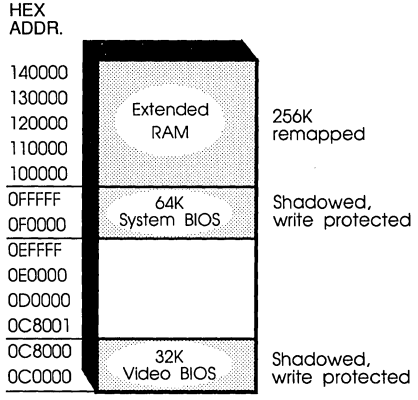

FIGURE 6-2. X_MEM = 0

X_MEM = 1 - SHD = 11
ROM_TYP = 10 - VB_SIZE = 01

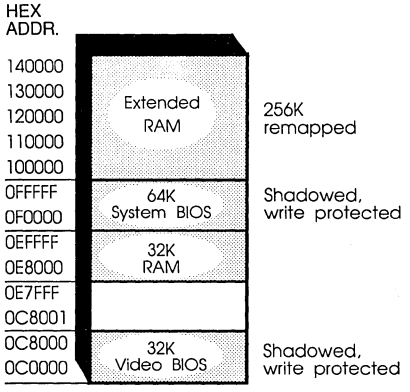

FIGURE 6-3. X_MEM = 1

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS Size

VB_SIZ †
05 04

0 0 - 16 KB video BIOS (Default value)

0 1 - 32 KB video BIOS

1 0 - 48 KB video BIOS

1 1 - 64 KB video BIOS

† See note following bits 01, 00.

Bits 03, 02 - ROM_TYP, ROM Type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000H - 0FFFFFH or FE0000H - FFFFFFH.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000H - 0FFFFFH or FF0000H - FFFFFFH.

For ROM type 10, CSPROM is asserted when the address is 0F0000H - 0FFFFFH, FF0000H - FFFFFFH or 0C0000H - 0CXFFFH where X is determined by VB_SIZ. This allows either a 128 Kbyte BIOS with a 64 Kbyte system BIOS and a 64 Kbyte video BIOS, or a 64 Kbyte BIOS with a 32 Kbyte system BIOS and a 32 Kbyte video BIOS. The 32 Kbyte video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000H - CX000H and F0000H - FX000H. A

64 Kbyte EPROM needs addresses SA15 - SA0. A 128 Kbyte EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128 KB system BIOS, located at E0000H - FFFFFH
- 0 1 - 64 KB system BIOS, located at F0000H - FFFFFH (Default value)
- † 1 0 - 64 KB or 128 KB shared BIOS System BIOS located at F0000H - FFFFFH, video BIOS located at C0000H - CX000H
- 1 1 - Reserved

† See note following bits 01, 00.

Bits 01, 00 - BL_MOU, Backlight Mouse Control
Featured only in the WD7910LP

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port 1072H bit 11. Enabling the Backlight Mouse Control also affects the Back/light and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00

- 0 0 - No mouse control (Default value)
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

† NOTE

When SHD = 11 and X_MEM = 0, or SHD = 00 and ROM_TYP = 10, the portion of 0E0000H DRAM memory that is not mapped to 0C0000H (as determined by VB_SIZ) is not accessible. Once a portion of 0E0000H segment is mapped to 0C0000H, all 0E0000H accesses go to the expansion bus without generation of $\overline{\text{CSPROM}}$. This allows AT bus plug-in boards and/or drivers to access the E0000H segment.

6.2.5 High Memory Write Protect Boundary

Port Address C072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At RSTIN
Bits 15-08	None
A24 - A17	00

Bits 15-08 - Not used, state is ignored

Bits 07-00 - A24-A17, Boundary Address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at Port 6072H. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at Port 4072H, the memory timing mode changes immediately. The code that programs this register should be in ROM and not shadowed in RAM.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072H - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_ RAW	NP_WCAS		_NP_RCAS	

07	06	05	04	03	02	01	00
	NP_RAS_ HLD		NP_PWE			NP_WS	

Signal Name	Default At RSTIN
Bits 15, 07	None
NP_MODE	00
NP_RAW	0
NP_WCAS	00
NP_RCAS	00
NP_RAS_HLD	00
NP_PWE	000
NP_WS	00

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-Page Mode

There are two non-page modes available, Mode-00 and Mode-01. Mode-00 provides one processor clock of row address hold time and is used for 1, 2 or 3 wait state memory cycles. Mode-01 provides a half processor clock of row address hold time and is used for 0 wait state memory cycles. Because the memory timing may be adjusted in increments of half a processor clock, Mode-00 is suited for all DRAM and processor speeds. Mode-01 provides a half processor clock row address hold time, which is usually sufficient for system speeds of 12.5 MHz and slower. This compressed timing allows zero wait state operation.

Table 6-1A shows typically required DRAM speeds and register programming values for various processor speeds. Because DRAM timing varies among manufacturers, the required DRAM speed may differ from those listed in the table.

NP_MODE
14 13

0 0 - Minimum 1 wait state.

0 1 - Minimum 0 wait state.

PROCESSOR SPEED	NP_ MODE	DRAM SPEED	WAIT STATES	REGISTER 4072H
12.5 MHz	01	80 ns	0	3560H
16 MHz	01	53 ns	0	3560H
16 MHz	00	80 ns	1	1025H
20 MHz	00	80 ns	1	1025H
20 MHz	00	100 ns	2	107AH

TABLE 6-1A. TYPICAL DRAM SPEEDS

Bit 12 - NP_RAW, Non-page disable Read After Write

EMS accesses and interleave miss cycles (I/O cycle to device on RAD) may add one additional wait state.

NP_RAW = 0 -
Memory read cycles immediately following a write cycle causes an automatic wait state to be added before initiating the read cycle.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bit 11, 10 - NP_WCAS, Non-page Write CAS Delay

NP_WCAS
11 10

0 0 - CAS write delay 1.0 CLK2
0 1 - CAS write delay 1.5 CLK2
1 0 - CAS write delay 2.0 CLK2
1 1 - CAS write delay 2.5 CLK2

Bit 09, 08 - NP_RCAS, Non-page Read CAS Delay

NP_RCAS
11 10

0 0 - CAS read delay 1.0 CLK2
0 1 - CAS read delay 1.5 CLK2
1 0 - CAS read delay 2.0 CLK2
1 1 - CAS read delay 2.5 CLK2

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS Hold Time

The RAS active delay is reduced by half a clock during writes if NP_WCAS is set to 1X, or during reads if NP_RCAS is set to 1X.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS.

0 1 - RAS active until 1.5 clock after CAS.

1 0 - RAS active until 2.0 clock after CAS.

1 1 - RAS active until 2.5 clock after CAS.

Bits 04-02 - NP_PWE, Non-page CAS Pulse Width Extension

The pulse width is reduced by half a clock during writes if NP_WCAS is set to X1, or during reads if NP_RCAS is set to 1X.

NP_PWE
04 03 02

0 0 0 - No extension (2 CLK2 normal)
0 0 1 - Extended by 0.5 CLK2
0 1 0 - Extended by 1.0 CLK2
0 1 1 - Extended by 1.5 CLK2
1 0 0 - Extended by 2.0 CLK2
1 0 1 - Extended by 2.5 CLK2
1 1 0 - Extended by 3.0 CLK2
1 1 1 - Extended by 3.5 CLK2

Bits 01, 00 - NP_WS, Non-page Wait States

NP_WS makes it possible to unconditionally add wait states to all DRAM cycles. Condional wait states may be added to read after write cycles, EMS accesses and interleave miss cycles, with NP_RAW (bit 12).

NP_WS
01 00

0 0 - No wait states added
0 1 - 1 Wait state added
1 0 - 2 Wait states added
1 1 - 3 Wait states added

TIMING	NUMBER OF CLK2'S	
	MODE-00	MODE-01
Row address to RAS	2	2
RAS width	3 + NPH + NPHB / 2	1 + NPH + NPHB / 2
Row address hold	1	0.5
Column address setup (read)	1 + NPRF / 2	0.5 + NPRF / 2
Column address setup (write)	1 + NPWF / 2	1 + NPWF / 2
RAS hold (read from CAS)	1 + NPHB / 2 - NPRF / 2 + NPH	0.5 - NPRF / 2 + NPH
RAS hold (write)	1 + NPHB / 2 - NPWF / 2 + NPH	0.5 - NPWF / 2 + NPH
CAS width (read)	① + NPCAS + NPCB / 2 - NPRF / 2	① + NPCAS + NPCB / 2 - NPRF / 2
CAS width (write)	① + NPCAS + NPCB / 2 - NPWF / 2	① + NPCAS + NPCB / 2 - NPWF / 2
RAS precharge	2 × (2 + NP_WS) - RAS width	2 × (2 + NP_WS) - RAS width
Column address hold	1 - NPCB / 2	1 - NPCB / 2

① 2 if NPCAS = 0 or 1
1 if NPCAS = 2 or 3

NPWF = Bit 10 NPRF = Bit 08 NPH = Bit 06 NPHB = Bit 05
NPCAS = Bits 04, 03 NPCB = Bit 02 NP_WS = Bits 01, 00

TABLE 6-1B. NON-PAGE MODE TIMING

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6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access †	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access, pipline mode †	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit, pipeline mode †	1
	Read page first access non-pipeline mode †	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4

† Equal Bank sizes, non-EMS cycle

First access is a page mode memory cycle which immediately follows a refresh, DMA or master cycle. It is not necessary for the DRAMs to be precharged for a first access cycle, since all RAS signals have been high in the previous cycle. This shortens a first access page mode cycle by one wait state. For example, a read page miss, non-pipeline mode in 80386SX mode is four wait states. A read page miss, non-pipeline mode, first access in 80386SX mode is three wait states. All installed DRAMs must be the same size and configuration and the memory cycle cannot be an EMS cycle for a first access to occur.

TABLE 6-2. PAGE MODE WAIT STATES

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64 Kbyte, 256 Kbyte, 1 Mbyte or 4 Mbyte SIMM memory modules.

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	64 KBITS NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 4-WAY INTERLEAVE, 256K 2-WAY INTERLEAVE, 1MBITS NON-INTERLEAVE OR 512 KBITS X 8 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	256 KBITS 4-WAY INTERLEAVE, 1 MBITS 2-WAY INTERLEAVE, 4 MBITS NON-INTERLEAVE OR 512 KBITS X 8 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1 MBITS 4-WAY OR 4 MBITS 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	4 MBITS 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	512K X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A22	A19	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: NON-INTERLEAVE											
ROW	A13	A9	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A10	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A22	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	2M X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A23	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	REFRESH ADDRESS											
ROW		A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER (Continued)

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872H - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_ RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	00
Bits 12, 09, 08	None
EMS_EN	00
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS Pointer

The INC bit controls whether or not the EMS Pointer at Port E072H is to be incremented after each read or write of the EMS Page Register at Port E872H.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper Page Frame Location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000H (Default value)

0 1 - Upper page frame starts at C8000H

1 0 - Upper page frame starts at CC000H

1 1 - Upper page frame starts at D0000H

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS Enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming without having to enable a Page Frame. This is useful for initializing the lower Page Frame.

1 0 - Enable upper Page Frame assignments and EMS register programming.

1 1 - Enable upper and lower Page Frame assignments and EMS register programming.

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable Lower Boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17,
LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128 Kbyte below the actual start address. For example, to start EMS at the 1 Mbyte boundary, this field should be set to 07H.

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6.4.2 EMS Page Register Pointer

Port Address E072H - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
DLT							
16	15	15	13	12	11	10	9

07	06	05	04	03	02	01	00
DLT		POINTER					
8	7						

Signal Name	Default At RSTIN
DLT	0-0
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in Port 6872H, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at Port E872H. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

Bits 15-06 - DLT, Delay Line Test

In the Delay Line Test Mode, these bits represent the state of internal Delay Line signals.

The Delay Line Test is initiated by bit 8 (TDL) in the Test Enable Register at Port Address A872H.

Bits 05-00 - POINTER, EMS Page Register Number

Decimal number, 00 through 39. When programming this field, the hex equivalent 00 through 27H should be used.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF

EMS registers 32 through 39 (decimal) can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See Port E872H description.

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 (decimal) are enabled or disabled as a block. If the EMS_EN field of Port 6872H is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See Port E872H description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872H - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

There are 40 EMS Page Registers accessible through Port E872H. Only EMS registers 32 through 39 are initialized to zero. EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at Port E072H provides the offset location for Port E872H.

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
Bits 14-12	0
P11-P0	0

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at Port 6872H. When EMS_EN equals 11, the EN bit in this register is treated as a one for the lower Page Frame.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MBytes of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16 Kbytes, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128 Kbytes of memory and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MBytes, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOCHRDY to make the transfer.

NOTE

When using external EMS memory with P11 = 1, EN (bit 15) must be 0.

7.0 CACHE CONTROLLER

The Cache Controller provides an effective way to increase the memory bandwidth by storing the most frequently used data in the internal Cache DATA RAM. The WD7910 provides both software and hardware mechanisms to assure coherency of the data between CPU, DMA and Bus Master cycles. During DMA/Master write cycles, the controller will compare the system address and the tag contents. If the address matches, the data will be written into the data RAM. The cache can also be flushed by writing to the flush register.

7.1 CACHE ARCHITECTURE

The cache controller contains of eight functional blocks.

- Processor Interface
- TAG RAM
- DATA RAM
- SNOOP Interface
- Non-cacheable Control
- Diagnostic Control Logic
- LRU
- Flush

Figure 7-1 shows a block diagram of the cache.

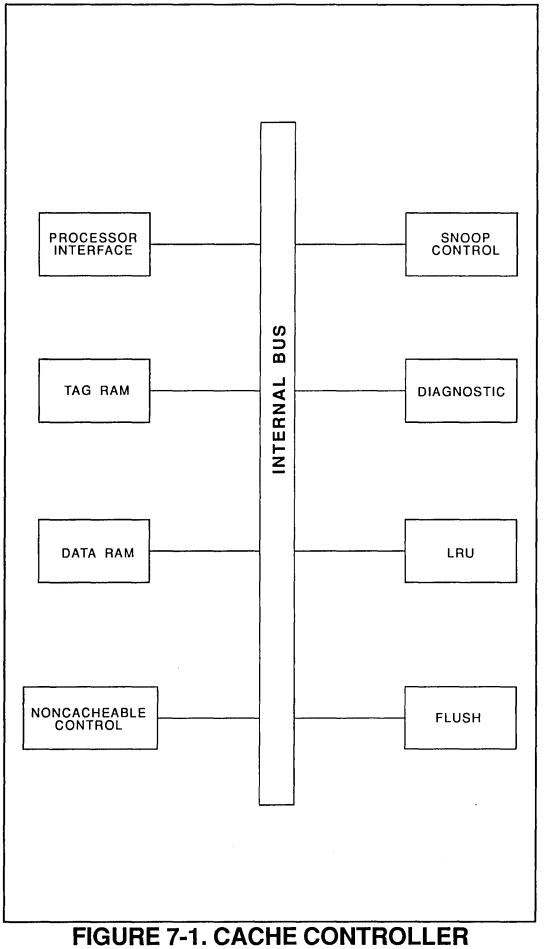

FIGURE 7-1. CACHE CONTROLLER FUNCTIONAL DIAGRAM

7.1.1 Processor Interface

The processor interface supports the 80386SX in both pipeline and non-pipeline mode. It keeps track of the 80386SX processor states a generates READY for read hit cycles. It ignores all the I/O and co-processor cycles.

7.1.2 TAG RAM

BIST (Built-In-Self-Test)logic is included in the TAG RAM to reduce test time.

The internal TAG RAM is organized as two sets of 256 x 21 self-timed synchronous static RAM. Twelve bits are used to store A12:23 from the processor; 8 bits are used to store the demultiplexed A1:3 as line valid, and 1 bit is used as block valid. The block valid bit can be cleared by the FLUSH function which flushes the cache contents and causes block miss for all the subsequent cycles.

A4 through A11 from the 80386SX selects one of the entries from each set. The output from the TAG RAM is compared against the address (A12:23,A1:A3) from the processor. If the address is the same and the corresponding line valid and block valid bits are set, a cache hit cycle is activated. If an address match occurs when the block valid bit is set, and the line valid is clear, it is a line miss. On the other hand, if the address does not compare or the block valid bit is clear, it is a block miss cycle.

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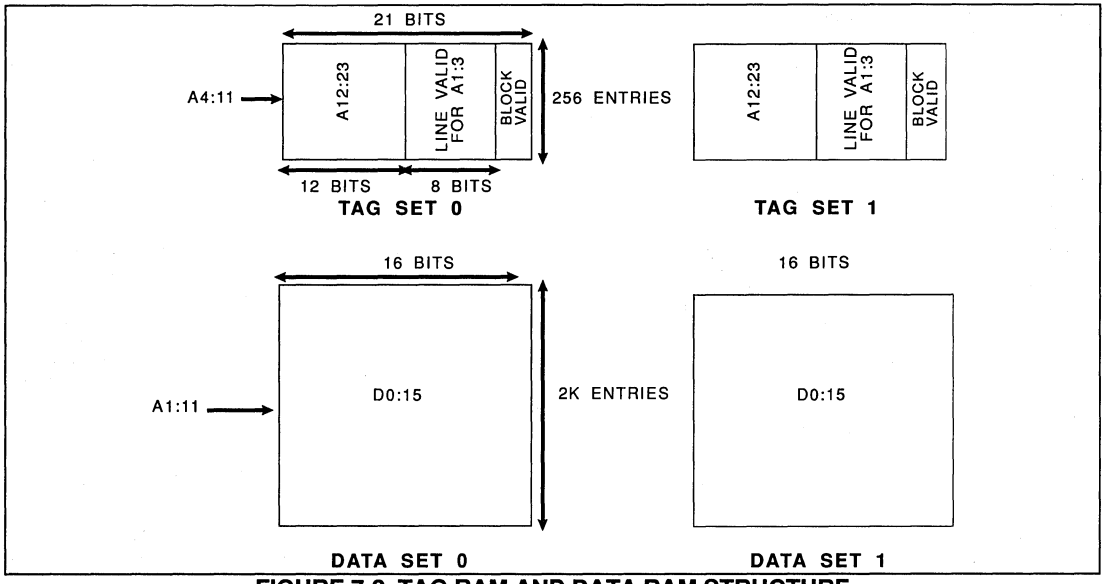

FIGURE 7-2. TAG RAM AND DATA RAM STRUCTURE

During the read block miss cycle, the address is written into the TAG RAM, the block valid bit is set, and the corresponding line valid bit is set.

During the read line miss cycle, the corresponding line valid bit is set, and all other bits are not altered.

Address Compare	Line Valid	Block Valid	
X	X	0	Block Miss
0	X	1	Block Miss
1	0	1	Line Miss
1	1	1	Hit

During a memory write cycle, the contents of the TAG RAM is not affected. The Block size of the TAG RAM is eight lines and each line is 2 bytes. The TAG RAM enters low power mode during Full Power Down to conserve power.

7.1.3 Data RAM

The internal DATA RAM is organized as 2 sets of 2K x 16. During a read hit cycle, the data is provided by one of the sets of DATA RAM to the processor. During a read miss cycle, the data is provided by the DRAM to the processor and is written into the DATA RAM. If the read cycle is a page hit, it will be a one wait state cycle. If it is a page miss, it will be a four wait states cycle. See Section 13.4, Cache Controller Timing.

During a write hit cycle, the data from the processor is written into the DATA RAM to maintain data coherency. In a write miss cycle, either block miss or line miss, no action is taken and DATA RAM contents are not affected. See Section 13.4, Cache Controller Timing.

The DATA RAM enters low power mode during Full Power Down to conserve power. BIST logic is included in the DATA RAM to reduce test time.

7.1.4 Snoop Interface

The Snoop interface maintains the data coherency when DMA or Master cycles take place. When a DMA or Bus Master write cycle occurs, the Snoop logic will update the data in the DATA RAM if the address from DMA or the Bus Master is the same as the corresponding TAG address(Hit cycle). If no match is indicated (Miss cycle), the DATA RAM will not be updated. See Section 13.4, Cache Controller Timing.

7.1.5 Non-cacheable Control

Two user definable and twelve standard non-cacheable regions are provided. Ten of the twelve standard regions are 16KB increments from C8000H - EFFFFH. These regions can be used as EMS memory or for DOS 5.0 Upper Memory Blocks and can be enabled or disabled individually. The other two standard non-cacheable regions are the video BIOS area (C0000-CXFFF or E0000-EFFFF) and the system BIOS area (F0000-FFFFF). The Non-cacheable control logic allows cacheing of these regions to be enabled or disabled individually.

The two user definable non-cacheable regions can also be enabled individually. The non-cacheable regions are set by the upper and lower limit registers. These regions are assigned on 4Kbyte boundaries anywhere in the 16MB physical address space of the 80386SX.

The typical applications of these user defined noncacheable areas are the memory between 512KB and 640KB, and the memory accessed on the AT bus. When powered up, the WD7910 assumes all the memory from 0KB to 640KB and 1M to 16MB are cacheable. It is necessary to have the BIOS to program the noncacheable region registers.

7.1.6 Diagnostic Control Logic

The function of the diagnostic control logic, when enabled, is to map the internal TAG RAM and LRU RAM to address 20000H and DATA RAM to address 40000H. In this mode, memory accesses to these address ranges are diverted to the internal TAG RAM and DATA RAM. This permits the system BIOS to test the internal DATA RAM and TAG RAM.

During Diagnostic Access, the 21-bit TAG RAM (D20:0) and the 2-bit LRU RAM (L1:0) are concatenated to 23 bits and mapped into the Address Space by using A1 to determine whether the data presented is TAG RAM bits D20-D9 (A1 Low) or TAG RAM bits {L1:0,D8:0} (A1 high). Since the LRU RAM has 128 entries (See Section 3.1.7) whereas the TAG RAM has 256 entries, so address A4 has no effect on the selection of the LRU RAM.

7.1.7 LRU

The LRU section has 128 entries and each entry has 2 bits. Addresses 11:5 are used to select one of the entries and Address 4 is used to select one of the two bits. In the event of a read miss, either group can be updated with new data. The LRU bit of the corresponding entry flags the candidate for replacement. Once the replacement is done, LRU bit of the corresponding entry is changed and pointed to the other set. In the event of read hit, the LRU bit of the corresponding entry points to the other set. During a write hit cycle, the corresponding LRU bit is changed and pointed to the other set. The LRU bit is not changed for write miss cycles. All the entries are reset to zero by NRESIN.

7.1.8 Flush

Flush is used to clear all the block valid bits in the TAG RAM and to clear all the LRU bits. This force the cache controller to rebuild the cache contents and force all the subsequent fetch to the DRAM. This is used after an EMS page change.

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7.2 CACHE CONTROL REGISTER

Port Address C472 Read / Write

15	14	13	12	11	10	09	08
C_ ENBL	C_ SSB	C_ DIAG	C_ SVB	MFR	C_M	HI_ME M9	HI_ME M8

07	06	05	04	03	02	01	00
HI_ME M7	HI_ME M6	HI_ME M5	HI_ME M4	HI_ME M3	HI_ME M2	HI_ME M1	HI_ME M0

Bit 15 - C_ENBL, Cache Enable

This bit is used to enable the cache controller. Before writing to this bit, the memory controller must be programmed to support the cache mode. This can be done by writing (01) to bit 13 and 12 of register 3872. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_ENBL= 1 Cache Enable
C_ENBL= 0 Cache Disable (Default)

Bit 14 - C_SSB, Cache Shadowed System BIOS at F0000H through FFFFFH

When the System BIOS is shadowed, it can also be cached to increase the system BIOS performance.When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SSB = 1 Enable caching of shadow RAM. When Custom mode is enabled, the address from 0F0000H - 0F0FFFH is not cached.

C_SSB = 0 Disable caching of shadow RAM (Default)

Bit 13 - C_DIAG, Cache Diagnostic Mode

Enabling the cache and this bit puts the cache into diagnostic mode as described in section 7.1.6. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_DIAG = 1 Cache is in diagnostic mode

C_DIAG = 0 Standard cache mode (Default)

Bit 12 - C_SVB, Cache Shadowed Video BIOS at E0000H through EFFFFH or C0000H through CXXXXH

When the Video BIOS is shadowed, it can also be cached to increase the Video BIOS performance.When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SVB = 1 Enable Cacheing Video BIOS

C_SVB = 0 Disable Cacheing Video BIOS (Default)

Bit 11 - C_MFR, Manufacturing Test Bit

Bit 10 - C, Cache Mode

C = 1 2-way set associative
C = 0 Direct-mapped (Default)

Bits 9:0 - HI-MEM, High memory region caching control. Setting these bits enables the caching of the HI-MEM region. Default after reset is 0.

BIT 9 EC000H - EFFFFH
BIT 8 E8000H - EBFFFH
BIT 7 E4000H - E7FFFH
BIT 6 E0000H - E3FFFH
BIT 5 DC000H - DFFFFH
BIT 4 D8000H - DBFFFH
BIT 3 D4000H - D7FFFH
BIT 2 D0000H - D3FFFH
BIT 1 CC000H - CFFFFH
BIT 0 C8000H - CBFFFH

Bits 9:0 = 1, Enable caching
Bits 9:0 = 0, Disable caching

7.2.1 Noncacheable Region 1 Upper Boundary

Port Address BC72. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S_REF	INT_DIS	INT_ST	S_IO RDY

This register determines the upper address boundary of the user defineable noncacheable region 1. Default after reset is zero.

Bits 15:4, = A23: 12 of the upper address boundary

Bit 3, Slow Refresh

When this bit is set, the DRAM refresh rate is slowed down to 120µs. This bit does not affect the refresh toggle bit in Port 61.

Bit 3 = 1, Enable Slow Refresh

Bit 3 = 0, Disable Slow Refresh (Default)

Bit 2, Interrupt Disable

When this bit is set, the interrupt from the interrupt controller is disabled. The command will not take effect immediately if the interrupt request signal from the interrupt controller is active. The command will take effect immediately if the interrupt request signal is inactive. This allows control of the interrupt regardless of the Operating system privilege level.

Bit 2 = 1, Disable the hardware interrupt from the interrupt Controller

Bit 2 = 0, Enable hardware interrupt.

Bit 1, Interrupt Disable Status (Read Only)

This enables reading of Interrupt Status regardless of Operating System privilege Level.

Bit 1 = 1, Indicates the Interrupt Disable command is pending

Bit 1= 0, Indicates the Interrupt Disable command is processed

Bit 0, SNOOP with IOCHRDY active

During periods when the CPU Clock is slower than the AT BUS clock (slowed for power savings), the Snoop Logic may be unable to properly track the memory cycle during DMA or BUS Master Cycles. Setting this bit enables the WD7910 to use the IOCHRDY signal to lengthen the cycle.

Bit 0 = 1, Enable IOCHRDY for DMA/Master cycle

Bit 0 = 0, Disable IOCHRDY for DMA/Master cycle (Default)

7.2.2 Noncacheable Region 1 Lower Boundary

Port Address B472. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S DMA_ CLK	X_ WS	S_ BIST	BIST _S

This register determines the lower address boundary of the user defineable noncacheable region 1. Noncacheable region 1 is disabled when the upper boundary is set below the lower boundary. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary.

Bit 3, Stop DMA Clock

Setting this bit causes the DMA clock to stop while there is no DMA activity. Upon any DMA request (DRQn), the DMA clock starts up again and continues to run until 16 DMA clocks after the end of the DMA Acknowledge (DACKn).

Bit 3 = 1, Enable Stop DMA Clock

Bit 3 = 0, Disable Stop DMA Clock (Default)

Bit 2, Extra Wait State for Page Mode

If this bit is active, it adds an extra wait state to all the memory cycles. With this featury system manufacturer can use slower DRAM for WD7910 system without loss of huge performance and achieve saving since the majority of the memory access are directly to the internal cache.

Bits 1, Start BIST

Setting bit 1 forces the BIST to check the TAG RAM and DATA RAM. The result can be checked by reading BIT 0. Bit 0 is a read only register.

Bit 0, BIST Status

Bit 0 = 1, RAM error.

Bit 0 = 0, No error found.

7.2.3 Noncacheable Region 2 Lower Boundary

Port Address CC72 Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12				NR 2C

This is used to determine the lower address boundary of the user defineable noncacheable region 2. Any address above or equal to this address is considered non-cacheable. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary

Bits 3:1, Test Register

For Factory use only.

Bit 0, Non-cacheable Region 2

Bit 0 = 1, enables non-cacheable Region 2
Bit 0 = 0, disables non-cacheable Region 2 (default)

7.2.4 Flush

Port Address F872H Write Only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00

Signal Name	Default At RSTIN
All signals	None

Writing to this I/O port with any data will clear all the valid bits in the TAG RAM. This is ordinarily used to clear the cache when there is a change to the EMS page register and also causes the WD7910 to output Chip Select number 13H.

8.0 PORT CHIP SELECT AND WD7910LP REFRESH

This section describes refresh control logic peculiar to the WD7910LP and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 8-1 identifies the ports, their Chip Select number, I/O address and function.

8.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H - Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF †	0
V_REF †	0
CBR_REF †	0
CBR_SR	0
SCSI	0
PAR	00
PAR_L	0
SER_A	000
SER_AL	0
SER_B	000
SER_BL	0

† Featured only in the WD7910LP

Bit 15 - M_REF, Memory Refresh Power Down Mode
Featured only in the WD7910LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and M_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value).

M_REF = 1 -
Slow refresh main on-board memory.

Bit 14 - V_REF, Video Refresh Power Down Mode
Featured only in the WD7910LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and V_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS Before RAS Refresh For On-board DRAM
Featured only in the WD7910LP

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not.

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 8-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353XH

Bits 10, 09 - PAR, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 8-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BCH - 3BFH

1 0 - PAR chip select at I/O port 378H - 37FH

1 1 - PAR chip select at I/O port 278H - 27FH

Bit 08 - PAR_L, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, Serial Port A Chip Select

The serial port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port A chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port A chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port A chip select at I/O port 2E8H - 2EFH

Bit 04 - SER_AL, Serial A Port Bus Location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B Serial Port B Chip Select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port B chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port B chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port B chip select at I/O port 2E8H - 2EFH

Bit 00 - SER_BL, Serial B Port Bus Location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_BL = 1 -
Serial port B is located on the expansion data bus

8.2 RTC, PVGA, 80287 TIMING, AND DISK CHIP SELECTS

Port Address 2872H - Read and Write

Bits 12 through 07 and Port Address 3072H control the use and location of the Programmable Chip Select.

15	14	13	12	11	10	09	08
RTC_L	FST_VGA	FST_SCSI	EN_PCS1	U_MSK1	L_MSK1		

07	06	05	04	03	02	01	00
PRG_L	HS_HD		P/S	HS_287	LK_PSW	DS_HD	DS FLP

Signal Name	Default At RSTIN
RTC_L	0
FST_VGA	0
FST_SCSI	0
EN_PCS	0
U_MSK1	00
L_MSK1	00
PRG L	0
HS HD	000
P/S	000
HS 287	0
LK PSW	0
DS HD	0
DS FLP	0

Bit 15 - RTC_L, Real-Time Clock

The Real-Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

Bit 14 - FST_VGA, Fast VGA Video

The performance of Western Digital Imaging PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital Imaging PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
One wait state I/O cycle to PVGA

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 SCSI Contoller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS1, Enable Programmable Chip Select 1

The Programmable Chip Select logic is selected with chip select 11 and may be disabled or enabled. See Table 8-1.

EN_PCS = 0 -
Disable Programmable Chip Select (Default value)

EN_PCS = 1 -
Enable Programmable Chip Select

Bit 11 - U_MSK1, Upper Address Bits Masked

U_MSKI determines whether or not the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

U_MSKI = 0 -
A15 through A10 are ignored (Default value).

U_MSKI = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK1, Lower Address Bits Masked

L_MSK1 determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

L_MSK1
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value).

0 0 1 - A00 is ignored.

0 1 0 - A00, A01 are ignored.

0 1 1 - A00, A01, A02 are ignored.

1 0 0 - A00, A02, A03 are ignored, A01 is not ignored, ver. A-F. A00, A01, A02 A03 are ignored, WD76C10A and newer.

Bit 07 - PRG_L, Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable Chip Select is on the expansion bus.

Bit 06 - HS_HD, High Speed Hard Disk Data Transfer Rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with IOCS16 ignored and the WD76C20 hard disk chip select remaining stable.

NOTE

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives WD-AC280, WD-AC140, WD-AC160, WD-AC2120, WD-AP4200, WD-AB130 and WD-AH260.

HS_HD = 0 -
Compatible bus timing enabled (Default value).

HS_HD = 1 -
High speed hard disk accesses enabled.

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 8-1, chip select numbers 08H through 0BH.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value).

P/S = 1 -
Secondary hard disk and Floppy address selected.

Bit 03 - HS_287, Co-processor 80287 High Speed Timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_287 results in 16-bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value).

HS_287 = 1 -
Fast 80287 timing.

Bit 02 - LK_PSW, Prevent Locking Password

Port 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092H bit 3, Lock_Pass can be set (Default value).

LK_PSW = 1 -
Port 092H bit 3, Lock_Pass can not be set.

Bit 01 - DS_HD, Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

8.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072H - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

Signal Name	Default At RSTIN
All signals	None

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8.4 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 8-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
ROM Chip Select	N/A	00	Chip select for BIOS ROM
Keyboard Control	060 - 06E even	01	Chip select for 8042
80287	00E0 - 00FF	02	Chip select for numeric processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real-time Clock	070	05	RTC ALE
Real-time Clock	071	06	RTC Write Strobe
Real-time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary address Secondary address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary address Secondary address
Floppy Control Chip Select	3F7 377	0A	Primary address Secondary address (Floppy enabled, HD disabled)
Floppy and HD Control Chip Select	3F7 377	0B	Primary address Secondary address (Floppy enabled, HD enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary address Secondary address
Hard Disk Chip Select	3F6 3F7 † 376 377 †	0D	Primary Address Secondary address
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ††	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	

TABLE 8-1. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ††	
Program Chip Select 1	PROG 1	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Floppy Chip Select	3F0 - 3F1 370 - 371	18	Primary address Secondary address
Floppy Chip Select	3F3 373	19	Primary address Secondary address
Program Chip Select2	PROG 2	1A	
Program Chip Select 3	PROG 3	1B	
Reserved		1E	Reserved
Reserved		1F	Reserved

† IDE Hard disk enabled, floppy disabled

†† The Chip Select Number is the decoded value of CS4 - CS0. If the Programmed Chip Select corresponds to any other decode, the Programmed Chip Select is suppressed. If Serial Port A and B are programmed for the same address, Serial Port B Chip Select is suppressed.

TABLE 8-1. I/O PORT ADDRESSES (Continued)

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9.0 POWER MANAGEMENT CONTROL

The WD7910LP supports all PMC inputs, output and interrupt functions.

9.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD7910LP is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2 and VCPI.

With the WD7910LP a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approch to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

System Activity
System activity denotes periods of time in which the system performs useful tasks. The sources Of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ 0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ 8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A progammable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

Using SAM for System Power Management:

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period, SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation, and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order to do this, control to the CPU must be relin-

quished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds, and establish a clean breakpoint for Suspending the system.

Advantages of SAM:

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

- Detection of system activity for extended periods of time, for the purposes of system timeout.
- Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program.

7. SAM also carries information on DMA activity state. This is used for determining whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at powerup time on Resume.

NOTE

SAM cannot be used for determining when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2.

9.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control Register is used to control the power converter from the processor. The WD7910LP holds CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT273 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD7910LP's internal registers by way of the PMC logic. The keyboard processor starts a local ac-

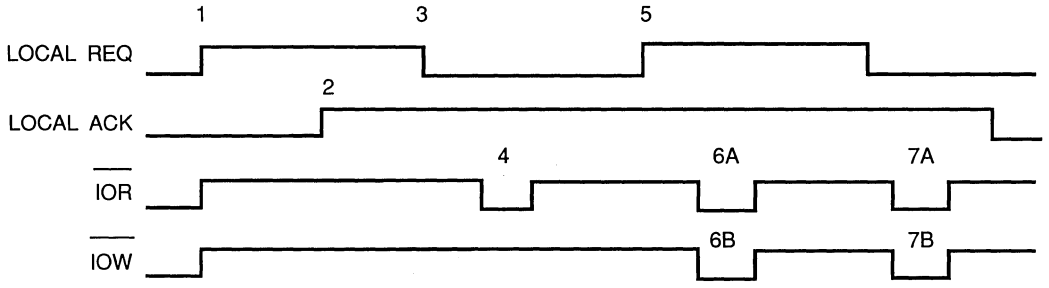
cess by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1 and Table 9-2). The WD7910LP arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD7910LP asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD7910LP on the data bus and drops the LCL_REQ. The WD7910LP responds by de-asserting LCL_ACK.

If the opcode specified a register write, data high (D15 through D08) and data low (D07 through D00), bytes are passed to the WD7910LP. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD7910LP to the keyboard processor.

All special operation registers within the WD7910LP may be accessed in this manner without first unlocking the register. See section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 9-1 shows the handshake procedure, followed by the keyboard controller and the WD7910LP.

Figures 9-2 and 9-3 represents the powerdown and powerup sequence and control.



1 8042 Requests local data transfer

2 WD7910LP returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD7910LP reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD7910LP Reads high byte

7A WD7910LP Read low byte, writes to internal register

FOR READ CYCLE OF WD7910LP INTERNAL REGISTER:

6B WD7910LP Writes high byte to 8042

7B WD7910LP writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	RSV	A15	A14	A13	A12	A11	A10

DIR = 1 - Read register (generates IOW to 8042)

DIR = 0 - Write register (generates IOR to 8042)

FIGURE 9-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

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9.3 PMC OUTPUT CONTROL REGISTERS

Port Address 7072H - Bits 07-00 are Read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 7:0

Featured only in the WD7910LP

Port Address 7872H - Bits 07-00 are Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 15:08

Featured only in the WD7910LP

PMC	PMC OUTPUT SIGNAL PORT 7072H	PMC	PMC OUTPUT SIGNAL PORT 7872H
0H	CPU Clock Driver Enable	8H	User Defined
1H	LCD Enable	9H	User Defined
2H	Backlight Enabled	AH	User Defined
3H	LCL_ACK	BH	User Defined
4H	LCL_ATN	CH	User Defined
5H	Processor powerdown	DH	User Defined
6H	Gate A20	EH	User Defined
7H	Full Powerdown	FH	User Defined

TABLE 9-1. PMC OUTPUT SIGNALS

9.4 PMC TIMERS

Port Address 8072H - Read and Write

When no keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 9-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 01 and 00 (BL_MOU) in the RAM Shadow And Write Protect Register at Port Address 6072H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default RSTIN
BL_TIMEOUT †	0
LCD_TIMEOUT †	0

† Featured only in the WD7910LP

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - LCD enabled

9.5 PMC INPUTS

Port Address 8872H - Read and Write

15	14	13	12	11	10	09	08
PMC_UPD	EN_LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD	0
EN_LCL †	0
AF7-AF2 †	0
IN7-IN0	None

† Featured only in the WD7910LP

Bit 15 - PMC_UPD, Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (Port Address 7072H) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

8

Bit 14 - EN_LCL, Enable Local Request - Featured only in the WD7910LP

EN_LCL enables the PMCIN 2 to initiate a local access of the WD7910LP internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

Bits 13-08 - AF7-AF2, Local Attention Flags Featured only in the WD7910LP

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

Bits 07-00 - IN7-IN0, PMC Inputs 7-0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7 through IN0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 9-2.

9.6 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
Non-maskable Interrupt Enable							

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
Local Attention Enable							

Signal Name	Default At RSTIN
EI7-EI2 †	0
EA7-EA2 †	0

† Featured only in the WD7910LP

Bits 15-10 - EI7-EI2, Non-maskable Interrupt Enable 7 through 2 - Featured only in the WD7910LP

EI7 through EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7 through IN_2 in Port 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Non-maskable Interrupt not enabled

EI7-EI2 = 1 -
Non-maskable Interrupt is enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Local Attention Enable Featured only in the WD7910LP

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled

Bits 01, 00 - Not used, state is ignored

9.7 NMI STATUS

Port Address 9072H - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
	Non-maskable Interrupt Flags						

Signal Name	Default At RSTIN
IF7-IF2 †	0-0

† Featured only in the WD7910LP

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Non-maskable Interrupt Flags 7 through 2 - Featured only in the WD7910LP

NMI interrupt flags IF7 through IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

Bits 01, 00 - Not used, must be 0

8

PMC INPUT NUMBER[1]	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER[2]
00H	$\overline{\text{TURBO}}$		
01H	PROC_PWR_GOOD		
02H	LCL_REQ or User Defined	Transistion	IF2 or AF2
03H	User Defined	Transistion	IF3 or AF3
04H	User Defined	Transistion	IF4 or AF4
05H	User Defined	Transistion	IF5 or AF5
06H	User Defined	Transistion	IF6 or AF6
07H	User Defined	Active Edge	IF7 or AF7

[1] Port Address 8872H, section 9.5
[2] Port Address 9072H, section 9.7
Port Address 8872H, section 9.5

TABLE 9-2. PMCIN INPUTS

9.8 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN
All signals	None

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

9.9 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the WD7910. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

15	14	13	12	11	10	09	08
AMT OUT	DEV		TM7	TS7	S F N M	AUT_ EOI	RA_ EOI

07	06	05	04	03	02	01	00
PLM2 PLM1 PLM0 Priority Level Master			PLS2 PLS1 PLS0 Priority Level Slave			SMM M	SMM S

Signal Name	Default At RSTIN
Bits 15, 12-00	None
Bits 14, 13	00

Bit 15 - AMTOUT, Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

Bit 14, 13 - DEV, Device

DEV identifies the device as WD7910 or WD7710 and is used in conjunction with VER at Port Address 9872H and SVER at Port Address A872H. DEV, VER and SVER are defined in Table 10.1.

Bit 12 - TM7, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 11 - TS7, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 10 - SFNM, Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD7910 does not require SFNM for the slave interrupt controller and ignores its state.

Bit 09 - AUT_EOI, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD7910 does not require AUT_EOI for the slave interrupt controller and ignores its state.

Bit 08 - RA_EOI, Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7 through 5 of OCW2). The WD7910 does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

Bits 07-05 - PLM2-PLM0, Priority Level Master

PLM2-PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bits 04-02 - PLS2-PLS0, Priority Level Slave

PLS2-PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bit 01 - SMMM, Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

Bit 00 - SMMS, Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

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9.10 PORT 70 SHADOW REGISTER

Port Address E472

15	14	13	12	11	10	09	08
CLK 32K	REF DET	INTR	NOD MA	TOD UN	RSVD	RSVD	RSVD

07	06	05	04	03	02	01	00
NMI MSK	RTC IR6	RTC IR5	RTC IR4	RTC IR3	RTC IR2	RTC IR1	RTC IR0

This register provides read-only information on the status of interrupts and DMA which is useful for determining when the processor may be put to sleep. Two bits are also provided for generating software delays without incurring the operating system traps that would result from accessing I/O port 0061 in virtual 86 mode. This register also contains a shadow of the real time clock address register, a write only I/O port. It is necessary to access the real-time clock CMOS RAM during Suspend/Resume operations. This shadow of Port 0070 allows it to be restored to the same state it was in at suspend time.

This register can be read without first unlocking the WD7910. This is important since the CLK32K, REFDET, and TODUN bits may need to be read frequently.

Bit 15 - CLK32K

This read-only bit is a divide by 2 of the PDREF input. It can be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 microsecond period with a 50% duty cycle.

Bit 14 - REFDET

This read-only bit is a copy of the REFDET bit available from I/O Port 0061, Bit 4.

Bit 13 - INTR

This read-only bit gives the state of the INTR output pin to the CPU.

Bit 12 - NODMA, No DMA

This read-only bit is set whenever it has been at least 30.5 microseconds since the last DMA or bus master cycle occurred.

Bit 11 - TODUN, Time of Day Update Needed (R/W)

This is a general purpose storage bit which can be written and read but has no effect on internal logic. Its purpose is to allow an SMI handler to signal the operating system that the time of day has been corrupted. This bit is checked by the Timer 0 Interrupt Handler. Note that although this bit is readable without unlocking the WD7910, it cannot be written unless the WD7910 is unlocked.

Bits 10:8 - RSVD

These read-only bits are reserved for future use. They currently are read back as a 0.

Bit 7 - NMIMSK, NMI Mask

This read-only bit gives the state of the NMI mask bit as it was set the last time I/O port 0070 was written.

Bits 6:0 - RTCIR6-0

These read-only bits give the state of the real time clock address register as it was set the last time I/O port 0070 was written.

9.11 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13-11, 08-00 Read and Write Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in section 9.12.

15	14	13	12	11	10	09	08
IRR AE	CB12	AM TM	ACT LCH	IND ET	ACT AFT	ACT BEF	AM EN

07	06	05	04	03	02	01	00
Coarse Timeout Count AMC7 AMC6 AMC5 AMC4				Fine Timeout Count AMC3 AMC2 AMC1 AMC0			

Signal Name	Default At $\overline{RSTIN}$
IRRAE	0
CB12	None
AMTM	0
ACTLCH	None
INDET	None
ACTAFT	None
ACTBEF	None
AMEN	0
AMC7-AMC0	0-0

Bit 15 - IRRAE, Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

Bit 14 - CB12, Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

Bit 13 - AMTM, Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

Bit 12 - ACTLCH, Activity Latch

This latch is always enabled, regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

Bit 11 - INDET, Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07-00) to be reached.

NOTE

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

Bit 10 - ACTAFT, Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -
Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

Bit 09 - ACTBEF, Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -
Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC7-AMC0 (bits 07-00). It would be necessary for the routine to clear the software counter if ACTBEF were set, since there would have been no activity only for the period of time programmed in AMC7-AMC0.

Bit 08 - AMEN, Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -
Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -
Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected, the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM7 through ACM0, INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

Bits 07-04 - AMC7-AMC4, Activity Monitor Counter Coarse

AMC7-AMC4 establish the timeout values from 64 seconds to 16 minutes in 64-second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

8

AMC7	AMC6	AMC5	AMC4	
0	0	0	0	0 seconds
0	0	0	1	1 min., 4s
0	0	1	0	2 min., 8s
0	0	1	1	3 min., 12s
0	1	0	0	4 min., 16s
0	1	0	1	5 min., 20s
0	1	1	0	6 min., 24s
0	1	1	1	7 min., 28s
1	0	0	0	8 min., 32s
1	0	0	1	9 min., 36s
1	0	1	0	10 min., 40s
1	0	1	1	11 min., 44s
1	1	0	0	12 min., 48s
1	1	0	1	13 min., 52s
1	1	1	0	14 min., 56s
1	1	1	1	16 min., 0s

Bits 03-00 - AMC3-AMC0, Activity Monitor Counter Fine

AMC3-AMC0 establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC3	AMC2	AMC1	AMC0	
0	0	0	0	0 ms
0	0	0	1	7.8 ms
0	0	1	0	15.6 ms
0	0	1	1	23.4 ms
0	1	0	0	31.3 ms
0	1	0	1	39.1 ms
0	1	1	0	46.9 ms
0	1	1	1	54.7 ms
1	0	0	0	62.5 ms
1	0	0	1	70.3 ms
1	0	1	0	78.1 ms
1	0	1	1	85.9 ms
1	1	0	0	93.8 ms
1	1	0	1	101.6 ms
1	1	1	0	109.4 ms
1	1	1	1	117.2 ms

NOTE

The fine timeout delay (AMC3 through AMC0) is added to the coarse timeout delay (AMC7 through AMC4) to obtain the total timeout delay.

9.12 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

15	14	13	12	11	10	09	08
PCSM	PMCILS	PMCIS2	PMCIS1	PMCIS0	NMIM	HDDM	COPM

07	06	05	04	03	02	01	00
IMS1	IMS0	IRR8M	IRR7M	IRR0M	ISR8M	ISR7M	ISR0M

Signal Name	Default RSTIN
All signals	0

Bit 15 - PCSM, Programmable Chip Select Mask

PCSM = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7910LP are considered activity.

PCSM = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7910LP are ignored.

Bit 14 - PMCILS, Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13-11, PMCIS2-0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

Bits 13-11 - PMCIS2-PMCIS0, Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

NOTE

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

PMCIS 2 1 0
0 0 0 - PMC input 2 selected
0 0 1 - PMC input 3 selected
0 1 0 - PMC input 4 selected
0 1 1 - PMC input 5 selected
1 0 0 - PMC input 6 selected
1 0 1 - PMC input 7 selected
1 1 0 - Reserved
1 1 1 - Disabled, no PMC inputs checked

Bit 10 - NMIM, Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

Bit 9 - HDDM, Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

Bit 8 - COPM, Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. For an 80286 system, this is I/O address range 00F8H through 00FFH. For an 80386SX system, this is when A23 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

Bits 07, 06 - IMS1-0, Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS1 through 0 provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

IMS 1 0
0 0 - IRQ5 masked
0 1 - IRQ10 masked
1 0 - IRQ11 masked
1 1 - IRQ15 masked

Bit 05 - IRR8M, Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register

at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

NOTE

See Test Enable Register (A872), Section 11.3 for information about IRQ9 enable control.

See SMI Auxillary Control Register (5472), Section 10.10, for a definition of the activity masks for PCS2 and PCS3.

Bit 04 - IRR7M, Interrupt Request Register 7 Mask

IRR7M = 0 -
Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -
Parallel Port or Spurious Interrupt (IRR7) is ignored.

Bit 03 - IRR0M, Interrupt Request Register 0 Mask

IRR0M = 0 -
Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -
Time Of Day Interrupt (IRR0) is ignored.

Bit 02 - ISR8M, Interrupt Service Register 8 Mask

ISR8M = 0 -
Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -
Real-Time Clock Interrupt (ISR8) is ignored.

Bit 01 - ISR7M, Interrupt Service Register 7 Mask

ISR7M = 0 -
Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -
Parallel Port or Spurious Interrupt (ISR7) is ignored.

Bit 00 - ISR0M, Interrupt Service Register 0 Mask

ISR0M = 0 -
Time of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -
Time Of Day Interrupt (ISR0) is ignored.

9.13 3V Suspend Shadow Registers

The 3V suspend mode provides maximum power savings for the system. The contents of the DRAM, chip set registers, CPU registers and video RAM are all written to the hard disk and then all voltages are shut down, including the power supply. The only logic left on in this mode is the real-time clock and a 3V suspend controller. The real-time clock and the 3V suspend controller run off of the real-time clock battery. When the resume request is sampled by the suspend controller, the suspend controller enables the power supply and resumes the system.

To maintain compatibility with the IBM AT, the timer and DMA registers cannot be read back. To overcome this, these registers are shadowed and read back through other registers. (See descriptions for registers 3C72, 4472 and 4C72.)

9.13.1 DMA Shadow Register 1

Port Address 3C72H (R)

15	14	13	12	11	10	09	08
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

07	06	05	04	03	02	01	00
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

Bit 15, the AD_DEC bit of register 0B for DMA channel 2.

Bit 14, the AUTO bit of register 0B for DMA channel 2.

Bits 13:12, the TRA_TYP bits of registers 0B for DMA channel 1.

Bits 11:10, the TRA_MOD bits of register 0B for DMA channel 1.

Bit 9, the AD_DEC bit of register 0B for DMA channel 1.

Bit 8, the AUTO bit of register 0B for DMA channel 1.

Bits 7:6, the TRA_TYP bits of register 0B for DMA channel 1.

Bits 5:4, the TRA_MOD bits of register 0B for DMA channel 0.

Bit 3, the AD_DEC bit or register 0B for DMA channel 0.

Bit 2, the AUTO bit of register 0B for DMA channel 0.

Bits 1:0, the TRA_TYP bits of register 0B for DMA channel 0.

9.13.2 DMA Shadow Register 2

Port Address 4472H (R)

15	14	13	12	11	10	09	08
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

07	06	05	04	03	02	01	00
TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD

Bits 15:14, the TR_TYP bits of register 0D6 for channel 6.

Bits 13:12, the TRA_MOD bits of register 0D6 for channel 5.

Bit 11, the AD_DEC bit of register 0D6 for channel 5.

Bit 10, the AUTO bit of register 0D6 for channel 5.

Bits 9:8, the TRA_TYP bits of register 0D6 for channel 5.

Bits 7:6, the TRA_MOD bits of register 0B for channel 3.

Bit 5, the AD_DEC bit of register 0B for channel 3.

Bit 4, the AUTO bit of register 0B for channel 3.

Bit 3:2, the TRA_TYP bits of register 0B for channel 3.

Bits 1:0, the TRA_MOD bits of register 0B for channel 2.

9.13.3 DMA Shadow Register 3

Port Address 4C72H (Read only for bits 14:0)

15	14	13	12	11	10	09	08
SCB		EX_ WR	RO_ PRI		CO_ DIS	TRA_ MOD	TRA_ MOD

07	06	05	04	03	02	01	00
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

Bit 15, Shadow Control BIT (SCB)

Bit 14, Reserved

Bit 13, When SCB is low, this bit represents the EX_WR bit of register 08. When SCB is high, this bit represents the EX_WR bit of register of register 0D0.

Bit 12, When SCB is low, this bit represents the RO_PRI bit of register 08. When SCB is high, this bit represents the RO_PRI bit of register 0D0.

Bit 11, Reserved.

Bit 10, When SCB is low, this bit represents the CO_DIS bit of register 08. When SCB is high, this bit represents the CO_DIS bit of register 0D0.

Bits 9:8, These bits represent the TRA_MOD bits of register 0D6 for channel 7.

Bit 7, AD_DEC bit of register 0D6 for channel 7.

Bit 6, AUTO bit of register 0D6 for channel 7.

Bits 5:4, the TRA_TYP bits of register 0D6 for channel 7.

Bits 3:2, the TRA_MOD bits of register 0D6 for channel 6.

Bit 1, the AD_DEC bit of register 0D6 for channel 6.

Bit 0, the AUTO bit of register 0D6 for channel 6

9.13.4 DMA Base Address and Count Register

When the SCB is high, the DMA base aaddress and base count can be read back from register 0 to 7. When SCB is low, register 0 to 7 represents the current address and current count.

9.13.5 Timer Count

When SCB is high, the timer base count can be read back from register 40:43. When SCB is low, the register 40:43 represents the timer current count.

9.14 SAVE AND RESUME

When the WD7910LP is in the Save And Resume Mode, it typically draws less than 500 µA. Figures 9-2 and 9-3 illustrate the steps that the WD7910LP goes through during power down and power up.

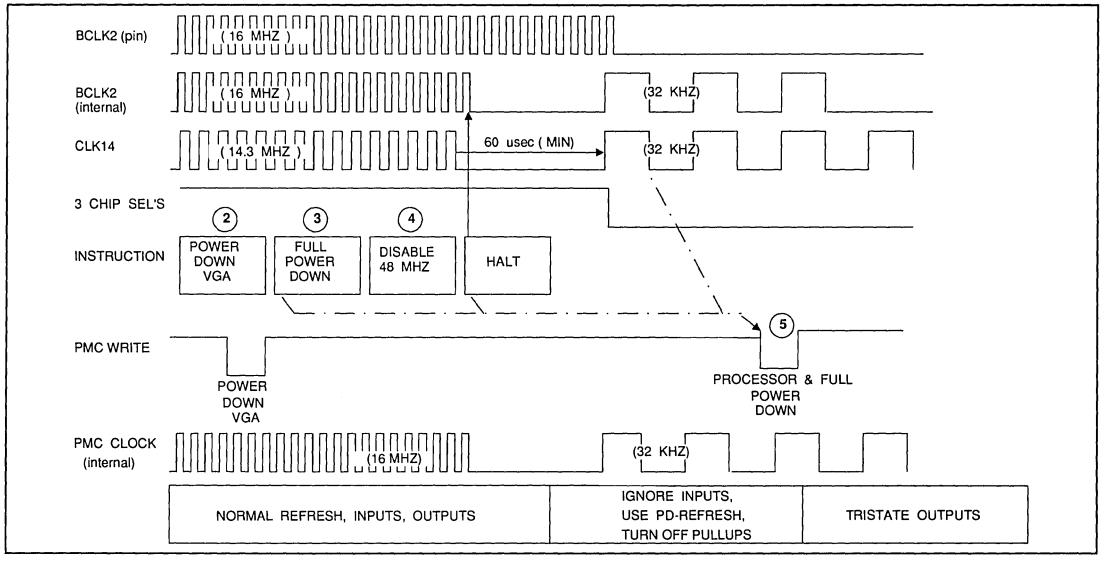

FIGURE 9-2. POWER DOWN

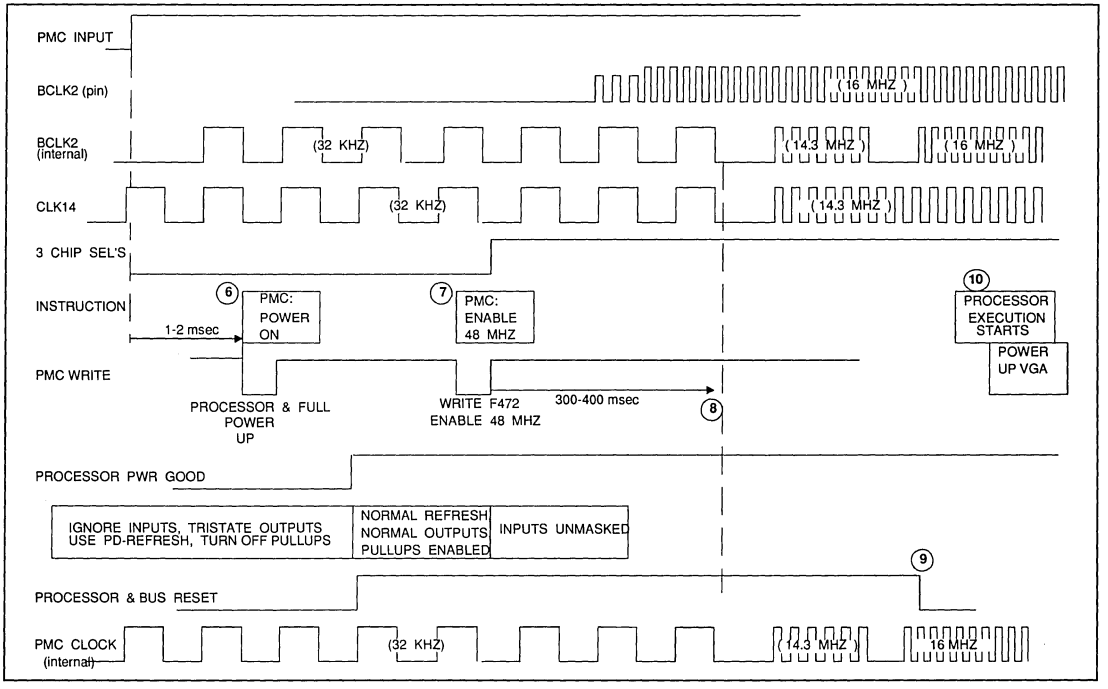

FIGURE 9-3. POWER UP

10.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

10.1 I/O TRAPS

In order to conserve power, certain I/O peripherals can be put to sleep when they are not in use. To accomplish this in a transparent manner, hardware must intercept (trap) any accesses made to the sleeping device and wake it up before allowing the access to proceed. The WD7910 can trap accesses to I/O devices controlled by the following chip selects:

- Programmable Chip Select 1
- Programmable Chip Select 2
- Programmable Chip Select 3
- Serial Port A Chip Select
- Serial Port B Chip Select
- Parallel Port Chip Select

When access to an I/O device is trapped, the WD7910 asserts the SMI pin to the AM386SX. Control is transferred to the SMI handler routine which determines which I/O access caused the SMI handler to be invoked. The handler looks at Registers 7C72 and 8472 to determine the I/O address accessed and how many bytes have been read or written. If the I/O access was unaligned, up to three I/O transfers may have taken place since SMI only breaks AM386SX execution on an instruction boundary. A memory write can also occur if the AM386SX is executing a string input instruction. If unaligned, the memory write can also involve up to three transfers.

Registers 8C72 and 9472 contain either the data written to the I/O device or the memory address written while trapping a string input instruction. Using this information allows the SMI handler to reconstruct the events causing the I/O trap. The handler can then wake up the I/O device, repeat the I/O instruction, rewrite memory if needed, and finally exit to allow normal code execution to continue.

The SMI handler is located in SMI RAM. SMI RAM consists of 64 Kbytes of DRAM space taken from the top of the DRAM space specified by Register 7472. Once the SMI service routine is loaded into SMI RAM space, the SMI RAM space can be hidden from system access and remapped to SMI address space 6000:0H. The only way to access the SMI address space after remap is to put the AM80386SX in SMI mode.

Support for I/O trapping and the generation of SMI is only available on the WD7910LP.

10.2 SMI I/O TRAP CONTROL REGISTER

Port Address 7C72

15	14	13	12	11	10	09	08
LAEN	NAC1	NAC0	PCS TPE	PC2 TPE	SPA TPE	SPB TPE	PAR TPE

07	06	05	04	03	02	01	00
TRPS	IOWS	IOS2	IOS1	IOS0	MS2	MS1	MS0

Bit 15 - LAEN, Local Attention Enable (R/W)

There are three sources that can cause the Local Attention PMC output to be asserted. One is a transition on an unmasked PMC input pin (see description for registers 8872 and C872). The second is a signal from the system activity monitor (see description for registers B072 and D872). The third is a watch dog timer. These sources will also cause an SMI if LAEN is set high. The SMI is based on an internal version of Local Attention and occurs even if PMC updates are disabled.

Bit 15 = 1, Enables SMI to be caused by a Local Attention

Bit 15 = 0, Disables generation of SMI by a Local Attention (Default)

Bits 14:13 - NAC1-0, Next Address Control 1-0 (R/W)

These bits control the function of the NA output pin.

NAC1	NAC0	FUNCTION
0	0	NA is always deasserted (inactive), forcing all 386SX cycles to be nonpipelined. (default)
0	1	NA is always asserted (active), allowing the 386SX to run pipelined whenever possible.
1	0	Reserved setting. Do not use.
1	1	NA is normally asserted allowing pipelined cycles. However, NA is deasserted during T1P (pipelined cycle) or the first T2 (nonpipelined cycle) of all I/O cycles, except coprocessor cycles. NA is asserted again in the next T state unless SMI is active. This setting must be used if pipelining is allowed when I/O traps are enabled.

Bit 12 - PCSTPE, Programmable Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Programmable Chip Select (See registers 2872 and 3072).

Bit 12 = 1, Enable Trap

Bit 12 = 0, Disable Trap (Default)

Bit 11 - PC2TE, Programmable Chip Select 2 Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the second programmable chip select (see registers 5C72 and 6472). This trap occurs even if the ENPCS2 bit in register 5C72 is not set.

Bit 11 = 1, Enable Trap

Bit 11 = 0, Disable Trap (Default)

Bit 10 - SPATPE, Serial Port A Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port A Chip Select (see register 2072).

Bit 10 = 1, Enable Trap

Bit 10 = 0, Disable Trap (Default)

Bit 9 - SPBTPE, Serial Port B Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port B Chip Select (see register 2072)

Bit 9 = 1, Enable Trap

Bit 9 = 0, Disable Trap (Default)

Bit 8 - PARTPE, Parallel Port Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Parallel Port Chip Select (see register 2072).

Bit 8 = 1, Enable Trap

Bit 8 = 0, Disable Trap (Default)

Bit 7 - TRPS, Trap Status (R/Clear)

When read as a 1, this bit indicates an I/O trap has occurred. If read as a zero, then no I/O trap has occurred. The SMI handler can poll this status bit to determine if an I/O trap caused the SMI. When this bit is written as a zero, the TRPS, IORD, IOS2-0, and MS2-0 status bits are all reset to 0, readying the I/O trap state machines to capture future I/O and memory cycles. This should be done by the SMI handler each time it services an I/O trap. Writing a 1 to TRPS has no effect.

Bit 6 - IOWS, I/O Write Status (R)

This read only bit is set when the I/O cycle that caused the trap is a write operation. This tells the SMI handler that the contents of Registers 8C72 and 9472 hold the data that was written to the I/O device. This bit is cleared during reset or when TRPS is written with a 0.

Bits 5:2 - IOS2-0, I/O Address Status 2-0 (R)

These read-only bits provide information about the the I/O Cycles captured by the I/O trap (See Table 10-1). This information, along with the I/O address of the first transfer stored in Register 8472, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. These bits are cleared during reset or when TRPS is written with a 0.

Bits 2:0 - MS2-0, Memory Address Status 2-0 (R)

These read-only bits provide information about memory write cycles, if any, captured by the I/O trap (See Table 10-2). Memory write cycles will only be captured if an indivisible string input instruction is being executed. The status information from MS2-0, along with the memory address of the first transfer stored in registers 8C72 and 9472, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. These bits are cleared during reset or when TRPS is written with a 0.

10.3 SMI I/O ADDRESS CAPTURE REGISTER

Port Address 8472

15	14	13	12	11	10	09	08
CIOA 15	CIOA 14	CIOA 13	CIOA 12	CIOA 11	CIOA 10	CIOA 9	CIOA 8

07	06	05	04	03	02	01	00
CIOA 7	CIOA 6	CIOA 5	CIOA 4	CIOA 3	CIOA 2	CIOA 1	CIOA 0

Bits 15:0 - CIOA15-0, Captured I/O Address (R)

These read only bits hold the I/O address being written or read which caused the I/O trap to occur. If multiple I/O cycles were required due to an unaligned transfer, then this is the first address and may need to be adjusted as discussed in the description of the ISO2-0 bits in register 7C72. These bits are cleared during reset or when TRPS (Register 7C72) is written with a 0.

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	TRANSFER TYPE	ADJUSTMENT TO REG. 8472 TO OBTAIN ACTUAL I/O ADDRESS
0	0	0	X	None	Only occurs after a clear
0	0	1	X	16-bit	No adjustment needed
0	1	0	X	32-bit	No adjustment needed
0	1	1	X	32-bit	Subtract 2
1	0	0	X	32-bit	Subtract 1
1	0	1	X	8-bit	No adjustment needed
1	1	0	0	16-bit	Subtract 1
1	1	0	1	16-bit	No adjustment needed
1	1	1	X	32-bit	Subtract 3
X = Don't Care					

TABLE 10-1. I/O ADDRESS STATUS

10.4 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER LOW

Port Address 8C72 (R)

15	14	13	12	11	10	09	08
MAID 15	MAID 14	MAID 13	MAID 12	MAID 11	MAID 10	MAID 9	MAID 8

07	06	05	04	03	02	01	00
MAID 7	MAID 6	MAID 5	MAID 4	MAID 3	MAID 2	MAID 1	MAID 0

Bits 15:0 - MAID 15-0, Memory Address or I/O Data Bits

This read only register holds 16 bits of either the memory address being written after SMI was asserted or the I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in Register 7C72 indicates the type of data. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when TRPS (Register 7C72) is written with a 0.

When capturing the memory write address, this register holds the 16 least significant bits of the address of the first memory write cycle (register 9472 holds the eight most significant bits). More cycles will be completed if the transfer was unaligned. Status bits MS2 through 0 in register 7C72 show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds up to 16 bits of data, and Register 9472 holds the rest, if any. The data bytes may be stored in a jumbled order if it was an unaligned transfer. The format of the stored data bytes can be obtained from the IOS2-0 bits in Register 7C72 using Table 10-3.

10.5 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER HIGH

Port Address 9472 (R)

15	14	13	12	11	10	09	08
MAID 31	MAID 30	MAID 29	MAID 28	MAID 27	MAID 26	MAID 25	MAID 24

07	06	05	04	03	02	01	00
MAID 23	MAID 22	MAID 21	MAID 20	MAID 19	MAID 18	MAID 17	MAID 16

Bits 15:0 - MAID 31-16, Memory Address or I/O Data Bits

This read-only register holds either: (1) 8 bits of the memory address being written after

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	TRANSFER TYPE	ADJUSTMENT TO REG. 8C72 and 9472 TO OBTAIN ACTUAL MEMORY ADDRESS
0	0	0	X	None	No memory write cycles occurred
0	0	1	X	16-bit	No adjustment needed
0	1	0	X	32-bit	No adjustment needed
0	1	1	X	32-bit	Subtract 2
1	0	0	X	32-bit	Subtract 1
1	0	1	X	8-bit	No adjustment needed
1	1	0	0	16-bit	Subtract 1
1	1	0	1	16-bit	No adjustment needed
1	1	1	X	32-bit	Subtract 3
X = Don't Care					

TABLE 10-2. MEMORY ADDRESS STATUS

SMI is asserted; or (2) the 16 bits of I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in register 7C72 indicates the type of information. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when TRPS (register 7C72) is written with a 0.

When capturing the memory write address, MAID 23 through MAID 16 holds the eight most significant bits of the address of the first memory write cycle (register 8C72 holds the 16 least significant bits). More cycles will be done if the transfer is unaligned. Status bits MS2 through MS0 in register 7C72 show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds 16 bits of data if it is a 32-bit I/O write. Register 8C72 holds the rest of the data. See the data format description table for register 8C72.

10.6 SMI I/O TIMEOUT

As a power conservation measure, it is desirable to put some I/O peripherals to sleep when they are not in use. This may involve shutting off clocks or removing power. In order to do this, there must be a mechanism for determining that a device is not in use. In the 7910, timers are included for each I/O device that is a candidate for power reduction measures. Each timer causes an SMI when no access is made to an I/O device for a programmable amount of time. The timers are reset by I/O read or write operations to any address which falls within the range of its chip select.

When an SMI is generated, the SMI handler takes whatever action is appropriate to power down the I/O peripheral. The handler then enables the I/O trap for that device so that it can be awakened the next time it is accessed.

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	DATA SIZE	REGISTER 9472 HI BYTE	REGISTER 9472 LO BYTE	REGISTER 8C72 HI BYTE	REGISTER 8C72 LO BYTE
0	0	0	X	None				
0	0	1	X	16-bit			B1	B0
0	1	0	X	32-bit	B3	B2	B1	B0
0	1	1	X	32-bit	B1	B0	B3	B2
1	0	0	X	32-bit	B0	B3	B2	B1
1	0	1	0	8-bit			-	B0
1	0	1	1	8-bit			B0	-
1	1	0	X	16-bit			B0	B1
1	1	1	X	32-bit	B2	B1	B0	B3

Where:
B0 = least significant byte
B1 = next most significant byte (MSB for 16-bit data)
B2 = next most significant byte (32-bit data only)
B3 = most significant byte (32-bit data only)
X = Don't Care

TABLE 10-3. MEMORY ADDRESS OR I/O DATA CAPTURE

10.7 SMI I/O TIMEOUT CONTROL REGISTER

Port Address 9C72

15	14	13	12	11	10	09	08
FSMI	PCS ADS	PC2 ADS	SPA ADS	SPB ADS	PAR ADS	PCS TOS	PC2 TOS

07	06	05	04	03	02	01	00
SPA TOS	SPB TOS	PAR TOS	PCS TOE	PC2 TOE	SPA TOE	SPB TOE	PAR TOE

Bit 15 - FSMI, Force SMI (R/W)

This bit provides a means to invoke the SMI handler through software. When this bit is set to 1, the SMI pin is asserted. FSMI should be cleared by the SMI handler before it exits to prevent another SMI.

Bit 15 = 1, Force SMI Enable

Bit 15 = 0, Force SMI Disable (Default)

Bit 14 - PCSADS, Programmable Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the programmable chip select I/O address range has been accessed since PCSTOS was set. If PCSADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PCSADS is cleared by reset or when PCSTOE is cleared.

Bit 13 - PC2ADS, Programmable Chip Select 2 Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the second Programmable Chip Select's I/O address range has been accessed since PC2TOS was set. If PC2ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PC2ADS is cleared by reset or when PC2TOE is cleared.

Bit 12 - SPAADS, Serial Port A Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the Programmable Chip Select's I/O address range has been accessed since SPATOS was set. If SPAADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPAADS is cleared by reset or when SPATOE is cleared.

Bit 11 - SPBADS, Serial Port B Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the Programmable Chip Select's I/O address range has been accessed since SPBTOS was set. If SPBADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPBADS is cleared by reset or when SPBTOE is cleared.

Bit 10 - PARADS, Parallel Port Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the programmable chip select I/O address range has been accessed since PARTOS was set. If PARADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PARADS is cleared by reset or when PARTOE is cleared.

Bit 9 - PCSTOS, Programmable Ship Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Programmable Chip Select I/O address range. It can be polled by the SMI handler to determine the source of the SMI. PCSTOS is cleared by reset or when PCSTOE is cleared.

Bit 8 - PC2TOS, Programmable Chip Select 2 Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the second programmable chip select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC2TOS is cleared by reset or when PC2TOE is cleared.

Bit 7 - SPATOS, Serial Port A Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Serial Port A Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. SPATOS is cleared by reset or when SPATOE is cleared.

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Bit 6 - SPBTOS, Serial Port B Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Serial Port B Chip Select's I/O address range. It can be polled by the SMI handler in determining the source of the SMI. SPBTOS is cleared by reset or when SPBTOE is cleared.

Bit 5 - PARTOS, Parallel Port Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Parallel Port Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PARTOS is cleared by reset or when PARTOE is cleared.

Bit 4 - PCSTOE, Programmable Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Programmable Chip Select I/O address range. When written with a 0, this bit disables programmable chip select timeouts and clears PCSTOS.

Bit 4 = 1, Timeout Enable

Bit 4 = 0, Timeout Disable (Default)

Bit 3 - PCSTOE, Programmable Chip Select 2 Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the second Programmable Chip Select I/O address range. When written with a 0, this bit disables programmable chip select 2 timeouts and clears PC2TOS.

Bit 3 = 1, Timeout Enable

Bit 3 = 0, Timeout Disable (Default)

Bit 2 - SPATOE, Serial Port A Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Serial Port A Chip Select I/O address range. When written with a 0, this bit disables serial port A chip select timeouts and clears SPATOS.

Bit 2 = 1, Timeout Enable

Bit 2 = 0, Timeout Disable (Default)

Bit 1 - SPBTOE, Serial Port B Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Serial Port B Chip Select I/O address range. When written with a 0, this bit disables serial port B chip select timeouts and clears SPBTOS.

Bit 1 = 1, Timeout Enable

Bit 1 = 0, Timeout Disable (Default)

Bit 0 - PARTOE, Parallel Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Parallel Port Chip Select I/O address range. When written with a zero, this bit disables parallel port chip select timeouts and clears PARTOS.

Bit 0 = 1, Timeout Enable

Bit 0 = 0, Timeout Disable (Default)

10.8 SMI I/O TIMEOUT COUNT REGISTER 1

Port Address A472

15	14	13	12	11	10	09	08
SMI WUE	PCS TC4	PCS TC3	PCS TC2	PCS TC1	PCS TC0	PC2 TC4	PC2 TC3

07	06	05	04	03	02	01	00
PC2 TC2	PC2 TC1	PC2 TC0	SPA TC4	SPA TC3	SPA TC2	SPA TC1	SPA TC0

Bit 15 - SMIWUE, SMI Wake Up Enable (R/W)

This bit, when set to a 1, causes the assertion of SMI to wake up the processor from a powerdown or stop clock state. An INTR, NMI, or DMA request continues to wake up the processor as in the WD76C10, regardless of the state of this bit. Note that setting this bit does not enable SMI to initiate a resume from suspend.

Bit 15 = 1, Enable SMI Wakeup

Bit 15 = 0, Disable SMI Wakeup (Default)

Bits 14:10 - PCSTC 4-0, Programmable Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select PCSTCS (Register AC72), determine the time period during which an I/O peripheral

(selected by the Programmable Chip Select) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PCSTCS = 0, (Count in PCSTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PCSTCS = 1, (Count in PCSTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 9:5 - PC2TC 4-0, Programmable Chip Select 2 Timeout Count (R/W)

These bits, along with the timeout clock select PC2TCS (Register AC72), determine the time period during which an I/O peripheral (selected by Programmable Chip Select 2) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PC2TC = 0, (Count in PC2TC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC2TC = 1, (Count in PC2TC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 4:0 - SPATC4-0, Serial Port A Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select SPATCS (Register AC72), determine the time period during which Serial Port A must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

SPATCS = 0, (Count in SPATC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPATCS = 1, (Count in SPATC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

10.9 SMI I/O TIMEOUT COUNT REGISTER 2

Port Address AC72

15	14	13	12	11	10	09	08
IOT CTM	SPB TC4	SPB TC3	SPB TC2	SPB TC1	SPB TC0	PAR TC4	PAR TC3

07	06	05	04	03	02	01	00
PAR TC2	PAR TC1	PAR TC0	PCS TCS	PC2 TCS	SPA TCS	SPB TCS	PAR TCS

Bit 15 - IOTCTM, I/O Timeout Counter Test Mode (R/W)

This bit, when written as a 1, puts the timeout counters into test mode. For factory use only.

Bits 14:10 - SPBTC4-0, Serial Port B Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select SPBTCS (Register AC72), determine the time period during which Serial Port B must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

SPBTCS = 0, (Count in SPBTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPBTCS = 1, (Count in SPBTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 9:5 - PARTC4-0, Parallel Port Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select PARTCS (Register AC72), determine the time period during which the parallel port must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PARTCS = 0, (Count in PARTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PARTCS = 1, (Count in PARTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bit 4 - PCSTCS, Programmable Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Programmable Chip Select Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PCSTC4-0 (Register A472) for more details. Default after reset is 0.

Bit 3 - PC2TCS, Programmable Chip Select 2 Timeout Clock Select (R/W)

This bit selects the clock to be used for the second Programmable Chip Select Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PC2TC4-0 (Register A472) for more details. Default after reset is 0.

Bit 2 - SPATCS, Serial Port A Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Serial Port A Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPATC4-0 (Register A472) for more details. Default after reset is 0.

Bit 1 - SPBTCS, Serial Port B Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Serial Port B Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 seconds timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPBTC4-0 (Register A472) for more details. Default after reset is 0.

Bit 0 - PARTCS, Parallel Port Chip Select Timeout Clock Select

This bit selects the clock to be used for the Parallel Port Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 seconds timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PARTC4-0 (Register A472) for more details. Default after reset is 0.

10.10 SMI AUXILIARY CONTROL REGISTER

Port 5472

15	14	13	12	11	10	09	08
TOM SK	7910	WDO GEN	WDO GS	PCS 3M	PCS 2M	PC3 TPE	PC3 TOE

07	06	05	04	03	02	01	00
PC3 TOS	PC3 ADS	PC3 TC4	PC3 TC3	PC3 TC2	PC3 TC1	PC3 TC0	PC3 TCS

Bit 15 - TOMSK, Timeout Mask (R/W)

When set to one, TOMSK masks I/O device timeouts from causing assertion of the SMI output. The I/O device timers continue to count down, if enabled, and, if a timeout occurs, the SMI

output is asserted after TOMSK is cleared. Also, when TOMSK is set, the I/O device timers will not detect I/O activity, thus preventing the timer from being reset.

Bit 14 - 7910 (R)

This read only bit is set to 1 if the device is a WD7910 or WD7910LP. It is set to 0 if the device is a WD7710 or WD7710LP.

Bit 13 - WDOGEN, Watchdog Timer Interrupt Enable (R/W)

This bit, when set to a 1, enables a periodic interrupt to be generated every 125 ms. Each interrupt causes LCL_ATN to be set, so that it is useful both with or without SMI suppport. The interrupt is cleared either by writing WDOGST with a zero or by writing WDOGEN with a zero to disable further watchdog interrupts. Note that the first interrupt after the watchdog timer is enabled can occur anytime from 62.5 ms to 125 ms later.

Bit 12 - WDOGS, Watchdog Timer Interrupt Status (Read/Clear)

This bit is read as a 1 when LCL_ATN has been set due to a Watchdog Timer Interrupt Request. WDOGST is cleared by writing it with a zero, although the watchdog timer continues to run and will set WDOGST at 125 ms intervals. WDOGST is also cleared when WDOGEN is set to a zero. Writing WDOGST with a 1 has no effect.

Bit 11 - PCS3M, Programmable Chip Select 3 Mask (R/W)

This bit is an extension to register D872. When zero, PCS3M allows I/O accesses to the third Programmable Chip Select address range (see registers 5C72 and 6C72) to be observed as a source of activity by the system activity monitor. When set, it masks I/O accesses to the third Programmable Chip Select from being seen by the system activity monitor. Note that the setting of ENPCS3 in register 5C72 has no effect on I/O activity detection.

Bit 10 - PCS2M, Programmable Chip Select 2 Mask (R/W)

This bit is an extension to register D872. When set to 0, PCS2M allows I/O accesses to the second Programmable Chip Select address range (see registers 5C72 and 6472) to be observed as a source of activity by the system activity monitor. When set, it masks I/O accesses to the second Programmable Chip Select from being seen by the system activity monitor. Note that the setting of ENPCS2 in register 5C72 has no effect on I/O activity detection.

Bit 9 - PC3TPE, Programmable Chip Select 3 Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the third Programmable Chip Select (see registers 5C72 and 6C72). This trap occurs even if the ENPCS3 bit in register 5C72 is not set.

Bit 8 - PC3TOE, Programmable Chip Select 3 Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the third Programmable Chip Select I/O address range. The timeout count will be reset by I/O to the Programmable Chip Select 3 address range even if the ENPCS3 bit in register 5C72 is not set. When written with a 0, PC3TOE disables Programmable Chip Select 3 timeouts and clears PC3TOS.

Bit 7 - PC3TOS, Programmable Chip Select 3 Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the third Programmable Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC3TOS is cleared by reset or when PC3TOE is cleared.

Bit 6 - PC3ADS, Programmable Chip Select 3 Activity Detect Status (R)

This bit can be polled by the SMI Handler to see if the third Programmable Chip Select I/O address range has been accessed since PC3TOS was set. If PC3ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI Handler would ignore the timeout and restart the timeout counter. PC3ADS is cleared by reset or when PC3TOE is cleared.

Bit 5:1 - PC3TC4-0, Programmable Chip Select 3 Timeout Count (R/W)

These bits, along with the timeout clock select PC3TCS, determine the time period during which an I/O peripheral (selected by Programmable Chip Select 3) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PC3TCS = 0, (Count in PC3TC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC3TCS = 1, (Count in PC3TC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bit 0 - PC3TCS, Programmable Chip Select 3 Timeout Clock Select (R/W)

This bit selects the clock to be used for the third Programmable Chip Select timeout counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PC3TC4-0 for more details.

10.11 PROGRAMMABLE CS2 AND CS3 CONTROL REGISTER

Port 5C72

15	14	13	12	11	10	09	08
PCS 2L	ENP CS2	UMS K2	2LM SK4	2LM SK3	2LM SK2	2LM SK1	2LM SK0

07	06	05	04	03	02	01	00
PCS 3L	ENP CS3	UMS K3	3LM SK4	3LM SK3	3LM SK2	3LM SK1	3LM SK0

Bit 15 - PCS2L, Programmable Chip Select 2 Location (R/W)

When this bit is set to a 1, the I/O device selected by the second Programmable Chip Select is located on the expansion bus. When this bit is low, the device is located on the RA0-7/ED0-7 bus.

Bit 14 - ENPCS2, Enable Programmable Chip Select 2 (R/W)

When this bit is set to a 1, the second Programmable Chip Select is enabled. When set to a 0, the second Programmable Chip Select is not enabled.

Bit 13 - UMSK2, Upper Address Bits Mask 2 (R/W)

When this bit is set to a 1, then A15 through A10 from register 6472 are compared against CPU address Bits 15 through 10 when qualifying the second programmable chip select. When UMSK2 is set to a 0, then Bits A15 through A10 are ignored.

Bits 12:8 - 2LMSK4-0, Programmable CS2 Lower Address Bits MASK 4-0 (R/W)

These mask bits allow individual qualification of the lower five address bits in register 6472. When a mask bit is set to 1, the corresponding bit in register 6472 is compared against that CPU address bit. When a mask bit is set to 0, the corresponding bit in register 6472 is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (2LMSK4-0 would all be zeroes), as well as unusual requirements such as odd addresses only.

Bit 7 - PCS3L, Programmable Chip Select 3 Location (R/W)

When this bit is set to a 1, the I/O device selected by the third Programmable Chip Select is located on the expansion bus. When this bit is low, the device is located on the RA0-7/ED0-7 bus.

Bit 6 - ENPCS3, Enable Programmable Chip Select 3 (R/W)

When this bit is set to a 1, the third Programmable Chip Select is enabled. When set to a 0, the third Programmable Chip Select is not enabled.

Bit 5 - UMSK3, Upper Address Bits Mask 3 (R/W)

When this bit is set to a 1, then A15 through A10 from register 6C72 are compared against CPU address bits 15 through 10 when qualifying the third Programmable Chip Select. When UMSK3 is set to a zero, then Bits A15 through A10 are ignored.

Bits 4:0 - 3LMSK4-0, Programmable CS3 Lower Address Bits Mask (R/W)

These mask bits allow individual qualification of the lower five address bits in Register 6C72. When a mask bit is set to 1, the corresponding bit in Register 6C72 is compared against that CPU address bit. When a mask bit is set to 0, the corresponding bit in Register 6C72 is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (3LMSK4-0 would all be zeroes), as well as unusual requirements such as odd addresses only.

10.12 PROGRAMMABALE CS2 ADDRESS REGISTER

Port 6472

15	14	13	12	11	10	09	08
PC2 A15	PC2 A14	PC2 A13	PC2 A12	PC2 A11	PC2 A10	PC2 A9	PC2 A8

07	06	05	04	03	02	01	00
PC2 A7	PC2 A6	PC2 A5	PC2 A4	PC2 A3	PC2 A2	PC2 A1	PC2 A0

Bits 15:0 - PC2A15-0, Programmable Chip Select 2 Address (R/W)

These bits determine the base address of the I/O device corresponding to the second programmable chip select. Register 5C72 provides the enable for Programmable Chip Select 2 and allows selective masking of some of the address bits.

10.13 PROGRAMMABLE CS3 ADDRESS REGISTER (R/W)

Port 6C72

15	14	13	12	11	10	09	08
PC3 A15	PC3 A14	PC3 A13	PC3 A12	PC3 A11	PC3 A10	PC3 A9	PC3 A8

07	06	05	04	03	02	01	00
PC3 A7	PC3 A6	PC3 A5	PC3 A4	PC3 A3	PC3 A2	PC3 A1	PC3 A0

Bits 15:0 - PC3A15-0, Programmable Chip Select 3 Address (R/W)

These bits determine the base address of the I/O device corresponding to the third Programmable Chip Select. Register 5C72 provides the enable for Programmable Chip Select 3 and allows selective masking of some of the address bits.

10.14 DRAM SIZE AND SMI RAM REGISTER

Port Address 7472

15	14	13	12	11	10	09	08
Bank 3	Bank 2	Bank 1	Bank 0				SMI_R ENB

07	06	05	04	03	02	01	00
SMI_RAM							

This register is used to set up the starting address of the SMI DRAM and support extra DRAM types.

Bits 15:12 - DRAM Type

These four bits are used with Bits 7:0 of Register 3872 to determine the DRAM sizes.

Bit 15 is the MSB of DRAM size for bank 3

Bit 14 is the MSB of DRAM size for bank 2

Bit 13 is the MSB of DRAM size for bank 1

Bit 12 is the MSB of DRAM size for bank 0

See Section 6.2, Memory Configuration.

Bits 11:10, Reserved

These bits should be programmed to zero.

Bit 9 - HSRPD, Holdoff SMI When Reset Pending Disable (R/W)

When HSRPD is set to 0, then all SMI sources, except I/O traps, are held off whenever a reset-pending condition is detected. The sources remain active internally, but do not cause the SMI output to be asserted until the reset-pending condition is cleared. When HSRPD is set to a 1, the reset pending condition does not gate off the assertion of SMI. Reset pending is defined as: (1) Port 92 reset pending; or (2) KB controller ports 60 or 64 have been written within the last 14 µs or (3) the CPU is in a halt state.

Bit 9 = 1, SMI is not held off.

Bit 9 = 0, SMI is held off when reset is pending (Reset default).

Bit 8, SMI RAM Enable

Setting this bit enables the SMI RAM remapping and protection. The system BIOS should load the SMI service routine into the SMI RAM before setting this bit.

Bit 8 = 0, SMI RAM disable (default)

Bit 8 = 1, SMI RAM enable

Bits 7:0, SMI RAM Starting Address

These bits determine the physical location of the SMI DRAM. These are also used to read/write protect the SMI RAM when the SMI RAM Enable bit is set.

11.0 DIAGNOSTIC MODE

Simultaneously asserting MASTER, MEMR and MEMW while RSTIN is asserted, causes all output pins to become tristated. The outputs remain tristated if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted and any of the MASTER, MEMR or MEMW are not asserted. The output tristate mode allows an in-circuit board tester to drive the WD7910's output pins.

I/O Pin Mapping Mode

The I/O Pin Mapping Mode provides the in-circuit tester for evaluating the connectivity of the WD7910 to the printed circuit board. Simultaneously asserting MASTER, MEMR, MEMW when A1 is high, A2 is low, and RSTIN is asserted, causes the WD7910 to switch to I/O Mapping Mode. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR, and MEMW are asserted.

Full Tristate Mode

Simultaneously asserting MASTER, MEMR, and MEMW with A1 low and A2 high while RSTIN is asserted, causes all the output pins of the WD7910 to tristate and disablesall the pullup and pulldown register. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test for leakage current of the device.

Pullup and Pulldown Test Mode

Simultaneously asserting MASTER, MEMR, MEMW with A1 and A2 high while RSTIN is asserted, causes all the output pins of the WD7910 to become tristated and enables all the pullup and pulldown resistors. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test the pullup and pulldown resistors of the device.

11.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

15	14	13	12	11	10	09	08
RSVD			CLK_ TST	REF_ MAS	AUT_ A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
AUT_A20	0
Bit 09	None
CLK_SW	0
SX	None
DS	0
DIAG	0-0

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - AUT_A20, Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

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The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 9-1).

AUT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

AUT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX Processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, Diagnostic Function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 11-2. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	Reserved
00010	Reserved	10010	Reserved
00011	Reserved	10011	Reserved
00100	Reserved	10100	Reserved
00101	Reserved	10101	Reserved
00110	Reserved	10110	Reserved
00111	Reserved	10111	Reserved
01000	Reserved	11000	Reserved
01001	Reserved	11001	Reserved
01010	Reserved	11010	Reserved
01011	Reserved	11011	Reserved
01100	Reserved	11100	Reserved
01101	Reserved	11101	Reserved
01110	Reserved	11110	Reserved
01111	Reserved	11111	Reserved

TABLE 11-1. DIAGNOSTIC TESTS

11.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default RSTIN
Bits 15-08	None
LAT	0
DL	0
DELAY	None

Bit 07 - LAT, Latch Output Strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

11.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15-10 Read only
Bits 09-00 Read and Write

The test function bits 07-03 are for factory use only.

15	14	13	12	11	10	09	08
SVER				BF40	BC40	IRQ9 EN	TDL

07	06	05	04	03	02	01	00
OLD IHLD	BFC 3	BIST 3	BFC 40	BIST 40	EN_ PLD	DISFA	EN_ LVL

Signal Name	Default At RSTIN
All signals	0-0

Bits 15-12 - SVER, Secondary Version Number.

See VER at Port Address 9872H.

PORT ADDRESS D472H DEVICE - Bits 14, 13			PORT ADDRESS A872H SECONDARY VERSION - Bits 15-12				
14	13	Device	15	14	13	12	Rev
0	0	WD76C10	0	0	0	0	A
0	1	WD7710/7910	0	0	0	1	B
1	0	Reserved	0	0	1	0	C
1	1	Reserved	-	-	-	-	-
			1	1	1	1	P

Bit 11 - BF40, EMS Register Self Test Status

Bit 10 - BC40, EMS Register Self Test Status

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Bit 09 - IRQ9EN = 0, Masks IRR9 and ISR9 so that the System Activity Monitor does not detect these signals. This prevents vertical retrace from being a source of activity for SAM.

IRQ9EN = 0 ,
Masking of IRR9 and ISR9 enabled

IRQ9EN = 1,
Masking disabled

Bit 08 - TDL, Test Delay Line.

Bit 07 - OLD_IHLD,

OLD_IHLD = 0 -
SX test not enabled

OLD_IHLD = 1 -
SX test enabled

Bit 06 - BFC3,

BFC3 = 0 -
DMA register file test

BFC3 = 1 -
DMA register file test

Bit 05 - BIST3,

BIST3 = 0 -
DMA register file test

BIST3 = 1 -
DMA register file test

Bit 04 - BFC40,

BFC40 = 0 -EMS mapping RAM

BFC40 = 1 -EMS mapping RAM

Bit 03 - BIST40,

BIST40 = 0 -
EMS mapping RAM

BIST40 = 1 -
EMS mapping RAM

Bit 02 - EN_PLD, Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23 through A00, and on processor data lines D15 through D00.

Bit 01 - DISFA, Disable First Access

DISFA = 0 -
First access Page Mode cycles are not disabled.

DISFA = 1 -
First access Page Mode cycles are disabled. Page Miss cycles occur instead.

Bit 00 - EN_LVL, Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of edge-sensed or level-sensed interrupts.

11.4 TEST STATUS REGISTER

Port Address DC72H - Read only

For factory use only.

15	14	13	12	11	10	09	08
Delay Line Status CAL	MED	SLOW	DLT6	DLT5	DLT4	DLT3	DLT2

07	06	05	04	03	02	01	00
DLT1	DLT0	BF34	BF33	BF32	BF31	BF30	BC

Signal Name	Default RSTIN
All signals	None

Bit 15 - CAL, Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

Bits 14, 13 - MED, SLOW, Medium and Slow

These bits provide information regarding the output buffer strength.

MEDIUM	SLOW	
0	0	Output buffers are set to low strength (fast WD7910/7910LP).
0	1	Invalid
1	0	Output buffers are set to medium strength (medium speed WD7910/7910LP).
1	1	Output buffers are set to full strength (slow WD7910/7910LP).

Bits 12-06 - DLT6-DLT0,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

Bits 05-01 - BF34-BF30,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

Bit 00 - BC

This bit provides information about internal nodes and are for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

8

12.0 DC ELECTRICAL SPECIFICATIONS

12.1 MAXIMUM RATINGS

Supply Voltage (Vcc) with respect to Vss (ground) . . . . . Vcc - Vss ≤ 7.0 Volts

Voltage on any pin with respect to Vss (ground) . . . . . Vss -0.3 Volts to Vdd +0.3 Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -40°C (-40°F) to 125°C (257°F)

Power Dissipation . . . . . 600 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

12.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
Vcc = +5V ±.25V (5%) for WD7910 and WD7910LP

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tristate And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD7910LP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 12-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend and resume mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

M/IO, PEACK, NPERR, NPBUSY, S0, S1, NPRST, CPURES, DPH, DPL

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not processor down or suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

PMCIN, IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, BHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

CASL3, CASL2, CASH3, SDT/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	RESET IN = 0

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR PINS WITH INTERNAL PULLDOWNS:

A23-A0, D15-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current	-30	-110	µA	Processor power down or suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, $\overline{\text{READY}}$, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, $\overline{\text{BHE}}$, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage		.4	V	IOUT = 2 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage		.4	V	IOUT = 4 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

$\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:

$\overline{\text{REFRESH}}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

13.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into three major categories: Memory Timing (Section 13.1), AT Bus Timing (Section 13.2), Processor Timing (Section 13.3), and Cache Controller Timing (Section 13.4).

Table 13-1 lists the timing tables and figures, and their section location.

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
13-3		80286 - Page Mode Memory Timing	13.1.1
	13-1	80286 - Page Mode First Access Read/Write	13.1.1
	↕		
	13-6	80286 - Page Mode Read Hit Followed By Write Hit	13.1.1
13-4		80286 - Non-Page Mode 00 Memory Timing	13.1.2
	13-7	80286 - Non-Page Mode 00 1 Wait State Write	13.1.2
	13-8	80286 - Non-Page Mode 00 1 Wait State Read	13.1.2
	13-9	80286 - Non-Page Mode 00 2 Wait States Read After Write	13.1.2
13-5		80286 - Non-Page Mode 01 Memory Timing	13.1.3
	13-10	80286 - Non-Page Mode 01 0 Wait State Write	13.1.3
	13-11	80286 - Non-Page Mode 01 0 Wait State Read	13.1.3
13-6		80386SX - Page Mode Memory Timing	13.1.4
	13-12	80386SX - Page Mode, First Access Read/Write	13.1.4
	↕		
	13-17	80386SX - Page Mode, Write Miss Following A Write	13.1.4
13-7		80386SX - Non-Page Mode 00 And Mode 01	13.1.5
	13-18	80386SX - Non-Page Mode 00 1 Wait State Read	13.1.5
	↕		
	13-21	80386SX - Non-Page Mode 00 1 Wait State Read	13.1.5
13-8		CPU Initiated AT Bus Cycles	13.2.1
	13-22	AT Bus I/O Or Memory Read: 8-Bit, Default Timing	13.2.1
	↕		
	13-31	AT Bus I/O Or Memory Write: 16-Bit, Default Timing	13.2.1
13-9		Entering The AT Bus	13.2.2
	13-32	80286 CPU - Asysnchronous CPUCLK To SYSCLK, BREQ Delay = 1/2 Clock	13.2.2
	↕		
	13-37	80386SX CPU - Synchronous CPUCLK To SYSCLK	13.2.2
13-10		Exiting The AT Bus	13.2.3
	13-38	Synchronous AT Bus Cycle Completion, AT Bus Clock = 1/2 CPUCLK	13.2.3
	↕		
	13-41	Asynchronous AT Bus Cycle Completion, BAK_DEL = 0 Or +0.5 AT Bus Cycles	13.2.3
13-11		DMA Entering And Exiting The AT Bus	13.2.4
	13-42	Basic DMA Cycle, Default Timing	13.2.4
	13-43	DMA Cycle, 8-Bit I/O To On-board Memory	13.2.4
	13-44	DMA Cycle, On-board Memory To 8-Bit I/O	13.2.4
13-12		AT Bus Master Cycle	13.2.5
	13-45	AT Bus Master, Bus Acquisition/Release	13.2.5
	13-46	AT Bus Master, Write To On-board Memory	13.2.5
	13-47	AT Bus Master, Read From On-board Memory	13.2.5
13-13		AT Bus Refresh Cycle, Default Timing	13.2.5
	13-48	AT Bus Refresh Cycle, Default Timing	13.2.5

TABLE 13-1. TIMING FIGURE/TABLE NUMBERS

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
13-14		80286 CPU TIMING	13.3
	13-49	80286 - CPURES AND NPRST DURING POWER UP	13.3
	↕		
	13-54	80286 - MISCELLANEOUS TIMING	13.3
13-15		80386SX CPU TIMING	13.3
	13-55	80386SX - CPURES AND NPRST DURING POWER UP	13.3
	↕		
	13-62	80386SX - OUTPUT DELAY TIMING	13.3

TABLE 13-1. TIMING FIGURE/TABLE NUMBERS cont.

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
CPURES	50 pF	NPRST	50 pF	$\overline{BHE}$	50 pF
W/$\overline{R}$	50 pF	ALE	50 pF	$\overline{DEN1}$, $\overline{DEN0}$	50 pF
$\overline{SDEN}$	50 pF	DT/$\overline{R}$	50 pF	$\overline{SDT/R}$	50 pF
MXCTL2 - 0	50 pF	DACKEN	50 pF	$\overline{CSEN}$	50 pF
$\overline{LOMEG}$	50 pF	SPKR	50 pF	$\overline{READY}$	50 pF
HOLD	50 pF	INTRQ	50 pF	NMI	50 pF
$\overline{BUSYCPU}$	50 pF	EPEREQ	50 pF	A23 - A0	60 pF
CPUCLK	70 pF	SYSCLK	75 pF	$\overline{CASH3}$ - $\overline{0}$	75 pF
$\overline{CASL3}$ - $\overline{0}$	75 pF	D15 - D0	100 pF	DPH	100 pF
DPL	100 pF	$\overline{RAS3}$ - $\overline{RAS0}$	150 pF	$\overline{IOW}$	200 pF
$\overline{IOR}$	200 pF	$\overline{MEMW}$	200 pF	$\overline{MEMR}$	200 pF
LA20	200 pF	SA0	200 pF	AEN	200 pF
BALE	200 pF	$\overline{REFRESH}$	200 pF	RA10 - RA0	350 pF

TABLE 13-2. SIGNAL LOADING

13.1 MEMORY TIMING

Sections 13.1.1 through 13.1.5 present the memory timing for Page Mode and Non-Page Mode, for the 80286 and 80386SX processors.

Categories are grouped as follows:

80286
- Page Mode
- Non-Page Mode 00
- Non-Page Mode 01

80386SX
- Page Mode
- Non-Page Mode 00 and 01

Mnemonics used in the timing diagrams and tables are defined as:

TC - Command Cycle
TW - Wait State Cycle
TS - Status Cycle
WNRDRAM - Write Not Read DRAM (W/$\overline{R}$ pin 119).

13.1.1 80286 Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T220	Processor address to RAM address valid, Page Hit	32	30
T221	CPUCLK fall to $\overline{CAS}$ fall, 2.5 CLK CAS	36	34
T222	CPUCLK rise to $\overline{CAS}$ rise	29	27
T223	CPUCLK rise to $\overline{CAS}$ fall, 2.0 CLK CAS	30	26
T224	Processor data to parity valid	25	22
T225	CPUCLK fall to RAM address valid, Page Miss	39	36
T226	CPUCLK fall to WNRDRAM rise	34	31
T227	CPUCLK rise to $\overline{RAS}$ fall, first access	28	26
T228	CPUCLK fall to column address valid	44	41
T229	CPUCLK fall to WNRDRAM fall	34	31
T232	CPUCLK fall to $\overline{RAS}$ rise, Page Miss	29	27
T233	CPUCLK rise to $\overline{RAS}$ fall, Page Miss	28	26
T234	CPUCLK rise to $\overline{READY}$ rise	24	22
T235	CPUCLK rise to READY fall	24	22

TABLE 13-3. 80286 - PAGE MODE MEMORY TIMING

8

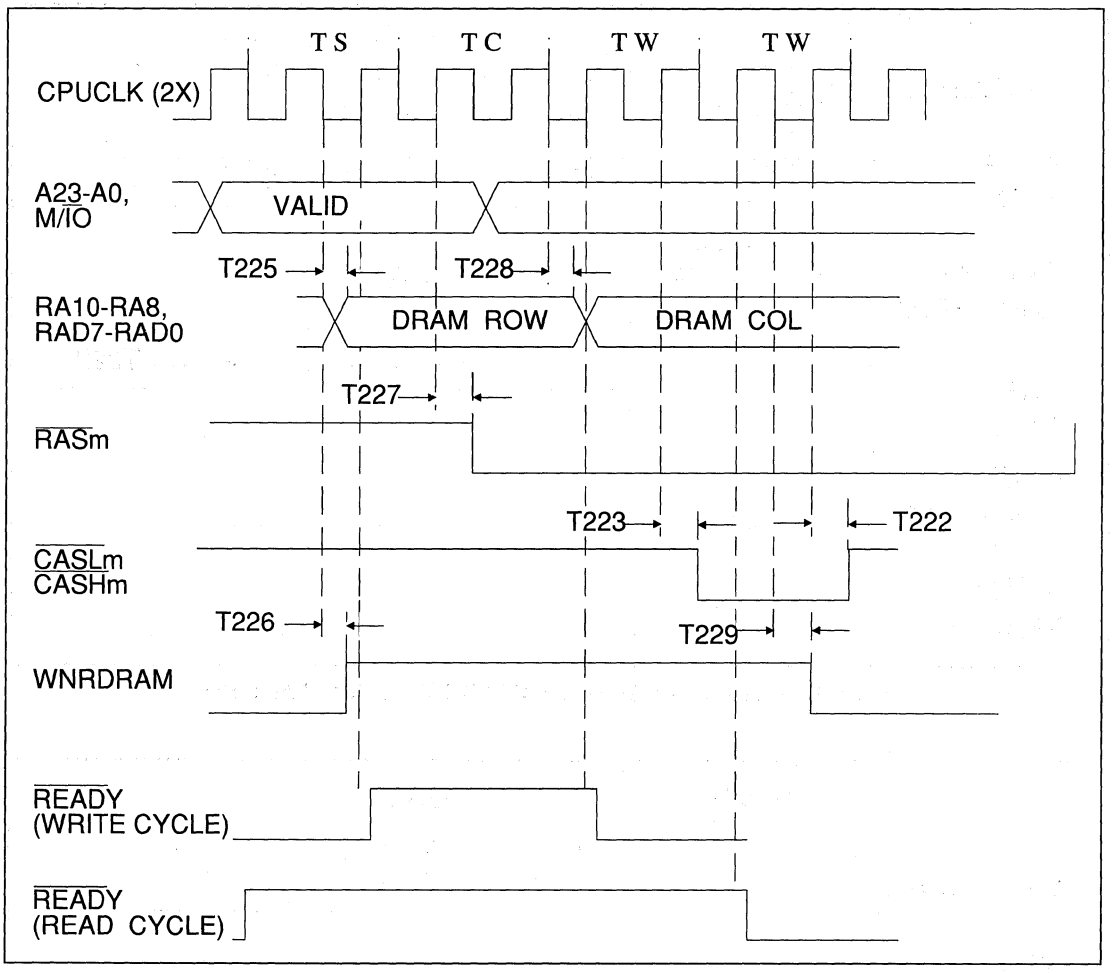


FIGURE 13-1. 80286 - PAGE MODE FIRST ACCESS READ/WRITE

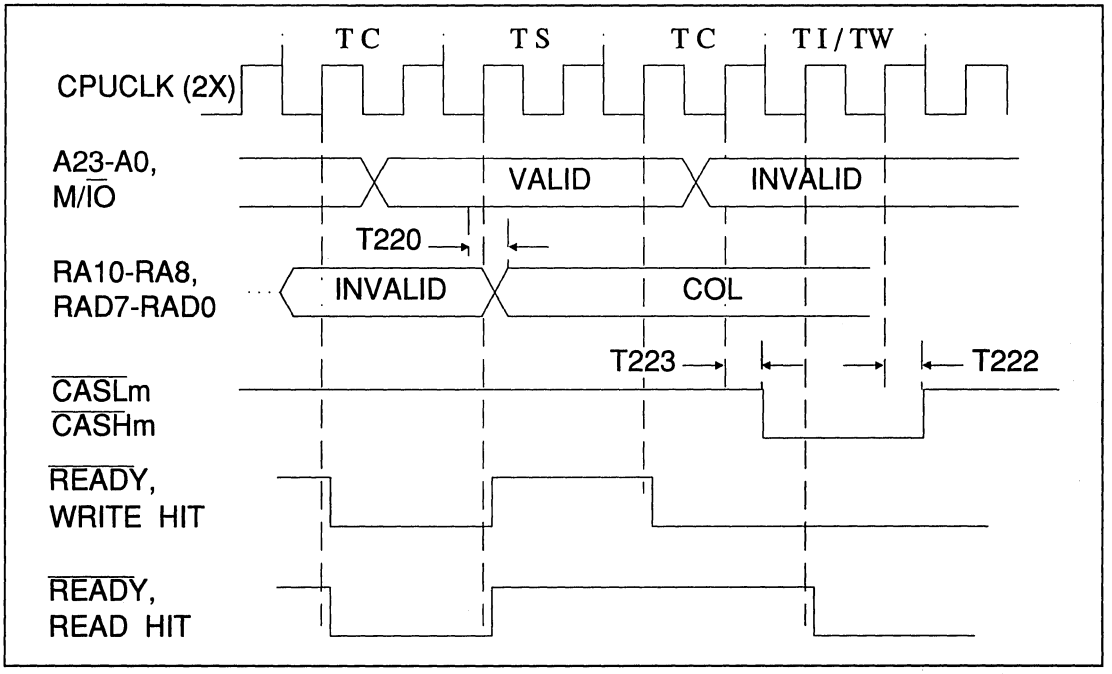


FIGURE 13-2. 80286 - PAGE MODE READ CYCLE AND PAGE HIT

8

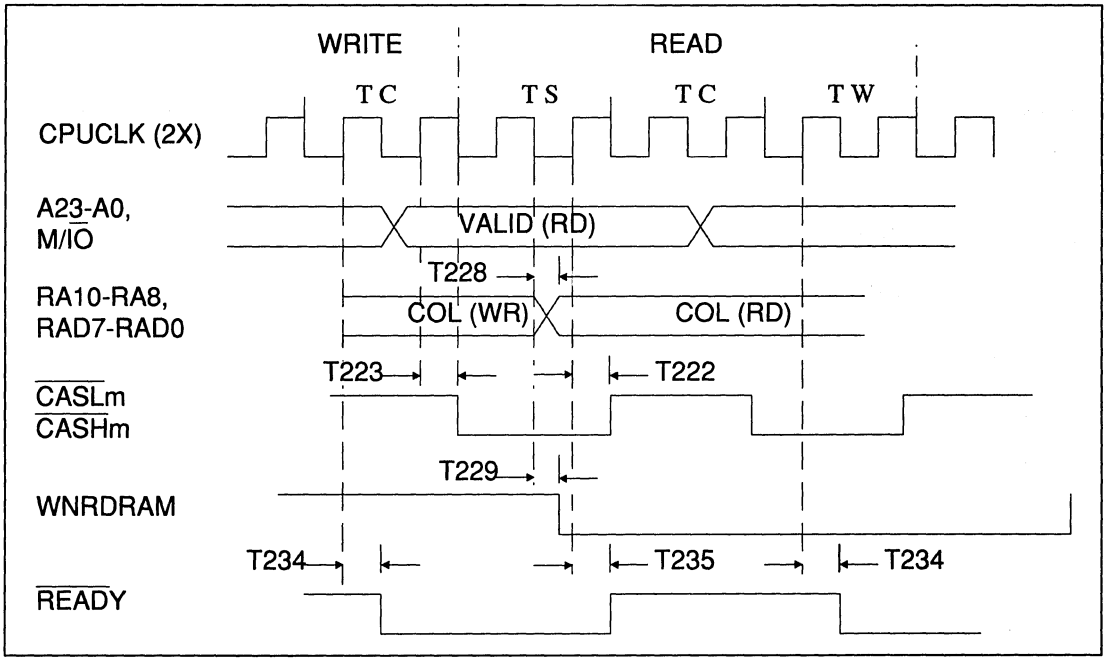


FIGURE 13-3. 80286 - PAGE MODE READ AFTER WRITE

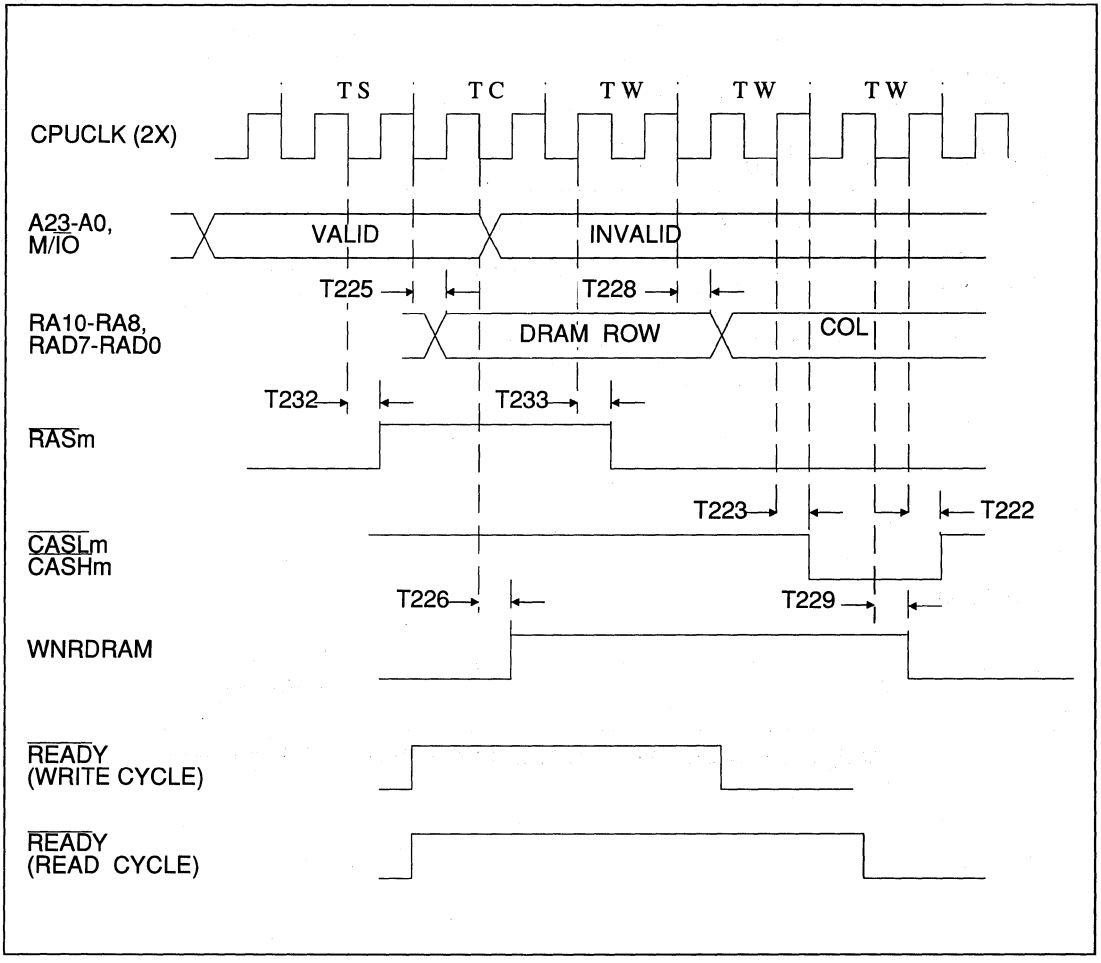


FIGURE 13-4. 80286 - PAGE MODE, PAGE MISS READ/WRITE

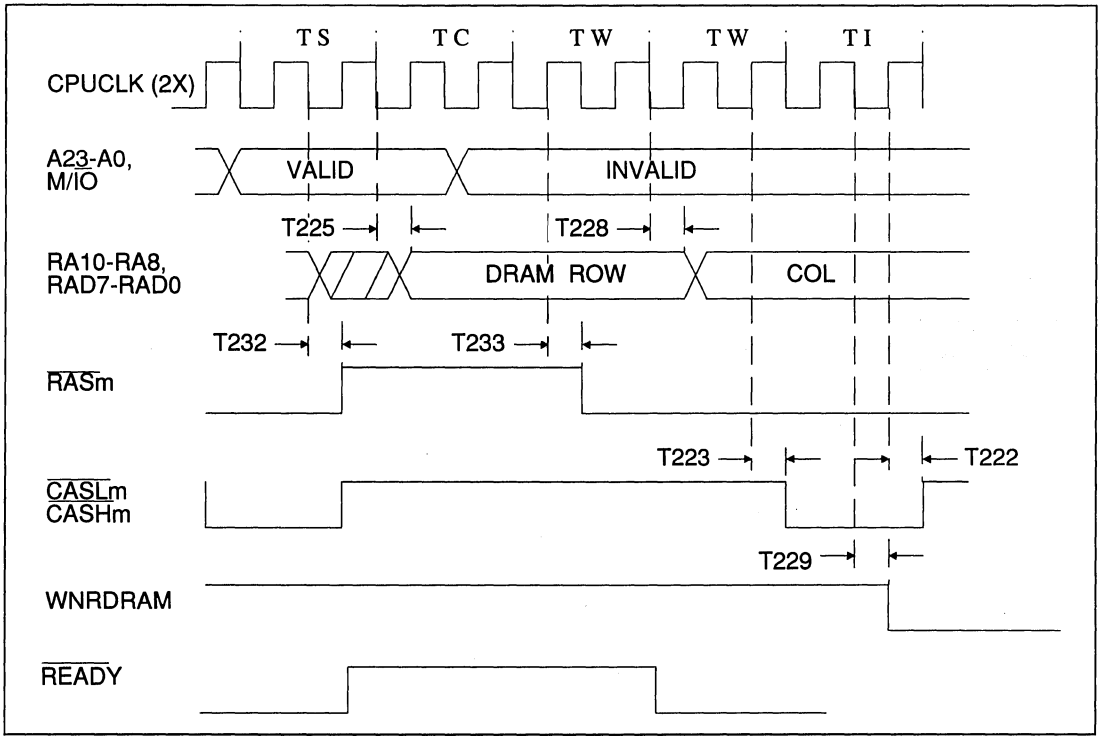


FIGURE 13-5. 80286 - PAGE MODE, WRITE MISS AFTER WRITE

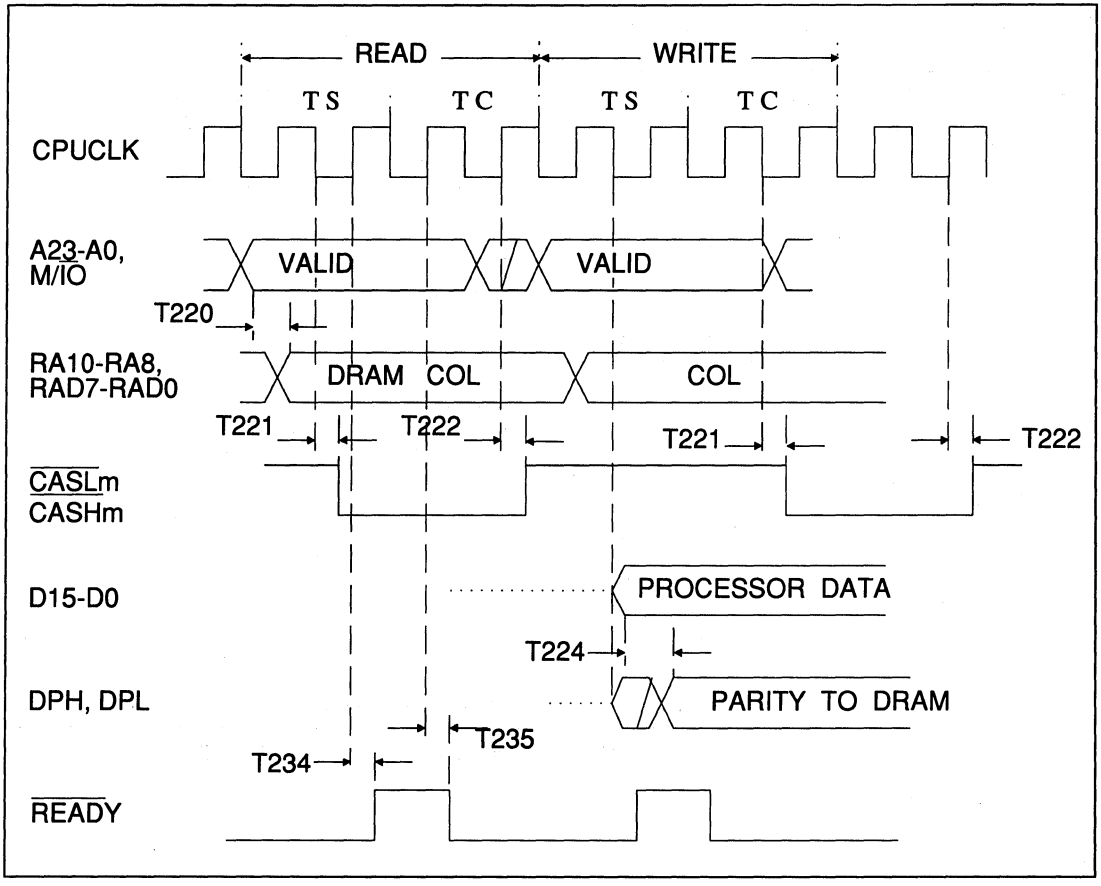


FIGURE 13-6. 80286 - PAGE MODE READ HIT AND WRITE HIT

13.1.2 80286 Non-Page Mode 00 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T234	See Table 13-3		
T235	See Table 13-3		
T252	CPUCLK fall to $\overline{CAS}$ rise	33	30
T255	CPUCLK fall to $\overline{RAS}$ fall	35	32
T270	CPUCLK fall to ROW address	46	42
T271	CPUCLK fall to $\overline{CAS}$ fall	37	34
T273	CPUCLK fall to WNRDRAM fall	33	31
T274	CPUCLK fall to WNRDRAM rise	33	31
T275	Data holding tristate. ①	12	12
T276	Clock fall to parity valid	30	27
T277	CPUCLK fall to RAS rise	30	28
T278	CPUCLK fall to COLUMN address valid	41	38
T279	Processor address to ROW address	32	30

① Tristate times are not tested. Timing specifications are derived from simulation.

TABLE 13-4. 80286 - NON-PAGE MODE 00 MEMORY TIMING

8

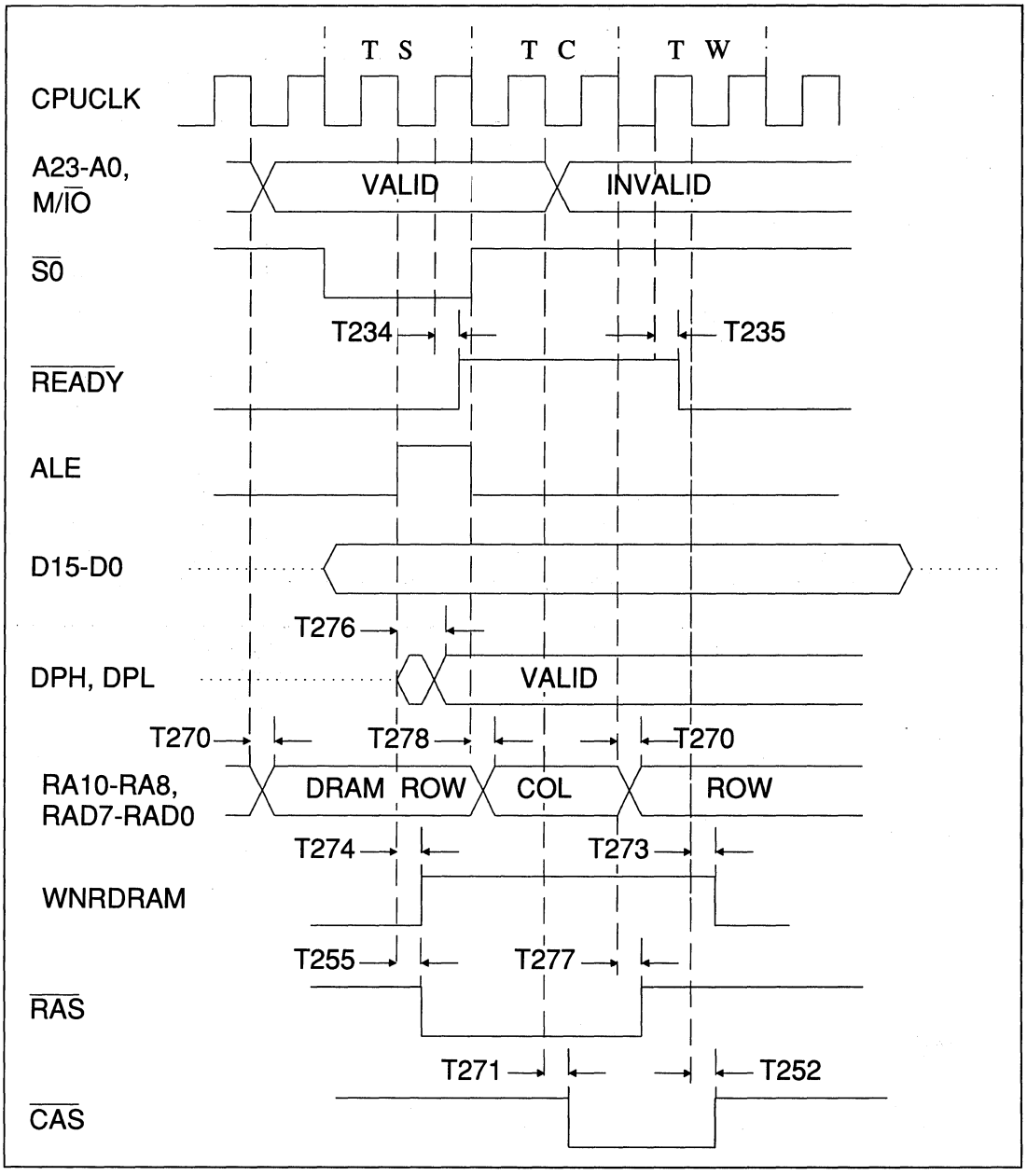


FIGURE 13-7. 80286 - NON-PAGE MODE 00, 1 WAIT STATE WRITE (4072H = 0001)

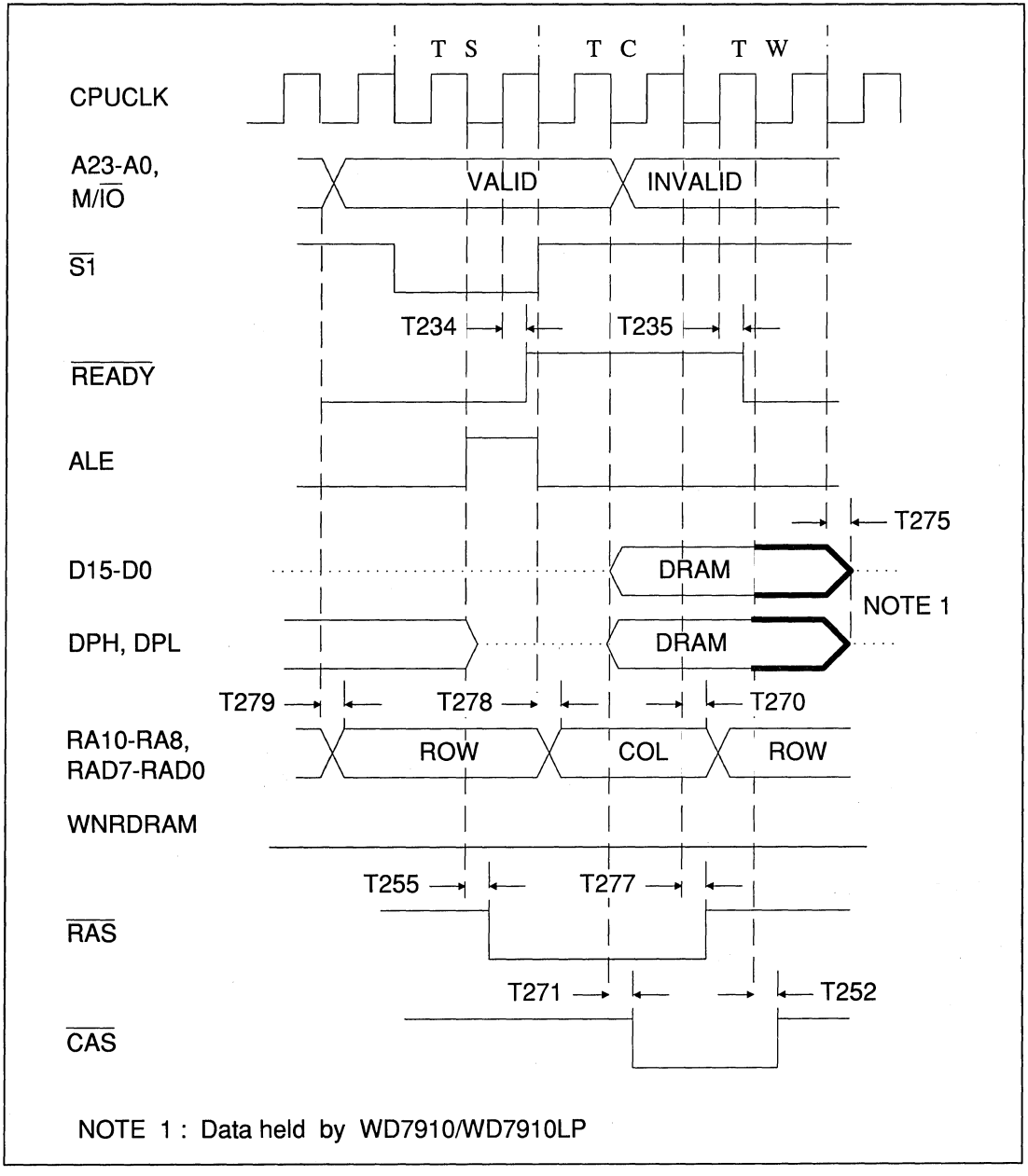


FIGURE 13-8. 80286 - NON-PAGE MODE 00, 1 WAIT STATE READ (4072H = 0001)

8

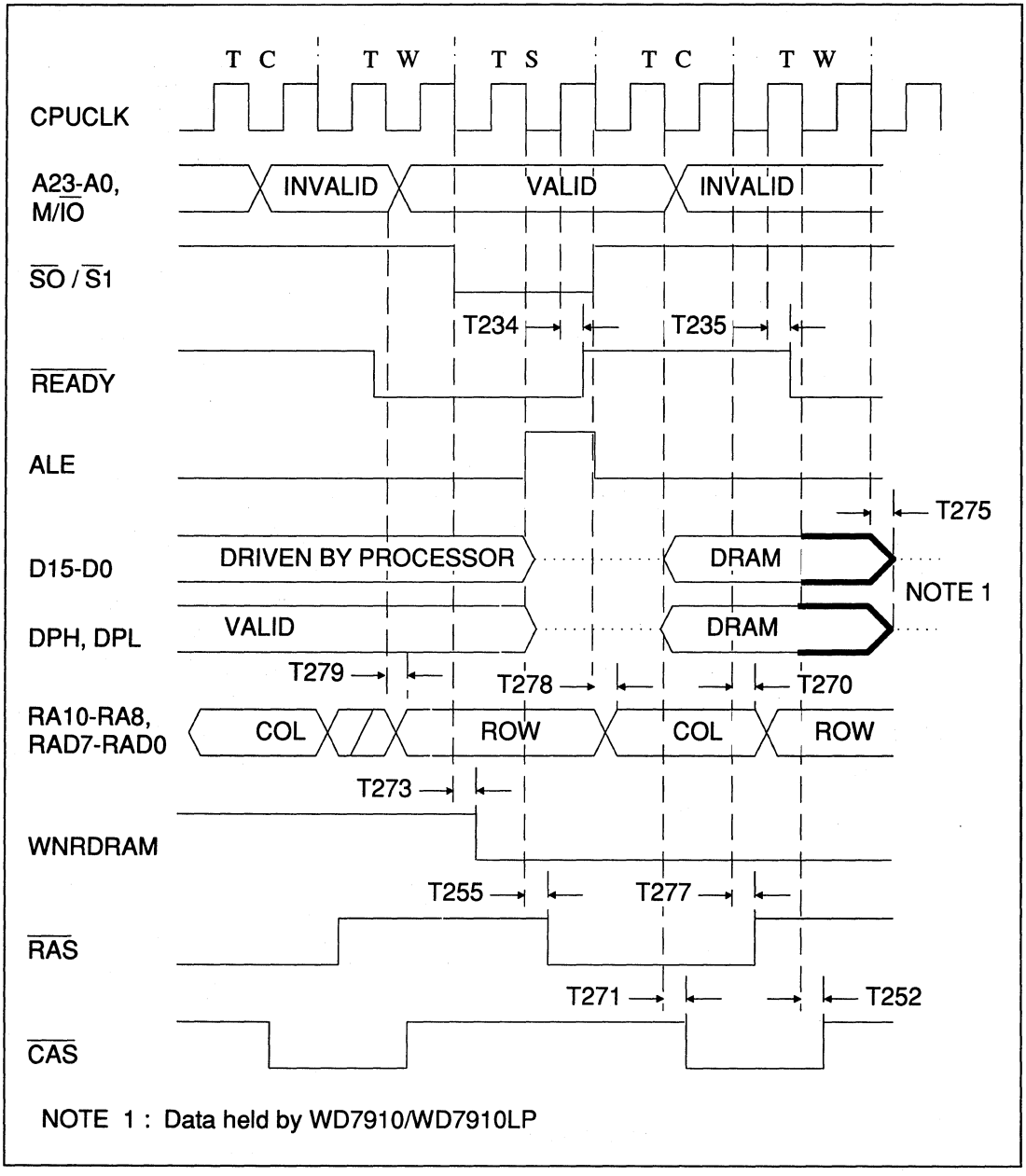


FIGURE 13-9. 80286 - NON-PAGE MODE MODE 00, 2 WAIT STATES READ AFTER WRITE (4072H = 0001)

13.1.3 80286 Non-Page Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T224	See Table 13-3		
T234	See Table 13-3		
T235	See Table 13-3		
T252	See Table 13-4		
T253	CPUCLK fall to WNRDRAM fall	34	31
T254	CPUCLK fall to WNRDRAM rise	34	31
T255	See Table 13-4		
T257	CPUCLK rise to $\overline{RAS}$ rise	35	32
T258	CPUCLK rise to COLUMN address valid	44	40
T276	See Table 13-4		

TABLE 13-5. 80286 - NON-PAGE MODE 01 MEMORY TIMING

8

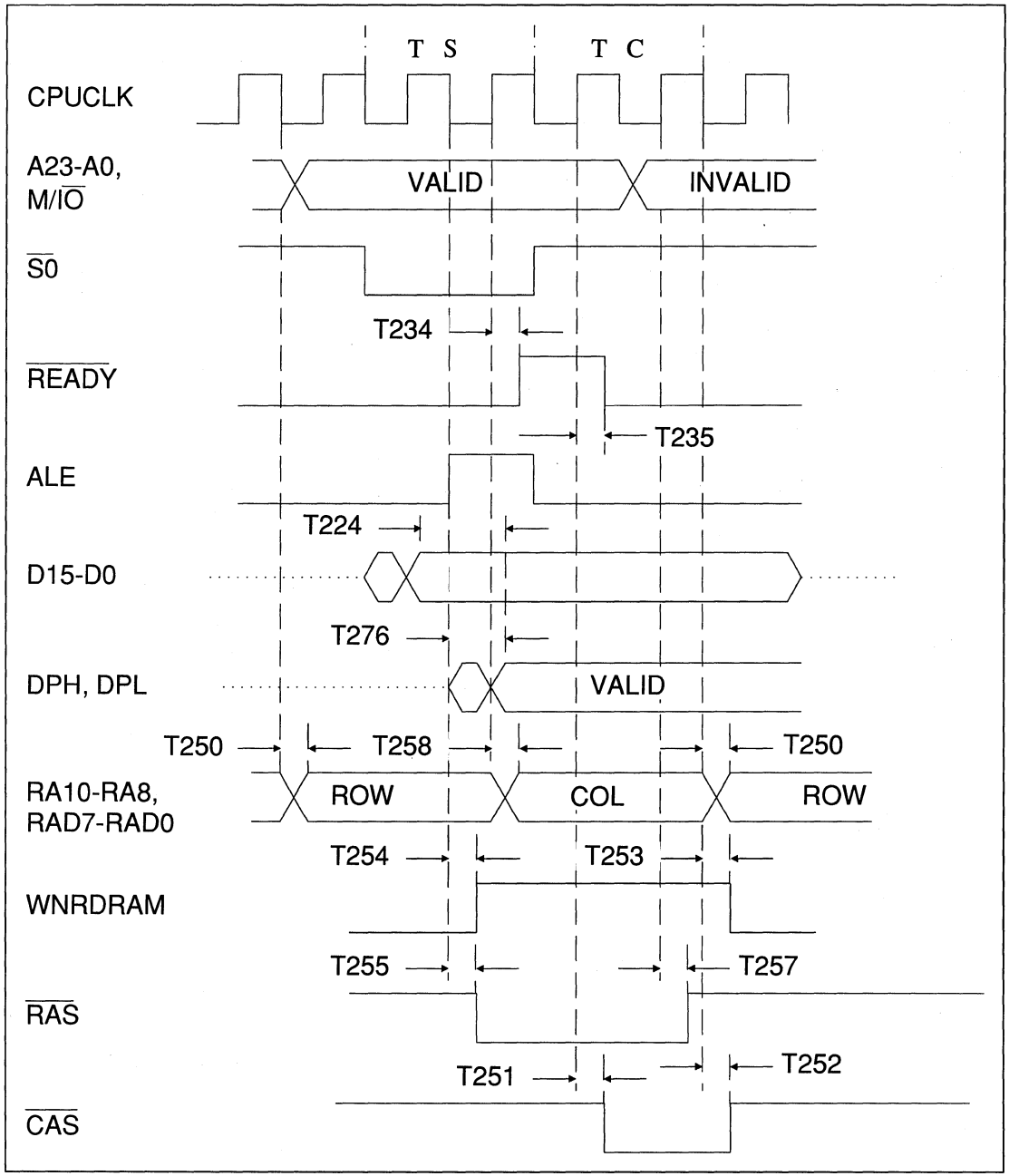


FIGURE 13-10. 80286 - NON-PAGE MODE 01, 0 WAIT STATE WRITE (4072H = 3560H)

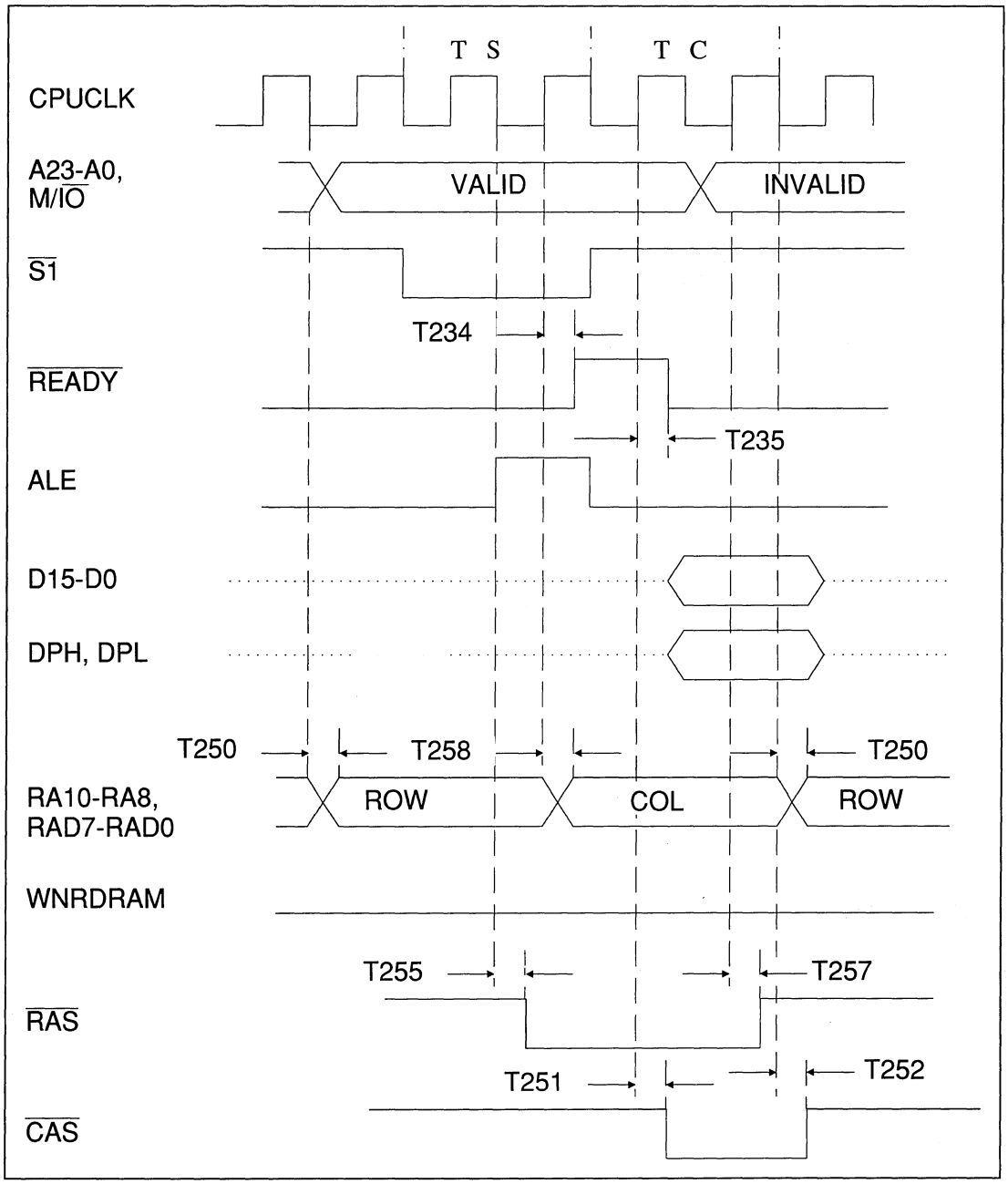


FIGURE 13-11. 80286 - NON-PAGE MODE 01, 0 WAIT STATE READ (4072H = 3560H)

13.1.4 80386SX Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T200	Processor ADDRESS to RAM address valid, Page Hit		34	27
T201	CPUCLK rise to CAS fall, 2.5 CLK CAS		31	25
T202	CPUCLK fall to CAS rise		24	21
T203	CPUCLK fall to CAS fall, 2.0 CLK CAS		27	22
T204	Processor data to parity valid		25	20
T205	CPUCLK rise to RAM address valid, Page Miss		48	43
T206	CPUCLK rise to WNRDRAM rise		31	28
T207	CPUCLK fall to RAS fall, first access		27	21
T208	CPUCLK rise to COLUMN address valid		49	33
T209	CPUCLK rise to WNRDRAM fall		31	28
T212	CPUCLK rise to RAS rise, Page Miss		27	24
T213	CPUCLK fall to RAS fall, Page Miss		27	24
T214	CPUCLK rise to READY fall		19	18
T215	CPUCLK rise to READY rise		19	18

TABLE 13-6. 80386SX - PAGE MODE MEMORY TIMING

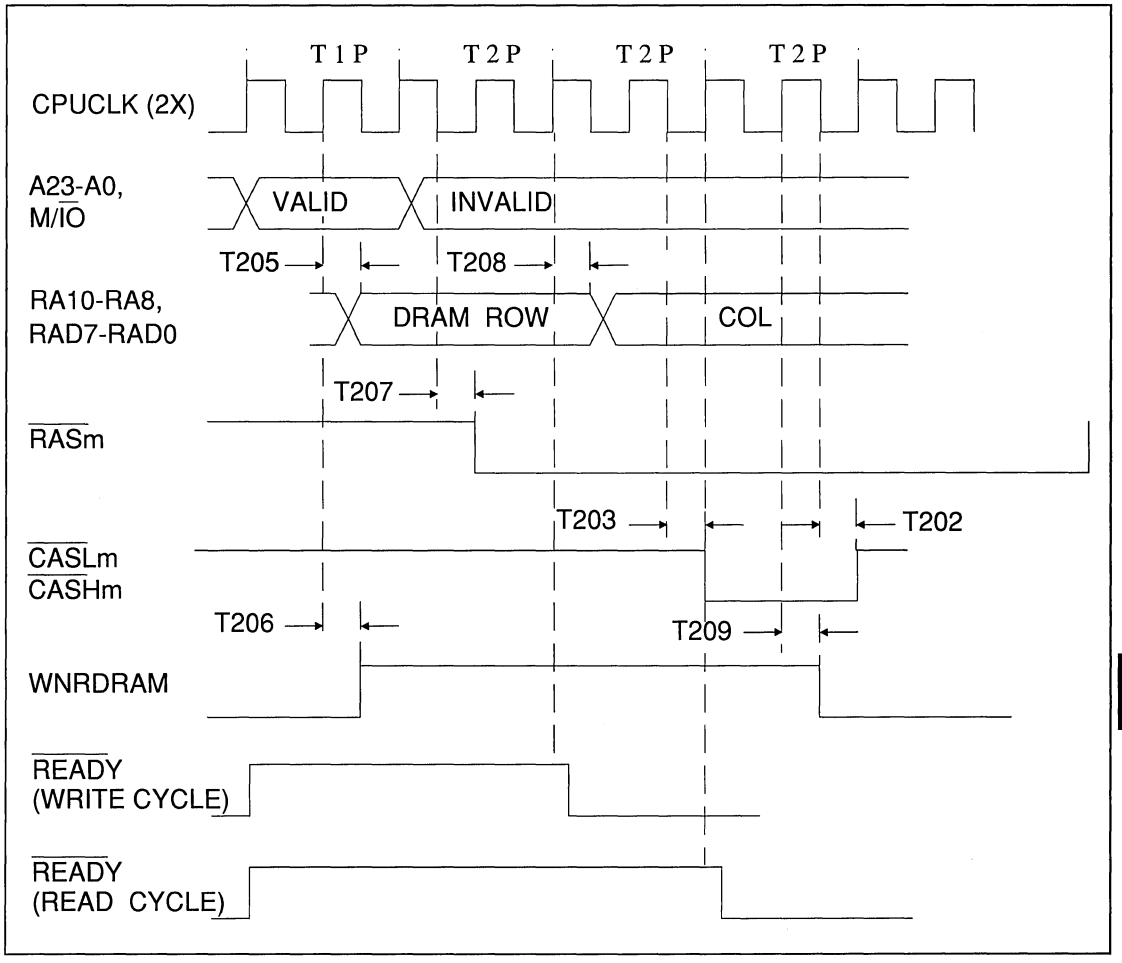


FIGURE 13-12. 80386SX - PAGE MODE, FIRST ACCESS READ/WRITE

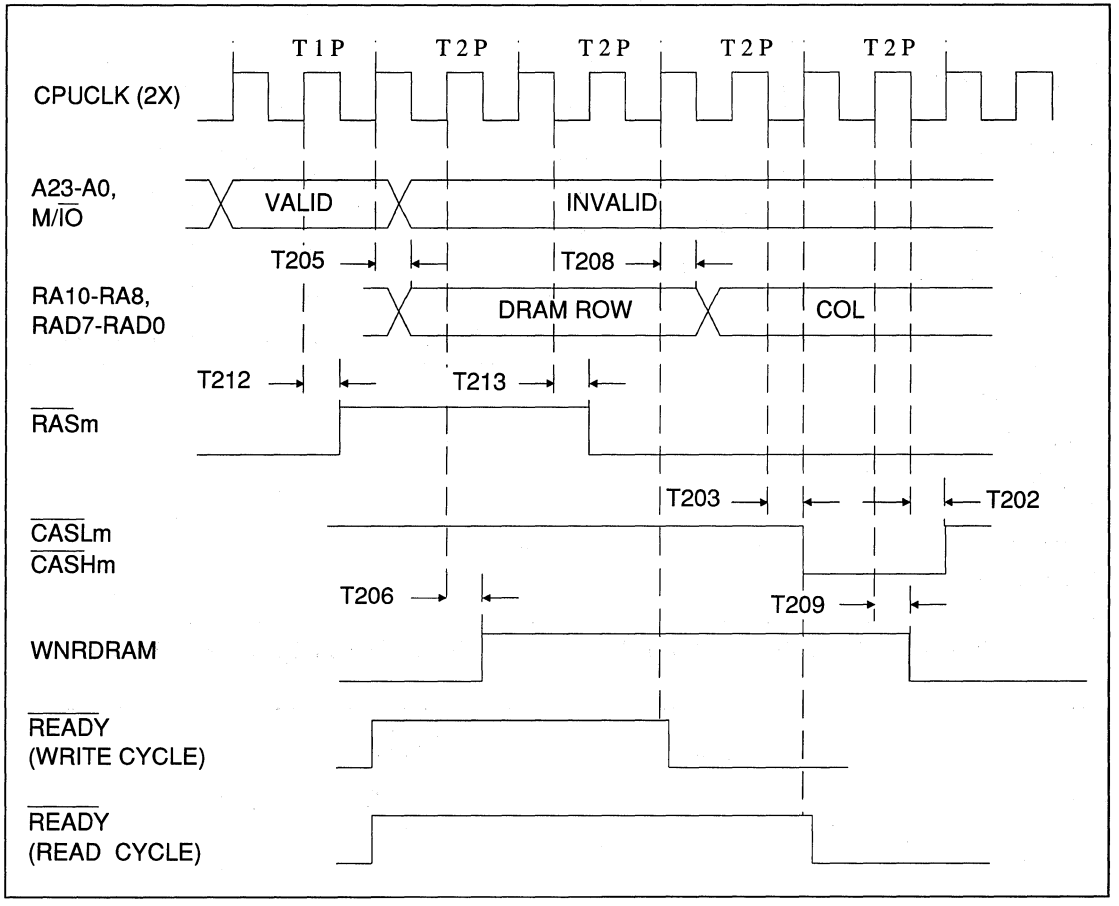


FIGURE 13-13. 80386SX - PAGE MODE, PAGE MISS READ/WRITE

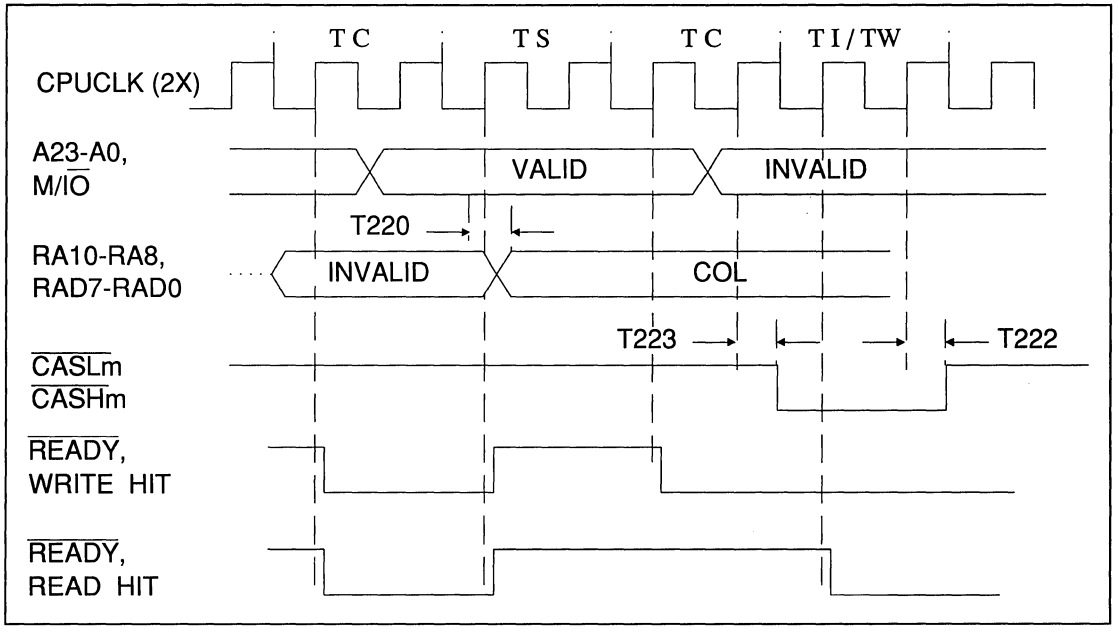


FIGURE 13-14. 80386SX - PAGE MODE, RAD CYCLE FOLLOWED BY A PAGE HIT

8

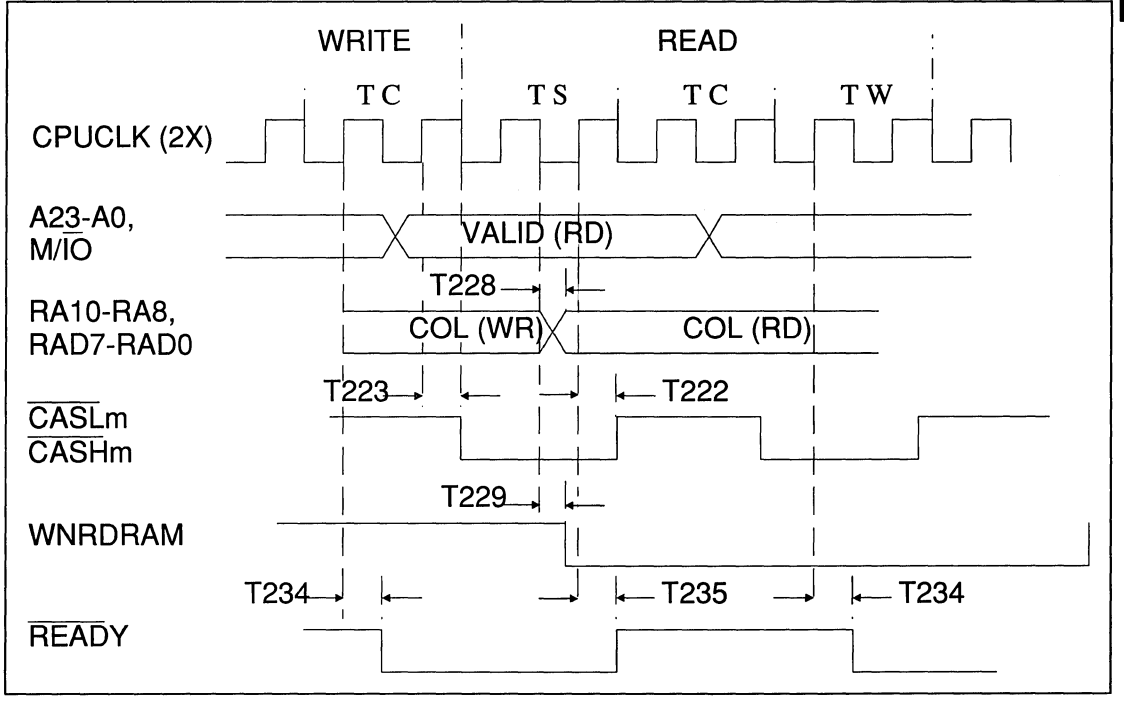


FIGURE 13-15. 80386SX - PAGE MODE, READ AFTER WRITE

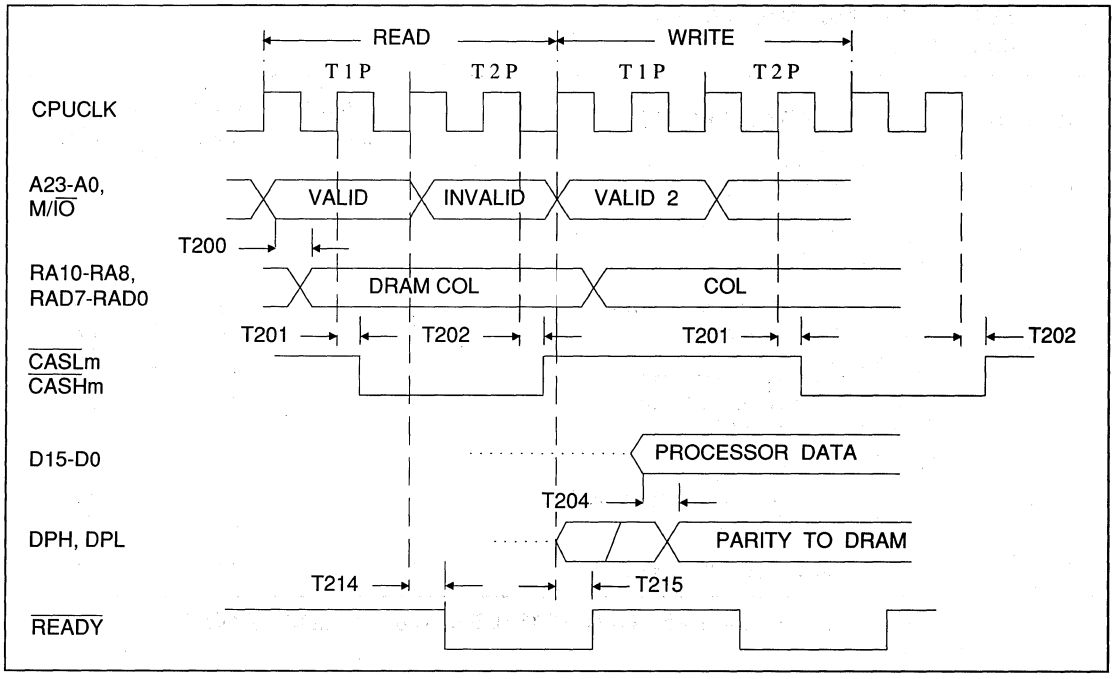


FIGURE 13-16. 80386SX - PAGE MODE, READ HIT FOLLOWED BY A WRITE HIT

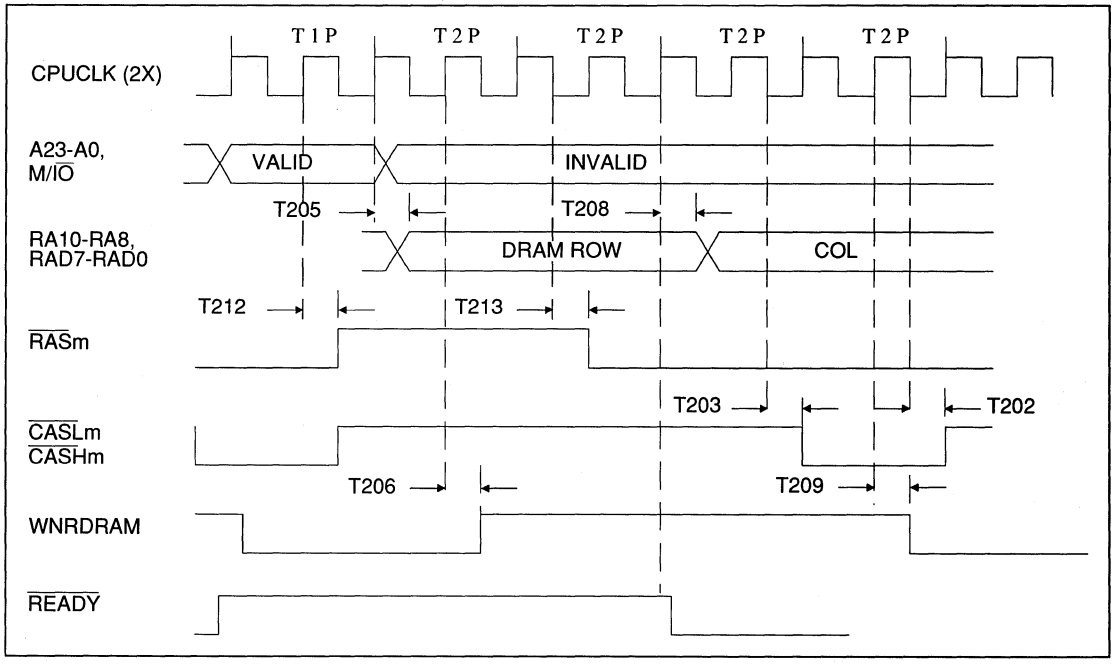


FIGURE 13-17. 80386SX - PAGE MODE, WRITE MISS CYCLE FOLLOWING A WRITE CYCLE

13.1.5 80386SX Non-Page Mode 00 And Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T204	See Table 13-6			
T214	See Table 13-6			
T215	See Table 13-6			
T240	CPUCLK rise to ROW address valid		42	42
T241	CPUCLK fall to CAS fall		27	27
T242	CPUCLK rise to CAS rise		28	24
T243	CPUCLK rise to WNRDRAM fall		28	28
T244	CPUCLK rise to WNRDRAM rise		28	28
T245	CPUCLK rise to RAS fall		25	23
T246	CPUCLK rise to RAS rise		25	23
T247	CPUCLK fall to RAS rise		29	29
T248	CPUCLK fall to COLUMN address valid		44	44
T249	CPUCLK rise to CAS fall		29	29
T260	CPUCLK rise to COLUMN address		43	41

TABLE 13-7. 80386SX - NON-PAGE MODE 00 & 01 MEMORY TIMING

8

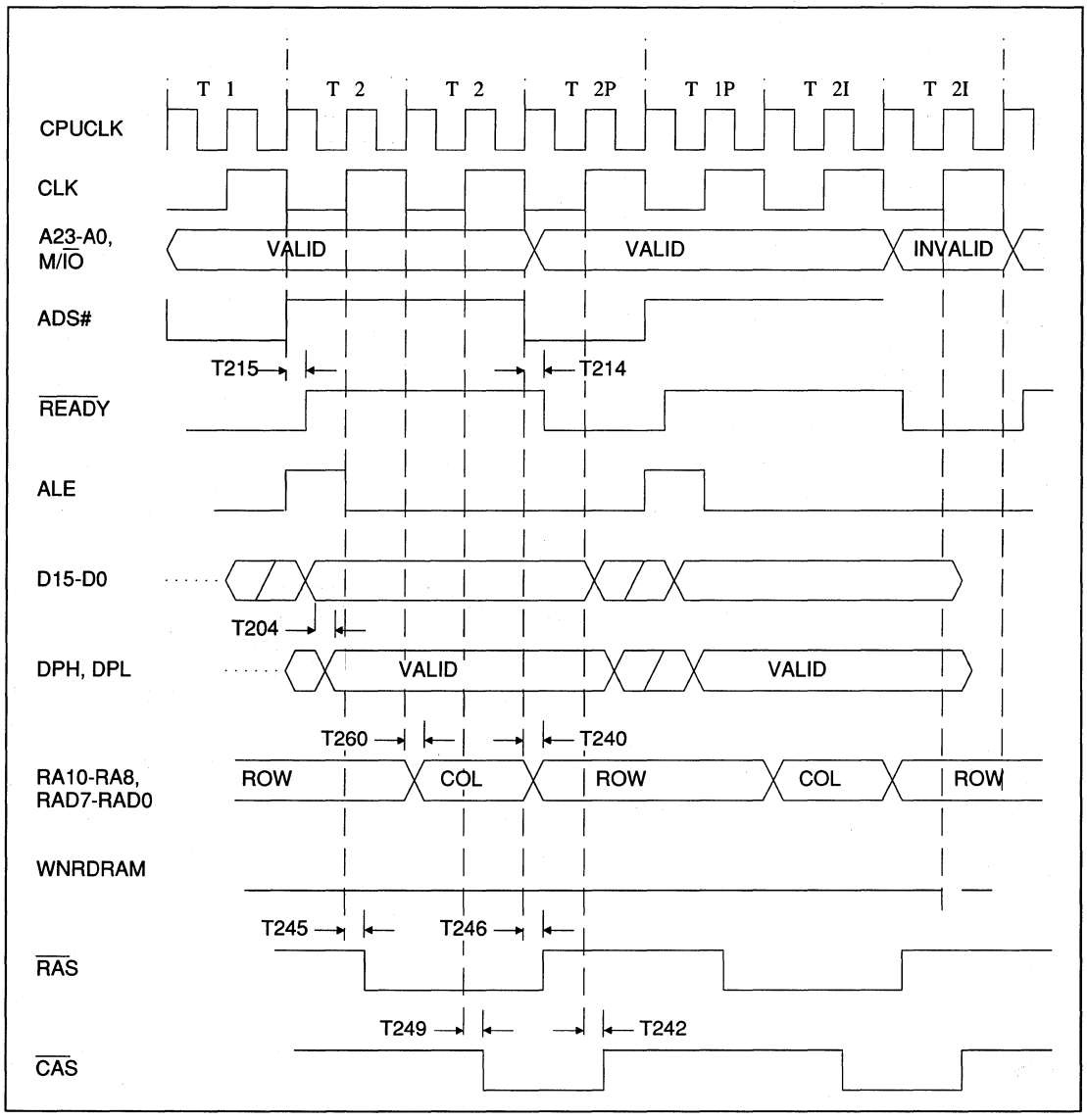


FIGURE 13-18. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE READ (PIPELINE) (4072H = 0001)

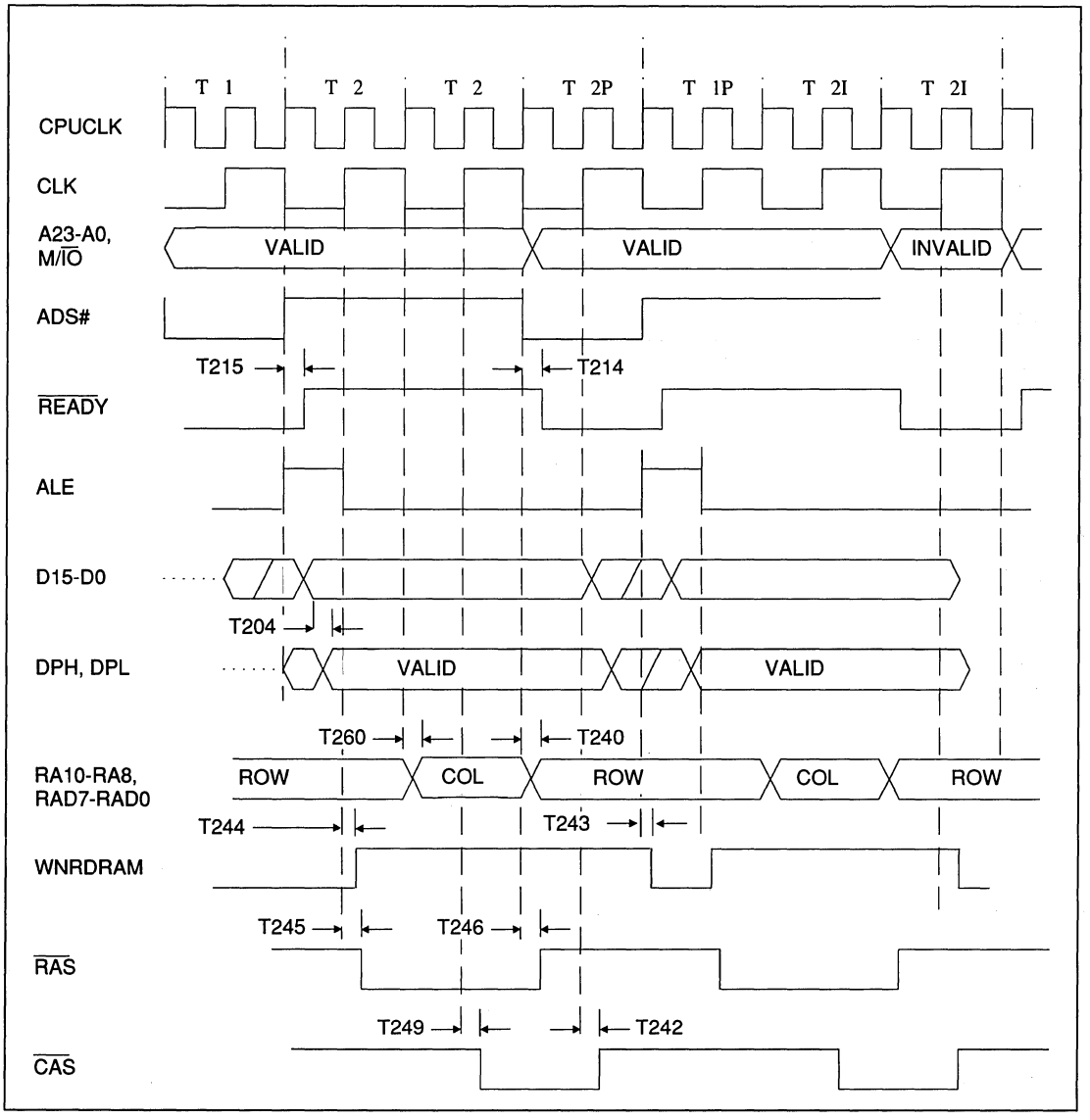


FIGURE 13-19. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE WRITE (PIPELINE) (4072H = 0001)

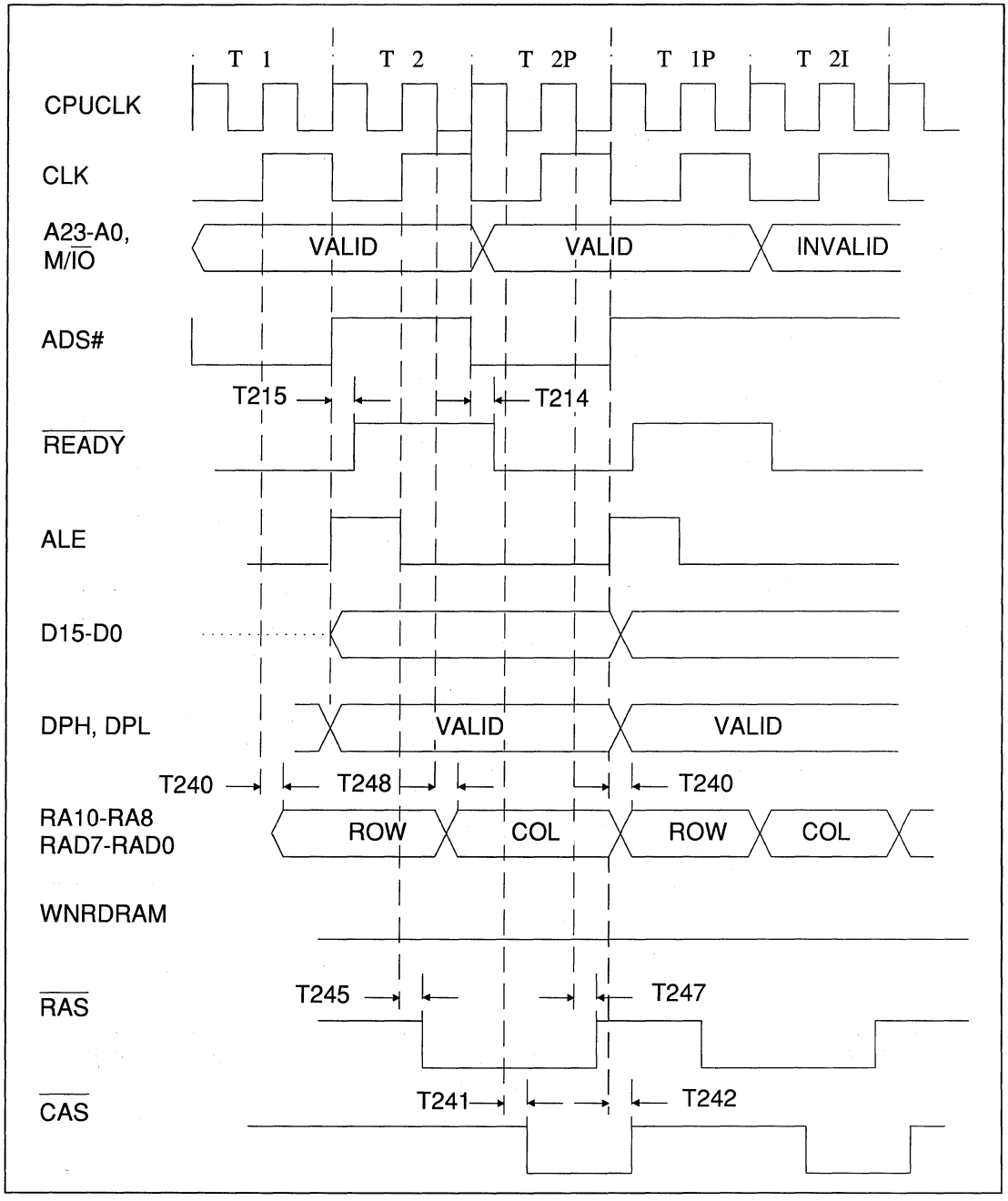


FIGURE 13-20. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

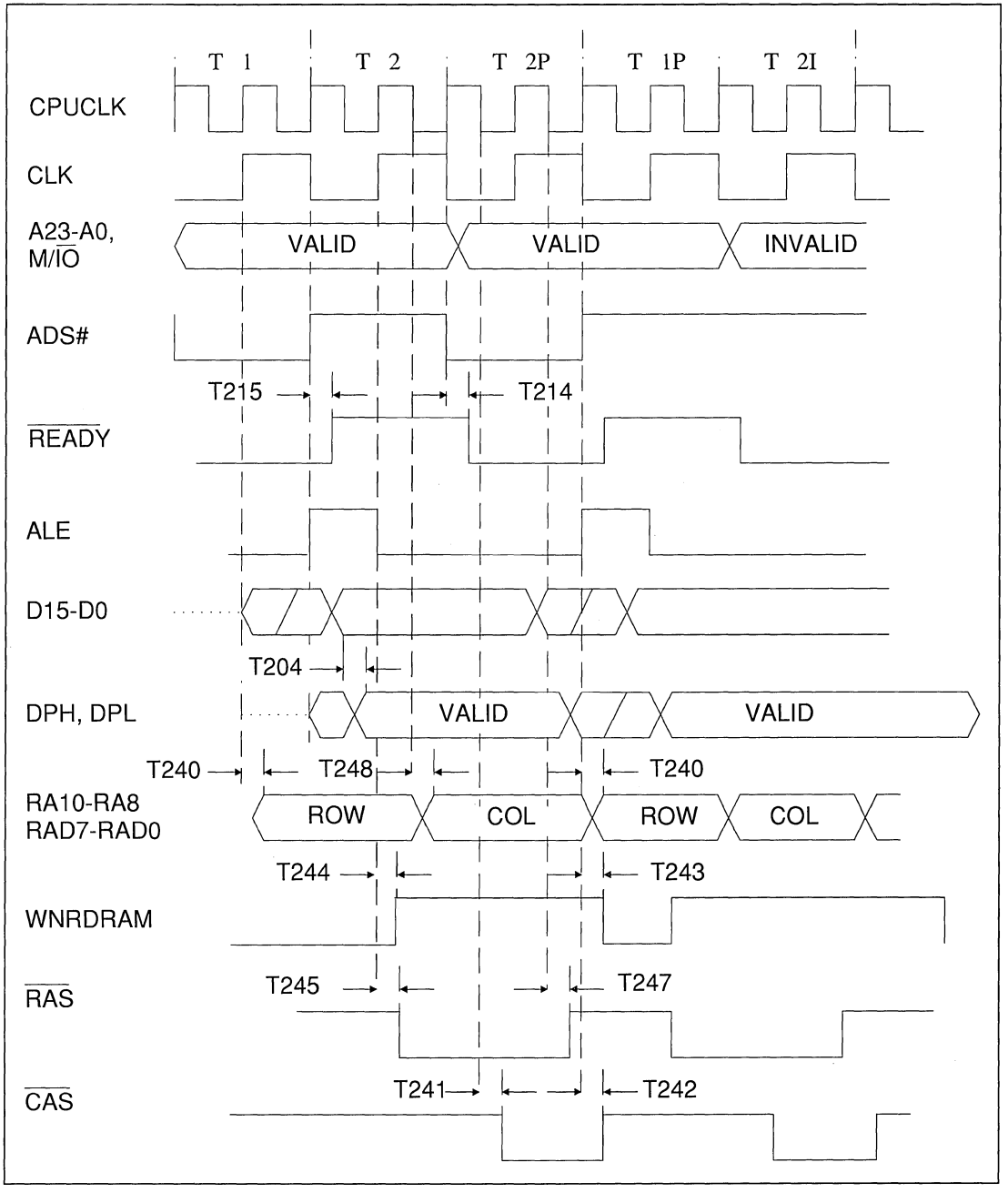


FIGURE 13-21. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

13.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus refresh cycle

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

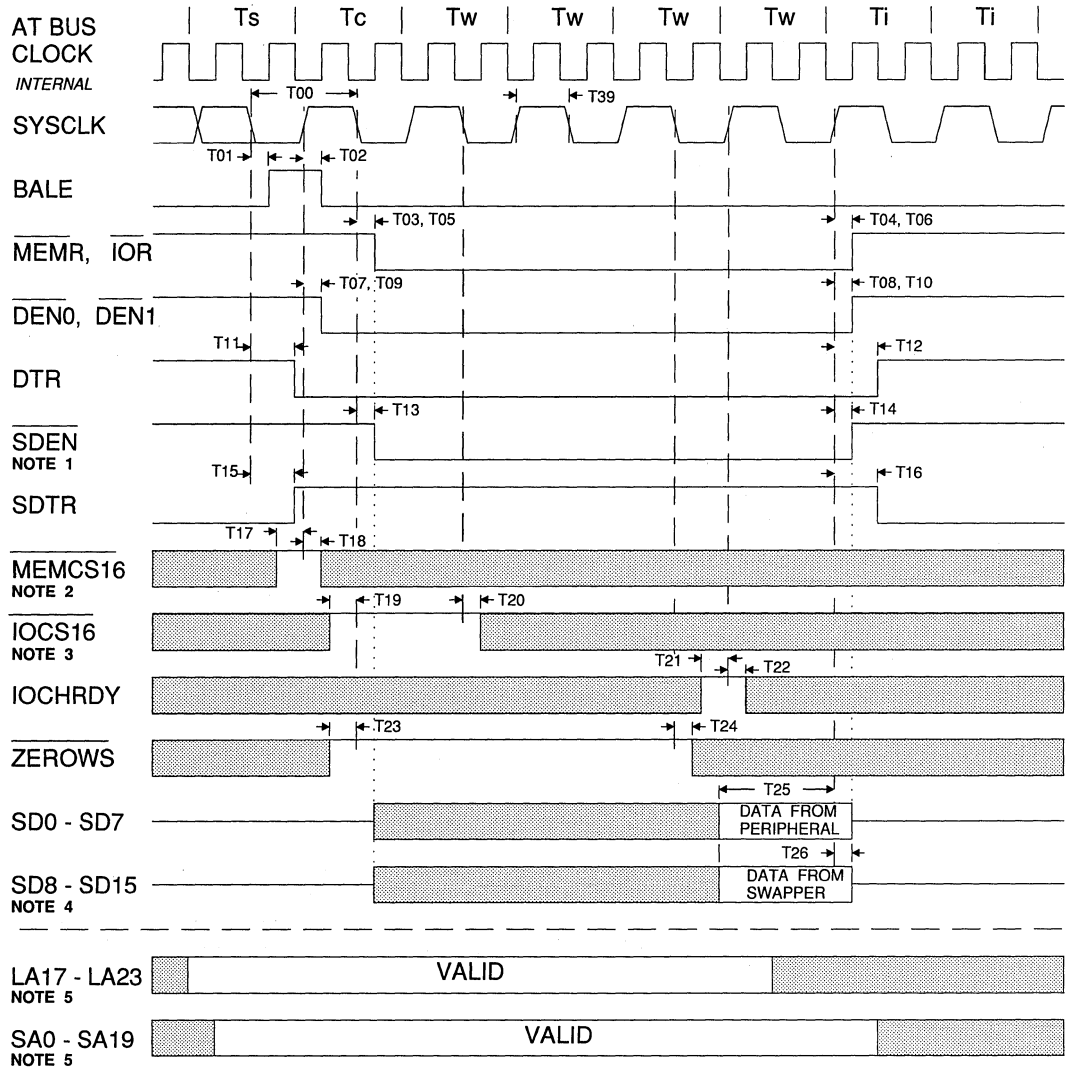
13.2.1 CPU Initiated AT Bus Cycles

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T00	SYSCLK Cycle Time	100		ns	
T01	SYSCLK fall to BALE rise		12	ns	
T02	SYSCLK rise to BALE fall		9	ns	
T03	SYSCLK fall to $\overline{\text{MEMR}}$ fall		9	ns	8-bit cycle
T04	SYSCLK rise to $\overline{\text{MEMR}}$ rise		6	ns	
T05	SYSCLK fall to $\overline{\text{IOR}}$ fall		10	ns	
T06	SYSCLK rise to $\overline{\text{IOR}}$ rise		7	ns	
T07	SYSCLK rise to $\overline{\text{DEN0}}$ fall		7	ns	Read Cycle
T08	SYSCLK rise to $\overline{\text{DEN0}}$ rise		11	ns	Read Cycle
T09	SYSCLK rise to $\overline{\text{DEN1}}$ fall		7	ns	Read Cycle
T10	SYSCLK rise to $\overline{\text{DEN1}}$ rise		9	ns	Read Cycle
T11	SYSCLK fall to DTR fall		19	ns	Delay is number given plus (T00 × 0.25)
T12	SYSCLK rise to DTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T13	SYSCLK fall to $\overline{\text{SDEN}}$ fall		10	ns	
T14	SYSCLK rise to $\overline{\text{SDEN}}$ rise		8	ns	
T15	SYSCLK fall to SDTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T16	SYSCLK rise to SDTR fall		11	ns	Delay is number given plus (T00 × 0.25)
T17	$\overline{\text{MEMCS16}}$ setup time to SYSCLK rise	25		ns	
T18	$\overline{\text{MEMCS16}}$ hold time from SYSCLK rise	0		ns	
T19	$\overline{\text{IOCS16}}$ setup time to SYSCLK fall	23		ns	
T20	$\overline{\text{IOCS16}}$ hold time from SYSCLK fall	0		ns	8-bit cycle

TABLE 13-8. CPU INITIATED AT BUS CYCLES

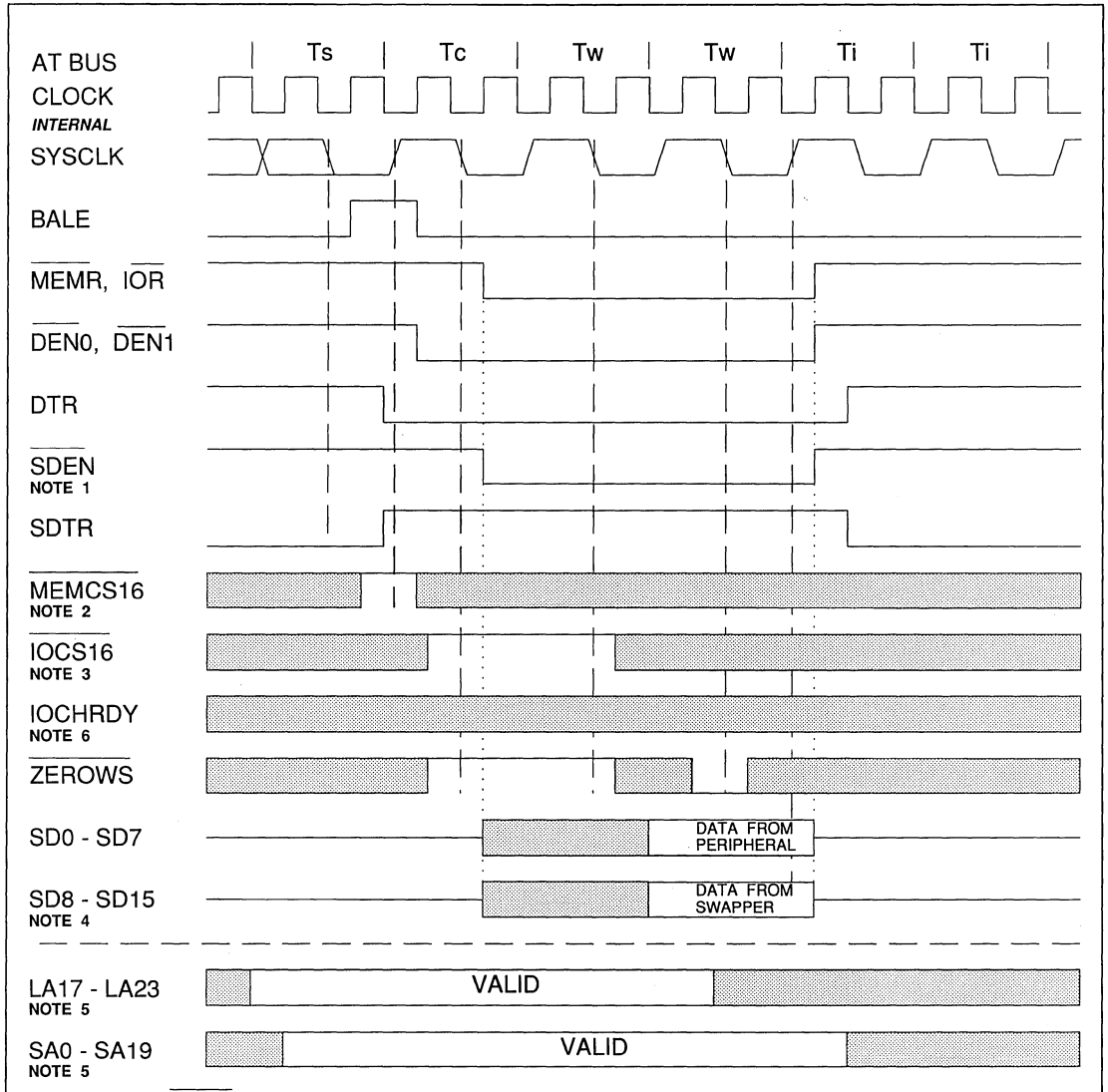
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T21	IOCHRDY setup time to SYSCLK rise	22		ns	
T22	IOCHRDY hold time from SYSCLK rise	0		ns	
T23	$\overline{\text{ZEROWS}}$ setup time to SYSCLK fall	24		ns	
T24	$\overline{\text{ZEROWS}}$ hold time from SYSCLK fall	0		ns	
T25	AT Bus data setup time to SYSCLK rise	22		ns	Total setup time is number given plus delay through AT Bus data buffers.
T26	AT Bus data hold time from SYSCLK rise	0		ns	
T27	SYSCLK fall to $\overline{\text{MEMW}}$ fall		9	ns	
T28	SYSCLK rise to $\overline{\text{MEMW}}$ rise		5	ns	
T29	SYSCLK fall to $\overline{\text{IOW}}$ fall		10	ns	
T30	SYSCLK rise to $\overline{\text{IOW}}$ rise		8	ns	
T31	SYSCLK fall to $\overline{\text{DEN0}}$ fall		10	ns	Write cycle
T32	SYSCLK fall to $\overline{\text{DEN0}}$ rise		9	ns	Write cycle
T33	SYSCLK fall to $\overline{\text{DEN1}}$ fall		10	ns	Write cycle
T34	SYSCLK fall to $\overline{\text{DEN1}}$ rise		9	ns	Write cycle
T35	SYSCLK fall to $\overline{\text{SDEN}}$ rise		11	ns	
T36	SYSCLK fall to SA0 rise		16	ns	Word to byte conversion cycle
T37	SYSCLK rise to $\overline{\text{MEMR}}$ fall		6	ns	16-bit cycle
T38	$\overline{\text{IOCS16}}$ hold time from SYSCLK rise	0		ns	16-bit cycle
T39	SYSCLK high time	-4	0	ns	(T00 ÷ 2) plus number given

TABLE 13-8. CPU INITIATED BUS CYCLES cont.



NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.
NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.
NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-22. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING



NOTE 1: SDEN is asserted only when SA0 is high.

NOTE 2: MEMCS16 is sampled only during memory cycles.

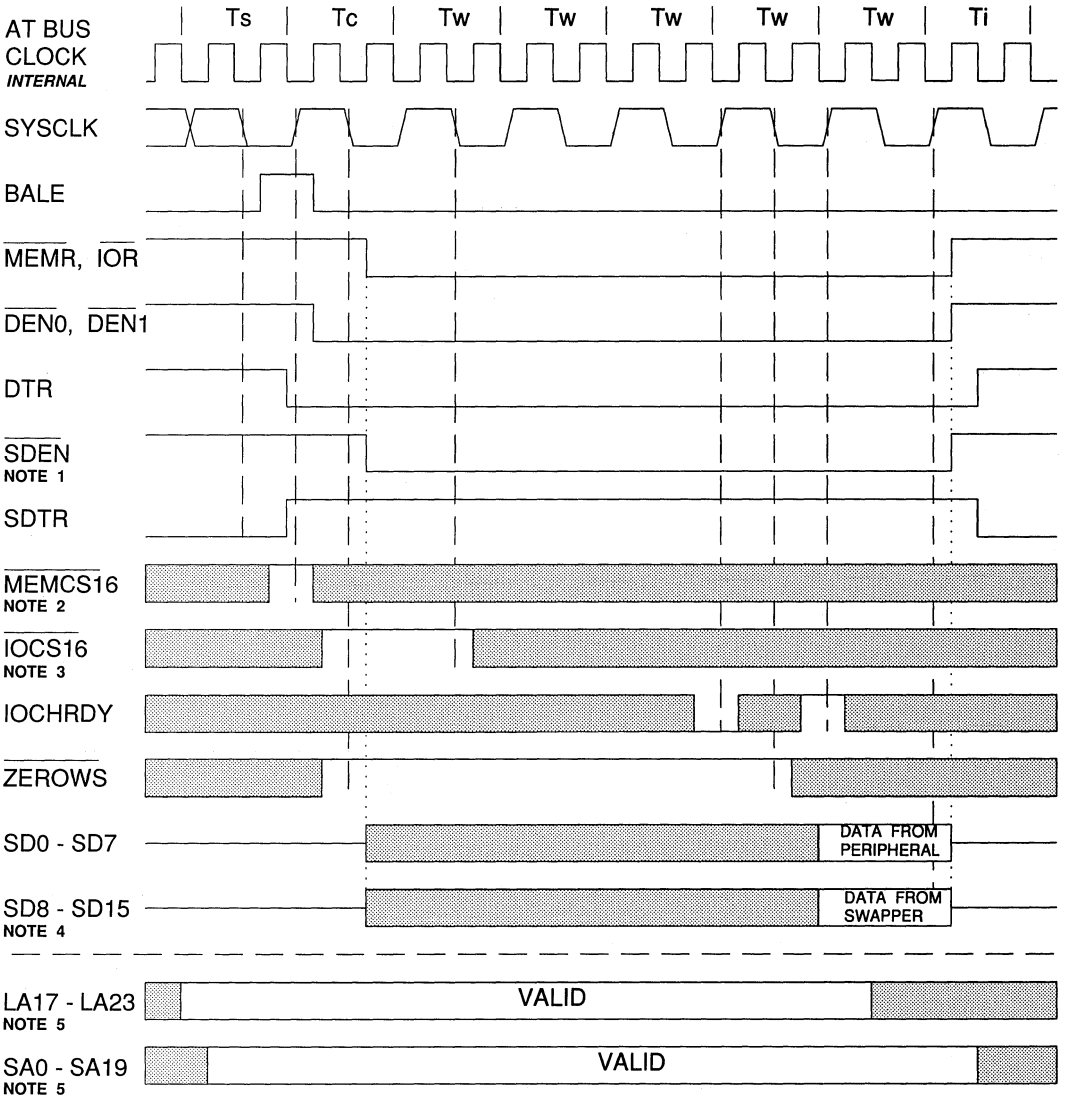
NOTE 3: IOCS16 is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

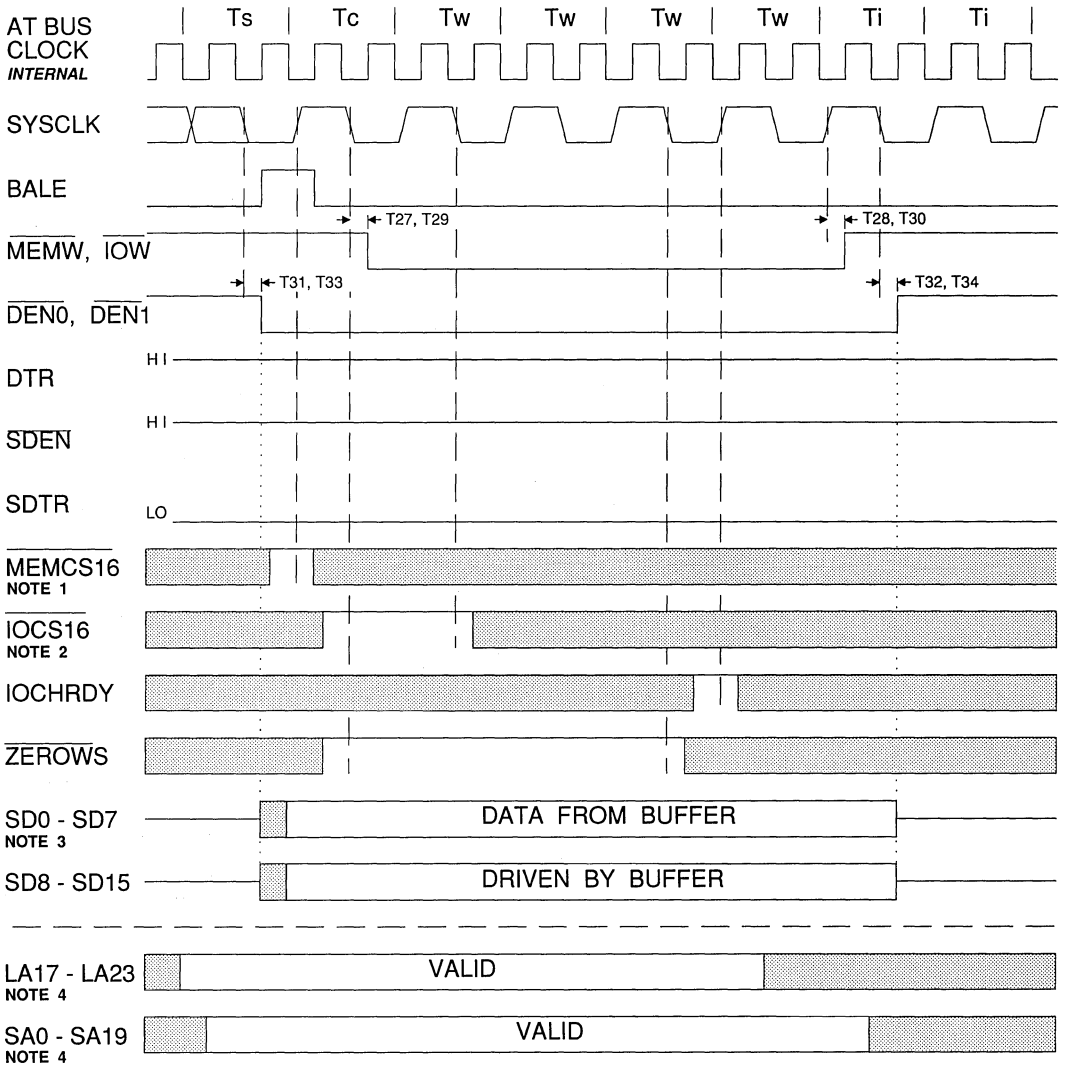
NOTE 6: IOCHRDY overrides ZEROWS only during the first cycle of a word to byte conversion.

FIGURE 13-23. AT BUS I/O OR MEMORY READ: 8-BIT, ZEROWS ASSERTED



NOTE 1: SDEN is asserted only when SA0 is high.
NOTE 2: MEMCS16 is sampled only during memory cycles.
NOTE 3: IOCS16 is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by data swapper only when SA0 is high (SDEN asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-24. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED



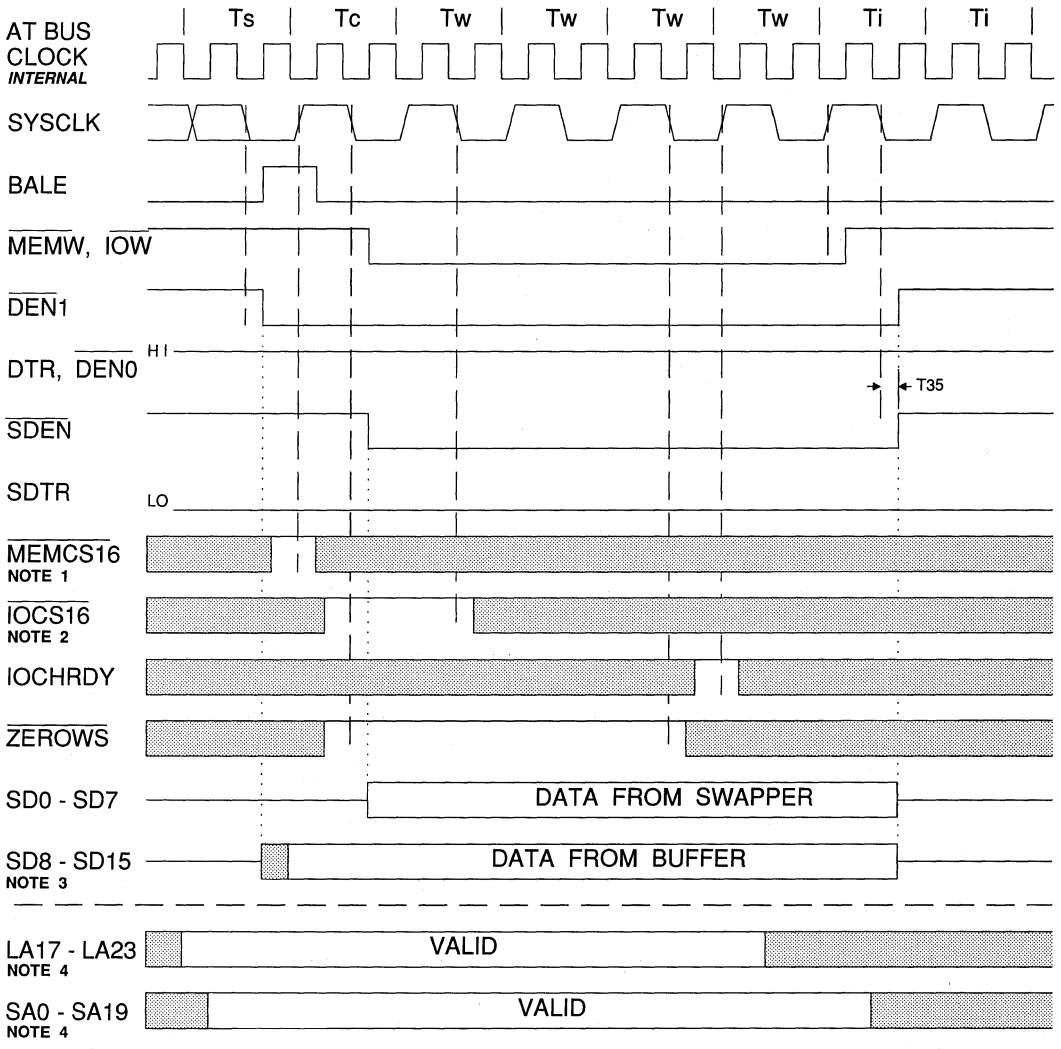
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when $\overline{\text{DEN0}}$ is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-25. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING



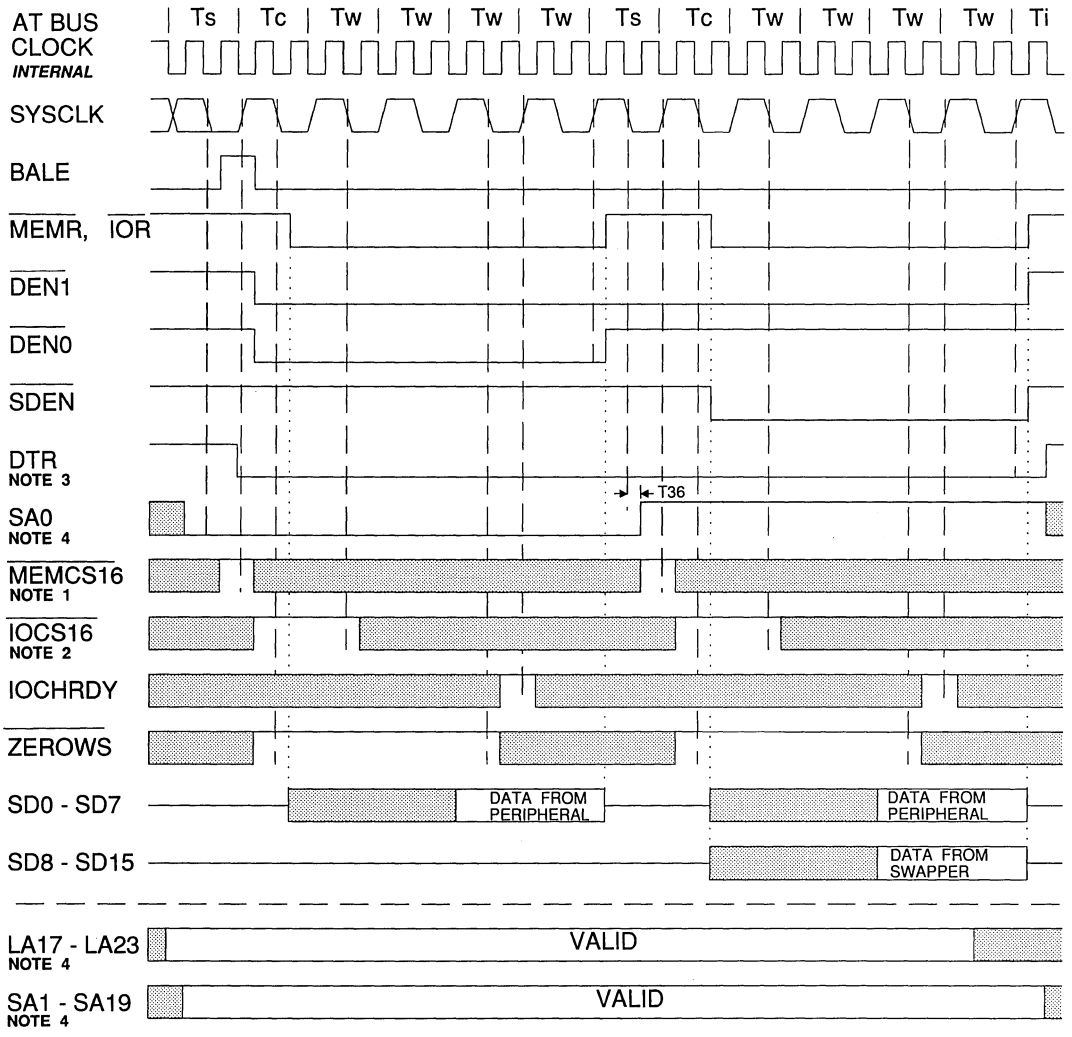
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD8 - 15 when $\overline{\text{DEN1}}$ is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-26. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING



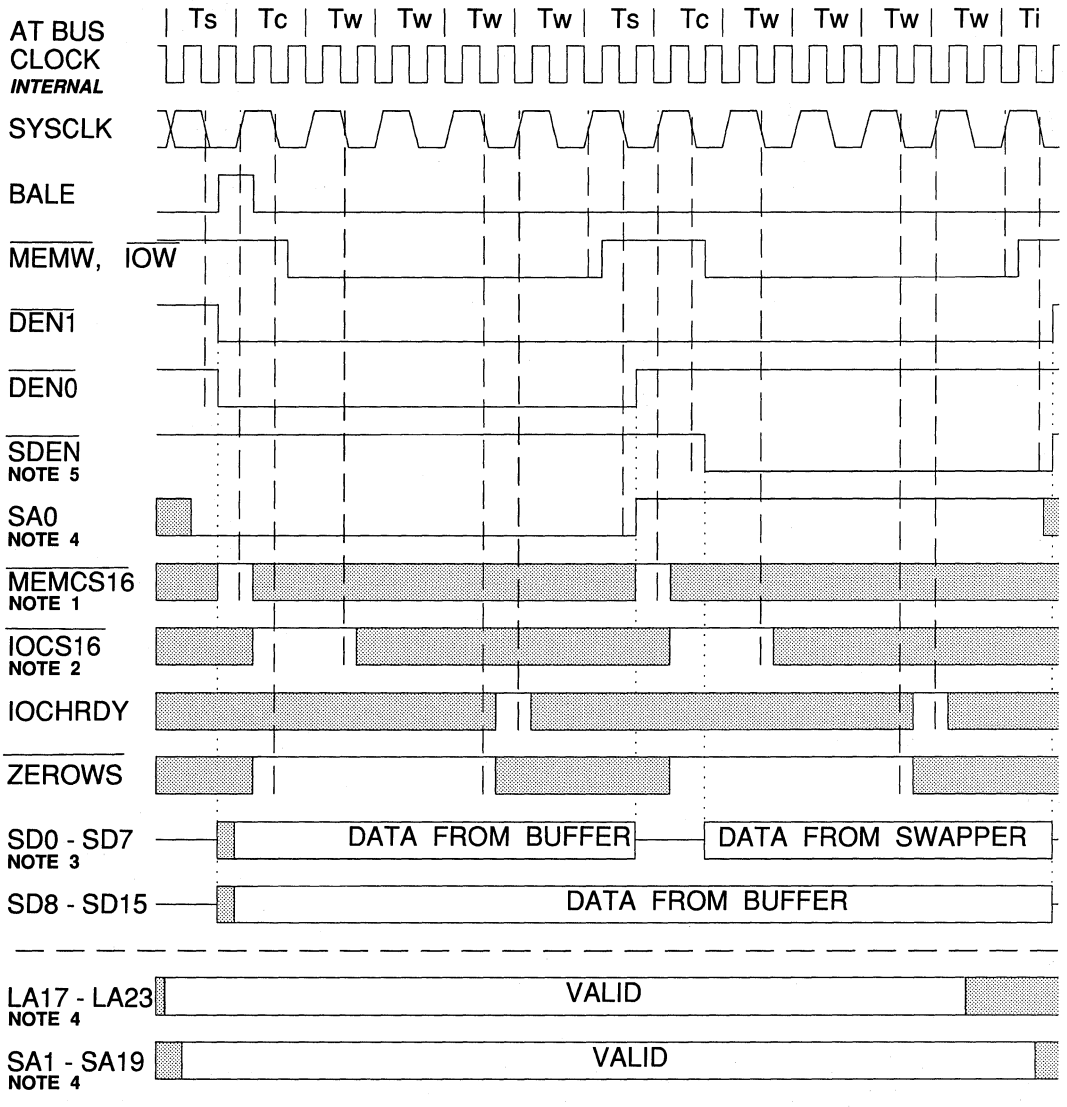
NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: SDTR is the inversion of DTR during CPU transfer cycles.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-27. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.

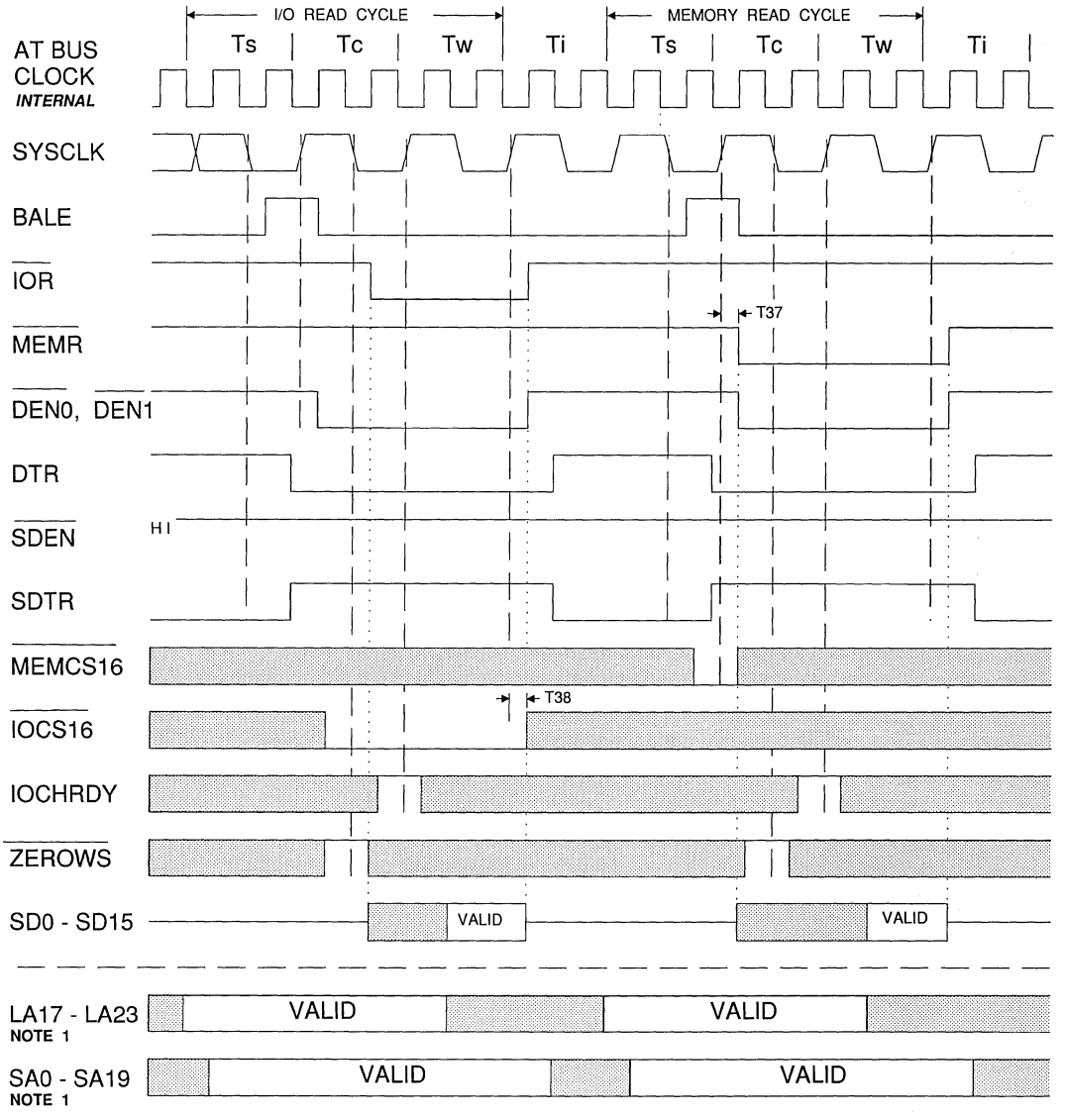
NOTE 2: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when $\overline{\text{DEN0}}$ is asserted is dependent on register settings and may be synchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

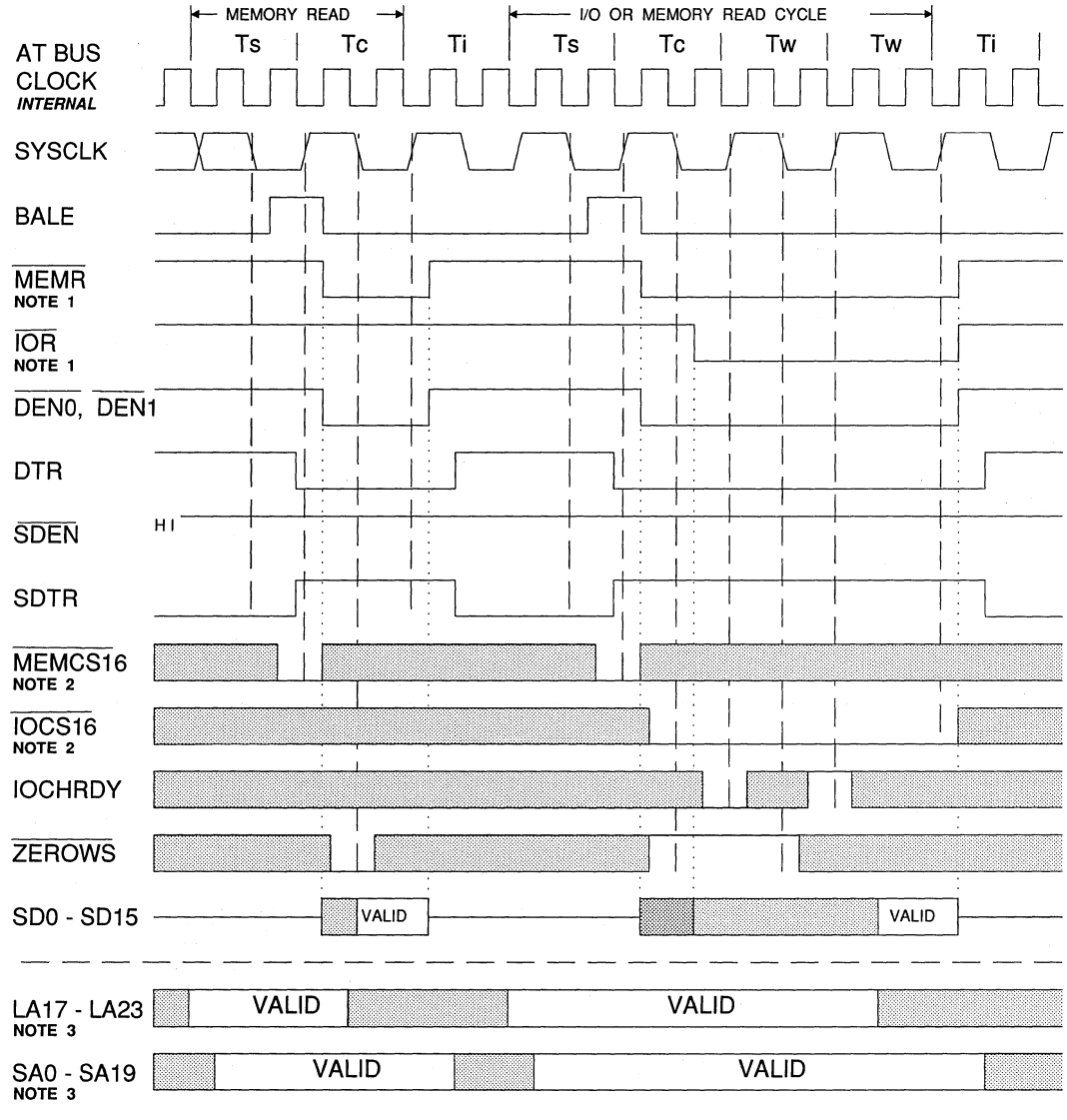
NOTE 5: SDTR remains low and DTR remains high for this cycle.

FIGURE 13-28. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-29. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING

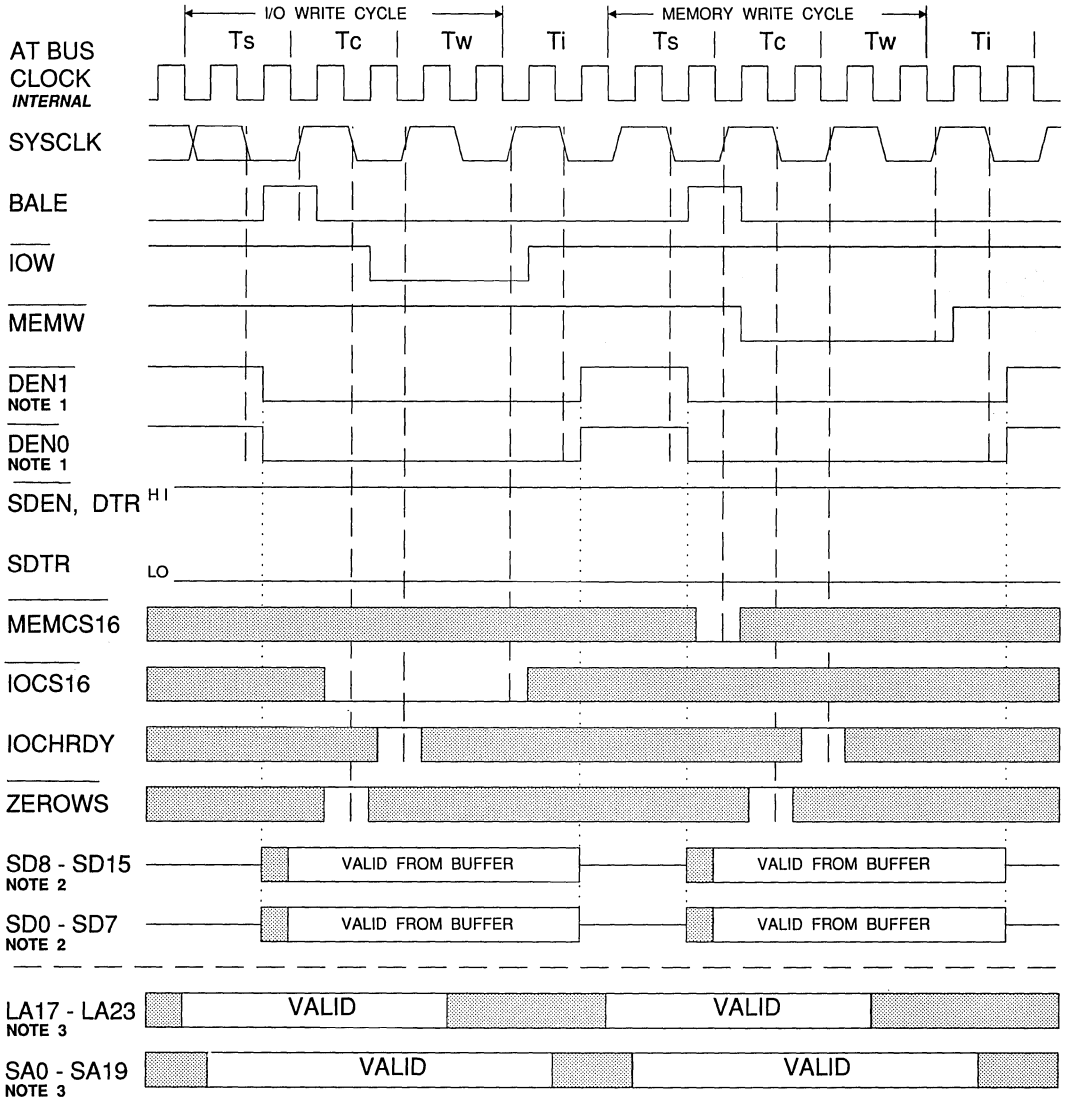


NOTE 1: MEMR and IOR will not be asserted simultaneously. The first cycle must be to memory, as zero wait state I/O cycles are not supported.

NOTE 2: MEMCS16 is sampled only during memory cycles. IOCS16 is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-30. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED



NOTE 1: $\overline{DEN0}$ is asserted only in cycles where SA0 is low. $\overline{DEN1}$ is asserted only in cycles where $\overline{SBHE}$ is low.

NOTE 2: SD8 - SD15 are driven when $\overline{DEN1}$ is low. SD0 - SD7 are driven when $\overline{DEN0}$ is low. The small period of unknown data is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-31. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING

13.2.2 Entering the AT Bus

The timing in this section is presented in the following sequence:

80286 CPU

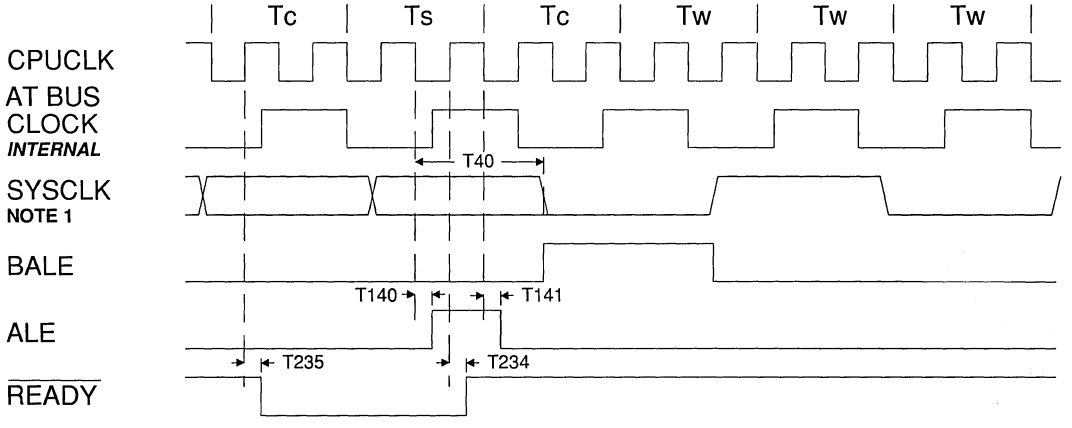
Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

80386SX CPU

Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T40	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	4		ns	Register 1872H: BRQ_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T41	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	9		ns	Register 1872H: BRQ_DEL = 00 BUS_MOD = 0X Delay is number given plus (T00 × 0.5)
T42	CPUCLK fall to SYSCLK fall 80386SX CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T43	CPUCLK rise to SYSCLK fall 80386SX CPU mode.		35	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T44	CPUCLK rise to SYSCLK fall 80286 CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T45	CPUCLK fall to SYSCLK fall 80286 CPU mode.		36	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T140	CPUCLK fall to ALE rise 80286 CPU mode. CPUCLK rise to ALE rise 80386SX CPU mode.		20	ns	
T141	CPUCLK fall to ALE fall 80286 CPU mode. CPUCLK rise to ALE fall 80386SX CPU mode.		20	ns	
T214	See TABLE 13-6				
T215	See TABLE 13-6				
T234	See TABLE 13-3				
T235	See TABLE 13-3				

TABLE 13-9. ENTERING THE AT BUS

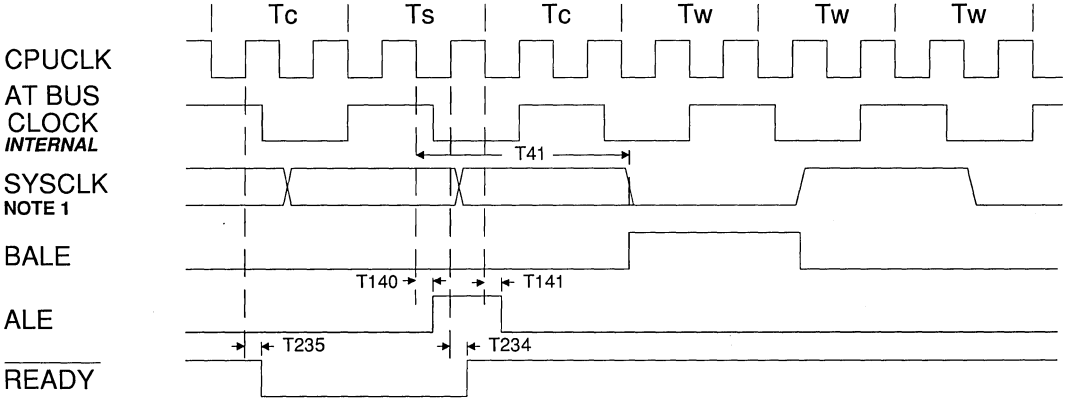


NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

FIGURE 13-32. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1/2 CLOCK

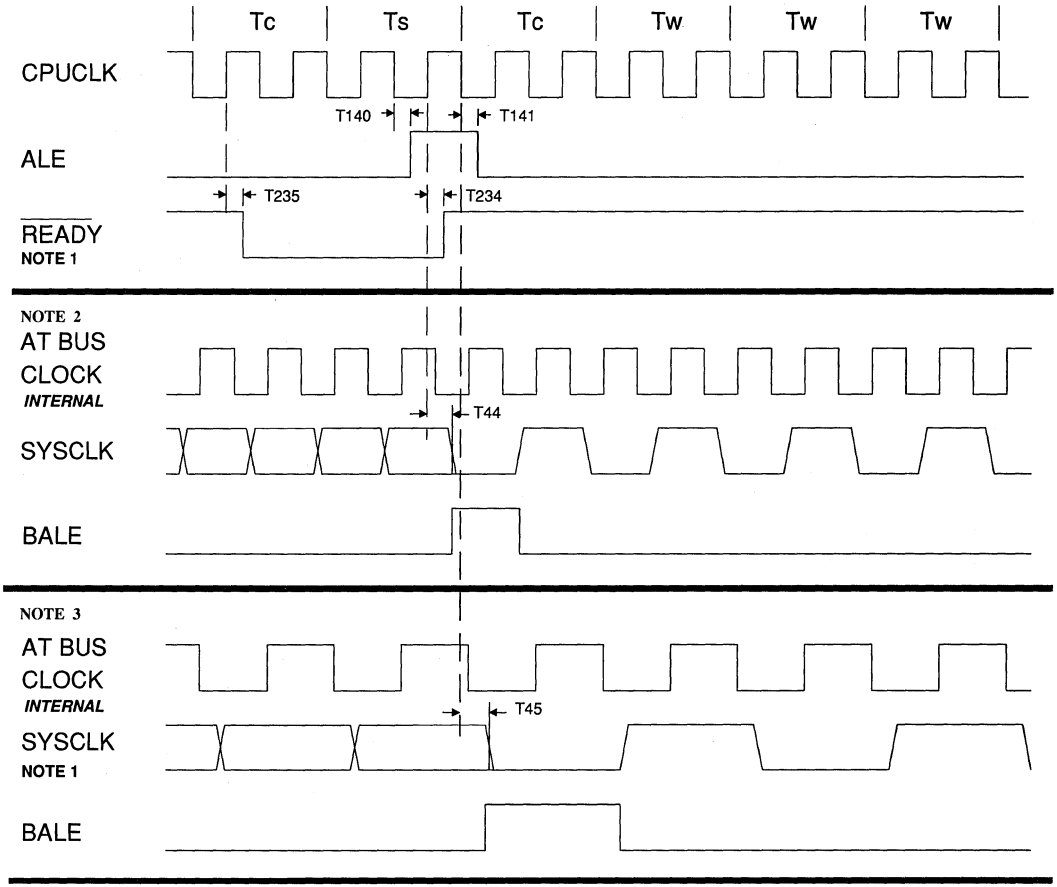
8



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 13-33. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1 CLOCK

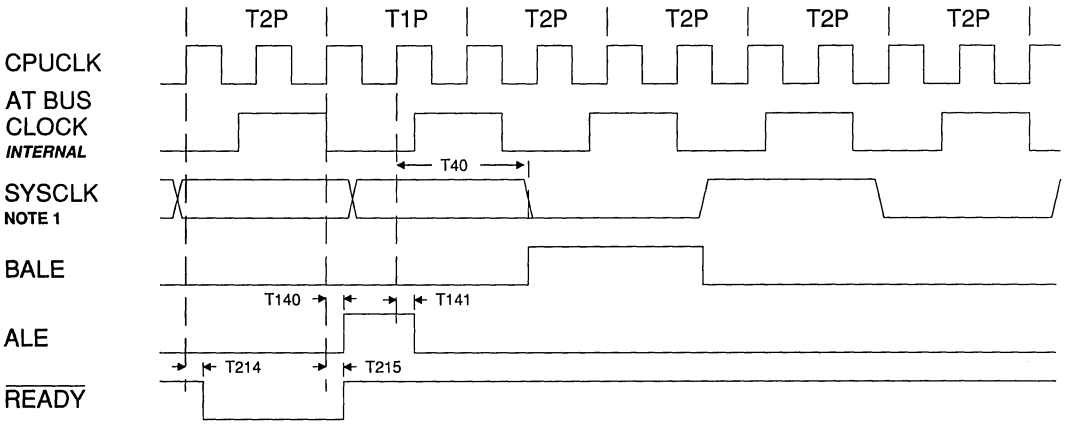


NOTE 1: $\overline{\text{READY}}$ timing is shown for when the previous cycle was not an AT bus cycle.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

FIGURE 13-34. 80286 CPU - SYCNHRONOUS CPUCLK TO SYSCLK

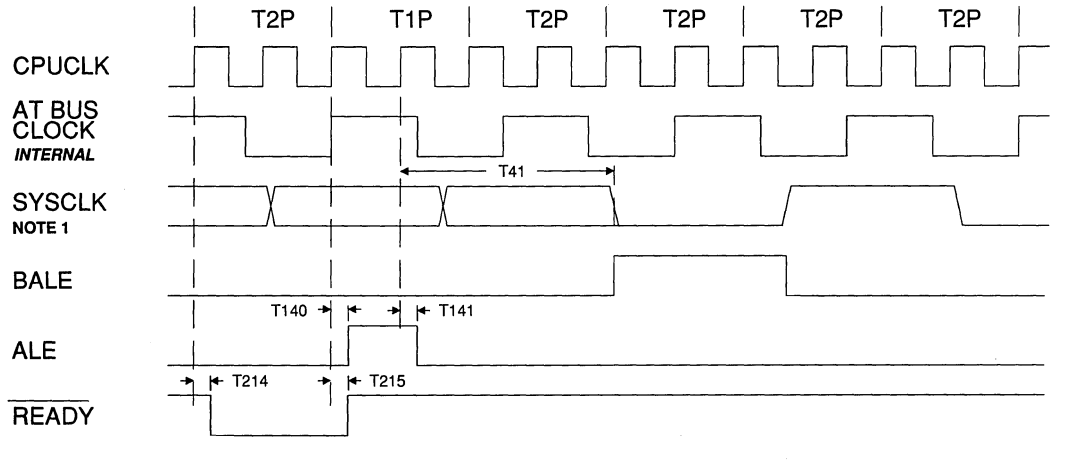


NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

FIGURE 13-35. 80386SX CPU - BREQ DELAY = 1/2 CLOCK

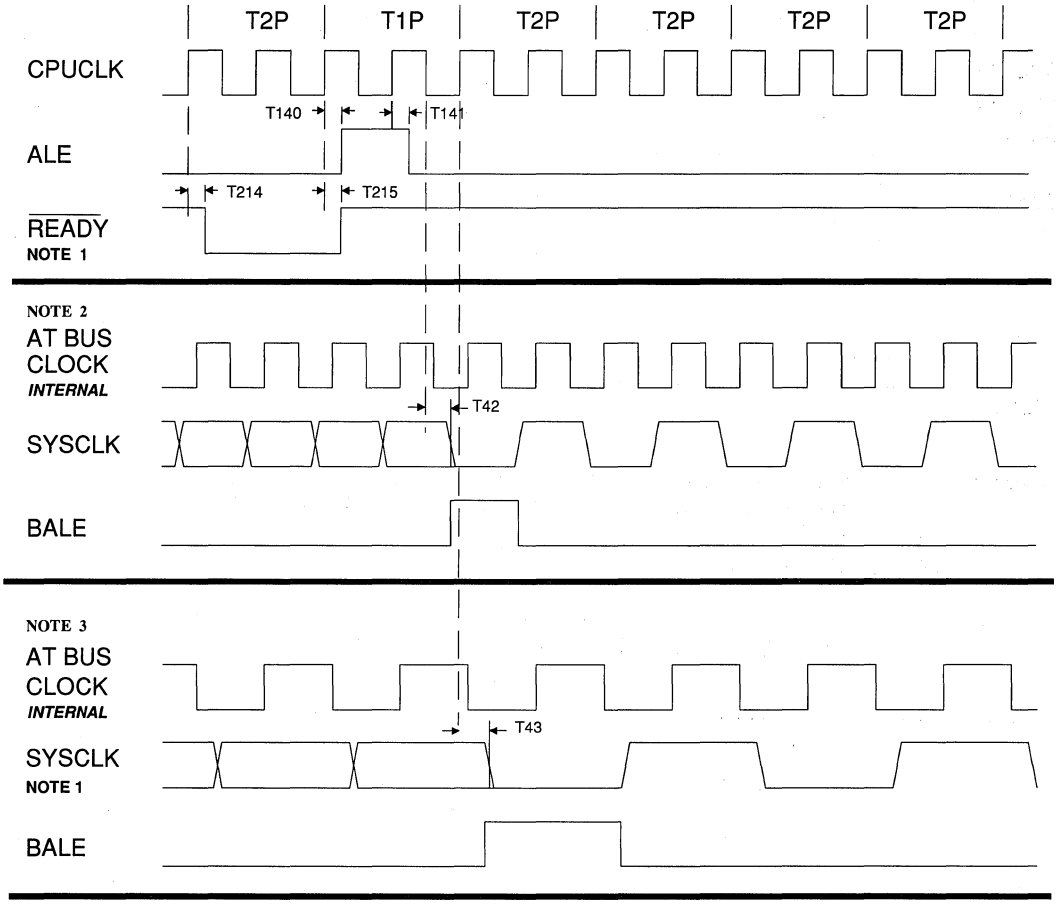
8



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 13-36. 80386SX - BREQ DELAY = 1 CLOCK



NOTE 1: If this AT bus cycle is immediatly preceded by another bus cycle and the BUS_MOD field in register 1872 = 11, READY will fall 1 CPUCLK later than shown.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

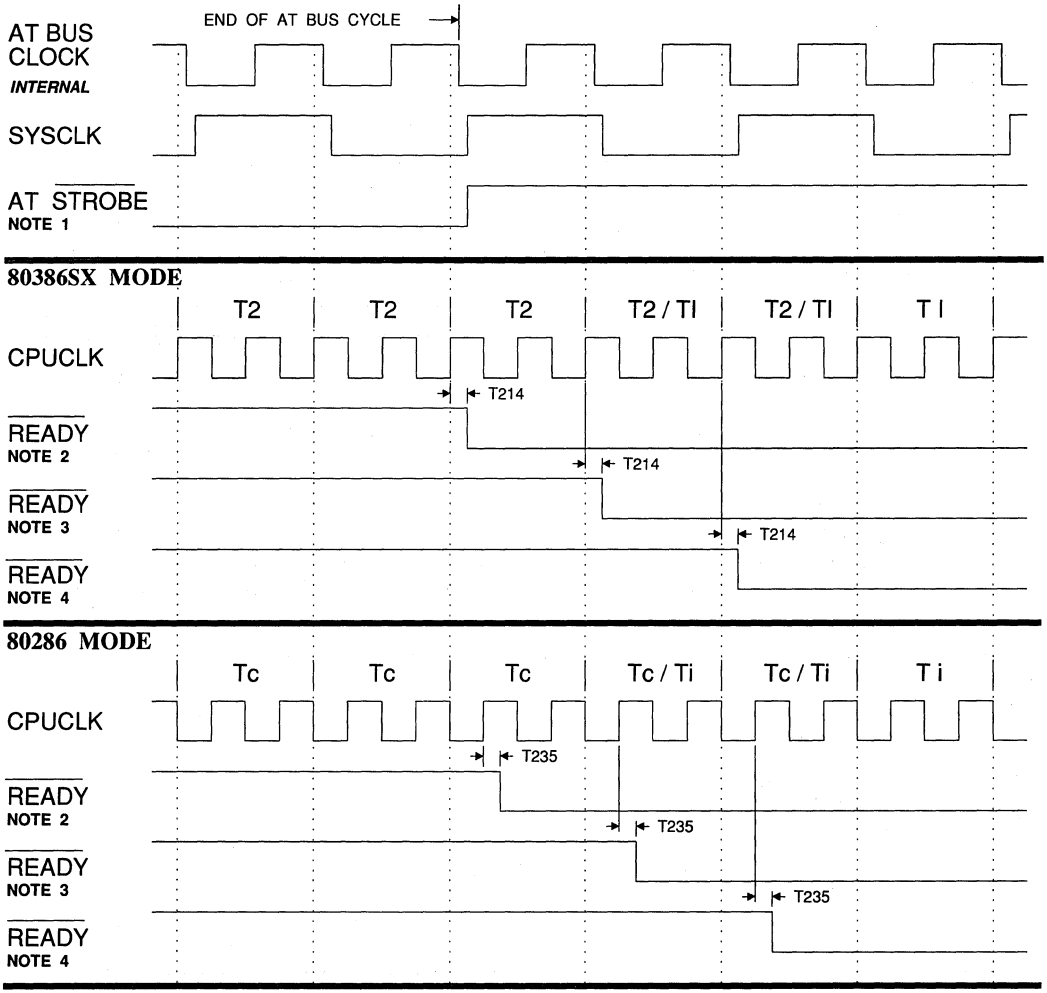
FIGURE 13-37. 80386SX CPU - SYCNHRONOUS CPUCLK TO SYSCLK

13.2.3 Exiting The AT Bus

Exiting a synchronous AT bus is covered first, followed by the asynchronous bus.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T46	SYSCLK fall to CPUCLK	-5		ns	Register 1872H: BAK_DEL = 10 BUS_MOD = 0X
T47	SYSCLK fall to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T48	SYSCLK rise to CPUCLK	-10		ns	Register 1872H: BAK_DEL = 00 BUS_MOD = 0X
T49	SYSCLK rise to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 11 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T144	CPUCLK fall to $\overline{\text{READY}}$ fall, 80286 CPU mode.		24	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T145	CPUCLK fall to $\overline{\text{READY}}$ rise, 80286 CPU mode.		26	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T214	See TABLE 13-6				
T215	See TABLE 13-6				
T234	See TABLE 13-3				
T235	See TABLE 13-3				

TABLE 13-10. EXITING THE AT BUS



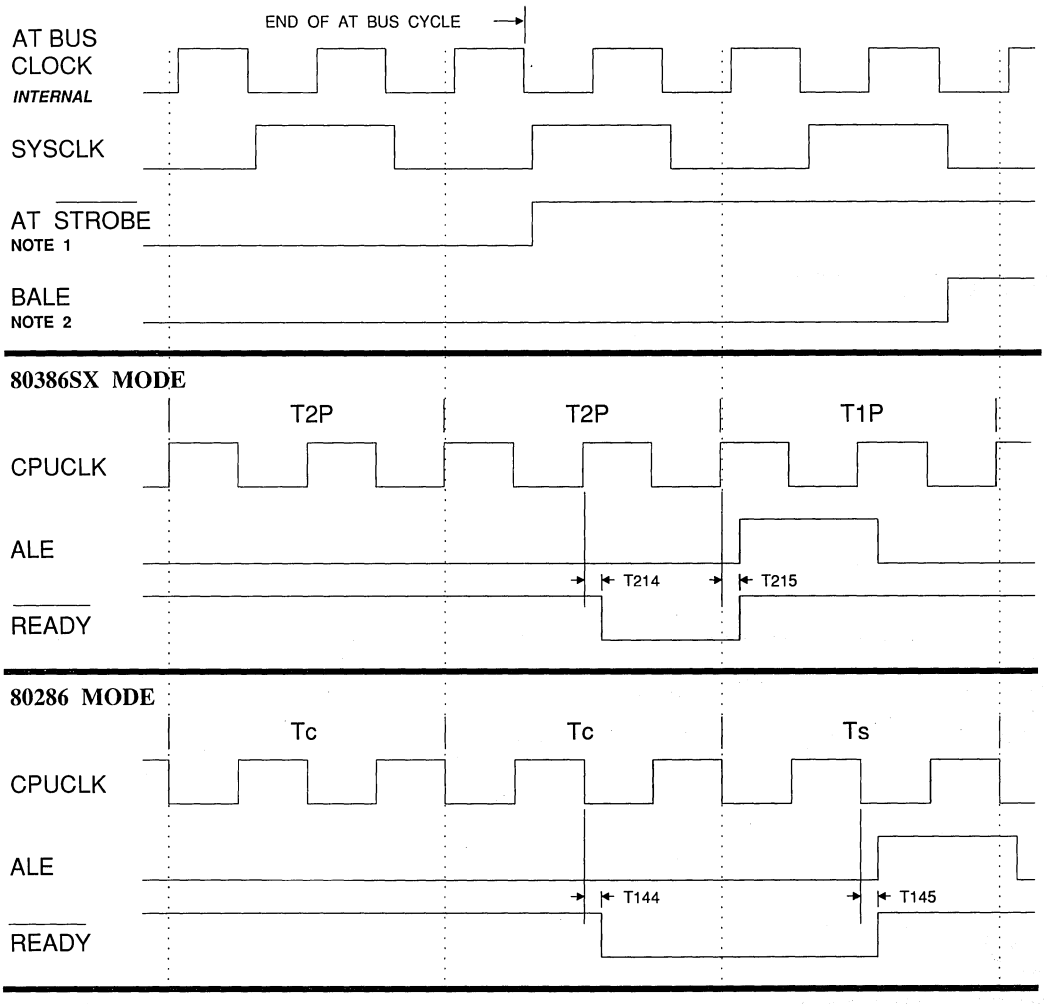
NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BUS_MOD = 10, BAK_DEL = 10 (-1 AT bus clock).

NOTE 3: Register 1872H: BUS_MOD = 10, BAK_DEL = 01 or 00 (-0.5 AT bus clock or no delay).

NOTE 4: Register 1872H: BUS_MOD = 10, BAK_DEL = 11 (+0.5 AT bus clock).

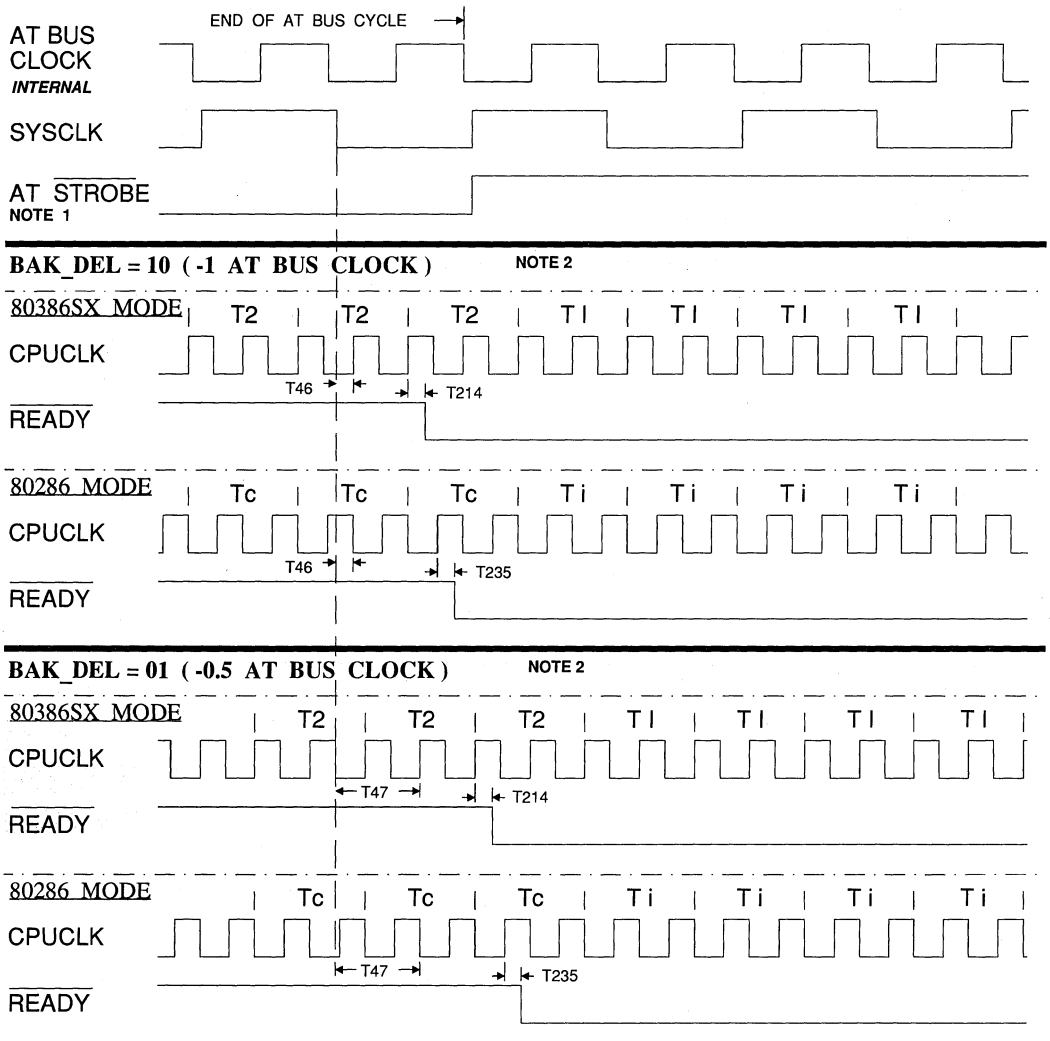
FIGURE 13-38. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 2



NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BRQ_DEL = 10, BUS_MOD = 11, BAK_DEL = XX.

FIGURE 13-39. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 1

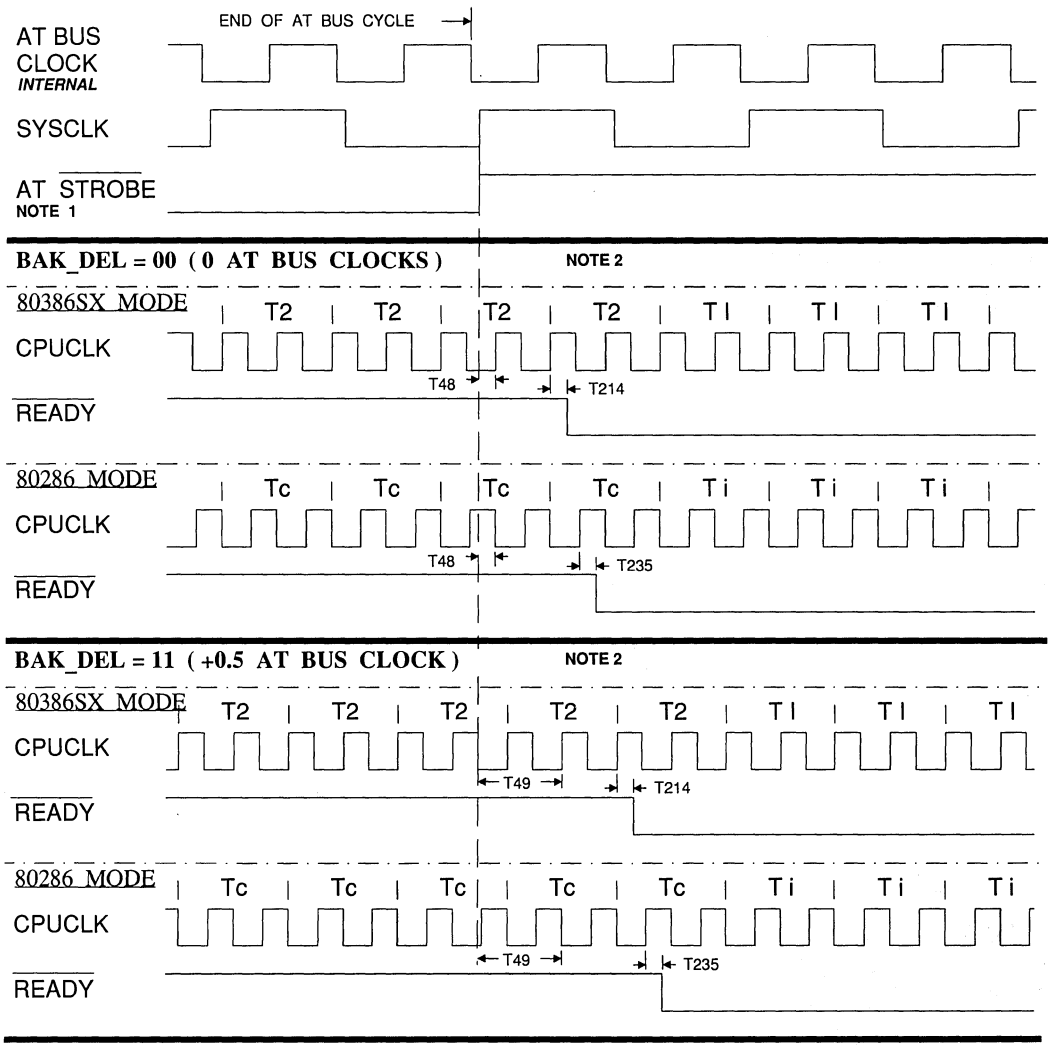


NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 13-40. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = -1 OR -0.5 AT BUS CLOCKS



NOTE 1: AT $\overline{\text{STROBE}}$ is either $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for $\overline{\text{READY}}$ to be asserted is shown here. Reducing the delay further would cause $\overline{\text{READY}}$ to be asserted one CPU "T" state later.

FIGURE 13-41. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = 0 OR +0.5 AT BUS CLOCKS

13.2.4 DMA Cycles

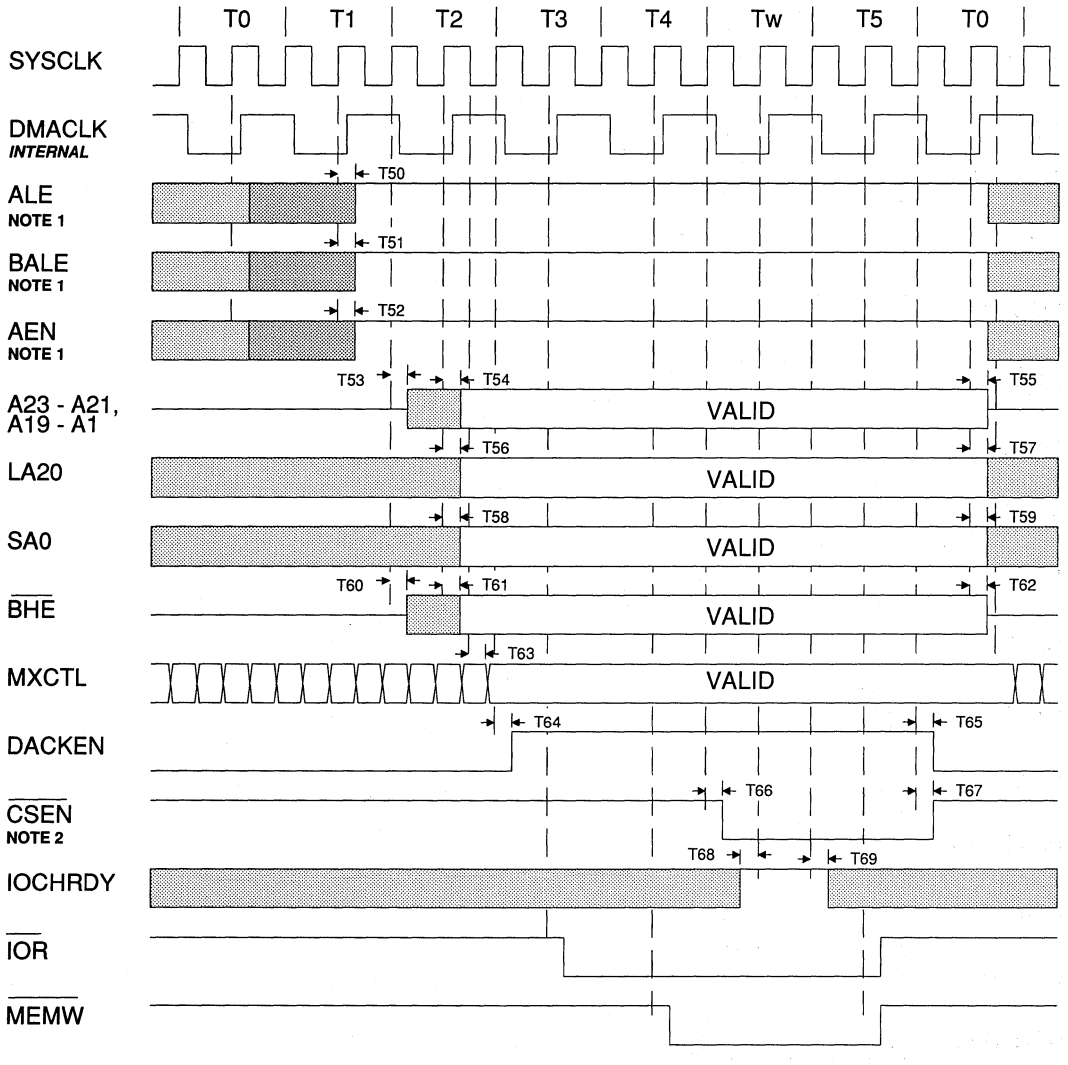
Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T54	SYSCLK rise to Address valid		60	ns	
T55	Address hold from SYSCLK rise	0		ns	
T56	SYSCLK rise to LA20 valid		49	ns	
T57	LA20 hold from SYSCLK rise	0		ns	
T58	SYSCLK rise to SA0 valid		40	ns	
T59	SA0 hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T66	SYSCLK rise to $\overline{CSEN}$ fall		32	ns	
T67	SYSCLK rise to $\overline{CSEN}$ rise		33	ns	
T68	IOCHRDY setup to SYSCLK rise	12		ns	
T69	IOCHRDY hold from SYSCLK rise	0		ns	
T70	SYSCLK rise to $\overline{IOR}$ fall		28	ns	
T71	SYSCLK rise to $\overline{IOR}$ rise		35	ns	
T72	SYSCLK rise to $\overline{MEMW}$ fall		47	ns	
T73	SYSCLK rise to $\overline{MEMW}$ rise		35	ns	
T74	SYSCLK rise to $\overline{DEN1}$ fall		32	ns	I/O to memory
T75	SYSCLK rise to $\overline{DEN1}$ rise		42	ns	I/O to memory
T76	SYSCLK rise to $\overline{DEN0}$ fall		32	ns	I/O to memory
T77	SYSCLK rise to $\overline{DEN0}$ rise		42	ns	I/O to memory
T78	SYSCLK rise to $\overline{SDEN}$ fall		21	ns	
T79	SYSCLK rise to $\overline{SDEN}$ rise		37	ns	I/O to memory

TABLE 13-11. DMA CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T80	SYSCLK rise to SDTR rise		30	ns	
T81	SYSCLK rise to SDTR fall		20	ns	
T82	SYSCLK rise to $\overline{IOW}$ fall		53	ns	
T83	SYSCLK rise to $\overline{IOW}$ rise		37	ns	
T84	SYSCLK rise to $\overline{MEMR}$ fall		17	ns	
T85	SYSCLK rise to $\overline{MEMR}$ rise		38	ns	
T86	SYSCLK rise to $\overline{DEN1}$ fall		22	ns	Memory to I/O
T87	SYSCLK rise to $\overline{DEN1}$ rise		116	ns	Memory to I/O
T88	SYSCLK rise to $\overline{DEN0}$ fall		22	ns	Memory to I/O
T89	SYSCLK rise to $\overline{DEN0}$ rise		116	ns	Memory to I/O
T90	SYSCLK rise to $\overline{SDEN}$ rise		116	ns	Memory to I/O
T91	SYSCLK rise to DTR rise		31	ns	
T92	SYSCLK rise to DTR fall		22	ns	
T100	$\overline{MEMW}$ fall to $\overline{RASn}$ fall		27	ns	
T101	$\overline{MEMW}$ rise to $\overline{RASn}$ rise		29	ns	
T102	$\overline{MEMW}$ fall to $\overline{CASn}$ fall		108	ns	
T103	$\overline{MEMW}$ rise to $\overline{CASn}$ rise		30	ns	
T105	$\overline{MEMW}$ fall to RA10 - RA0 valid		100	ns	
T107	$\overline{MEMW}$ fall to W/$\overline{R}$ high		29	ns	
T108	$\overline{MEMW}$ rise to W/$\overline{R}$ low	10		ns	
T120	$\overline{MEMR}$ fall to $\overline{RASn}$ fall		28	ns	
T121	$\overline{MEMR}$ rise to $\overline{RAS}$ rise		29	ns	
T122	$\overline{MEMR}$ fall to $\overline{CASn}$ fall		110	ns	
T123	$\overline{MEMR}$ rise to $\overline{CAS}$ rise		31	ns	
T125	$\overline{MEMR}$ fall to RA10 - RA0 valid		100	ns	
T126	$\overline{MEMR}$ fall to DPH, DPL float		25		
T127	$\overline{MEMR}$ rise to DPH, DPL driven	35			
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T305	D15 - D0 setup to $\overline{MEMR}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{MEMR}$ rise	10		ns	

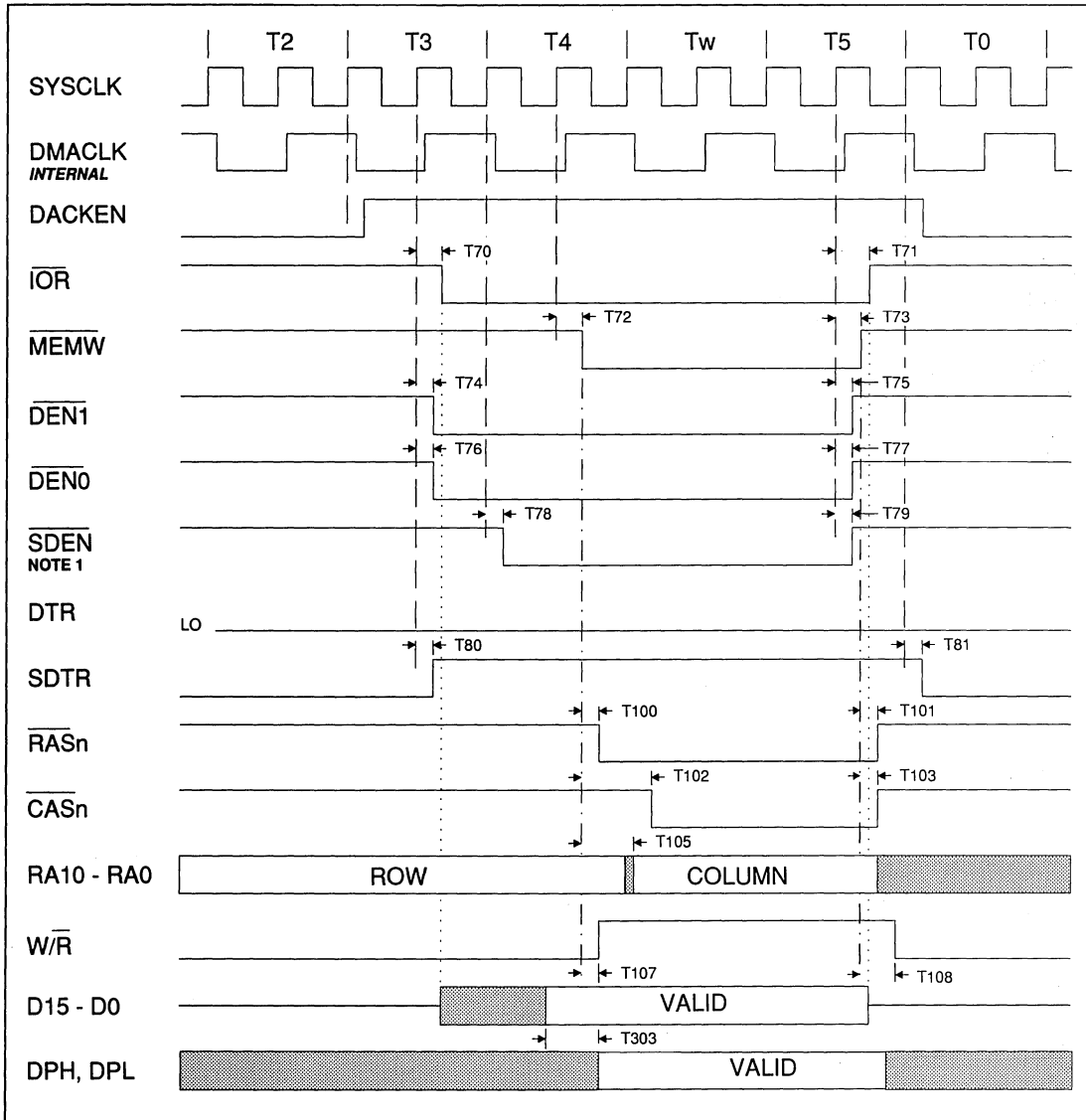
TABLE 13-11. DMA CYCLES cont.



NOTE 1: ALE, BALE and AEN may be asynchronous. Minimum valid time is shown. DMA channels 0, 1, 2, and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

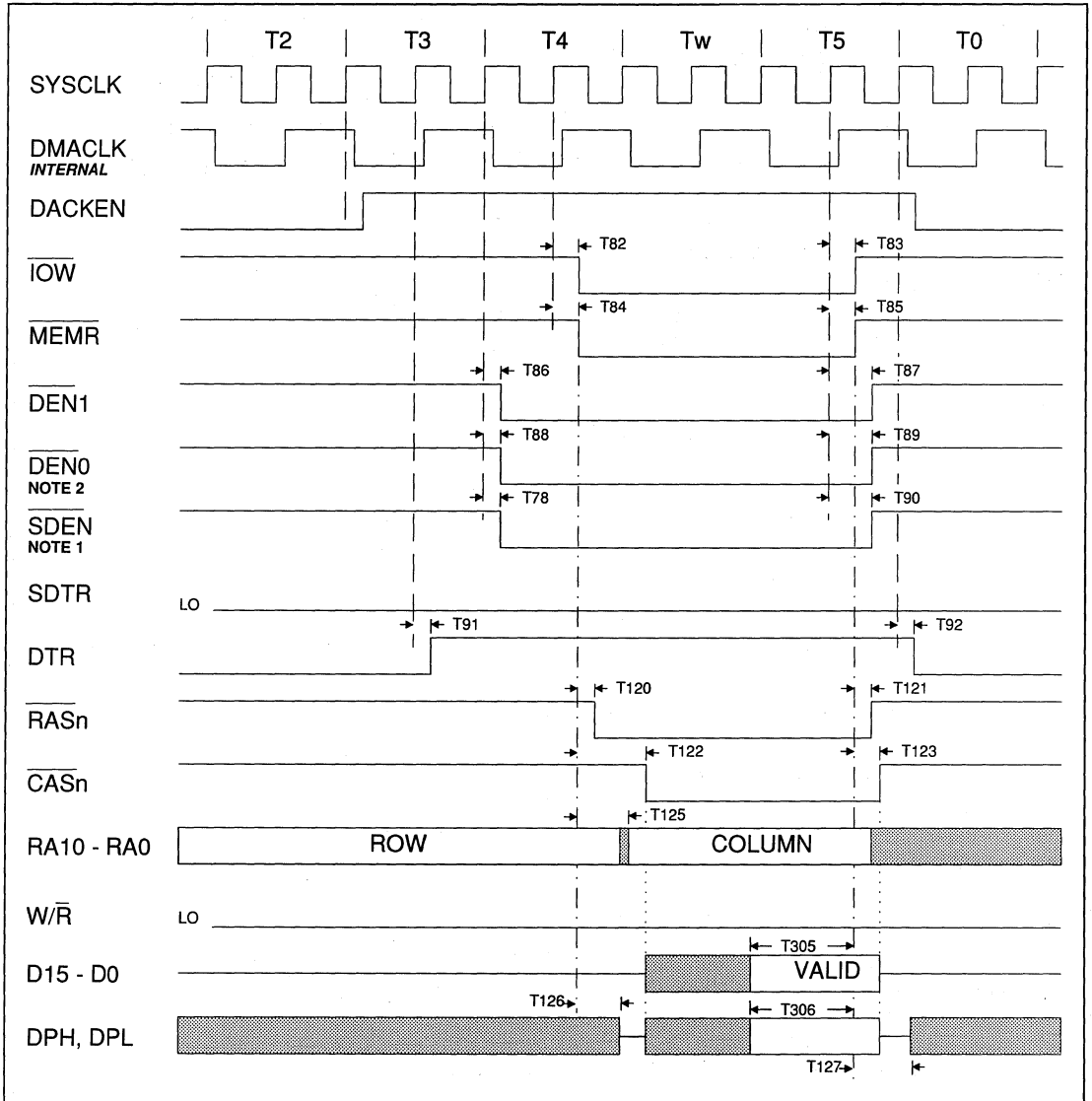
NOTE 2: $\overline{\text{CSEN}}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

FIGURE 13-42. BASIC DMA CYCLE, DEFAULT TIMING



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.

FIGURE 13-43. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY



NOTE 1: $\overline{\text{SDEN}}$ is asserted only in cycles with an odd numbered address.
NOTE 2: $\overline{\text{DEN0}}$ is asserted only in cycles with an even numbered address.

FIGURE 13-44. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O

13.2.5 AT Bus Master

The AT bus master timing is covered in the following sequence:

- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T55	Address hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T150	$\overline{MASTER}$ fall to AEN fall		30	ns	
T151	$\overline{MASTER}$ rise to AEN rise		30	ns	
T152	$\overline{MASTER}$ fall to A23 - A21, A19 - A1 float		30	ns	
T153	$\overline{MASTER}$ rise to A23 - A21, A19 - A1 driven	15		ns	
T154	$\overline{MASTER}$ fall to LA20 float		23	ns	
T155	$\overline{MASTER}$ rise to LA20 driven	10		ns	
T156	$\overline{MASTER}$ fall to SA0 float		24	ns	
T157	$\overline{MASTER}$ rise to SA0 driven	10		ns	
T158	$\overline{MASTER}$ fall to $\overline{BHE}$ float		30	ns	
T159	$\overline{MASTER}$ rise to $\overline{BHE}$ driven	10		ns	
T160	$\overline{MASTER}$ fall to $\overline{CSEN}$ fall		32	ns	
T161	$\overline{MASTER}$ rise to $\overline{CSEN}$ rise		35	ns	
T162	$\overline{MASTER}$ fall to $\overline{MEMR}$ float		24	ns	
T163	$\overline{MASTER}$ rise to $\overline{MEMR}$ driven	10		ns	
T164	$\overline{MASTER}$ fall to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, float		23	ns	
T165	$\overline{MASTER}$ rise to $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$ driven	10		ns	

TABLE 13-12. AT BUS MASTER CYCLE

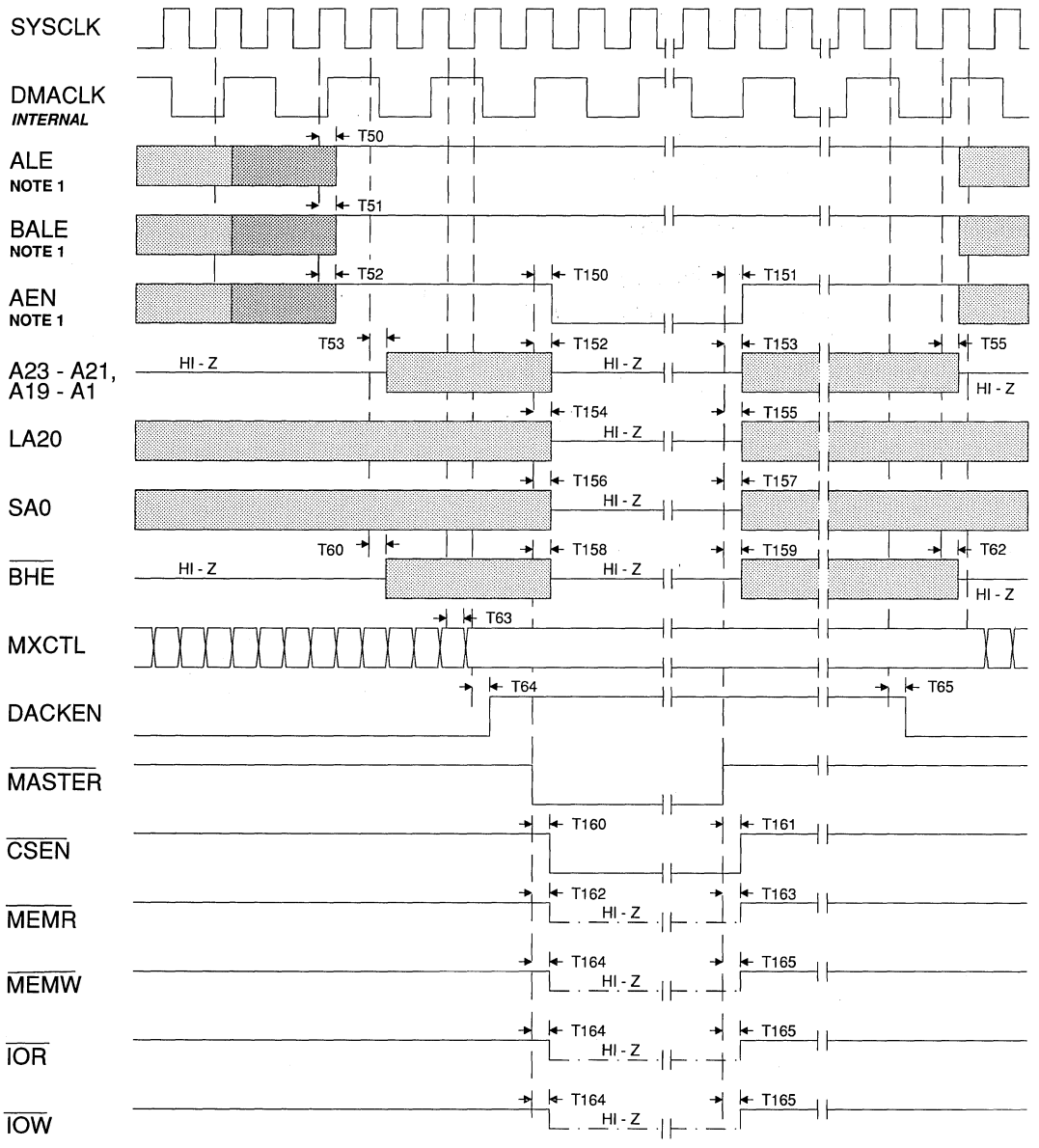
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T166	A23 - A21, A19 - A1 setup to MEMR, MEMW	45		ns	
T167	LA20 setup to MEMR, MEMW	50		ns	
T168	BHE setup to MEMR, MEMW	0		ns	
T169	SA0 setup to MEMR, MEMW	0		ns	
T170	A23 - A21, A19 - A1 hold from MEMR, MEMW	15		ns	
T171	LA20 hold from MEMR, MEMW	15		ns	
T172	BHE hold from MEMR, MEMW	15		ns	
T173	SA0 hold from MEMR, MEMW	15		ns	
T174	SA0 in to A0 out delay		45	ns	
T175	MEMW fall to DEN1 fall		30	ns	
T176	MEMW fall to DEN0 fall		30	ns	
T177	MEMW rise to DEN1 rise		83	ns	
T178	MEMW rise to DEN0 rise		83	ns	
T179	MEMR fall to DEN1 fall		85	ns	
T180	MEMR fall to DEN0 fall		85	ns	
T181	MEMR rise to DEN1 rise		32	ns	
T182	MEMR rise to DEN0 rise		32	ns	
T183	MEMR fall to DTR rise		29	ns	
T184	MEMR rise to DTR fall		82	ns	
T190	MEMR, MEMW fall to RASn fall		83	ns	
T191	MEMR, MEMW rise to RASn rise		33	ns	
T192	MEMR, MEMW fall to CASn fall		126	ns	
T193	MEMR, MEMW rise to CASn rise		33	ns	
T194	MEMR, MEMW fall to RA10 - RA0 column address valid		120	ns	
T196	MEMR, MEMW fall to RA10 - RA0 row address valid		42	ns	
T197	RA10 - RA0 column address hold from MEMR, MEMW rise	5		ns	

TABLE 13-12. AT BUS MASTER CYCLE cont.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T300	$\overline{MEMW}$ fall to W/$\overline{R}$ rise		33	ns	
T301	$\overline{MEMW}$ rise to W/$\overline{R}$ fall	10		ns	
T302	$\overline{MEMW}$ fall to DPH, DPL valid		32	ns	
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T304	DPH, DPL hold from $\overline{MEMW}$ rise	5		ns	
T305	D15 - D0 setup to $\overline{MEMR}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{MEMR}$ rise	10		ns	
T307	$\overline{MEMR}$ fall to DPH, DPL float		35	ns	
T308	$\overline{MEMR}$ rise to DPH, DPL driven	58		ns	

TABLE 13-12. AT BUS MASTER CYCLE cont.

8



NOTE 1: The shaded regions of ALE, BALE and AEN show a possible asynchronous relarionship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

FIGURE 13-45. AT BUS MASTER, BUS ACQUISITION/RELEASE

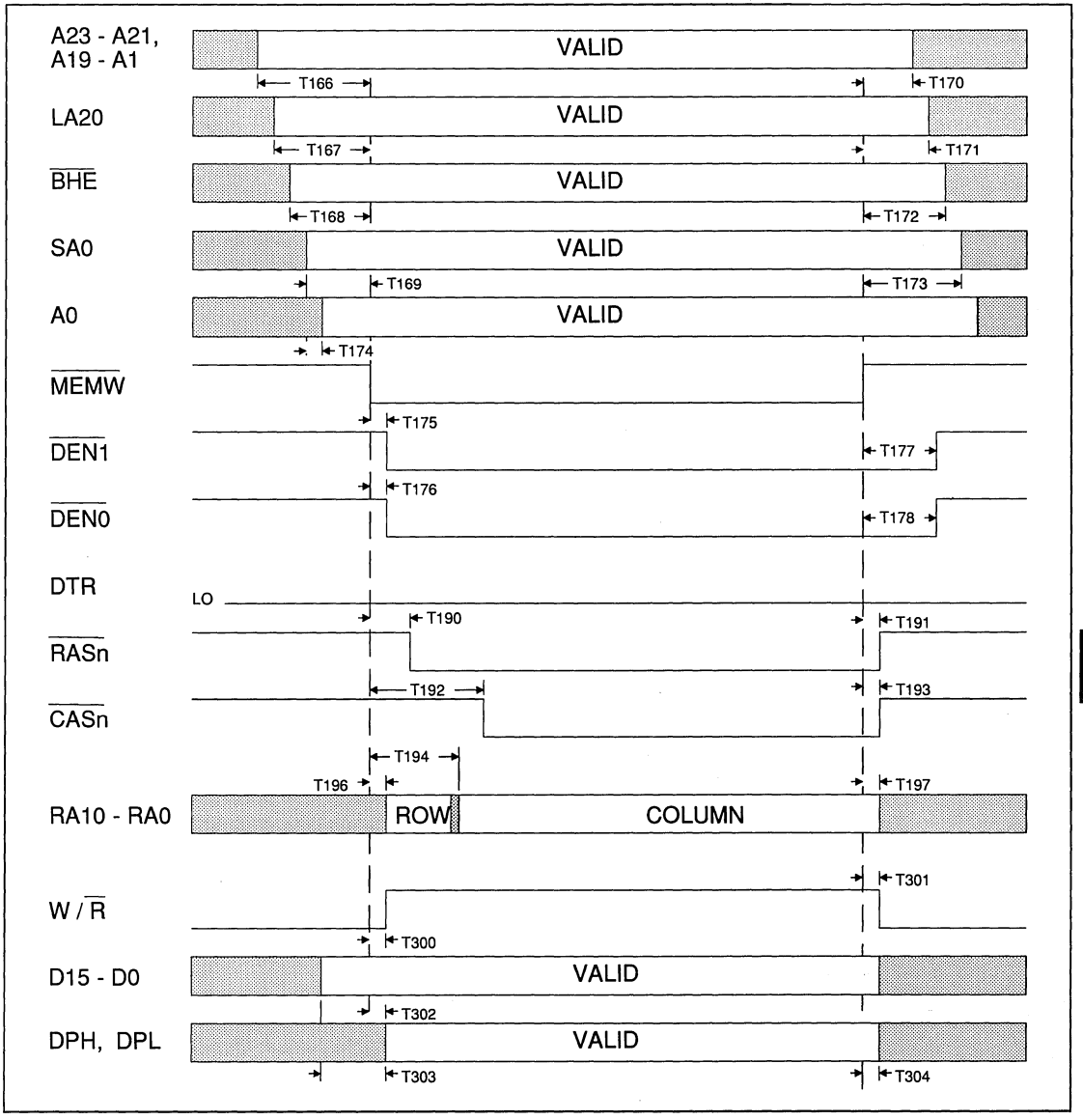


FIGURE 13-46. AT BUS MASTER, WRITE TO ON-BOARD MEMORY

8

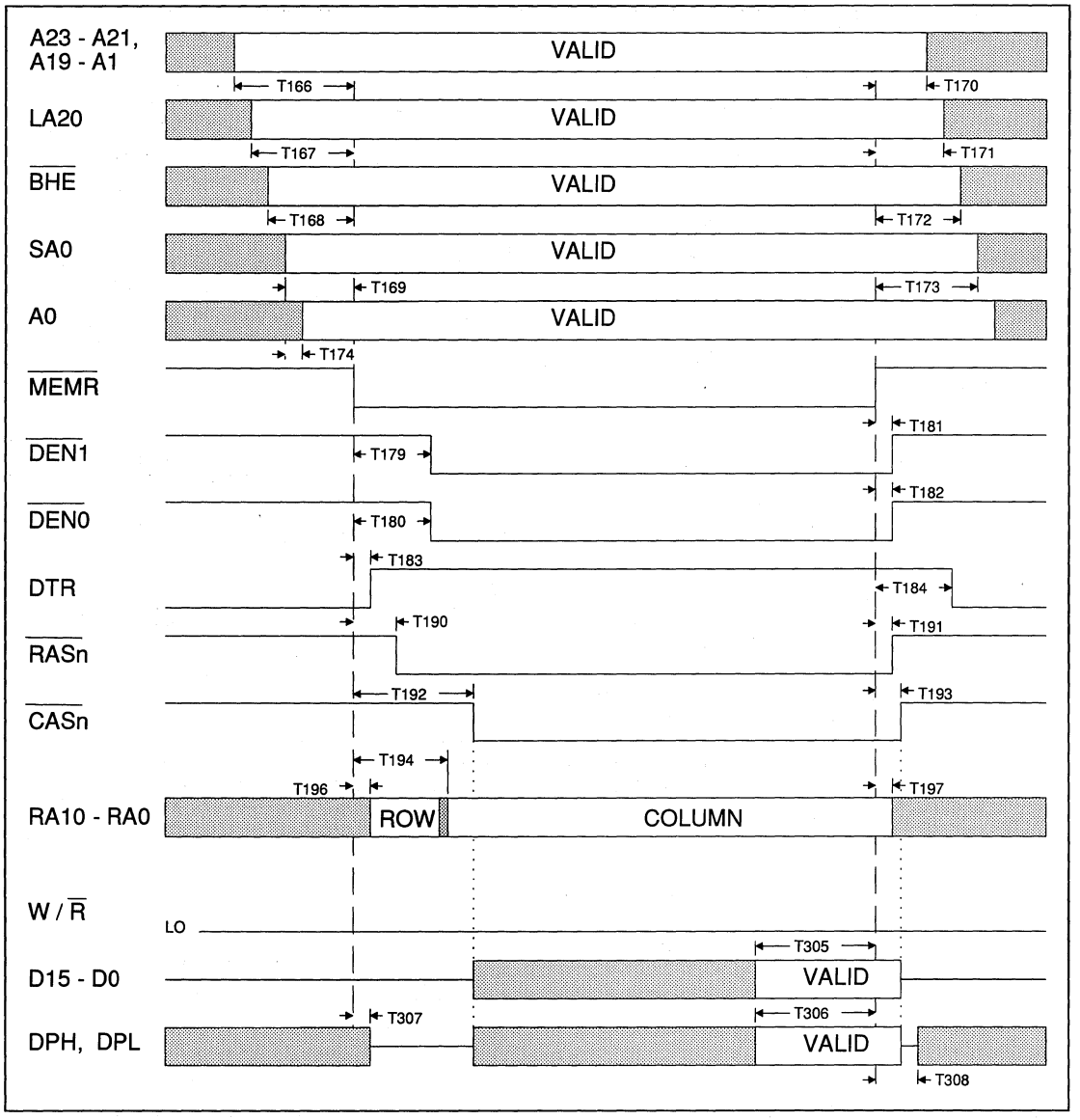


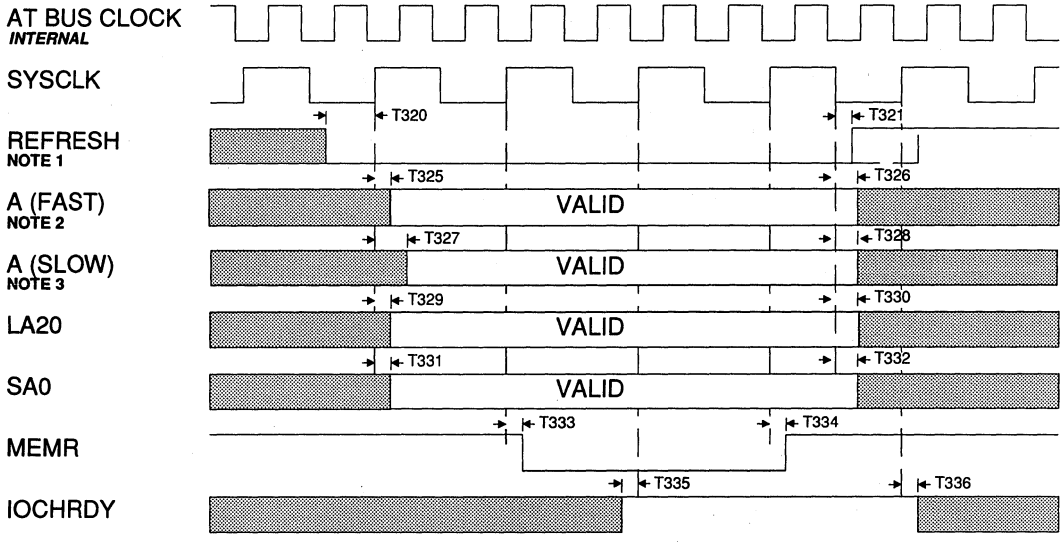
FIGURE 13-47. AT BUS MASTER, READ FROM ON-BOARD MEMORY

13.2.6 AT Bus Refresh

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T320	$\overline{\text{REFRESH}}$ low before SYSCLK rise	4		ns	$\overline{\text{REFRESH}}$ setup is number given plus (T00 × 0.25)
T321	SYSCLK fall to $\overline{\text{REFRESH}}$ rise		16	ns	
T325	SYSCLK rise to A23 - A21, A19 - A16 and A7 - A1 valid		35	ns	
T326	SYSCLK fall to A23 - A21, A19 - A16 and A7 - A1 invalid	2		ns	
T327	SYSCLK rise to A20, A15 - A8 valid		45	ns	
T328	SYSCLK fall to A20, A15 - A8 invalid	2		ns	
T329	SYSCLK rise to LA20 valid		30	ns	
T330	SYSCLK fall to LA20 invalid	2		ns	
T331	SYSCLK rise to SA0 valid		30	ns	
T332	SYSCLK fall to SA0 invalid	2		ns	
T333	SYSCLK rise to $\overline{\text{MEMR}}$ low		8	ns	
T334	SYSCLK rise to $\overline{\text{MEMR}}$ high		7	ns	
T335	IOCHRDY setup to SYSCLK rise	23		ns	
T336	IOCHRDY hold time from SYSCLK rise	0		ns	

TABLE 13-13. AT BUS REFRESH CYCLE, DEFAULT TIMING

8



NOTE 1: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

NOTE 2: (FAST) is address lines A23 - A21, A19 - A16 and A7 - A1.

NOTE 3: (SLOW) is address lines A20, and A15 - A8

FIGURE 13-48. AT BUS REFRESH CYCLE, DEFAULT TIMING

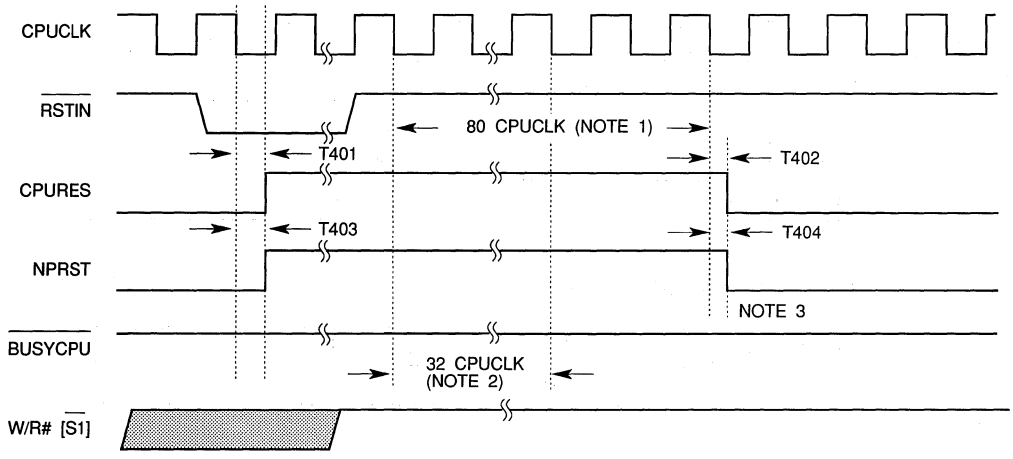
13.3 PROCESSOR TIMING

This section covers the 80286 CPU timing, followed by the 80386SX.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T140	See Table 13-9				
T141	See Table 13-9				
T143	See Table 13-9				
T401	CPUCLK fall to CPURES rise delay		14	ns	
T402	CPUCLK fall to CPURES fall delay		13	ns	
T403	CPUCLK fall to NPRST rise delay		14	ns	
T404	CPUCLK fall to NPRST fall delay		13	ns	
T405	CPUCLK fall to $\overline{\text{BUSYCPU}}$ fall delay		35	ns	①
T406	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35	ns	①
T408	$\overline{\text{S0}}$, $\overline{\text{S1}}$ setup time to CPUCLK	9		ns	
T409	$\overline{\text{S0}}$, $\overline{\text{S1}}$ hold time to CPUCLK	1		ns	
T410	M/$\overline{\text{IO}}$ setup time to CPUCLK	26		ns	
T411	M/$\overline{\text{IO}}$ hold time to CPUCLK	1		ns	
T412	Address setup time to CPUCLK	26		ns	
T413	Address hold time to CPUCLK	1		ns	
T414	$\overline{\text{PEACK}}$ setup time to CPUCLK	7		ns	
T415	$\overline{\text{PEACK}}$ hold time to CPUCLK	1		ns	
T416	DPH, DPL setup time to CPUCLK fall	5		ns	
T417	DPH, DPL hold time from CPUCLK fall	19		ns	
T418	D15 - D0 setup time to CPUCLK fall	5		ns	
T419	D15 - D0 hold time from CPUCLK fall	19		ns	

① T405 and T406 are for reference only since $\overline{\text{BUSYCPU}}$ is an asynchronous signal to the 80286. These two parameters are guaranteed by design and will not be tested.

TABLE 13-14. 80286 CPU TIMING

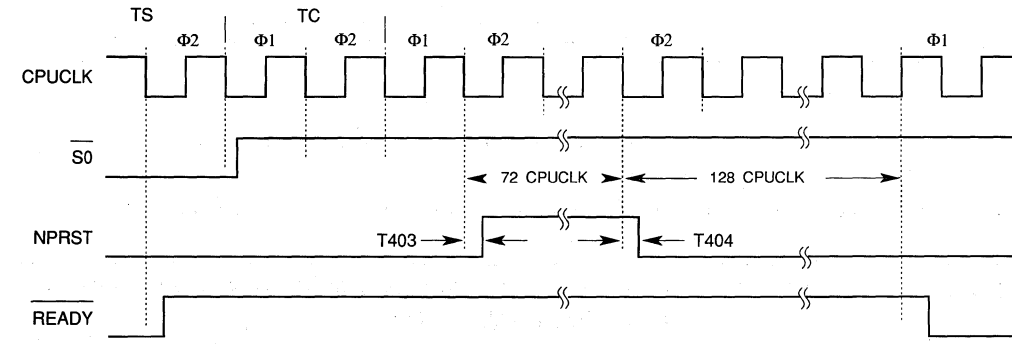


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

FIGURE 13-49. 80286 - CPURES AND NPRST DURING POWER UP

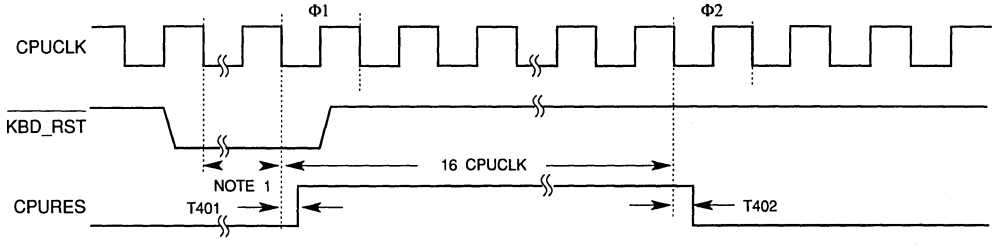


NOTE 1: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

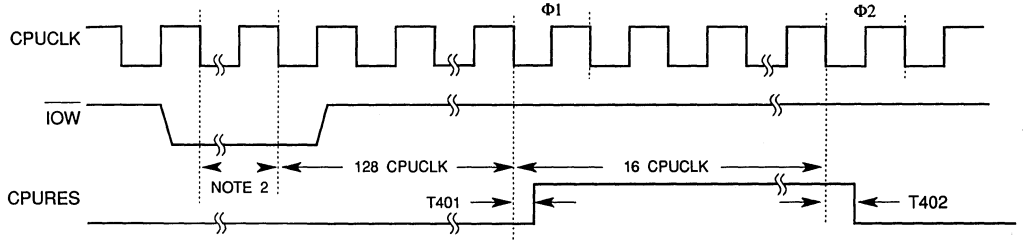
NOTE 2: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's C287A.

FIGURE 13-50. 80286 - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1

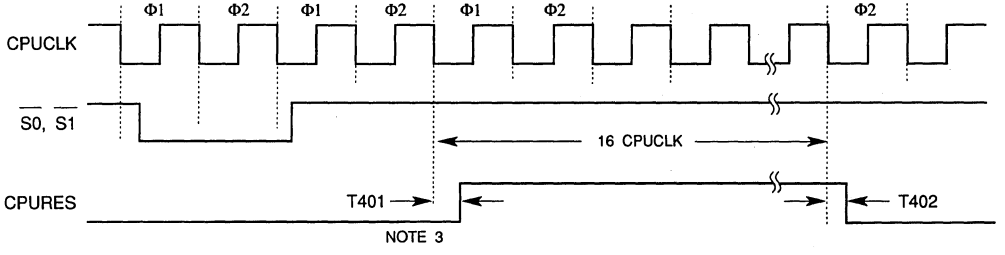
Keyboard Controller Initiated Reset



Hot-Reset by setting bit 0 of port 92 to 1



Shut-down initiated Reset ($\overline{M/IO}$=1, $\overline{S1}$=0, $\overline{S0}$=0, A1=0)



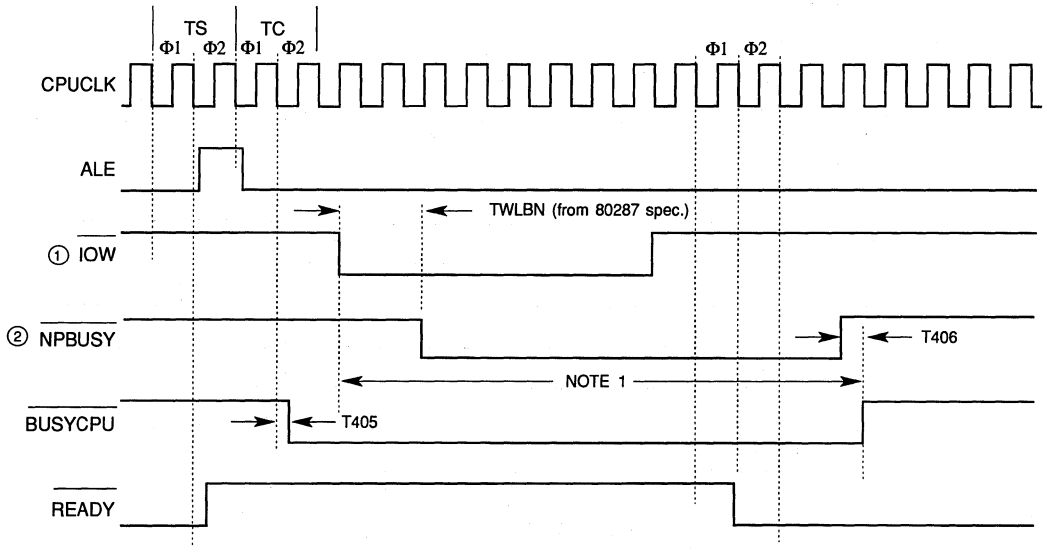
NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is asserted at the beginning of phase 1 to maintain the phase relationship with the 80286.

FIGURE 13-51. 80286 - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

8

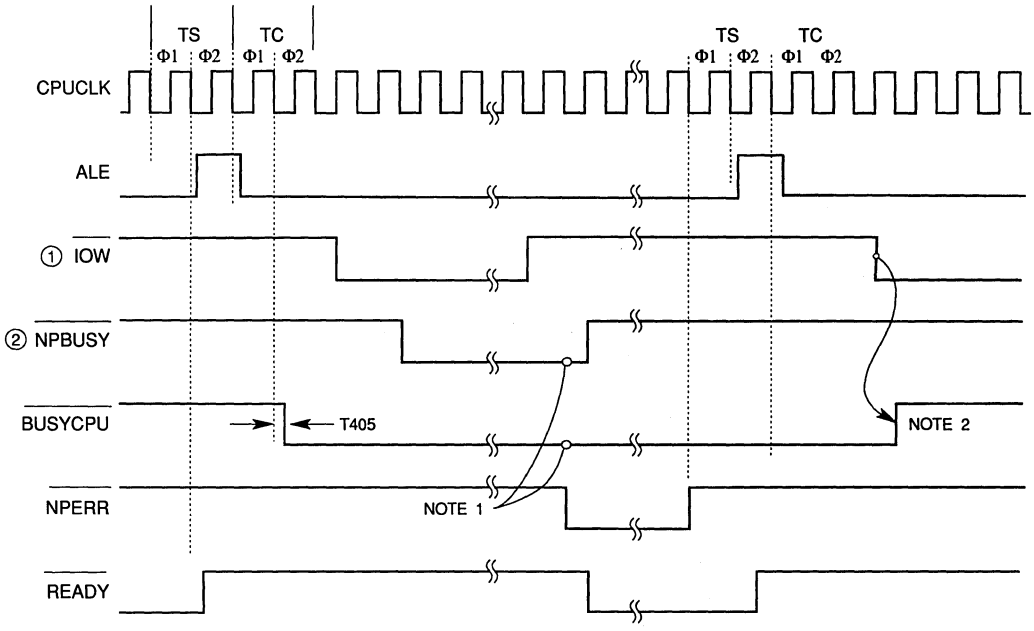


① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: During a write to the 80287, BUSYCPU is asserted at the middle of the first Tc and continues for one SYSCLK plus two CPUCLKs beyond the active edge of IOW, then follows the NPBUSY from the 80287. This early assertion of BUSYCPU is required to maintain compatibility with the 80287.

FIGURE 13-52. 80286 - BUSYCPU ASSERTED DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is still active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW, delayed by a low half of SYSCLK, when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

FIGURE 13-53. 80286 - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

8

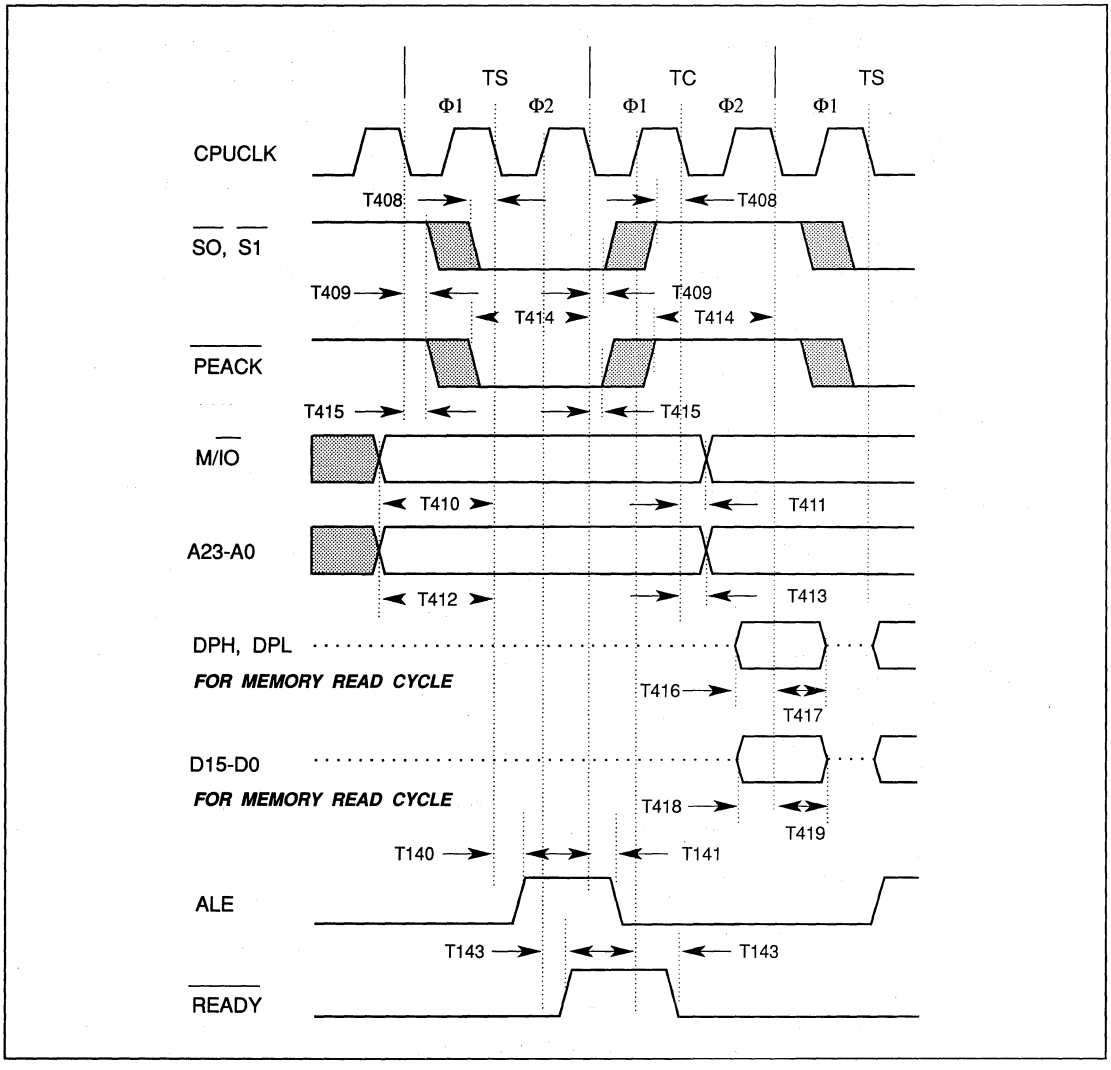


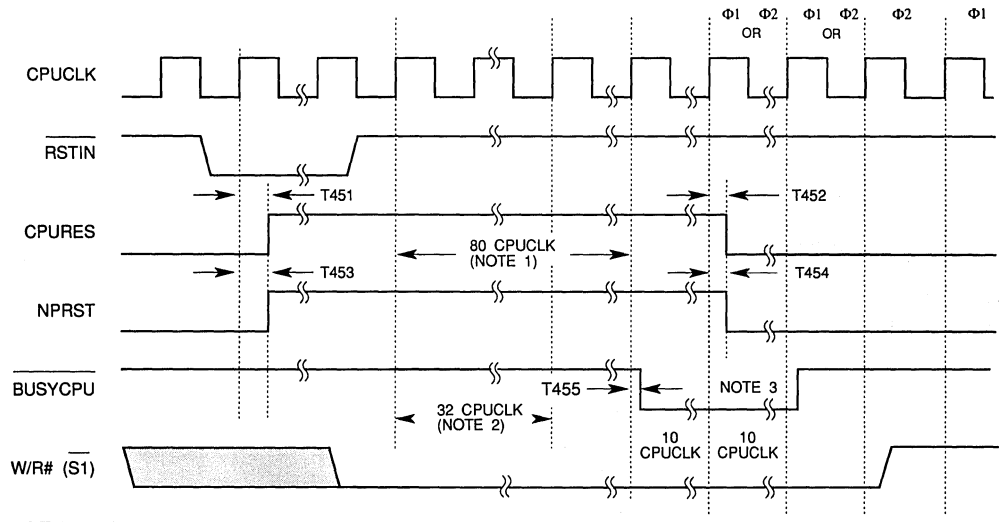
FIGURE 13-54. 80286 - MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T140	See Table 13-9					
T141	See Table 13-9					
T204	See Table 13-6					
T214	See Table 13-6					
T215	See Table 13-6					
T451	CPUCLK rise to CPURES rise delay		14		10	ns
T452	CPUCLK rise to CPURES fall delay		13		10	ns
T453	CPUCLK rise to NPRST rise delay		14		10	ns
T454	CPUCLK rise to NPRST fall delay		13		10	ns
T455	CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay		35		35	ns
T456	CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay		35		30	ns
T457	$\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay		30		30	ns
T458	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35		35	ns
T460	$\overline{\text{NPERR}}$ fall to EPEREQ rise delay		30		30	ns
T462	ADS# setup time to CPUCLK rise	14		10		ns
T463	ADS# hold time from CPUCLK rise	5		4		ns
T464	W/R# setup time to CPUCLK rise	14		8		ns
T465	W/R# hold time from CPUCLK rise	5		4		ns
T466	D/C# setup time to CPUCLK rise	14		6		ns
T467	D/C# hold time from CPUCLK rise	5		4		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise	17		15		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	5		4		ns
T470	$\overline{\text{BHE}}$ setup time to CPUCLK rise	17		15		ns
T471	$\overline{\text{BHE}}$ hold time from CPUCLK rise	3		4		ns

TABLE 13-15. 80386SX CPU TIMING

SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T472	HLDA setup time to CPUCLK rise	10		6		ns
T473	HLDA hold time from CPUCLK rise	3		4		ns
T474	HOLD valid delay from CPUCLK rise		26		20	ns
T475	DPH setup time to CPUCLK rise	5		5		ns
T476	DPH hold time from CPUCLK rise	19		19		ns
T477	D15-D0 setup time to CPUCLK rise	5		5		ns
T478	D15-D0 hold time from CPUCLK rise	19		19		ns
T479	A23-A1, BLE# setup time to CPUCLK rise	40		38		ns
T480	A23-A1, BLE# hold time from CPUCLK rise	3		4		ns

TABLE 13-15. 80386SX CPU TIMING cont.



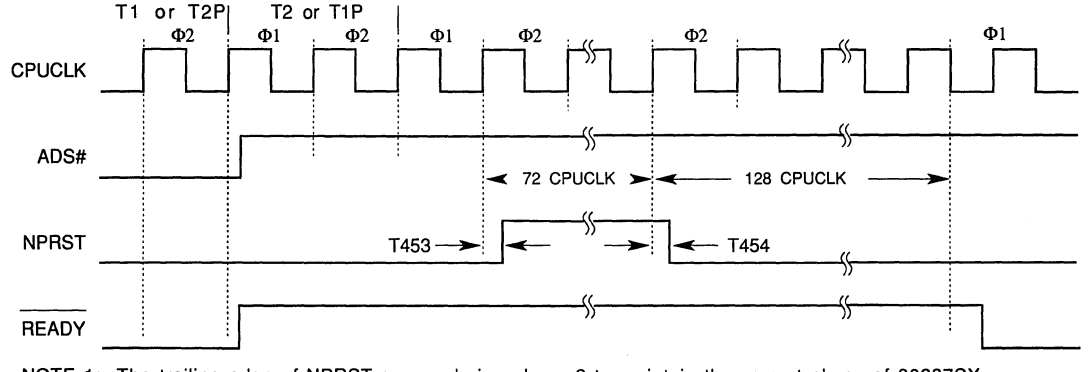
NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

8

FIGURE 13-55. 80386SX - CPURES AND NPRST DURING POWER UP



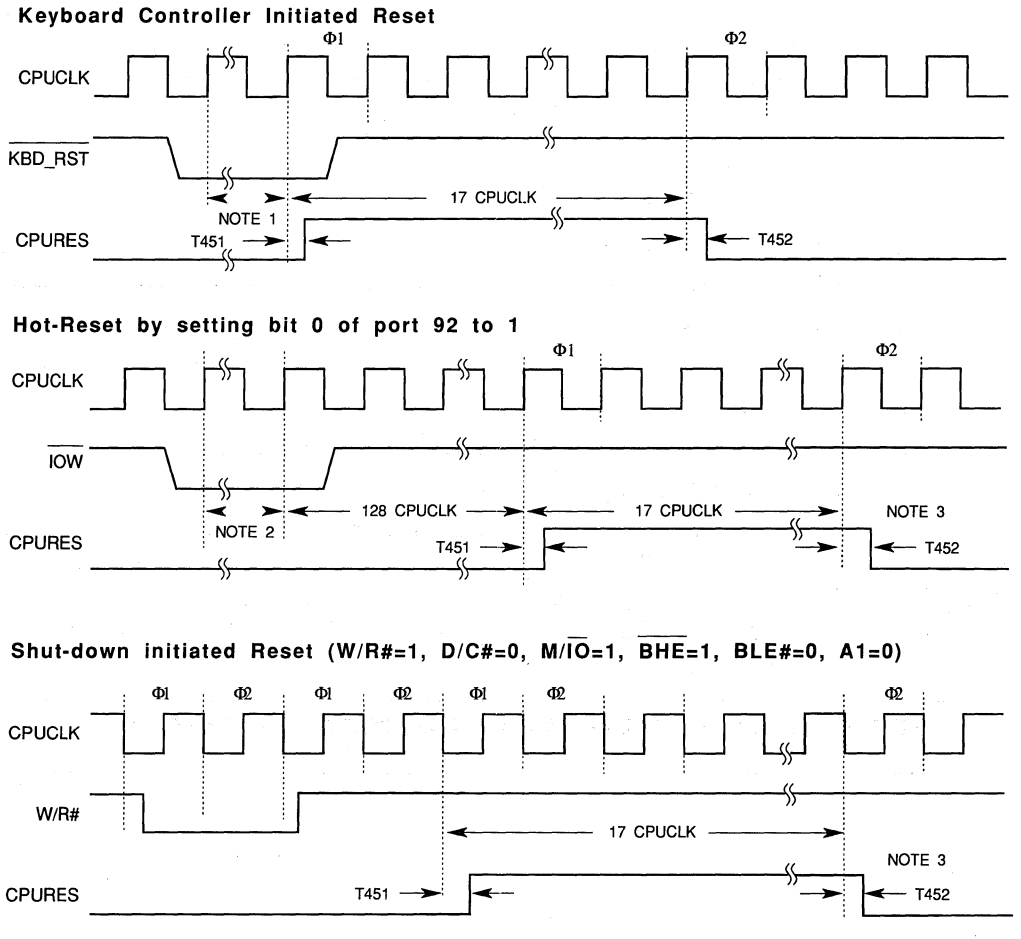
NOTE 1: The trailing edge of NPRST occurs during phase 2 to maintain the correct phase of 80387SX with the 80386SX.

NOTE 2: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 3: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's 80C287A.

NOTE 4: 25 MHz operation requires a minimum of 8 MHz for AT Bus Clock.

FIGURE 13-56. 80386SX - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1



NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

FIGURE 13-57. 80386SX - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

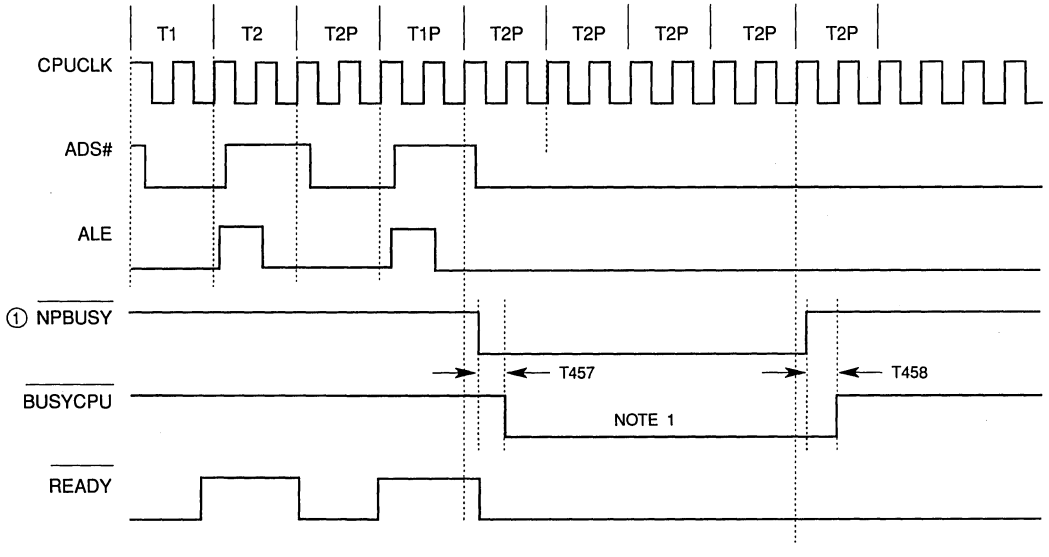
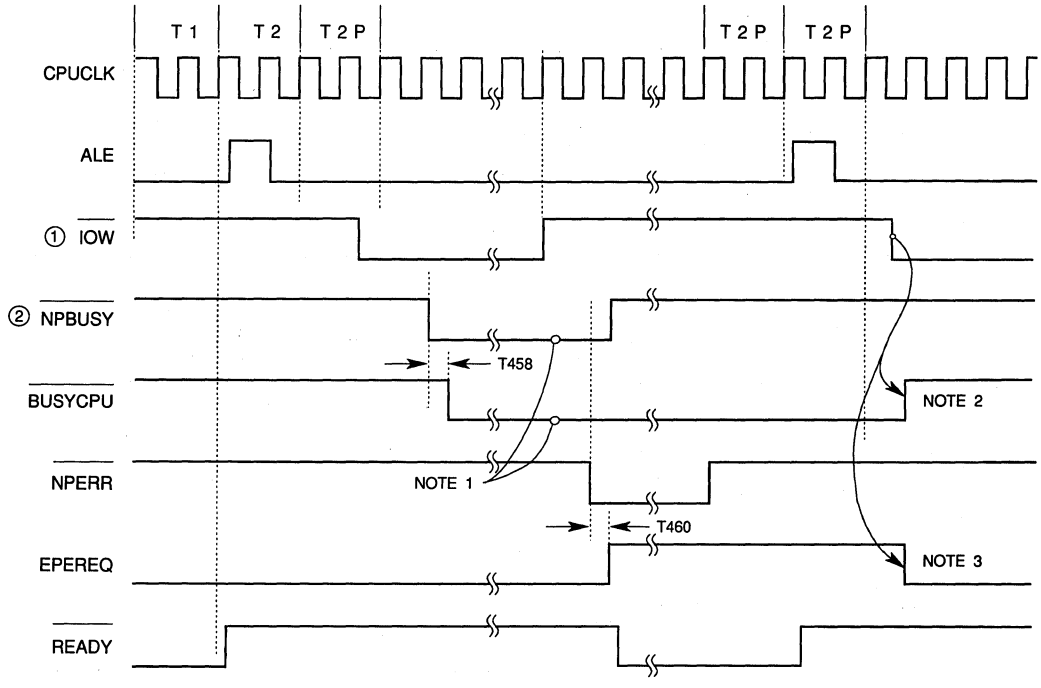


FIGURE 13-58. BUSYCPU ASSERTION DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW delayed by a low half of SYSCLK when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

NOTE 3: EPEREQ is asserted if NPERR occurs while NPBUSY from the coprocessor is active. EPEREQ is de-asserted by the leading edge of IOW delayed by the low half of SYSCLK when any data is written to port F0. EPEREQ can be asynchronous to the processor and is shown for reference only.

FIGURE 13-59. 80386SX - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

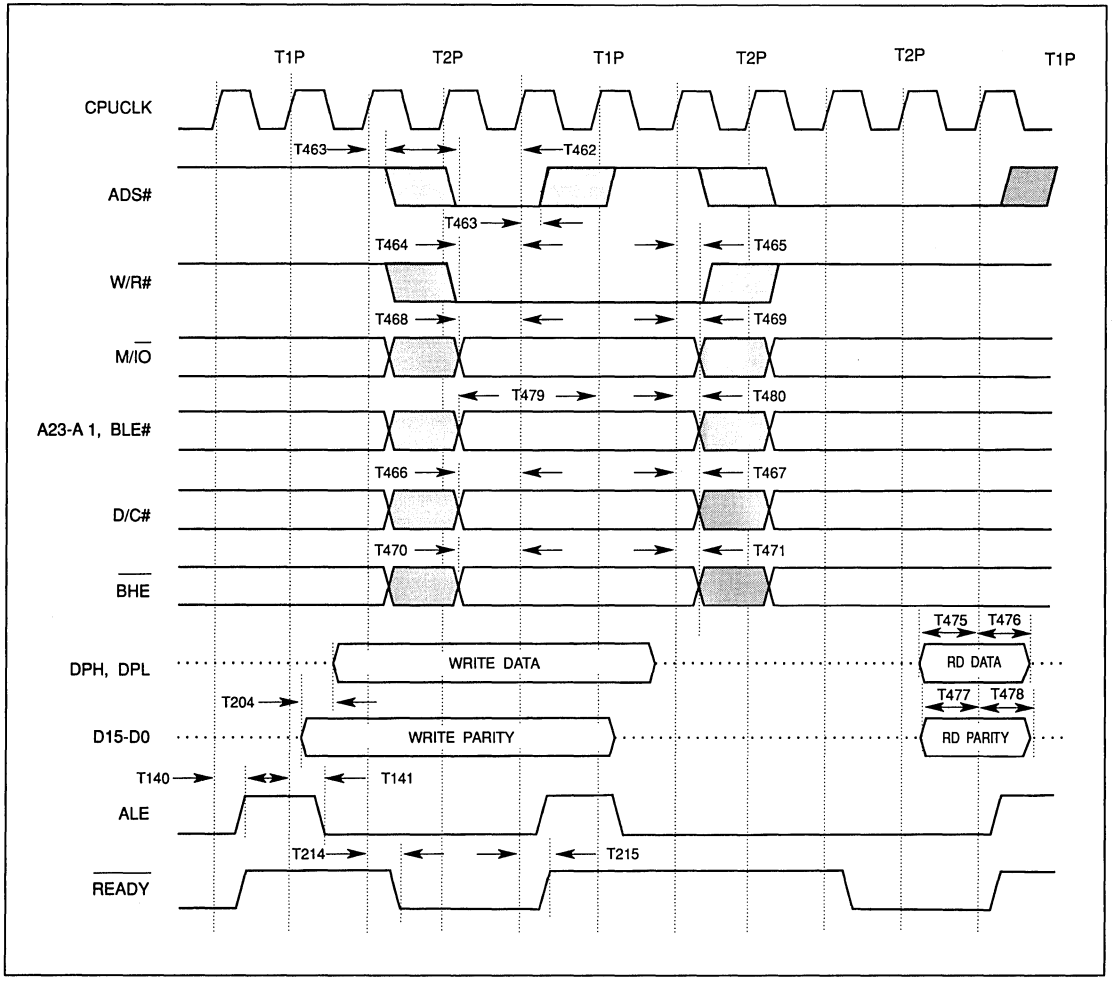


FIGURE 13-60. 80386SX - MISCELLANEOUS TIMING

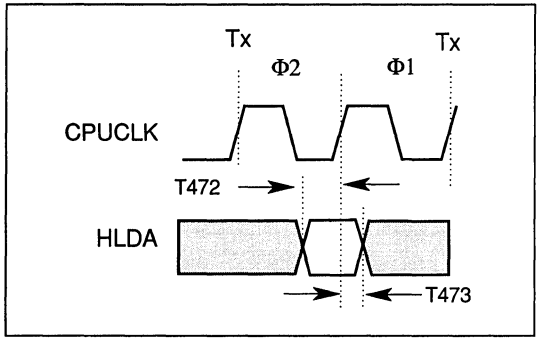


FIGURE 13-61. 80386SX - INPUT SETUP AND HOLD TIMING

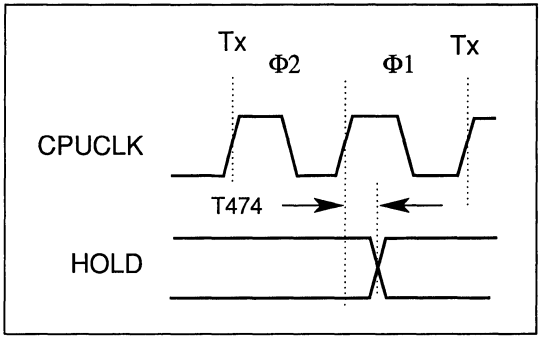


FIGURE 13-62. 80386SX - OUTPUT DELAY TIMING

13.4 CACHE CONTROLLER TIMING

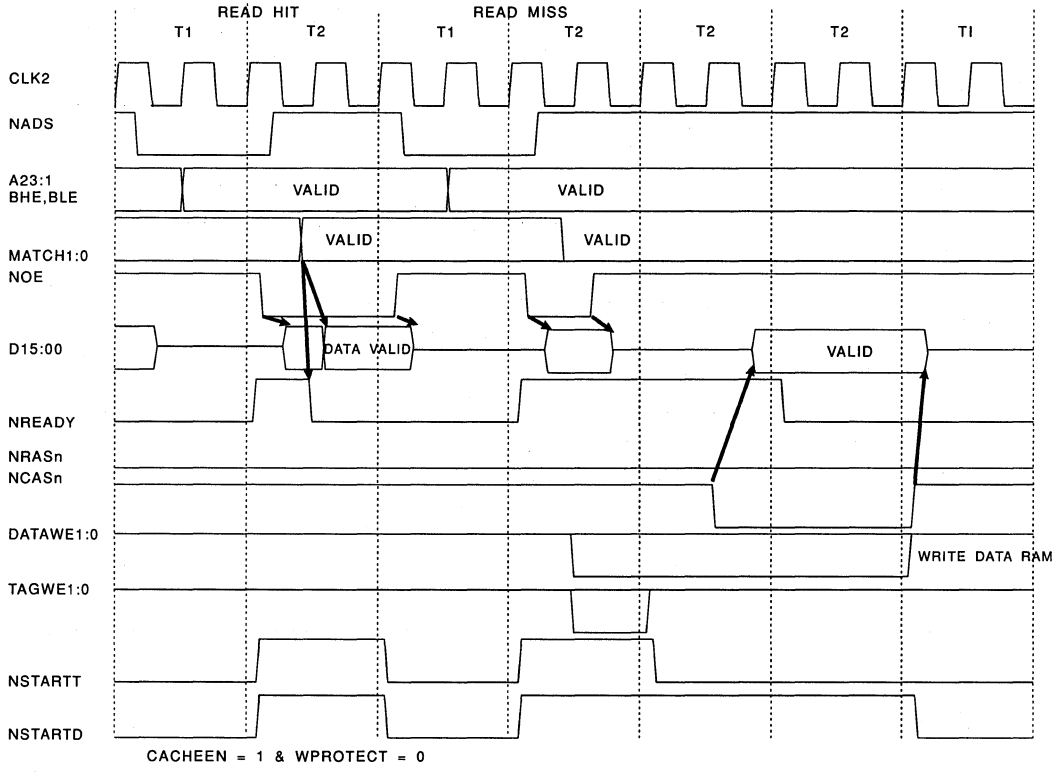


FIGURE 13-63. READ HIT/READ MISS CYCLE

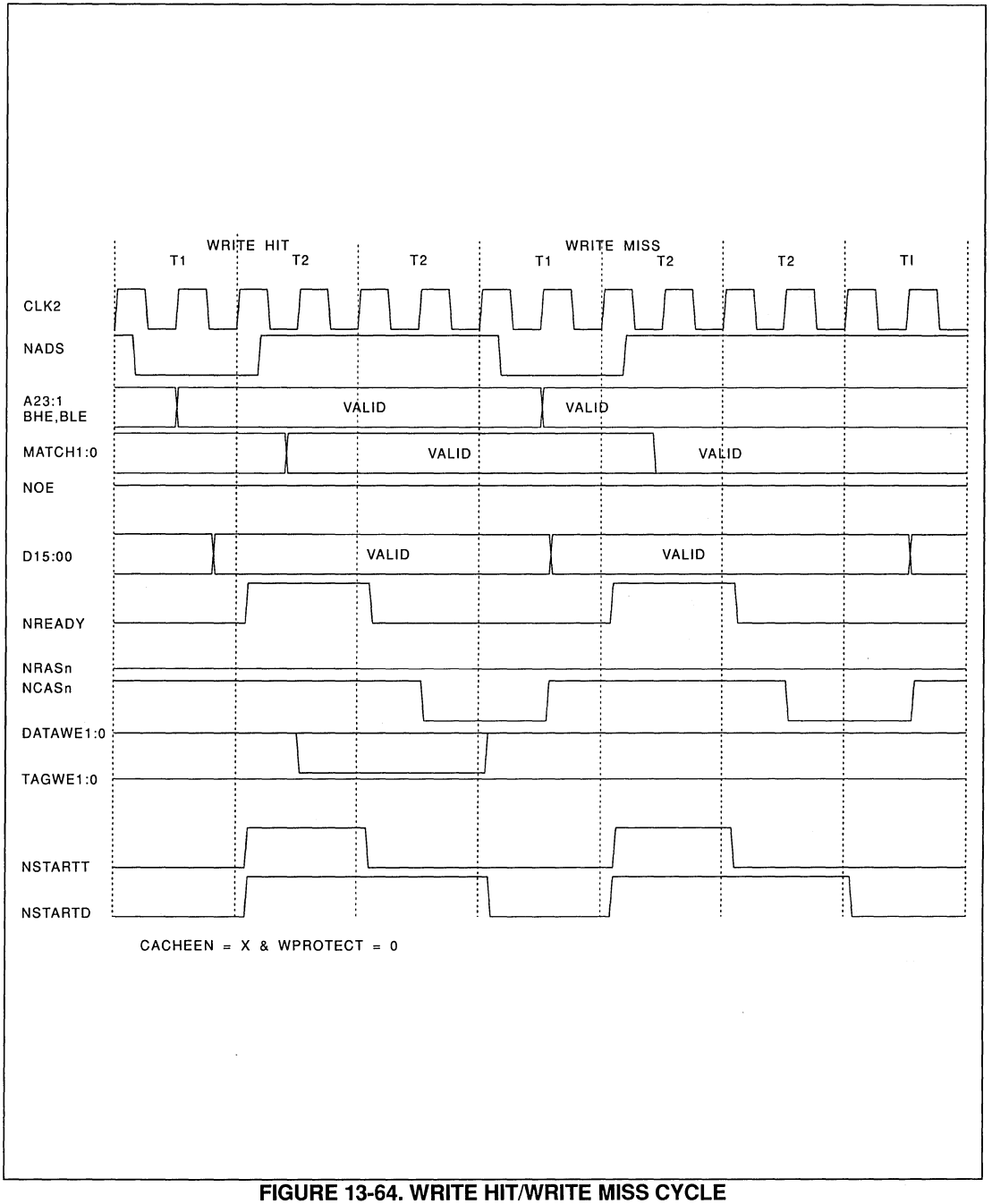


FIGURE 13-64. WRITE HIT/WRITE MISS CYCLE

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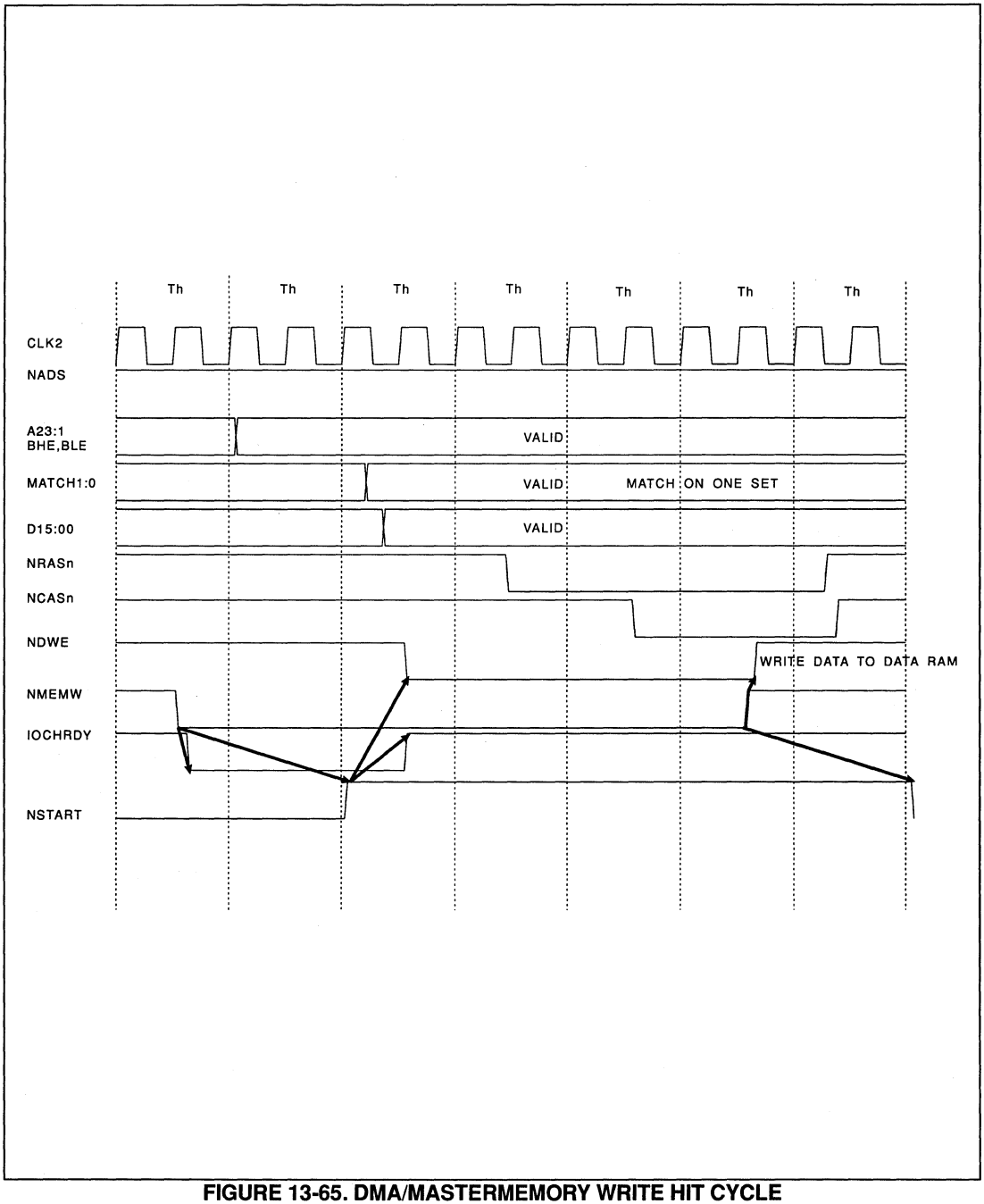

FIGURE 13-65. DMA/MASTERMEMORY WRITE HIT CYCLE

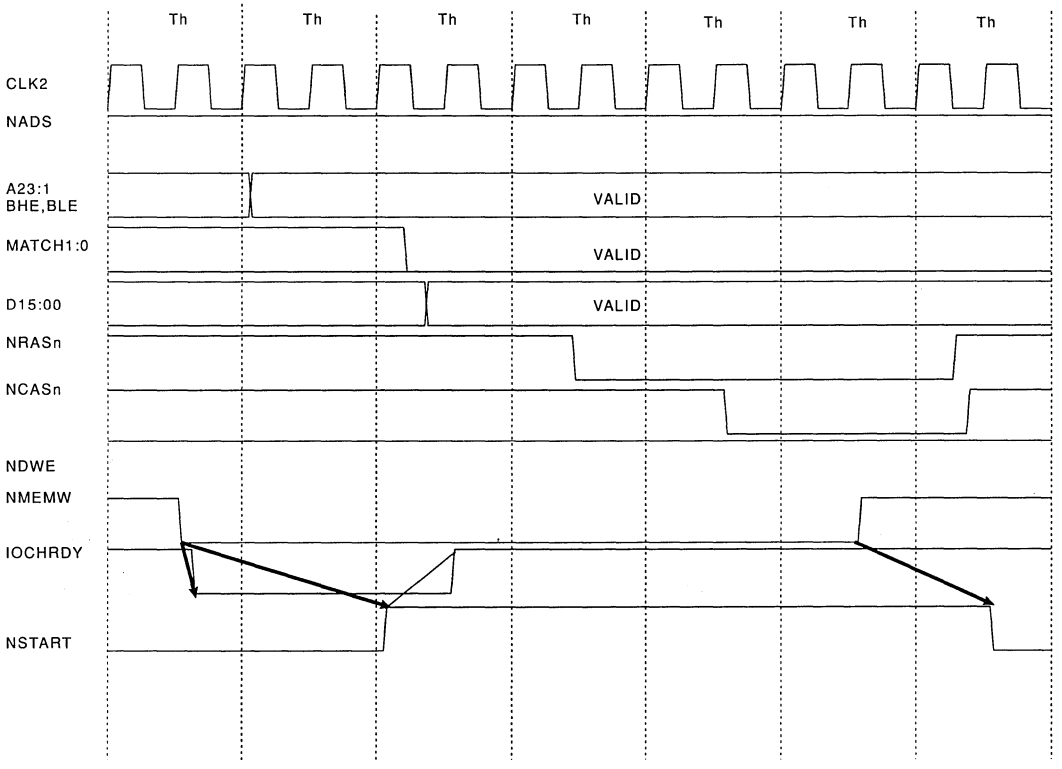

FIGURE 13-66. DMA/MASTER MEMORY WRITE MISS CYCLE

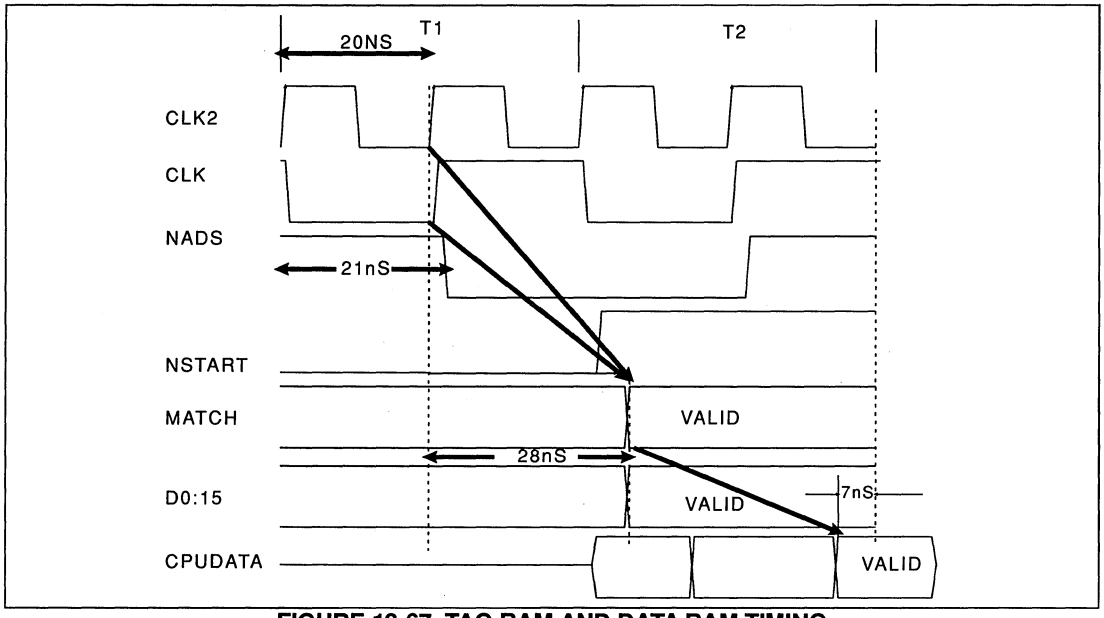

FIGURE 13-67. TAG RAM AND DATA RAM TIMING

ICS90C61A

Dual Video/Memory

Clock Generator

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

LIST OF TABLES

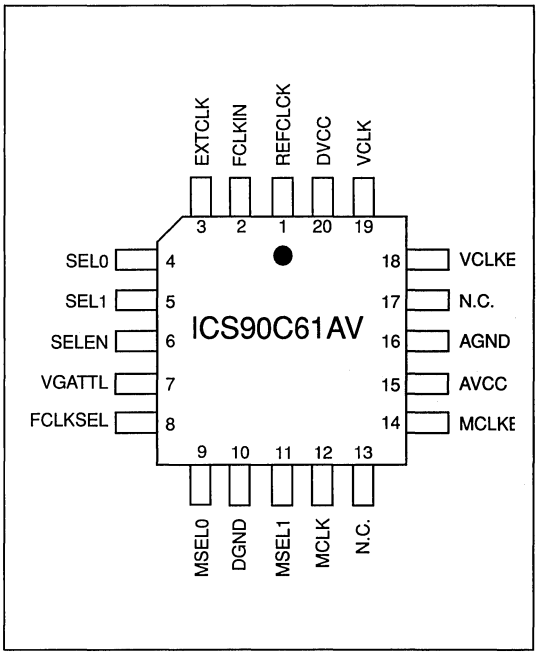
PREFACE

The Integrated Circuit Systems ICS90C61A dual video/memory clock generator was designed exclusively to work with Western Digital video graphics chips.

Because you get optimum video subsystem performance when you use this video/memory clock generator with Western Digital video graphics chips, we have included the ICS90C61A in our databook.

You can contact Integrated Circuit Systems at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
Valley Forge, PA 19482
Phone: (215) 666-1900
Fax: (215) 666-1099



20-PIN PLCC DIAGRAM

1.0 INTRODUCTION

The Integrated Circuit Systems ICS90C61A is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 DESCRIPTION

The Integrated Circuit Systems Video Graphics Array Clock Generator (ICS90C61A) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 7 internally generated frequencies or two external inputs. The selection of the video dot clock frequency is done through four inputs.

- SEL0
- SEL1
- VGATTL
- FCLKSEL

SEL0 and SEL1 are latched by the SELEN signal. VGATTL and FCLKSEL are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

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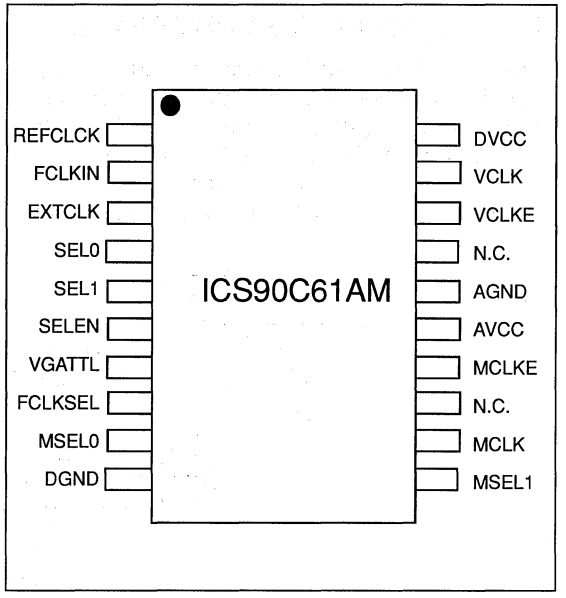
The input and truth table have been designed to allow a direct connection to one of the many Western Digital VGA controllers or 8514/A chip sets.

The MCLK output is one of four internally generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

The ICS90C61A is capable of extended frequency output up to 80 MHz in custom applications. See page 9-6 for details.



20-PIN S.O.DIAGRAM

1.2 FEATURES

- Dual Clock generator for the IBM-compatible Western Digital Video Graphics Array (VGA) LSI devices, and 8514/A chip sets.
- Integral loop filter components.
- Generates 7 video clock frequencies derived from a 14.318 MHz system clock reference frequency.
- Video clock is selectable among the 7 internally generated clocks and two external clocks.
- On-chip generation of four memory clock frequencies.
- CMOS technology.
- Available in a 20-pin PLCC, S.O., and DIP packages.
- Extended frequency capabilities to 80 MHz in custom frequency patterns.

Ordering Information

ICS90C61AV-PRx (PLCC Package)
ICS90C61AM-PRx (S.O. Package)
ICS90C61AN-PRx (DIP Package)
(PRx = Pattern Number)

Note: Unless a specific pattern is ordered, PR2 will be shipped.

Note: ICS90C61AN (DIP) pinout is identical to ICS90C61AM (S.O.) pinout.

2.0 ICS90C61A VGA INTERFACE

The ICS90C61A has two system interfaces: System Bus and VGA Controller, and six user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock ICS90C61A is connected to a VGA controller. Western Digital VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video frequency.

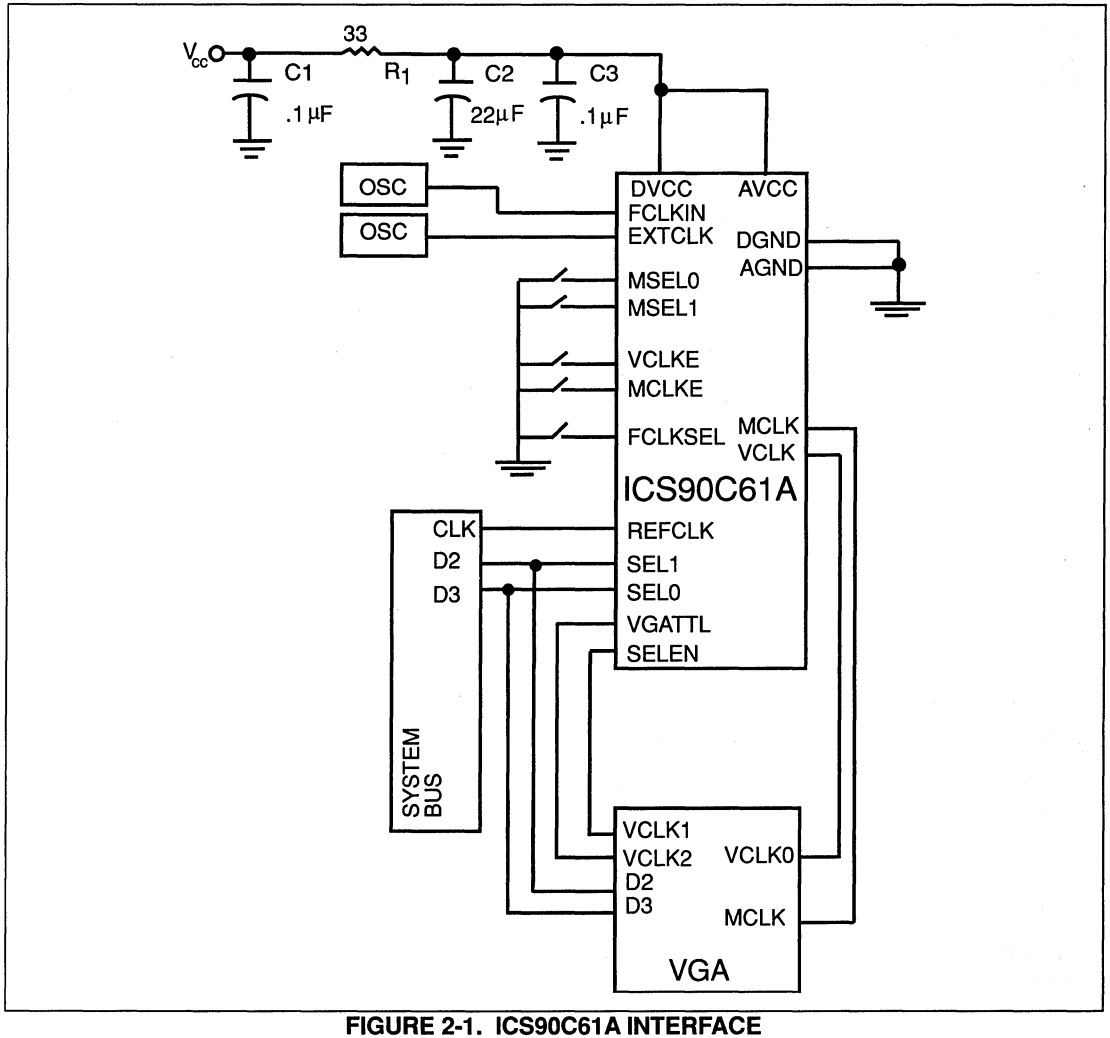


FIGURE 2-1. ICS90C61A INTERFACE

Note:
C_3 should be placed as close as possible to the ICS90C61A AVDD pin

2.1 SYSTEM BUS INPUTS

The system bus inputs are:

- REFCLK
- SEL0
- SEL1

The ICS90C61A uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

2.2 INPUTS FROM VGA CONTROLLER

The VGA controller input the the ICS90C61A is:

- SELEN

The ICS90C61A is programmed to generate different video clock frequencies using the inputs of SEL0, SEL1, VGATTL, and REFCLK. The signals VGATTL and REFCLK may be supplied by the VGA controller as is the case in Western Digital VGA controllers. The inputs SEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital VGA controllers during I/O writes to internal register 3C2h.

Note: Only SEL0 and SEL1 are latched with signal SELEN.

2.3 OUTPUTS TO VGA CONTROLLER

The outputs from the ICS90C61A to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.4 ANALOG FILTERS

The analog filters are integral to the ICS90C61A device. No external components are required. This feature reduces PC board space requiremenrs and component costs. Phase jitter is reduced as externally generated noise cannot easily influence the phase locked loop filter.

2.5 USER DEFINABLE INPUTS

The user definable inputs are:

- EXTCLK
- FCLKIN
- VCLKE, MCLKE
- MSEL0-1
- VGATTL, FCLKSEL

EXTCLK and FCLKSEL are additional inputs that may be internally routed to the VCLK output. The additional inputs are useful for supporting modes that require frequencies not provided by the ICS90C61A.

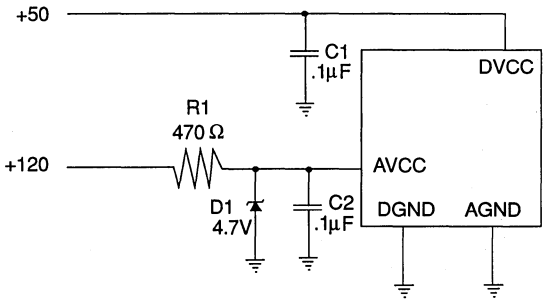
VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

MSEL0-1 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

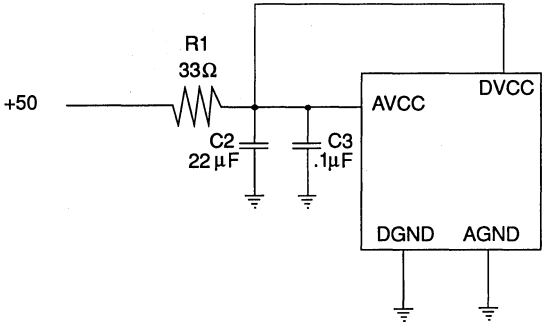
VGATTL and FCLKSEL are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

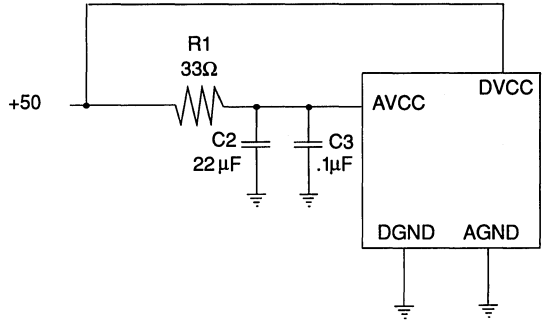
2.6 POWER CONSIDERATIONS

The **ICS90C61A** product requires an AV_{CC} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is not only dependent on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a Zener diode and dropping resistor. A 470 ohm resistor and 4.7 volt Zener diode is the least costly way to accomplish this. A 0.047 to 0.1 microfarad bypass capacitor tied from AV_{CC} to AGND insures good high frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply, however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise generating components. Most systems provide power that is clean enough to allow for jitter free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a 33 ohm resistor and 22 microfarad Tantalum capacitor. Avdd is not particularly sensitive to supply voltage and will work fine at 4.1 volts over the full frequency range of the ICS90C61A, so drop across the decoupling resistor is not a problem. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.





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ICS90C61A-PR2				
FCLKSEL	**VGATTL**	**SEL0**	**SEL1**	**VCLK FREQUENCY (MHz)**
1	0	0	0	REFCLK
1	0	0	1	16.108
1	0	1	0	32.216
1	0	1	1	44.744
1	1	0	0	25.057
1	1	0	1	28.089
1	1	1	0	EXTCLK*
1	1	1	1	36.242
0	X	X	X	FCLKIN*

TABLE 1-1. VCLK SELECTION

* Note:
FCLKIN and EXTCLK may be programmed to output custom frequencies up to 80 MHz in applications which require this capability. Custom frequencies in these addresses require a significant volume commitment and/or one-time mask charge. Contact ICS sales for details.

ICS90C61A-PR2		
MSEL1	**MSEL0**	**MCLK FREQUENCIES (MHz)**
0	0	41.612
0	1	37.585
1	0	36.242
1	1	44.744

TABLE 1-2. MCLK SELECTION

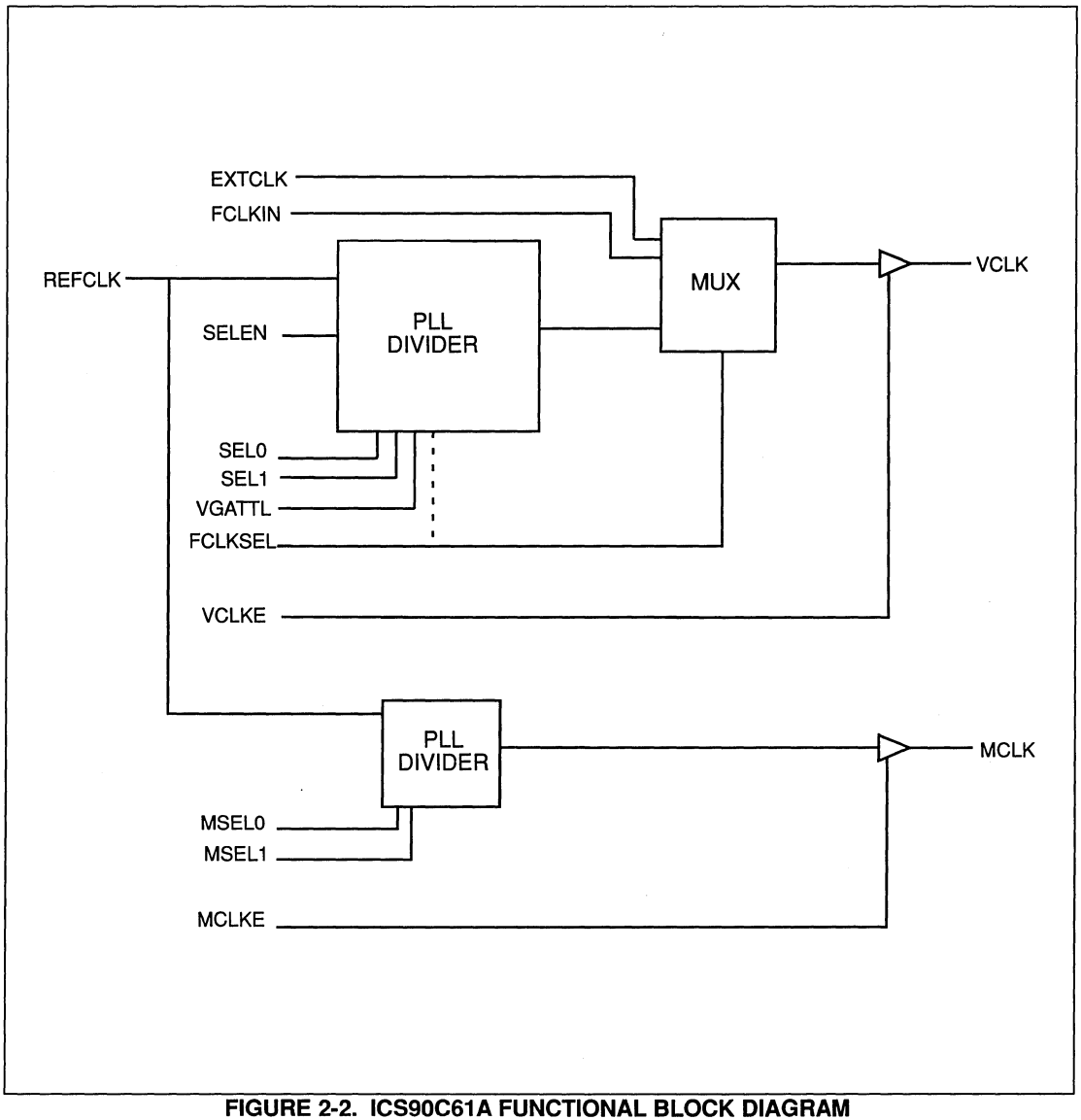

FIGURE 2-2. ICS90C61A FUNCTIONAL BLOCK DIAGRAM

3.0 PIN DESCRIPTIONS

The following table provides the pin definitions for the 20-pin ICS90C61A packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	REFCLK	IN	Reference input clock from system
2	FCLKIN	IN	Feature clock input pin
3	EXTCLK	IN	External clock input for an additional frequency
4	SEL0	IN	Control input for VCLK selection
5	SEL1	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL (0,1) *(Low enable)*
7	VGATTL	IN	Control input for VCLK selection
8	FCLKSEL	IN	Control input for FCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	--	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	--	No Connection
14	MCLKE	IN	Enable input for MCLK output (*high enables output*)
15	AVCC	--	Power supply for analog circuit
16	AGND	--	Ground for analog circuit
17	N.C.	--	No Connection
18	VCLKE	IN	Enable input for VCLK output (*high enables output*)
19	VCLK	OUT	Video Clock Output
20	DVCC	--	Power supply for Digital Circuit

TABLE 3-1. PIN DESCRIPTIONS

Note:
CLKI, EXTCLK, FCLKIN, SEL0, SEL1, VGATTL, FCLKSEL
SELEN, MSEL0, MSEL1, VCLKE, & MCLKE - input pins have internal pullup resistors.

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to VSS	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

4.2 D. C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{CC} = 5V
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V
I_{IH}	Input Leakage Current	---	20	µA	V_{in} = V_{CC}
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	Kohm	V_{CC} = 5V
C_{in}	Input Pin Capacitance	---	8	pF	Fc = 1MHz
C_{out}	Output Pin Capacitance	---	12	pF	Fc = 1MHz

TABLE 4-1. D.C. CHARACTERISTICS

5.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max.
t_f	Fall Time	---	10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS			
t_r	Rise Time	---	3	Phase Jitter 3 ns max.
t_f	Fall Time	---	3	Duty Cycle 40% min. to 60% max.
---	Frequency Error		1.0	%
---	Maximum Frequency		80	MHz
---	Propagation Delay for Pass Through Frequency	---	20	ns
---	Output Enable to tri-state (into and out of) time	---	15	ns

TABLE 5-1. AC TIMING CHARACTERISTICS

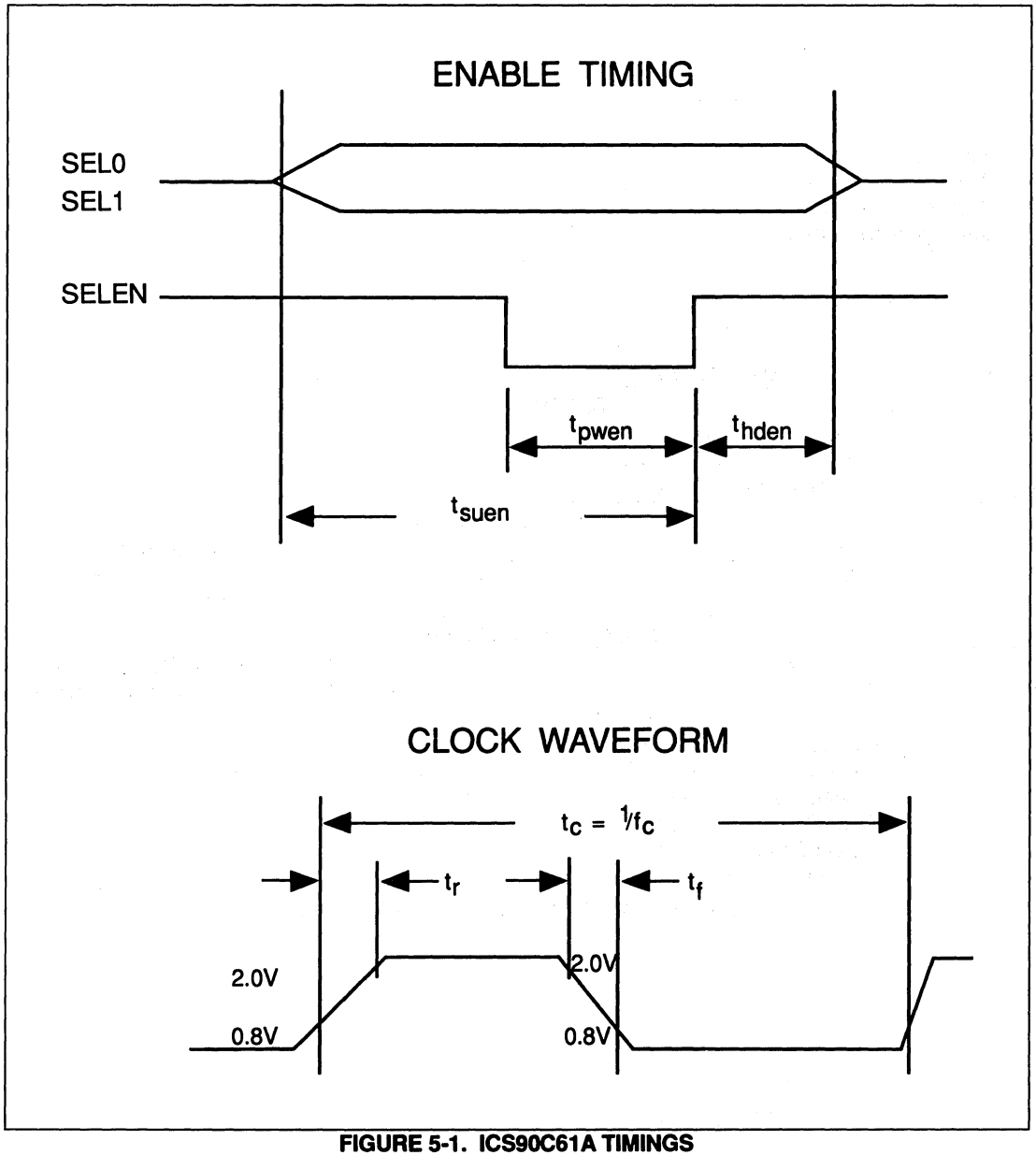

FIGURE 5-1. ICS90C61A TIMINGS

6.0 PACKAGING INFORMATION

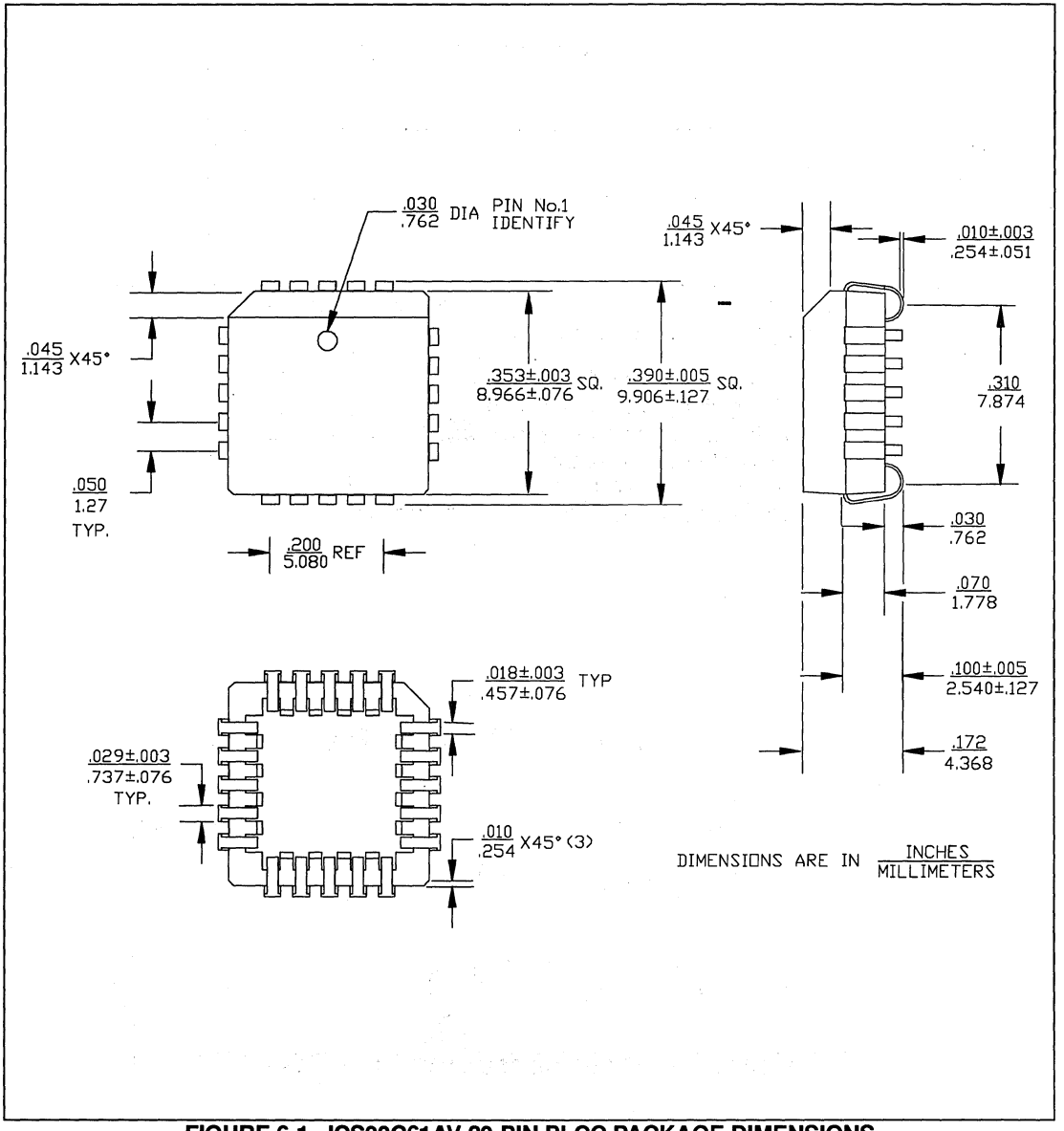

FIGURE 6-1. ICS90C61AV 20-PIN PLCC PACKAGE DIMENSIONS

Contact Integrated Circuit Systems for other package diagrams at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
Valley Forge, PA 19482
Phone: (215) 666-1900
Fax: (215) 666-1099

FIGURE 6-2. OTHER ICS PACKAGE DIMENSIONS

ICS90C63

Dual Video/Memory

Clock Generator

WESTERN DIGITAL

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PREFACE

The Integrated Circuit Systems ICS90C63 dual video/memory clock generator was designed exclusively to work with Western Digital video graphics chips.

Because you get optimum video subsystem performance when you use this video/memory clock generator with Western Digital video graphics chips, we have included the ICS90C63 in our databook.

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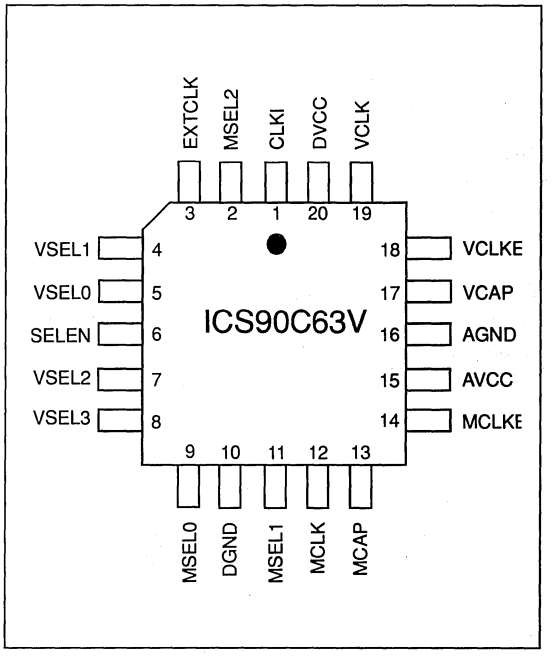

20-PIN PLCC DIAGRAM

1.0 INTRODUCTION

The Integrated Circuit Systems ICS90C63 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 DESCRIPTION

The Integrated Circuit Systems Video Graphics Array Clock Generator (ICS90C63) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

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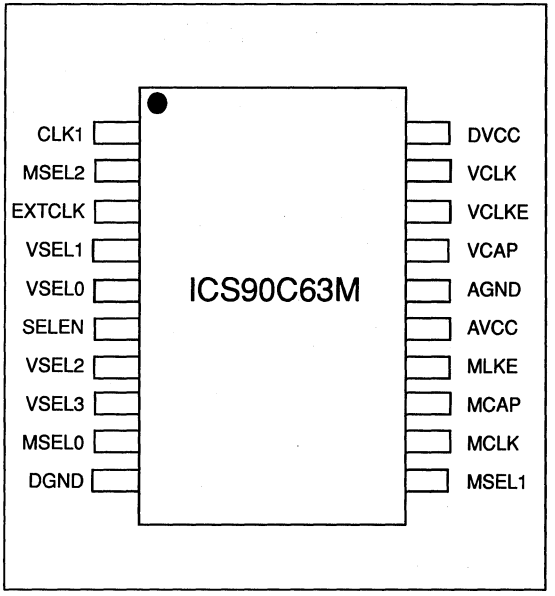
The input and truth table have been designed to allow a direct connection to one of the many Western Digital VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing. External filter components are attached to the MCAP and VCAP pins for the internal phase lock loops.

1.2 FEATURES

- Dual Clock generator for the IBM compatible Western Digital Video Graphics Array (VGA) LSI devices, and 8514/A chip sets.
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency.
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the 15 internally generated clocks and one external clock.
- CMOS technology.



20-PIN S.O.DIAGRAM

- Backward compatibility to the WD90C61 device.
- Available in a 20-pin PLCC, S.O., and DIP packages.

Ordering Information

ICS90C63V (PLCC Package)
ICS90C63M (S.O. Package)
ICS90C63N (DIP Package)

Note: ICS90C63N (DIP) pinout is identical to ICS90C63M (S.O.) pinout.

2.0 ICS90C63 VGA INTERFACE

The ICS90C63 has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock ICS90C63 is connected to a VGA controller. Western Digital VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video frequency.

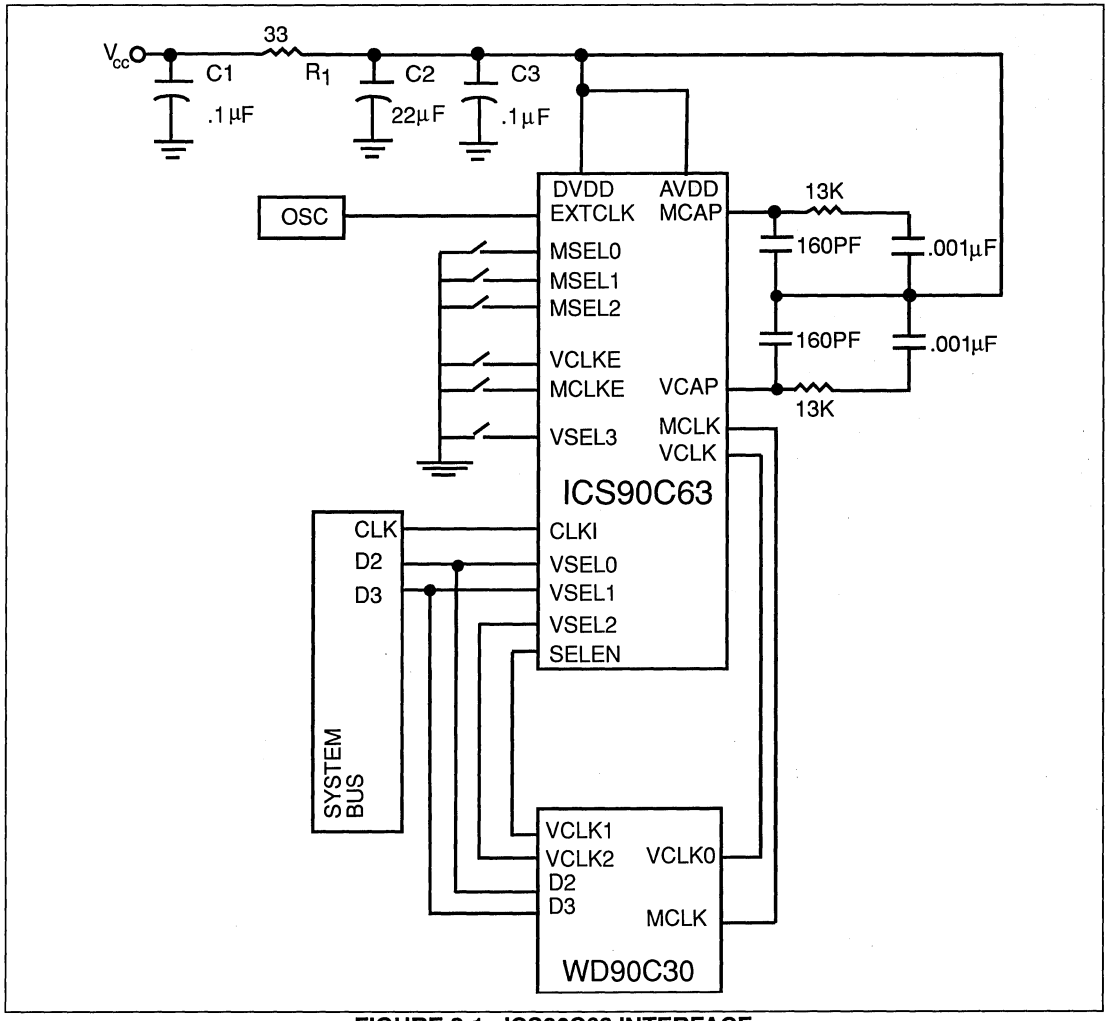


FIGURE 2-1. ICS90C63 INTERFACE

Note:
C_3 should be placed as close as possible to the ICS90C63 AVDD pin

2.1 SYSTEM BUS INPUTS

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The ICS90C63 uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

2.2 INPUTS FROM VGA CONTROLLER

The VGA controller input the the ICS90C63 is:

- SELEN

The ICS90C63 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

2.3 OUTPUTS TO VGA CONTROLLER

The outputs from the ICS90C63 to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.4 ANALOG FILTERS

The analog filters are:

- MCAP
- VCAP

These connections are for the analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. Figure 2-1 shows the filter circuit. The capacitor tolerances are ±20%. The resistor tolerance is ±2%.

2.5 USER DEFINABLE INPUTS

The user definable inputs are:

- EXTCLK
- VCLKE, MCLKE
- MSEL0-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the ICS90C63.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

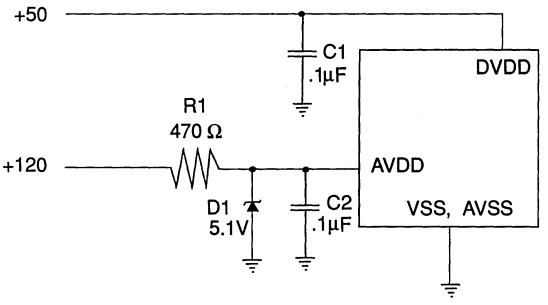
MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

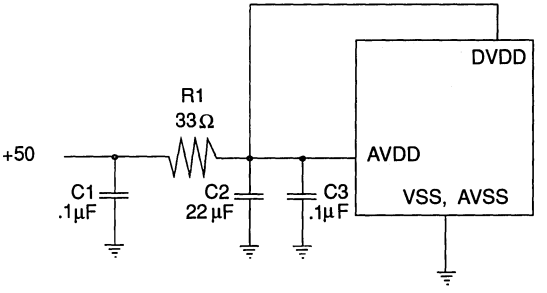
VSEL2 and VSEL3 have internal pullups.

2.6 POWER CONSIDERATIONS

The **ICS90C63** product requires an Avdd supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is not only dependent on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a Zener diode and dropping resistor. A 470 ohm resistor and 5.1 volt Zener diode is the least costly way to accomplish this. A 0.047 to 0.1 microfarad bypass capacitor tied from Avdd to Avss insures good high frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply, however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise generating components. Most systems provide power that is clean enough to allow for jitter free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a 33 ohm resistor and 22 microfarad Tantalum capacitor. Avdd is not particularly sensitive to supply voltage and will work fine at 4.1 volts over the full frequency range of the ICS90C63, so drop across the decoupling resistor is not a problem. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.



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VSEL				
3	2	1	0	VCLK FREQUENCY (MHz)
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	EXTCLK
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.175
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

TABLE 1-1. VCLK SELECTION

MSEL			
2	1	0	MCLK FREQUENCIES (MHz)
0	0	0	33.0
0	0	1	50.0
0	1	0	60.0
0	1	1	30.5
1	0	0	40.0
1	0	1	37.5
1	1	0	36.0
1	1	1	44.9

TABLE 1-2. MCLK SELECTION

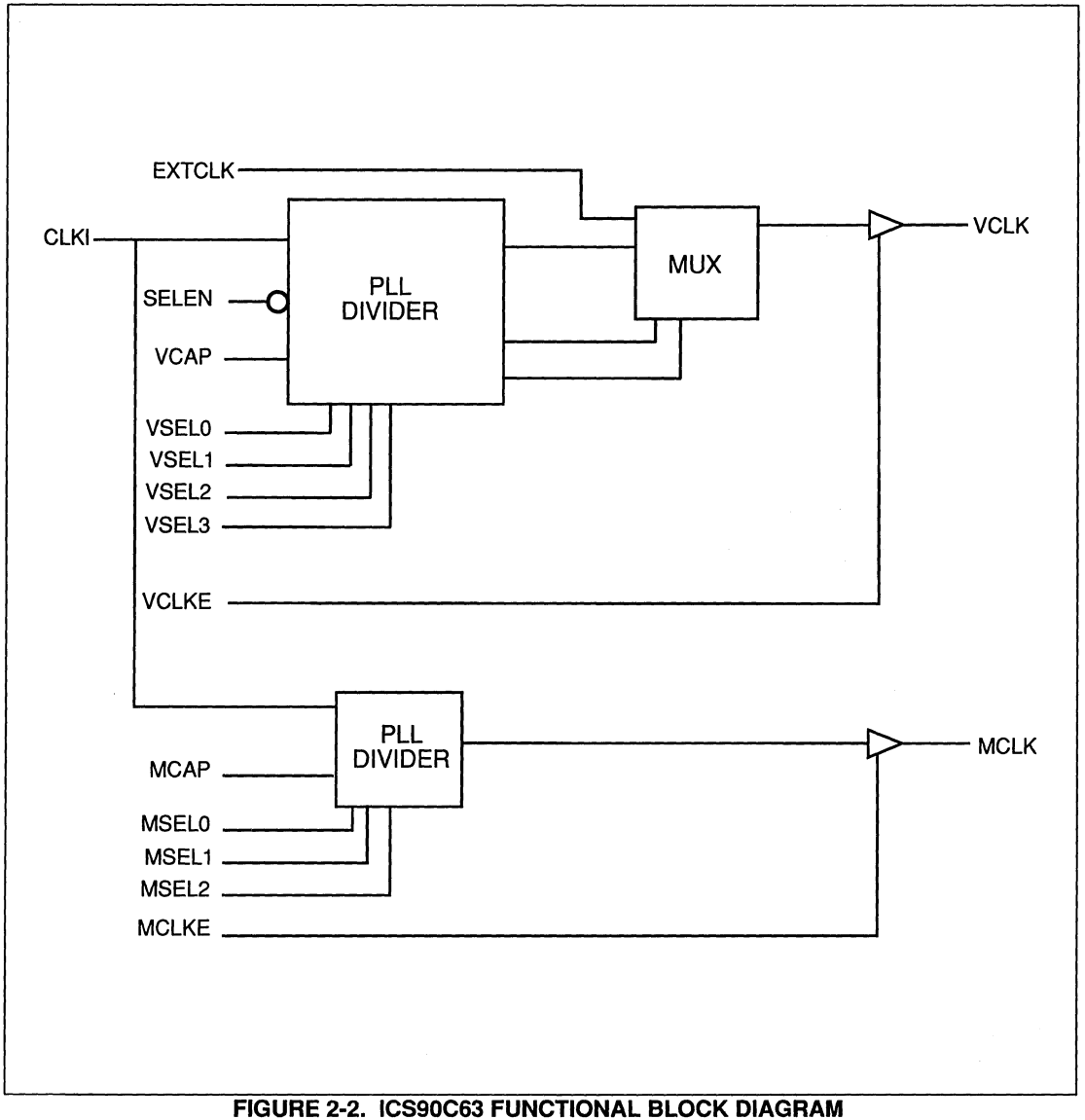

FIGURE 2-2. ICS90C63 FUNCTIONAL BLOCK DIAGRAM

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3.0 PIN DESCRIPTIONS

The following table provides the pin definitions for the 20-pin ICS90C63 package.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL (0,1)(Low enable)
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	--	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	MCAP	IN	External filter connection for MCLK generation
14	MCLKE	IN	Enable input for MCLK output (*high enables output*)
15	AVCC	--	Power supply for analog circuit
16	AGND	--	Ground for analog circuit
17	VCAP	IN	External filter connection for VCLK generation
18	VCLKE	IN	Enable input for VCLK output (*high enables output*)
19	VCLK	OUT	Video Clock Output
20	DVCC	--	Power supply for Digital Circuit

TABLE 3-1. PIN DESCRIPTIONS

Note:
CLKI, EXTCLK, VSEL0, VSEL1, VSEL2, VSEL3
SELEN, MSEL0, MSEL1, MSEL2, VCLKE, & MCLKE - input pins have internal pullup resistors.

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to VSS	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

4.2 D. C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{CC} = 5V
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V
I_{IH}	Input Leakage Current	---	20	µA	V_{in} = V_{CC}
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	Kohm	V_{CC} = 5V
C_{in}	Input Pin Capacitance	---	8	pF	Fc = 1MHz
C_{out}	Output Pin Capacitance	---	12	pF	Fc = 1MHz

TABLE 4-1. D.C. CHARACTERISTICS

5.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. tc = 1/fc
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 μs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max.
t_f	Fall Time	---	10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS			
t_r	Rise Time	---	3	Phase Jitter 3 ns max.
t_f	Fall Time	---	3	Duty Cycle 40% min. to 60% max.
---	Frequency Error		0.5	%
---	Maximum Frequency		80	MHz
---	Propagation Delay for Pass Through Frequency	---	20	ns
---	Output Enable to tri-state (into and out of) time	---	15	ns

TABLE 5-1. AC TIMING CHARACTERISTICS

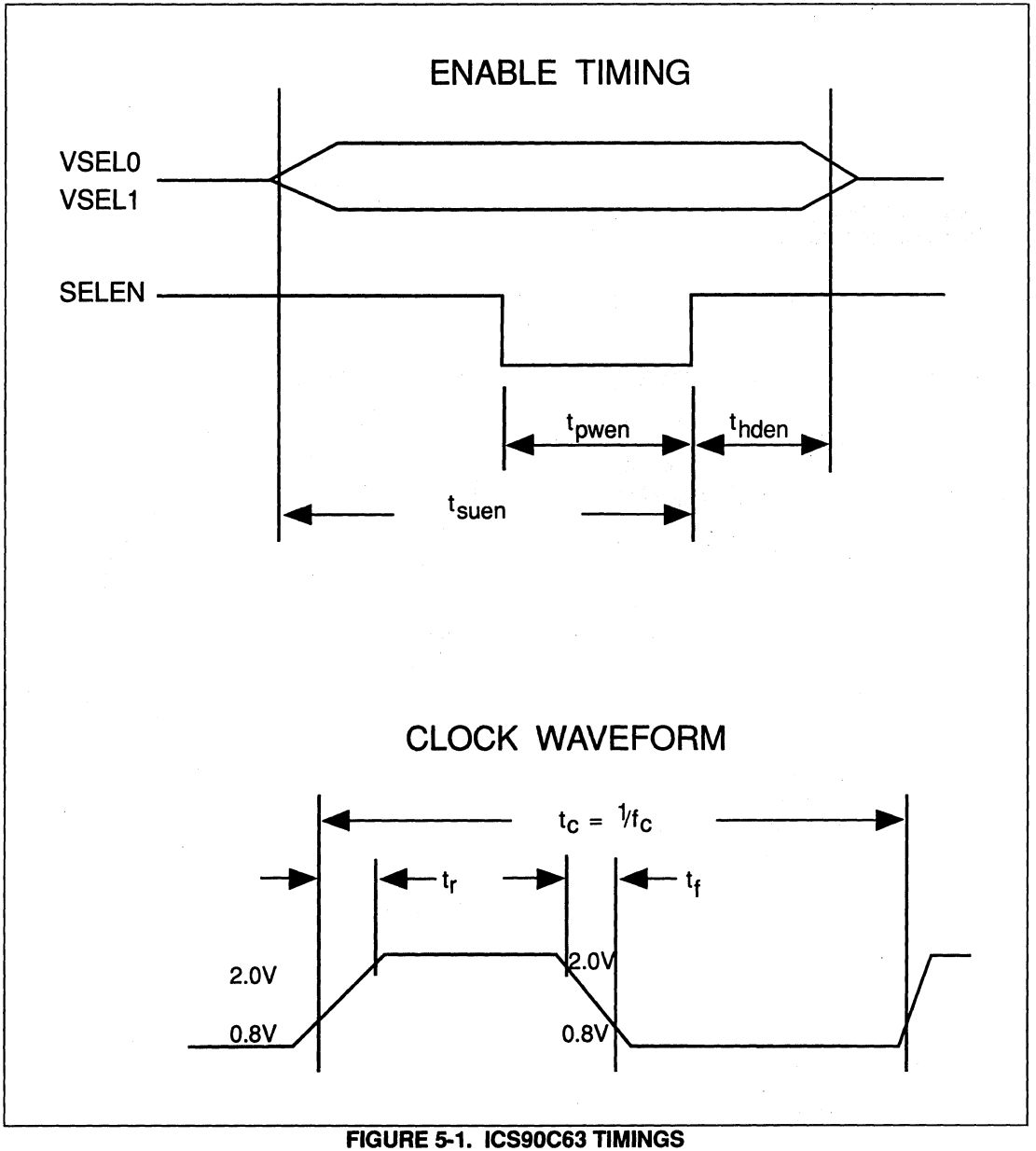

FIGURE 5-1. ICS90C63 TIMINGS

6.0 PACKAGING INFORMATION

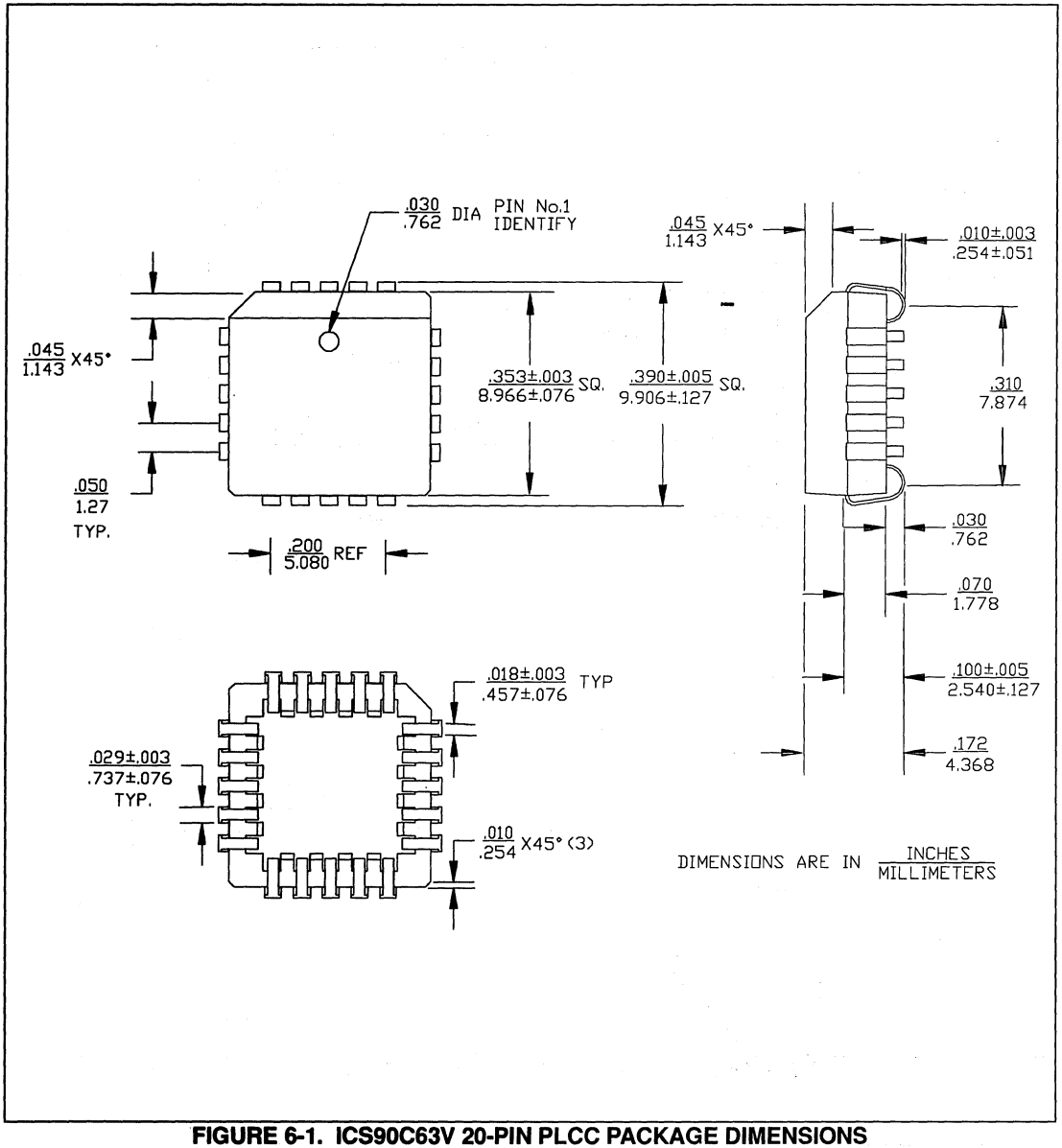

FIGURE 6-1. ICS90C63V 20-PIN PLCC PACKAGE DIMENSIONS

Contact Integrated Circuit Systems for other package diagrams at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
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FIGURE 6-2. OTHER ICS PACKAGE DIMENSIONS

ICS90C64

Dual Video/Memory

Clock Generator

WESTERN DIGITAL

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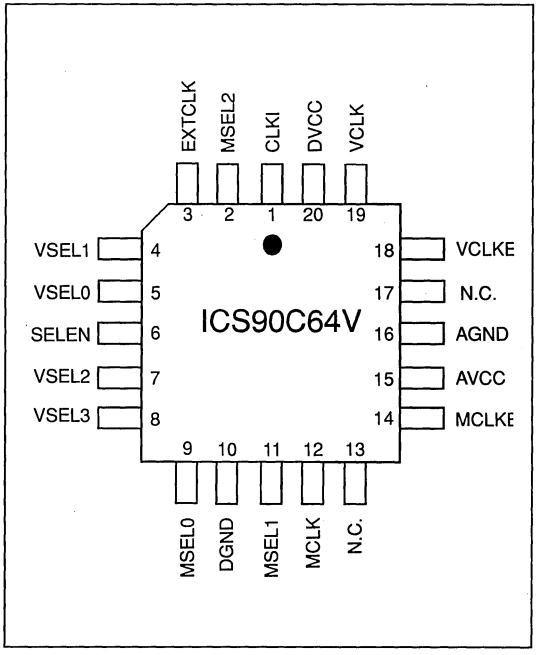


20-PIN PLCC DIAGRAM

1.0 INTRODUCTION

The Integrated Circuit Systems ICS90C64 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 DESCRIPTION

The Integrated Circuit Systems Video Graphics Array Clock Generator (ICS90C64) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

11

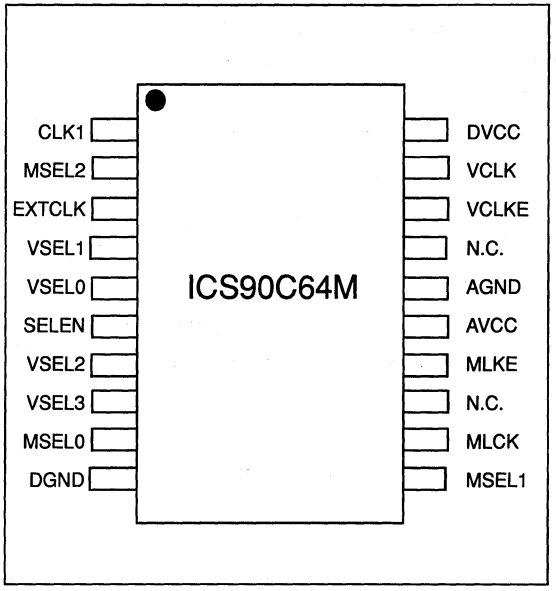
The input and truth table have been designed to allow a direct connection to one of the many Western Digital VGA controllers or 8514/A chip sets.

The MCLK output is one of eight internally generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

1.2 FEATURES

- Dual Clock generator for the IBM compatible Western Digital Video Graphics Array (VGA) LSI devices, and 8514/A chip sets.
- Integral loop filter components. Reduces cost and phase jitter.
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency.
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the 15 internally generated clocks and one external clock.
- CMOS technology.



20-PIN S.O.DIAGRAM

- Backward compatibility to the WD90C63 and WD90C61 device.
- Available in a 20-pin PLCC, S.O., and DIP packages.

Ordering Information

ICS90C64V (PLCC Package)
ICS90C64M (S.O. Package)
ICS90C64N (DIP Package)

Note: ICS90C64N (DIP) pinout is identical to ICS90C64M (S.O.) pinout.

2.0 ICS90C64 VGA INTERFACE

The ICS90C64 has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock ICS90C64 is connected to a VGA controller. Western Digital VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video frequency.

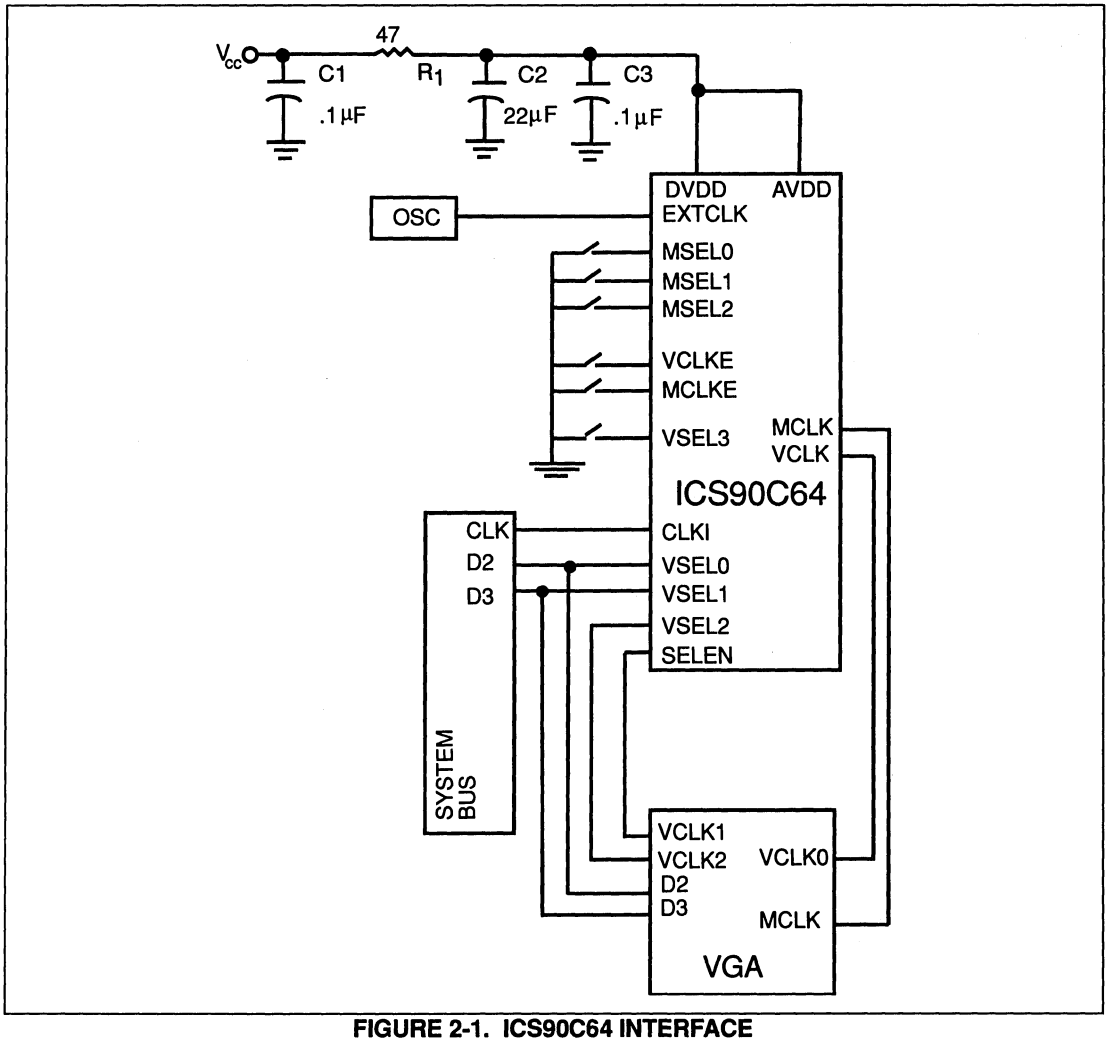


FIGURE 2-1. ICS90C64 INTERFACE

Note:
C_3 should be placed as close as possible to the ICS90C64 AVDD pin

2.1 SYSTEM BUS INPUTS

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The ICS90C64 uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

2.2 INPUTS FROM VGA CONTROLLER

The VGA controller input the the ICS90C64 is:

- SELEN

The ICS90C64 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

2.3 OUTPUTS TO VGA CONTROLLER

The outputs from the ICS90C64 to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.4 ANALOG FILTERS

The analog filters are integral to the ICS90C64 device. No external components are required. This feature reduces PC board space requirements and component costs. Phase jitter is reduced as externally generated noise cannot easily influence the phase locked loop filter.

2.5 USER DEFINABLE INPUTS

The user definable inputs are:

- EXTCLK
- VCLKE, MCLKE
- MSEL0-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the ICS90C64.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tristated.

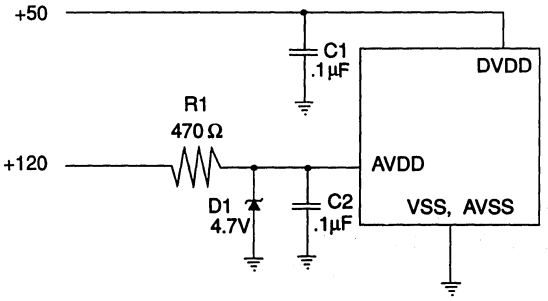
MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

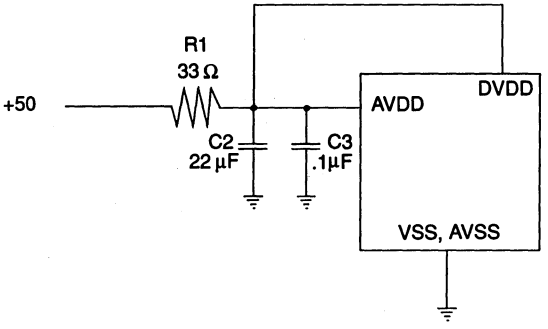
VSEL2 and VSEL3 have internal pullups.

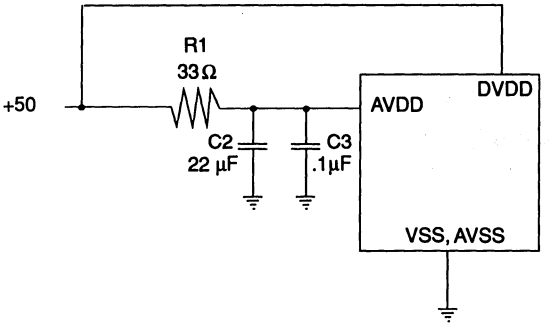
2.6 POWER CONSIDERATIONS

The **ICS90C64** product requires an Avdd supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is not only dependent on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a Zener diode and dropping resistor. A 470 ohm resistor and 5.1 volt Zener diode is the least costly way to accomplish this. A 0.047 to 0.1 microfarad bypass capacitor tied from Avdd to Avss insures good high frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply, however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise generating components. Most systems provide power that is clean enough to allow for jitter free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a 33 ohm resistor and 22 microfarad Tantalum capacitor. Avdd is not particularly sensitive to supply voltage and will work fine at 4.1 volts over the full frequency range of the ICS90C64, so drop across the decoupling resistor is not a problem. Digital inputs that are desired to be held at a static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.





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VSEL				
3	2	1	0	VCLK FREQUENCY (MHz)
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	EXTCLK
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.175
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

TABLE 1-1. VCLK SELECTION

MSEL			
2	1	0	MCLK FREQUENCIES (MHz)
0	0	0	33.0
0	0	1	49.218
0	1	0	60.0
0	1	1	30.5
1	0	0	41.612
1	0	1	37.5
1	1	0	36.0
1	1	1	44.296

TABLE 1-2. MCLK SELECTION

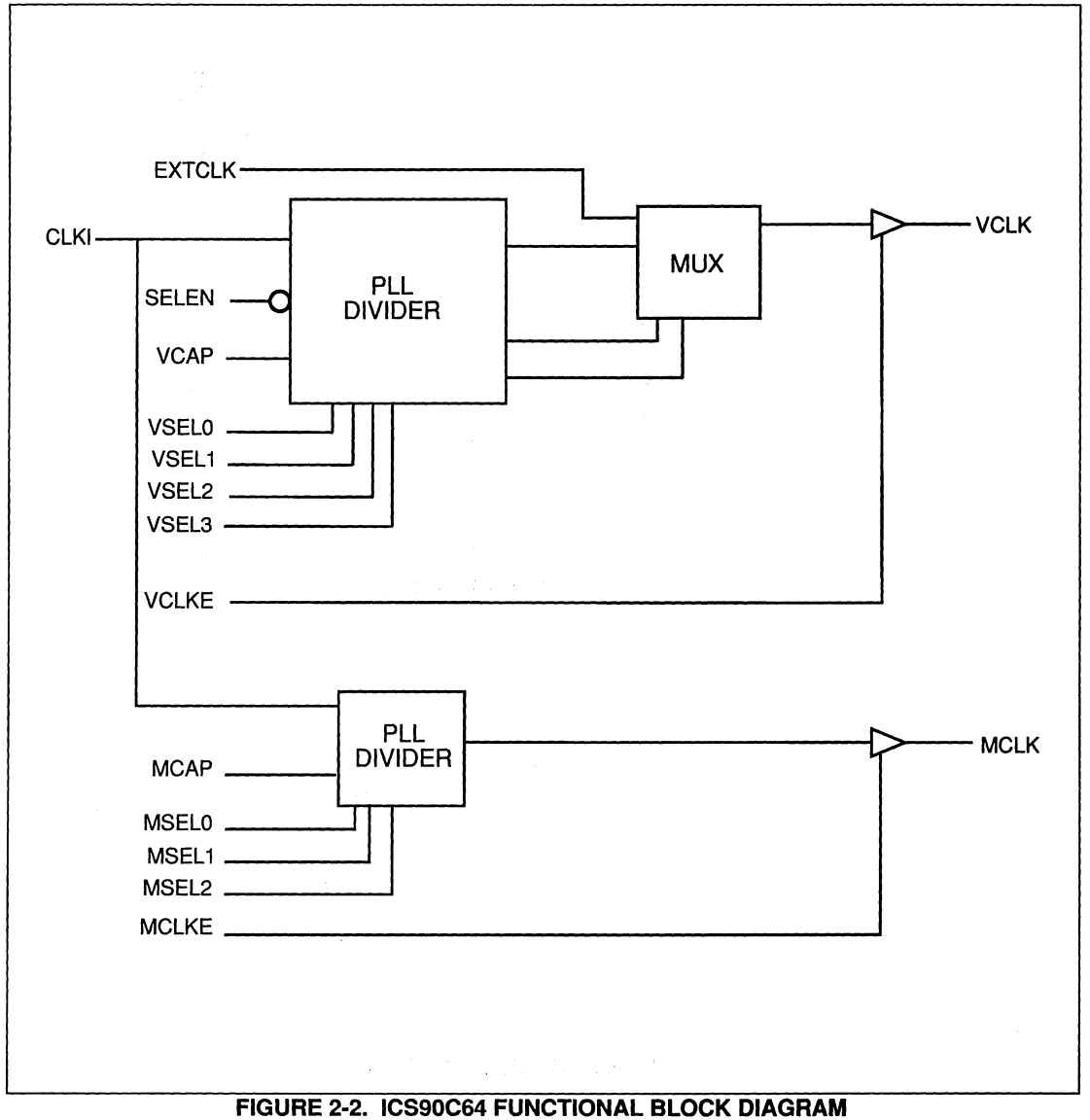

FIGURE 2-2. ICS90C64 FUNCTIONAL BLOCK DIAGRAM

3.0 PIN DESCRIPTIONS

The following table provides the pin definitions for the 20-pin ICS90C64 package.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL (0,1)(*Low enable*)
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	--	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	--	No connection
14	MCLKE	IN	Enable input for MCLK output (*high enables output*)
15	AVCC	--	Power supply for analog circuit
16	AGND	--	Ground for analog circuit
17	N.C.	--	No connection
18	VCLKE	IN	Enable input for VCLK output (*high enables output*)
19	VCLK	OUT	Video Clock Output
20	DVCC	--	Power supply for Digital Circuit

TABLE 3-1. PIN DESCRIPTIONS

Note:
CLKI, EXTCLK, VSEL0, VSEL1, VSEL2, VSEL3
SELEN, MSEL0, MSEL1, MSEL2, VCLKE, & MCLKE - input pins have internal pullup resistors.

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to VSS	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

4.2 D. C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{CC} = 5V
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V
I_{IH}	Input Leakage Current	---	20	µA	V_{in} = V_{CC}
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	Kohm	V_{CC} = 5V
C_{in}	Input Pin Capacitance	---	8	pF	Fc = 1MHz
C_{out}	Output Pin Capacitance	---	12	pF	Fc = 1MHz

TABLE 4-1. D.C. CHARACTERISTICS

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5.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. tc = 1/fc
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max.
t_f	Fall Time	---	10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS			
t_r	Rise Time	---	3	Phase Jitter 3 ns max.
t_f	Fall Time	---	3	Duty Cycle 40% min. to 60% max.
---	Frequency Error		0.5	%
---	Maximum Frequency		80	MHz
---	Propagation Delay for Pass Through Frequency	---	20	ns
---	Output Enable to tristate (into and out of) time	---	15	ns

TABLE 5-1. AC TIMING CHARACTERISTICS

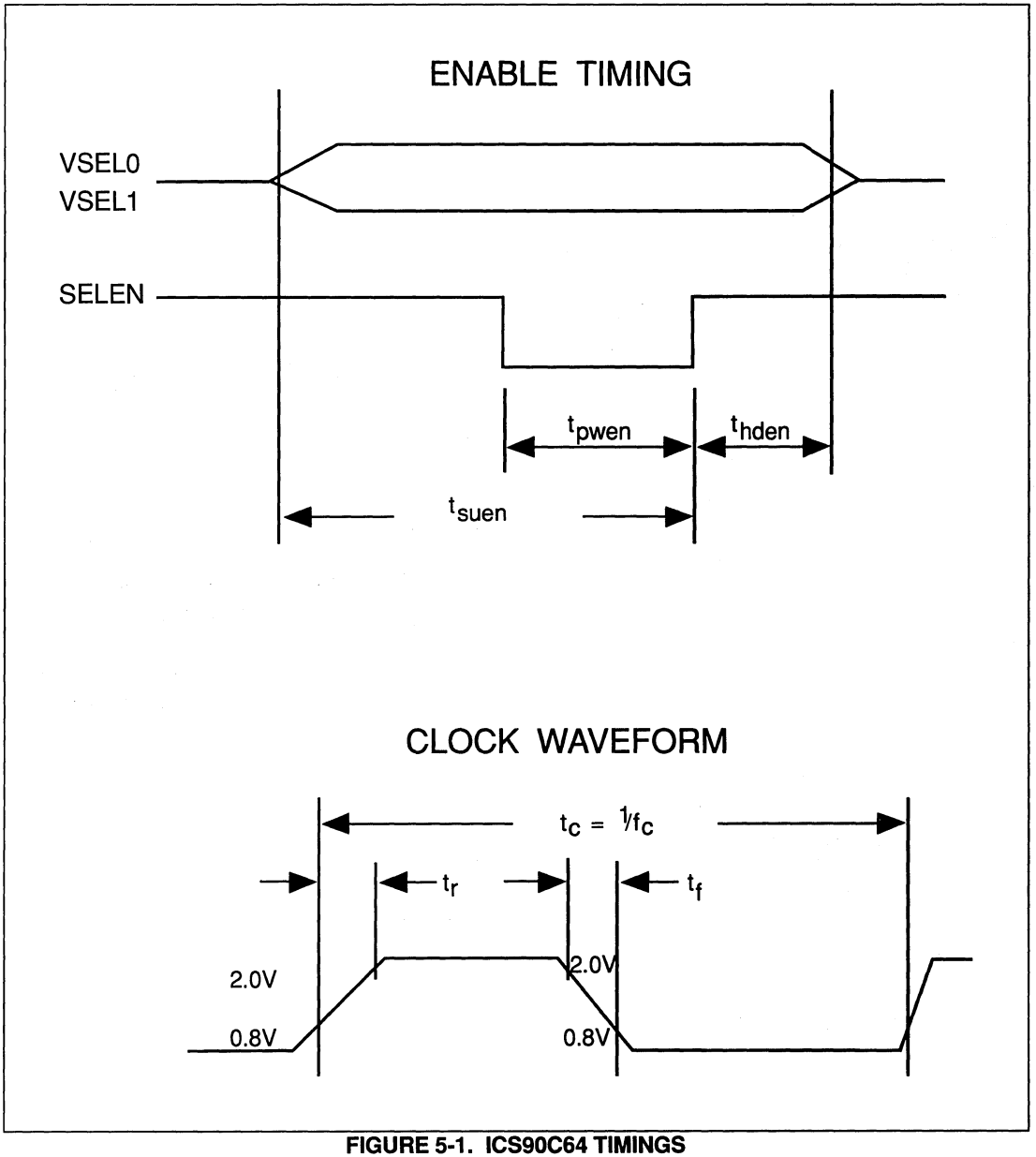

FIGURE 5-1. ICS90C64 TIMINGS

6.0 PACKAGING INFORMATION

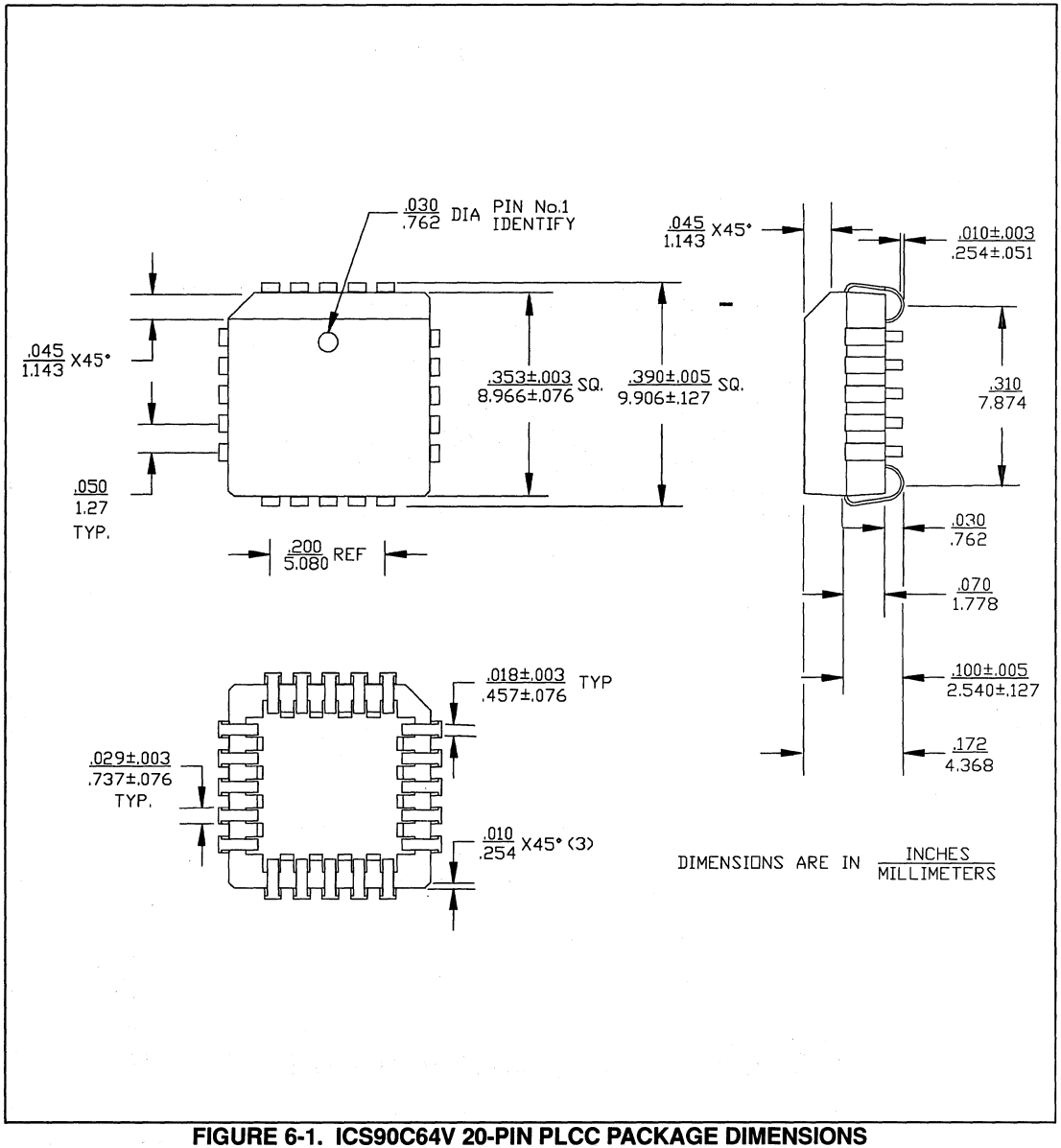

FIGURE 6-1. ICS90C64V 20-PIN PLCC PACKAGE DIMENSIONS

Contact Integrated Circuit Systems for other package diagrams at the following address:

Integrated Circuit Systems, Inc.
Valley Forge Corporate Center
2626 Van Buren Ave., P.O. Box 968
Valley Forge, PA 19482
Phone: (215) 666-1900
Fax: (215) 666-1099

FIGURE 6-2. OTHER ICS PACKAGE DIMENSIONS

WD90C00

VGA

Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multi Color Graphics Array (MCGA), and the Video Graphics Array (VGA). The WDI WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device that fulfills this need and allows for the design of very high performance VGA graphics subsystems that are able to interface with the PC/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards.

A major advantage of using the WD90C00 is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, EGA, Hercules graphics, AT&T (640 by 400 graphics mode), VGA hardware and BIOS level compatibility on analog and TTL monitors. In addition, it includes full support for running extended high resolution 1024 by 768 by 16 colors interlaced graphics mode on 8514 Color Displays. A Noninterlaced 1024 by 768 by 16 colors graphics mode requires external circuitry along with a 56 MHz MCLK and 80 ns DRAMs.

1.1 FEATURES

- Provides single chip Video Graphics Solution for IBM PC/XT/AT and Personal System/2 compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% EGA, CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC/XT/AT, and Micro Channel
- 800 by 600 x 16 colors, 640 by 400 x 256 colors
- 640 by 480 x 256 colors (512 Kbytes DRAM)
- 800 by 600 x 256 colors (512 Kbytes DRAM)
- 1024 by 768 x 16 colors interlaced graphics mode support - 8514 monitor compatible
- 1024 by 768 x 16 colors noninterlaced with external logic
- 132 column text modes, with 25, 43, or 50 rows
- Up to four simultaneous displayable fonts
- Special register locking for flat panel applications
- Lockable palette, RAMDAC, and overscan registers
- Display memory offset registers to control 4 Kbyte windows or 64 Kbyte windows
- Provides adapter video BIOS ROM decoding
- True 7, 8, 9, 10, and 16 pixel wide fonts
- Supports up to 1 Mbyte display memory addressing
- Load up to 16 fonts
- Special underlining in color text mode
- Two additional bits for a total of 18 address bits for cursor location and start address
- Special double scanning
- Special display enable or blanking output signal
- Special border disable
- Page mode addressing for CRTC refresh cycles
- High performance FIFO memory architecture
- Includes 8- or 16-bit wide CPU data bus
- Support for external color lookup table (Palette Chip) with 256K available colors
- Pin for pin compatible with the PVGA1A (AT bus mode)
- Enhanced virtual VGA support
- Up to 45 MHz maximum video clock rate
- Up to 56 MHz maximum memory clock rate
- 1.25 micron CMOS VLSI technology
- 100-pin Plastic Leadless Chip Carrier (PLCC) or Plastic Quad Flat Pack (PQFP) JEDEC package
- Minimizes circuit board space requirements and lowers system cost

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1.2 DESCRIPTION

The Western Digital Imaging (WDI) WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device designed to implement the IBM Personal System/2 Standard video modes along with all of the popular modes used in the IBM PC/AT family. The WD90C00 is designed to offer more improvements for a wider range of applications. These enhancements include additional extended PR registers for EGA register level compatibility for analog and TTL monitors, high resolution interlaced graphics support, improved bus interface design, and an improved memory and video interface for higher performance.

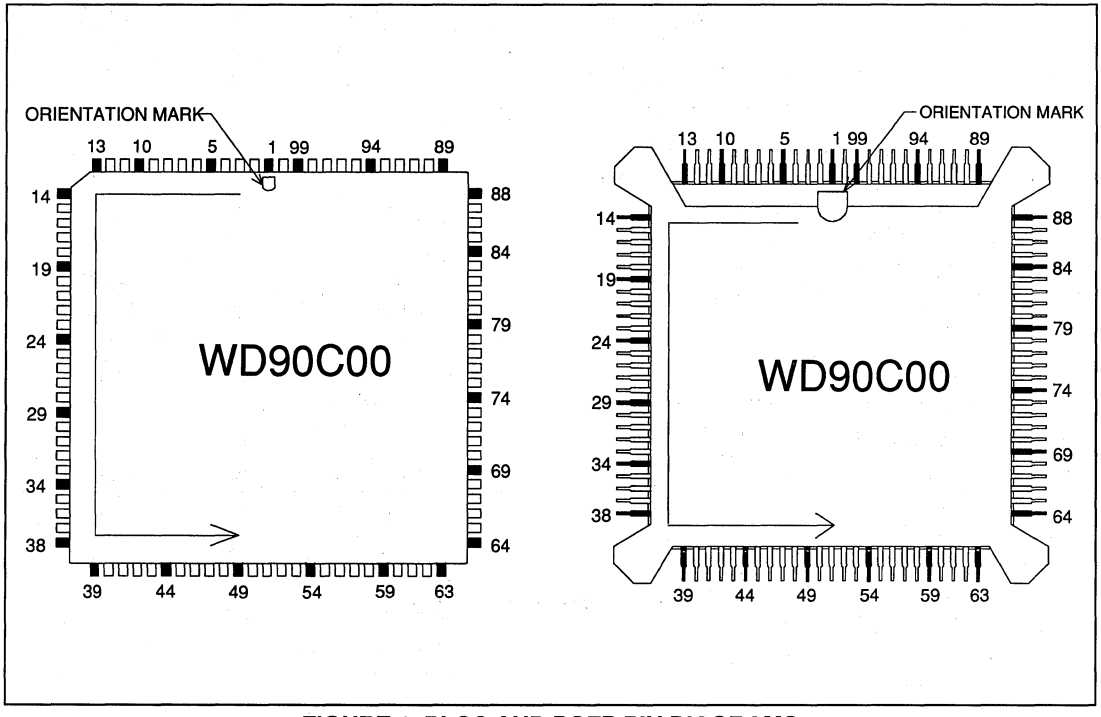

FIGURE 1. PLCC AND PQFP PIN DIAGRAMS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	26	GND	51	GND	76	MCLK
2	MD4	27	A18	52	VCC	77	GND
3	MD3	28	A19	53	VID4	78	VCC
4	MD2	29	$\overline{IOR}$	54	VID3	79	$\overline{RAS10}$
5	MD1	30	$\overline{IOW}$	55	VID2	80	$\overline{CAS10}$
6	MD0	31	$\overline{MRD}$	56	VID1	81	$\overline{OE10}$
7	$\overline{EBROM}$	32	$\overline{MWR}$	57	VID0	82	$\overline{RAS32}$
8	$\overline{DS16}$	33	$\overline{EIO}$	58	$\overline{WPLT}$	83	$\overline{CAS32}$
9	$\overline{BHE}$	34	RDY	59	PCLK	84	$\overline{OE32}$
10	$\overline{SFDBK}$	35	IRQ	60	HSYNC	85	$\overline{WE0}$
11	$\overline{EABUF}$	36	RSET	61	VSYNC	86	$\overline{WE1}$
12	DA8	37	DIR	62	$\overline{BLNK}$	87	$\overline{WE2}$
13	DA9	38	$\overline{EDBUF}$	63	MA8	88	$\overline{WE3}$
14	DA10	39	DA0	64	GND	89	MD15
15	GND	40	DA1	65	MA7	90	MD14
16	DA11	41	DA2	66	MA6	91	MD13
17	DA12	42	DA3	67	MA5	92	MD12
18	DA13	43	DA4	68	MA4	93	MD11
19	DA14	44	DA5	69	MA3	94	MD10
20	DA15	45	DA6	70	MA2	95	MD9
21	EMEM	46	DA7	71	MA1	96	MD8
22	A15	47	$\overline{RPLT}$	72	MA0	97	MD7
23	A16	48	VID7	73	VCLK2	98	MD6
24	A17	49	VID6	74	VCLK1	99	MD5
25	VCC	50	VID5	75	VCLK0	100	VCC

TABLE 1. PIN ASSIGNMENTS

2.0 ARCHITECTURE

The WD90C00 is a highly integrated device that internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics controller and the Attribute Controller.

- **CRT Controller**

The CRT Controller maintains screen refresh functions for the various display modes defined by the programming of its registers either by the BIOS ROM resident firmware or from the application program. These screen refresh functions include display page control, cursor control, sync generation and resolution.

- **Sequencer**

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock and the dot clock for the CRT, Graphics and Attribute controllers.

- **Graphics Controller**

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

- **Attribute Controller**

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, pixel panning, reverse video, overscan color and background or foreground color.

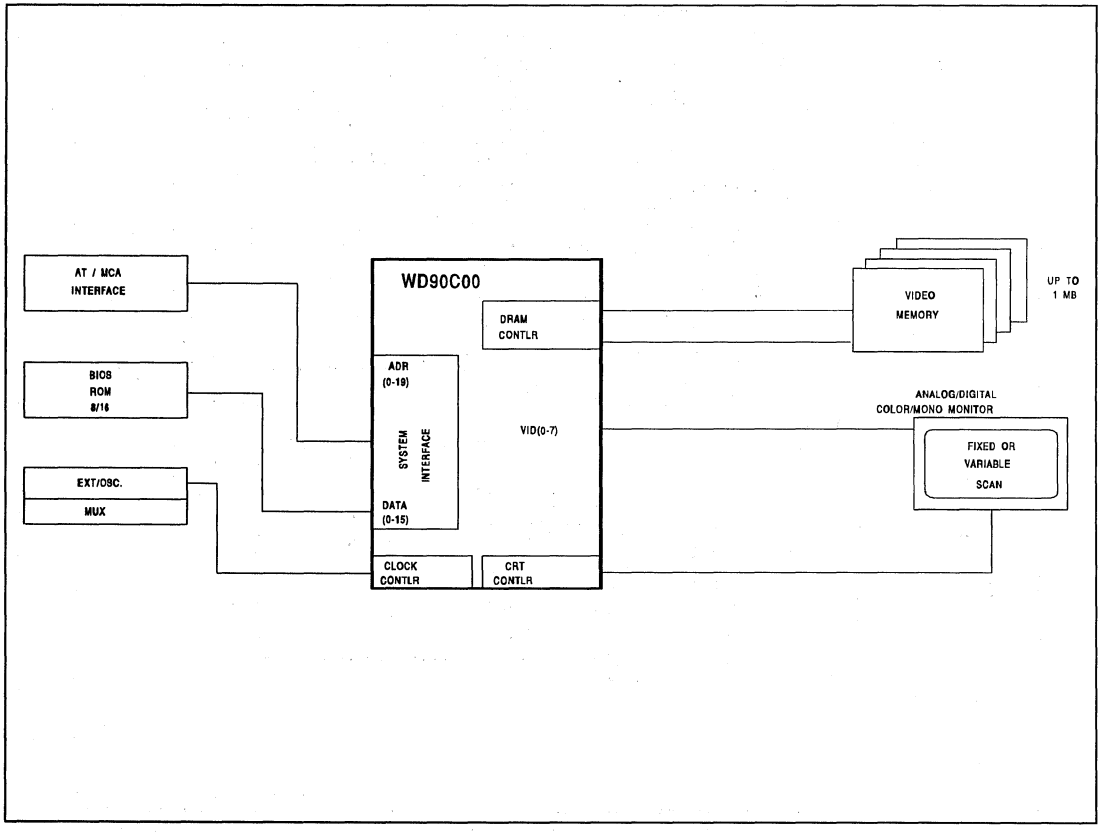

FIGURE 2. SYSTEM BLOCK DIAGRAM

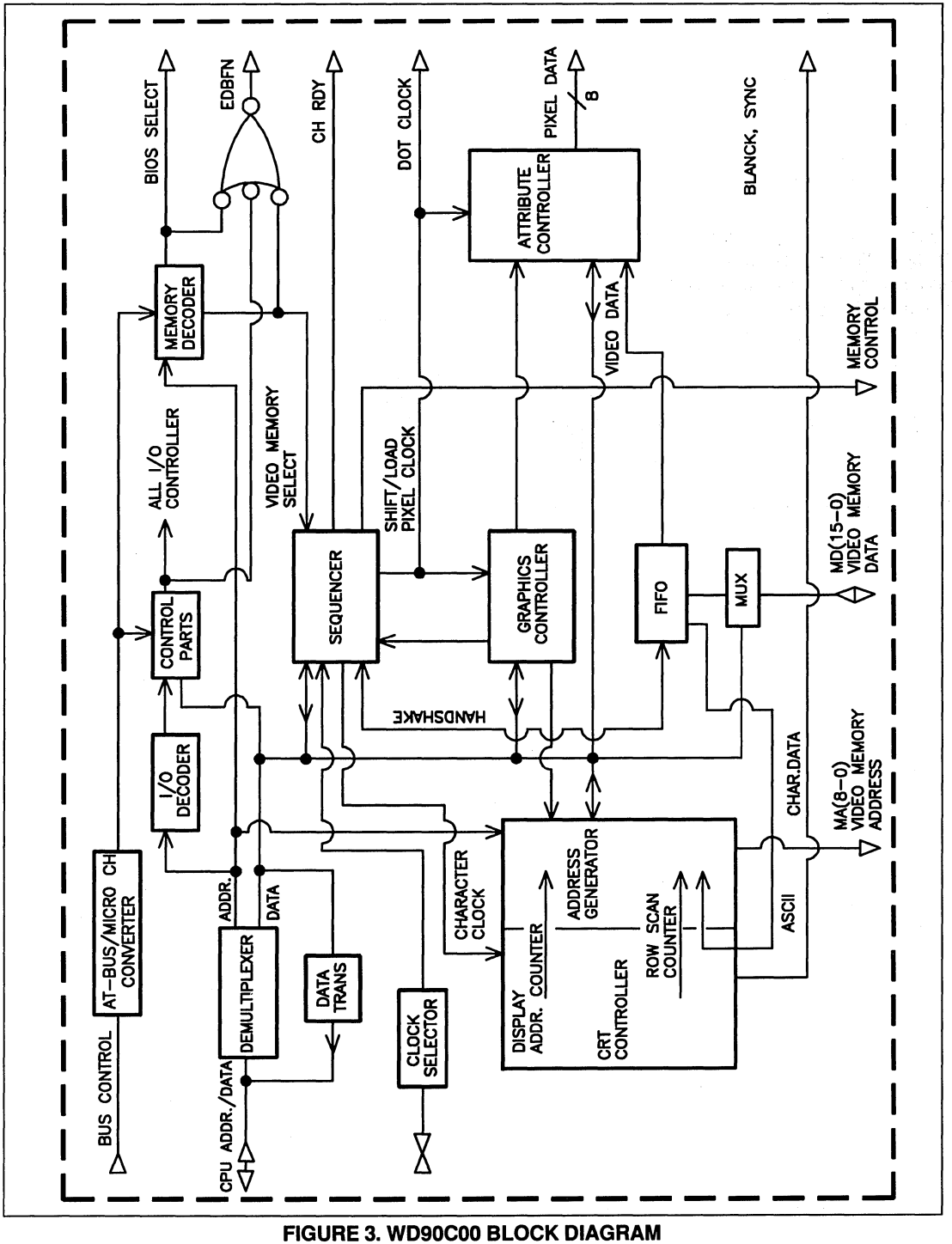

FIGURE 3. WD90C00 BLOCK DIAGRAM

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3.0 WD90C00 INTERFACES

The WD90C00 has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

3.1 CPU AND BIOS ROM INTERFACE

The WD90C00 is designed to operate in two different bus architecture configurations. These are the PC/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the pin strapping upon power up that sets Configuration Register CNF(2).

When configured for AT or Micro Channel operation, the WD90C00 operates functionally in a manner that is conducive to PC/AT or Micro Channel interfacing respectively. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C00 provides all the signals and decodes all the necessary memory and I/O addresses for either an 8 or 16 bit data bus. It also provides the necessary decoding of the Adapter Video BIOS ROM and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 Display adapter. Using the provided signals, the customer can implement designs which multiplex the address/data signals to the WD90C00 in 8 or 16 bit mode, control an 8 or 16 bit BIOS ROM, and generate the desired control and handshake signals such as -MEMCS16.

The I/O data path is eight bit. The memory display buffer data path can be eight or sixteen bits wide. EGA Planar modes have a mandatory eight bit data path with the CPU. Text modes, odd/even, and 256 color modes can support a sixteen bit data path if the video subsystem supports a 16 bit bus implementation. The WD90C00 will provide the necessary wait states for CPU accesses to the video memory. Wait states for I/O accesses and BIOS ROM accesses are not generated. Special I/O ports such as 46E8H (AT mode) and 102H for VGA Enable have been implemented internally in the WD90C00. VGA Subsystem Enable port 3C3h (MCA mode) needs to be implemented externally.

3.2 DRAM DISPLAY BUFFER INTERFACE

The WD90C00 has an optimized interface to the video memory display buffer. The video memory DRAMS can be considered as being organized as four planes. Three configurations of DRAMs exist for the WD90C00 where each plane can be configured as 64 Kbytes (256 Kbytes total), 128 Kbytes (512 Kbytes total), or 256 Kbytes (1 Mbyte total).

The Video memory address range can be up to 1 Mbyte depending on the configuration. Its range is usually from A000:0H to BFFF:FH. External circuitry can be used to map the video memory in different (up to) 1 Mbyte windows.

Eight 64K by 4 page mode DRAM chips are supported for the default IBM memory size. Sixteen 64K by 4 DRAMs and a multiplexer are needed to have a total of 512 KB DRAM. This configuration is needed to support extended video modes such as 640 by 480 x 256 colors and 1024 by 768 x 16 colors. Eight 256 KB by 4 DRAMs are needed to support 1 Mbyte total memory. The WD90C00 provides the support to access all of the available memory. As the WD90C00 has a separate memory clock, 36 MHz to 40 MHz clocks are needed to drive 120 ns DRAMs. With 100 ns DRAMs, up to a 44.9 MHz clock can be used. The WD90C00 can support up to a 56 MHz MCLK which allows it to support much higher extended resolutions such as an 800 by 600 x 256 color mode.

The combination of video clock and memory clock and DRAM speed will determine the video modes available. Usually, a 44.9 MHz MCLK and 44.9 MHz VCLK will support the 1024 by 768 resolution modes. A 42 MHz MCLK will be needed to support the extended 256 color modes but the 44.9 MHz is recommended. A 36 MHz MCLK and VCLK will support the 800 by 600 x 16 color mode.

3.2.1 DRAM Cycle Types

The WD90C00 will do standard RAS/CAS single cycle accesses to the DRAM during CPU writes and reads in graphics modes and alphanumeric modes. For CRTC display refresh cycles, the WD90C00 will do page mode access reads for all cycles in graphics modes. It will also do page mode reads to the DRAM when selected to do so to increase performance in alphanumeric modes. The default mode of DRAM access in alphanumeric mode is the standard single RAS/CAS cycle. The WD90C00 provides the necessary control signals and address/data lines to access the video memory as two 16 bit data interleaved banks. The WD90C00 will also refresh the DRAMs with 3 or 5 refresh cycles after every horizontal scan line.

3.3 VIDEO AND RAMDAC INTERFACE

3.3.1 RAMDAC

The WD90C00 is designed to connect to an analog CRT monitor through an external RAMDAC, but it may also be used to drive other types of displays such as TTL monitors along with the correct register programming and clocks. All the necessary signals to interface to the video RAMDAC are provided.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C00 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color). In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel such as a 1024 by 768 noninterlaced mode.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to the WD90C00. The WD90C00 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C00 has four clock input signal pins. These are: separate memory clock, MCLK, which drives the DRAM timing in graphics and alpha modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. WD90C00 also provides the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as the video dot clock.

3.5 WD90C00 POWER-UP CONFIGURATION

The WD90C00 uses the memory data pins that are "strapped" to ground or Vcc through resistors to configure an internal configuration register upon powerup/reset. CNF(2) will determine whether the WD90C00 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by WD90C00 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C00 power-up configuration, refer to the PR Register section of this data sheet.

4.0 PIN DESCRIPTION

The following tables provide WD90C00 pin definitions for the 100-Pin Plastic Leadless Chip Carrier (PLCC) and Plastic Flat Pack (PQFP) package.

The WD90C00 mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO	PIN SYMBOL	TYPE	DESCRIPTION
		POWER ON	
36	RSET	I	RESET: This signal input will reset the WD90C00 in order for the WD90C00 to initialize during Reset. PR registers PR1, PR11, and CNF are initialized at power-up reset based on the logic level on the MD(7:0), MD(15:11) bus as determined by pull-up/pull-down resistors. Outputs $\overline{\text{EABUF}}$ and $\overline{\text{EDBUF}}$ are tri-stated during reset. The active high reset pulse width should be at least ten MCLK clock periods.
		CLOCK SELECTION	
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics and alpha mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be equal to or greater than VCLK. It is 36 to 40 MHz for 120 ns DRAMs, and recommended to be 44.9 MHz for 100 ns DRAMs.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be either the second video display clock input or an output selection signal to the external clock selection module. Pin direction is determined on Reset by a pull-up/down register on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 can be an active low pulse during I/0 writes to port 3C2H or the state of 3C2H bit 2 as per PR15(5). Refer to the Configuration Register description.
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user defined external clock input, or as an output reflecting the content of bit PR2(1) or the state of 3C2H bit 3 as per PR15(5) if CNF(3) is set to 1 . Refer to the Configuration Register description.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			CLOCK SELECTION (CONT)
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register (3C2H) bits 3 and 2 when both are set to 0 will select this clock.
			CPU ADDRESS BUS
28	A19	I	ADDRESS ONLY BUS A(19:15): These active high inputs form the high-order five bits of video memory address. These addresses (19:16) are not decoded during I/O accesses in AT or MCA implementation. These inputs are directly connected to the system bus.
27	A18	I	
24	A17	I	
23	A16	I	
22	A15	I	
			CPU DATA BUS
20	DAI5(*)	I/O	DATA/ADDRESS BUS DA(15:0): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information. NOTE: "*" DA15 signal is multiplexed with data bit 15 and CRT monitor sense input for auto monitor detection.
19	DA14	I/O	
18	DA13	I/O	
17	DA12	I/O	
16	DA11	I/O	
14	DA10	I/O	
13	DA9	I/O	
12	DA8	I/O	
46	DA7	I/O	
45	DA6	I/O	
44	DA5	I/O	
43	DA4	I/O	
42	DA3	I/O	
41	DA2	I/O	
40	DA1	I/O	
39	DA0	I/O	
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the WD90C00 video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the WD90C00. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

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PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
10	$\overline{\text{ROM16}}$ $\overline{\text{SFDBK}}$	O	16 BIT WIDE BIOS ROM: In AT mode this active low status signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the signal -MEMCS16 in AT mode. In Micro Channel mode, $\overline{\text{SFDBK}}$ is the unlatched address decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the CPU bus cycles during video memory accesses. It is pulled inactive by WD90C00 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. This is a tri-state signal.
35	IRQ	O	INTERRUPT REQUEST: It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of a Vertical Display occurs, this signal will transition active at the start of vertical retrace, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In a AT mode, IRQ is tri-state upon power up reset and may be enabled by PR14(7). In Micro Channel mode, PR14(7) will power up IRQ enabled. This is a tri-state signal.
8	$\overline{\text{DS16}}$	O	DATA SIZE 16: Active low enable for 16 bit video memory word transfers. It is a mode dependent signal. In AT mode, $\overline{\text{DS16}}$ is a status signal as programmed in bit PR1(2) (and other registers) and is used to control the high and low byte 16 bit external data buffers. See the PR Register (PR1) description for further details. This status signal is also used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR(1) and/or during memory 16 bit data path access (if enabled by PR1(2)).

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
33	$\overline{EIO}$ VGASETUP	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the WD90C00. In Micro Channel mode, this signal is the VGASETUP input pin and is connected to the latched card setup or the VGA setup. The externally designed system I/O port signals (96H for Adapter card or 94H bit 5 for system board design) is connected to the $\overline{EIO}$ pin. When this signal is high, the WD90C00 is enabled or in the operating state. An active low signal on this pin puts the WD90C00 into set up mode. During the set up mode, write logic 1H to WD90C00 internal port 102H to awaken the WD90C00 after power on.
9	$\overline{BHE}$	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates a 16 bit transfer of data
31	$\overline{MRD}$ M/-I/O	I	MEMORY READ: In AT mode, this is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-I/O) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process.
32	$\overline{MWR}$ -S0	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands.
29	$\overline{IOR}$ -S1	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle.
30	$\overline{IOW}$ -CMD	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write cycle. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle.

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PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY DATA
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA MD(15:0): These lines are the data bus to the video display DRAMS. Data lines MD(7:0) are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD — Power-Up Function — Register (Bit) 15 EGA SW4 PR11(7)+ 14 EGA SW3 PR11(6)+ 13 EGA SW2 PR11(5)+ 12 EGA SW1 PR11(4)+ 11 ANALOG/TTL Display CNF(8) * 7 General Purpose CNF(7) * 6 General Purpose CNF(6) * 5 General Purpose CNF(5) * 4 General Purpose CNF(4) * 3 VCLK1,2 Input/Output CNF(3) + 2 AT/MicroChannel Mode CNF(2) + 1 BIOS ROM Data Path PR1(1) * 0 BIOS ROM Mapout PR1(0) * NOTE: "*" Pulldown resistor sets these bits to logic 1. "+" Pullup resistor sets these bits to logic 1. For more details refer to PR Registers.
			VIDEO MEMORY ADDRESS
63 65 66 67 68 69 70 71 72	MA8+ MA7+ MA6+ MA5+ MA4+ MA3+ MA2+ MA1+ MA0+	O	MEMORY ADDRESS MA(8:0): Display memory DRAM address. NOTE: "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
			VIDEO MEMORY CONTROL SIGNALS
80	$\overline{\text{CAS10}}$+	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	$\overline{\text{CAS32}}$+	O	COLUMN ADDRESS STROBE: Active low memory maps 3 & 2 CAS output signal.
79	$\overline{\text{RAS10}}$+	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
82	$\overline{RAS32}$+	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	$\overline{OE10}$+	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	$\overline{OE32}$+	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	$\overline{WE0}$+	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, upper byte (Memory map 0).
86	$\overline{WE1}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1)
87	$\overline{WE2}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	$\overline{WE3}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3). NOTE: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7* VID6* VID5* VID4* VID3* VID2* VID1* VID0*	O	VIDEO VID(7:0): Pixel video data output to DAC. NOTE: "*" For testing purposes, these pins can be tri-stated by setting PR Register PR4 (5) = 1.
47	$\overline{RPLT}$	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses at 3C6H, 3C8H, and 3C9H.
58	$\overline{WPLT}$	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses at 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the RAMDAC to latch video signals VID(7:0). Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1, or 2 is divided by two in 320/360 pixel display mode to derive PCLK. MCLK can be the source of this clock.
62	$\overline{BLNK}$ *	O	BLANK: Active low RAMDAC blank pulse. NOTE: "*" For testing purposes, this pin can be tri-stated by setting PR Register PR4 (5) = 1.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		CRT CONTROL	
60	HSYNC+	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming. SEE NOTE BELOW.
61	VSYNC+	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register. NOTES: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(5)=1.
		BIOS ROM CONTROL	
7	$\overline{\text{EBROM}}$	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C000:0H-C7FF:FH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C600:0H-C67F:FH. However, the C600:0H-C67F:FH address range can be mapped in to increase BIOS space by setting PR17(0) = 0. In AT mode only, a write to the WD90C00 internal I/0 port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
		BUFFER CONTROL	
11	$\overline{\text{EDBUFH}}$	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing aqyddress and data to WD90C00. It is tri-stated while Reset is active. When in MCA implementation, this output becomes the high byte data bus enable signal during the 16 bit data transfers and is referred as $\overline{\text{EDBUFH}}$.
38	$\overline{\text{EDBUF}}$	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to WD90C00. It is tri-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the DA(15:0) data bus in AT and MCA implementation. The default state is low until a read cycle occurs, and the WD90C00 will drive DIR high to change the direction of the data buffers.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
POWER AND GROUND			
25	VCC	—	+5VDC
52	VCC	—	+5VDC
78	VCC	—	+5VDC
100	VCC	—	+5VDC
1	GND	—	Ground
15	GND	—	Ground
26	GND	—	Ground
51	GND	—	Ground
64	GND	—	Ground
77	GND	—	Ground

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0 °C to 70 °C
Storage temperature	- 40 °C to 125 °C
Voltage on all inputs and outputs to Vss	- 0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

6.0 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the reference pin.

Operating temperature range	0° C to 7 °C
Power supply voltage	4.75 to 5.25 Volts

7.0 D.C CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	--	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	--	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +4.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=4.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	0V
I(CC)	Stand By Current (All Inputs at TTL Levels)	--	22	mA	VCC=5.25 VDC TA=0 °C, Static
I(DD)	Operating current	--	130	mA	VCC=5.25V, MCLK=VCLK=45 MHz
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 2. DC CHARACTERISTICS

NOTES

1. WD90C00 outputs have 4.0 mA maximum source and sink capability except for pin RDY = 24.0 mA sink and 4.0 mA source and pin IRQ = 24.0 mA sink and 4.0 mA source.

2. Pullups on MD(0:15), DA(0:15), $\overline{\text{EDBUF}}$, $\overline{\text{EABUF}}$ = 100 K ohms. Pullup on $\overline{\text{BHE}}$ = 50 K ohms.

8.0 AC TIMING CHARACTERISTICS

C_L = load capacitance = 70 pf unless specified otherwise.

t=1/MCLK in all modes
Units are in nanoseconds (ns).

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		1
2	MD Setup to RSET low	2t		
3	MD Hold from RSET low	2t		
4	Vcc high to RSET high setup	100		
5	RSET low to first $\overline{MRD}$/ $\overline{IOW}$	10t		
	CLOCK TIMING			
1	Input Clock (MCLK or VCLK) Period	t	t	
2	Clock low	40%t		2
3	Clock high		60%t	2
4	Clock Rise Time		3	3
5	Clock Fall Time		3	3
6	Input VCLK to PCLK Delay		13	
9a	PCLK to Hsync and Vsync Delay		6.5	
9b	PCLK to $\overline{BLNK}$ Delay		6.5	
9c	PCLK to VID(7:0) Delay		3	
	AT MODE I/O & MEMORY READ/WRITE TIMING			
1	$\overline{EIO}$ setup to $\overline{IOR}$ and $\overline{IOW}$ active	8		
2	$\overline{EIO}$ hold from $\overline{IOR}$ and $\overline{IOW}$ inactive	5		
3	EMEM setup to $\overline{MR}$ and $\overline{MW}$ active	4		
4	EMEM hold from $\overline{MR}$ and $\overline{MW}$ inactive	4		
5	$\overline{EABUF}$ inactive from $\overline{IOR}$/ $\overline{W}$, $\overline{MR}$/ $\overline{W}$ active		30	
6a	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (I/O R&W)		21	
6b	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (M R&W)		15	
7a	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (I/O R&W)		13	
7b	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (M R&W)		35	

TABLE 3. AC TIMING CHARACTERISTICS

1. The MCLK should be running with the reset applied.
2. Measured at 1.4V.
3. Measured between 0.8V and 2.0V.

NUMBER	PARAMETER	MIN	MAX	NOTES
AT MODE I/O & MEMORY READ/WRITE TIMING (CONTINUED)				
8	EDBUF inactive from IOR/ W, MR/ W inactive		21	
9	DIR active from IOR and MR active		24	
10	DIR inactive from IOR and MR inactive		21	
11a	BHE setup to MR and MW active	4		
11b	Address setup to IOR and IOW active	8		
11c	Address setup to MR and MW active	4		
12a	BHE hold to MR and MW active	6		
12b	Address hold to IOR and IOW active	4		
12c	Address hold to MR and MW active	6		
13	DA(15:0) valid address setup to IOR/ W, MR/ W	13		
14	DA(15:0) valid address hold from IOR/ W, MR/ W	4		
15	Data setup to IOW inactive	10		
16	Data hold from IOR/ W, MR/ W inactive	8		
17a	Data valid from IOR active		2t + 42	
17b	Data valid (CAS32 inactive) from MR active	11.5t		
17c	Write data valid from MW active	4.5t-50		4
18	Read data setup to RDY high	3.5t-40		5
19	RDY inactive from MR and MW active		13	
20	RDY active from MW, MR active	15t		
21	RDY tri-state from MW, MR inactive		10	
22	WPLT active from IOW active		2t+35	
23	WPLT inactive from IOW inactive		22	
24	RPLT active from IOR active		31	
25	RPLT inactive from IOR inactive		21	
26	EBROM active from IOW active (46E8)		2t+29	
27	EBROM inactive from IOW inactive		20	
28	EBROM active from valid address		20	
29	EBROM inactive from MRD inactive		23	
30	VCLK1 (as output) delay from IOW		2t+33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

4. This spec includes 50 ns worst case delay from DA to MD bus.
5. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	MICRO CHANNEL I/O & MEMORY READ AND WRITE TIMING			
1	$\overline{\text{CDSETUP}}$ setup to $\overline{\text{CMD}}$ active	0		
2	$\overline{\text{CDSETUP}}$ hold from $\overline{\text{CMD}}$ inative	4		
3	EMEM, $\overline{\text{BHE}}$, Address setup to $\overline{\text{CMD}}$	10		
4	EMEM, $\overline{\text{BHE}}$, Address hold from $\overline{\text{CMD}}$	6		
5	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ setup to $\overline{\text{CMD}}$	10		
6	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ hold from $\overline{\text{CMD}}$	6		
7	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ active from $\overline{\text{CMD}}$ active		26	
8	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
9	DIR active from $\overline{\text{CMD}}$ active		22	
10	DIR inactive from $\overline{\text{CMD}}$ inactive		22	
11a	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (IO R&W)		27	
11b	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (M R&W)		19	
12a	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(IO R&W)		25	
12b	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(M R&W)		19	
13	$\overline{\text{SFDBK}}$ inactive from invalid address		25	
14	$\overline{\text{DS16}}$ active from valid address (M R&W)		29	
15	$\overline{\text{DS16}}$ inactive from invalid address		20	
16	Address setup to $\overline{\text{CMD}}$ active	7		
17	DA (15:0) valid address hold from $\overline{\text{CMD}}$ active	4		
18	Write data setup to $\overline{\text{CMD}}$ inactive	10		
19	Write data hold from $\overline{\text{CMD}}$ inactive	7		
20a	Read data valid from $\overline{\text{CMD}}$ active	11.5t		
20b	Write data valid from $\overline{\text{CMD}}$ active	4.5t-50		6
21	Read data setup to RDY high	3.5t-40		7
22	RDY inactive from status (MR)		22	
23	RDY active from $\overline{\text{CMD}}$ active	15t		
24	RDY inactive from $\overline{\text{CMD}}$ inactive		41	
25	$\overline{\text{EBROM}}$ active from valid address		22	
26	$\overline{\text{EBROM}}$ inactive from $\overline{\text{CMD}}$ inactive		29	
27	$\overline{\text{WPLT}}$ active from $\overline{\text{CMD}}$ active		41	
28	$\overline{\text{WPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
29	$\overline{\text{RPLT}}$ active from $\overline{\text{CMD}}$ active		31	
30	$\overline{\text{RPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		23	
31, 32	VCLK1 delay from $\overline{\text{CMD}}$		33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

6. This spec includes 50 ns worst case delay from DA to MD bus.
7. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING, CPU READ AND WRITE			
1	$\overline{RAS10}$, $\overline{RAS32}$ cycle time	9t		
2a	$\overline{RAS10}$, $\overline{RAS32}$ pulse width low	5t-8	5t	
2b	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ high	5t-11	5t-2	
3	$\overline{RAS10}$, $\overline{RAS32}$ precharge	4t+1	4t+8	
4	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ low	2t-11	2t+2	
5a	$\overline{CAS10}$, $\overline{CAS32}$ low to $\overline{RAS10}$, $\overline{RAS32}$ high	3t-8	3t+3	
5b	$\overline{CAS10}$, $\overline{CAS32}$ pulse width low	3t-4	3t	
6	$\overline{CAS10}$, $\overline{CAS32}$ high to $\overline{RAS10}$, $\overline{RAS32}$ low	4t+2	4t+14	
7	Row Address setup to $\overline{RAS10}$, $\overline{RAS32}$ low	1t-10	1t+5	
8	Row Address hold from $\overline{RAS10}$, $\overline{RAS32}$ low	1t-6	1t+8	
9	Column address setup to $\overline{CAS10}$, $\overline{CAS32}$ low	1t-12	1t+1	
10	Column address hold from $\overline{CAS10}$, $\overline{CAS32}$ low	1.5t	1.5t+14	
11	$\overline{CAS10}$, $\overline{CAS32}$ precharge high	6t	6t+4	
12	WE0:1 low setup to $\overline{CAS10}$, $\overline{RAS10}$ high	2.5t-7	2.5t+4	
13a	WE3:2 low setup to $\overline{CAS32}$, $\overline{RAS32}$ high	5t-7	5t+4	
13b	$\overline{WE3}$, $\overline{WE2}$ pulse width low	5t-2	5t+2	
17	$\overline{WE0}$, $\overline{WE1}$ pulse width low	3t-2	3t+2	
18	Data hold from $\overline{WE0}$, $\overline{WE1}$ active	2t-5		
19	Data setup to $\overline{WE0}$, $\overline{WE1}$ active	1t-5		
20	$\overline{WE0}$, $\overline{WE1}$ low from $\overline{CAS10}$ low	.5t-7	.5t+4	
21	$\overline{WE3}$, $\overline{WE2}$ setup to $\overline{CAS32}$ low	2t-4	2t+7	
22	$\overline{OE10}$, $\overline{OE32}$ low after $\overline{CAS10}$, $\overline{CAS32}$ low	1t-6	1t+5	
23	$\overline{OE10}$, $\overline{OE32}$ high after $\overline{CAS10}$, $\overline{CAS32}$ high	1t-5	1t+5	
24	$\overline{OE10}$, $\overline{OE32}$ pulse width low	3t-3	3t+1	
25	Read data setup to CAS inactive	10		
26	Read data hold from CAS inactive	10		
27	$\overline{RAS32}$ low after $\overline{RAS10}$ low	4.5t-7	4.5t+7	
28	Write data setup to $\overline{CAS\ 32}$	2t-5		
29	Write data hold from $\overline{CAS32}$	1t-5		
30	$\overline{CAS10}$, $\overline{CAS32}$ high after $\overline{OE10}$, $\overline{OE32}$ low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM PAGE MODE READ AND WRITE TIMING			
1	$\overline{RAS10}$, $\overline{RAS32}$ pulse duration	7t		
2	Page mode $\overline{CAS10}$ cycle time	5t		8
3	$\overline{RAS10}$, $\overline{RAS32}$ precharge	4t	4t+8	
4	$\overline{RAS10}$ low to first $\overline{CAS10}$ high	5t-14	5t-2	
5	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ low	2t-11	2t+2	
7	$\overline{CAS10}$, $\overline{CAS32}$, $\overline{OE10}$, $\overline{OE32}$ pulse width high	2t	2t+4	9
8	$\overline{CAS10}$, low to $\overline{RAS10}$ high	3t-8	3t+3	
9	$\overline{CAS32}$ low to $\overline{RAS32}$ high	5t-8	5t+3	
10, 14	Row address setup to $\overline{RAS10}$, $\overline{RAS32}$ low	1t-10	1t+5	
11, 15	Row address hold from $\overline{RAS10}$, $\overline{RAS32}$ low	1t-6	1t+8	
12, 16	Column address setup to $\overline{CAS10}$, $\overline{CAS32}$ low	1t-12	1t+1	
13, 17	Column address hold from $\overline{CAS10}$, $\overline{CAS32}$ low	1.5t	1.5t+14	
18	$\overline{RAS32}$ low after $\overline{RAS10}$ low	4.5t-7	4.5t+7	
19	Read data setup to CAS inactive	10		
20	Read data hold from CAS inactive	10		
21	$\overline{OE10}$, $\overline{OE32}$ pulse width low	3t-3	3t+1	
22	$\overline{OE10}$, $\overline{OE32}$ low after $\overline{CAS10}$, $\overline{CAS32}$ low	1t-6	1t+5	
23	$\overline{OE10}$, $\overline{OE32}$ high after $\overline{CAS10}$, $\overline{CAS32}$ high	1t-5	1t+5	
24	$\overline{CAS10}$, $\overline{CAS32}$ pulse width low	3t-4	3t	
25	$\overline{CAS10}$, $\overline{CAS32}$ high after $\overline{OE10}$, $\overline{OE32}$ low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

8. First cycle is two mclocks longer than this spec.
9. $\overline{CAS10}$ and $\overline{OE10}$ are two mclocks longer for the first cycle.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM REFRESH TIMING			
1	Address Setup to $\overline{RAS10}$ active	2t-5		10
2	Address Hold from $\overline{RAS32}$ active	3t-5		
3	$\overline{RAS10}$ low time	5t-8		
4	$\overline{RAS10}$ high time	4t+1		
5	$\overline{RAS32}$ low time	5t+1		
6	$\overline{RAS32}$ high time	4t-8		
7	RAS cycle time	9t		

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

10. This spec is shorter by 1 mclock for the first cycle.

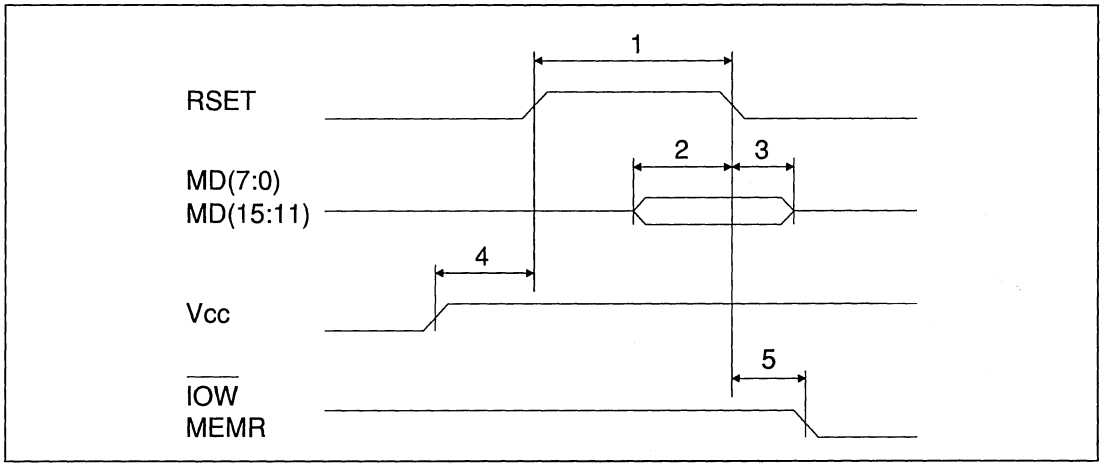

FIGURE 4. RESET TIMING

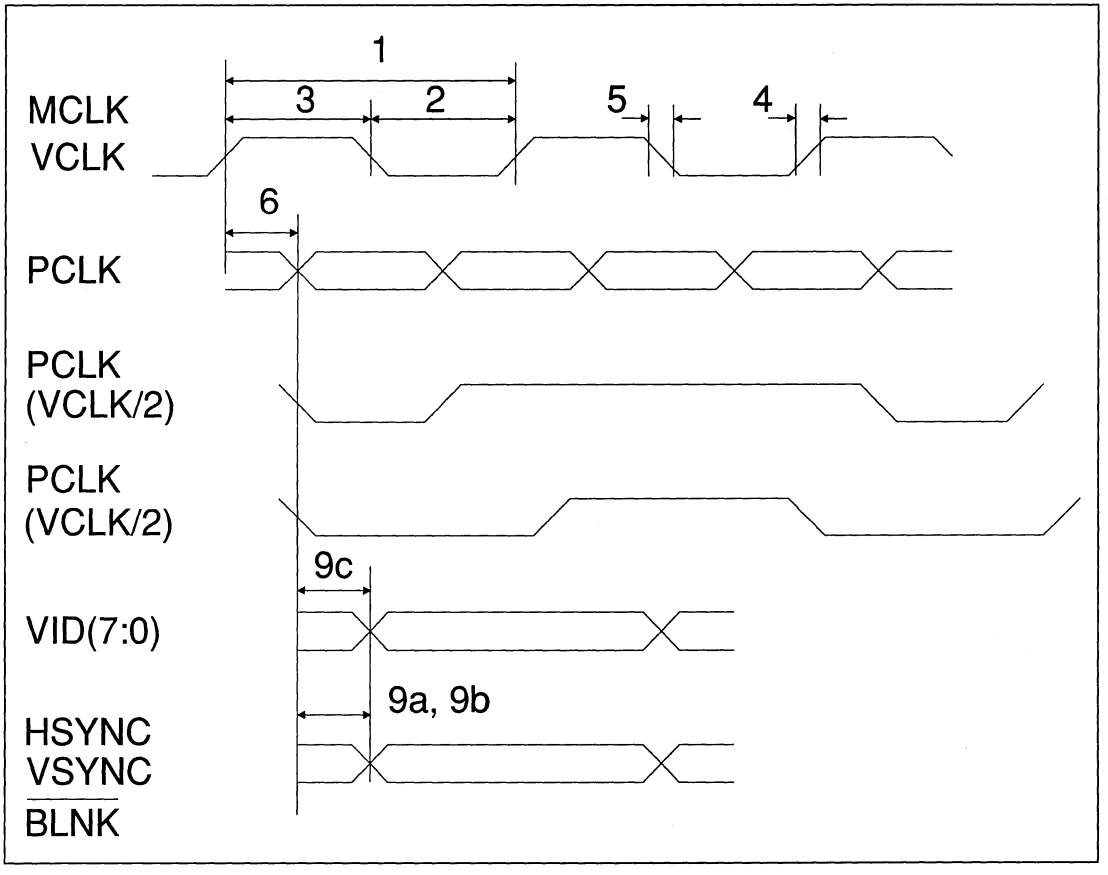

FIGURE 5. CLOCK AND VIDEO TIMING

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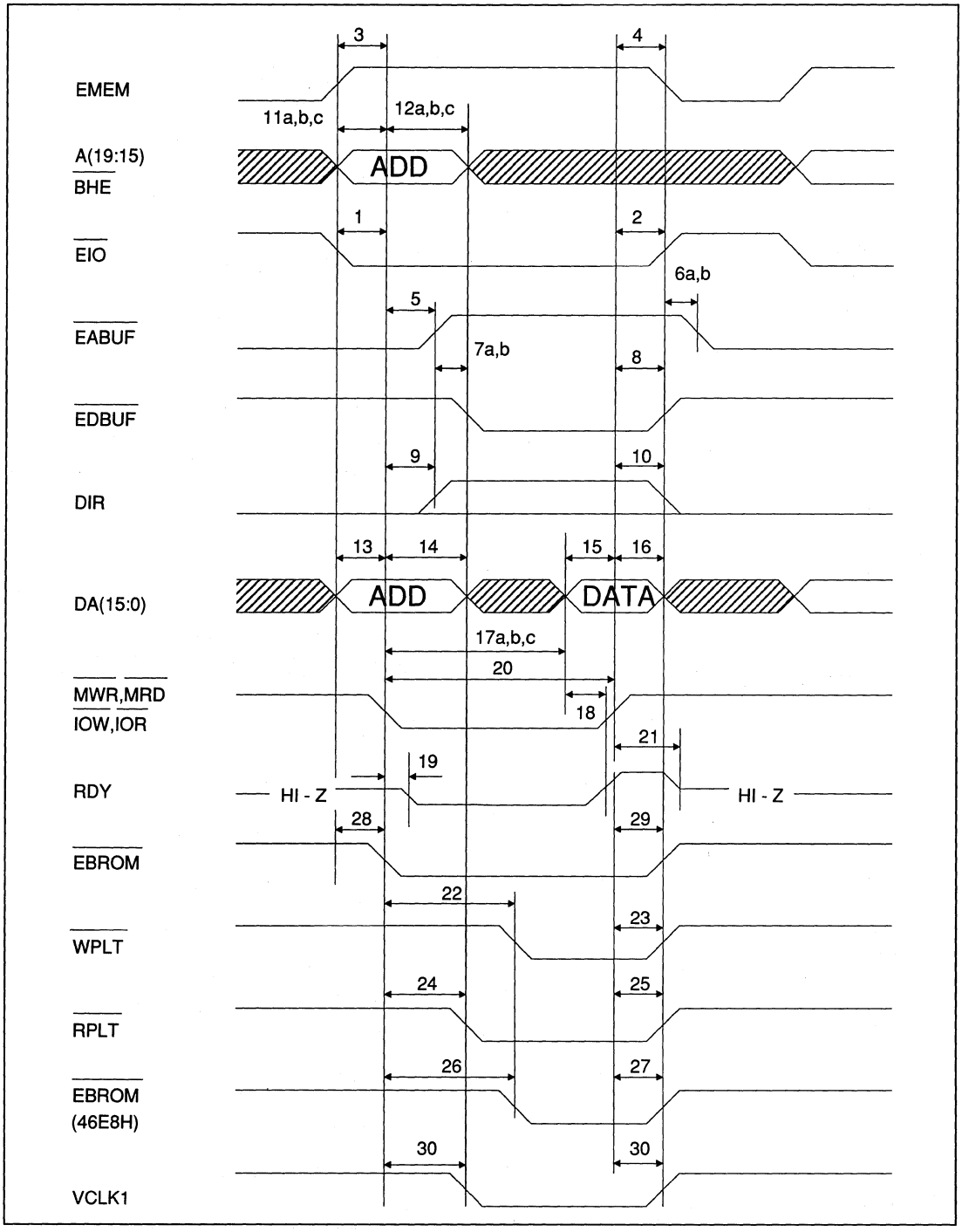

FIGURE 6. AT MODE I/O & MEMORY READ/WRITE TIMING

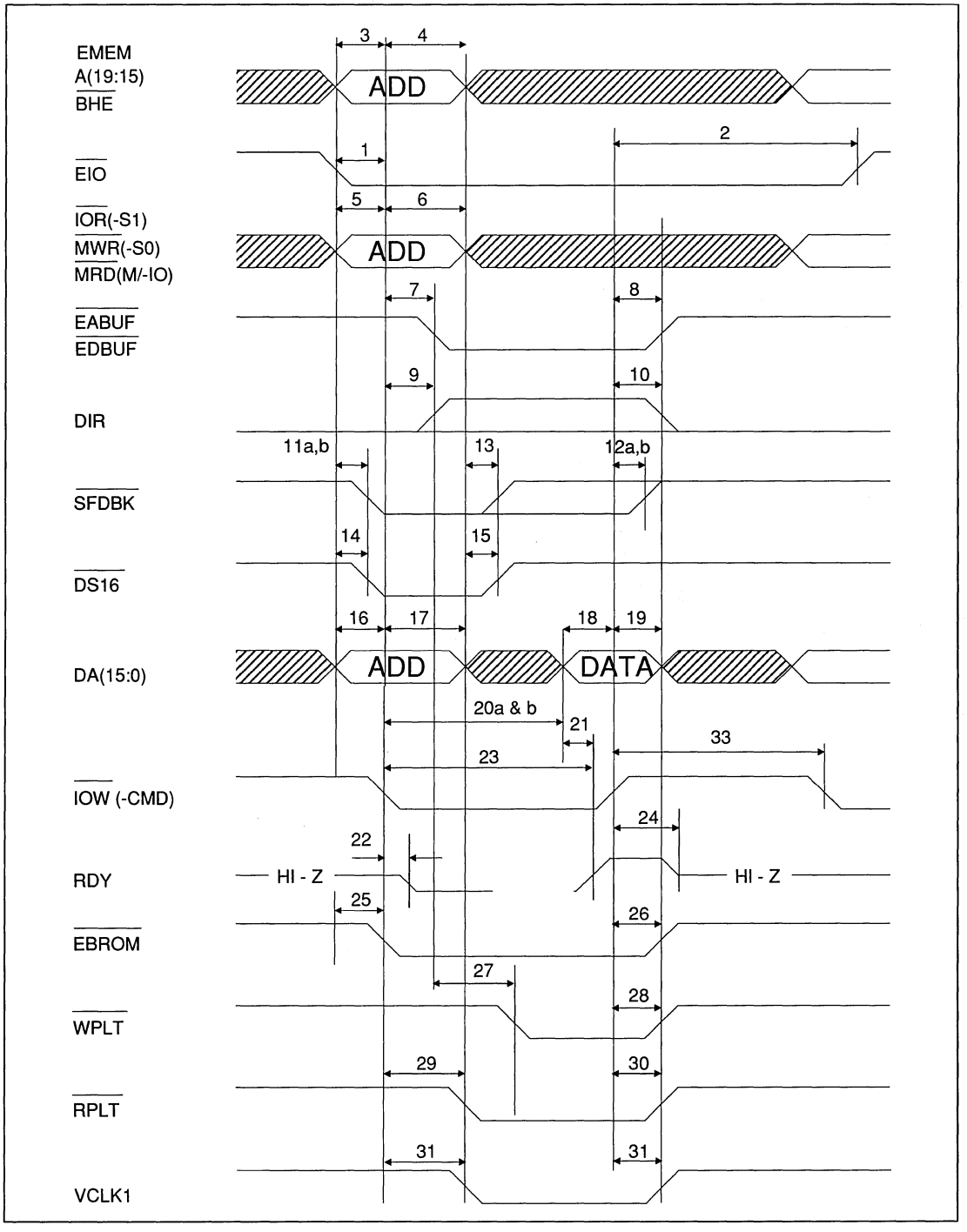

FIGURE 7. MICRO CHANNEL I/O & MEMORY READ & WRITE TIMING

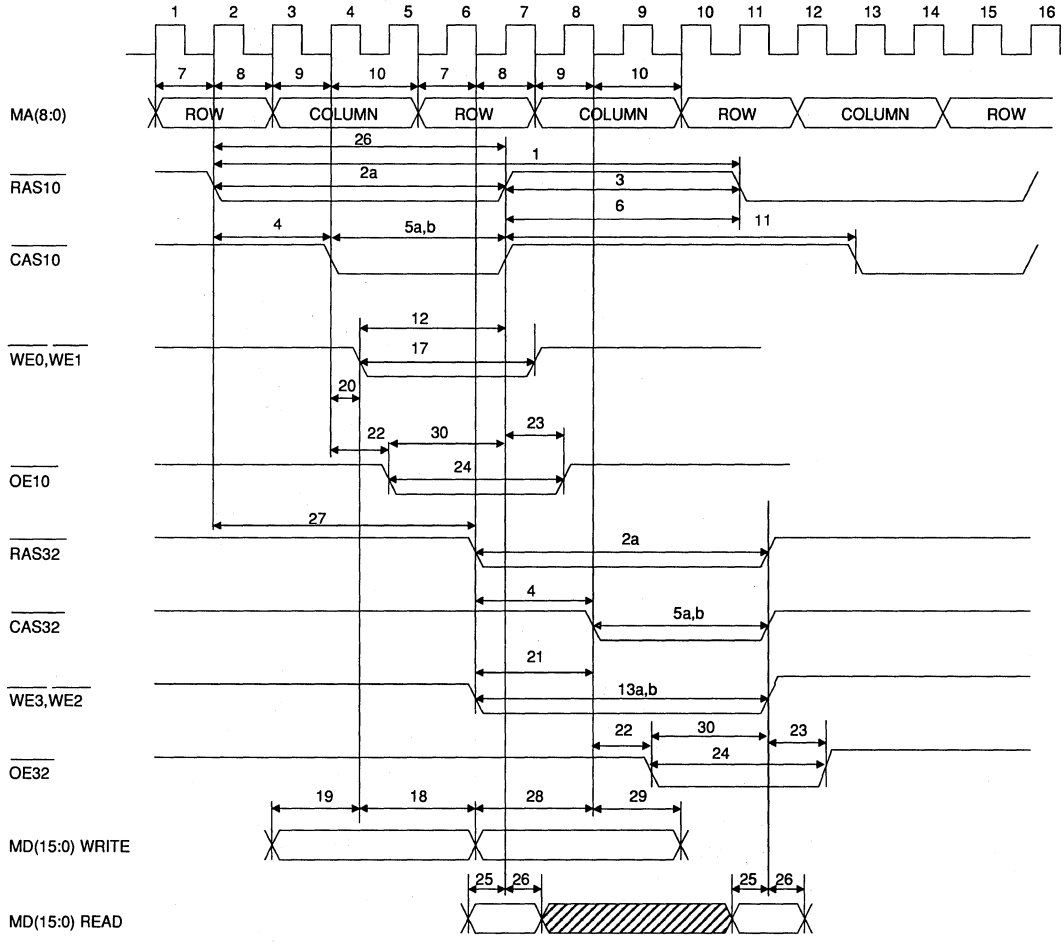

FIGURE 8. CPU READ/WRITE DRAM TIMING

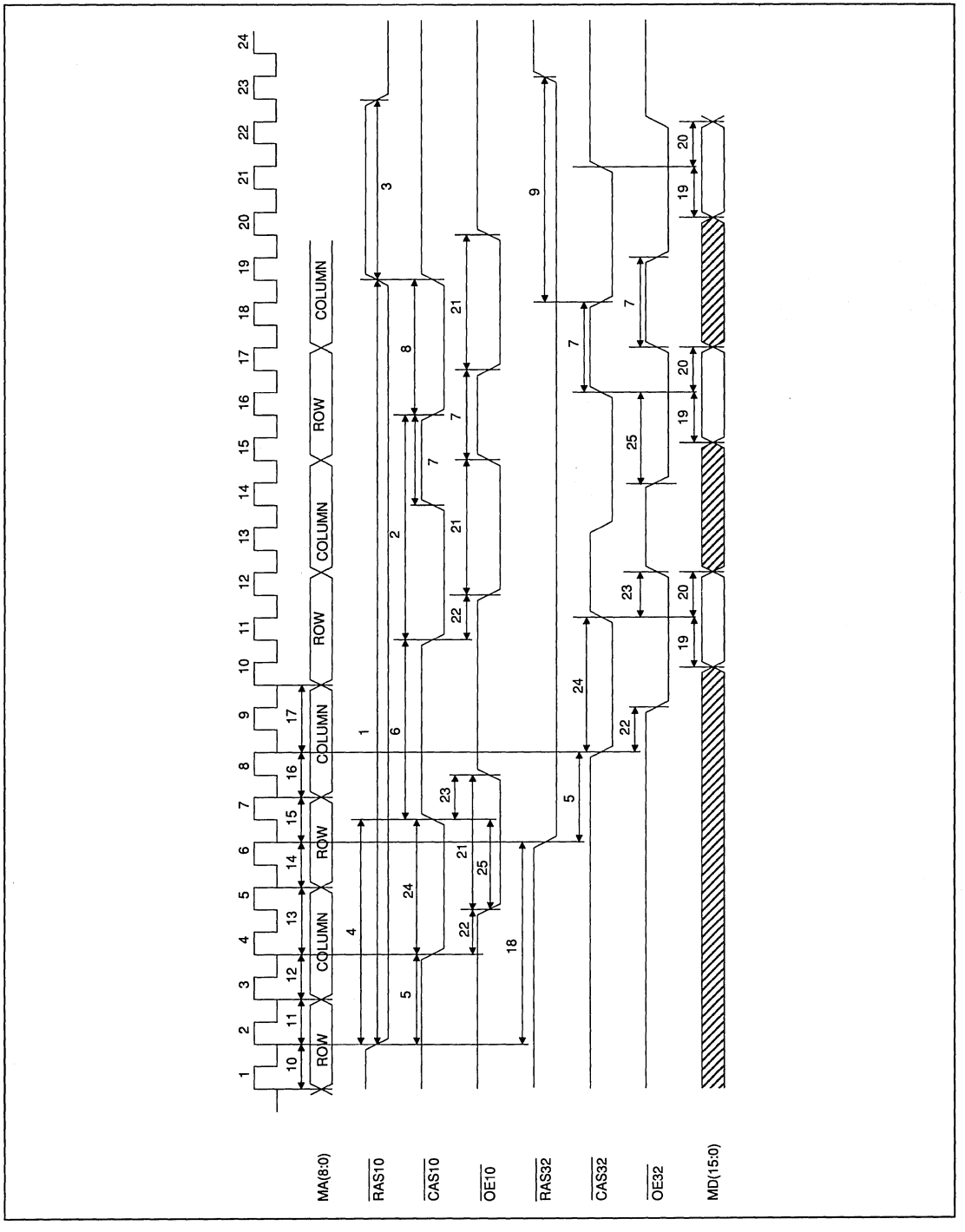

FIGURE 9. DRAM PAGE MODE READ TIMING

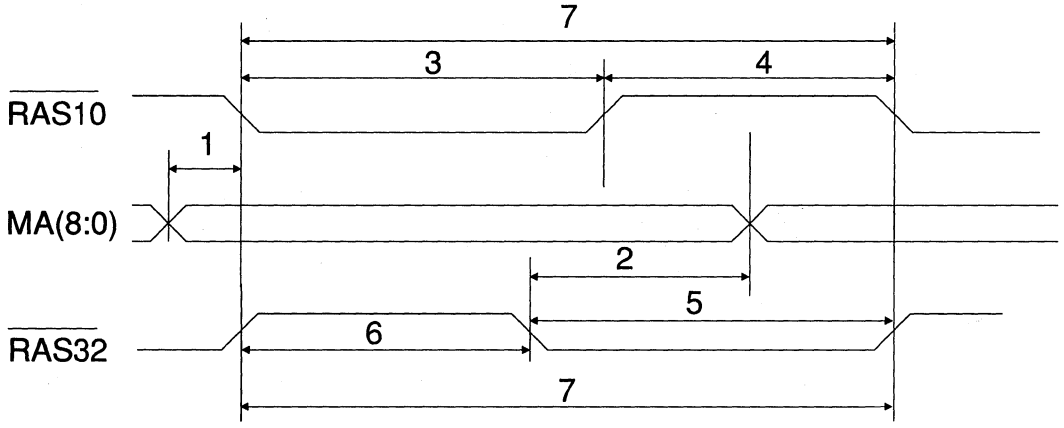

FIGURE 10. DRAM REFRESH TIMING

9.0 WD90C00 REGISTERS

All of the standard IBM registers incorporated inside the WD90C00 are functionally equivalent to the VGA implementation while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the WD90C00 registers in greater detail.

9.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
+Video Subsystem Enable	RW			3C3
NOTE: + Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 4. VGA REGISTERS SUMMARY

9.2 PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR Register Index	RW	3CE	3CE
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10-PR17 INDEX	RW	3B4	3D4
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F			

TABLE 5. PR REGISTERS SUMMARY

NOTE: ALL THE PR REGISTERS ARE WRITE PROTECTED. SEE THE PR REGISTERS' DESCRIPTION FOR MORE DETAILS.

9.3 COMPATIBILITY REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 6. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers

9.4 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

9.5 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

9.5.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

9.5.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

9.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

9.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

9.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

9.6.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

9.6.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

NOTE:

Due to the improved design of the WD90C00, the fuction of Bits (1:0) are not required and are instead implemented as shadow registers.

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

9.6.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

9.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

9.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

9.6.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

9.7 CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	+
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 7. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

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9.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

9.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

9.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

Horizontal blanking begins when the horizontal character counter reaches this character clock value.

9.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.5 End Horizontal Blanking Register Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Signal Width.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

9.7.6 Start Horizontal Retrace Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

9.7.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7
Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**
Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5
Vertical Total Bit 9 (index = 06H).

Bit 4
Line Compare Bit 8 (index = 18H).

++Bit 3
Start Vertical Blank Bit 8 (index =15H).

++Bit 2
Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**
Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0
Vertical Total Bit 8 (index = 06H).

NOTES:
** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

9.7.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7
Reserved.

Bit(6:5)
Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)
Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

9.7.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

9.7.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

9.7.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

9.7.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits. Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

9.7.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

9.7.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

9.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits. The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

9.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) an internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

9.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1.
Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

9.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

9.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

9.7.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

9.7.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

9.7.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

9.7.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared. This creates a split screen where the lower screen does not scroll.

9.8 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

9.8.1 Graphics Index Register Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

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9.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

9.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

9.8.4 Color Compare Register, Read/Write Port 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

9.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

9.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11b to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

9.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all of the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

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9.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

9.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

9.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

9.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

9.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

9.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

9.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

9.9.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.

They determine the overscan or border color.
For monochrome display, this register is set to 0.
Border colors are set as shown above.

9.9.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

9.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

9.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

9.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

9.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

9.10.2 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)
Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

9.10.3 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)
Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2

B/W or Color Display Mode.
0= Color mode selected.
1= B/W mode selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

9.10.4 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2

Red Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

9.10.5 CRT Status Register MDAOperation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

9.10.6 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

9.10.7 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode. A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

9.11 WD90C00 PR REGISTERS

NAME	DESIGNATION	I/0 LOCATION
Address Offset A	PR0A(6:0)	3CF.09
Alternate Address Offset B	PR0B(6:0)	3CF.0A
Memory Size	PR1(7:0)	3CF.0B
Video Select	PR2(7:0)	3CF.0C
CRT Control	PR3(7:0)	3CF.0D
Video Control	PR4(7:0)	3CF.0E
Unlock PRO-PR4	PR5(7:0)	3CF.0F
Unlock PR11 - PR17	PR10(7:0)	3?5.29
EGA Switches	PR11(7:0)	3?5.2A
Scratch Pad	PR12(7:0)	3?5.2B
Interlace H/2 Start	PR13(7:0)	3?5.2C
Interlace H/2 End	PR14(7:0)	3?5.2D
Miscellaneous Control 1	PR15(7:0)	3?5.2E
Miscellaneous Control 2	PR16(7:0)	3?5.2F
Miscellaneous Control 3	PR17(0)	3?5.30
Reserved	---	3?5.31-3?5.3F

The WD90C00 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C00 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port)

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

9.11.1 Address Offset Registers PR0A & PR0B

PR0A - Address Offset Register A
Read/Write Port = 3CF, Index = 09H

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B
Read/Write Port = 3CF, Index = 0AH

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C00 can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. To allow a second video card to co-exist, this space is further limited to a 64 Kbyte video memory partition.

The WD90C00 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 bit 3 is set to 1. PR0A and PR0B provide a seven bit offset that is added to address bits A (18:12) of the system address to form a 20-bit address. It can be thought of as being like segment register DS and ES of the 8088/80X86 architecture. PR0A and PR0B will then provide 4 Kbyte segments.

When PR0B is enabled by setting PR1 bit 3 = 1, PR address offset registers, in a 64K VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), PR0A and Alternate Offset Address register (PR0B) may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H-AFFF:FH while PR0B is mapped from A000:0H-A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register bits 3 and 2), PR0A is mapped from B000:0H-BFFF:FH while PR0B is mapped from A000:0H-AFFF:FH when the Alternate Offset register is enabled.

9.11.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map select
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	16-Bit BIOS ROM
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 KB STANDARD VGA	VGA*
0	1	0	256 KB WD90C00 VGA	PVGA**
1	0	0	512 KB WD90C00 VGA	PVGA
1	1	0	1024 KB WD90C00 VGA	PVGA
X	X	1	ANY OF THE ABOVE	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
** WDI extended modes can fully utilize up to 256 Kbytes.

According to the VGA video memory organization, 256 KB of the available memory space is divided into four 64 KB maps (0-3), each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane. The starting address of the 256 KB video memory buffer can be configured to match other video adapters, and/or, application programs. For example, 256 KB video display buffer with 128 KB or 64 KB segments can start at address A000:0 (Hex) while 32KB segments start at address B000:0 (Hex) or B800:0 (Hex). WD90C00 enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512 KB or 1024 KB. The DRAM organizations supported by the WD90C00 and its associated video space table are shown below.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64Kx4	N/U	256 KB	Four (64KB Per Plane)
64Kx4	BANK SELECT	512 KB	Four (128KB Per Plane)
256Kx4	DRAM PIN A8	1024KB	Four (256KB Per Plane)

When video memory size is 512 KB, and 64Kx4 DRAMs are used two banks of 64 KB form 128 KB per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the $\overline{CAS10}$ and $\overline{CAS32}$ signals. Four planes form the desired 512 KB video memory space. For 1024 KB video memory size, MA8 is directly connected to the A8 address pin of the 256Kx4 DRAMS, and two DRAMS form a 256 KB per plane. Four planes make the desired 1024 KB video memory space.

PR1 bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is same as IBM VGA regardless of PR1 (6) and PR1(7).

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

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RAM ADDRESSING:

PR1(7)	PR1(6)	
1	0	512K TOTAL;128KB/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: "*" Controls CAS external to WD90C00

RAM ADDRESSING:

PR1(7)	PR1(6)	
1	1	1024K TOTAL IN FOUR PLANES;256K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:

1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 bit 5 = 0.

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping in 64 KB space - A000:0H to BFFF:FH Address Range
0	1	First 256 KB in 1MB space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 KB in 1MB space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 KB in greater or equal to 1 MB space - 0000:0H to FFFF:FH Address Range

Bits 5 and 4 can be used in conjunction with external control of EMEM to map video memory decode above the 1 Mbyte address space.

Bit 3

Enable Alternate Address Offset Register PR0B

Bit 2

Enable 16-bit bus for Video Memory
When set to 1, $\overline{DS16}$ will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ be inactive.

Bit 1

This bit will directly reflect signal pin $\overline{ROM16}$ in AT mode or $\overline{CDDS16}$ in MCA mode.
When set to 1, the BIOS ROM has 16 bits data path.

If set to 0, the BIOS ROM data path is 8 bits wide. A pull-up on MD (1) sets this bit to 0 at power on reset. $\overline{ROM16}$ will have the value of 0 when this bit is set.

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

9.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

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Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

9.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0H

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

9.11.5 WD90C00 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

9.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Shift register control. It configures the video shift registers for extended 256-color mode.

9.11.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7 CNF(7) [READ ONLY]
Bit 6 CNF(6) [READ ONLY]
Bit 5 CNF(5) [READ ONLY]
Bit 4 CNF(4) [READ ONLY]
Bit 3 CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

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9.11.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

9.11.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

9.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

9.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

9.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

9.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Low VCLK. Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ)>2

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to 1 in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin $\overline{BLNK}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=$\overline{BLNK}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{BLNK}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

9.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{EBROM}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H)
Programming this bit to 1 causes output $\overline{\text{WPLT}}$ to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C00 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

9.11.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30H

BIT	FUNCTION
7 - 1	Reserved
0	Map out 2K of BIOS ROM

Bit (7:1)

Reserved.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 1. Clearing this bit to 0, enables access of all 32K addresses of the BIOS ROM from C000:0H - C7FF:FH.

9.12 INTERNAL I/O PORTS

9.12.1 AT Mode Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C00 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses. Does not affect Port 46E8H and 102H.

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

9.12.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C00 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C00 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP ($\overline{EIO}$) signal pin is active low, the WD90C00 is in setup mode and port 102H can be accessed.

9.13 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C00. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C00. Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Read/write
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* NOTE: This port is internal to WD90C00.

9.13.1 WD90C00 Configuration Bits CNF (8:2) Non-Read/Non-Write Hardware Port

BIT	FUNCTION
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select

Bits CNF (3:2) are latched internally at power on reset from the corresponding memory data bus pins MD (3:2) while CNF (8) is latched from MD (11). They are connected to the external pull-up or pull-down resistors. Pull-up resistor sets MD(3:2) to logic 1 while pull down resistor sets MD(11) to logic 1. Note, that the configuration bits (3:2) are not readable since they are latched after power up. However, the configuration register bits (8:4) are readable after power up as PR5 bits (7:3). They appear as general purpose read only status bits in the PR5 register.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F).

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

VIDEO CLOCK SOURCE CONTROL
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C00 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

Bus Architecture Select
This bit cannot be written or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.

0 =Micro Channel architecture

1=AT BUS architecture

9.14 EXTERNAL I/O PORT CONSIDERATIONS

9.14.1 Video Subsystem Enable Register Micro Channel Only Read/Write Port 3C3H

BIT	FUNCTION
7 - 1	Unused
0	Video Subsystem Enable

Bit(7:1)

Reserved

Bit 0

When this bit is set to 1, the I/O and memory address decoding for the video subsystem are enabled. When set to 0, this bit disables the video I/O and memroy address decoding. Accessing this register does not affect addressing port 102h POS register.

The WDI WD90C00 does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I/O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I/O port 102H bit O) of the Programmable Option Select (POS). When, WD90C00 is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally.

A.0 APPENDIX

A.1 EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
2. Unlock all the PR registers.
3. Program PR2(6) to 0 for EGA mode.
4. Set PR4 bit 1 to logic 1 for EGA compatibility.
5. Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:

a) Initialize all the registers.
b) Lock CRT controller registers.
c) Force Clock Control rate of the CRT controller.
d) Set EGA emulation mode by programming:
PR11(3)=1; Set EGA emulation on PS/2 type display
PR14(6)=1; Vertical double scan
PR11(2)=1; Lock clock select
PR11(0)=1; Lock 8/9 dot timing.
PR14(7)=1; Enable IRQ (optional)
e) Lock the PR registers PRO-PR5 and PR10-PR17.
f) Read protect PR registers.

8. When EGA is required on a TTL monitor, the suggested steps are:

a) Initialize all the registers.
b) Set EGA TTL mode by programming:
PR11(3)=0;EGA TTL
PR14(7)=1;Enable IRQ
PR15(6)=1;Set Low Clock
PR14(7)=1;Enable IRQ
c) Lock PR registers PRO-PR5 and PR10-PR17
d) Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlights all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?"= "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)
EGA: Not used

A.3 SEQUENCER REGISTERS INDEX PORT = 3C4, PORT 3C5

A.3.1 Clocking Mode Register (Index = 01)

Bits (7:4)
EGA: Not Used

Bits (3,2)
EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1
EGA: Set to zero

Bit (0)
EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)
EGA: Not Used

Bits (3:2)
EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)
EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)
EGA: Not Used

Bits (2:1)
EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0
EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS INDEX PORT= 3?4 DATA PORT = 3?5

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to CRT Controller Overflow Register bits (4:0) in the VGA section.

A.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definitions in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

Enable Vertical Retrace Interrupt.
EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

Clear Vertical Retrace Interrupt.
EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS INDEX PORT = 3CEH DATA PORT = 3CFH

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)

EGA: Not Used

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per the table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec. Green/Inten	VID 4
3	Sec. Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register (Index = 10)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register (Index = 11)

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register (Index = 13)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7 APPLICATIONS

The WD90C00 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data book should supplement the information provided in this section. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 11 through 20 are shown along with their brief description on the subsequent pages.

Figure 11 highlights the various WD90C00 Processor, memory, and I/0 interfaces.

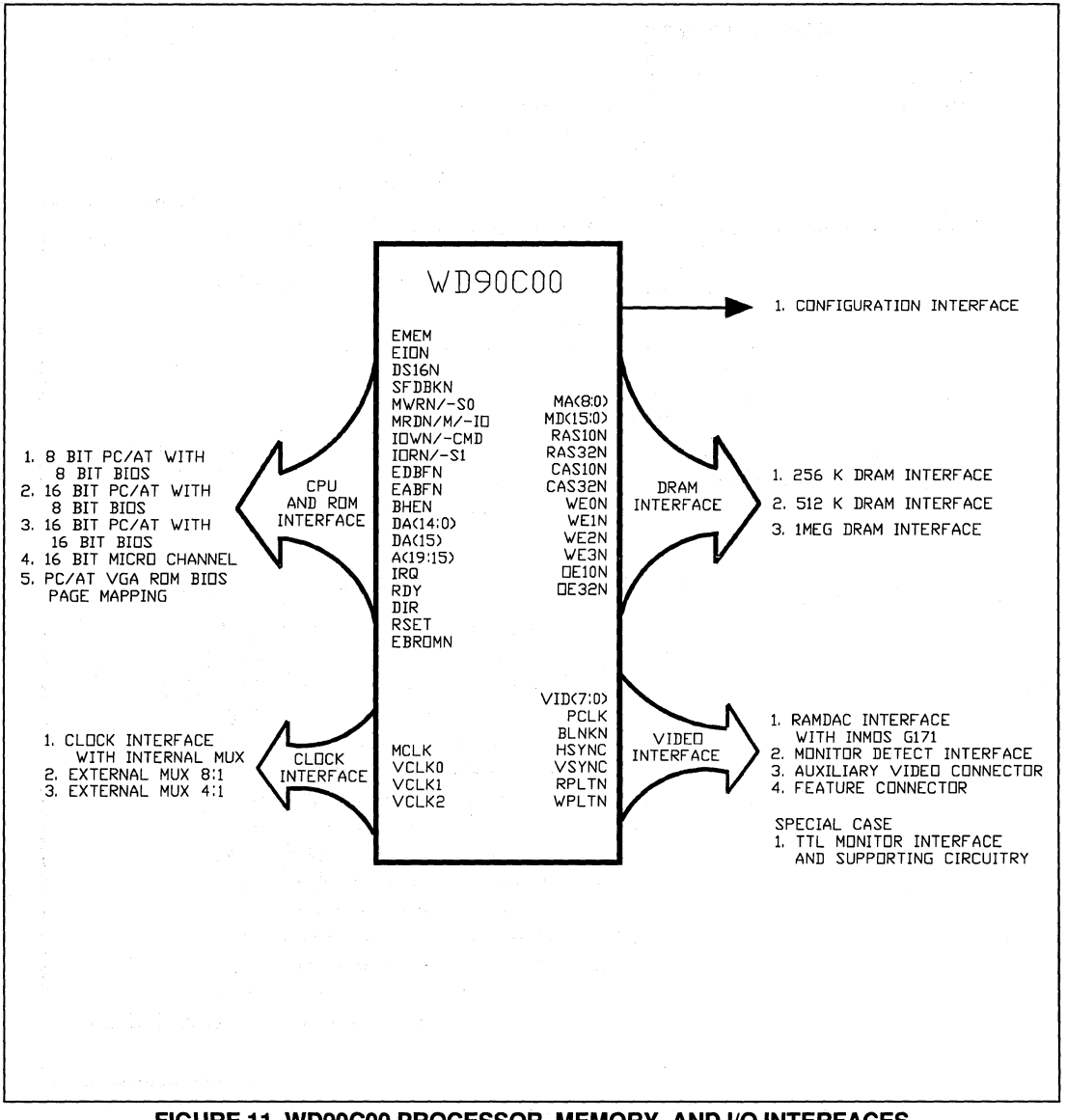

FIGURE 11. WD90C00 PROCESSOR, MEMORY, AND I/O INTERFACES

Figure 12 shows a block diagram of the WD90C00 with 8-bit PC/AT interface using an 8-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: "*" = Logic AND function, "/" = Inverted function, and "+" = Logic OR function.

"*" NOTE PA(14:12) CAN BE FROM PAGE MAPPING LOGIC.

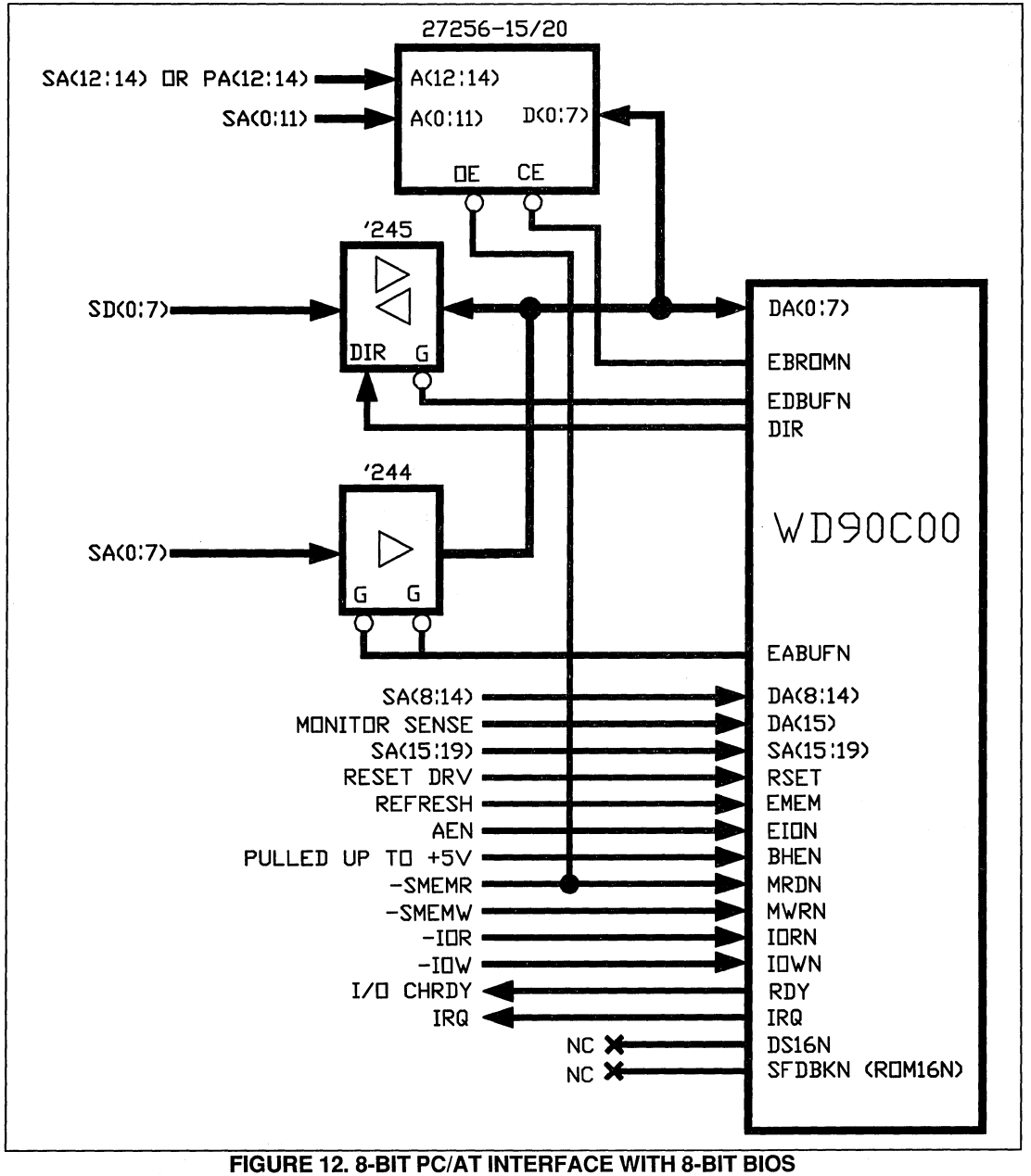

FIGURE 12. 8-BIT PC/AT INTERFACE WITH 8-BIT BIOS

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Figure 13 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C00. The processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers, BIOS ROM, and auto monitor sense are also shown in it. Note, PA (14:12) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBFN1.

/EDBFN1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N + EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N.

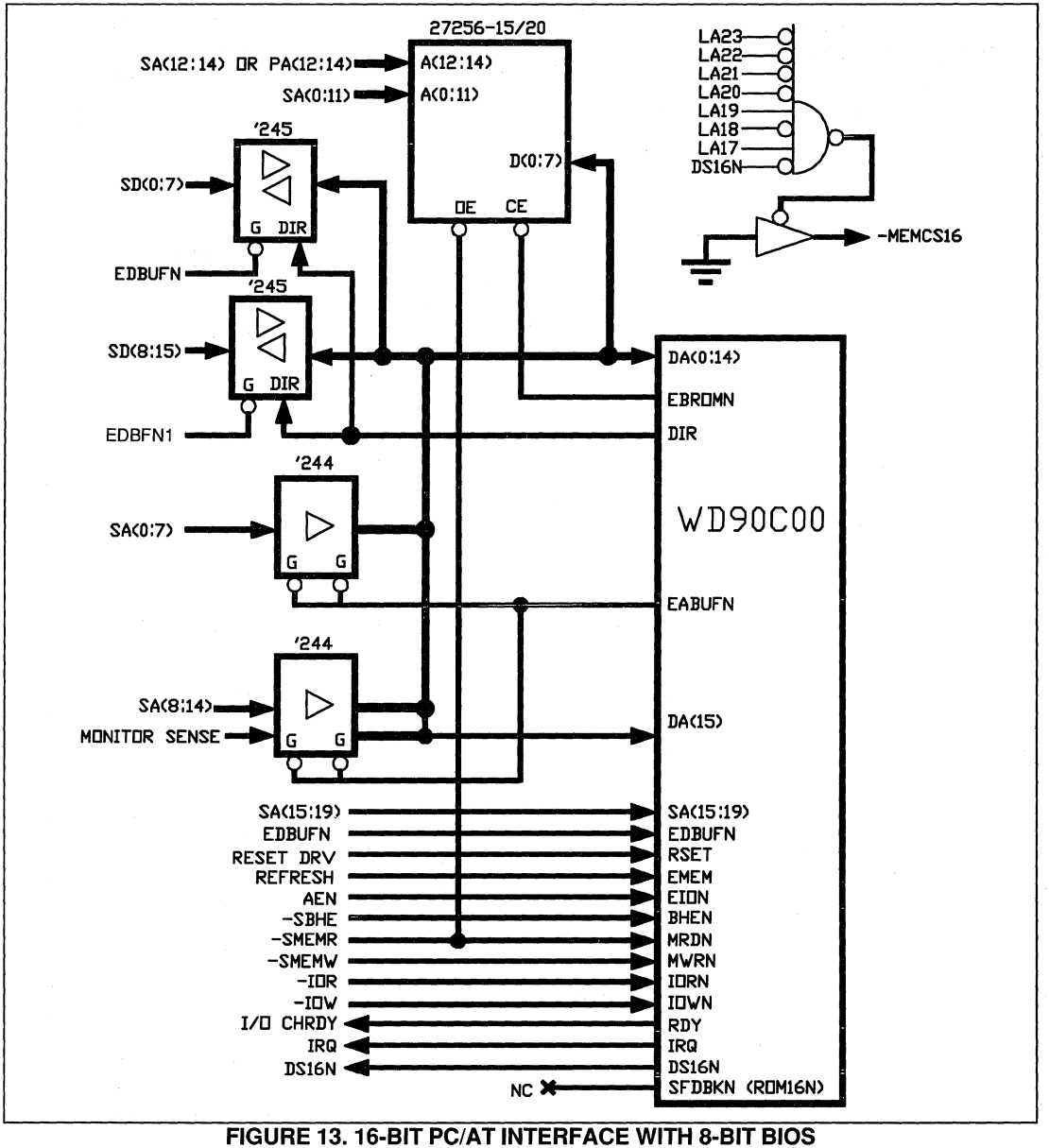

FIGURE 13. 16-BIT PC/AT INTERFACE WITH 8-BIT BIOS

Figure 14 illustrates a 16-bit PC/AT interface with a 16-bit BIOS ROM implementation using WD90C00. The system data bus SD(15:0), address and data bus buffers, and auto monitor sense input is presented. The (16K X 8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation is limited to certain bus speeds as SA15 and SA16 are used.

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N + /EBROMN * /SBHE * SA0 * /ROM16N * /SMEMR

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N + /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN.

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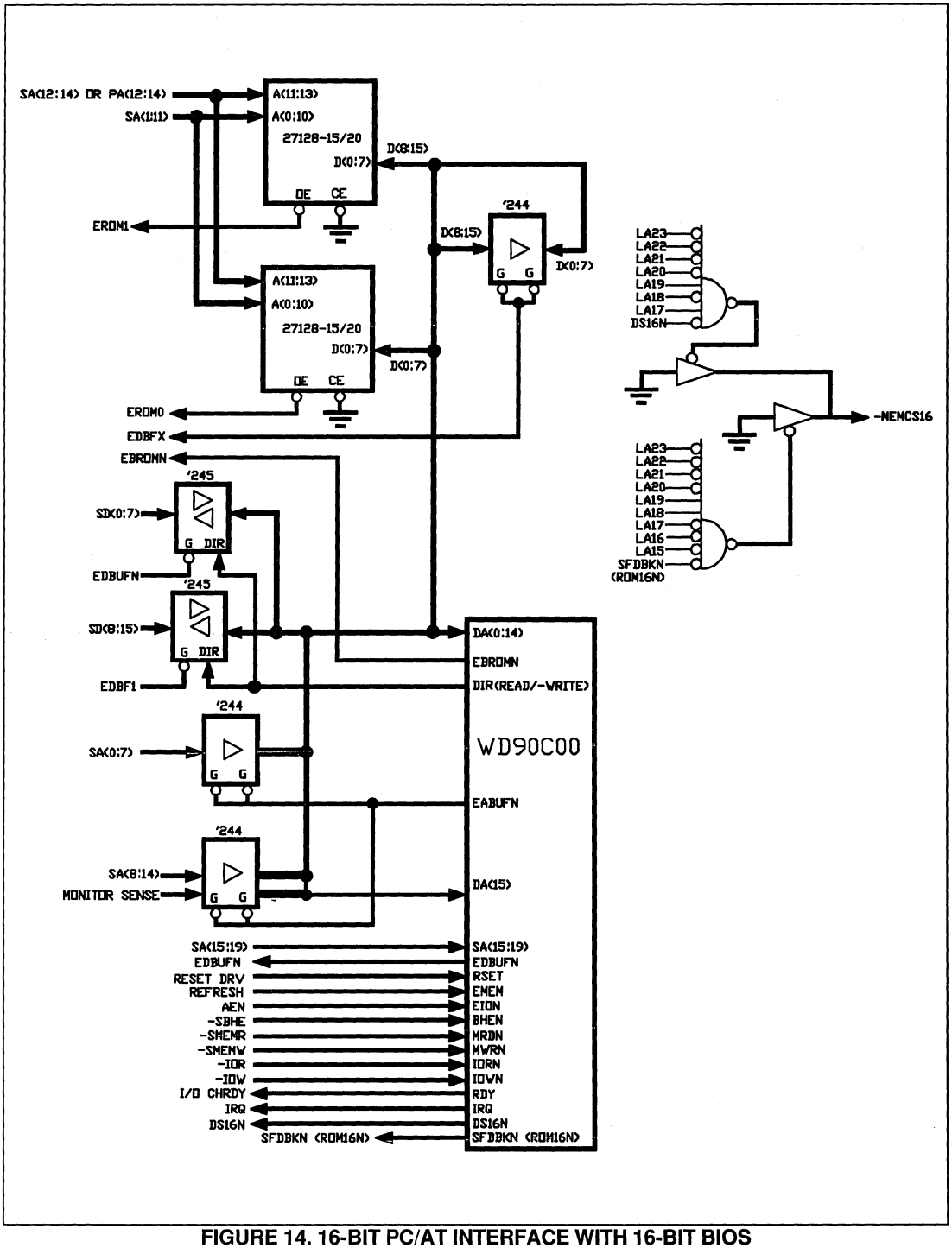

FIGURE 14. 16-BIT PC/AT INTERFACE WITH 16-BIT BIOS

Figure 15 illustrates the WD90C00 and a 16-bit Micro Channel interface. The system data bus upper byte bits D(14:8) and lower data bus byte D(7:0) are sampled and buffered for the WD90C00 input pins DA(14:0). Likewise, system address byte upper bits A(14:8) and lower address byte A(7:0) are buffered and gated to the WD90C00 input pins DA(14:0). The monitor sense input buffer and D15 are gated into the DA15 input of the WD90C00. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the WD90C00. Setup must be latched (OFF) with -CMD.

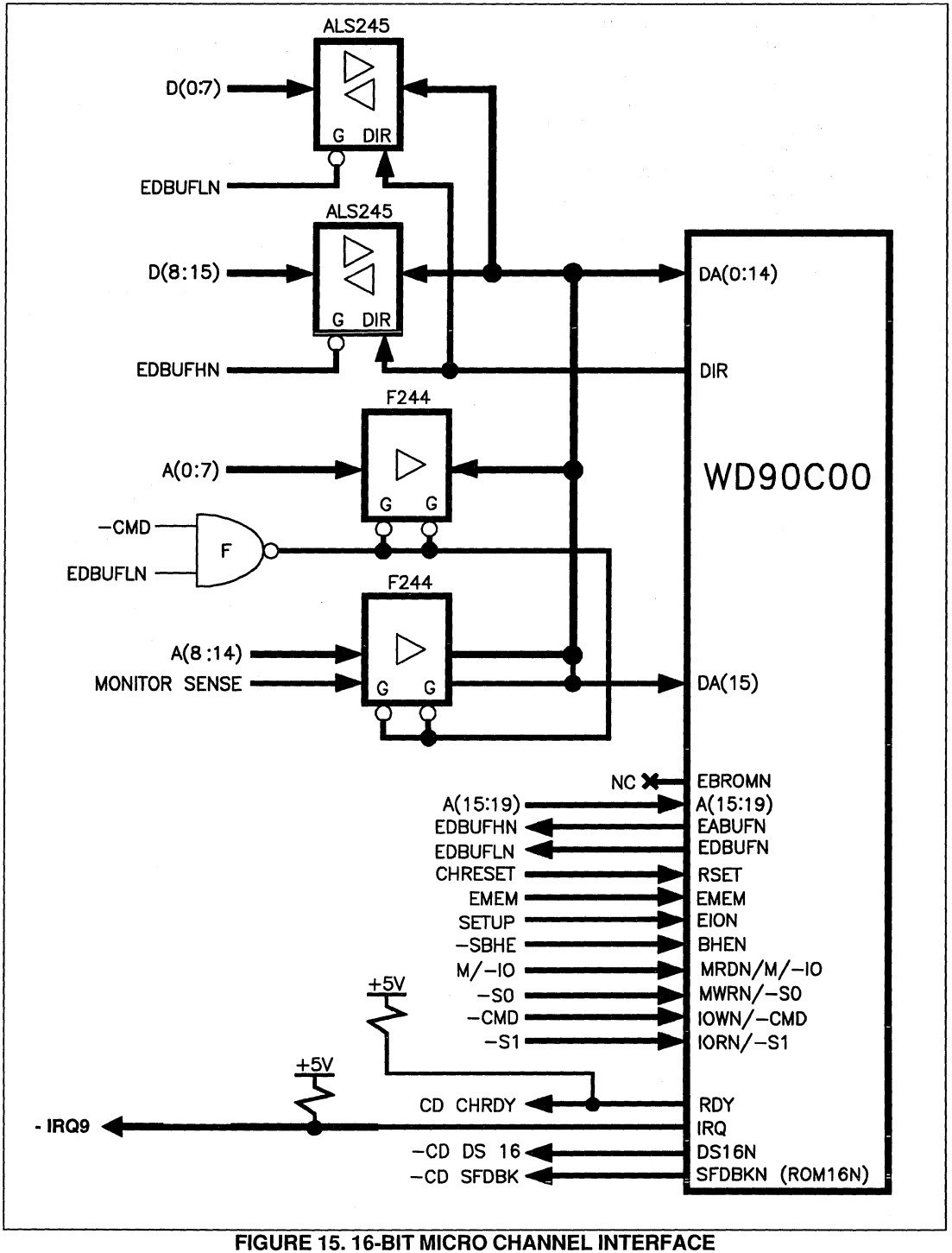

FIGURE 15. 16-BIT MICRO CHANNEL INTERFACE

Figure 16 illustrates the WD90C00 with 1024 KB video memory organization using four 256 KB maps. Each 256 KB map is made from two (256K X 4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles. The WD90C00 also supports 256 KB, or 512 KB video memory organization using (64K X 4) DRAM modules. The 256 KB configuration just does not have MA8 connected to the DRAMs. The 512 KB configuration uses MA8 as select to multiplex the $\overline{CAS10}$ and $\overline{CAS32}$ signals to two 256 KB banks of eight 64K X 4 DRAMs.

Figure 17 illustrates the WD90C00 and RAMDAC (INMOS G171) interface block diagram for analog monitors.

NOTE:
LA(1), LA(0) ARE LATCHED ADDRESSES.
DA(7:0) ARE MULTIPLEXED DATA BITS.

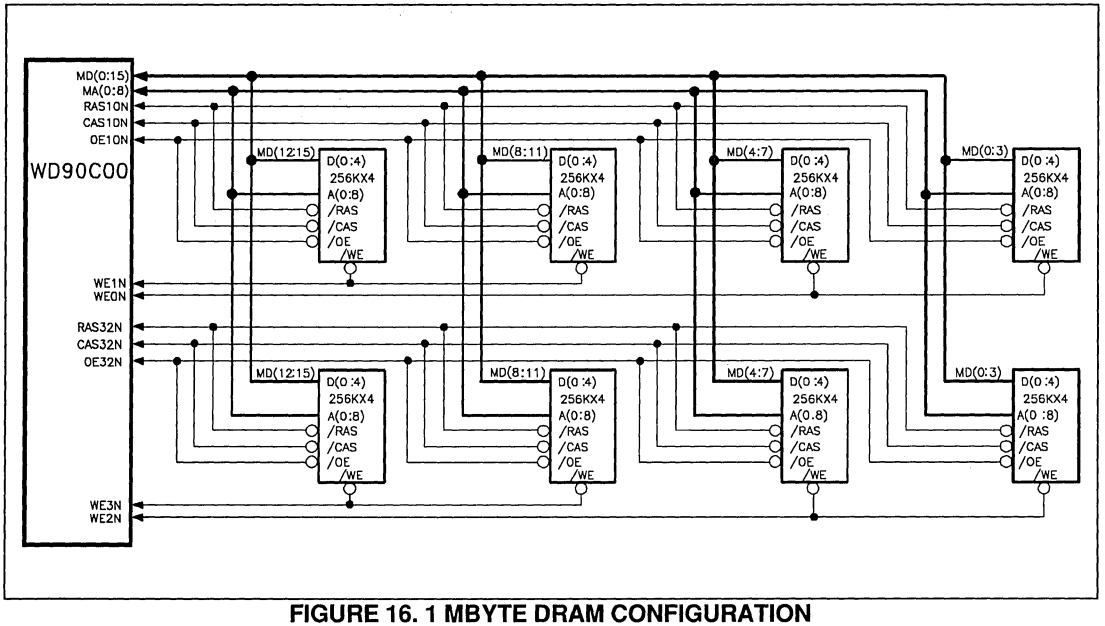

FIGURE 16. 1 MBYTE DRAM CONFIGURATION

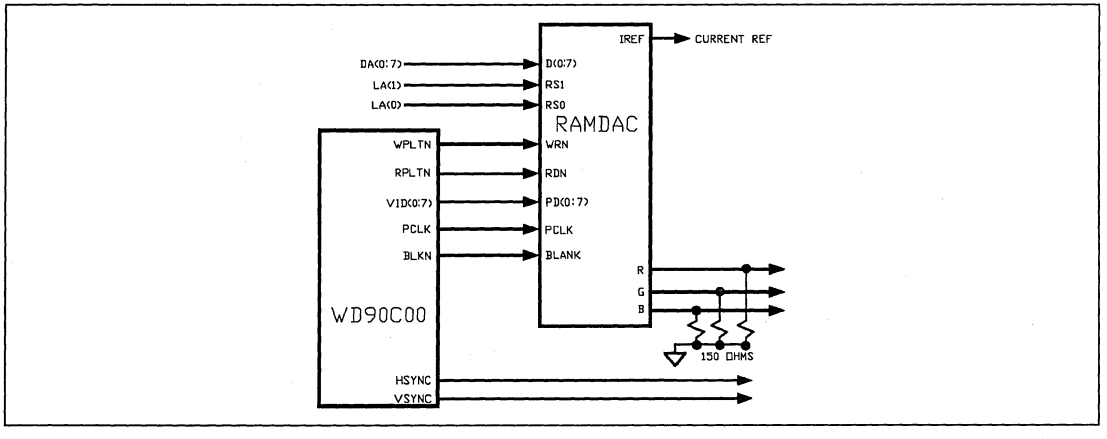

FIGURE 17. RAMDAC INTERFACE

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Figure 18 illustrates the WD90C00 and TTL monitor connections.

NOTE:
1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using WD90C00, install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

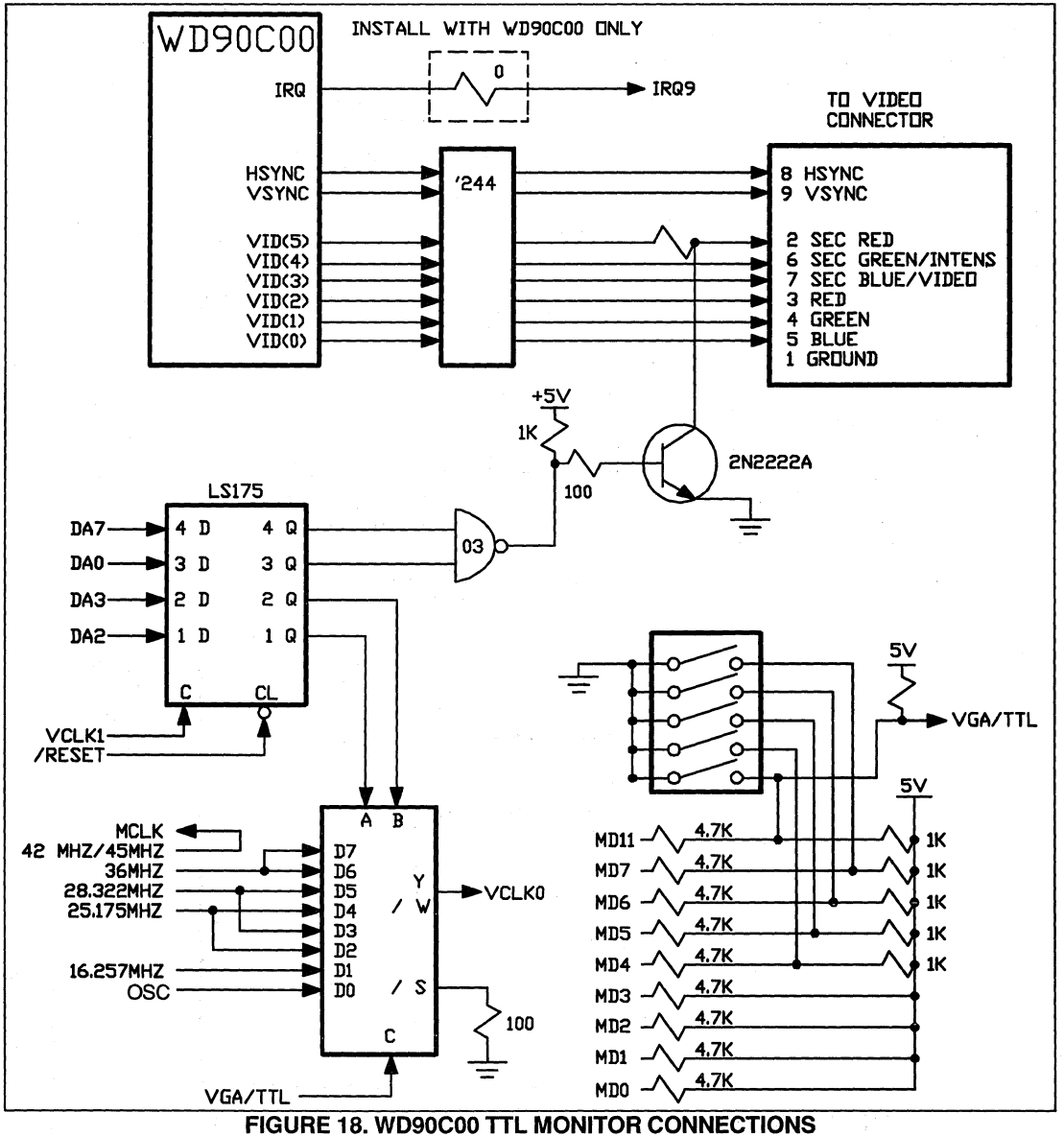

FIGURE 18. WD90C00 TTL MONITOR CONNECTIONS

Figure 19 presents WD90C00 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C00 signal pins (VCLK1, VCLK2) inputs with a 10K Ohm resistor.

Figure 20 illustrates WD90C00 pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high with a 4.7K Ohm resistor and PR 15 bit 5 = 1 .

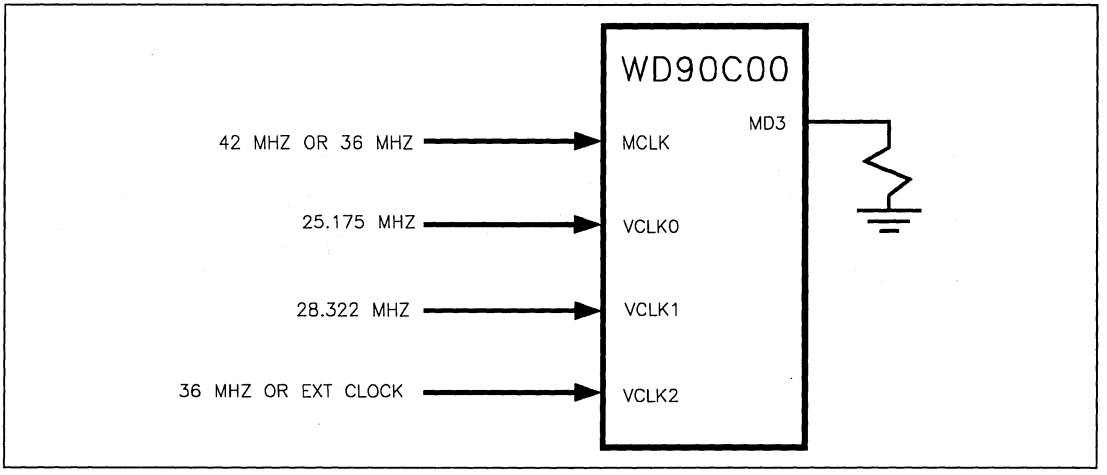

FIGURE 19. CLOCK INTERFACE

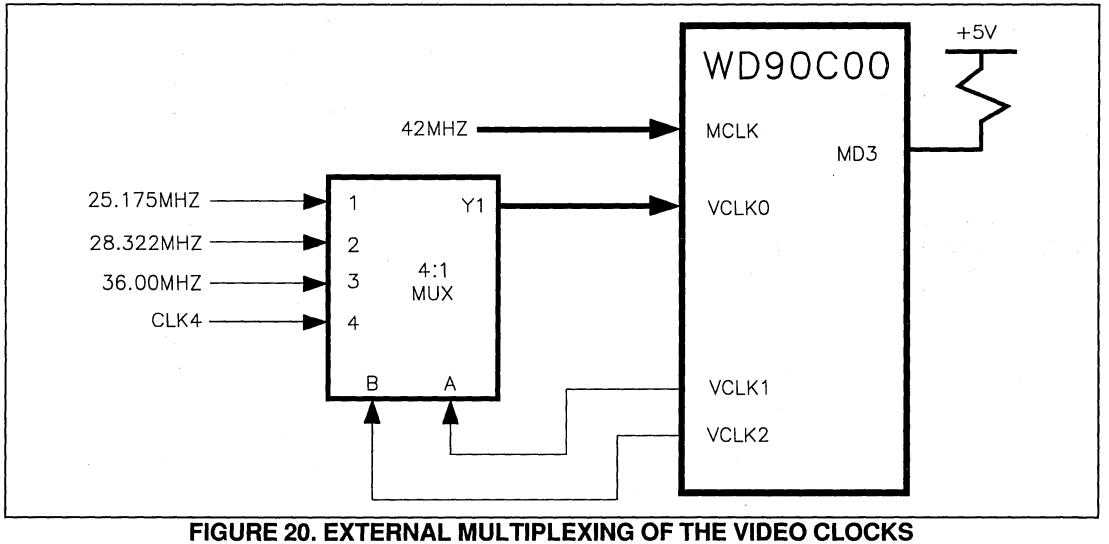

FIGURE 20. EXTERNAL MULTIPLEXING OF THE VIDEO CLOCKS

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A.8 WD90C00 POWER UP CONFIGURATION

The WD90C00 uses the MD(0:7) and MD(11:15) input pins to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0), PR11(7:4), and CNF(8:2) are the internal registers that are configured on power up. CNF(3:2) and PR11(7:4) will latch a noninverted value (pull up register = 1) into it and the other will latch an inverted value. For more details see the PR register and Pin out sections.

PR 1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the WD90C00. A value will map it in.

PR 1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the WD90C00 that the ROM BIOS data path is 16 bits. The WD90C00 will bring SFDBKN active low in AT mode (static signal) and SFKBKN can be used to externally generate -MEMCS16 (of the AT bus) for 16 bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

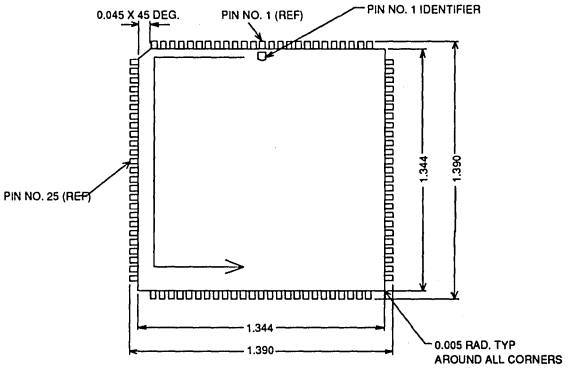
PR11(4:7) bits will latch the EGA switch settings (SW4:SW1) after power up. A pull up resistor will set the appropriate PR11 register bit (4:7) to a logic 1.

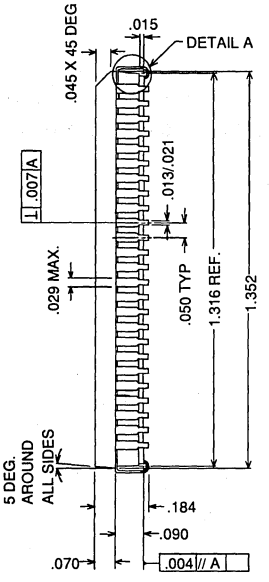
CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the WD90C00 for IBM PC/XT/AT architecture. A value of 0 will configure the WD90C00 for IBM PS/2 Micro Channel Architecture. WD90C00 Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the WD90C00 pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

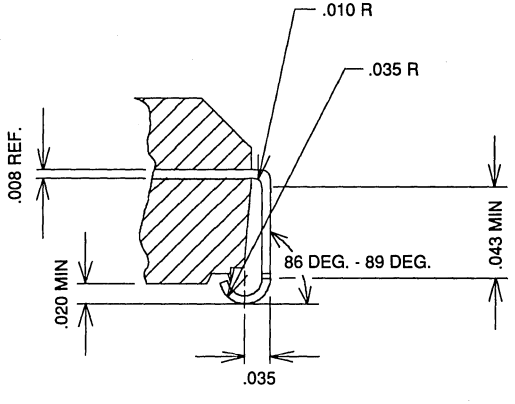
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through PR Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If unused by the BIOS, they are available to the application software.

CNF(8) will indicate that a TTL display or an analog monitor is present in the video subsystem. A Pull up resistor on MD(11) causes CNF(8) to be latched 0 indicating that VGA compatible analog display is in the video subsystem.





DETAIL A



NOTE: ALL DIMENSIONS ARE IN INCHES.

FIGURE 21. 100-PIN PLCC PACKAGE DIMENSIONS

12

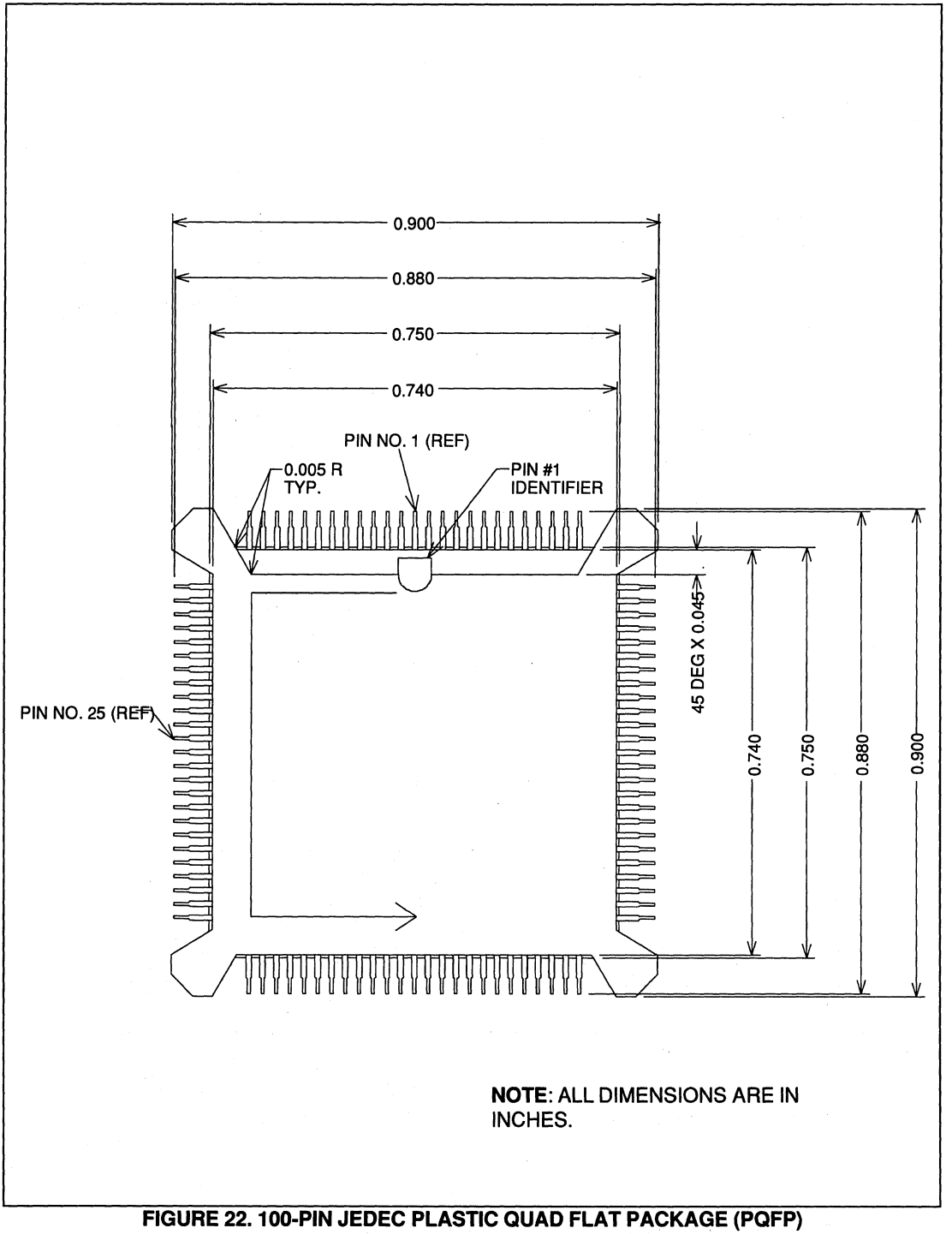
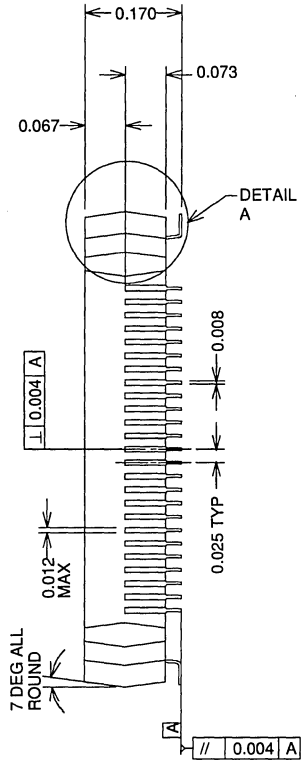
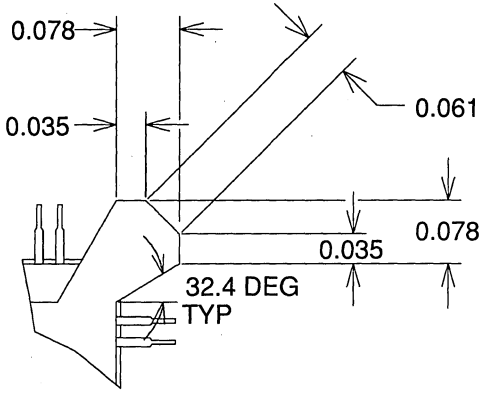


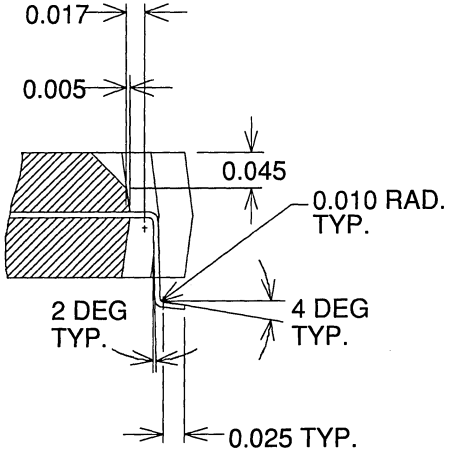
FIGURE 22. 100-PIN JEDEC PLASTIC QUAD FLAT PACKAGE (PQFP)



SIDE VIEW



BUMPER DETAIL



DETAIL A

NOTE: ALL DIMENSIONS ARE IN INCHES.

FIGURE 23. 100-PIN JEDEC (PQFP) PACKAGE DIMENSIONS

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A.9 REFERENCES

A list of references for generating the WD90C00 data sheet is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available in the market.

WD90C11, WD90C11A

Enhanced VGA

Controller

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD90C11 and WD90C11A devices. WD90C11 is a 1.25 micron CMOS device, and WD90C11A is a 0.9 micron CMOS device. In most instances the WD90C11 and WD90C11A operate similarly and are referred to in this document as WD90C11(A). Where there are differences, the devices are identified specifically.

This document supplies order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information, and associated references.

Ordering Information:
WD90C11 Part Numbers:
WD90C11LR00 03 or
WD90C11LR00 02
- device tested to 45 MHz, VCLK
WD90C11A Part Number:
WD90C11ALR00 02

1.2 FEATURES

- Provides single chip video graphics solution for IBM PC, XT, AT, and PS/2 compatible systems.
- Supports two or four 256 Kbyte by 4 DRAMs, providing high performance, high resolution, and 256 colors.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
- With 512 Kbytes of DRAM (four 256 Kb by 4), will support 1024 by 768 by 16 colors interlaced or non-interlaced, 640 by 400 by 256 colors, 640 by 480 by 256 colors, 800 by 600 by 256 colors. With two 256K by 4 DRAMs will support 1024 by 768 by 2/4 colors, 800 by 600 by 16 colors, 132 column text.
- Write cache for improved CPU write performance.
- 8- or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Up to 65 MHz maximum video clock rate.
- Up to 42 MHz maximum memory clock rate. (45 MHz for WD90C11A)
- Up to four simultaneous displayable fonts.
- 6, 7, 8, and 9 pixel wide fonts.
- Up to 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Total of 18 address bits for cursor location and start address.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC, and overscan registers.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- 132-pin Plastic Flat Pack (PFP) JEDEC package.
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for PC / XT / AT, and Micro Channel with minimum external component support.
- I/O pin mapping and video output signature analysis to facilitate system level test. (WD90C11A only).

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1.3 GENERAL DESCRIPTION

The Western Digital Imaging WD90C11 and WD90C11A are CMOS VLSI devices that allow the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300.

The enhancements include Western Digital registers for EGA register level compatibility for PS/2 and TTL monitors, 1024 by 768 color graphics support, and integrated Micro Channel and AT interface. A major advantage of the WD90C11(A) is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C11(A) supports either two or four 256 Kbyte by 4 DRAMs for operation.

2.0 WD90C11(A) ARCHITECTURE

The WD90C11(A) contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C11(A) also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

The WD90C11(A) controls the interfacing between the system microprocessor and video memory. Since the WD90C11(A) arbitrates video memory between the system microprocessor and the CRT Controller contained within the WD90C11(A), all data passes through the WD90C11(A) when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using only two or four 256K by 4 DRAMs.

2.1 WD90C11(A) MODULES

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.

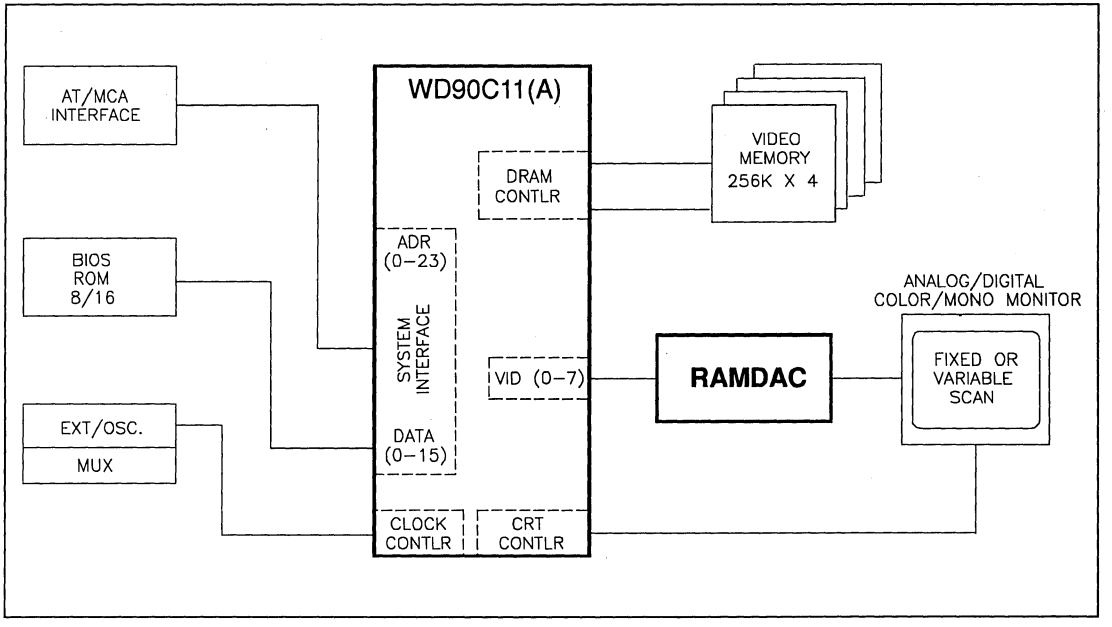

FIGURE 2-1. SYSTEM BLOCK DIAGRAM

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3.0 WD90C11(A) INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C11(A) is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C11(A) Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C11(A) operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C11(A) provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8 or 16 bit data path modes. WD90C11(A) also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8- or 16-bit mode and control an 8 or 16 bit BIOS ROM.

The I/O data path can be programmed to be either 16- or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C11(A).

The WD90C11(A) has a display memory write cache which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C11(A) will provide the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT for setup, and 102H for VGA enable, have been implemented internally in the WD90C11(A).

3.2 DRAM INTERFACE

The WD90C11(A) optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as four planes to support all modes from only two or four 256K by 4 DRAMs by making use of its Fast Page Access of memory. Each plane can be configured as 64 KBytes (128, 256, or 512 Kbyte total).

For display refresh cycles, the WD90C11(A) will perform page mode read operations on the video memory in graphics modes. In alpha modes, a choice of page video memory read operation is also provided. For video memory write operations during graphics or alpha modes, the WD90C11/A will generate standard RAS/CAS cycles as needed. The WD90C11(A) will also refresh the DRAMs with 3 or 5 (CAS before RAS) refresh cycles after every horizontal scan line.

Two or four 256K by 4, 80 ns DRAMs and a 37.5 MHz MCLK are required for all modes. 70 ns DRAMs can be used with 42 MHz MCLK.

3.3 VIDEO INTERFACE

The WD90C11(A) is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C11(A) provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C11(A) can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C11(A). The WD90C11(A) also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

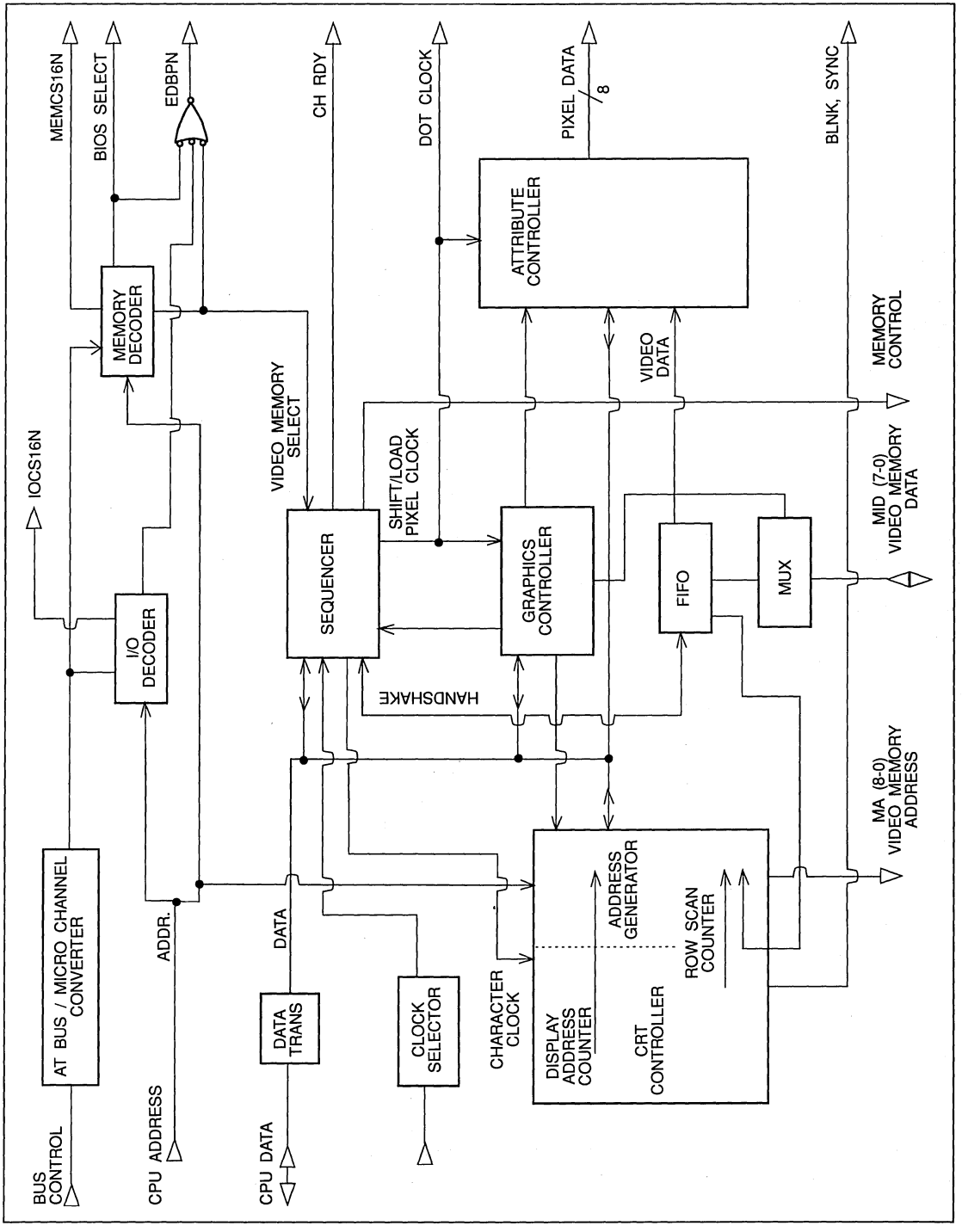

FIGURE 3-1. WD90C11(A) BLOCK DIAGRAM

3.4 CLOCK INTERFACE

The WD90C11(A) has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCK1 and VCK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock .

3.5 POWER-UP CONFIGURATION

The WD90C11(A) uses the memory data pins to configure an internal configuration register upon power- up/reset. CNF(2) will determine whether the WD90C11(A) will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C11(A) at power-up/reset are used as status bits, or for clock source control. For more information on WD90C11(A) power-up configuration, refer to the Configuration Bits section of this document.

4.0 SIGNAL DESCRIPTIONS

Figure 4-1 displays the WD90C11(A) pin layout. The following table provides a signal listing for the 132-pin WD90C11(A) package. The signals are grouped according to their application and described in Table 4-2.

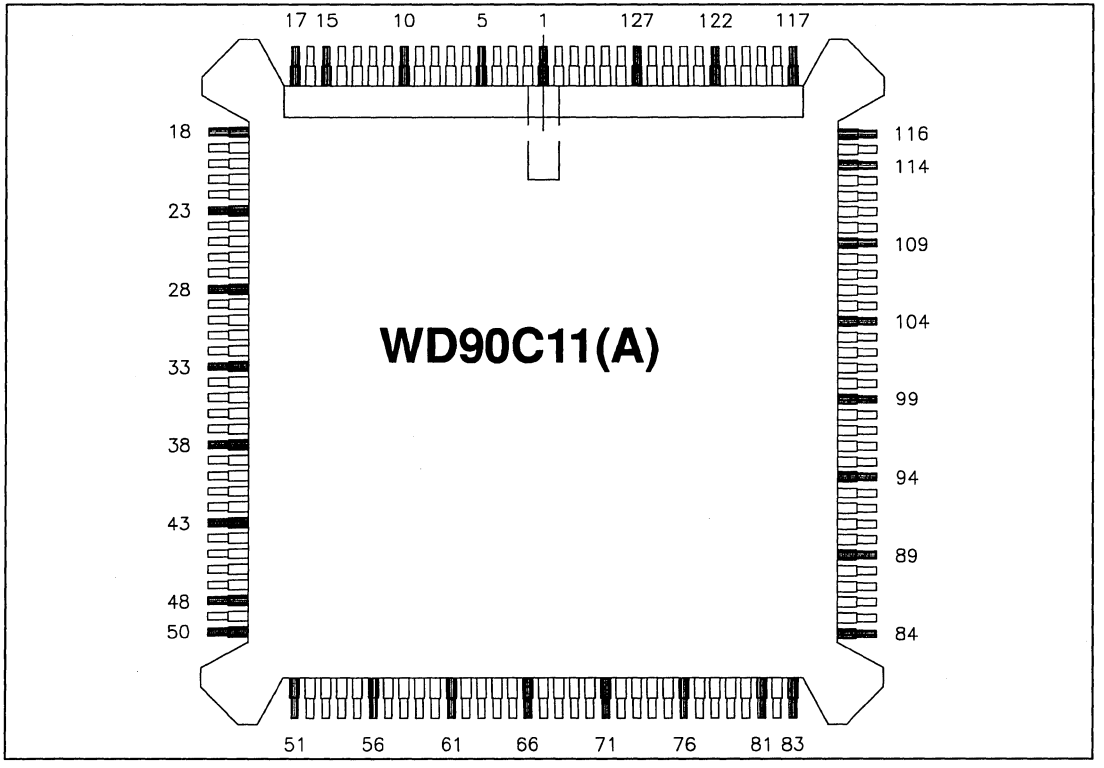

FIGURE 4-1. WD90C11(A) SIGNAL/PIN ASSIGNMENT

13

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	- A14	34	- D8	67	- MD14	100	- VID0
2	- A15	35	- D7	68	- MD13	101	- VID1
3	- A16	36	- D6	69	- MD12	102	- VID2
4	- A17	37	- D5	70	- MD11	103	- VID3
5	- A18	38	- D4	71	- MD10	104	- VID4
6	- A19	39	- D3	72	- MD9	105	- VID5
7	- A20	40	- D2	73	- MD8	106	- VID6
8	- A21	41	- D1	74	- MD7	107	- VID7
9	- A22	42	- D0	75	- MD6	108	- +5VDC
10	- A23	43	- $\overline{WE1}$	76	- MD5	109	- $\overline{EXVID}$
11	- $\overline{BHE}$	44	- GND	77	- GND	110	- GND
12	- EMEM	45	- $\overline{MRD}$ (M/$\overline{IO}$)	78	- MD4	111	- NC
13	- $\overline{EIO}$ (3C3D0)	46	- $\overline{MWR}$ ($\overline{S0}$)	79	- MD3	112	- MDET
14	- $\overline{IOCS16}$ ($\overline{CDSETUP}$)	47	- $\overline{IOR}$ ($\overline{S1}$)	80	- MA8	113	- NC
15	- GND	48	- $\overline{IOW}$ ($\overline{CMD}$)	81	- MD1	114	- NC
16	- IRQ ($\overline{IRQ}$)	49	- RSET	82	- MD0	115	- NC
17	- +5VDC	50	- +5VDC	83	- +5VDC	116	- NC
18	- $\overline{EBROM}$	51	- GND	84	- $\overline{EXPCLK}$	117	- A0
19	- DIR	52	- MA0	85	- GND	118	- A1
20	- RDY	53	- MA1	86	- USR1	119	- A2
21	- $\overline{MEMCS16}$ ($\overline{CDDS16}$)	54	- MA2	87	- USR0	120	- A3
22	- $\overline{EDBUFH}$	55	- MA3	88	- PCLK	121	- A4
23	- $\overline{EDBUFL}$	56	- MA4	89	- $\overline{BLNK}$	122	- A5
24	- $\overline{ROM16}$ ($\overline{CSFB}$)	57	- MA5	90	- VSYNC	123	- NC
25	- $\overline{HTL}$	58	- MA6	91	- HSYNC	124	- A6
26	- D15	59	- MA7	92	- $\overline{RPLT}$	125	- A7
27	- D14	60	- MA8	93	- $\overline{WPLT}$	126	- A8
28	- GND	61	- GND	94	- VCLK2	127	- A9
29	- D13	62	- $\overline{RAS}$	95	- +5VDC	128	- A10
30	- D12	63	- $\overline{CAS}$	96	- VCLK1	129	- A11
31	- D11	64	- $\overline{WE0}$	97	- VCLK0	130	- A12
32	- D10	65	- $\overline{OE}$	98	- MCLK	131	- GND
33	- D9	66	- MD15	99	- GND	132	- A13

TABLE 4-1. WD90C11(A) PIN ASSIGNMENTS

PIN	MNEMONIC	I/O	DESCRIPTION
			POWER ON
49	RSET	I	**Reset** This signal input will reset the WD90C11(A). MCLK and VCLK0 should be connected to WD90C11(A) in order for the WD90C11(A) to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
98	MCLK	I	**Memory Clock** This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
97	VCLK0	I	**Video Clock 0** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The miscellaneous output register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
96	VCLK1	I/O	**Video Clock 1** This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, bit 2). Refer to the Configuration Register and PR15 Register, bit 5 description.
94	VCLK2	I/O	**Video Clock 2** A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of bit PR2(1) (or it reflects the contents of 03C2, Miscellaneous Register, bit 3) if CNF (3) is set to 1. See the Configuration Register and PR15 Register, bit 5 description.

TABLE 4-2. SIGNAL DESCRIPTIONS

PIN	MNEMONIC	I/O	DESCRIPTION
		HOST INTERFACE	
10 - 7	A23 - A20	I	**Address Bus** (A23 - A20) These address bits should be connected to address bus SA23 - 20 in Micro Channel mode. In AT mode, if CNF(11) = 1, then A23-20 should be connected to LA23-20 of the AT address bus. If CNF(11) = 0, then A22-20 should be connected to LA19 - 17 of the AT address bus, and A23 should be connected to an externally decoded ($\overline{LA23}$ x $\overline{LA22}$ x $\overline{LA21}$ x $\overline{LA20}$) = 1 from the AT address bus. CNF(11) = 0 when MD8 is pulled down with a 4.7 Kohm resistor.
6 - 1 132 130 - 124 122 - 117	A19 - A14 A13 A12 - A6 A5 - A0	I I I I	**Address Bus** (SA19-SA0) These inputs are directly connected to the system address bus (SA19 - SA0). Latched address. A19 - A17 can be connected to LA19 - LA17 in 386 systems when CNF (11) = 1. Refer to CNF(11) definition.
26 - 27 29 - 42	D15 - D14 D13 - D0	I/O I/O	**Data Bus** (SD15 - SD0) These bidirectional signals either may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external bus buffers controlled by $\overline{EDBUFH}$, $\overline{EDBUFL}$, and DIR.
20	RDY	O	**Ready** An active high output which signals to the system processor that a memory access is completed, and is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C11(A) to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Micro Channel only.

PIN	MNEMONIC	I/O	DESCRIPTION
16	IRQ/($\overline{\text{IRQ}}$)	O	**Interrupt Request** Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt.It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. $\overline{\text{IRQ}}$ is used to generate interrupt, usually in the Micro Channel mode.
21	$\overline{\text{MEMCS16}}$ ($\overline{\text{CDDS16}}$)	O	**$\overline{\text{Memory Chip Select 16 Bits}}$** In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
13	$\overline{\text{EIO}}$ (3C3D0)	I	**$\overline{\text{Enable I/O}}$** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
18	$\overline{\text{EBROM}}$	O	**$\overline{\text{Enable BIOS ROM}}$** In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A WRITE to WD90C11 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
25	$\overline{\text{HTL}}$	O	**$\overline{\text{Enable High-to-Low}}$** (for 16-bit BIOS) If only an 8-bit CPU interface is used, this output enables a data buffer to allow reading the upper byte of ROM data on the lower data bus when 2 ROMs (16-bit) are supported.
12	EMEM	I	**Enable Memory** This signal enables memory decoding when high. It is normally connected to the signal -Refresh.

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

NOTE: ( ) Micro Channel only.

PIN	MNEMONIC	I/O	DESCRIPTION
11	$\overline{BHE}$	I	**$\overline{Byte\ High\ Enable}$** If SA0 is "0", this signal enables 16-bit data transfer mode when $\overline{BHE}$ is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]). An internal pullup is on this input.
45	$\overline{MRD}$/(M/$\overline{IO}$)	I	**$\overline{Memory\ Read}$** In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
46	$\overline{MWR}$/($\overline{S0}$)	I	**$\overline{Memory\ Write}$** The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
47	$\overline{IOR}$/($\overline{S1}$)	I	**$\overline{I/O\ Read}$** Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
48	$\overline{IOW}$/($\overline{CMD}$)	I	**$\overline{I/O\ Write}$** Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$; address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	**$\overline{I/O\ Chip\ Select\ 16\ Bits}$** In AT mode, used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, is driven by the host to individually select channel connector slots during system configuration.
19	DIR	O	**Direction Control** Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C11(A) will then drive DIR high to change the direction of the data buffers.
22	$\overline{EDBUFH}$	O	**$\overline{Enable\ Data\ Buffer\ High}$** Active low signal allows control of an external data buffer for data bits D8 - D15.
23	$\overline{EDBUFL}$	O	**$\overline{Enable\ Data\ Buffer\ Low}$** Active low signal allows control of an external data buffer for data bits D0 - D7.

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

NOTE: ( ) Micro Channel only.

PIN	MNEMONIC	I/O	DESCRIPTION
24	$\overline{\text{ROM16}}$/ ($\overline{\text{CSFB}}$)	O	**$\overline{\text{BIOS ROM Select 16 Bits}}$** This signal decodes the ROM address space C0000 - DFFFF. It may be combined with SA15 and SA16 to control $\overline{\text{MEMCS16}}$ for the address space C0000 - C7FFF. This is an active low, totem-pole output. CARD SELECT FEEDBACK: (Micro Channel mode) This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. This is an active low output.
DISPLAY MEMORY INTERFACE			
63	$\overline{\text{CAS}}$	O	**$\overline{\text{Column Address Strobe}}$** Active low CAS output signal (for both two and four DRAM configurations).
62	$\overline{\text{RAS}}$	O	**$\overline{\text{Row Address Strobe}}$** Active low RAS output signal (for both two and four DRAM configurations).
65	$\overline{\text{OE}}$	O	**$\overline{\text{Output Enable}}$** Active low DRAM output enable signal (for both two and four DRAM configurations).
64	$\overline{\text{WE0}}$	O	**$\overline{\text{Write Enable}}$** Active low write enable signal for first two DRAMs.
43	$\overline{\text{WE1}}$	O	**$\overline{\text{Write Enable}}$** Active low write enable signal for the second pair of DRAMs in a four-DRAM configuration.
PROGRAMMABLE OUTPUTS			
87	USR0	O	May be used to control special card or system features.
86	USR1	O	May be used to control special card or system features.

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

NOTE: ( ) Micro Channel only.

13

<table>
<tr><th>PIN</th><th>MNEMONIC</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td colspan="4">VIDEO MEMORY DATA</td></tr>
<tr><td>66 - 76
78 - 82</td><td>MD15 - MD5
MD4 - MD0</td><td>I/O
I/O</td><td>Display Memory Data (MD15 - 0)
These lines are the data bus to the video display DRAMS. The MD15-MD8 data lines are used with 4-DRAM configurations of the WD90C11(A). Data lines MD0-15 are pulled up by internal 50K ohm resistors or may be pulled down by external 4.7K ohm resistors to provide setup information on power-up (reset) as follows:

<table>
<tr><th>MD</th><th>POWER-UP FUNCTION</th><th>REGISTER (BIT)</th></tr>
<tr><td>15</td><td>EGA SW4</td><td>PR11(7) +</td></tr>
<tr><td>14</td><td>EGA SW3</td><td>PR11(6) +</td></tr>
<tr><td>13</td><td>EGA SW2</td><td>PR11(5) +</td></tr>
<tr><td>12</td><td>EGA SW1</td><td>PR11(4) +</td></tr>
<tr><td>11</td><td>TTL Display/General Purpose Status</td><td>CNF (8) *</td></tr>
<tr><td>10</td><td>8- or 16-bit ROMs</td><td>PR1 (1) *</td></tr>
<tr><td>9</td><td>3C3 or 46E8 I/O Port for Setup</td><td>CNF(9) +</td></tr>
<tr><td>8</td><td>A23 - 20 Connection Select</td><td>CNF(11) +</td></tr>
<tr><td>7</td><td>General Purpose</td><td>CNF(7) *</td></tr>
<tr><td>6</td><td>General Purpose</td><td>CNF(6) *</td></tr>
<tr><td>5</td><td>General Purpose</td><td>CNF(5) *</td></tr>
<tr><td>4</td><td>General Purpose</td><td>CNF(4) *</td></tr>
<tr><td>3</td><td>VCLK1,2 Input/Output</td><td>CNF(3) +</td></tr>
<tr><td>2</td><td>AT/Micro Channel Mode</td><td>CNF(2) +</td></tr>
<tr><td>1</td><td>1 or 2 ROMs</td><td>CNF(1) *</td></tr>
<tr><td>0</td><td>BIOS ROM Mapping</td><td>PR1(0) *</td></tr>
</table>

NOTES:
"*" Pulldown resistor sets these bits to logic 1.
"+" Pulldown resistor sets these bits to logic 0.
For more details refer to PR and Configuration Registers.</td></tr>
<tr><td colspan="4">VIDEO MEMORY ADDRESS</td></tr>
<tr><td>60 - 52</td><td>MA8 - MA0</td><td>O</td><td>Memory Address (MA0 - MA8)
Display memory DRAM address. For testing purposes, these pins can be tri-stated by setting PR4(4)=1.</td></tr>
</table>

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		RAMDAC INTERFACE	
107 - 100	VID7 - VID0	O	**Video** (VD0-VD7) Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
92	$\overline{\text{RPLT}}$	O	**$\overline{\text{Read Palette}}$** Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
93	$\overline{\text{WPLT}}$	O	**$\overline{\text{Write Palette}}$** Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H-3C9H.
88	PCLK	O	**Pixel Clock** Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output register.
		CRT CONTROL	
89	$\overline{\text{BLNK}}$	O	**$\overline{\text{Blank}}$** Active low display monitor blank pulse to external RAMDAC.
91	HSYNC	O	**Horizontal Sync** Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous Output Register programming.
90	VSYNC	O	**Vertical Sync** Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
112	MDET	I	**Monitor Detect** This pin is used when the RAMDAC is external. It is used to determine the monitor type and can be read at port 3C2H bit 4.
		FEATURE CONNECTOR SUPPORT	
109	$\overline{\text{EXVID}}$	I	**$\overline{\text{Enable External Video Data}}$** A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided.
84	$\overline{\text{EXPCLK}}$	I	**$\overline{\text{Enable External Pixel Clock}}$** A Feature Connector input. A low tri-states the PCLK output. An internal pullup resistor is provided.

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

13

PIN	MNEMONIC	I/O	DESCRIPTION
NO CONNECT			
123	NC		
116-113	NC		
111	NC		
POWER AND GROUND			
17	VCC	-----	+5VDC
50	VCC	-----	+5VDC
83	VCC	-----	+5VDC
95	VCC	-----	+5VDC
108	VCC	-----	+5VDC
15	GND	-----	Ground
28	GND	-----	Ground
44	GND	-----	Ground
51	GND	-----	Ground
61	GND	-----	Ground
77	GND	-----	Ground
85	GND	-----	Ground
99	GND	-----	Ground
110	GND	-----	Ground
131	GND	-----	Ground

TABLE 4-2. SIGNAL DESCRIPTIONS (Continued)

5.0 WD90C11(A) REGISTERS

All the standard IBM registers incorporated inside the WD90C11(A) are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
AT Mode Setup and Enable	W			46E8
Setup Video Enable	RW			102
* I/O Port 3C3 can be used to replace 46E8 (if CNF (9) = 0) for setup in AT mode. In Micro Channel mode, writes to 3C3, bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hex.

TABLE 5-1. VGA REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
** CNF Configuration	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad (WD90C11A only)	RW	3C5.08	3C5.08
PR23 Scratch Pad (WD90C11A only)	RW	3C5.09	3C5.09
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE: All of the PR Registers may be read/write protected. Refer to the PR Registers' description for more details.

TABLE 5-2. PR REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

TABLE 5-3. COMPATIBILITY REGISTERS SUMMARY

5.1 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

5.1.1 General Registers

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.1.1.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:
*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

5.1.1.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. MDET monitor status (pin 112) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

5.1.1.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.1.1.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0 = Vsync output enabled
1 = Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

5.1.2 Sequencer Registers

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE:
Reserved bits should be set to zero.

5.1.2.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

5.1.2.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

5.1.2.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

5.1.2.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

5.1.2.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

5.1.2.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.

0 = Processor sequentially accesses data using map mask register.

1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.

0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.

1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.

0 = 64 Kbyte of video memory.

1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0

Reserved.

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PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 5-4. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0=B in Monochrome Modes and
   1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater in the reference literature.
3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.

5.1.3 CRT Controller Registers

5.1.3.1 CRT Address Register Read/Write Port= 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

5.1.3.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

5.1.3.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total displayed characters less one are programmed in this register. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register bit 7= 1.

5.1.3.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.1.3.5 End Horizontal Blanking Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

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Bit (4:0)

End Horizontal Blanking.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

5.1.3.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.1.3.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

5.1.3.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.1.3.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12)

++ Bit 0

Vertical Total Bit 8 (index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

5.1.3.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

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5.1.3.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

5.1.3.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

5.1.3.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

Cursor End Scanline
These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

5.1.3.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

5.1.3.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

5.1.3.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

5.1.3.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

5.1.3.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

5.1.3.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

5.1.3.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

5.1.3.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

5.1.3.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

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5.1.3.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

5.1.3.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

5.1.3.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256 Kbyte of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.

0 = Selects horizontal retrace clock rate

1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter bit 1 as output at MA14 address pin.

1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.

0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.

1 = Enable memory address pin 13 to be output at MA13 address pin.

5.1.3.26 Line Compare Register
Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.1.4 Graphics Controller Registers

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

5.1.4.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.1.4.2 Set/Reset Register, Read/Write Port 3CF, Index = 00

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

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5.1.4.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

5.1.4.4 Color Compare Register, Read/Write PORT 3CF, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.

The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.1.4.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

5.1.4.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11 to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

5.1.4.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.

Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 - Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.

The table on the following page defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.1.4.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown in the following table.

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A) is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.1.4.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

5.1.4.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.2 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:

1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as follows:

   0 = B in Monochrome Modes and
   1 = D in Color Modes

5.2.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).

1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:

The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

5.2.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:

0 = Current pixel color deselected.

1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

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5.2.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

5.2.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

5.2.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

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5.2.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

5.2.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

5.3 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.
3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

0 = B in Monochrome Modes
1 = D in Color Modes

5.3.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

5.3.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its bits 0 and 1. The associated details are shown below.

5.3.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6:2,0)

Not Applicable.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

5.3.4 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.3.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

5.3.6 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

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Bit 2

Red Border/Background
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

5.3.7 CRT Status Register MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrac e mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

5.3.8 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

5.3.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

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Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

5.4 PR REGISTERS

The WD90C11(A) has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C11/A architecture is optimized with additional I/O registers. The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte)–3CF (Data Port).

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

5.4.1 Address Offset Registers PR0A & PR0B

PR0A - Address Offset Register A
Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B
Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C11 can control up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C11 has two CPU address offset registers PR0A and PR0B which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PR0A (bit 6:0) or PR0B (bit 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PR0A and PR0B will then provide 4 Kbyte segmentation of the display memory. (Increment PR0A or PR0B by one of its equivalents to jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)

PR0A and PR0B are all set to zero value at power on reset. There are two ways to control whether PR0A or PR0B get added into CPU address.

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- **Sequencer Extension Register 3C5 (Index 11) bit 7 = 0.**

PR0A is the primary offset register being added with the CPU address. PR1, bit 3 enables PR0B which becomes the secondary offset register. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 00b, A000:0 for 128K, then PR0A will offset the CPU address from B000:0H to BFFF:FH while PR0B offsets the CPU address from A000:0H to AFFF:FH. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 01(A000:0H for 64K), then PROA will offset the CPU address from A800:0H to AFFF:FH while PR0B offsets the CPU address from A000:0H - A7FF:FH.

- **Sequencer Extension Register 3C5 (Index 11) bit 7 = 1.**

Both PR0A and PR0B are enabled. A CPU memory write will select PR0B as the offset register. Otherwise, PR0A is selected as the offset register.

5.4.2 PR1 - Memory Size, Read/Write Port = 3CF, Index = 0B

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Reserved
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	ROM Data Width
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16 (1) select the way memory is mapped into the CPU address space. IF PR16 (1) is set to 1, the memory mapping will be set identical to the IBM VGA regardless of PR1 (7), PR1 (6).

The WD90C11(A) supports 512 Kbytes (four 256K by 4 DRAM) display memory. This makes it possible to support some extended graphics modes such as 640 by 480 by 256 colors and 800 by 600 by 256 colors.

The setting of these two bits will be overwritten by PR16 (1). When PR16(1) is set to 1, memory mapping will be identical to the IBM VGA (equivalent to PR1 (7,6) = 00).

The following tables list the different settings on these two bits for different memory organizations.

GRAPHICS MODE RAM ADDRESSING:

PR1(7) **PR1(6)**
0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(2)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C11(A) MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) **PR1(6)**
1 1 RESERVED

PR1(7) **PR1(6)**
1 0 512K TOTAL IN FOUR PLANES; 128K/PLANE; WD90C11(A) MEMORY ORGANIZATION (EACH PLANE HAS TWO BANKS OF 64 KBYTES)

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
MA (15)	A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)
MA0	A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)

NOTES:

1. A(19:0) are WD90C11(A) internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(2) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(2) if CRTC Mode Register 17 bit 5 = 0.
5. For two 256K by 4 DRAMs, MA(1) and MA(0) are used as memory plane select for 256 Kbytes. For four 256K by 4 DRAMs, MA(1) is the plane select, MA(0) selects one of two 64 Kbytes within a 128 Kbyte plane.

Bits 5, 4

Reserved

Bit 3

Enable Alternate Address Offset Register PR0B

Bit 2

Enable 16 bit bus for Video Memory
When set to 1, $\overline{\text{MEMCS16}}$ will be active low for all of the video memory cycles.

Bit 1

When set to 1 and bit 0=0, the BIOS ROM has a 16 bit data path from C000:0 - DFFF:FH ($\overline{\text{ROM16}}$ will respond to ROM access). Otherwise, the BIOS ROM has an 8 bit data path.

A pull down resistor on MD(10) will set this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write to PR1 register if the CNF(1) = 1 (2 ROMs).

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

5.4.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0C

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0= VGA or EGA mode
1= Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character text mode only)
1	0	6 dots (for text modes only)
1	1	6 dots (for text modes only)

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

5.4.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0D

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

5.4.5 WD90C11 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). 11 When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9

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CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

5.4.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control.
This register should only be used with 4 DRAMs to configure the video shift register for extended 256 color modes.

5.4.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0F

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

BIT	FUNCTION
7	CNF(7) [READ ONLY]
6	CNF(6) [READ ONLY]
5	CNF(5) [READ ONLY]
4	CNF(4) [READ ONLY]
3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

5.4.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10 through PR17. Bits 7 and 3 enable register read operation for PR10 through PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test

5.4.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

5.4.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

5.4.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.4.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

5.4.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Reserved
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Reserved.

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 of 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0= BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

5.4.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2f

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64 Kbyte or 128 Kbyte locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512 Kbyte or 1024 Kbyte of video memory in which CRT controller is limited to only 64 Kbyte or 128 Kbyte locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 Kbyte locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256 Kbyte
0	1	128 Kbyte
1	X	64 Kbyte

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64 Kbyte boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H)
Programming this bit to 1 causes output WPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C11(A) is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

5.4.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

BIT	FUNCTION
7 - 4	Reserved
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bit (7:4)

Reserved.

Bit (3)

Map out 4K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C6FF:FH. Power on reset sets this bit to 0.

Bit (2)

Enable 64K BIOS ROM.
Setting this bit to 1 enables access of the BIOS ROM in the system address range C000:0H - CFFF:FH. Power on reset sets this bit to 0.

Bit (1)

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BF). Power on reset sets this bit to 0.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 0.

5.4.16 PR20 3C5 Index 6: Unlock Sequencer Extended Registers (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer index reads as a full eight bits.

5.4.17 PR21 3C5 Index 7: Display Configuration Status and Scratch Pad Bits

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7 - 4	Scratch Pad Bits
3	Status of 3C2 bit 0
2	Status of PR2 bit 6
1	Status of PR4 bit 1
0	Status of PR5 bit 3

Bits 7:4

Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.
A 1 means CGA (3Dx) addresses have been selected by this read-only bit, while a 0 means MDA (3Bx) addresses have been selected.

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).
A 1 means 6845 compatibility has been selected by this read-only bit, while a 0 means VGA or EGA compatibility has been selected.

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).
A 1 means EGA compatibility has been selected by this read-only bit, while a 0 means VGA was selected.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).
The video BIOS may define this as a 0 meaning an an analog monitor was selected by this read-only bit, while a 1 means a TTL-type monitor was selected.

5.4.18 PR22 Scratch Pad Register Read/Write Port = 3C5, Index = 8H

Bits (7:0)

Scratch Pad Bits

5.4.19 PR23 Scratch Pad Register Read/Write Port = 3C5, Index = 9H

Bits (7:0)

Scratch Pad Bits

5.4.20 PR30 3C5 Index 10 Memory Interface and FIFO Control Register

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7, 6	Reserved
5	8- or 16-bit Memory data path
4	Disable 16-bit CPU interface
3	Enable write buffer extension
2	4 or 8 level FIFO
1, 0	Display memory bandwidth

Bits (7,6)

Reserved

Bit 5

When set to 1, the display memory data path becomes 16-bits wide. Otherwise, the data path is 8-bits wide. The WD90C11(A) can support 8/16-bits memory data path with four 256 Kbyte by 4 DRAMs installed.

Bit 4

When set to 1, the 16-bit CPU interface is unchained mode is disabled. This is for debug only and should be set to 0 under normal conditions.

Bit 3

When set to 1 enables the write buffer extension. This will make the write buffer effectively two deep. Should be set to 1 under normal conditions.

Bit 2

When set to 1, will set the internal FIFO to 4 levels deep. Otherwise the FIFO is 8 levels deep. In general, when 16-bits display memory is enabled (bit 1 of this register is set to 1), then the 4 level deep FIFO is recommended. In "Super VGA" mode (800 by 600 by 256 color) an 8 level deep FIFO will be required.

Bit 1, 0

These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

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5.4.21 PR31 3C5 Index 11: System Interface Control (Reset State = 00H)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Operation on Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

When set to 1, the offset register PR0-A will be added to the CPU address for read cycles, while PR0-B will be added for write cycles. When cleared to 0, the offset registers operate the same as in the PVGA1B. Refer to PR0A and PR0B definitions.

Bit 6

When set to 1, system performance is improved by 10% by removing extra memory cycles on blank lines.

Bit 5

When set to 1, text mode performance will be improved.

Bit 4:3

These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it will take longer for the read cycle to be completed.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle

01, 10 = RDY is inserted 1MCK before the end of a CPU memory cycle.

11 = RDY is inserted 1MCK after the end of a CPU read memory cycle. RDY is inserted at the end of a memory write cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2

When set to 1, a single-level , 16-bit write buffer is enabled. This willl greatly reduce the number of wait states for CPU writes to display memory.

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. $\overline{\text{IOCS16}}$ is asserted for all cycles to 3C0 or 3C1.

Bit 0

When set to 1, this bit enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output $\overline{\text{IOCS16}}$ will be active for any I/O read or write to these addresses. When set at 0, the VGA I/O is all 8-bit.

5.4.22 PR32 3C5 Index 12: Miscellaneous Control 4 (Reset State = 00H)

This register provides control for several different features. Some of these features help to support Genlock of the PVGA1M to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

Bit 7

When set to 1, $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync, and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external HSYNC signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID7:0 and PCLK output buffers. A 0 setting places this bit into its normal operation mode.

Bit 6

When set to 1, the text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

A 1 setting causes the USR1 output to indicate when the WD90C11 is reading font data in text mode (FONTCYC). A 0 causes the USR1 output to reflect the state of bit 4, which can be used to control new features that the system board designer may wish to add.

Bit 4

Controls the USR1 output when selected by bit 5.

Bit 3

A 1 setting causes the USR0 output to indicate that the WD90C11 is reading both the character and the attribute data from the DRAMs in text mode (TEXTCYC). USR0 will be high during the RAS cycles for character/attribute read. The DRAM data may be sampled when USR0 is high. A 0 setting causes the USR0 output to reflect the state of bit 2, which can be used to control new features that the system board designer may wish to add.

Bit 2

Controls the USR0 output when selected by bit 3.

Bit 1

When set to 1, this bit allows reading the registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

When set to 1, the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

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REGISTERS	EGA	I/O PORT
GENERAL REGISTERS		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
SEQUENCER REGISTERS		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT CONTROLLER REGISTERS		
Index Reg	WO	3?4
CRT CONTROLLER DATA REGISTERS		
Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
GRAPHICS CONTROLLER REGISTERS		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
ATTRIBUTE CONTROLLER REGISTERS		
Index Reg	WO	3CO*
Attribute Controller Data Reg	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

TABLE 5-5. EGA REGISTERS SUMMARY

5.5 EGA REGISTERS

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
2. Unlock all the PR registers.
3. Program PR2(6) to 0 for EGA mode.
4. Set PR4 bit 1 to logic 1 for EGA compatibility.
5. Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:
   Initialize all the registers.
   Lock CRT controller registers.
   Force Clock Control rate of the CRT controller.
8. Set EGA emulation mode by programming:
   PR11(3)=1; Set EGA emulation on PS/2 type display
   PR14(6)=1; Vertical double scan
   PR11(2)=1; Lock clock select
   PR11(0)=1; Lock 8/9 dot timing.
   PR14(7)=1; Enable IRQ (optional)
9. Lock the PR registers PRO-PR5 and PR10-PR17.
10. Read protect PR registers.

When EGA is required on a TTL monitor, the suggested steps are:

1. Initialize all the registers.
2. Set EGA TTL mode by programming:
   PR11(3)=0;EGA TTL
   PR14(7)=1;Enable IRQ
   PR15(6)=1;Set Low Clock
   PR14(7)=1;Enable IRQ
3. Lock PR registers PRO-PR5 and PR10-PR17
4. Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

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5.5.1 General Registers

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

5.5.1.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

5.5.1.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

5.5.1.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

5.5.1.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not used

5.5.2 Sequencer Registers (Port 3C5)

5.5.2.1 Clocking Mode Register (Index = 01)

Bits (7:4)

EGA: Not Used

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to zero

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

5.5.2.2 Character Map Select Register (Index 03)

Bits (7:4)

EGA: Not Used

Bits (3:2)

EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)

EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:

1. Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

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5.5.2.3 Memory Mode Register (Index = 04)

Bits (7:3)

EGA: Not Used

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

5.5.3 CRT Controller Registers (Port 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

5.5.3.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

5.5.3.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

5.5.3.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

5.5.3.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

5.5.3.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

5.5.3.6 CRT Controller Overflow Register (Index = 07)

Bits (7:5)

EGA: Not used.

Bits (4:0)

Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

5.5.3.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definition in the VGA section.

5.5.3.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

5.5.3.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

5.5.3.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

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5.5.3.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

5.5.3.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

5.5.3.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

5.5.3.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

5.5.3.15 Mode Control Register (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

5.5.4 Graphics Controller Registers (Port 3CF)

5.5.4.1 Read Map Select Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

5.5.4.2 Mode Register (Index = 05)

Bit (7:6)

EGA: Not Used

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

5.5.5 Attribute Controller Registers (Ports = 3C0/3C1)

5.5.5.1 Palette Registers (Index = 00 through 0F)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Dynamic color selection

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

5.5.5.2 Mode Control Register (Index = 10)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

5.5.5.3 Overscan Color Register (Index = 11)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Overscan color for border

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

5.5.5.4 Color Plane Enable Register (Index = 12)

BIT	FUNCTION
7 - 6	Same as Color Plane Enable - VGA
5 - 4	Video Status Multiplexer
3 - 0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

5.3.5.5 Horizontal PEL Panning Register (Index = 13)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

5.6 INTERNAL I/O PORTS

5.6.1 AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C11(A) into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C11(A) also provides an alternative port 3C3H instead of port 46E8H. If a pull down resistor is connected to MD(9) during power on reset (CNF9 = 0), then port 3C3H will be decoded instead of port 46E8H to support the same functions described above. Otherwise, port 46E8H is selected and decoded.

5.6.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C11(A) must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C11(A) after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP (EION) signal pin is active low, the WD90C11(A) is in setup mode and port 102H can be accessed.

5.7 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C11(A). However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C11(A). Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* This port is internal to the WD90C11(A).

5.8 CONFIGURATION BITS

Memory Data lines 15:0 are used to input configuration data at power-on reset (RST) by pullup or pulldown resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on.

BIT	FUNCTION
15 - 12	EGA Switches
11	A23 - A20 Connection Select
10	16-bit BIOS
9	46E8/3C3 Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select
1	ROM Configuration
0	Map out BIOS

5.8.1 WD90C11 Configuration Register Bits CNF(15:0)

CNF(15:12)

EGA CONFIGURATION SWITCHES SW4-SW1. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. PULLING DOWN MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as bit 4 of port 3C2H (as on a standard EGA) if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of which bit is read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE		READ
3c2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF (11) (Refer to Figure 12)

A 4.7K pull down resistor on the pin MD 8 will set CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C11/A to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).
If there is no pull down resistor on MD8, the CNF(11) will be set to 1 by the internal pull up. Pins A(23:17) should be connected to AT bus signals LA(23:17). In most 80286 systems, the early address LA(23:17) is not latched during a bus operation. CNF(11) = 0 is required to ensure proper decoding of $\overline{\text{MEMCS16}}$ without many external components. In most 80386 systems, the early address LA(23:17) is latched during a bus operation. CNF(11) = 1 is recommended for design simplification. In Micro Channel applications, CNF(11) should be set to 1.

CNF (10)

A 4.7K pull down on pin MD10 will set CNF(10) = PR1(1). Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding. Otherwise the internal pull up will set CNF(10) = PR1=0. To enable the 16-bit BIOS, PR1 must be set to 1 by writing to port 3CF (index 0B) and the CNF (1) must be 1. This bit is read/write at PR1(1).

CNF (9)

A 4.7K pull down on pin MD9 will set CNF(9) = 0. Then port 03C3 will be selected as the VGA setup and enable register instead of port 46E8 in the AT interface. Otherwise, the internal pull up will set CNF(9) = 1. Port 46E8 will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

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CNF (8)

TTL DISPLAY STATUS BIT/GENERAL PURPOSE STATUS BIT.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). In designs with TTL display, CNF(8) must be set to 1, as shown in Figure A-8. In designs with analog displays, CNF(8) can be used as a general purpose status bit. Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched high.

CNF (3)

VIDEO CLOCK SOURCE CONTROL.
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C11(A) pins VCLK1 and VCLK2 as inputs or outputs.

0 = For inputs.
1 = For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

BUS ARCHITECTURE SELECT.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0 = Micro Channel architecture
1 = AT BUS architecture

Select CNF(2) will change PINOUT definition between AT BUS and Micro Channel bus (see PINOUT description).

PC-AT BUS	I/O	Micro Channel	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	CMD	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF (1)

ROM CONFIGURATION.
When set to 0, the WD90C11(A)'s data bus buffer controls are configured for 1 ROM (8 bits). An internal pullup on MD (1) sets this bit to 0 at power-on reset.
When set to 1, the WD90C11(A)'s data bus buffer controls are configured for 16-bits (as with two ROMs).
If CNF (1) = 0, then PR1(1) can not be set high. This bit can not be written or read.

CNF (0)

BIOS ROM MAPPING.
If set to 1, the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 K ohm pulldown resistor may be used to set this bit to 1 on power-on (reset).
This bit is read/write at PR1(0).

6.0 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz
C(I/O)	I/O Pin Capacitance	--	12	pF	FC=1 MHz

TABLE 6-1. DC CHARACTERISTICS

NOTE:
The WD90C11/A outputs have 4.0 mA maximum source and sink capability except as follows:

IRQ, RDY= 4.0 mA source and 24.0 mA sink.
$\overline{\text{MEMCS16}}$, $\overline{\text{IOCS16}}$ = 20 mA sink.
D15:0, PCLK, VID7:0, $\overline{\text{ROM16}}$ = 8.0 mA source/sink.

6.1 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

6.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts
Power Dissipation	130 mA (WD90C11) 110 mA (WD90C11A)

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7.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

All units are in nanoseconds
C_L = 30 pF unless otherwise noted

		WD90C11		WD90C11A		
NO.	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**NOTES**
	RESET TIMING					
1	Reset Pulse Width	6t		6t		t = 1/MCLK
2	MD Setup to RSET low	20		20		
3	MD Hold from RSET low	30		30		
4	RSET low to first $\overline{IOW}$	3t		3t		
	CLOCK TIMING					
1	VCLK Period	15.3		15.3		
2	VCLK high	6		5		@1.4V
3	VCLK low	6		5		@1.4V
4*	Clock Rise Time		3		3	0.8V - 2.0V
5*	Clock Fall Time		3		3	0.8V - 2.0V
6	VCLK to PCLK Delay	4	12	4	12	45 ns @ 120 pF load up to
7a	VCLK to Hsync Delay	4	18	4	18	30MHz
7b	VCLK to $\overline{Vsync}$ Delay	4	12	4	12	
7c	VCLK to $\overline{BLNK}$ Delay	4	12	4	12	
7d	VCLK to VID(7:0) Delay	4	12	4	12	45 ns @ 120 pF load up to 30 MHz
8	MCLK period	23.8	27	22.2	27	Maximum skew between
9	MCLK high	9.5		8.9		PCLK and VID (7:0) is ± 10
10	MCLK low	9.5		8.9		ns.
11	VID (7:0) setup to PCLK	3		3		@ 1.4V
12	VID (7:0) hold from PCLK	3		3		@ 1.4V

NOTE: * Apply to both VCLK and MCLK.

TABLE 7-1. AC TIMING CHARACTERISTICS

		WD90C11		WD90C11A		
NO.	PARAMETER	MIN	MAX	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING					
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	8		8		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	10		10		
3a	A(23:0) setup to $\overline{MRD}$,$\overline{MWR}$ low	22		15		
3b	A(15:0) setup to $\overline{IOR}$,$\overline{IOW}$ low	10		8		
3c	$\overline{BHE}$ setup to $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	10		5		
4a	A(23:0) hold from $\overline{MRD}$, $\overline{MWR}$ low	8		5		
4b	A(15:0) hold from $\overline{IOR}$, $\overline{IOW}$ low	8		5		
4c	$\overline{BHE}$ hold from $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	8		5		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	10		10		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	10		10		
7	EDBUFxN low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low		22		22	
8	EDBUFxN high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ high		22		22	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		18		18	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		18		18	
11	D(15:0) write data setup to $\overline{IOW}$ & $\overline{MWR}$ high	10		8		
12a	D(15:0) read data hold from $\overline{IOR}$ high		18		18	
12b	D(15:0) read data hold from $\overline{MRD}$ high		18		18	
12c	D(15:0) write data hold from $\overline{IOW}$ high	8		5		
12d	D(15:0) write data hold from $\overline{MWR}$ high	10		8		
13a	D(15:0) read data valid from $\overline{IOR}$ low		90		90	C_L = 70 pF
13b	D(15:0) write data valid after $\overline{MWR}$ low		2t		3t	t= 1/MCLK
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	10	2.45 µs	
15*	Memory read data valid from RDY high		40		40	C_L = 70 pF C_L = 100 pF
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	8	18	6	15	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	18	6	15	
18	$\overline{EBROM}$ low from valid A(23:15)		25		15	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		25		15	

TABLE 7-1. AC TIMING CHARACTERISTICS (Continued)

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		WD90C11		WD90C11A		
NO.	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**NOTES**
	I/O AND MEMORY READ/WRITE AT MODE TIMING					
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		15		10	
20b	$\overline{RPLT}$ low from $\overline{IOR}$ low		26		18	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high		17		17	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high		17		17	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		61		55	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		20		10	
24	VCLK1 low from $\overline{IOW}$ low (3C2 port)		46		46	
25	VCLK1 high from $\overline{IOW}$ high (3C2 port)		39		39	
26	A(15:0) valid to $\overline{IOCS16}$ low		25		25	C_L = 100 pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		49		45	C_L = 100 pF
28	A(23:17) valid to $\overline{MEMCS16}$ low		40		40	C_L = 100 pF
29	$\overline{MEMCS16}$ hold after valid A(23:17)		20		15	C_L = 100 pF
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING					
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	8		5		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	8		5		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	8		5		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	8		5		
5	STATUS setup to $\overline{CMD}$ low	8		5		
6	STATUS hold from $\overline{CMD}$ low	8		5		
7	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low		22		18	
8	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high		22		18	
9	DIR active from $\overline{CMD}$ low		18		18	
10	DIR inactive from $\overline{CMD}$ high		18		18	
11	CSFB delay from valid address/status		25		25	CL = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		22		18	CL = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		25		25	CL = 100 pF
14	$\overline{CDDS16}$ delay from valid address		30		22	
15	$\overline{CDDS16}$ hold from invalid address		25		18	
16	D(15:0) I/O write data setup to $\overline{CMD}$ high		36		36	
17a	D(15:0) I/O Write data hold after CMD high	8		5		
17b	D(15:0) Memory Write data hold after $\overline{CMD}$ high	0		0		
17c	D(15:0) I/O Read data hold from $\overline{CMD}$ high	5	15	5	15	CL = 70 pF
17d	D(15:0) Memory Read data hold from $\overline{CMD}$ high	5	15	5	15	CL = 100 pF CL = 70 pF

TABLE 7-1. AC TIMING CHARACTERISTICS (Continued)

		WD90C11		WD90C11A		
NO.	PARAMETER	MIN	MAX	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING					
18a	D(15:0) Memory Write data valid after $\overline{CMD}$ low		50		50	
18b	D(15:0) I/O Read data valid from $\overline{CMD}$ low		90		90	CL = 70 pF
19	RDY high delay from $\overline{CMD}$ low	0	2.45µs	0	2.45µs	
20*	D(15:0) Memory Read Data valid from RDY high		40		40	C_L = 70 pF
21	$\overline{CMD}$ high (inactive)	2t+15		2t+15		
22	RDY low delay from valid address/status	9	18	6	12	
23	$\overline{EBROM}$ low from valid address		25		18	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		25		18	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low		26		18	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high		17		17	
27	VCLK1 low from $\overline{CMD}$ low (3C2 port)		46		46	
28	VCLK1 high from $\overline{CMD}$ high (3C2 port)		39		39	

* Depends on setting of 3C5, Index 11, bit 4, 3.

0	0	max 40 ns
0	1	max 40 ns + 1t
1	0	max 40 ns + 1t
1	1	max 40 ns - 1t

TABLE 7-1. AC TIMING CHARACTERISTICS (Continued)

13

		WD90C11		WD90C11A		
NO.	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**NOTES**
	DRAM TIMING					
1	$\overline{RAS}$ cycle time	6t	See Note	6t	See Note	
2	$\overline{RAS}$ pulse width low	3.5t-6	See Note	3.5t-6	See Note	
3	$\overline{RAS}$ high time (precharge)	2.5t+6		2.5t+6		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	2.5t-9	2.5t -6	2.5t-9	2.5t -6	
5	$\overline{CAS}$ cycle time	2t		2t		
6	$\overline{CAS}$ pulse width low	1t		1t		
7	$\overline{CAS}$ high time (precharge)	1t		1t		
8	Row address setup to $\overline{RAS}$ low	1.5t-10		1.5t-10		
9	Row address hold time from $\overline{RAS}$ low	1t-6		1t-6		
10	Column address setup to $\overline{CAS}$ low	1t-10		1t-10		
11	Column address hold from $\overline{CAS}$ low	1t		1t		
12	Read Data valid before $\overline{CAS}$ high	2		2		
13	Read data hold after $\overline{CAS}$ high	0		0		
14	Write Data setup to $\overline{CAS}$ low	1t-21		1t-21		
15	Write Data hold after $\overline{CAS}$ low	1t-5		1t-5		
16	$\overline{WE0}$ low setup $\overline{CAS}$ low	1t-5	1t+5	1t-5	1t+5	
17	$\overline{WE0}$ low hold after $\overline{CAS}$ high	0		0		
18	$\overline{OE}$ high before $\overline{WE0}$ low	2t-5	2t+5	2t-5	2t+5	
19	$\overline{OE}$ low after $\overline{WE0}$ high	1t-5	1t+5	1t-5	1t+5	

MCLK edge to $\overline{RAS}$,$\overline{CAS}$, MA(8:0) edgedelay may be up to 40 ns

NOTES:
Page-mode CRT reads may be 4-32 $\overline{CAS}$ cycles.
CPU writes use 1-4 $\overline{CAS}$ cycles in Page-mode.
CPU reads use 4 $\overline{CAS}$ cycles in Page-mode.

t = 1/MCLK
It is recommended that MCLK = 37.5 MHz for 80 ns DRAM with longer RAS precharge. MCLK = 40 MHz for 80 ns DRAM with shorter RAS precharge. This can be accomplished with selected DRAMs.

TABLE 7-1. AC TIMING CHARACTERISTICS (Continued)

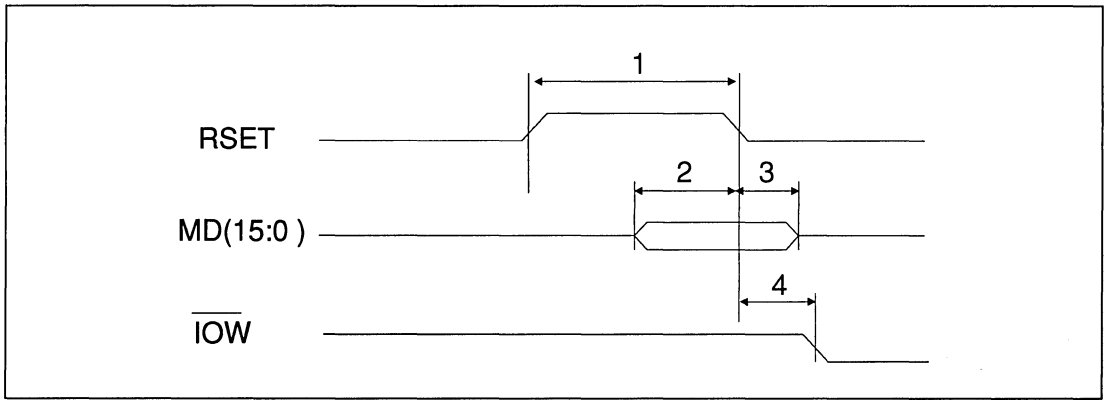

FIGURE 7-1. RESET TIMING

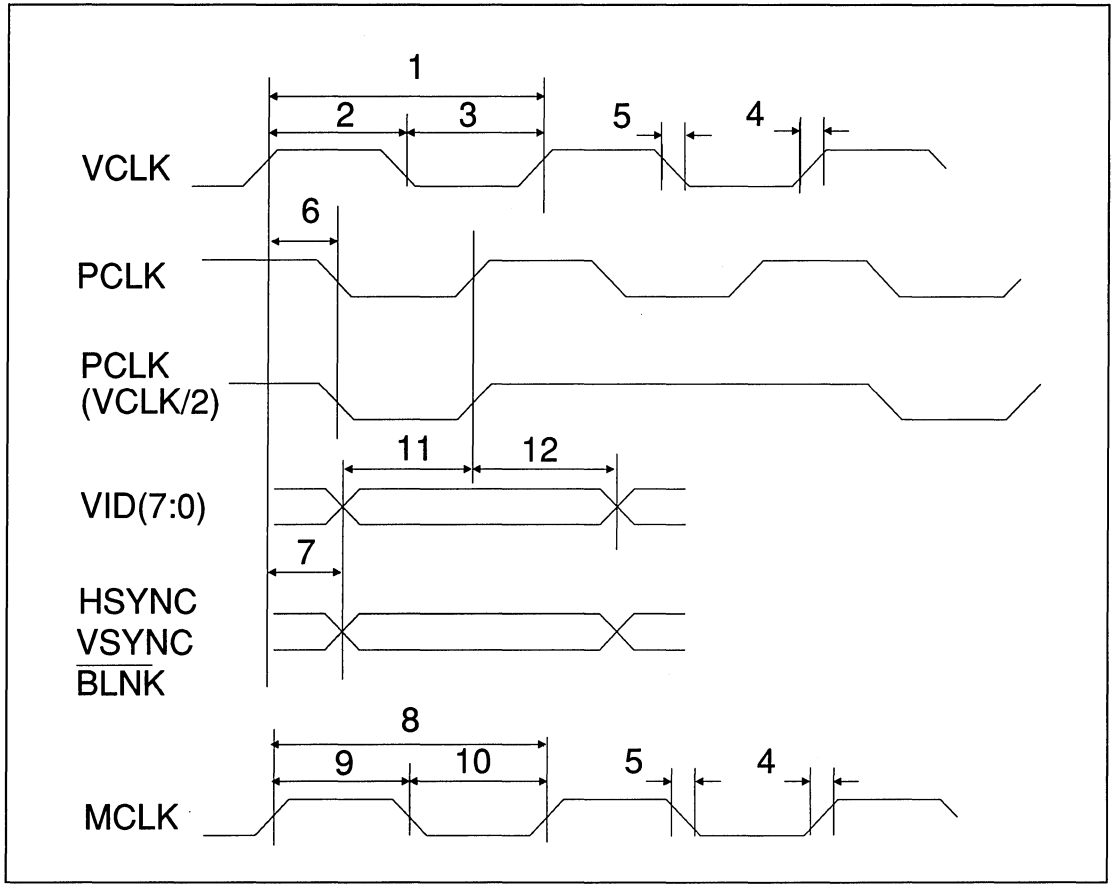

FIGURE 7-2. CLOCK AND VIDEO TIMING

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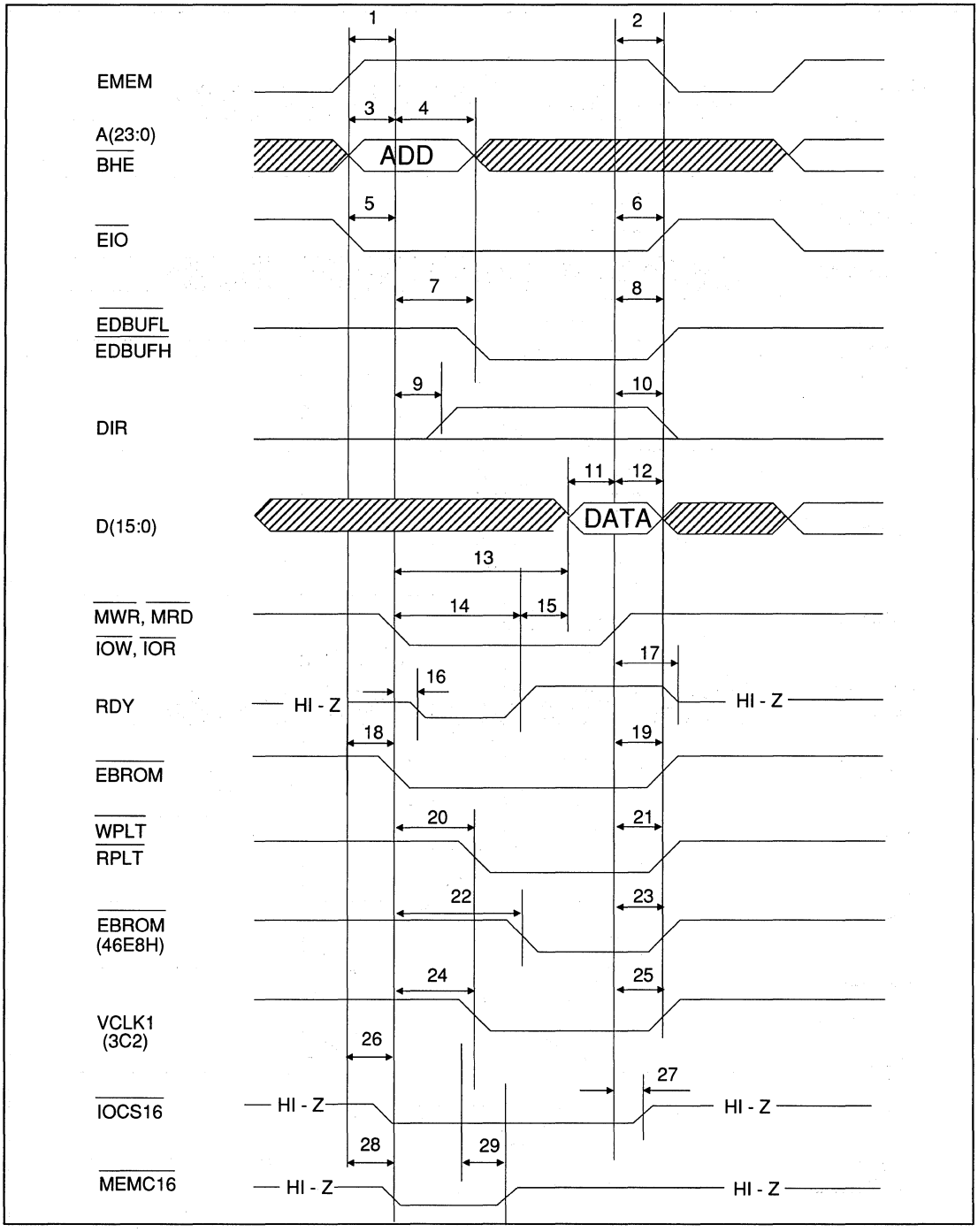

FIGURE 7-3. AT MODE BUS TIMING

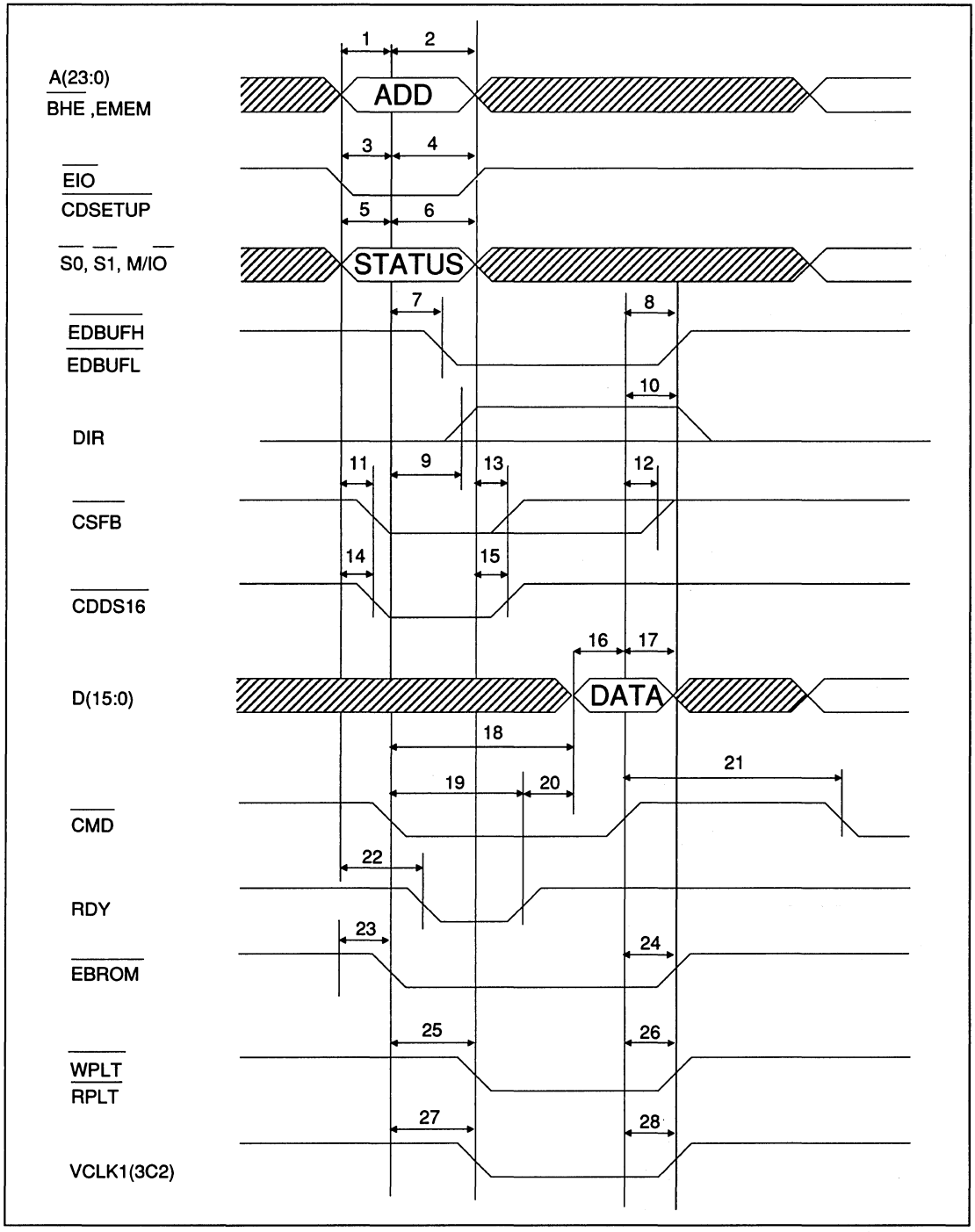

FIGURE 7-4. MICRO CHANNEL MODE BUS TIMING

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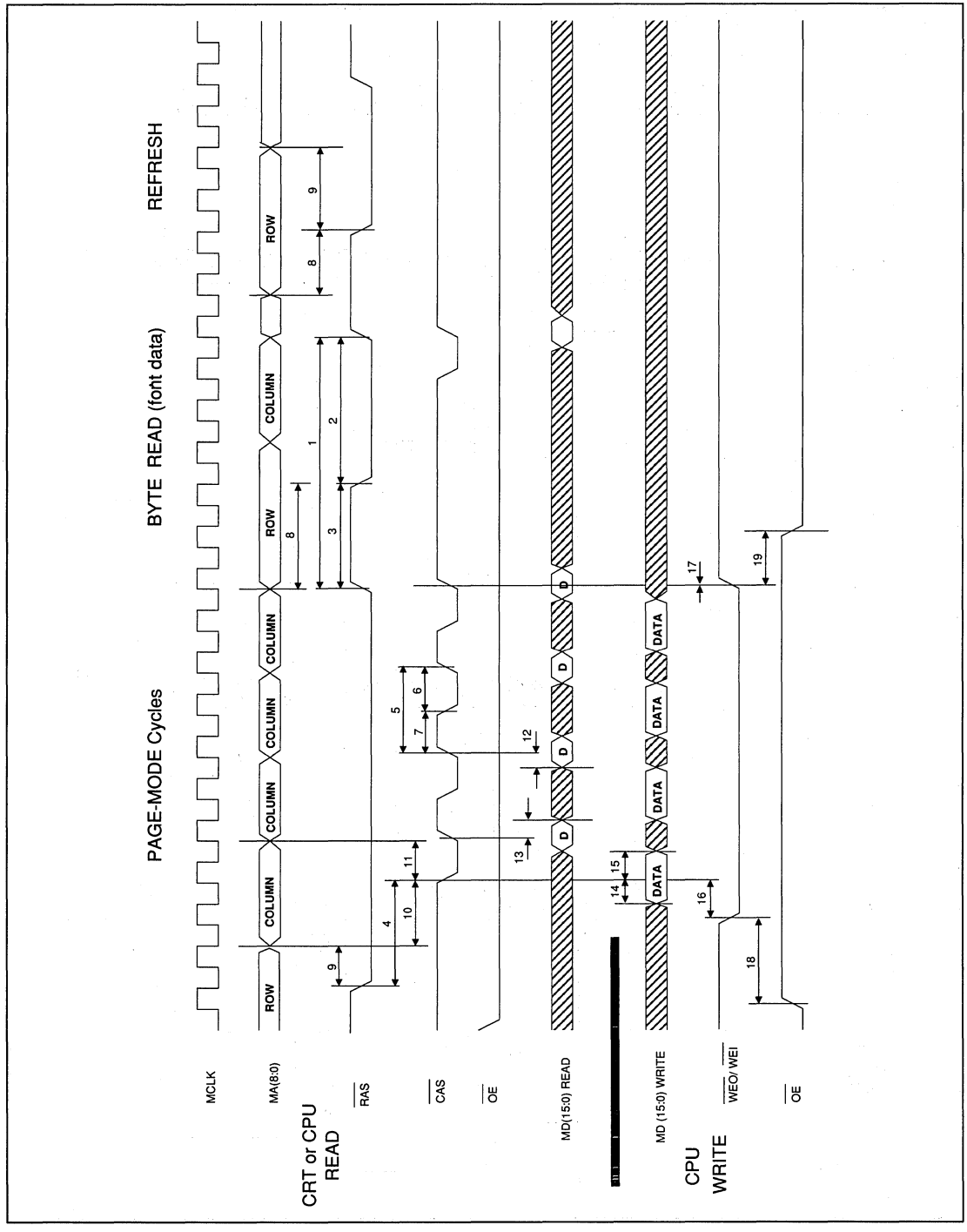

FIGURE 7-5. DRAM TIMING

8.0 PACKAGE DIMENSIONS

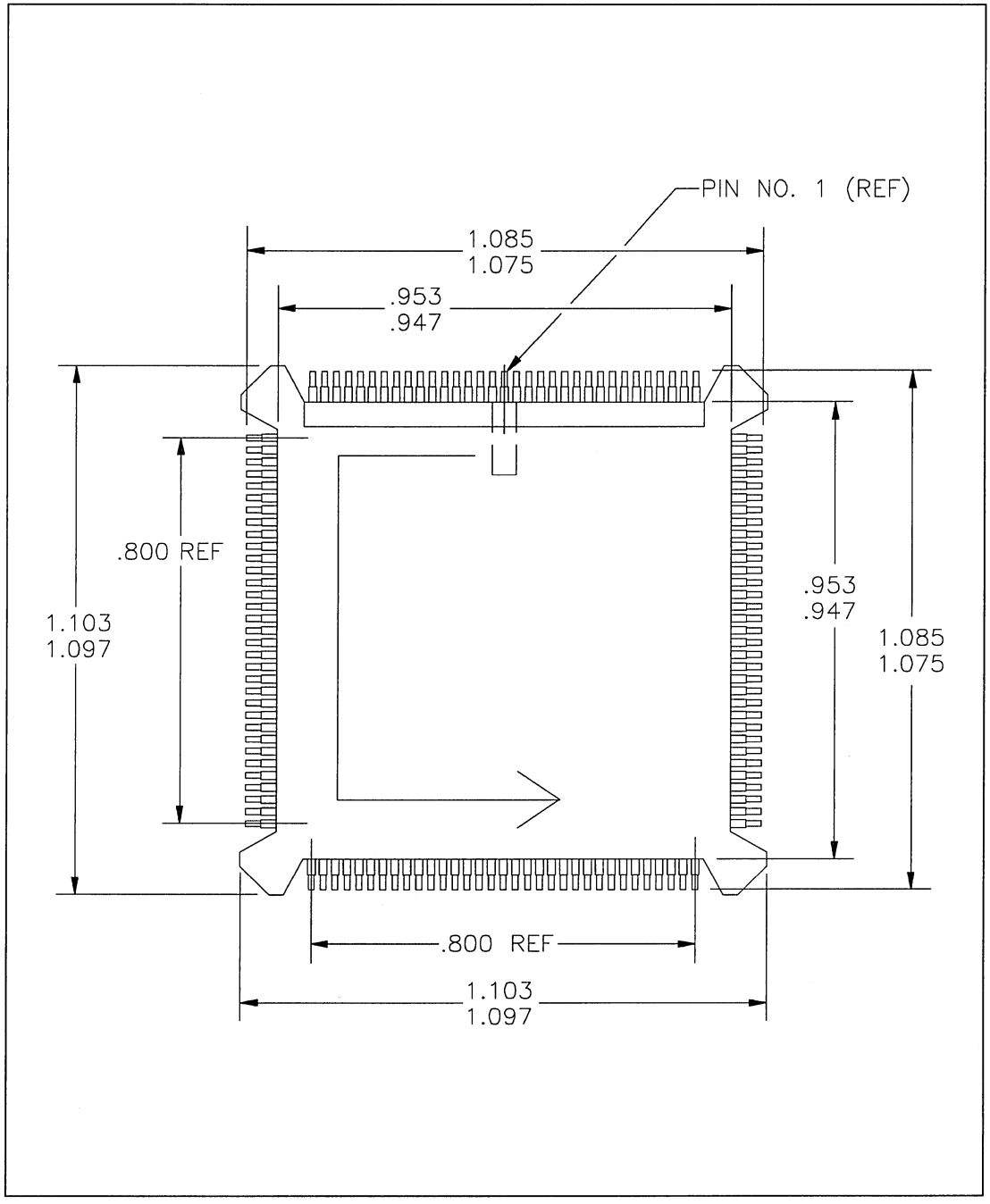

FIGURE 8-1. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP)

13

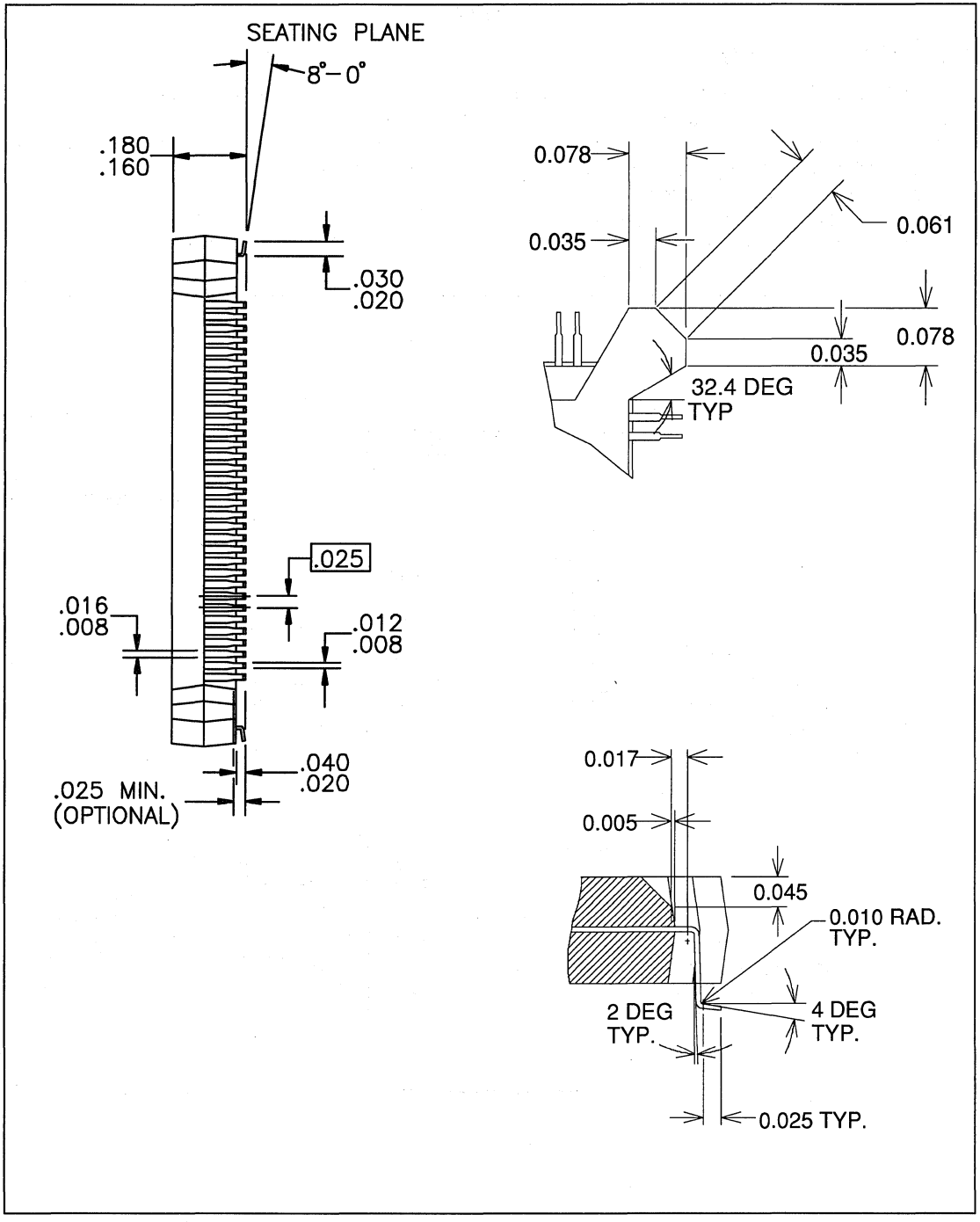

FIGURE 8-2. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP)

APPENDIX A

A.0 APPLICATIONS

The WD90C11(A) applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data book should supplement the information provided in this section. The Figures A-1 through A-9 are shown along with their brief description on the subsequent pages.

Figure A-1 highlights the various WD90C11(A) Processor, memory, and I/0 interfaces.

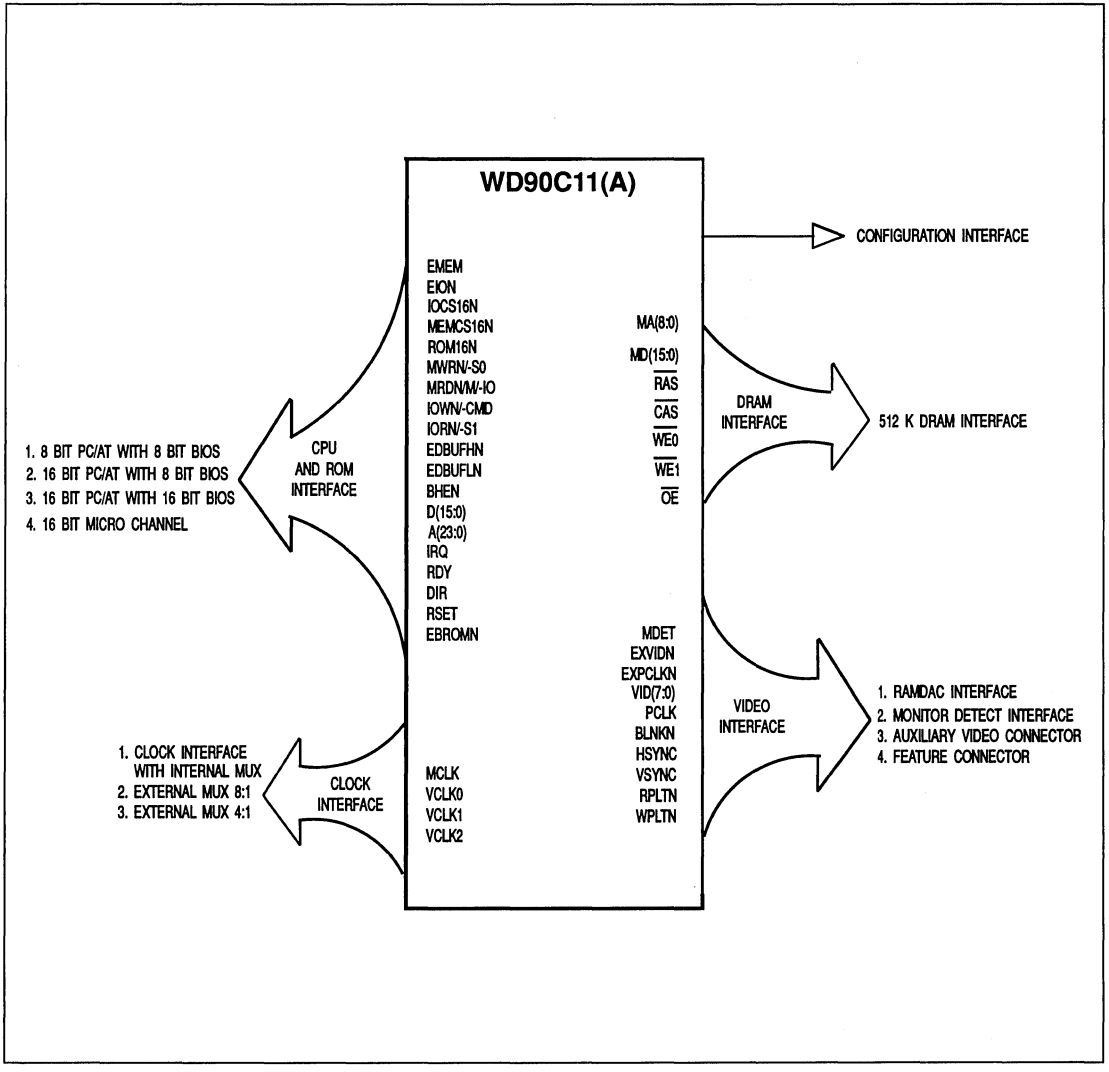

FIGURE A-1. WD90C11(A) INTERFACES

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Figure A-2 shows a block diagram of the WD90C11(A) with 8 bit PC/AT interface using 8 bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

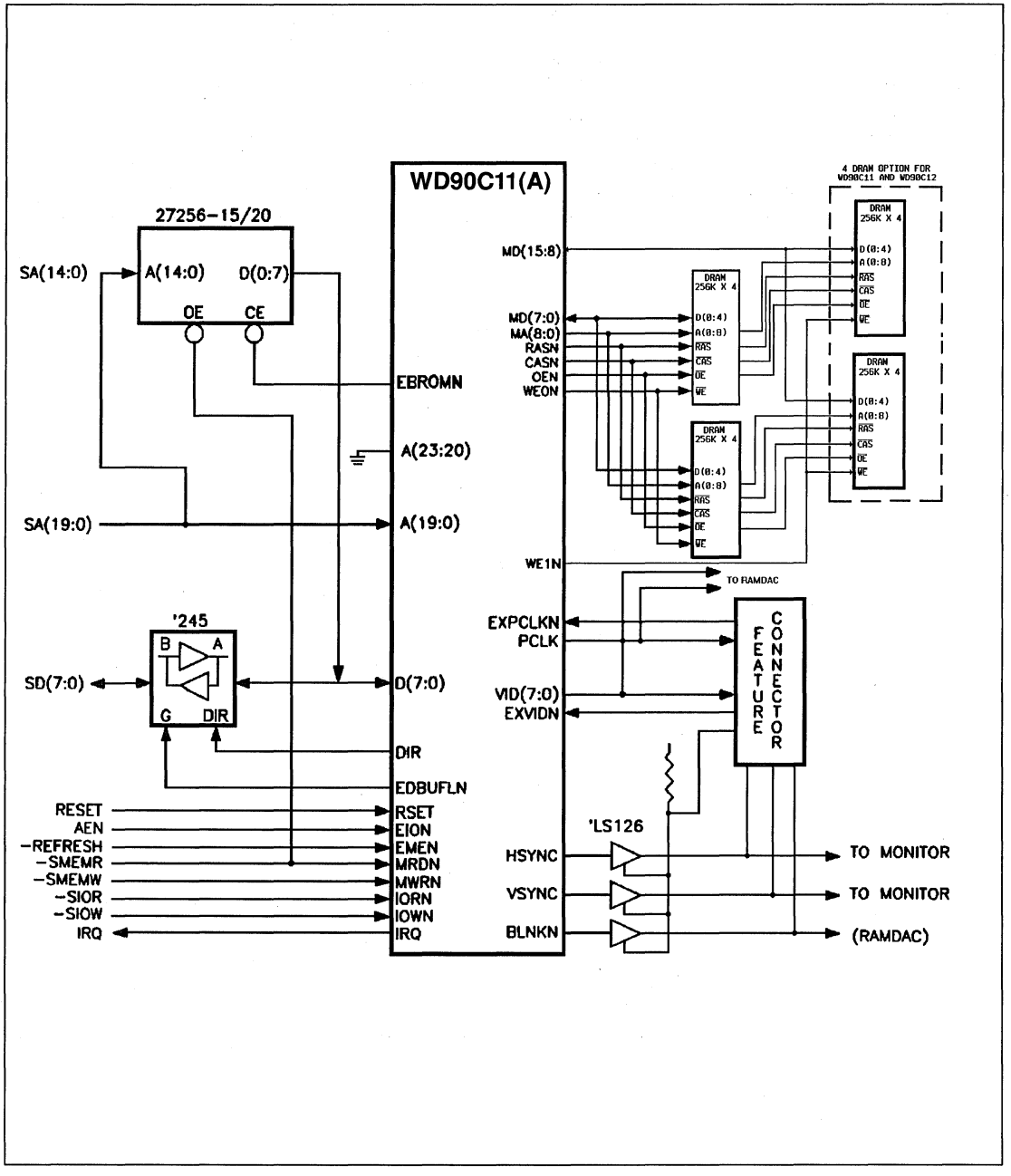

FIGURE A-2. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure A-3 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C11(A). For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown in it.

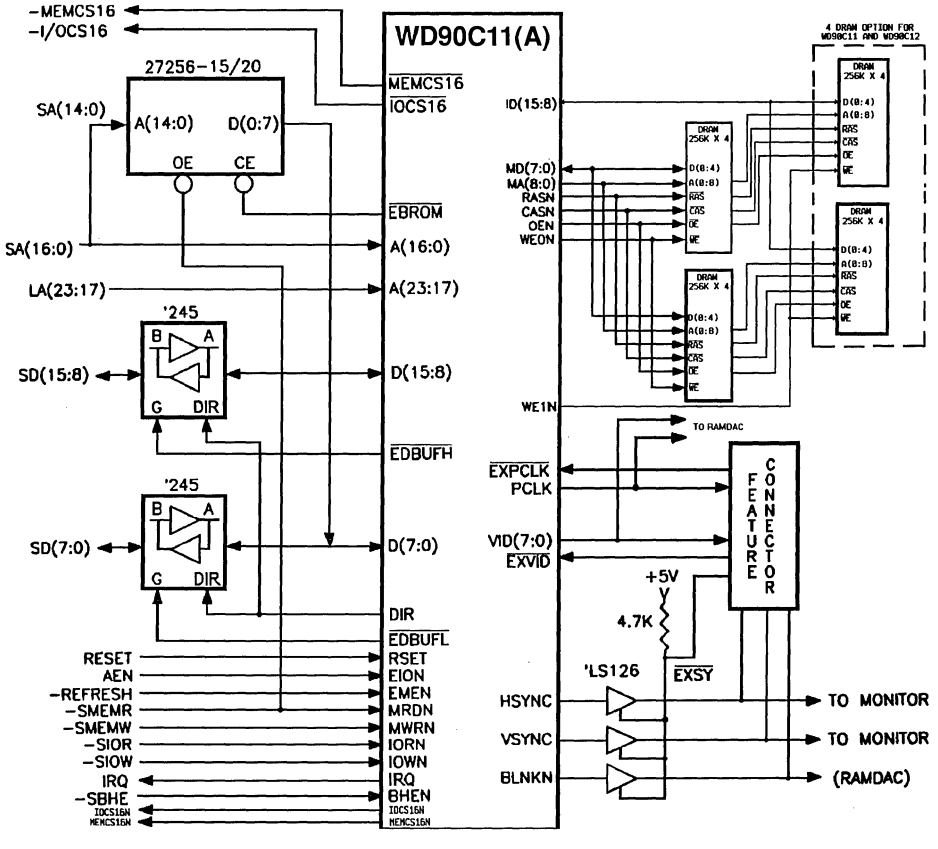

FIGURE A-3. 16-BIT BIOS PC AT INTERFACE WITH 8-BIT BIOS

13

For systems that do not meet hold time of LA address valid from falling edge of MEMR or MEMW, then pull MD8 down and connect LA addresses and SA addresses as shown in Figure A-4. This applies to most 286 systems. Otherwise, connect LA addresses and SA addresses as shown in Figure A-5. This applies to most 386 systems.

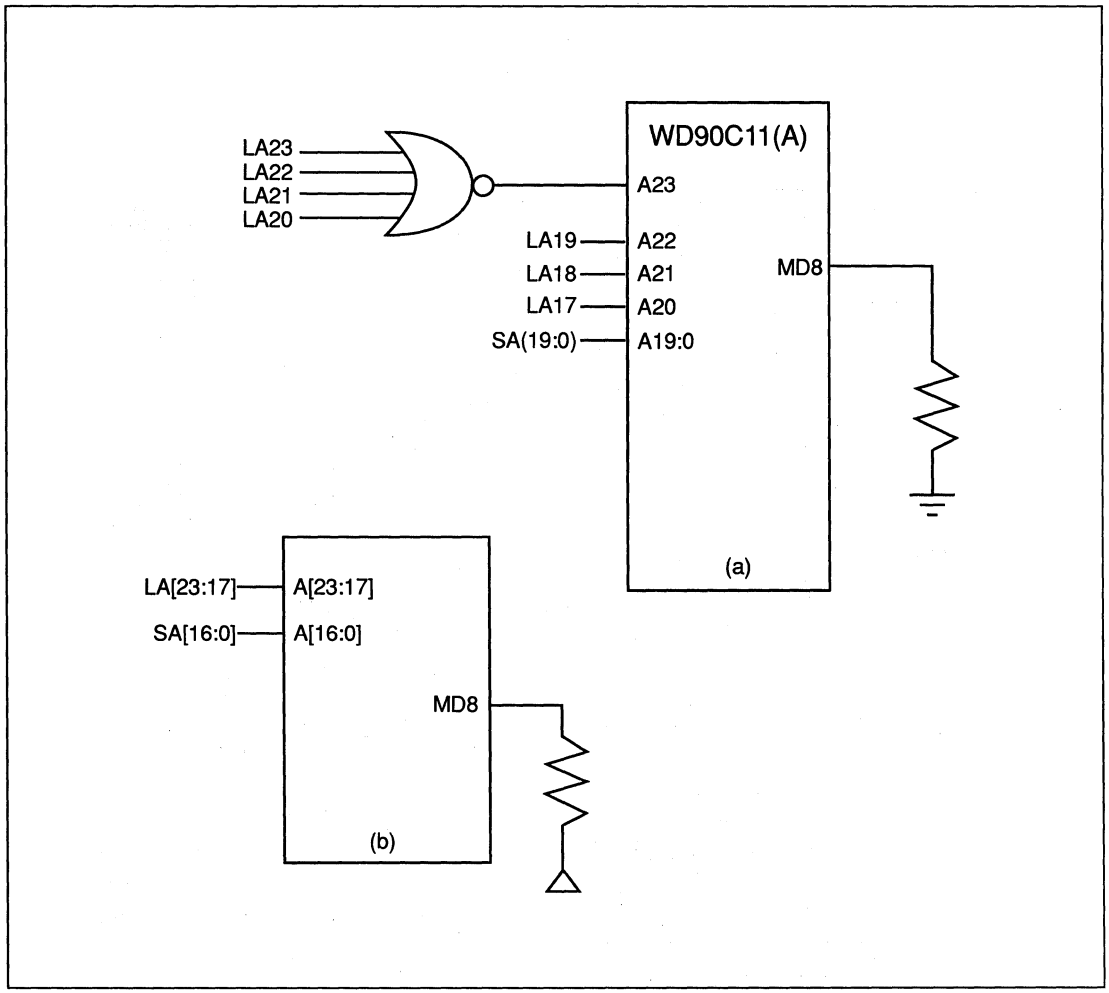

FIGURE A-4. WD90C11(A) INTERFACE FOR 286 OR 386-BASED SYSTEM

Figure A-5 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C11(A). The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds as SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure A-4 for 286-based systems.

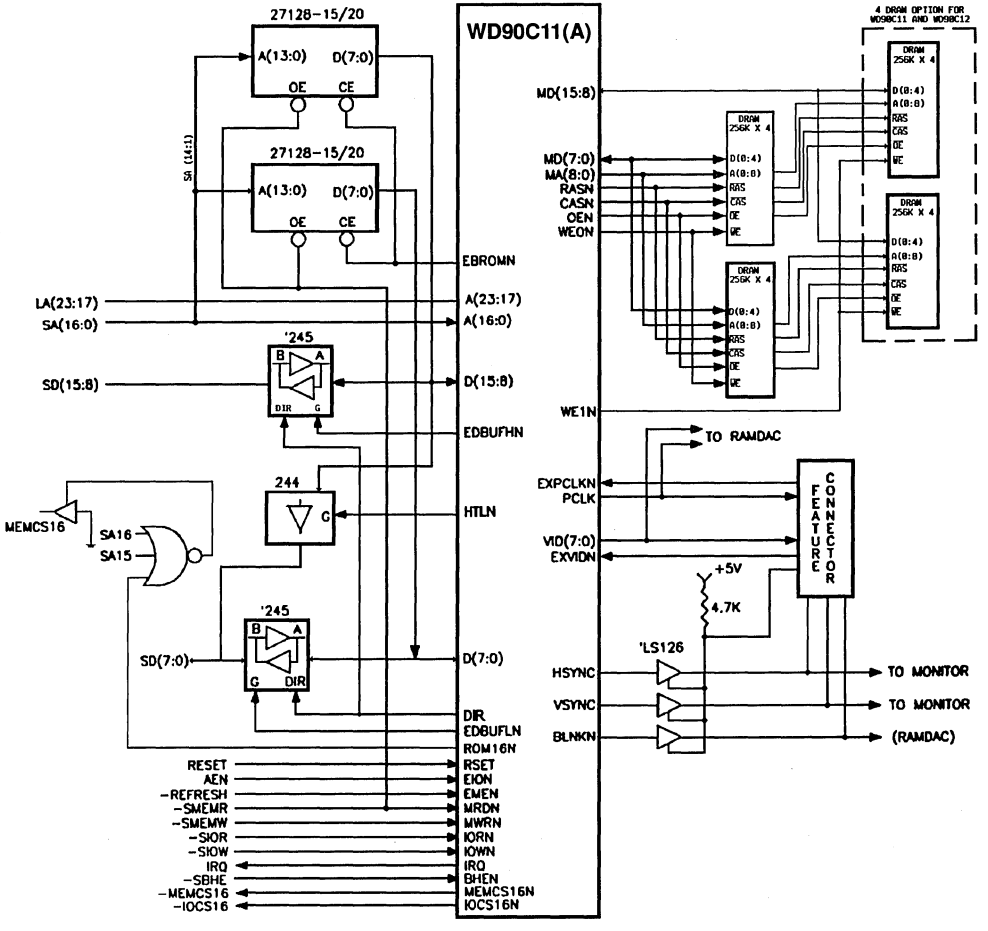

FIGURE A-5. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS (With Optional 512 KBytes: 4- 256K by 4 DRAM)

Figure A-6 illustrates the WD90C11(A) and 16-bit Micro Channel interface. 3C3.D0 is output of port 3C3H bit 0 VGA Subsystem Enable Register.

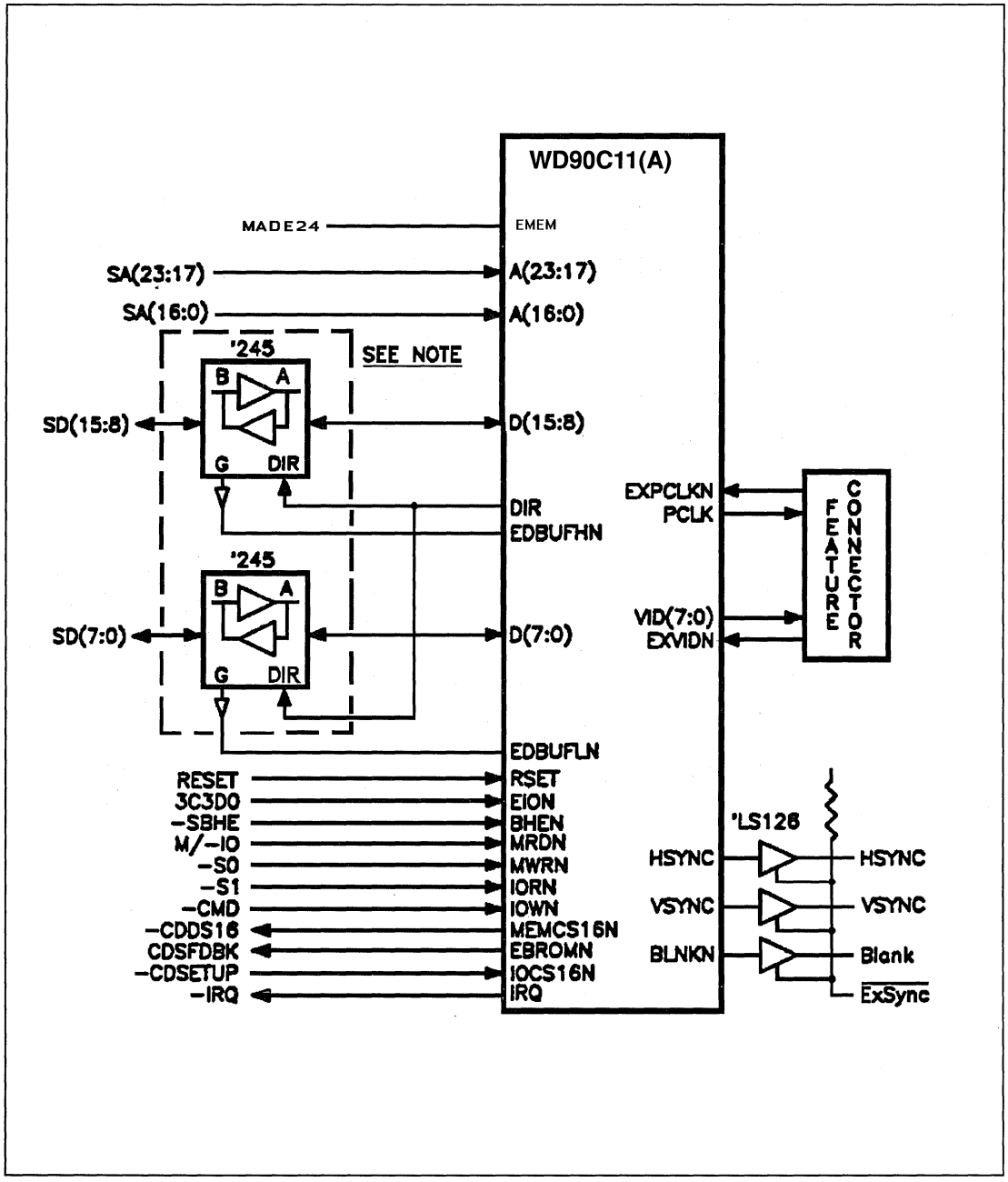

FIGURE A-6. 16-BIT MICRO CHANNEL INTERFACE

Figure A-7 illustrates the WD90C11(A) and RAM-DAC interface block diagram for analog monitors.

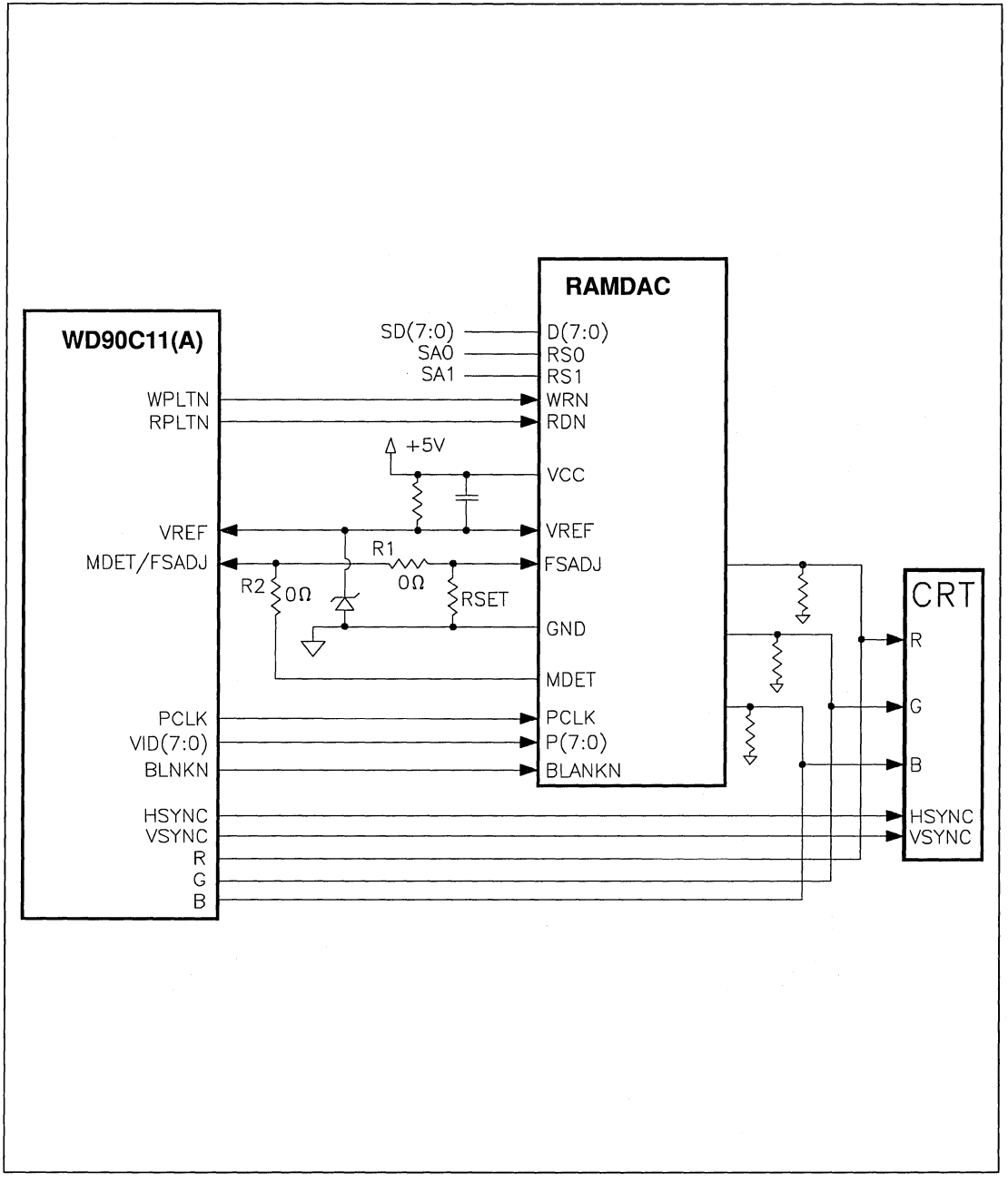

FIGURE A-7. WD90C11(A) WITH RAMDAC INTERFACE

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Figure A-8 illustrates the WD90C11(A) and TTL monitor connections.

NOTES:

1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using the WD90C11(A), install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

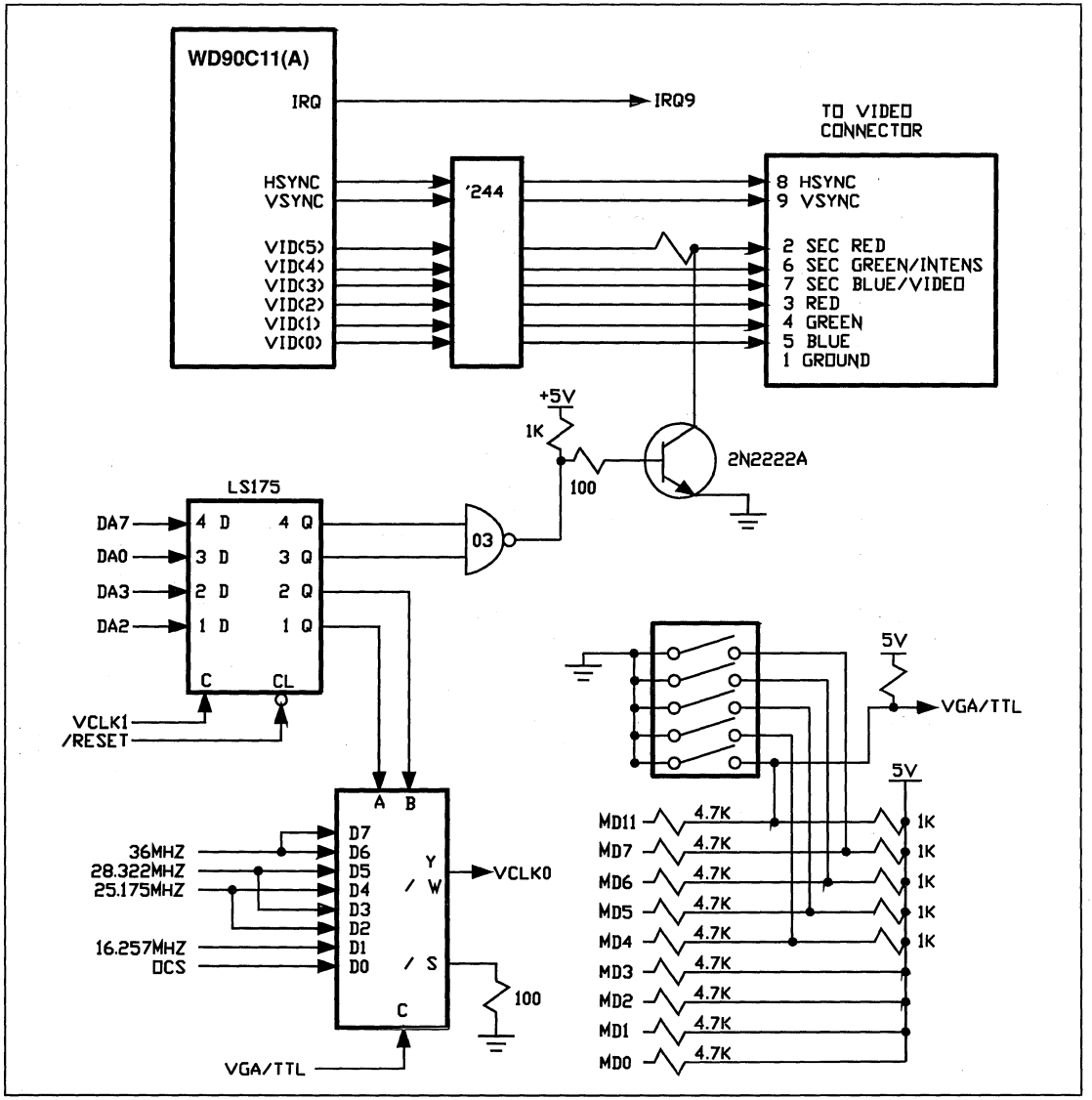

FIGURE A-8. WD90C11(A) AND TTL MONITOR CONNECTIONS

Figure A-9 illustrates the WD90C11(A) with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C11(A) signal pins (VCLK1, VCLK2) inputs.

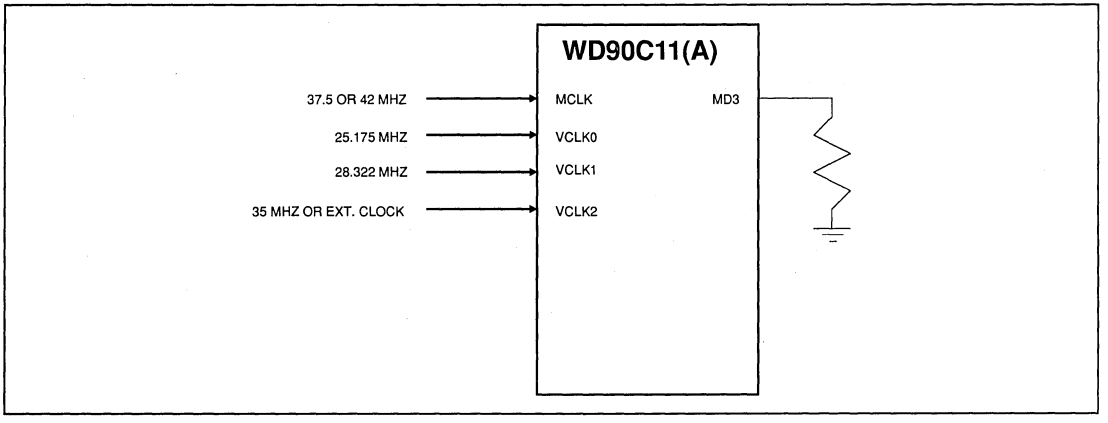

FIGURE A-9. CLOCK INTERFACE

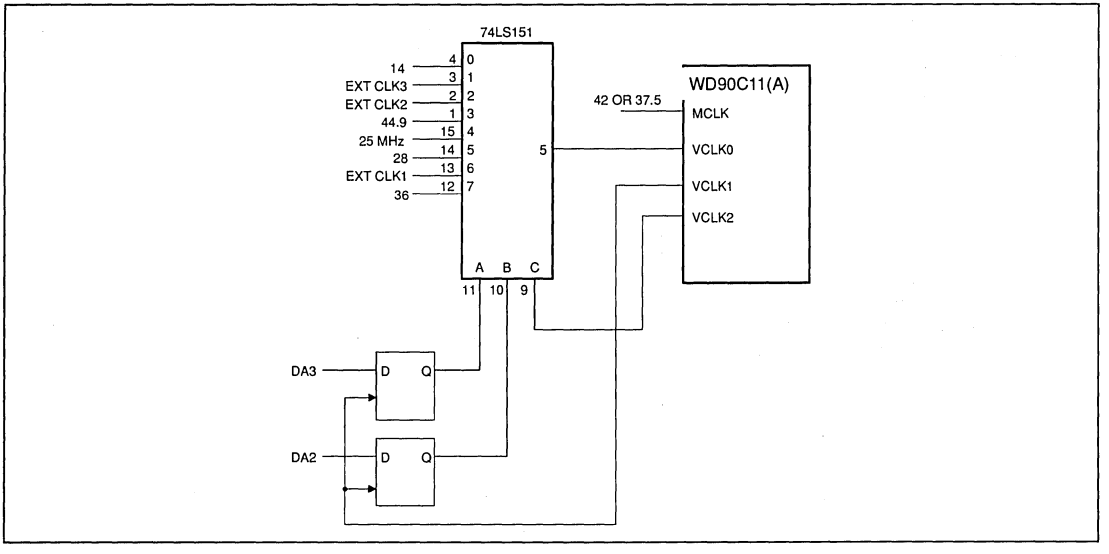

FIGURE A-10. EXTERNAL VIDEO CLOCK MULTIPLEXING

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B.0 SIGNATURE ANALYZER (WD90C11A Only)

A signature analyzer was designed for use in the WD90C11A only. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

B.1 DESCRIPTION

The basis of the signature analyzer is a linear feedback shift register (LFSR). The inputs to the LFSR tap onto the VID_[0:7] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately one half where n is the length of the shift register. A 16-bit signature register is used on the WD90C11A. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$) has been implemented on the WD90C11A. It was modified for multiple inputs as shown in the block diagram.

B.2 OPERATION

The signature analyzer was designed to collect signature of the VID_[0:7] outputs over one vertical frame. The signal path of the VID_[0:7] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3F). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 bits 2 through 0. PR10 also serves as the lock for other registers.

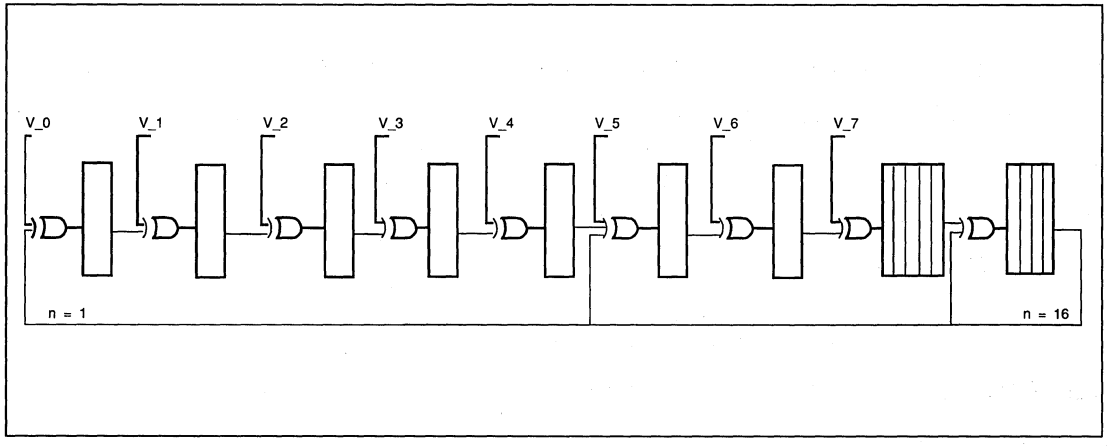

FIGURE B-1. LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/WRITE	DESCRIPTION
0	Start/status	R/W	Writing "1" to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. 1: Busy 0: Finished or not enabled
1	Clear	R/W	Writing "0" to this bit position preloads the LFSR with 0001H. This bit must be set to operate the signature analyzer. 1: Normal operation 0: Preload LFSR
2	Disable Video Input	R/W	This bit is used in a self-test mode. A fixed signature will be generated for any given mode (independent of video memory data). 1: Disable video inputs 0: Enable video inputs
3	Lock Read Port	R/W	This bit must be set in order to read the signature and status. 1: Enable read of LFSR (addresses 3?5.20 and 3?5.21) 0: Disable reads of LFSR

TABLE B-1. CONTROL REGISTER PR19

The following programming steps highlight the sequence that will setup, check and read the signature.

Step 1) 85H-> 3?5.29; release control register (PR10)read and write lock

Step 2) 00H-> 3?5.3F; clear signature analyzer

Step 3) 03H-> 3?5.3F; enable signature analyzer to collect signature

Step 4) read 3?5.3F; check status to check for busy

if LSB = 1 go to step 4)
if LSB = 0 signature is collected, proceed

Step 5) OAH-> 3?5.3F; enable signature analyzer read port

Step 6) read 3?5.20; read low byte of signature

Step 7) read 3?5.21; read high byte of signature

Step 8) 00H-> 3?5.3F; clear signature analyzer and lock read port

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C.0 I/O MAPPING (WD90C11A Only)

C.1 INTRODUCTION

The I/O Mapping was designed for use in the WD90C11A only to isolate board level solder defects. The I/O Mapping allows the IC to enter a test mode where all of the pins in the IC are divided into various groups as inputs and output. The path from PCB trace through inputs, IC, output and PCB trace can be treated as a simple path. With test points on board, quick opens and shorts test can be performed.

C.2 TEST MODE

There are four requirements to meet for the WD90C11A to enter the I/O Mapping test mode.

- MWRN is LOW
- IORN is LOW
- CONFIGURATION SWITCH 2 is HIGH (MD2 is pulled high)
- RESET is HIGH

If both MWRN Aand IORN are low at the same time, it becomes an illegal condition in AT machines and a reserved condition in the PS/2 machines. Configuration switch 2 high will ensure that WD90C11A is in AT mode. Reset controls a transparent latch as shown in Figure C-1. Reset can be dopped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

C.3 PIN GROUPINGS

The following pin groups are done to minimize routing overhead of I/O pin mappings. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the pin name that corresponds to the input pin(s).

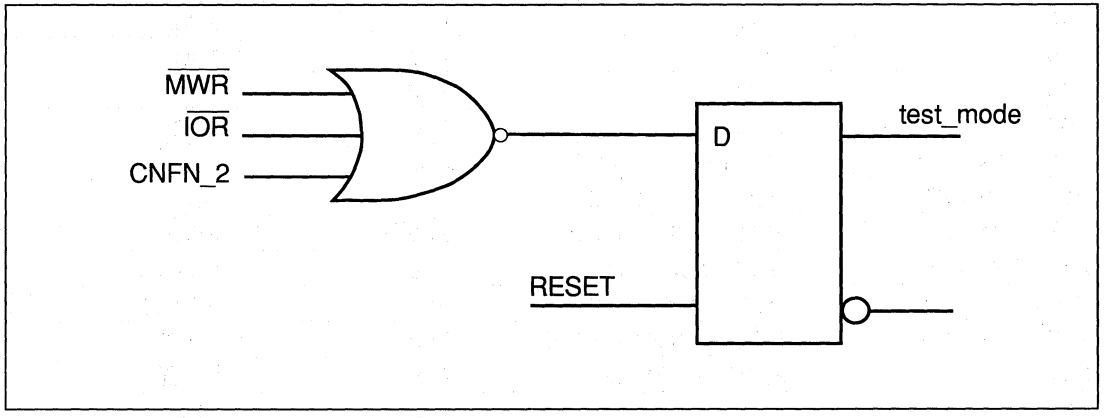

FIGURE C-1. TEST MODE CIRCUIT

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P1 + P4 + P7	A14 + A17 + A20	P16	IRQ
P2 + P5 + P8	A15 + A18 + A21	P18	$\overline{\text{EBROM}}$
P3 + P6 + P9	A16 + A19 + A22	P20	RDY
P10 + P13 + P31	A23 + $\overline{\text{EIO}}$ + D11	P21	$\overline{\text{MEMCS16}}$
P11 + P14 + P24	$\overline{\text{BHE}}$ + $\overline{\text{IOCS16}}$ + D13	P22	$\overline{\text{EDBUFH}}$
P12 + P26	EMEM + D15	P23	$\overline{\text{EDBUFL}}$
P27 + P30	D14 + D12	P24	$\overline{\text{ROM16}}$
P32	D10	P25	$\overline{\text{HTL}}$
P33	D9	P64	$\overline{\text{WE0}}$
P34	D8	P62	$\overline{\text{RAS}}$
P35	D7	P65	$\overline{\text{OE}}$
P36	D6	P59	MA7
P37	D5	P58	MA6
P38	D4	P57	MA5
P39	D3	P56	MA4
P40	D2	P43	$\overline{\text{WE1}}$
P41	D1	P55	MA3
P42	D0	P54	MA2
P45	$\overline{\text{MRD}}$	P53	MA1
P46	$\overline{\text{MWR}}$	P52	MA0
P63	$\overline{\text{CAS}}$	P60	MA8
P66 + P69 + P72	MD15 + MD12 + MD9	P86	USR0
P67 + P70 + P73	MD14 + MD11 + MD8	P87	USR1
P68 + P71 + P74	MD13 + MD10 + MD7	P89	$\overline{\text{BLNK}}$
P75 + P78 + P81	MD6 + MD4 + MD1	P90	VSYNC
P76 + P79 + P82	MD5 + MD3 + MD0	P91	HSYNC
P80 + P94 + P96	MD2 + VCLK2 + VCLK1	P92	$\overline{\text{RPLT}}$
P84 + P98	$\overline{\text{EXPCLK}}$ + MCLK	P93	$\overline{\text{WPLT}}$
P97	VCLK0	P88	PCLK
P109 + P132	$\overline{\text{EXVID}}$ + A13	P100	VID0
P112 + P126	MDET + A8	P105	VID5
P117 + P127	A0 + A9	P104	VID4
P118 + P128	A1 + A10	P103	VID3
P119 + P129	A2 + A11	P102	VID2
P120 + P130	A3 + A12	P101	VID1
P121 + P124	A4 + A6	P107	VID7
P122 + P125	A5 + A7	P106	VID6

NOTE: A + in the input column indicates an OR function for the test input pins only.

TABLE C-1. WD90C11A PIN SCAN MAP

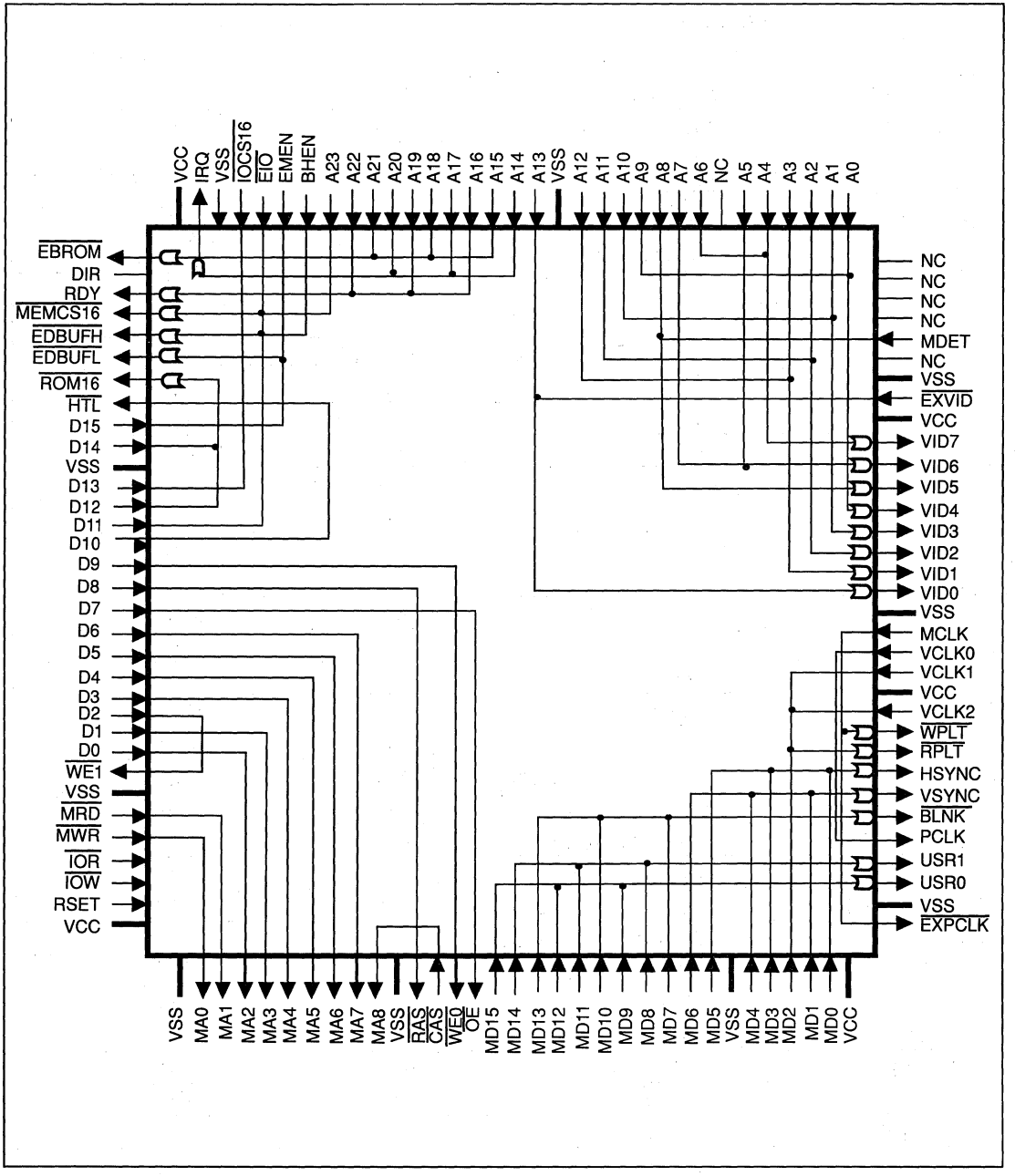

FIGURE C-2. WD90C11A PIN SCAN MAP

WD90C20, WD90C20A

VGA Flat Panel

Display Controller

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

This data sheet applies to both the WD90C20, and WD90C20A. The WD90C20A is a 0.9 micron version of the WD90C20 VGA controller chip.

For convenience all references to these two devices will be referred to as the WD90C20. When a particular feature is available only on one of these devices, it is called out in the text.

See Appendix F for a detailed explanation of the differences between the WD90C20 and the WD90C20A.

1.1 DESCRIPTION

The WD90C20 is a VGA display controller that has been optimized for applications that require flat panel display support. It is an extension of the WD90C00 and as such supports all of the WD90C00's features and modes when driving a standard CRT. The WD90C20's highly integrated design includes a complete Micro Channel or AT compatible bus interface, as well as an on-chip PS/2 compatible RAMDAC with integral monitor detection logic.

The WD90C20 is a VGA controller for up to 640 by 480 plasma and LCD display applications. It provides complete flat panel display subsystems for Micro Channel and AT compatible interfaces and has expanded Micro Channel compatibility.

The WD90C20 is 1.25 micron device and the WD90C20A is a 0.9 micron CMOS device.

1.2 FEATURES

- On-chip Micro Channel interface
- On-chip 8- or 16-bit AT bus interface
- Direct interface with CRT and flat panel displays (monochrome and color TFT LCD)
- On-chip frame rate modulation logic
- Supports all functions of WD90C00 VGA chip in CRT mode
- 32-shade gray scale mapping
- Software-selectable vertical screen centering
- Hardware vertical expansion(WD90C20A)*
- On-chip PS/2 compatible RAMDAC*
- On-chip monitor detection logic
- 32 MHz maximum LCD video clock (WD90C20)
  36 MHz maximum LCD video clock (WD90C20A)
- 45 MHz maximum CRT video clock
- Flexible power management features *
- Vcc may be removed in powered system
- 256 out of 512 color support for DSTN color LCD(WD90C20)
  256 out of 4K color support for DSTN color LCD (WD90C20A)
  8 or 512 color support for TFT color LCD
- Four powerdown modes

* Patent pending

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2.0 THEORY OF OPERATION

The WD90C20 contains six major functional modules. In addition to the CRT controller, there is a sequencer, a graphics controller, an attribute controller, a flat panel interface, and a RAMDAC. The WD90C20 handles all display buffer management functions, including display refresh cycles, memory refresh cycles, and the arbitration and sequencing of host access cycles.

- **Sequencer**

The sequencer provides the display memory control signals and timing. It also provides the synchronization between the CRT controller and the attribute controller. The sequencer controls the arbitration between the CPU cycle and the CRT cycle, or the CPU cycle and the memory refresh cycle.

- **Graphics Controller**

The graphics controller manages data flow between video memory and the attribute controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the sequencer.

- **Attribute Controller**

The attribute controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video (as well as background or foreground video) in VGA and enhanced VGA BIOS modes.

- **Flat Panel Adapter**

The flat panel adapter section includes color-to-gray scale mapping*, a dithering mapping RAM, a dithering engine, a row buffer*, shading control*, and panel interface logic.
* Patent pending.

- **RAMDAC**

The WD90C20's on-board RAMDAC is a low power, PS/2-compatible device with special power-down modes and PS/2 monitor detection logic.
The RAMDAC's 256 by 18 color look-up table has triple 6-bit D/A converters, a pixel mask register, and composite blank generation on the three channels. It also supports the use of an external voltage reference. Without external buffering the RAMDAC will generate RS-343A-compatible video signals into a doubly terminated 75 ohm load or a 50 ohm load. Integral and differential linearity errors are a maximum of ± 1/2 LSB.

2.1 WD90C20 INTERFACES

The WD90C20 has five main system interfaces: the CPU, a display memory, a RAMDAC/CRT, a clock, and a flat panel display. In most implementations, these interfaces eliminate the need for glue logic.

- **CPU Interface**

The WD90C20 host interface supports both the AT and Micro Channel buses with both 8- and 16-bit data path widths. The WD90C20 may also be directly connected to the bus if drive requirements permit. The bus mode is determined by the status of the configuration register bit, CNF(2), which is loaded by the de-assertion of reset. The value that is loaded reflects the status of one of the memory data pins at reset.
I/O transfers to and from the device are 8-bits wide, and display memory transfers are 8- or 16-bits wide, depending on the video mode selected. Because of their architecture, EGA type planar modes are restricted to 8-bit display data transfers. Text and 256 color extended modes allow 16-bit transfers on a 16-bit bus.

The controller generates wait states as required during display memory accesses. Wait states are not generated for I/O or video BIOS ROM accesses. Special I/O ports, such as 46E8H (when in AT bus mode) for setup, and 102H for VGA enable, are internally implemented.

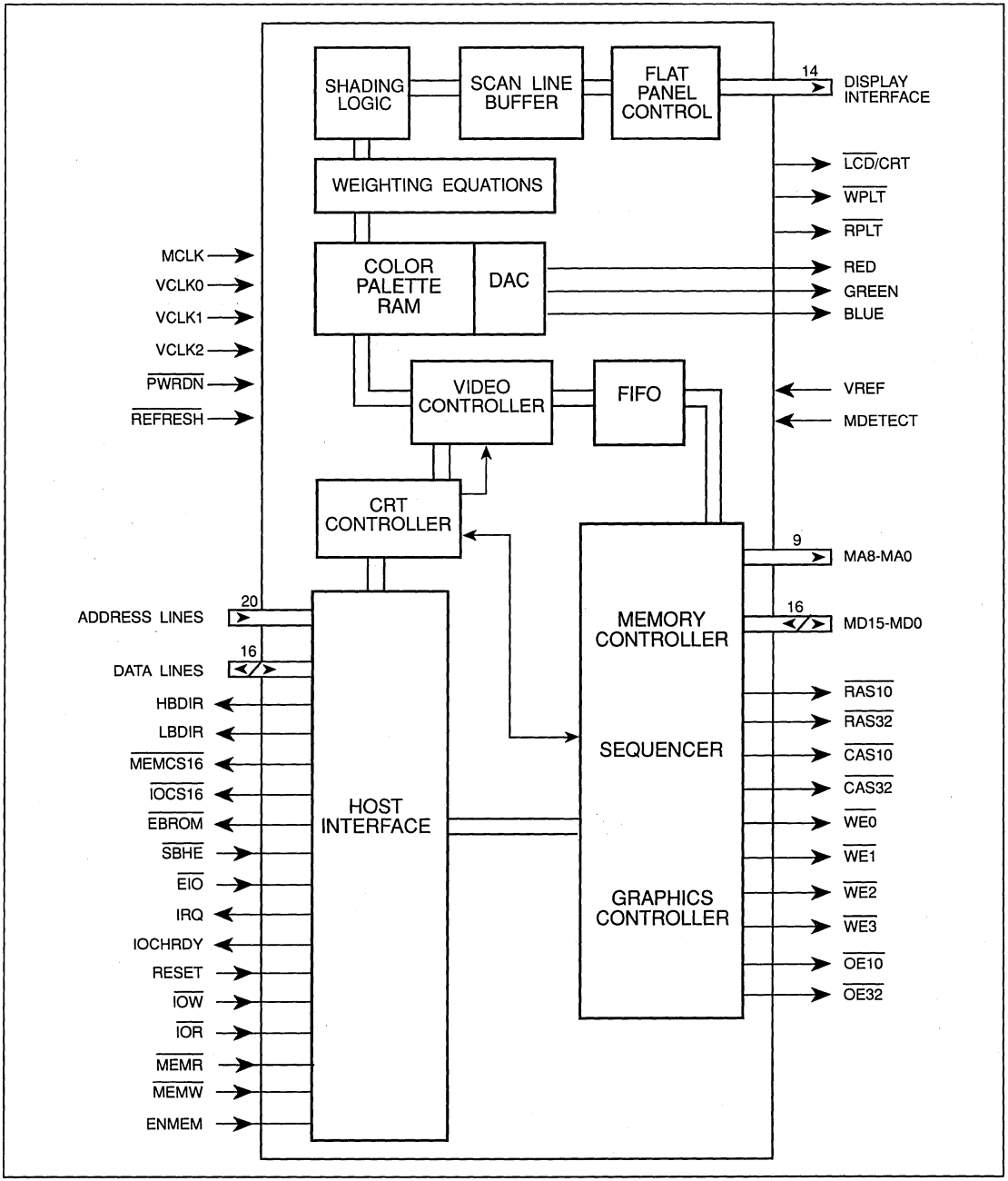

FIGURE 2-1. WD90C20 BLOCK DIAGRAM

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- **Display Memory Interface**

The WD90C20 generates all signals and memory timing required to operate the display memory. It directly controls three display memory sizes, 256 Kbyte, 512 Kbyte, and 1 Mbyte, as follows:

MEMORY SIZE	NUMBER AND TYPE OF DRAM REQUIRED
256 Kbytes	8 64 Kbyte by 4 DRAMs, or 2 64 Kbyte by 16 DRAMs
512 Kbytes	16 64 Kbyte by 4 DRAMs*, or 4 64 Kbyte by 16 DRAMs
1 Mbyte*	8 64 Kbyte by 16 DRAMs, or 8 256 Kbyte by 4 DRAMs

* Requires minimal support logic.

Page mode memories are required for all configurations. With a 36 MHz memory clock (MCLK), 120 ns devices may be used. If 256 color CRT modes are to be supported, 100 ns DRAMs and a 45 MHz MCLK are required. The WD90C20 includes special offset registers that allow the host to address up to 1 Mbyte of display memory.

- **CRT/RAMDAC Interface**

In addition to its internal RAMDAC, the WD90C20 allows the use of an external RAMDAC. This is helpful in specialized applications where a 24-bit wide color lookup table or pixel demultiplexing (to obtain higher video rates) is required. The external RAMDAC interface will support any Bt471/478/476 compatible device.

- **Clock Interface**

The WD90C20 has four clock input signal pins. Three of these (VCLK0, VCLK1, and VCLK2) are normally connected to oscillators. VCLK1 and VCLK2 may be configured to control an external clock multiplexor or clock generator, such as the WD90C61. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 36 MHz for 120 ns DRAMs or 45 MHz for 100 ns DRAMs.

- **Flat Panel Interface**

The WD90C20 is designed to interface with 640 by 480 LCD or plasma panels. The flat panel interface lines change function to support the specific panel type chosen. Table 2-1 summarizes their use for each mode of operation.

When in LCD mode, with frame rate modulation selected, the controller supplies eight pixels per shift clock (four for the upper panel, and four for the lower). If pulse width modulation is selected, the controller provides two pixels per shift clock (one 4-bit pixel for the upper screen, and one 4-bit pixel for the lower screen).

When in Plasma mode, pulse width modulation is used to provide shading, while the controller supplies one pixel (four bits per pixel) per clock.

When in color STN LCD mode, the controller supplies two pixels per shift clock and uses hardware dithering. Each pixel (three bits, one each for R, G, and B), with dithering, provides 16 colors. The user can select:

– 256 out of 512 colors (WD90C20)
– 256 out of 4K colors (WD90C20A)

LCD	PLASMA	CRT
UD (3:0)	VD (3:0)	P (7:4)
LD (3:0)	Reserved	P (3:0)
FR	Reserved	BLANK
FP	VS	VSYNC
LP	HS	HSYNC
XSCLK	XSCLK	Reserved
WGTCLK	ENABLE	Reserved
Reserved	Reserved	PCLK

TABLE 2-1. DISPLAY INTERFACE OUTPUT FUNCTIONS

MONOCHROME LCD	COLOR LCD Device
UD (3)	R1
UD (2)	G1
UD (1)	B1
UD (0)	Border Information
LD (3)	R2
LD (2)	G2
LD (1)	B2
LD (0)	Reserved

TABLE 2-2. LCD DATA BIT ASSIGNMENTS

- **Powerup Configuration**

An internal 8-bit configuration register, CNF, controls the behavior of the major interfaces. Its bits are loaded with the inverted state of memory data lines 0 through 7 at the time RESET is deasserted. Pullup or pulldown resistors on the MD lines are used to set the configuration.

3.0 FLAT PANEL SUPPORT CONSIDERATIONS

Supporting VGA compatible graphics on flat panel displays involves several non-trivial issues, including:

- Display Timing Differences
- Screen Size Mapping
- Color-to-Gray Scale Mapping
- Shading Mechanics
- Split Screen Refresh

The following paragraphs address each of these issues.

• Display Timing Differences

Typically, flat panel displays have different timing requirements from a CRT. To overcome this problem, the WD90C20 provides a set of hidden display timing registers, which are read/write protected in locked mode.

• Screen Size Mapping

Unlike those of a CRT, the pixels on a flat panel display are real, discrete entities of a fixed size. This can result in problems when different display modes are mapped onto a single panel. The WD90C20 has been designed to support VGA and various backward compatible display modes on a 640 by 480 dot flat panel and it provides integral hardware support to deal with screen size incompatibilities.

In case of backward compatible display modes, such as EGA, which has a maximum resolution of 640 by 350, the vertical resolution of the mode is less than the number of dots of vertical resolution of the panel. This results in an active display area that is smaller than that of the panel and shifted up on the display, as shown in Figure 3-1(A). There are two ways to enhance screen size mapping as described below.

The simplest approach, supported by the WD90C20 is to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel. In the case of an EGA 350 line mode being displayed on a 480 line panel, this would involve shifting the active display area down 65 lines (that is, 480 minus 350, the quantity divided by two). The effect of such a mapping is shown in Figure 3-1(B).

If the goal is to have the active display area fill the panel in all modes, then the active display area can be expanded by double scanning a portion of the active scan lines. Previously available controllers simply double scan lines at regular intervals, every third line in the case of EGA 350 line modes.

The WD90C20A uses an advanced proprietary algorithm that automatically expands to fill all 480 lines*. This algorithm can be used to support better "screen scrolling" when in 350 line modes.

* Patent pending on Hardware Vertical Expansion.

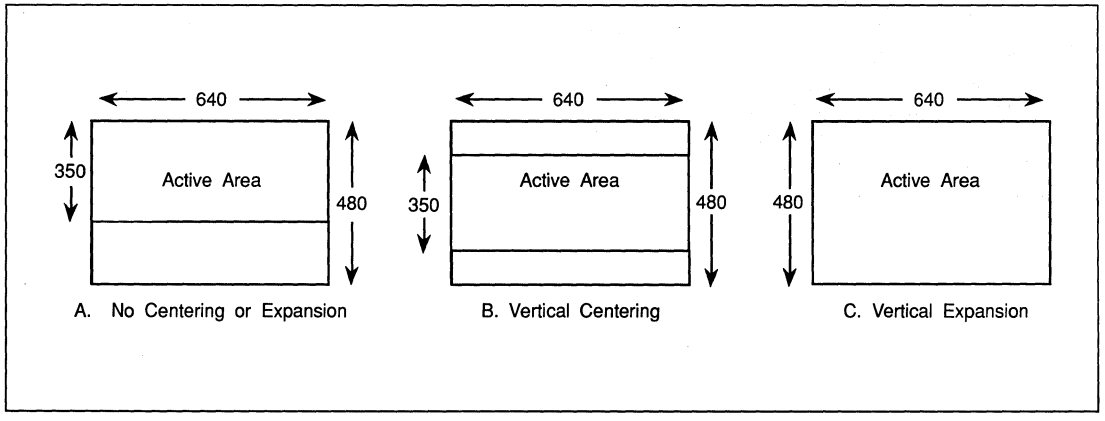

FIGURE 3-1. EXAMPLE OF SCREEN SIZE MAPPING

Under certain display conditions, any expansion scheme can result in undesirable aliasing effects of the displayed data. For this reason the WD90C20A allows the system designer flexibility to choose between vertical expansion or centering as shown below.

	CENTERING	VERTICAL EXPANSION
WD90C20	Y	N
WD90C20A	Y	Y

Horizontal resolution issues involve 720 dot modes such as VGA text and Hercules graphics. In VGA text mode, the 9th dot in each character box is dropped. The net effect is a slight compression in the spacing between characters. Alternatively, a different font may be loaded, although a nonstandard font size may not be fully compatible.

- **Color-to-Gray Scale Mapping**

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following RGB weighting equation:

$$I = .30R + .59G + .11B$$

Unfortunately, many of the currently available panels support at most sixteen shades and some only support two. In order to provide faithful support of all of the standard VGA modes on a flat panel, the WD90C20 provides a range of features to map colors to intensities and control panel shading. Foremost among these is sophisticated logic that converts gray scale values into dithering patterns. Additionally, the device allows software modification of the weighting values used in the gray scale mapping equation. Figure 3-2 gives an overview of the color-to-gray scale support provided by the WD90C20.

- **Shading Mechanics**

The WD90C20 supports shading via either frame rate or pulse width modulation. Pulse width modulation is handled via the display panel. The controller transfers 2, 3, or 4 bits per pixel to the driver logic on the panel, along with a high speed clock signal used to sequence the shading logic. Frame rate modulation, on the other hand, must be implemented in the display controller. The WD90C20 provides support for 2, 4, 8, 16, or 32 shade frame rate modulation with its integrated dithering controller. Any combination of dithering patterns can be selected via the dithering controller's mapping RAM. This design allows the WD90C20 to provide flicker-free frame rate modulation with frame rates as low as 70 Hz.

- **Split Screen Refresh**

The WD90C20 provides support for panels that are split into upper and lower panels requiring simultaneous refresh. This type of refresh is typically used by non-active matrix LCDs.

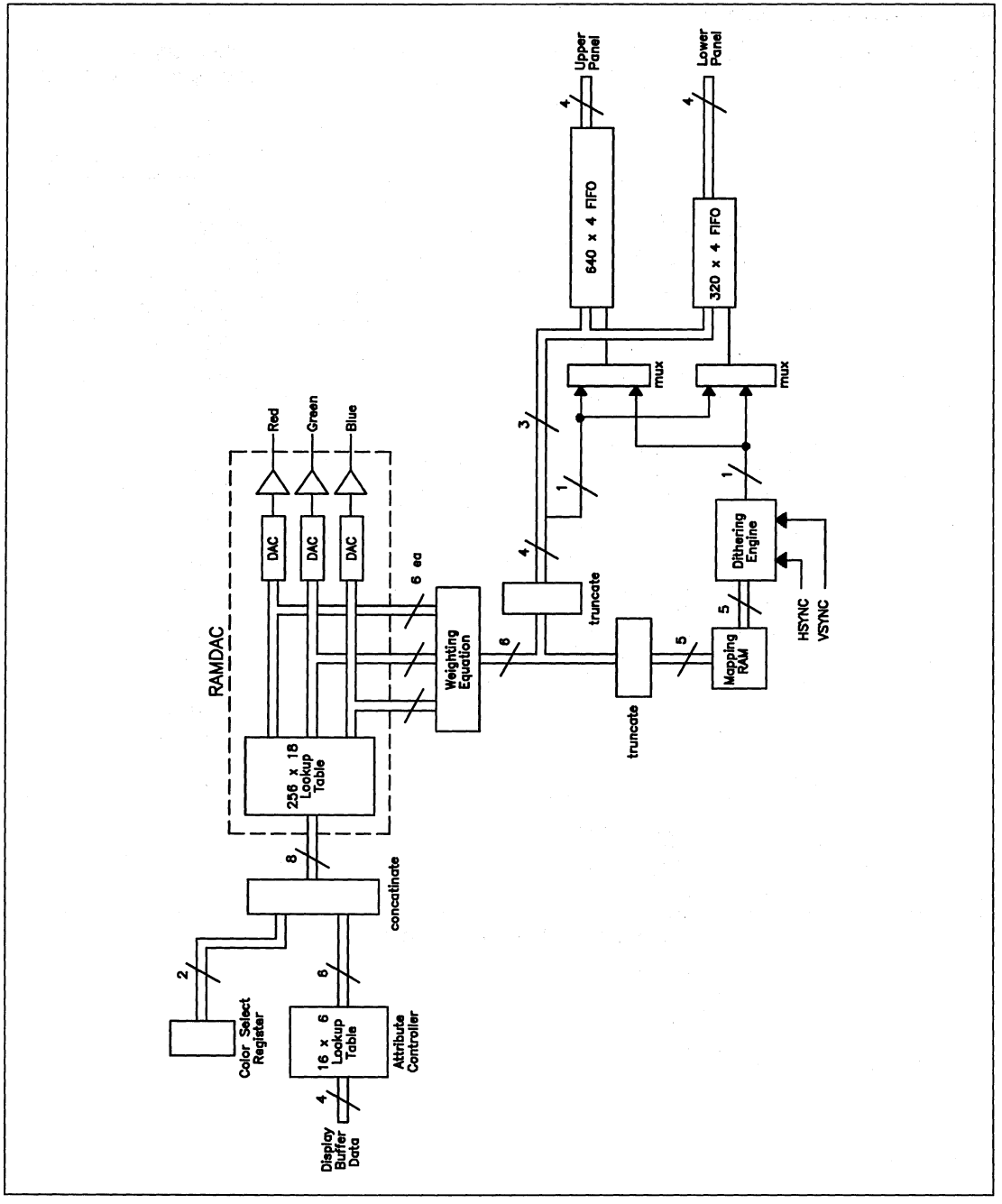

FIGURE 3-2. WD90C20 COLOR MAPPING

4.0 SIGNAL DESCRIPTION

Figure 4-1 illustrates the 132 plastic flat pack (PFP).

Table 4-1 lists all pins referenced in Figure 4-1 and provides a detailed description of each signal.

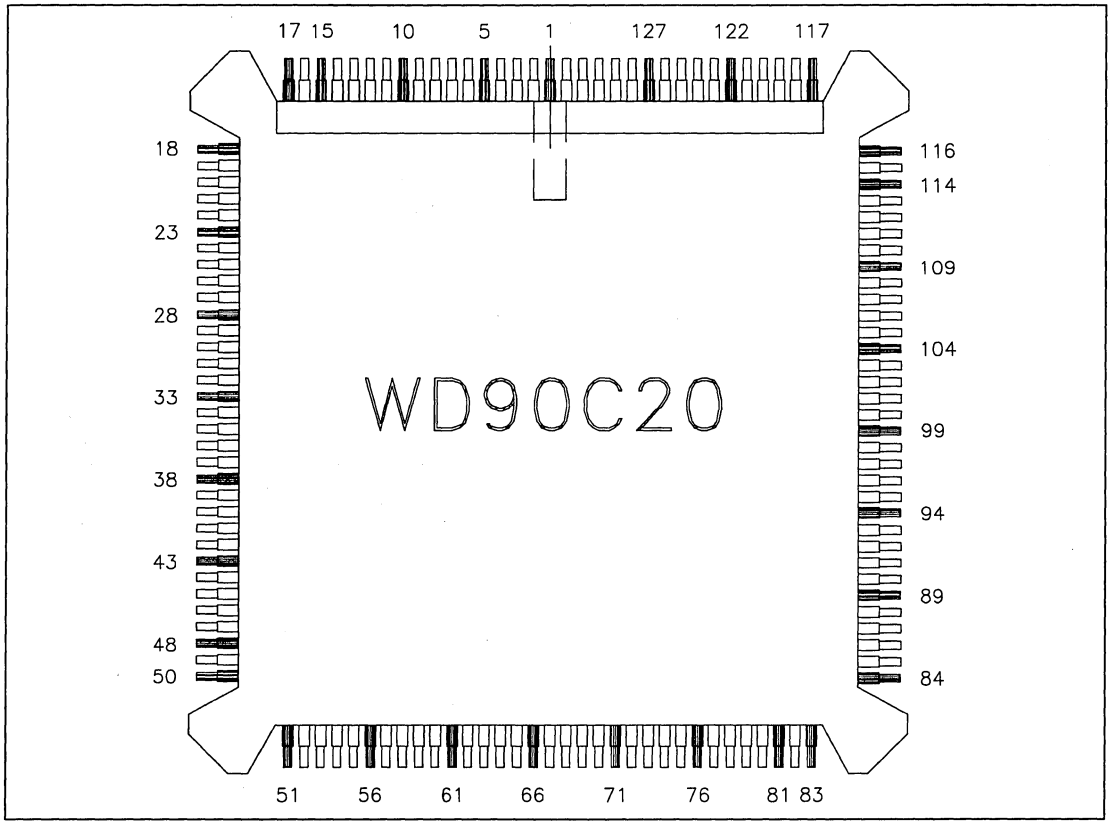

FIGURE 4-1. 132-PIN PFP (TOP VIEW)

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PIN	MNEMONIC	I/O	DESCRIPTION
			POWERON
42	RESET	I	**Reset** This signal input will reset the WD90C20. MCLK and VCLK0 should be connected to the WD90C20 in order for the WD90C20 to initialize during reset. Western Digital Imaging Registers, PR1 and CNF, are initialized at powerup reset based on the logic level on the MD15-0 bus as determined by pullup/ pulldown resistors. The reset pulse width should be at least ten MCLK clock periods.
			CLOCK SELECTION
96	VCLK2	I/O	**Video Clock 2** This pin can be a third video display clock input or an output to the external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
97	VCLK1	I/O	**Video Clock 1** This pin can be a second video display clock input or an output to the external clock selection module. Pin direction is determined on reset by a pullup/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
98	MCLK	I	**Memory Clock** This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system micro-processor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 45.0 MHz for 100 ns DRAMS.
99	VCLK0	I	**Video Clock 0** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
			HOST INTERFACE
1 - 2 117 - 122 124 - 132	SA15 - SA16 SA0 - SA5 SA6 - SA14	I	**Address Bus (SA16-SA0)** These active high inputs form the lower order 17 bits of video memory address. These inputs are directly connected to the system bus.

TABLE 4-1. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
3 - 5	LA17 - LA19	I	**Unlatched Address Bus (LA19 -LA17)** These active high inputs form the high-order three bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
6	SBHE	I	**System Byte High Enable** If SA0 is "0", this signal is used to enable 16-bit data transfer mode when SBHE is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]).
7	ENMEM	I	**Enable Memory** This line is driven by external decode logic. In AT mode, this signal is decoded by LA23 - LA20 and $\overline{\text{REFRESH}}$. In Micro Channel mode, this signal is decoded by LA23 - LA20 and MADE24 ("1" = enable).
8	$\overline{\text{EIO}}$/3C3D0	I	**Enable I/O** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0, and enables video subsystem memory and I/O address decoding ("1" = enable).
11	ALE $\overline{\text{CDSETUP}}$	I	**ALE** In AT mode, this line is ALE; in Micro Channel mode, it is driven by the host to individually select channel connector slots during system configuration and error recovery procedures.
12	IRQ/ $\overline{\text{IRQ}}$	O	**Interrupt Request** Programmable processor interrupt request. It is enabled via Bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of the vertical display occurs, this signal goes active, causing an interrupt. It will stay latched until CRTC11 Bit 4 clears it. In an AT system IRQ is not connected, although you may connect it if you desire. $\overline{\text{IRQ9}}$ is used to generate an interrupt in Micro Channel mode. For further details, see the reference literature.
13	$\overline{\text{EBROM}}$ $\overline{\text{CDSFDBK}}$	O	**Enable BIOS ROM** In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). It is not active for access to addresses in the range C60000H-C67FFH, but this address range may be mapped-in by setting PR17 (0) = 0. A write to the WD90C20 internal I/O port address, 46E8H, causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping. In Micro Channel mode, this signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the addresses specified by the host.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

14

PIN	MNEMONIC	I/O	DESCRIPTION
14	MEMCS16/ CDDS16	O	**Memory Chip Select 16 Bits** In AT mode, this line is used to respond to the host to enable a 16-bit video memory data transfer. In Micro Channel mode, this line provides CDDS16 for 16-bit video memory or I/O access. (For WD90C20 only, this line must be inverted to provide CDDS16).
15	IOCHRDY/ CDCHRDY	O	**Ready** An active high output which signals to the system processor that a memory access is complete. This signal is used only to add wait states to the bus cycles during video memory accesses. It is pulled inactive by the WD90C20 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
16	HBDIR/ HSYNC	O	**High Byte Direction** This line is used to control the data direction of an external high byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles. (For the WD90C20A only simultaneous display mode, the HBDIR pin can be programmed to output CRT HSYNC.)
17	LBDIR/ VSYNC	O	**Low Byte Direction** This line is used to control the data direction of an external low byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles. (For the WD90C20A only simultaneous display mode, the LBDIR pin can be programmed to output CRT VSYNC.)
19 - 26 29 - 36	SD15 - SD8 SD7 - SD0	I/O	**Data Bus (SD15 - SD0)** These bidirectional signals may either be connected directly to a local data bus requiring less than 8 ma. of source/sink, or may be connected through two external bus buffers.
38	MEMR/ M/IO	I	**Memory Read** In AT mode, this signal is called SMEMR and is an active low memory read strobe. It is asserted in 8-/16-bit memory read cycles. In Micro Channel mode, the signal is called M/IO. It distinguishes between memory and I/O cycles. When (M/IO) is high, a memory cycle is in process. A low on (M/IO) shows that an I/O cycle is in process. For further details, refer to the reference literature.
39	MEMW/ S0	I	**Memory Write** The active low memory write strobe in AT mode for 8-/16-bit data transfers. In Micro Channel mode, it becomes S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with the S1, M/IO and CMD signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
43	$\overline{\text{REFRESH}}$	I	**Refresh** This active low input pin is connected to the system $\overline{\text{REFRESH}}$ signal from the I/O bus.
40	$\overline{\text{IOR}}$/ $\overline{\text{S1}}$	I	**I/O Read** Active low I/O read strobe in AT mode. It is asserted in 8-/16-bit I/O read bus cycles. $\overline{\text{S1}}$ is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.
41	$\overline{\text{IOW}}$/ $\overline{\text{CMD}}$	I	**I/O Write** Active low strobe. In AT mode, the strobe signals an I/O write for 8-/16-bit I/O write cycles. In Micro Channel mode it is synonymous with $\overline{\text{CMD}}$; address bus validity is signaled by $\overline{\text{CMD}}$ going low while the rising edge of $\overline{\text{CMD}}$ indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
			DISPLAY MEMORY INTERFACE
45 - 52 55	MA0 - MA7 MA8	O	**Memory Address (MA0 - MA8)** Display memory DRAM address.
56	$\overline{\text{RAS10}}$	O	**Row Address Strobe** Active low Memory Maps 1 and 0 RAS output signal.
57	$\overline{\text{RAS32}}$	O	**Row Address Strobe** Active low Memory Maps 3 and 2 RAS output signal.
58	$\overline{\text{CAS10}}$	O	**Column Address Strobe** Active low Memory Maps 1 and 0 CAS output signal.
59	$\overline{\text{CAS32}}$	O	**Column Address Strobe** Active low Memory Maps 3 and 2 CAS output signal.
60	$\overline{\text{WE0}}$	O	**Write Enable** Active low Memory Map 0 DRAM write enable signal.
61	$\overline{\text{WE1}}$	O	**Write Enable** Active low Memory Map 1 DRAM write enable signal.
62	$\overline{\text{WE2}}$	O	**Write Enable** Active low, Memory Map 2 write enable signal.
63	$\overline{\text{WE3}}$	O	**Write Enable** Active low, Memory Map 3 write enable signal.
64	$\overline{\text{OE10}}$	O	**Output Enable** Active low, Memory Maps 1 and 0 output enable signal.
65	$\overline{\text{OE32}}$	O	**Output Enable** Active low, Memory Maps 3 and 2 output enable signal.
68-75 77-84	MD15 - MD8 MD7 - MD0	I/O	**Data Lines** Lines MD15 through MD0 are the data bus to the video display DRAMS. Data lines MD0 through MD15 are pulled up or down with resistors to provide setup information on power-up (reset) as shown in Table 4-2.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS
44	$\overline{\text{PWRDN}}$	I	**Power Down Selected** This active low input signal is used to disable screen refresh cycle.
110	$\overline{\text{LCD}}$/CRT	O	**LCD or CRT Selected** This active high output is used to power down an external RAM-DAC chip whenever the WD90C20 operates in LCD mode. "1" is CRT mode, and "0" is LCD mode.
			*DISPLAY INTERFACE**
86	PCLK	O	**Pixel Clock** This line is used to clock the video outputs into a RAMDAC in a CRT interface.
87	XSCLK	O	**Shift Clock** In an LCD interface, this signal is used to shift the upper and lower panel's data into the X-driver. In a Plasma interface, this signal is also used as shift clock.
88	WGTCLK	O	**Weight Control Clock** In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "ENABLE VIDEO" signal.
89	LP/HSYNC	O	**Latch Pulse** In an LCD interface, this signal is used to latch all the data in the current scan line. In either a Plasma or a CRT interface, this signal is used for horizontal sync.
90	FP/VSYNC	O	**Frame Pulse** This signal is used to indicate the start of scanning to the Y-driver in an LCD interface. In either a Plasma or a CRT interface, this signal is used for vertical sync.
91	FR/BLANK	O	**Frame Control** In an LCD interface, it is an AC signal which is toggled every frame. In a CRT interface, it is the $\overline{\text{BLANK}}$ signal. Some panels call this signal "M."
103 - 100	LD3 - LD0	O	**Lower Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the lower panel data bus. In a Plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAMDAC.
107 - 104	UD3 - UD0	O	**Upper Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the upper panel data bus. In a Plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

*The display interface functions are redefined for each display mode – see Table 2-1 on page 4 for details.

PIN	MNEMONIC	I/O	DESCRIPTION
			RAMDAC INTERFACE
92	$\overline{\text{RPLT}}$ /	O	**Read Palette** Video DAC register and color palette read signal. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H. This line is active in both internal and external RAMDAC configurations.
	VD9		**Video Data Bit 9** In color TFT mode, this is the ninth data bit of the LCD interface.
93	$\overline{\text{WPLT}}$	O	**$\overline{\text{Write Palette}}$** Video DAC register and color palette write signal. Active low during an I/O write to addresses 3C6H-3C9H. This line is active in both internal and external RAMDAC configurations.
111	VREF	I	**Voltage Reference Input** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC. Grounding this pin changes the function of pin 112 and disables the internal RAMDAC so that the WD90C20 can be used with an external RAMDAC.
112	MDETECT/	I	**Monitor Detect** When pin 111 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2H Bit 4.
	FSADJUST		**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DAC's.
114	BLUE	O	**Blue Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
115	GREEN	O	**Green Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
116	RED	O	**Red Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
			POWER AND GROUND
9,28, 53, 67, 94	Vcc	-	**Power**
10,18, 27,37,54, 66,76,85, 95	GND	-	**Ground**
123	AVcc	-	**+ 5VDC -** ANALOG (See Figure 4-2)
113	AGND	-	**Ground** - ANALOG (See Figure 4-2)
108	RVcc	-	**RAMDAC power** (See Figure 4-2)
	RGND	-	**RAMDAC ground** (See Figure 4-2)

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

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PIN	WD90C20	WD90C20A
	Pullup/Pulldown Type	Pullup/Pulldown Type
SD [15:0]	PU	
LA [19:17]	PD	
SA [16:0]	PD	PD
MEMEN	PD	PD

PU = 100K Ohm Nominal, PD = 200K Ohm Nominal

MEMORY DATA LINE	POWERUP FUNCTION	DATA STORED AT NAME	PORT
MD15	EGA SW4 / LCD Select*	PR11(7)**	3?5.2A.7
MD14	EGA SW3	PR11(6)**	3?5.2A.6
MD13	EGA SW2	PR11(5)**	3?5.2A.5
MD12	EGA SW1	PR11(4)**	3?5.2A.4
MD11	ANALOG/TTL Display	PR5(3)**	3CF.0F.3
MD10	–	–	–
MD9	Panel Select Bit 1	PR18(1)**	3?5.31.1
MD8	Panel Select Bit 0	PR18(0)**	3?5.31.0
MD7	General Purpose	PR5(7)***	3CF.0F.7
MD6	General Purpose	PR5(6)***	3CF.0F.6
MD5	General Purpose	PR5(5)***	3CF.0F.5
MD4	General Purpose	PR5(4)***	3CF.0F.4
MD3	VCLK1,2 (I/O)	None**	–
MD2	AT/Micro Channel Mode	None**	–
MD1	–	PR1(1)***	3CF.0B.1
MD0	BIOS ROM Mapping	PR1(0)***	3CF.0B.0

TABLE 4-2. PR REGISTER FUNCTIONS

NOTES:
Data lines MD0 - MD15 are pulled up or down with resistors to provide setup information on powerup (reset) as shown above.

* PR11(7) = 0 : mono LCD, PR11(7) = 1 : color LCD.
** Pullup resistor sets these bits to logic 1.
*** Pulldown resistor sets these bits to logic 1.

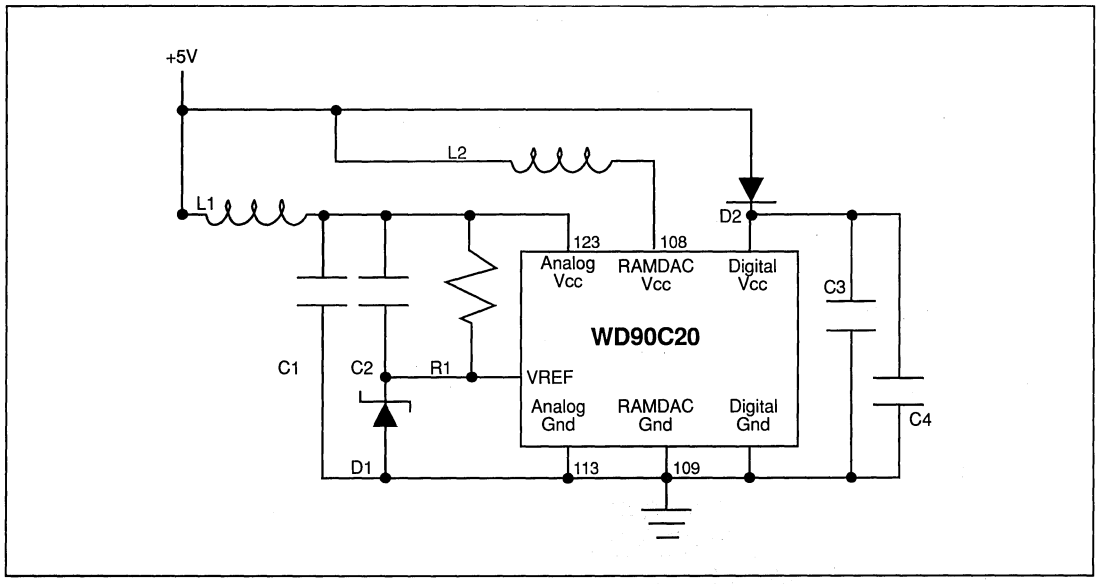

FIGURE 4-2. POWER DISTRIBUTION FOR WD90C20

COMPONENT	RECOMMENDED COMPONENT VALUE	SUGGESTED PART NUMBER/ COMMENTS
C1	0.1 UF	Reduces noise in analog portion of chip.
C2	0.1 UF	Stablizes VREF voltage.
C3	5 by 0.1 UF One each for Pins 9, 28, 53, 67, 94	Reduces noise to the VGA core.
C4	22 UF	Bulk decoupling.
D1	LM385	1.2 volt voltage reference.
D2	MBR150 (MBRL040-SMT) MBR160, or 2 1N5817s in series	Reduces voltage to digital portion of chip (40-50 mA reduction in current)
L1	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to analog portions of WD90C20.
L2	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to RAMDAC. No decoupling capacitor is to be used at Pin 108.

TABLE 4-3. RECOMMENDED COMPONENT VALUE

5.0 WD90C20 REGISTERS

All standard IBM registers incorporated in the WD90C20 are functionally equivalent to the VGA implementation, while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards using the 6845 CRT Controller. This section describes the VGA registers (and the differences between VGA and EGA), as well as the PR registers.

5.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
NOTE: *Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Red Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 5-1. VGA REGISTERS SUMMARY

5.2 COMPATIBILITY REGISTERS

FUNCTIONS	RW[1]	MDA[2]	CGA[2]	AT&T[2]	HERCULES[2]
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
CRTC[3]	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 5-2. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. 6845 Mode Registers.

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5.3 VGA REGISTERS

This section describes the VGA registers.

5.4 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:
1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.4.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

* These bits determine the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz in CRT mode).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz in CRT mode) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

5.4.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

The DAC output currents, I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. For the WD90C20, the output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

For the WD90C20A, the output current is determined by the formula:

$$I = \frac{code \times V_{REF} \times 1.036}{R_{SET}}$$

The results of the monitor detection circuitry is readable at port 3C2H Bit 4. (See Figure B-1) It is important that this output signal be read during active video ouput, not during retrace or any other blanking period.

Bit(3:0)

Reserved.

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5.4.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register Bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.4.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control.
0 = Vsync output enabled.
1 = Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved.

5.5 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to 0.

5.5.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

5.5.2 Reset Register, Read/Write Port = 3C5, Index = 00H

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

5.5.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01H

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection.
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels wide).

Bit 2

Shift Load. Effective only if Bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

5.5.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing to Memory Maps (0-3), respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

5.5.5 Character Map Select Register, Read/Write Port = 3C5, Index = 03H

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 Bit 1 is 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. "0" selects character map B. "1" selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5), and Bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A, along with Bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.
The MSB of character map B, along with Bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit(3:2)

Character Map Select A.
Refer to Bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to Bit 4 table.

5.5.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04H

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0

Reserved.

5.6 CRT CONTROLLER REGISTERS

PORT[1]	INDEX	VGA REGISTER NAME	6845 REG NAME[2]
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	See note 3.
3?5	03	End Horizontal Blanking	See note 3.
3?5	04	Start Horizontal Retrace	See note 3.
3?5	05	End Horizontal Retrace	See note 3.
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	See note 3.
3?5	08	Preset Row Scan	See note 3.
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	See note 3.
3?5	14	Underline Location	See note 3.
3?5	15	Start Vertical Blank	See note 3.
3?5	16	End Vertical Blank	See note 3.
3?5	17	CRTC Mode Control	See note 3.
3?5	18	Line Compare	See note 3.

TABLE 5-3. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   ?= B in monochrome modes.
   ?= D in color modes.

2. 6845 Mode Registers are defined and explained in greater in the reference literature.

3. This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

5.6.1 CRT Address Register, Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

5.6.2 Horizontal Total Register, Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the horizontal total period is the total of the character count in the active display plus the character count in the retrace time less 5, per horizontal scan line.

5.6.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total number of displayed characters less one is programmed into this register.

Horizontal overscan begins when the horizontal character counter reaches this character clock value.

5.6.4 Start Horizontal Blanking Register, Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the hexidecimal value in the character clocks in this register. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.5 End Horizontal Blanking, Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

Bit 7

Reserved.

Bit(6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

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Bit (4:0)

End Horizontal Blanking.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Blanking and the desired width of the horizontal blanking in character clocks. The least significant five bits are programmed into this register, while the sixth most significant bit is the End Horizontal Retrace register (index 05H) Bit 7. When the least significant six bits of the horizontal character counter match these six bits, the horizontal blanking is ended.

5.6.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.7 End Horizontal Retrace Register, Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

Bit 7

MSB (sixth bit) of the End Horizontal Blanking register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Retrace and the desired width of the horizontal retrace in character clocks. The least significant five bits are programmed into this register. When the least significant five bits of the horizontal character counter match these five bits, the horizontal retrace signal is turned off.

5.6.8 Vertical Total Register, Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant 8 bits of a 10-bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) Bit 0 and Bit 5, respectively. In 6845 modes, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H Bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0

Vertical Total Bit 8 (index = 06H).

NOTES:

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register Bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

5.6.10 Preset Row Scan Register, Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

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5.6.11 Maximum Scan Line Register, Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4 - 0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is Bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, Bits 5 through 7 are reserved, and Bits 4 through 0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

5.6.12 Cursor Start Register, Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. They contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, Bit 7 is reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value. Bit 6 is not used.

5.6.13 Cursor End Register, Read/Write, Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks; e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, Bits 7 through 5 are reserved and Bits 4 through 0 contain the row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode; i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

5.6.14 Start Address High Register, Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16-bit video memory address used for screen refresh. The low order 8-bit register is at index 0DH. The PR Register PR3 Bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes Bits 6 and 7 are forced to "0" regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

5.6.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

5.6.16 Cursor Location High Register, Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, Bits 6 and 7 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

5.6.17 Cursor Location Low Register, Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

5.6.18 Vertical Retrace Start Register, Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the 10-bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 through 0 as the light pen read back value, and Bits 6 and 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

5.6.19 Vertical Retrace End Register, Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
These bits specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add the number of scan count for "W" to the value of the Vertical Retrace Start register. The least significant four bits of the result are written in the Vertical Retrace End register. When the least significant four bits of the vertical scan line counter match these four bits, the vertical retrace signal is turned off.

5.6.20 Vertical Display Enable End Register, Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower 8 bits)

Bit(7:0)

Vertical Display Enable End Lower 8 Bits.
The lower eight bits of 10-bit register that defines where the active display frame ends.

The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

5.6.21 Offset Register, Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen Width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or doubleword display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

5.6.22 Underline Location Register, Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

5.6.23 Start Vertical Blank Register, Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the 10-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). The 10-bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

5.6.24 End Vertical Blank Register, Read/write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank Inactive Count.
End Vertical Blank is an 8-bit value calculated as follows:

8-bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) +
(value of vertical blank signal width in scan lines).

When the least significant eight bits of the vertical scan line counter match these eight bits, the vertical blank signal is turned off.

5.6.25 CRT Mode Control Register, Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1-bit and the MSB of the address counter appears on the LSB. See the table on the next page.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

* See Bit 5, defining address wrap. This table is applicable only when PR Register PR1 Bits 7 and 6 equal 0, or PR16 Bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) Bit 6 controls addressing. See the following table.

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.

1 = Select MA15 for odd/even mode when 256 Kbyte of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2.

0 = Character clock increments memory address counter.

1 = Character clock divided by 2 increments the address counter.

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Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter Bit 1 as output at MA14 address pin.
1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller Compatibility Mode Support for CGA Operation.

0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

5.6.26 Line Compare Register, Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower 8 Bits.
Lower 8 bits of the 10-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.7 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE: Reserved bits should be set to 0.

5.7.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.7.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) Bit 1 and Bit 0.

5.7.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

5.7.4 Color Compare Register, Read/Write PORT 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.7.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
This specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

5.7.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. This operation has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 and 1 or value 10b or 11 to select the chained maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

5.7.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode Bit 1
0	Write Mode Bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to 6 bits through internal palette and is sent out on the lower 6-bit pins (VID5 - VID0) every dot clock. The remaining two video outputs (VID6, VID7) are determined by Bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 – Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.

The table below defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the 8 bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.7.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0.
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128 Kbyte
0	1	A000:0H-AFFF:FH	64 Kbyte
1	0	B000:0H-B7FF:FH	32 Kbyte
1	1	B800:0H-BFFF:FH	32 Kbyte

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.7.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

5.7.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

The bit mask operation applies simultaneously to all four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation affects any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.8 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3C0	——	Index Register
3C0	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes.
1 = D in Color Modes.

5.8.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read through address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0, but does not toggle for reads to address 3C1.

5.8.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

BIT	FUNCTION
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

5.8.3 Attribute Mode Control Register, Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line Compare will have no effect on the PEL Panning Register.
1 = Allows a successful Line Compare to disable the PEL Panning Register and also Bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

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Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to 0 for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

5.8.4 Overscan Color Register, Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

5.8.5 Color Plane Enable Register, Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select two out of eight color outputs which can be read by the Input Status Register 1 (port = 03?A) Bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

5.8.6 Horizontal PEL Panning Register, Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 Dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

5.8.7 Color Select Register, Read Port 3C1/Write Port 3C0, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers to create 8-bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

5.9 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.9.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 4

Reserved.

Bit 3

Video Enable.
0 = Video disable.
1 = Video activated.

Bit 2

Reserved.

Bit 1

Port 3BFH Enable.
0 = Prevents setting of Port 3BF Bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh Bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode (should be 1).
0 = High resolution disabled.
1 = High resolution is enabled.

5.9.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its Bits 0 and 1.

5.9.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6,4,2)

Reserved.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF Bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF Bit 0 to switch for the alpha or graphics mode selection.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 3

Video Enable.
0 = Video disable.
1 = Video enable.

Bit 0

High Resolution (should be 1).
0 = High resolution disabled.
1 = High resolution enabled.

5.9.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) Bit 7 selects the displayed memory page address in the graphics mode. When it is reset, Bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) Bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.9.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

5.9.6 CGA Color Select Register, Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

5.9.7 CRT Status Register, MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

5.9.8 CRT Status Register, CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

5.9.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to 0 by reset. This register is enabled by setting Bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

5.10 WD90C20 PR REGISTERS

NAME	RW [1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0A(6:0)	3CF.09	5.10.1
Alternate Address Offset B	RW	PR0B(6:0)	3CF.0A	5.10.1
Memory Size	RW	PR1(7:0)	3CF.0B	5.10.2
Video Select	RW	PR2(7:0)	3CF.0C	5.10.3
CRT Control and Group Locking	RW	PR3(7:0)	3CF.0D	5.10.4
Video Control	RW	PR4(7:0)	3CF.0E	5.10.5
Unlock PR0-PR4	RW	PR5(7:0)	3CF.0F	5.10.6
Unlock PR11 - PR17	RW	PR10(7:0)	3?5.29[4]	5.10.7
EGA Switches	RW	PR11(7:0)	3?5.2A	5.10.8
Scratch Pad	RW	PR12(7:0)	3?5.2B	5.10.9
Interlace H/2 Start	RW	PR13(7:0)	3?5.2C	5.10.10
Interlace H/2 End	RW	PR14(7:0)	3?5.2D	5.10.11
Miscellaneous Control 1	RW	PR15(7:0)	3?5.2E	5.10.12
Miscellaneous Control 2	RW	PR16(7:0)	3?5.2F	5.10.13
Miscellaneous Control 3	RW	PR17(1:0)	3?5.30	5.10.14
Flat Panel Status	RW[5,6]	PR18(7:0)	3?5.31	5.10.15
Flat Panel Control I	RW	PR19(7:0)	3?5.32	5.10.16
Flat Panel Control II	RW	PR1A(7:0)	3?5.33	5.10.17
Flat Panel Unlock	RW	PR1B(7:0)	3?5.34	5.10.18
Mapping RAM Unlock	RW	PR30(7:0)	3?5.35	5.10.19
Mapping RAM Address Counter	RW	PR33(7:0)	3?5.38	5.10.20
Mapping RAM Data	RW	PR34(7:0)	3?5.39	5.10.21
Mapping RAM Control	RW[6]	PR35(1:0)	3?5.3A	5.10.22
LCD Panel Height Select	RW	PR36(7:0)	3?5.3B	5.10.23
Flat Panel Blinking Control	RW	PR37(7:0)	3?5.3C	5.10.24
Color LCD Control	RW	PR39(7:0)	3?5.3E	5.10.25
Vertical Expansion Initial Value	RW	PR41(7:0)	3?5.37	5.10.26
PR43 Unlock Register	WO	PR42(7:0)	3C5.06	5.10.27
Paradise VGA Status	RW	PR43(7:0)	3C5.07	5.10.28
Power-Down Memory Refresh	RW	PR44(7:0)	3?5.3F	5.10.29
CNF Configuration	HARD[6]	–	–	5.13

TABLE 5-4. PR REGISTERS SUMMARY

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. In the PR register notation, XXX.YY, XXX is the data port address and YY is the register index.
3. All register addresses are in hex.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. The register bits (1:0) are loaded as CNF (10:9) upon reset.
6. Not all bits are readable.

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The WD90C20 has additional features that enhance the performance and function of the Western Digital Imaging WD90C00 and basic VGA subsystem.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write-protected at power-up by the hardware reset. In order to load these registers, the appropriate unlock register, PR5 or PR10, must be loaded first with binary XXXXX101; the register remains unlocked until any other value is written to it. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power-up by hardware reset. To read registers PR10 through PR17, load PR10 with 1XXX0XXX. The registers remain readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them shows data to be FFH. Setting PR4 Bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power-on reset except where noted.

5.10.1 Address Offset Registers, PR0A & PR0B

PR0A - Address Offset Register A, Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B, Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C20 can control up to 1 Mbyte of video RAM. However, the memory map for IBM PC and compatibles assigns 128 Kbytes of the available 1 Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. This space is further limited to a 64 Kbyte video memory partition to allow a second video card to co-exist.

The WD90C20 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 Bit 3 is set to 1. PR0A and PR0B provide a 7-bit offset that is added to address Bits A (18:12) of the system address to form a 20-bit address. The arrangement is similar to that of the segment register DS and ES of the 8088/80X86 architecture, with PR0A and PR0B providing 4 Kbyte segments.

In a 64 Kbyte VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), when PR0B is enabled by setting PR1 Bit 3 = 1, PR address offset registers, PR0A and Alternate Offset Address register (PR0B), may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H–AFFF:FH while PR0B is mapped from A000:0H–A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register Bits 3 and 2) and the Alternate Offset register is enabled, PR0A is mapped from B000:0H-BFFF:FH, while PR0B is mapped from A000:0H-AFFF:FH.

5.10.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map Select
3	Enable Alternate Address Offset Register PROB
2	16-Bit Video Memory
1	Reserved
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1 (1:0) are latched internally at power-on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6
Memory Size.

256 Kbyte of available VGA video memory space is divided into four 64 Kbyte maps (0-3), each defining bit planes (0-3). In mode 13, the 4-bit planes are chained to form one large bit plane. The starting address of the 256 Kbyte video memory buffer can be configured to match other video adapters and/or application programs. WD90C20 enhances memory size capability when Bits 6 and 7 are programmed to extend video buffer size to 512 Kbyte or 1024 Kbyte.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64 Kbyte by 4	N/U	256 Kbyte	4 (64 Kbyte Per Plane)
64 Kbyte by 4	BANK SELECT	512 Kbyte	4 (128 Kbyte Per Plane)
256 Kbyte by 4	DRAM PIN A8	1024 Kbyte	4 (256 Kbyte Per Plane)

The DRAM organizations supported by the WD90C20 and its associated video space are shown in the table at the bottom of the page.

When video memory size is 512 Kbyte, and 64 Kbyte by 4 DRAMs are used, two banks of 64 Kbyte form 128 Kbyte per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the CAS10N and CAS32N signals. Four planes form the desired 512 Kbyte video memory space. For 1024 Kbyte video memory size, MA8 is directly connected to the A8 address pin of the 256 Kbyte by 4 DRAMS, and two DRAMS form a 256 Kbyte space per plane. Four planes make the desired 1024 Kbyte video memory space.

PR1 Bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is the same as IBM VGA regardless of PR1 (6) and PR1(7)

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 Kbyte Standard VGA	VGA*
0	1	0	256 Kbyte WDI VGA	PVGA**
1	0	0	512 Kbyte WDI VGA	PVGA
1	1	0	1024 Kbyte WDI VGA	PVGA
X	X	1	Any Of The Above	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
**WDI extended modes can fully utilize up to 256 Kbytes.

RAM ADDRESSING:
PR1(7) PR1(6)
0 0 256 Kbyte Total; 64 Kbyte Plane; IBM VGA Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(50)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:
PR1(7) PR1(6)
0 1 256 Kbyte Total; 64 Kbyte Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 0 512 Kbyte Total; 128 Kbyte/Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
*						
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 1 1024 Kbyte Total In 4 Planes; 256 Kbyte/Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16) *	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:
1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 Bit 3 or Bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 Bit 5 = 0.

BIT 5	BIT 4	MEMORY MAP
0	0	VGA Mapping in 64 Kbyte space - A000:0H to BFFF:FH Address Range
0	1	First 256 Kbyte in 1 Mbyte space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 Kbyte in 1 Mbyte space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 Kbyte in greater or equal to 1 Mbyte space - 0000:0H to FFFF:FH Address Range

Bit 3

Enable Alternate Address Offset Register PR0B.

Bit 2

Enable 16-Bit Bus for Video Memory.
When set to 1, DS16N will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ inactive.

Bit 1

Reserved. Set to 0.

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-up resistor latches 0 after power-up. A pull-up on MD(0) sets this bit to 0 at power-on reset.

5.10.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register and Mode.

Bit 6

0: VGA or EGA mode.
1: Non-VGA (6845) mode.

Bit 5

Character Map Select.
The following functions are overridden by setting PR15(2). This bit, in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected according to the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE: Setting PR15(2) = 1, i.e., selecting "page mode addressing" overrides the "plane selected" table shown above.

Bit(4:3)

Character Clock Period Control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE: The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and Character Map Select.
Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., Programming 1 gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are available. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, setting this bit locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK. Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

5.10.4 PR3 - CRT Lock Control Register, Read/Write Port=3CF, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e., the IBM Vertical Retrace End Register Bit 7 controlled by index register 11). When Bit 7 is 1, CRT controller registers (R0-7) are write protected by VGA definition. Information on the five groups, and their locking schemes, is provided below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1.
CRT Controller Register 00
–Horizontal Total Characters per scan
CRT Controller Register 01
–Horizontal Display Enable End
CRT Controller Register 02
–Start Horizontal Blanking
CRT Controller Register 03
–End Horizontal Blanking
CRT Controller Register 04
–Start Horizontal Retrace
CRT Controller Register 05
–End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1.
CRT Controller Register 07(Bit6)
–Vert. Display Enable End bit 9
CRT Controller Register 07(Bit1)
–Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1.
CRT Controller Register 06
– Vertical Total
CRT Controller Register 07(Bit7)
–Vertical Retrace Start bit 9
CRT Controller Register 07(Bit5)
–Vertical Total bit 9
CRT Controller Register 07(Bit3)
–Start Vertical Blank bit 8
CRT Controller Register 07(Bit2)
–Vertical Retrace Start bit 8
CRT Controller Register 07(Bit0)
–Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1.
CRT Controller Register 09(Bit5)
–Start Vertical Blank bit 9
CRT Controller Register 10
–Vertical Retrace Start
CRT Controller Register 11 [Bits(3:0)]
–Vertical Retrace End
CRT Controller Register 15
–Start Vertical Blanking
CRT Controller Register 16
–End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1.
CRTC mode Control Register 17(Bit2)
–Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 Bit 7.

Bit 6

Lock HSYNC polarity, as programmed in 3C2 Bit 6.

Bit 5

Lock Horizontal Timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 Bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address register values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 Bit 7=1.

Bit 0

Lock Vertical Timing.
1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 Bit 7=0.

5.10.5 PR4- Video Control Register, Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register Control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$.
Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. One of two types of display enable timings can be selected; the choice is determined by PR15(1).

Bit 6

Select PCLK Equal to VCLK.
0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

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Bit 4

Tri-state the Memory Control Outputs.
The memory address bus, MA(8:0), and all ten DRAM control signals, are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" Bit 3 of mode register 3D8, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal Palette and Overscan Registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) Bit 1 is 0) 3C0 register is read/write while 3C1 register is read only, according to the Attribute Controller register definitions.

Bit 0

Shift Register Control.
This bit configures the video shift registers for 256-color mode.

5.10.6 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 through PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register Bits 4 through 8. Setting PR(4) Bit 1 to 1 read protects registers PR0 through PR5.

BIT	FUNCTION
7	CNF(7) [READ ONLY]
6	CNF(6) [READ ONLY]
5	CNF(5) [READ ONLY]
4	CNF(4) [READ ONLY]
3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits are cleared to 0 by reset. They control writing to PR registers PR0 through PR4 as follows:

2	1	0	PR0-PR4
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected

5.10.7 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29H

This register is READ/WRITE and cleared to 0 by reset. PR10 can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10 through PR17. Bits 7 and 3 enable register read operation for PR10 through PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for Manufacturing Test

5.10.8 PR11 EGA Switches Read/Write Port = 3?5, Index = 2AH

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA configuration switches SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	WRITE 3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

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Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible analog) display.

Bit 2

Lock Clock Select.
This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer Screen Control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller and Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during a read operation.

Bit 0

Lock 8/9 Dots.
Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 Bit 0. Although 8 or 9 character timing is locked by setting PR11 Bit 0 to 1, the 3C5.01 Bit 0 appears unlocked to the system processor during reads.

5.10.9 PR12 Scratch Pad
Read/Write Port = 3?5, Index = 2BH

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

5.10.10 PR13 Interlace H/2 Start
Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00). The equation is as follows:

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE: HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.10.11 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2DH

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ.
This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in Micro Channel operation.

Bit 6

Vertical Double Scan.
This bit should be set to 1 when emulating EGA on a PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. The relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is as follows:

$$N=2(n+1)$$

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced Mode.
Setting this bit to 1 selects interlaced mode. Interlaced mode can be used in video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 End Bits (4:0).
Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

5.10.12 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2EH

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8H.
This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

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Bit 6

Low VCLK.
Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ) >2

Bit 5

Latched VCLK1 and VCLK2.
This bit is used only if CNF(3) = 1 (which configures the VCLK1 and VCLK2 pins as outputs). Setting this bit to 1 causes outputs VCLK1 and VCLK2 to equal Bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H, respectively.

Bit 4

Select MCLK as Video Clock.
Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs cannot be selected when this bit is set.

Bit 3

Interlaced Compatibility.
This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.

Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing.
Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory (by 30-40%). Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8 Kbyte memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register, while the map selection is determined by the bits (4:3). A pair of adjacent 8 Kbyte character maps in planes 2 and 3 (adjacent in the sense that they have the same addressing), may be selected by Bit 3 of the attribute code.

The Character attribute Bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE: The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to choose between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0= BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable Border.
Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

5.10.13 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H Register.
Setting this bit to 1 causes EBROMN output to be forced high (inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.
Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64 Kbyte or 128 Kbyte locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512 Kbyte or 1024 Kbyte of video memory in which the CRT controller is limited to only 64 Kbyte or 128 Kbyte locations. Bit PR16(6) should be set to 1 to ensure that the VGA and EGA compatible operation of the address counter is limited to 64 Kbyte locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256 Kbyte
0	1	128 Kbyte
1	X	64 Kbyte

Bit (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively. The 2-bit result defines the starting location of the displayed video buffer at one of the four 64 Kbyte boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

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Bit 1

VGA Memory Mapping.
Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC Write Strobe (3C6H - 3C9H).
Programming this bit to 1 causes output WPLTN to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C20, is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

5.10.14 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

This 2-bit register can be loaded only if PR10 (3?5.29) contains XXXXX101. It can be read only if PR10 contains 1XXX0XXX, and if both PR1B (7:5) is not 101 and PR30 (6:4) is not 011.

BIT	FUNCTION
(7:2)	Reserved
1	MDA Compatibility
0	Map Out 2 Kbyte From BIOS ROM

Bit (7:2)

Reserved.

Bit 1

MDA Compatibility Enable Bit.
Setting this bit to 1 enables MDA compatibility which will:

1. Disable I/O write to Hercules register 3BF.
2. Force Bit 7 of 3BA to 1.
3. Select underline decode of attribute XXXXX001 (if this bit is 0, underline decode is X000X001).

Reset sets this bit to 0.

Bit 0

Map Out 2 Kbyte of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C6000H – C67FFH. Power-on-reset sets this bit to 1. Clearing this bit to 0 enables access to all 32 Kbyte addresses of the BIOS ROM from CC000H – C7FFFH.

5.10.15 PR18 Flat Panel Status Register Read Write Port = 3?5, Index = 31

Bit 7

DAC shut-off.
0 = the built-in DAC is enabled as normal.
1 = the built-in DAC is forced off.
(This bit is used for the WD90C20A only)

Bit 6

Reserved.

Bit 5

Reserved.

Bit 4 (WD90C20A)*

Enable Reverse Video in Flat Panel Mode.
This bit controls reverse video in text mode and normal video in graphics mode and is used to reverse the polarity of the video output data UD(3:0) and LD (3:0).

– For WD90C20A:
If PR18 (4) = 0, then only normal video displayed.
If PR18 (4) = 1 and PR39 (3) = 0, then reverse video is displayed in both text and graphics modes.
If PR18 (4) = 1 and PR39 (3) = 1, then reverse video is displayed only in text mode, while normal video is displayed in graphics mode.

PR39 (3)	PR18 (4)	TEXT	GRAPHICS
X	0	Normal	Normal
0	1	Reverse	Reverse
1	1	Reverse	Normal

x=don't care
* This feature is not available for WD90C20

Bit 3

Reserved.

Bit 2

TFT Color LCD Select.
This bit is not readable.
0 = Disable TFT type color LCD panel interface.
1 = Enable TFT type color LCD panel interface.

Bit(1:0)

Panel Select Bit 1 and Bit 0.
These two bits are used to select different sets of parameters which will be loaded into the CRT controller. The parameters should be locked after loading.

PSB (1)	PSB(0)	PANEL TYPE
0	0	Dual Panel LCD Display
1	0	EL Display
1	1	Single Panel LCD Display

5.10.16 PR19 Flat Panel Control Register, Read/Write Port = 3?5, Index 32

BIT	FUNCTION
7	Reserved
6	FP Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Auto-Centering/Vertical Expansion Select
2	Enable Auto Centering and Vertical Expansion
(1:0)	Adjustment of HSYNC Timing

Bit 7

Reserved.

Bit 6

FP Timing Select.
This bit is used to select two different frame pulse (FP) timings for different LCD panels.
0 = Select ON time during first horizontal line.
1 = Select ON time during second horizontal line.

Bit 5

CRT Display Enable.
This bit enables CRT to be the display device.
0 = Disable CRT display.
1 = Enable CRT display.
NOTE: Upon hardware reset, PR19 (5) =0

PR18(1)	PR18(0)	PR19(5)	PR19(4)	CRT CONTROLLER (TIMING)
0	0	0	1	Based on LCD
0	0	1	0	Based on CRT
0	1	1	0	Based on CRT
1	0	0	1	Based on EL
1	0	1	0	Based on CRT

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Bit 4
Flat Panel Display Enable.
This bit enables the flat panel as the display device.
0 = Disable Flat Panel display.
1 = Enable Flat Panel display.

The WD90C20A supports simultaneous display of both a CRT and single-panel color LCD with vertical expansion and autocentering. The following table shows the LCD/CRT polarity in various modes.

DISPLAY MODE	LBDIR
CRT only	H
Flat panel only	L
Simultaneous display	L

Notes:
1. Upon hardware reset, PR19 (4) = 1
2. When the flat panel display is not enabled, the outputs UD (3:0) and LD (3:0) are active and may be used as the pixel address to drive an external RAMDAC.
3. For simultaneous display of CRT and certain flat panel, set PR19 (5:4) = 11. In this case, the display is locked in 8-dot clock mode and the output -LCD/CRT = 0. The following flat panel may be displayed simultaneously with a CRT: plasma, TFT LCD, and color STN LCD.

Bit 3 (WD90C20A only)*
Screen Autocentering/Vertical Expansion Select.
0 = Autocentering (default).
1 = Reserved for Vertical Expansion (set to 0).
* This feature is not available for WD90C20.

Bit 2
Enable Autocentering and Vertical Expansion.
0 = Disable (default).
1 = Enable.

NOTE: This is used only for pulse wave modulation on the LCD panel.

Bit (1:0) (WD90C20A only)*
Adjustment of HSYNC timing.

PR19(7), PR19(1), and PR19(0) are used to select number of VCLK delays to adjust the HSYNC timing.
* This feature is not available for WD90C20.

PR19(7)	PR19(1)	PR19(0)	NUMBER OF VCLK DELAY
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.10.17 PR1A Flat Panel Control II Register, Read/Write Port 3?5, Index = 33

BIT	FUNCTION
(7:6)	Select IOCHRDY Release Timing in CPU Memory Read Cycle
(5:4)	Select IOCHRDY Release Timing in CPU Memory Write Cycle
3	Enable CGA Color to Gray Scale Adjustment
2	Shading Method Select
1	Select Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit(7:6)

Select IOCHRDY Release Timing in CPU Memory Read Cycle.

BIT 7	BIT 6	RELEASE TIMING
0	0	1 MCLK before CPU completes read cycle
0	1	2 MCLKs before CPU completes read cycle
1	0	3 MCLKs before CPU completes read cycle
1	1	4 MCLKs before CPU completes read cycle

Bit (5:4)

Select IOCHRDY Release Timing in CPU Memory Write Cycle

BIT 5	BIT 4	RELEASE TIMING
0	0	1 MCLK before CPU completes write cycle
0	1	2 MCLK delay after CPU wins arbitration
1	0	3 MCLK delay after CPU wins arbitration
1	1	4 MCLK delay after CPU wins arbitration

Bit 3

Enable CGA Color to Gray Scale Adjustment.
This bit is used to add adjustment of weighting equation in CGA mode to get 16 different gray scale codes.
0 = Disable.
1 = Enable.

NOTE: For VGA, bit should be set to 0.

Bit 2

Shading Method Select.
0 = Frame rate modulation (default).
1= Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.
0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.
0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by PR1A(1).

5.10.18 PR1B Flat Panel Unlock Register, Read/Write Port 3?5, Index = 34

This register is used to protect PR18, PR19, PR1A, PR 30, PR36 through PR41, and PR44 from being read from or written into. In order to unprotect (read or write) the above registers, PR1B must be first loaded with 101XXXXX. The above registers remain unprotected until another value is written into PR1B.

PR1B is also used to lock all Shadow registers. To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

In WD90C20A upon hardware reset, PR1B is initialized to 101XX110, and the Shadow registers PR18, PR19, PR1A, PR30, PR36 through PR41, and PR44 are unprotected.

5.10.19 PR30 Mapping RAM Unlock Register, Read/Write Port = 3?5, Index = 35

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with X011XXXX; all mapping RAM registers remain unlocked until another value is written to the PR30 register.

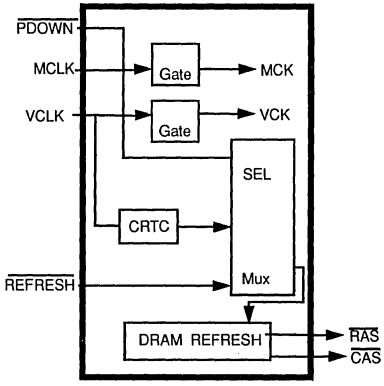
5.10.20 PR33 Mapping RAM Address Counter Register, Read/Write Port = 3?5, Index = 38

This register is used to select the RAM ADDRESS COUNTER register.

NOTE: Any I/O Read or Write to the I/O port 3?5.39H (Mapping RAM Data register) will increment the Mapping RAM Address Counter by one.

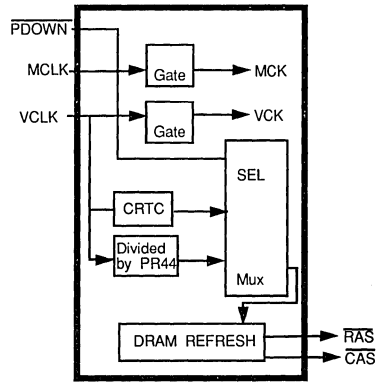
5.10.21 PR34 Mapping RAM Data Register, Read/Write Port = 3?5, Index = 39

This register is used to select the RAM data register for memory read or memory write.



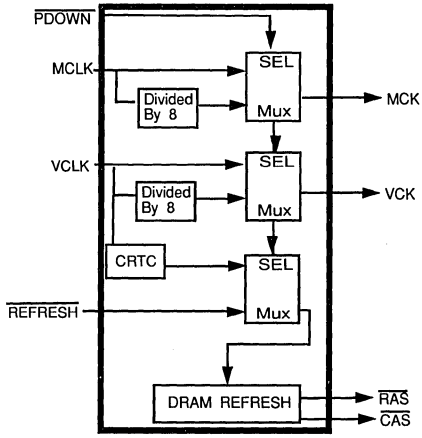
SYSTEM POWER DOWN MODE (SLEEP)

A. RAMDAC is off.
B. Clock inputs are turned off as they enter the chip.
C. CAS before RAS video memory refresh is generated from REFRESH input.
D. Neither video memory or I/O can be accessed in this mode.
E. RAMDAC and Mapping RAM contents are lost and must be reloaded to resume.



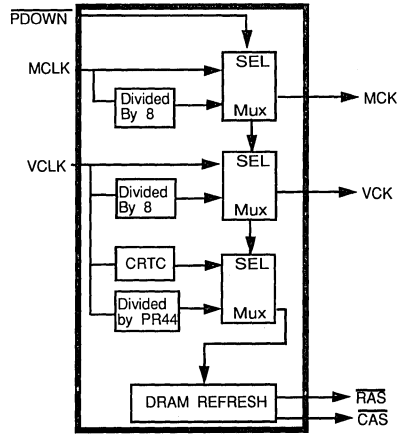
GENERAL POWER DOWN MODE (EXTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are not modified; their speed is reduced by system resources.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS.
D. Video memory and I/O are accessable.



DISPLAY IDLE MODE (SUSPEND/RESUME)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh is CAS before RAS and generated by REFRESH input.
D. I/O is accessable and memory is not accessable.



GENERAL POWER DOWN MODE (INTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS. PR44 can be RAS only.
D. Video memory and I/O are accessable.

FIGURE 5-1. SYSTEM POWER DOWN-MODE DISPLAY IDLE MODE

PR44(7)	PR35(7)	PR35(6)	MODE
0	1	X	System Power-Down Mode: MCLK and VCLK are turned off. Video memory refresh is generated from PDREF. Neither memory nor I/O can be accessed. RAMDAC and Mapping RAM must be reloaded.
0	0	X	Display Idle Mode: MCLK and VCLK are divided by 8 before being distributed across the chip. Video memory refresh is generated from PDREF. Only I/O can be accessed.
1	X	0	General Power-Down (External Clock Used): MCLK and VCLK inputs are used to drive the chip . The assumption is made that MCLK and VCLK have been reduced by some other part of the system. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.
1	X	1	General Power-Down (Internal Clock Used): MCLK and VCLK inputs are divided by 8 before being distributed across the chip. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.

5.10.22 PR35 Mapping RAM and Power-Down Control Register, Read/Write Port = 3?5, Index = 3A

BIT	FUNCTION
7[1]	Select System Power-Down Mode/Display Idle Mode
6[1]	Select Internal Divided By 8 Clock to Control General Power-Down Mode
5[1]	Host Release Control
4[1]	Reserved; set to 1.
3[1]	Reserved
2[1,2]	Enable $\overline{CAS}$ before $\overline{RAS}$ Memory Refresh Cycle
1	Enable Weighting Equation
0	Reserved; set to 1.

[1] Readable only in WD90C20A when PR30=X011XXXX.

[2] Used in WD90C20A only.

Bit 7

Select System Power-Down Mode/Display Idle Mode. Refer to Figure 5-1. This bit is not readable.

0 = Display idle mode (default).

1 = System power-down mode; MCLK and VCLK turned off.

Bit 6

Select Internal Divided by 8 Clock to Control General Power-Down Mode. This bit is active only when PR44(7) is set at 1. This bit is not readable.

0 = Disable internal clock.

1 = Enable internal clock; clock is divided by 8.

Bit 5

Host Release Control.

This bit is designed to allow another VGA controller in the I/O bus. When PR35(5) is set to 1 and PDOWN input is set to 0, the WD90C20 will not respond to any CPU memory or I/O accesses. All

output buffers of the system interface are turned off (tristate).

There are four power-down modes. The following conditions are true in each powerdown mode.
1. Video memory is maintained.
2. RAMDAC outputs are turned off.
3. Panel outputs are turned off.

Bit 4

Reserved. This bit is set at 1.

Bit 3

Reserved.

Bit 2 (WD90C20A)*

Enable CAS before RAS Memory Refresh Cycle.
0 = $\overline{RAS}$ only refresh cycle (default).
1 = $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
* This bit is used in WD90C20A only.

Bit 1

Enable Weighting Equation.

This bit is used to turn the IBM VGA weighting equation on and off in either color mode or monochrome mode.
0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved. This bit is set at 1.

5.10.23 PR36 Panel Height Select Register, Read/Write Port = 3?5, Index = 3B

This register is loaded with the height, less 1, of a single panel. This information is used to calculate autocentering, vertical expansion, and related values. In a 640 by 480 dual panel display, this register should be loaded with "EF". (480/2)-1 = 239_{10} = EFH. In a 640 by 400 dual panel display, the equation is: (400/2)-1 = 199_{10} = C7H.

5.10.24 PR37 Flat Panel Blinking Control, Read/Write Port = 3?5, Index = 3C

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

BIT	2	1	0	CURSOR BLINKING RATE SELECT
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
BIT	**5**	**4**	**3**	**CHARACTER BLINKING RATE SELECT**
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
BIT	**6**			**PLASMA SHIFT CLOCK SELECT**
	0			Select falling edge of the clock to latch data
	1			Select rising edge of the clock to latch data
BIT	**7**			**LCD LP SIGNAL SELECT**
	0			LP will be disabled during vertical blanking period
	1			LP will be generated continuously during vertical blanking period (SCLK will be turned off)

5.10.25 PR39 Color LCD Control Register, Read/Write Port = 3?5, Index = 3E

This register is used to support color LCD panel.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Panel
4	Micro Channel Interface
3	Enable Reverse Video
2	Enable CRT VSYNC and HSYNC
1	FP Polarity Select
0	LP Polarity Select

Bit 7

Enable Border LP Control.
This bit is used to generate a special LP pulse to latch border information (black or white).
0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select.
0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel.
This bit is used to select monochrome LCD or color LCD.
0 = Disable color LCD panel select.
1 = Enable color LCD panel select.

Bit 4

Enable Micro Channel Interface Enhancement.
This bit is used to select Micro Channel interface.
0 = Select default I/O cycle.
1 = Select synchronous-extended I/O cycle.

Bit 3

Enable Reverse Video.
See PR18 (4)

Bit 2 (WD90C20A)*

Enable CRT VSYNC and HYSNC
If PR39 (2) = 0, then LBDIR pin=LBDIR signal and HBDIR pin=HBDIR signal.
* This bit is used in WD90C20A only.

If PR39 (2) = 1, then LBDIR pin=CRT VSYNC signal and HBDIR pin=CRT HSYNC signal.

PR39 (2)	LBDIR	HBDIR
0	LBDIR	HBDIR
1	CRT VSYNC	CRT HSYNC

When the TFT panel is enabled, the polarities of CRT VSYNC and CRT HSYNC are now pulsed low, regardless of the values programmed in the Miscellaneous Output Register Bit 7 and Bit 6 in PR11(3).

Bit 1 (WD90C20A)*

FP Polarity Select.
If PR39 (1) = 0, then FP has normal polarity.
If PR39 (0) = 0, then FP has reverse polarity.
* This bit is used in WD90C20A only.

Bit 0 (WD90C20A)*

LP Polarity Select.
If PR39 (0) = 0, then LP has normal polarity.
If PR39 (0) = 1, then LP has reverse polarity.
* This bit is used in WD90C20A only.

PR39(1)	FP	PR39(0)	LP
0	Normal	0	Normal
1	Reverse	1	Reverse

5.10.26 PR41 Vertical Expansion Initial Value Register, Read/Write Port = 3?5, Index = 37

Reserved.

5.10.27 PR42 – PR43 Unlock Register, Write Only Port = 3C5, Index = 06

This register locks the PR VGA Status register. In order to read/write to the PR VGA status register (PR43), PR42 must be loaded first with X1X01XXX; PR43 will remain unlocked until another value is written to PR42.

5.10.28 PR43 PR VGA Status Register, Read/Write Port = 3C5, Index = 07

This register is used to indicate the current status of the PR VGA chip and to enhance programming compatibility.

BIT	FUNCTION
(7:4)	Read/Write Scratch Pad Bits
3	Color/Monochrome Emulation Status
2	Mode Type
1	EGA Compatibility Set
0	Display Type

Bit(7:4)

Read/Write Sctatch Pad Bits.
These four bits are available for temporary data storage.

Bit 3

Color/Monochrome Emulation Status.
Read only, Bit 0, of Miscellaneous Output register (3C2).
0 = Monochrome emulation is enabled.
1 = Color graphic emulation is enabled.

Bit 2

Mode Type.
Read only, Bit 6 of PR2.
0 = Either VGA or EGA mode is enabled.
1 = Non-VGA and non-EGA modes are enabled.

Bit 1

EGA Compatibility Set.
Read only of PR4, Bit 1.
0 = EGA compatibility is disabled.
1 = EGA compatibility and the ability to read PR0 – PR5 registers are enabled.

Bit 0

Display Type.
Read only of PR5, Bit 3.
0 = Analog (VGA-compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

5.10.29 PR44 Power-Down Memory Refresh Control Register, Read/Write Port = 3?5, Index = 3F

This register controls two power saving features when in the general power-down modes. Bit 7 is used with PR35(7:6) to determine which power-down mode is to be used. With some power-down modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. PR44(6:0) are loaded with a value that modifies the video memory refresh period during power-down.

BIT	FUNCTION
7	General Power-Down Mode Enable
(6:0)	Memory Refresh Cycle Period

Bit 7

General Power-Down Mode Enable Bit.
This bit enables general power-down mode.
0 = Disables general power-down.
1 = Enables general power-down.

Bit(6:0)

Memory Refresh Cycle Period.
These bits are loaded with the value Z, which is used to determine the refresh period when general power-down mode is used. Refresh period = VCLK x 8 x (Z+5). For example, assume:

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1. Two memory refresh cycles are selected during horizontal blanking period in Flat Panel display mode.
2. Each horizontal line has 96 character clocks.
3. MCLK = 36 MHz, VCLK = 25 MHz.
4. PR44 = 8EH.

When in powerdown mode, POWRDN = 0, MCLK = VCLK = 5 MHz.

1. Z = 14.
2. Refresh Cycle = 200 ns x 8 x (14 + 5).
3. Maximum Refresh Period = 200 ns x 8 x (14 + 5 - 7) = 19.2 µs.
4. Refresh Active Time = MCLK x 9 x 2 (cycle) = 200 ns x 9 x 2 = 3.6µs.

5.11 INTERNAL I/O PORTS

5.11.1 AT Mode, Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused.

Bit 4

Setup.
Puts WD90C20 into setup mode where only I/O port 102H is accessible.

Bit 3

I/O and Memory Accesses.
0 = Disable I/O and memory accesses.
1 = Enable I/O and memory accesses.

Bit(2:0)

Unused Internally.
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4 Kbyte pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4 Kbyte pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

5.11.2 Setup Mode Video Enable, (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C20 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C20 after power on in MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the $\overline{\text{CDSETUP}}$ (ALE) signal pin is active low, the WD90C20 is in setup mode and port 102H can be accessed.

5.12 VIDEO RAMDAC PORTS

The WD90C20 incorporates a complete Micro Channel-compatible RAMDAC, as well as the ability to support an optional external RAMDAC. Selection of the internal or external RAMDAC option is based on the state of the VREF pin when reset is de-asserted.

Data from the internal RAMDAC is always written to the data bus, even when the internal RAMDAC is configured for use with external RAMDAC. RPLT may be used as a gate to send data from an external RAMDAC to the data bus.

There are four operation modes for the built-in video RAMDAC:
– Palette Read Mode
– Palette Write Mode
– PEL Mask Mode
– Palette Status Mode

Which mode is activated depends on two conditions: 1) which I/O port is being addressed, and 2) whether a host write or a host read is being executed.

In other words, the registers, albeit at the same I/O port, may have different meanings, depending on the mode in which the color palette is being accessed. Specifically, the register at 03C7 may contain either PEL address or palette status, depending on whether the access is a read or write operation.

When in the Palette Read Mode, the PEL address is to be written into the 03C7 port. The data can then be read out through the SD bus by three successive read operations from the 03C9 port.

When in the Palette Write Mode, the PEL address is to be written into the 03C8 port. The data can then be written into the palette through the SD bus by three successive write operations into the 03C9 port.

During either Palette Read or Palette Write mode, the 03C7 port can be read to obtain the contents of the Palette Status Register. Please see below for more detail on the palette register.

5.12.1 PEL Mask Register, Read/Write Port = 03C6

The 8-bit PEL Mask Register, along with the eight bits of color information from the combination of the attribute controller and the color select register, are ANDed together and become the index into the color lookup table of the RAMDAC during display refresh. The contents of this register have no effect on host access to the lookup table. The host may access this register at any time without disturbing the contents of the lookup table. The contents of this register are undefined after reset.

5.12.2 Palette Status Register/ Palette-Read-MODE PEL Address Register Read/Write Port = 03C7

Palette Status Register (as a Read Port):
The Palette Status Register can be accessed by reading the 03C7 port (read only). Bits 0 and 1 of this register indicate whether the last active operation to the DAC was in Palette Read Mode or in Palette Write Mode. These bits are both 0 if a host write into the port 03C7 is more recent than a host write into the port 03C8. They are both 1 if a host write into the port 03C8 is more recent than a host write into the port 03C7.

Palette-Read-Mode PEL Address Register (as a Write Port):
The host reads data from the color palette RAM by first writing the index of the first location to be read into this PEL Address Register (write only). When this is done, the RAMDAC loads the RAM data specified by the index into an 18-bit holding

DAC ADDRESS	TYPE	REGISTER NAME
3C6H	Read/Write	PEL Mask
3C7H	Read/Write	When written: PEL Address (Read Mode); When read: Palette Status
3C8H	Read/Write	PEL Address (Write Mode)
3C9H	Read/Write	PEL Data Port

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register. The contents of this 18-bit register are read out via three reads from the PEL Data Port. The data read during these reads consists of six bits of color information packaged into the six least significant bits of the port. The two most significant bits of data during these reads are set to zero. The color information is delivered in the sequence: read, green, blue. After the three read cycles have completed, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be read by sets of three reads from the PEL Data Port, 03C9.

5.12.3 Pallette-Write-Mode PEL Address Register Read/Write Port = 03C8

The host writes data from the color palette RAM by first writing the index of the first location to be written into this register. Completed PEL data to be written is then loaded into an 18-bit holding register via three writes to the PEL Data Port. This is accomplished by concatenating the six least significant bits of the data from the three writes. The color information is extracted in the sequence: red, green, blue. When this is done, the RAMDAC loads the contents of the holding register into the palette RAM location indexed by the contents of the PEL Address (write mode) register. After the data has been transferred to the RAM, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be written by sets of three writes to the PEL Data Port.

5.12.4 PEL Data Read/Write Port = 03C9

This port is used to transfer 6-bit PEL data values to and from the palette RAM. The 18-bit palette locations are transferred in the order: red, green, blue.

5.13 WD90C20 CONFIGURATION BITS, CNF

The configuration register, CNF, is not a physical register, but a convenient way to reference the state of the video memory data lines which are latched at reset. These data lines–for the sake of convenience, collectively called the configuration register CNF– provide setup parameters to various areas on the chip.

When the WD90C20 is reset, it latches the state of the video memory data lines. This data provides setup parameters to various areas of the chip. In order to easily reference these individual bits, we collectively refer to them as the configuration register, (CNF). Only fifteen data lines are used in the WD90C20 and the data line MD10 is not used.

CNF (11)

Color/Mono LCD Panel Select.
This bit is latched internally at power-on-reset from corresponding memory data bus pin MD(15), provided with either pull-up or pull-down external resistors. This bit is read from PR11(7), I/O port 3?5.2A bit 7. This bit is affected by writing to 3?5.2A. Pulling up MD(15) causes CNF(11) to be latched high.
0 = Monochrome LCD panels.
1 = Color LCD panels.

CNF (10:9)

Panel Select Bits.
These bits are latched internally at power-on-reset from corresponding memory data bus pins MD(9:8), provided with either pull up or pull down external resistors. They are read only at I/O port 3?5.31 as bits 1:0 and are unaffected by writing to 3?5.31. Pulling up MD(9:8) data bus pin causes CNF (10:9) to be latched high.

CNF(10)	CNF(9)	DISPLAY TYPE
0	0	Dual Panel LCD Display
0	1	
1	0	EL Display
1	1	Single Panel LCD Display

CNF (8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). CNF(8) is unaffected by writing to PR5 (3CF.0F).
0 = Analog (VGA - compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

General Purpose Status Bits.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). They are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

Video Clock Source Control.

This bit cannot be written to or read as I/O port. Pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C20 pins VCLK1 and VCLK2 as inputs or outputs.
0= For inputs.
1= For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of the dot clock is by an internal multiplexor. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. VCLK1 and VCLK2 outputs are equal to Bits 2 and 3 of the Miscellaneous output register at 3C2H, respectively, when PR15 Bit 5 is set to 1.

CNF (2)

Bus Architecture Select.
This bit cannot be written to or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.
0 = Micro Channel architecture.
1 = AT BUS architecture.

Selecting CNF(2) will change the pinout definition between AT bus and Micro Channel bus. Refer to the pinout description.

PC AT BUS	I/O	MC	I/O
$\overline{\text{MEMCS16}}$	OUT	$\overline{\text{CDDS16}}$	OUT
IOCHRDY	OUT	CDCHRDY	OUT
$\overline{\text{EBROM}}$	OUT	$\overline{\text{CDSFDBK}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MEMR}}$	IN	M/IO	IN
$\overline{\text{MEMW}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
ALE	IN	$\overline{\text{CDSETUP}}$	IN

5.14 MAPPING RAM – 32 by 5 STATIC RAM

The 32 by 5 SRAM is designed for dithering pattern selecting. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM can be read or written to by the CPU. During normal operation, the outputs from the weighting equation (5 bits) will be connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (5 bits) are connected to the dithering logic.

To Write:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock the mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load WRITE starting address register with 00.
OUT 3?4, 39H	Program the index register.
OUT 3?5, 0AH	Write 0A directly to the mapping RAM at location 00.
OUT 3?5, 0BH	Write 0B directly to the mapping RAM at location 01.

To Read:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load READ starting address register with 00.
OUT 3?4, 39H	Program the index register.
IN 3?5	Read directly from the mapping RAM at 00.
IN 3?5	Read directly from the mapping RAM at 01.

NOTE: There is a minimum timing requirement between two consecutive RAM reads or writes (4 x VCLK period). If the system is running faster than 16 MHz, a "NOP" instruction should be inserted between consecutive reads and/or writes.

5.15 SHADOW TIMING REGISTERS

The shadow timing registers control the timing in the CRTC. When the regular timing registers are written to, the shadow timing registers, if unlocked (in CRT mode, they are unlocked), receive the same data. Locking the shadow timing registers is controlled by PR1B.

Timing data is always read from the regular timing registers. The WD90C20 never reads from the shadow timing registers.

In Flat Panel mode, the shadow timing registers are loaded once and then locked by PR1B. Once they are locked, data written to the timing registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

There are eleven shadow timing registers. All are indexed in port 03?5.

NAME	INDEX	SAMPLE VALUE*
Horizontal Total	00H	5FH
Start Horizontal Blanking	02H	50H
End Horizontal Blanking	03H	82H
Start Horizontal Retrace	04H	54H
End Horizontal Retrace	05H	80H
Vertical Total	06H	F2H
Overflow **	07H	00H
Vertical Retrace Start	10H	F0H
Vertical Retrace End	11H	02H
Start Vertical Blank	15H	F0H
End Vertical Blank	16H	F2H

* The sample values are for a monochrome dual panel LCD with 640 by 480 pixels.

** Only bits 7, 5, 3, 2 and 0 are locked by PR1B.

6.0 RAMDAC

6.1 GENERAL DESCRIPTION

The on-board RAMDAC was designed specifically for Personal System/2 compatible color graphics in a laptop computer environment. It integrates the functions of a color lookup table, digital-to-analog converters, power saving features and PS/2 compatible monitor detection logic.

The 256 by 18 color lookup table has triple 6 bit video D/A converters. A pixel mask register and composite blank generation on the three channels are provided. The RAMDAC also supports the use of an external voltage reference.

Without external buffering, the RAMDAC will generate RS-343A compatible video signals into a doubly-terminated 75 ohm load, and RS-170 compatible video signals into a singly-terminated 75 ohm load. Integral and differential linearity errors are a maximum of +/- 1/2 LSB.

The WD90C20A's improved RAMDAC was redesigned to do the following:

- reduce power dissipation
- reduce overshoot and undershoot noise
- reduce ampflier gain error
- improve linearity
- increase yield

6.2 FUNCTIONAL DESCRIPTION

The RAMDAC architecture consists of five major modules:

- Address Register
- Pixel Mask Register
- Color Palette RAM
- Power-Down Control
- Digital-to-Analog Converter (with automatic power-on reset)

Color Palette RAM: There are three 256 by 6 color palette RAMs for the red, green and blue polygun. They provide color information to the triple 6-bit D/A converters. The RAMDAC's color palette RAM memory cell is a custom, power saving cell.

Power-Down Control: The RAMDAC supports an intelligent power-down control sequence. When $\overline{\text{PWRDN}}$ input is low, the entire RAMDAC will enter the "IDLE" state; both the DAC and the color palette RAM will be turned off regardless of the CRT/-LCD signal. When $\overline{\text{PWRDN}}$ input is high in CRT mode, the RAMDAC will operate with the DAC and the color palette RAM always enabled. In LCD mode, when $\overline{\text{PWRDN}}$ input is high, the DAC is turned off. The color palette RAM will be enabled only when the MPU is accessing the RAMDAC because of the intelligent "MPU operation auto-detecting" circuit implemented.

Automatic Power-on Reset: The RAMDAC supports an "automatic poweron-reset" circuit that enables its DAC portion to initialize very quickly after power-on. And, since the DAC is totally turned off in LCD mode, a triggered signal will also initialize the "reset operation" of the DAC during the mode change from LCD mode to CRT mode.

See Section 5.12 and Appendix F for descriptions of RAMDAC registers.

6.3 FEATURES

- Personal System/2 compatible
- Bt471/478 and Bt476 compatible
- Power management features
- On-chip monitor detection logic
- Video signal output into 37.5 or 50 ohms
- 256 by 18 color palette RAM
- Triple 6-bit D/A converters
- Pixel mask register
- Up to 8 bits input per pixel
- RS-343/RS-170 compatible outputs
- 1.25 micron CMOS (WD90C20)
- 0.9 micron CMOS (WD90C20A)

6.4 TEST MODE

The WD90C20A has a new test mode which directly tests the built-in DAC. This allows the DAC to be tested more completely than in the WD90C20 and at the same time more efficiently.

7.0 POWER-DOWN MODES

7.1 SYSTEM POWER-DOWN MODE

7.1.1 Description of System Power-Down Mode (Sleep Mode)

System Power-Down mode is used when the entire system goes to sleep and provides the most power savings. Current requirements for this mode are approximately 4mA. This mode also requires the most system overhead and therefore in addition to being the most miserly in terms of power consumption, it is also the slowest. When the VGA subsystem has been placed in System Power-Down mode, the only activity required of the VGA subsystem is saving the contents of the video display buffer which is accomplished by maintaining refresh of the DRAM. In this mode the system CPU has no access to the display memory nor any access to the I/O of the WD90C20 VGA controller.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Turning off the internal MCLK and VCLK signals.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to WD90C20 I/O registers.
6. Denying the CPU access to video memory.

In System Power-Down mode only the content of the video display buffer is saved which implies that the rest of the dynamic data contained in the VGA subsystem is corrupted. This includes the color content of the RAMDAC palette and the content of the mapping RAM is lost when in this mode.

7.1.2 Entering System Power-Down Mode

To select System Power-Down mode, load bit PR35(7) with "1" (default value is "0"). The WD90C20 will enter a System Power-Down mode cycle when the motherboard power manager drives the "PDOWN" input of the WD90C20 low. After "PDOWN" is driven low, the CPU can not access the WD90C20.

The WD90C20's internal memory and video clocks will automatically be turned off (to save power) after the following time interval: 4 horizontal scan lines PLUS 3 "REFRESH" cycles.

The WD90C20 uses the "REFRESH" input to generate "CAS before RAS" memory refresh cycles which refresh display memory. The internal RAMDAC is also turned off, and display memory refresh is the only WD90C20 activity during this power-down mode. The VCC pins of the WD90C20 must remain powered.

Primary input MCLK may be clocked at the same frequency as VCLK, or may be left at a static "1" or "0". Primary input VCLK must NOT be turned off but may be reduced to as low as 8 KHz. When the VCLK and MCLK frequencies are reduced, they should not be reduced until the following time interval has passed: the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles.

There are several ways to slow down the clocks of the WD90C61. The most effective way is to use the "FCLKIN" input frequency. This is done by driving the "FCLKSEL" input low. "FCLKIN" could be connected to a slow frequency clock which is available on the motherboard.

During the System Power-Down Mode, the "OE10", "OE32", "WE0", "WE1", "WE2", "WE3" and MA(8:0) outputs are all driven high. The memory data bus, MD(15:0), will be in an unknown state. Note that all primary inputs must be driven to either VCC or VSS, as required by the system design. No inputs may be left floating.

7.1.3 Exiting System Power-Down Mode

Before returning to normal display mode, the power manager must first return the WD90C20 clock inputs back to their original frequencies (if they were slowed down during the power-down mode). Care must be taken to ensure that the clock inputs to the WD90C20 are stable BEFORE driving the "PDOWN" input high.

To return to normal mode, the power manager drives "PDOWN" high; the WD90C20 returns to normal operation mode after the following time interval; the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles. The screen automatically displays the information in video memory.

The power-up service routine must reload the RAMDAC RAM data and the 32 by 5 dithering mapping RAM data after the system returns to normal operation mode.

7.2 DISPLAY IDLE MODE

7.2.1 Description Of Display Idle Mode

The Display Idle Mode is used when the user can allow the display to be turned off, for example, when a keyboard key has not been pressed for five minutes. The DAC and LCD panel interfaces are turned off in this mode. Internal clocks are divided by eight from the primary inputs, thus internal logic runs eight times slower. The CPU can access I/O registers of the WD90C20, but it can not access display memory.

Power saving is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing internal WD90C20 clocks by eight.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to video memory.

7.2.2 Entering Display Idle Mode

Register bits PR35(7) and PR44(7) must be set to "0" (default values) to use this mode. The WD90C20 will enter a Display Idle Mode cycle when the motherboard power manager drives the "PDOWN" input of the WD90C20 low.

The WD90C20 will then divide the internal VCLK and MCLK signals by eight. For example, if the input VCLK is 32 MHz and the input MCLK is 44.9 MHz, the internal VCLK will be 4 MHz and the internal MCLK will be 5.61 MHz. Power consumption in this mode is approximately 1/10 of normal consumption. The internal RAMDAC turns off and screen refresh cycles are stopped. The WD90C20 uses the "REFRESH" input to generate "CAS before RAS" cycles to refresh display memory. The CPU will be the only user to access the display memory. There is no arbitration between CPU cycles and CRT cycles, or between CPU cycles and refresh cycles.

While in the Display Idle Mode, the video system continues to run, allowing the user to read/write WD90C20 I/O registers, however, the CPU CAN NOT read/write display memory.

7.2.3 Exiting Display Idle Mode

To return to normal operation mode, the power manager simply drives "PDOWN" high. The screen automatically displays the original picture. External clocks must maintain original frequencies for the Display Idle Mode.

7.3 GENERAL POWER-DOWN MODES

7.3.1 Description of General Power-Down Modes

There are two General Power-Down modes. These modes are used when: 1)the user doesn't need to view the display, 2)he needs to keep the system running, but 3)he can afford to reduce the frequencies of both MCLK and VCLK. Video system performance is reduced in exchange for significant power savings. Another advantage is that activating the WD90C20 PDOWN input is the only software interaction required.

One of the General Power-Down modes is designed to interface with an intelligent clock generator like the WD90C61, which slows down the clocks to the WD90C20 to a selectable frequency during the power-down interval. This is called the General Power-Down mode with External Clock Control.

The other is designed to be independent of the external clock control; the external clock maintains the same frequency during power-down, however internal clock circuitry in the WD90C20 divides the input clock by eight. This is called General Power-Down mode with Internal Clock Control.

Both General Power-Down modes allows the CPU to access BOTH I/O registers and display memory.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing the MCLK and VCLK inputs by a system chosen factor (external) or by eight (internal).

7.3.2 Entering General Powerdown Mode with External Clock Control

To select General Power-Down mode with External Clock Control, load bit PR44(7) with "1" and bit PR35(6) with "0". PR44(6:0) should be preloaded with its correct value, based on the power-down clock frequency.

The WD90C20 will enter a General Power-Down mode with External Clock Control cycle when the motherboard power manager drives the "$\overline{\text{PDOWN}}$" input of the WD90C20 low. At this time the PR44 register will replace the CRTC registers to control memory refresh timing.

7.3.3 Exiting General Power-Down Mode With External Clock Control

Before returning to normal display mode, the power manager must first return the WD90C20 clock inputs back to their original frequencies. Care must be taken to ensure that the clock inputs to the WD90C20 are stable BEFORE driving the "$\overline{\text{PDOWN}}$" input high.

To return to normal mode, the power manager drives "$\overline{\text{PDOWN}}$" high; the WD90C20 then returns to normal operation mode and displays the screen that is stored in video memory.

7.3.4 Entering General Power-Down Mode with Internal Clock Control

To enter the General Power-Down mode with the internal clock control, PR44(7) must be set to a "1" and PR35(6) must be set to a "1". PR44(6:0) should be pre-loaded with its correct value based on the VCLK frequency and the PR1A(1:0) value. The PR1A(1:0) is used to select different memory refresh cycles per each horizontal line.

After the input "$\overline{\text{PDOWN}}$" is driven low by the system, the WD90C20 will enter General Power-Down mode automatically. Register PR44 will replace the CRTC registers to control memory refresh timing.

7.3.5 Exiting General Power-Down Mode with Internal Clock Control

To return to normal mode, the power manager drives "PDOWN" high; the WD90C20 then returns to normal operation mode and returns the internal MCLK and VCLK signals to their normal frequencies. The information stored in video memory is displayed on the screen.

7.3.6 Example Calculations of PR44(6:0) Values

Described below are examples of how to calculate correct values of PR44(6:0) for both General Power-Down modes. Calculation of PR44(6:0) value is based upon the following equation:

7.3.7 Disabling the WD90C20 to Accommodate an Alternate VGA Controller

PR35 Bit 5 allows the WD90C20 to accommodate an alternate VGA controller. When the WD90C20 detects that "PDOWN" is low and PR35(5) is high, the WD90C20 isolates itself from the system I/O bus regardless of the programmed power-down mode. In this case, the CPU CAN NOT access the WD90C20. All outputs and I/Os of the host interface are tristated. This feature allows another VGA or graphic controller on the system I/O bus in case the system designer wished to switch display environments.

To return to normal operation mode, the CPU must drive "PDOWN" high.

PR44(6:0) = ((Refresh Rate*PR1A(1:0))/((1/(CLK/8))*Character)) - 5

Where: Refresh Rate = Period defined for Refresh of the DRAMs

CLK = External Clock input for General Power-Down mode with External Clock
VCLK input for General Power-Down mode with Internal Clock.

Example for General Power-Down mode with External Clock Control:

Example A == > How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 0
PR1A(1:0) = 11 (2 memory refresh cycles/horizontal line)
Normal Operation: VCLK = 32 MHz, MCLK = 44.9 MHz
Power-Down Mode: VCLK = 5 MHz, MCLK = 8 MHz (external control)

CALCULATE ==>
15 us x 2 = 30 us (2 refreshes/line)
1/5 MHz x 8 = 200 ns x 8 = 1.6 us (1 character clock in power-down mode)
(30 us / 1.6 us) - 5 = 14 (PR44(6:0) = OE hex)

Example B ==> How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 1 (internal divided by 8 control)
PR1A(1:0) = 01 (1 memory refresh cycle/horizontal line)
Normal Operation: VCLK = 28 MHz, MCLK = 42 MHz
Power-Down Mode: VCLK = 3.5 MHz, MCLK = 5.25 MHz (internal control)

CALCULATE ==>
15 us x 1 = 15 us (1 refresh/line)
285.7 ns x 8 = 2.286 us (1 character clock in power-down mode)
(15 us/ 2.286 us) - 5 = 2 (PR44(6:0) = 02 hex)

The following are descriptions of the output states of all output pins during the four power-down modes. These states are given for both "AT" and "Micro Channel" modes of operation. This information is provided for reference to the system designer.

PC-AT MODE					
OUTPUT STATE					
Pin No.	**Pin**	**System Powerdown Mode**	**Display Idle Mode**	**General Mode w/Ext. Clock**	**General Mode w/Int. Clock**
	SD[15:0]	Z	N	N	N
15	IOCHRDY	Z	N	N	N
12	IRQ	Z	N	N	N
14	$\overline{\text{MEMCS16}}$	Z	N	N	N
13	$\overline{\text{EBROM}}$	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	$\overline{\text{RAS32}}$	N	N	N	N
56	$\overline{\text{RAS10}}$	N	N	N	N
59	$\overline{\text{CAS32}}$	N	N	N	N
58	$\overline{\text{CASA10}}$	N	N	N	N
65	$\overline{\text{OE32}}$	H	N	N	N
64	$\overline{\text{OE10}}$	H	N	N	N
	$\overline{\text{WE}}$[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	$\overline{\text{LCD}}$/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	$\overline{\text{RPLT}}$	H	N	N	N
93	$\overline{\text{WPLT}}$	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tri-state.

NOTES: For on-chip pullups and pulldowns, see Section 4.0 "Signal Description."

MICRO CHANNEL MODE					
OUTPUT STATE					
Pin No.	Pin	System Powerdown Mode	Display Idle Mode	General Mode w/Ext. Clock	General Mode w/Int. Clock
	SD[15:0]	Z	N	N	N
15	IOCHRDY	H	N	N	N
12	IRQ	H	N	N	N
14	$\overline{\text{MEMCS16}}$	H	N	N	N
13	$\overline{\text{EBROM}}$	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	$\overline{\text{RAS32}}$	N	N	N	N
56	$\overline{\text{RAS10}}$	N	N	N	N
59	$\overline{\text{CAS32}}$	N	N	N	N
58	$\overline{\text{CASA10}}$	N	N	N	N
65	$\overline{\text{OE32}}$	H	N	N	N
64	$\overline{\text{OE10}}$	H	N	N	N
	$\overline{\text{WE}}$[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	$\overline{\text{LCD}}$/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	$\overline{\text{RPLT}}$	H	N	N	N
93	$\overline{\text{WPLT}}$	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tri-state.

8.0 LCD PANEL CONTROL

This section describes external power on/off control logic for an LCD panel interface.

8.1 DESCRIPTION OF SIGNALS FOR FIGURE 8-1

Described below are the signals related to the poweron/off control logic in Figure 8-1.

POWER-ON
(General motherboard signal, input to control logic)

Active high signal: indicates that the LCD +5 volt power supply (+VDD_LCD) and the backlight power supply (+VBL) are stable.

$\overline{\text{PDOWN}}$, +PDOWN
(General motherboard signal, input to control logic)

Active low and active high signals, respectively; indicate that the system has entered the POWER-DOWN mode.

RSET
(General motherboard signal, input to control logic)

Active high signal; is generated during power-on or system reset.

$\overline{\text{LCD}}$
(WD90C20 output)

WD90C20 active low output; indicates that the LCD panel is selected as main display.

$\overline{\text{LCDEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable the LCD drivers and DC power.

$\overline{\text{CFLEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable backlight power.

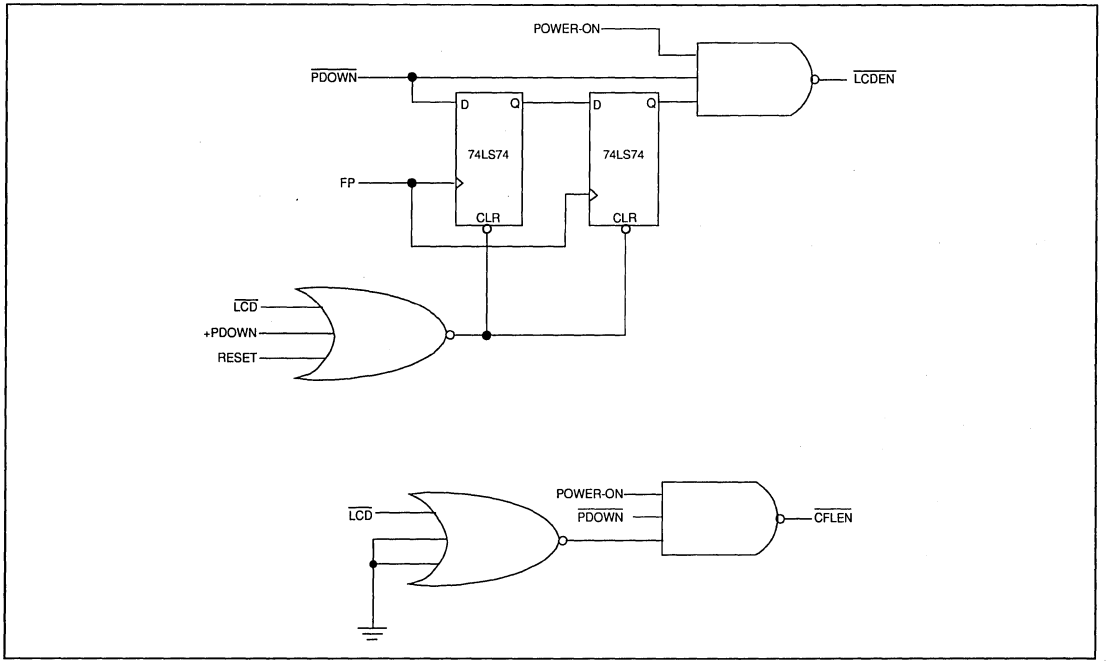

FIGURE 8-1. LCD PANEL CONTROL

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9.0 LCD POWER-ON/OFF OPERATIONS DESCRIPTION

9.1 SYSTEM POWER-ON

When main power is turned on, RESET guarantees the "LCDEN" remains "HIGH" during the power-on interval. This protects the LCD panel from damage. After RESET goes inactive and if a CRT monitor is connected, the "LCD" output from the WD90C20 will be a "1" which forces "LCDEN" high, keeping the LCD panel disabled.

After RESET goes inactive and if an LCD panel is connected, the "LCD" output from the WD90C20 will be a "0." Two "FP" strobes (one to two vertical frames) after "LCD" goes low, "LCDEN" is driven low, enabling LCD power. "CFLEN" (backlight power) is driven low immediately after "LCD" goes low.

9.2 SYSTEM POWER-OFF

When main power is turned off "POWERON" goes low, forcing both "-LCDEN" and "CFLEN" high, which immediately disables both LCD panel power and backlight power.

9.3 SWITCHING FROM CRT MODE TO LCD MODE

The system must:

1. Reset the CRT mode bit PR19(5) to "0."
2. Read and save the CRTC registers.
3. Load the shadow registers with default values from the table.
4. Lock the shadow registers.
5. Write back the CRTC registers.
6. Enable the LCD mode by setting PR19(4)=1 (which sets "LCD"=0).

Two "FP" strobes (one to two vertical frames) from "LCD" going low, "LCDEN" is driven low, enabling LCD power. "CFLEN" is driven low immediately after "LCD" goes low.

9.4 SWITCHING FROM LCD MODE TO CRT MODE

The system must:

1. Reset the LCD mode bit PR19(4) to "0", thus setting the WD90C20 output "LCD" to a "1" (since "LP" and "FP" are still toggling).
2. Read and save the CRTC registers.
3. Unlock the shadow registers.
4. Write back the CRTC registers.
5. Set the CRT mode bit PR19(5) to a "1".

9.5 ENTERING POWER-DOWN MODE

The system drives "PDOWN" low and "+PDOWN"high to enter a power-down mode. Both "LCDEN" and "CFLEN" are driven high immediately (before "LP" and "FP" stop toggling).

9.6 LEAVING POWER-DOWN MODE

When in LCD Mode: The system drives "PDOWN" high and "+PDOWN" low to leave a power-down mode (to return to normal operation mode). "LCDEN" remains high for two "FP" strobes (one to two vertical frame periods). This guarantees the "LP" and "FP" will be toggling before LCD panel power is turned on.

When in CRT Mode: Because "LCD" is always a "1" when entering and leaving a power-down mode, "LCDEN" and "CFLEN" will also remain high for the entire period, thus leaving the LCD panel power off.

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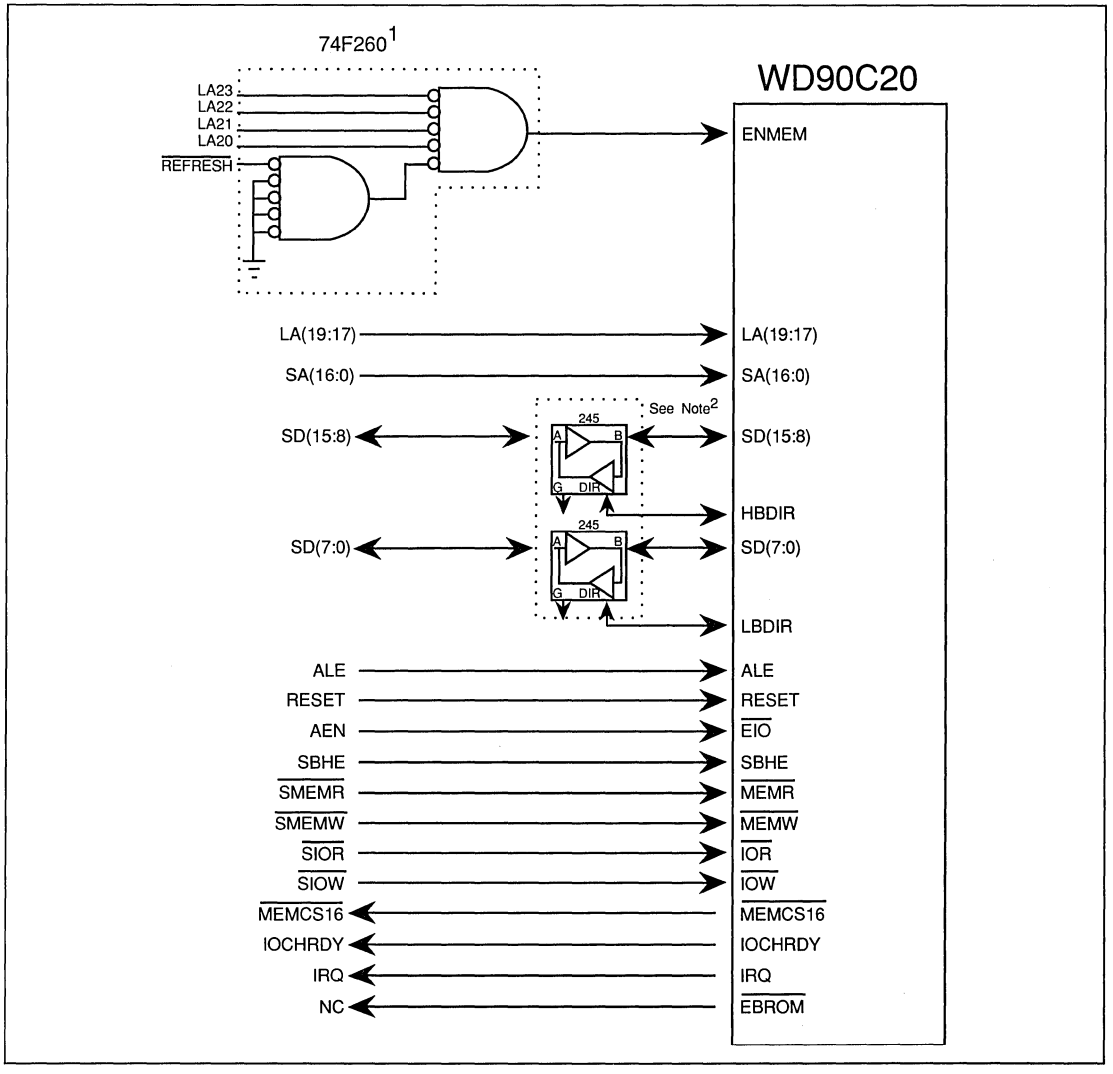

FIGURE A-1. PC/AT INTERFACE

NOTES:

[1] The 74F260 is used to determine if the current address is in the first megabyte. This function is already provided by most core logic chip sets.

[2] The 74245 buffers are only needed if system drive requirements exceed chip capabilities.

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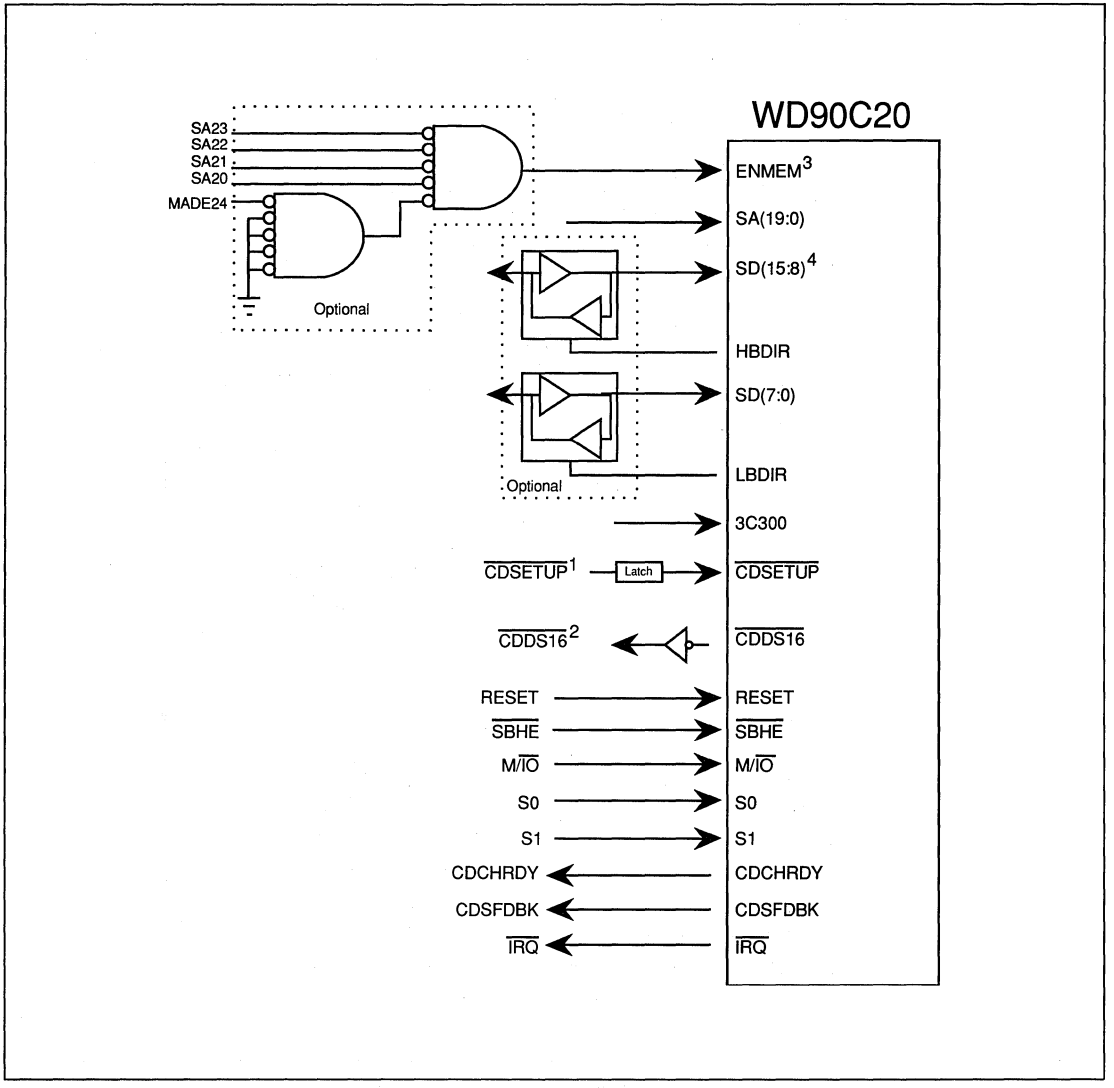

FIGURE A-2. MICRO CHANNEL INTERFACE

NOTES:

1 $\overline{\text{CDSETUP}}$ must be latched if core logic does not already latch it.
2 CDDS16 requires an inverter (changed in future revisions).
3 ENMEN must be qualified for the first megabyte of memory space. This is provided in many core logic designs; the two And Gates are not required.
4 The bidirectional buffers are only needed if the system design requires more current than the WD90C20 can deliver.

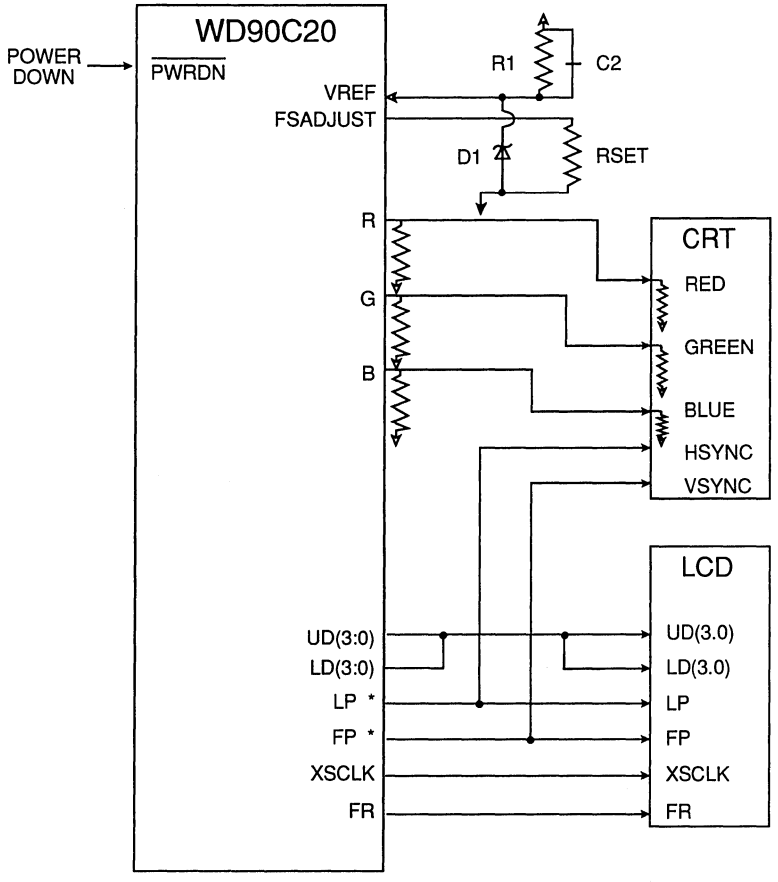

FIGURE A-3. WD90C20 DISPLAY INTERFACE

FULL-SCALE-VOLTAGE CALCULATION EXAMPLE:

$$V_{FULL\ SCALE} = [I_{FULL\ SCALE}] \quad [RLD]$$

$$= \left[\frac{code \times 0.04 \times VREF}{RSET}\right] [RLD]$$

$$= \left[\frac{63 \times 0.04 \times 1.235}{221}\right] [50] = 0.704 \text{ volts}$$

* These signals may require buffering if monitor sinks more than the 6mA drive of the WD90C20.

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B.0 EGA MODE APPENDIX

This appendix provides a general description of EGA mode. Details of the actual software implementation are not covered.

For those registers that are the same in both VGA and EGA mode, refer to the VGA description. Only the differences are described in this section. Bits not used should be set to 0 unless otherwise noted.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pullup or pulldown resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.

2. Unlock all the PR registers.

3. Program PR2(6) to 0 for EGA mode.

4. Set PR4 Bit 1 to logic 1 for EGA compatibility.

5. Load PR11(7:4) with EGA Configuration switches by using pullup or pulldown resistors on pins MD(15:12). (Pullup resistor causes logic 1 to be latched after power-on-reset.)

6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 Bit 4.

7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the steps listed below:

- Initialize all the registers
- Lock CRT controller registers
- Force Clock Control rate of the CRT controller

8. Set EGA emulation mode by programming:

- PR11(3)=1; Set EGA emulation on PS/2 type display
- PR14(6)=1; Vertical double scan
- PR11(2)=1; Lock clock select
- PR11(0)=1; Lock 8/9 dot timing
- PR14(7)=1; Enable IRQ (optional)

9. Lock the PR registers PRO-PR5 and PR10-PR17.

10. Read protect PR registers.

11. When EGA is required on a TTL monitor, the suggested steps are:

- Initialize all the registers
- Set EGA TTL mode by programming:
  PR11(3)=0;EGA TTL
  PR14(7)=1;Enable IRQ
  PR15(6)=1;Set Low Clock
  PR14(7)=1;Enable IRQ
- Lock PR registers PRO-PR5 and PR10-PR17
- Read protect PR registers

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3C4
CRT Controller Data Reg Except the Following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
High Pen High (Index=10)	R	3?5
Light Pen Low (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

TABLE B-1. EGA REGISTERS SUMMARY

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All register addresses are in hex.
3. ? = B in monochrome modes or D in color modes.
4. * = Identical responses from I/O ports 3C0 and 3C1.

B.1 GENERAL REGISTERS

The General Registers and the bit definitions that differ from VGA mode are covered below.

B.1.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Disables internal video drivers.
0 = Activate video drivers.
1 = Disable video drivers.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

B.1.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not Used.

Bit 4

EGA: Information on the four configuration switches stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not Used = 1

B.1.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not Used.

Bit 6

EGA: Not Used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: The following Light Pen Switch definition is applicable:
0 = Light Pen Switch is Closed.
1 = Light Pen Switch is Open.

Bit 1

EGA: The following Light Pen Trigger definition is applicable:
0 = Light Pen Trigger is Reset.
1 = Light Pen Trigger is Set.

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

B.1.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not Used.

B.2 SEQUENCER REGISTERS (PORT 3C5)

B.2.1 Clocking Mode Register , (Index = 01)

Bits (7:4)

EGA: Not Used.

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to Zero.

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

B.2.2 Character Map Select Register, (Index 03)

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Character Map Select A:

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

Bits (1:0)

EGA: Character Map Select B:

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

NOTE: 1. Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

B.2.3 Memory Mode Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha Mode Bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha mode and enables non-Alpha mode.

B.3 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. A "?" implies that a register is mapped into either 3B5 or 3D5 for Monochrome or Color display modes, respectively.

B.3.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Register Address index where the data is to be written.

B.3.2 Horizontal Total Register, (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

B.3.3 End Horizontal Blanking Register, (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: These bits define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

B.3.4 End Horizontal Retrace Register, (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

B.3.5 Vertical Total Register, (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

B.3.6 CRT Controller Overflow Register, (Index = 07)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bit (4:0) definitions in the VGA section.

B.3.7 Preset Row Scan Register, (Index = 08)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register (4:0) definition in the VGA section.

B.3.8 Maximum Scan Line Register, (Index = 09)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

B.3.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

B.3.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not Used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

B.3.11 Vertical Retrace Start Register, (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

B.3.12 Vertical Retrace End Register, (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not Used.

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if Bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

B.3.13 Underline Location Register, (Index = 14)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

B.3.14 End Vertical Blanking Register, (Index = 16)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

B.3.15 Mode Control Register, (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.4 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

B.4.1 Read Map Select Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

B.4.2 Mode Register, (Index = 05)

Bit (7:6)

EGA: Not Used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

B.5 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

B.5.1 Mode Control Register, (Index = 10)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.5.2 Overscan Color Register, (Index = 11)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the 6 bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

B.5.3 Color Plane Enable Register, (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer according to the following table.

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (PORT 3?A)	
		BIT 5	BIT 4
0	0	VID 2 (Red)	VID 0 (Blue)
0	1	VID 5 (SRed)	VID 4 (SGreen)
1	0	VID 3 (SBlue)	VID 1 (Green)
1	1	VID 5 (SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

B.5.4 Horizontal PEL Panning Register, (Index = 13)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: These 4 bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, a 9-dots/character image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B.6 MONITOR DETECTION

The DAC output currents I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparators against a voltage derived from the external voltage reference V_{REF}. For the WD90C20, the output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

For the WD90C20A, the output current is determined by the formula:

$$I = \frac{code \times V_{REF} \times 1.036}{R_{SET}}$$

The output signal MDETECT is readable at port 3C2H bit 4. It is important to read during active video ouput, not during retrace or any other blanking period.

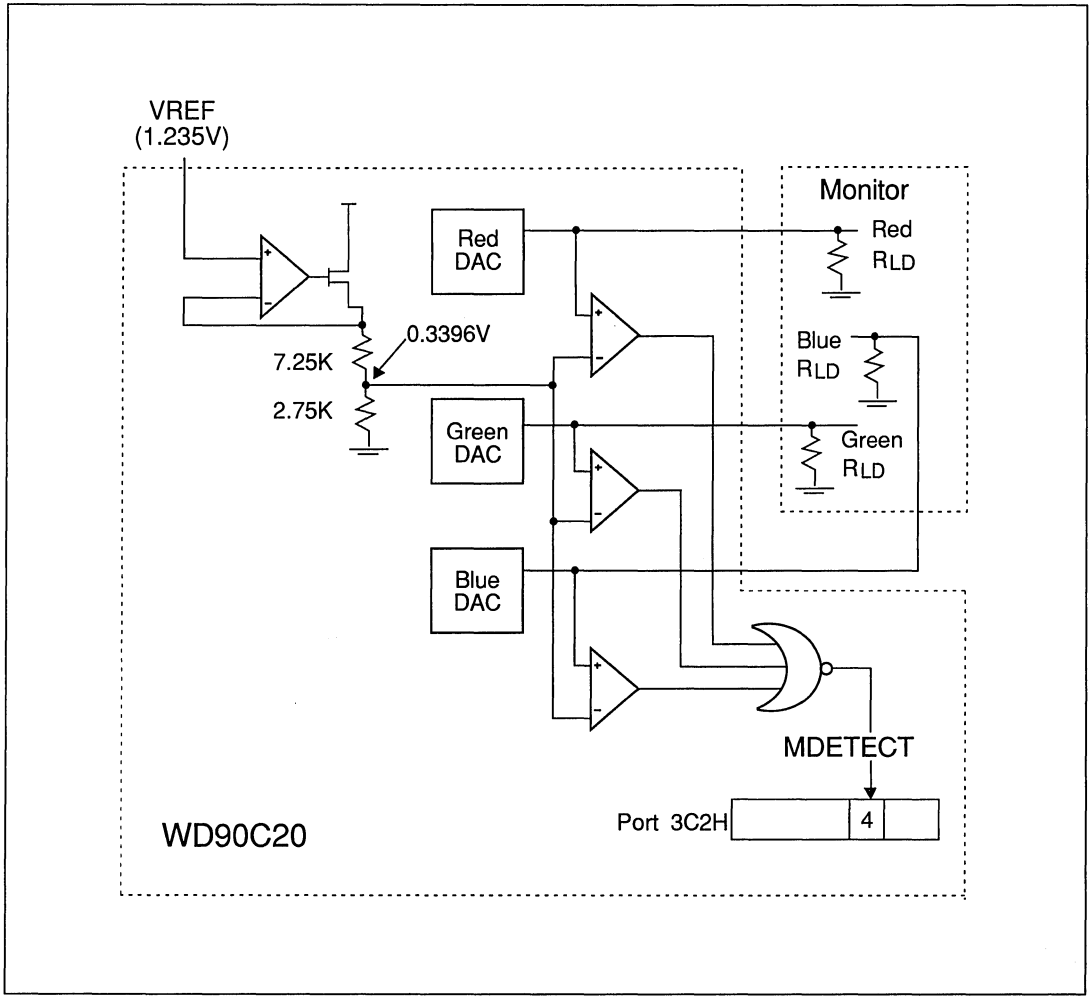

FIGURE B-1. MONITOR DETECTION FOR INTERNAL RAMDAC

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C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	I/O Write – AT Mode
C-2	I/O Read – AT Mode
C-3	Memory Write – AT Mode
C-4	Memory Read – AT Mode
C-5	I/O Write – Micro Channel Mode
C-6	I/O Read – Micro Channel Mode
C-7	Memory Write – Micro Channel Mode
C-8	Memory Read – Micro Channel Mode
C-9	CPU Write with Non-Page Mode
C-10	CPU Read Non-Page Mode, CRT Read
C-11	DRAM Page Mode Read Timing
C-12	WD90C20 LCD Timing (t = VCLK)
C-13	RAMDAC Timing
C-14	CRT Clock Timing
C-15	Reset Timing
C-16	RAS OnlyDRAM Refresh Timing
C-17	CAS Before RAS DRAM Refresh Timing
C-18	CAS Before RAS Refresh (Power-Down Mode)
C-19	STN Color LCD Interface Timing
C-20	IOCHRDY Release Timing in Memory Read Cycle
C-21	IOCHRDY Release Timing in Memory Write Cycle

TABLE C-1. TIMING DIAGRAMS

NOTE:

The following timing values are the same for the WD90C20 and WD90C20A, except as noted.

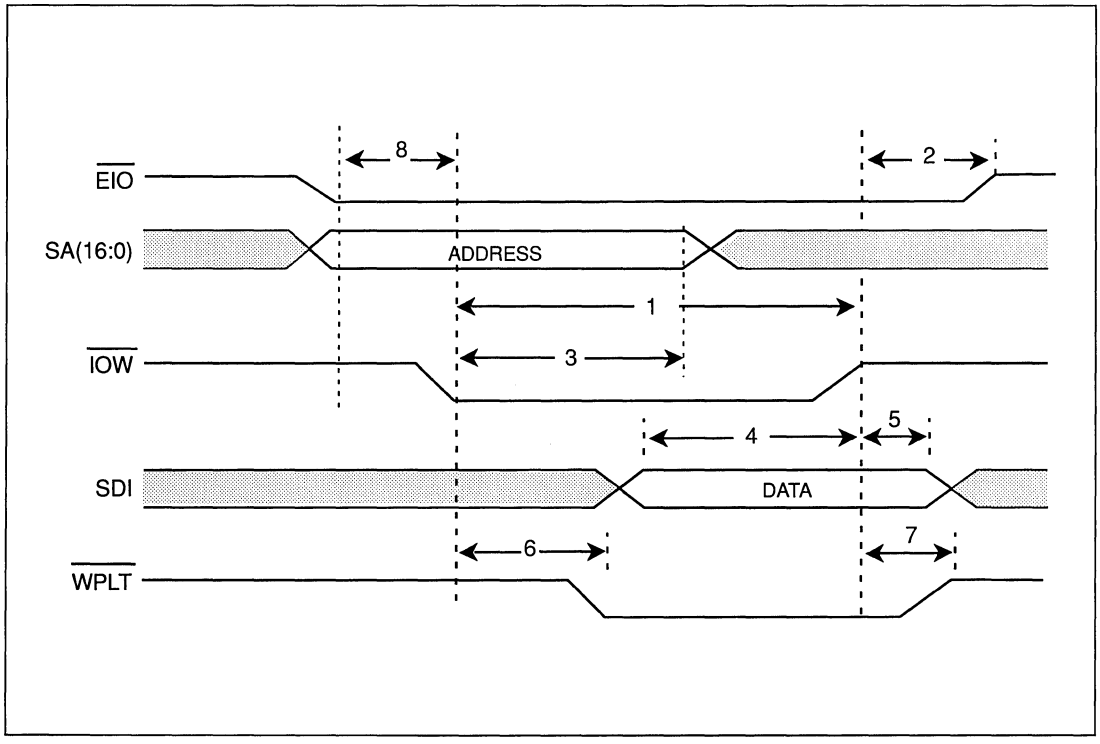

FIGURE C-1. I/O WRITE-AT MODE

NO.	I/O WRITE AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{IOW}$	active pulse width		2.5t			
2	$\overline{EIO}$	hold from	$\overline{IOW}$ inactive (high)	10			
3	SA(16:0),	hold from	$\overline{IOW}$ active	30		25	
4	Write Data SDI	setup to	$\overline{IOW}$ inactive	30			
5	Write Data SDI	hold from	$\overline{IOW}$ inactive	10			
6	$\overline{WPLT}$	active from	$\overline{IOW}$ active (C_L = 15pF)		50		45
7	$\overline{WPLT}$	inactive from	$\overline{IOW}$ inactive (C_L = 15pF)		50		45
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOW}$ active	15			

t = 1/MCLK

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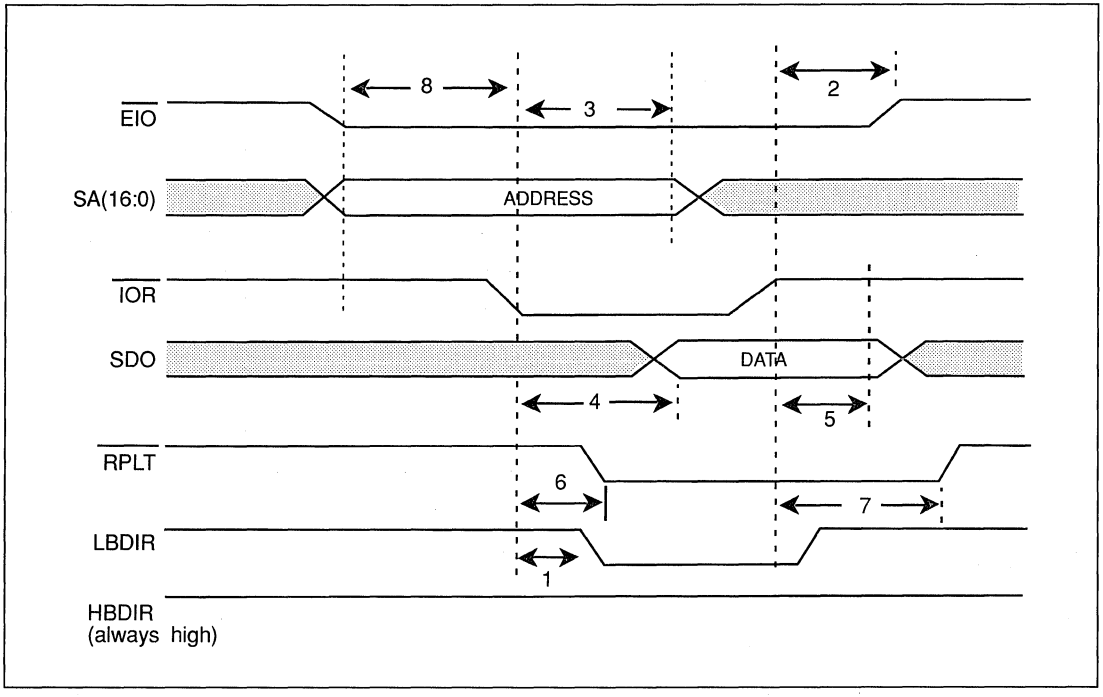

FIGURE C-2. I/O READ-AT MODE

NO.	I/O READ AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	LBDIR	delay from	$\overline{IOR}$		48		43
2	$\overline{EIO}$	hold from	$\overline{IOR}$ inactive (high)	10			
3	SA(16:0),	hold from	$\overline{IOR}$ active	25			
4a	Read Data SDO	valid from	$\overline{IOR}$ active	.5T	1.5T+65		1.5t+60
4b	Read Data SDO	valid from for mapping RAM only	$\overline{IOR}$ active		4t+65		1.5t+60
5	Read Data SDO	hold from	$\overline{IOR}$ inactive	10	40		
6	$\overline{RPLT}$	active from	$\overline{IOR}$ active (C_L = 15pF)		50		45
7	$\overline{RPLT}$	inactive from	$\overline{IOR}$ inactive (C_L = 15pF)		50		45
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOR}$ active	15			

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

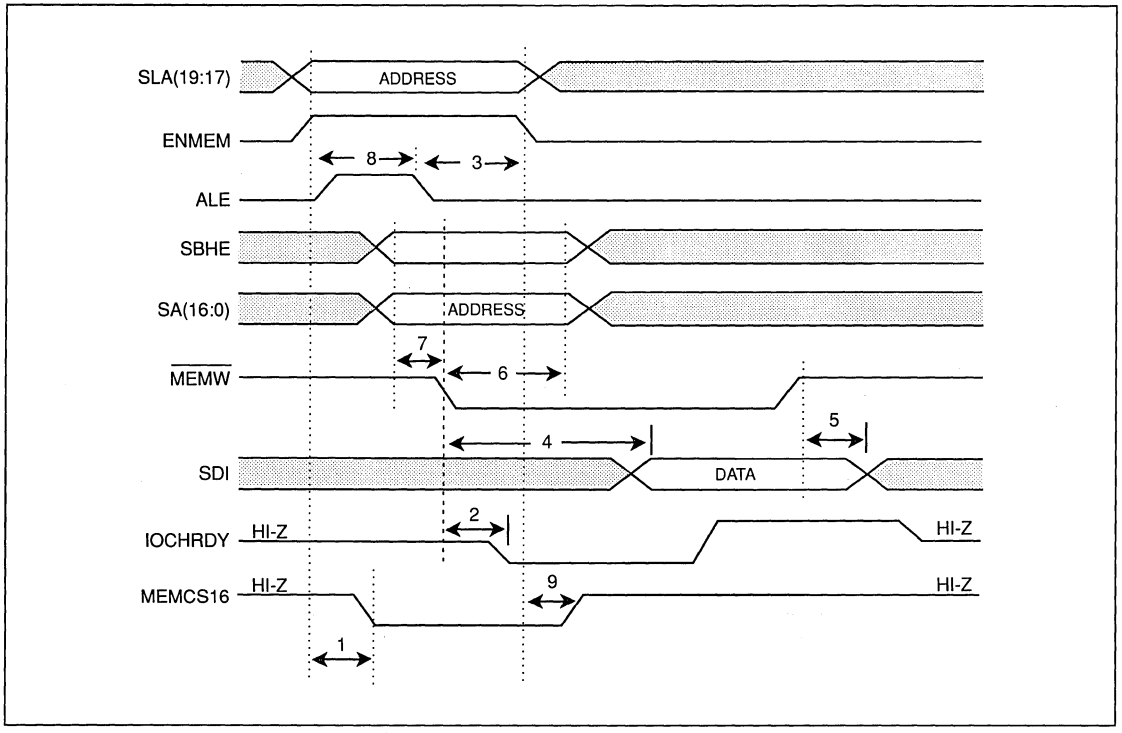

FIGURE C-3. MEMORY WRITE - AT MODE

NO.	MEMORY WRITE AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{\text{MEMCS16}}$	valid from	SLA (19:17) ENMEM valid		21		
2	IOCHRDY	inactive from	$\overline{\text{MEMW}}$ active	10			
3	SLA(19:17), ENMEM	hold from	ALE inactive	5			
4	Data SDI	valid from	$\overline{\text{MEMW}}$ active	30		25	
5	Data SDI	hold from	$\overline{\text{MEMW}}$ inactive	5			
6	SA(16:0), SBHE	hold from	$\overline{\text{MEMW}}$ active	20			
7	SA(16:0), SBHE	setup to	$\overline{\text{MEMW}}$ active	25			
8	SLA(19:17), ENMEM	setup to	ALE inactive	25			
9	$\overline{\text{MEMCS16}}$	invalid from	SLA (19:17) ENMEM invalid		35		30

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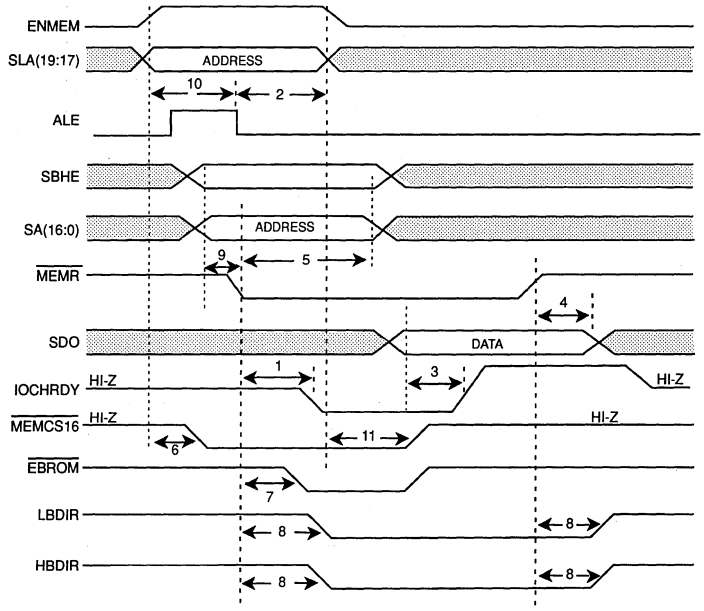

FIGURE C-4. MEMORY READ - AT MODE

NO.	MEMORY READ – AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	IOCHRDY	inactive from	$\overline{\text{MEMR}}$ active		26		
2	SLA(19:17), ENMEM	hold from	ALE inactive	30		25	
3	Data SDO	valid setup to	IOCHRDY active	1.5t-25			
4	Data SDO	hold from	$\overline{\text{MEMR}}$	10	50		
5	SA(16:0), SBHE	hold from	$\overline{\text{MEMR}}$ active	20			
6	$\overline{\text{MEMCS16}}$	valid from	SLA(19:17) ENMEM valid		24		
7	$\overline{\text{MEMR}}$	active to	$\overline{\text{EBROM}}$ active		50		45
8	LBDIR HBDIR	delay from	$\overline{\text{MEMR}}$		60		45
9	SA(16:0), SBHE	setup to	$\overline{\text{MEMR}}$ active	25			
10	SLA(19:17), ENMEM	setup to	ALE inactive	25			
11	$\overline{\text{MEMCS16}}$	invalid from	SLA(19:17) ENMEM invalid		35		30

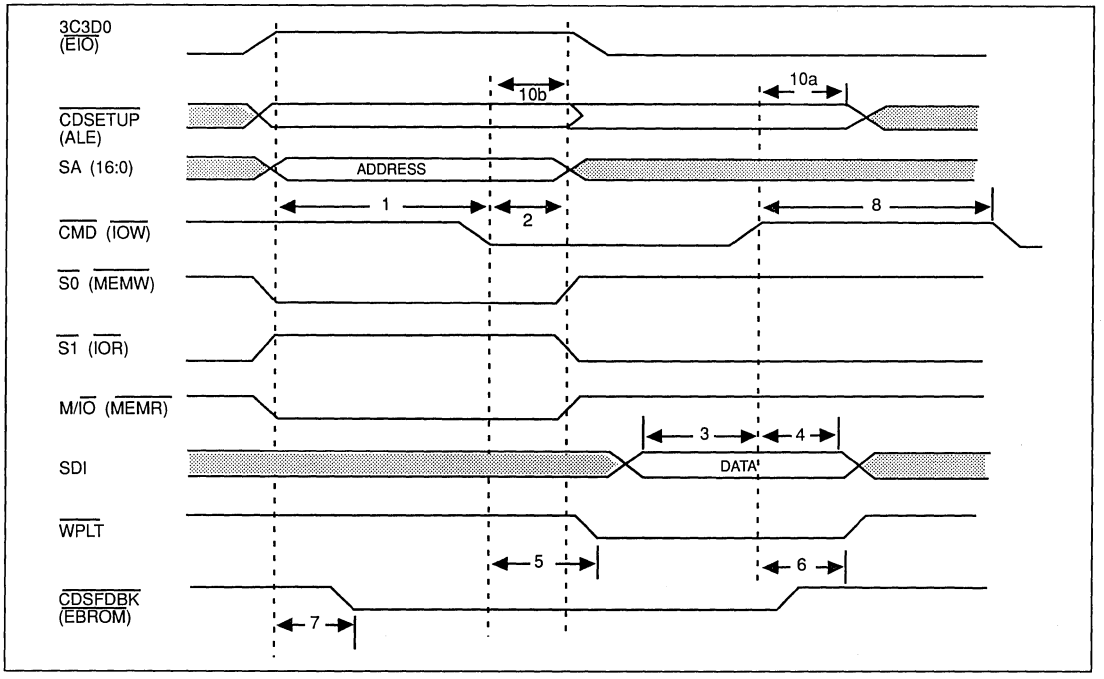

FIGURE C-5. I/O WRITE-MICRO CHANNEL MODE

NO.	I/O WRITE – MC MODE			WD90C20		WD90C20A	
				MIN.	MAX	MIN.	MAX
1	SA(16:0), S0, S1 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	15			
2	SA(16:0), S0, S1 3C3D0, M/IO	hold from	CMD active	30		25	
3	Write data SDI	setup to	CMD inactive	30			
4	Write data SDI	hold from	CMD inactive	10			
5*	WPLT	active from	CMD active		50		45
6*	WPLT	inactive from	CMD inactive		50		45
7	CDSFDBK	active from	Address Valid		58		53
8	CMD	inactive pulse width		2t			
9	CMD	active pulse width		2.5t			
10a	CDSETUP (WD90C20)	hold from	CMD inactive (high)	2t+30		2t+25	
10b	CDSETUP (WD90C20A)	hold from	CMD active (low)	30		25	

* C_L = 15pF
t = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

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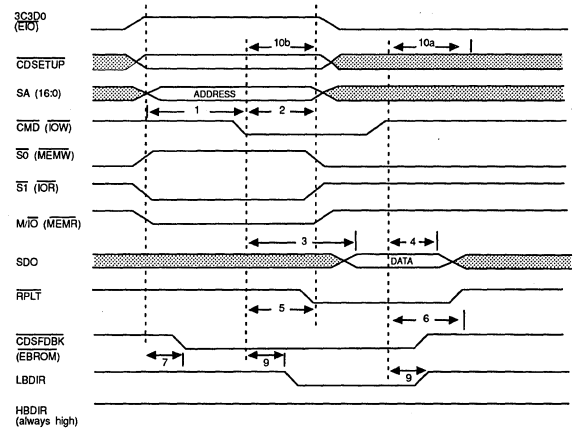

FIGURE C-6. I/O READ - MICRO CHANNEL MODE

NO.	I/O READ MC MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	SA(16:0), S0, S1, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	15			
2	SA(16:0), S0, S1, 3C3D0, M/IO	hold from	CMD active	30		25	
3a	Read data SDO	valid from	CMD active	.5T	1.5T+65		1.5t+60
3b	Read data SDO	valid from mapping RAM only	CMD active		4t+65		4t+60
4	Read data SDO	hold from	CMD inactive	10	40		
5	RPLT	active from	CMD active (C_L = 15pF)		50		45
6	RPLT	inactive from	CMD inactive (C_L = 15pF)		50		45
7	CDSFDBK	active from	Address Valid		58		53
8a	CMD	active pulse width		130			
8b	CMD	active pulse width mapping RAM only		4t+30		4t+25	
9	LBDIR	delay from	CMD		48		43
10a	CDSETUP (WD90C20)	hold from CMD inactive (high)		2t+30		2t+25	
10b	CDSETUP (WD90C20A)	hold from CMD active (low)		30		25	

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

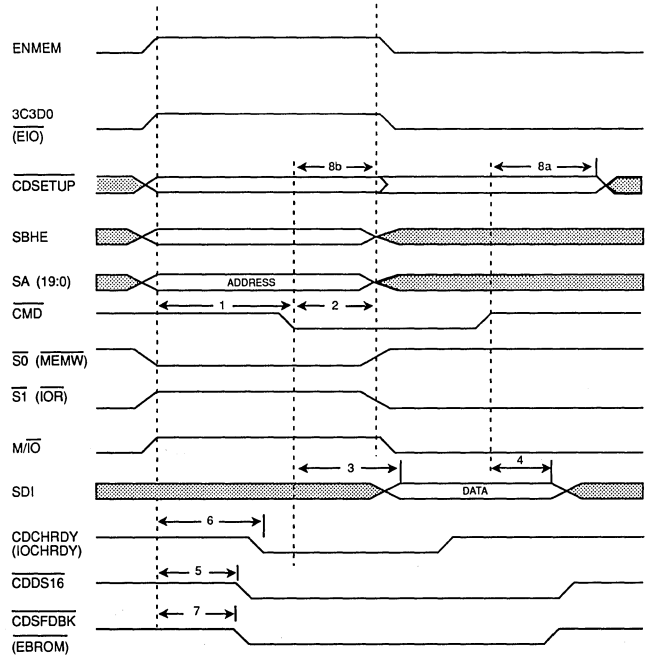

FIGURE C-7. MEMORY WRITE-MICRO CHANNEL MODE

NO.	MEMORY WRITE MC MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	25			
2	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, M/IO	hold from	CMD active	30		25	
3	Data SDI	valid from	CMD active		25		
4	Data SDI	hold from	CMD inactive	0			
5	CDDS16	valid from	SA(19:0) ENMEM valid		45		
6	SA(19:10) S0, S1	valid to	CDCHRDY inactive (low)		40		
7	CDSFDBK	active from	Address Valid		58		53
8a	CDSETUP (WD90C20)	hold from	CMD inactive (high)	2t+30		2t+25	
8b	CDSETUP(WD90C20A)	hold from	CMD active (low)	30		25	

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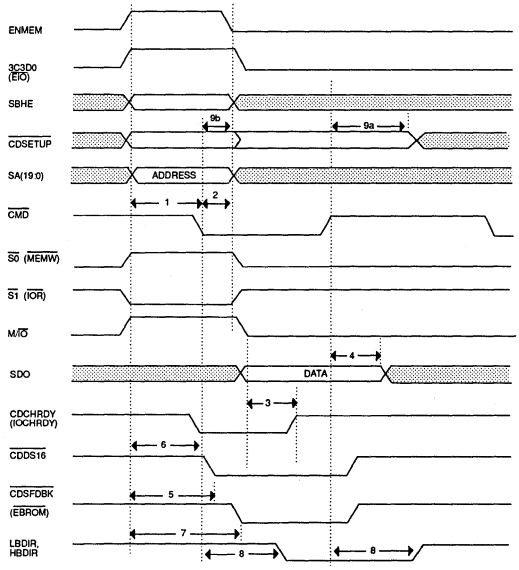

FIGURE C-8. MEMORY READ-MICRO CHANNEL MODE

NO.	MEMORY READ MC MODE		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, CDSETUP, M/IO	setup to CMD active (low)	25			
2	SA(19:0), S0, S1 ENMEM, SBHE, 3C3D0, M/IO	hold from CMD active	30		25	
3*	Read data SDO valid	setup to CDCHRDY active (high)	1.5t-25			
4	Read data SDO	hold from CMD inactive	10	50		45
5	CDDS16	valid from SA(19:0) ENMEM valid		45		40
6	SA(19:0) S0, S1	valid to CDCHRDY inactive (low)		40		
7	CDSFBK	active from Address Valid		58		53
8	HBDIR, LBDIR	delay from CMD		60		55
9a	CDSETUP (WD90C20)	hold from CMD inactive (high)	2t+30			2t+25
9b	CDSETUP (WD90C20A)	hold from CMD active (low)	30			25

NOTES: * PR1A (7:6) = 00

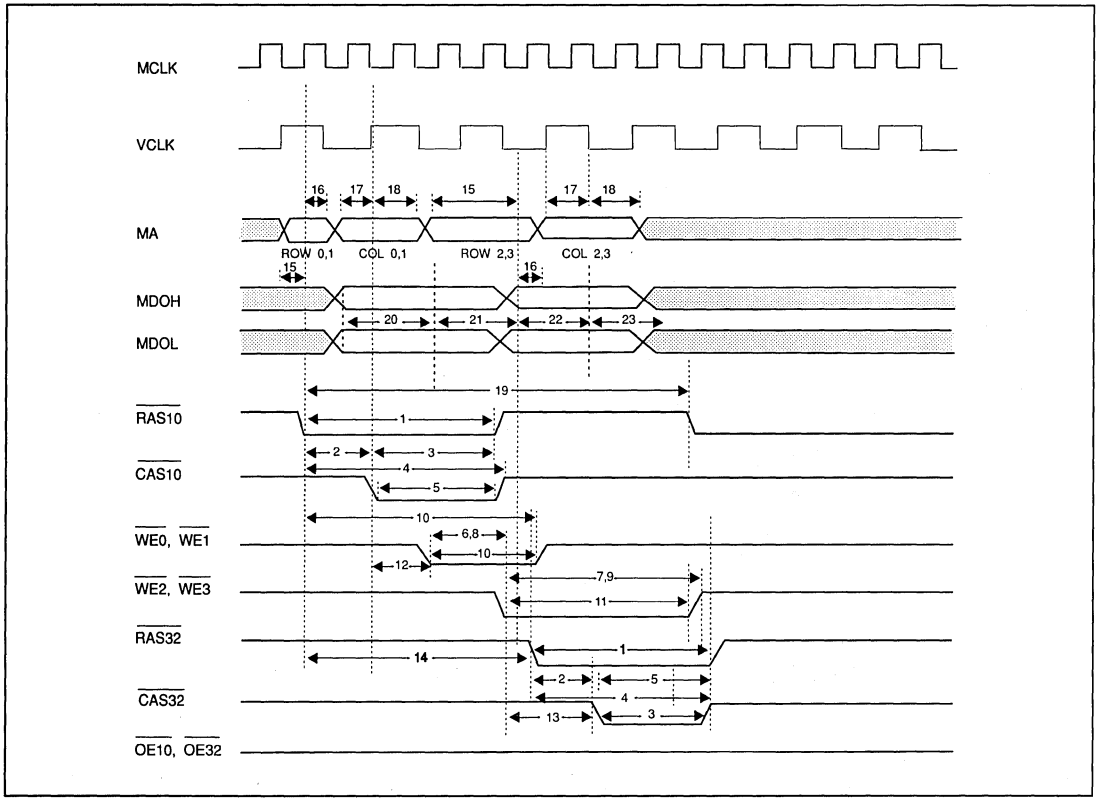

FIGURE C-9. CPU WRITE WITH NON-PAGE MODE

NO.	CPU WRITE MCLK = 45.046 MHz		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1	$\overline{RAS10}$ ($\overline{RAS32}$)	pulse width low	5t-25	5t	5t-20	
2	$\overline{RAS10}$ ($\overline{RAS32}$)	low to $\overline{CAS10}$ ($\overline{CAS32}$)(low)	2t-11	2t+2	2t-6	
3	$\overline{CAS10}$ ($\overline{CAS32}$)	low to $\overline{RAS10}$ ($\overline{RAS32}$)(high)	3t-20	3t+10	3t-5	
4	$\overline{RAS10}$ ($\overline{RAS32}$)	low to $\overline{CAS10}$ ($\overline{CAS32}$)(high)	5t-25	5t	5t-20	
5	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low	3t-25	3t	3t-20	
6	$\overline{WE0}$, $\overline{WE1}$	low to $\overline{CAS10}$ (high)	2.5t-20	2.5t	2.5t-15	
7	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{CAS32}$ (high)	5t-20	5t	5t-15	
8	$\overline{WE0}$, $\overline{WE1}$	low to $\overline{RAS10}$ (high)	2.5t-20	2.5t+2	2.5t-15	
9	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{RAS32}$ (high)	5t-20	5t+2	5t-15	
10	$\overline{WE0}$, $\overline{WE1}$	pulse duration	3t-20	3t	3t-15	
11	$\overline{WE3}$, $\overline{WE2}$	pulse duration	5t-20	5t	5t-15	
12	$\overline{WE0}$, $\overline{WE1}$	low from $\overline{CAS10}$ (low)	0.5t-5	0.5t+6		

t = 1/MCLK

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NO.	CPU WRITE MCLK = 45.046 MHz (CONTINUED)		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
13	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{CAS32}$ (low)	2t-10	2t		
14	$\overline{RAS10}$	low to $\overline{RAS32}$ (low)	4.5t-7	4.5t+7		
15	Row address	setup to $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-15	t+15		
16	Row address	hold from $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15		
17	Column address	setup to $\overline{CAS10}$, $\overline{RAS32}$ (low)	t-25	t+10	t-20	
18	Column address	hold from $\overline{CAS10}$, $\overline{CAS32}$ (low)	1.5t-5	1.5t+20		1.5t+15
19	Random Write Cycle		9t			
20	Write Data	setup to $\overline{WE0}$, $\overline{WE1}$ (low)	t-10			
21	Write Data	hold from $\overline{WE0}$, $\overline{WE1}$ (low)	2t-5			
22	Write Data	setup to $\overline{CAS32}$ (low)	2t-5			
23	Write Data	hold from $\overline{CAS32}$ (low)	t-5			

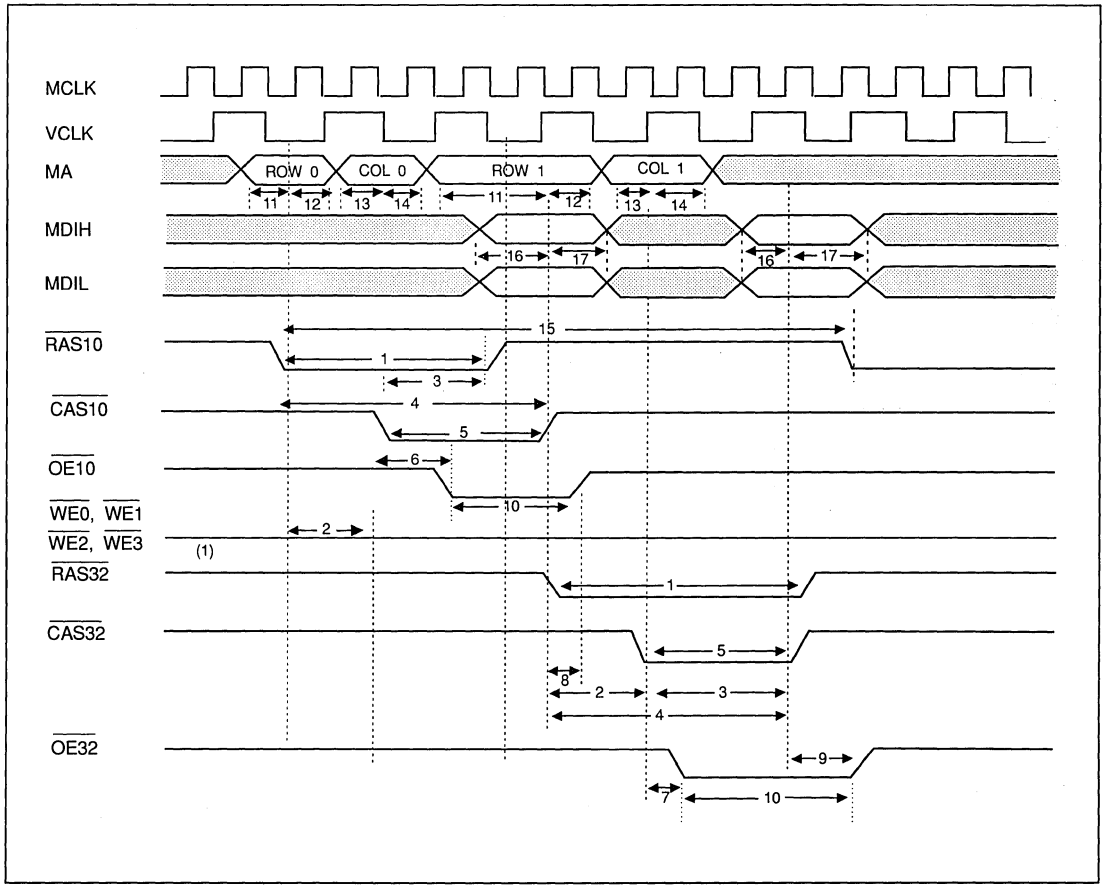

FIGURE C-10. CPU READ NON-PAGE MODE, CRT READ

NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{RAS10}$ ($\overline{RAS32}$)	pulse width low		5t-25	5t	5t-20	
2	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$)(low)	2t-11	2t+2		
3	$\overline{CAS10}$ ($\overline{CAS32}$)	low to	$\overline{RAS10}$ ($\overline{RAS32}$)(high)	3t-15	3t+10	3t-12	
4	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$)(high)	5t-20	5t	5t-15	
5	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-20	3t	3t-15	
6	$\overline{CAS10}$	low to	$\overline{OE10}$ (low)	t-6	t+5		
7	$\overline{CAS32}$	low to	$\overline{OE32}$ (low)	t-6	t+5		
8	$\overline{CAS10}$	high to	$\overline{OE10}$ (high)	t-6	t+5		

t = 1/MCLK

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NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz (CONTINUED)		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
9	$\overline{CAS32}$ high	to $\overline{OE32}$ (high)	t-6	t+5		
10	$\overline{OE10}$, $\overline{OE32}$	pulse width low	3t-20	3t	3t-15	
11	Row address	setup to $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-12	t+10		
12	Row Address	hold from $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15		t+12
13	Column Address	setup to $\overline{CAS10}$, $\overline{CAS32}$ (low)	t-12	t+10		
14	Column Address	hold from $\overline{CAS10}$, $\overline{CAS32}$ (low)	1.5t	1.5t+25		1.5t+20
15	Random Read Cycle		9t-2			
16	Read Data	setup to $\overline{CAS10}$, $\overline{CAS32}$ (high)	10			
17	Read Data	hold from $\overline{CAS10}$, $\overline{CAS32}$ (high)	15			

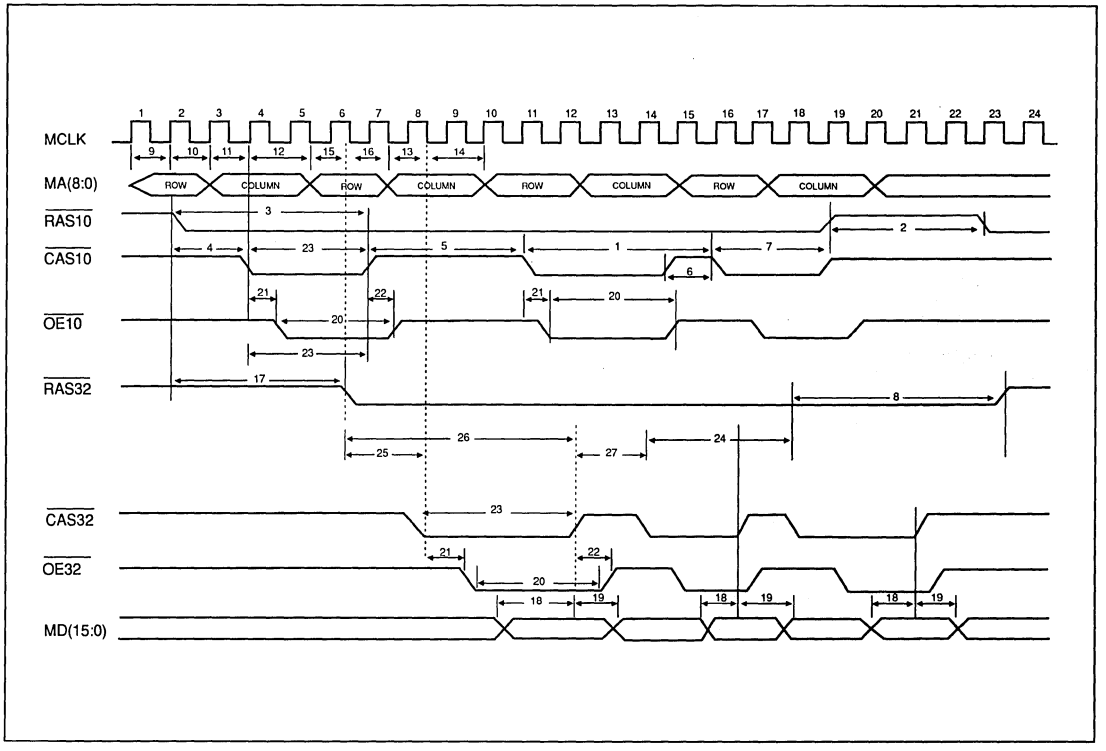

FIGURE C-11. DRAM PAGE MODE-READ TIMING

NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1*	Page mode	cycle time	$\overline{CAS10}$ low to CAS low	5t-2			
2	$\overline{RAS10}$	Precharge		4t-6	4t+14		4t+10
3	$\overline{RAS10}$	low to	$\overline{CAS10}$ high (first)	5t-20	5t-2	5t-15	
4	$\overline{RAS10}$	low to	$\overline{CAS10}$ low	2t-11	2t+2		
5	First $\overline{CAS10}$	pulse width high		4t-10	4t+10		
6	$\overline{CAS10}$	pulse width high		2t-10	2t+10		
7	$\overline{CAS10}$	low to	$\overline{RAS10}$ high	3t-15	3t+4	3t-12	
8	$\overline{CAS32}$	low to	$\overline{RAS32}$ high	5t-15	5t+4	5t-12	
9	Row address	setup to	$\overline{RAS10}$ low	t-5	t+16		t+12
10	Row address	hold from	$\overline{RAS10}$ low	t-5	t+5		
11	Column address	setup to	$\overline{CAS10}$ low	t-15	t+1		
12	Column address	hold from	$\overline{CAS10}$	1.5t	1.5t+18		
13	Column address	setup to	$\overline{CAS32}$	t-15	t+8		

* First cycle is +2t longer than this spec
t = 1/MCLK

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NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz (CONTINUED)			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
14	Column address hold from		$\overline{CAS32}$ low	1.5t-15	1.5t+2	1.5t-12	
15	Row address	setup to	$\overline{RAS32}$ low	t-15	t+5	t-12	
16	Row address	hold from	$\overline{RAS32}$ low	t-8	t+5		
17	$\overline{RAS32}$	low from	$\overline{RAS10}$ low	4.5t-7	4.5t+7		
18	Read data	setup to	CAS high	15			
19	Read data	hold from	CAS high	15			
20	$\overline{OE10}$ ($\overline{OE32}$)	pulse width low		3t-20	3t	3t-15	
21	$\overline{OE10}$ ($\overline{OE32}$)	low after	$\overline{CAS10}$ low ($\overline{CAS32}$)	t-6	t+6		
22	$\overline{OE10}$ ($\overline{OE32}$)	high after	$\overline{CAS10}$ high ($\overline{CAS32}$)	t-6	t+6		
23	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-20	3t	3t-15	
24	Page mode	cycle time	$\overline{CAS32}$ low to $\overline{CAS32}$ low	5t-2			
25	$\overline{RAS32}$	low to	$\overline{CAS32}$ high (first)	5t-22	5t	5t-15	
26	$\overline{RAS32}$	low to	$\overline{CAS32}$ low	2t-11	2t+2		
27	First $\overline{CAS32}$	pulse width high		2t-11	2t+11		

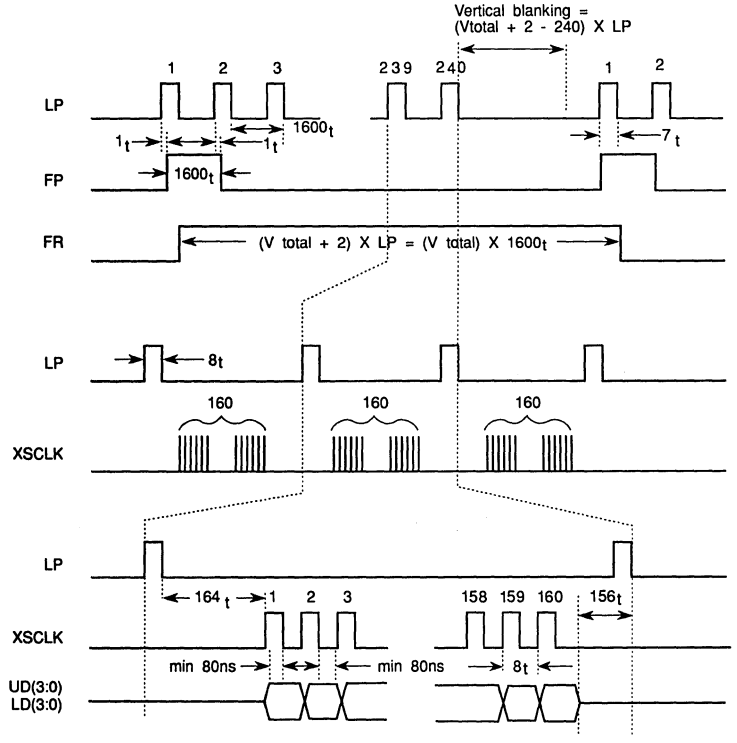

FIGURE C-12. WD90C20 LCD TIMING DIAGRAM (t=VCLK)

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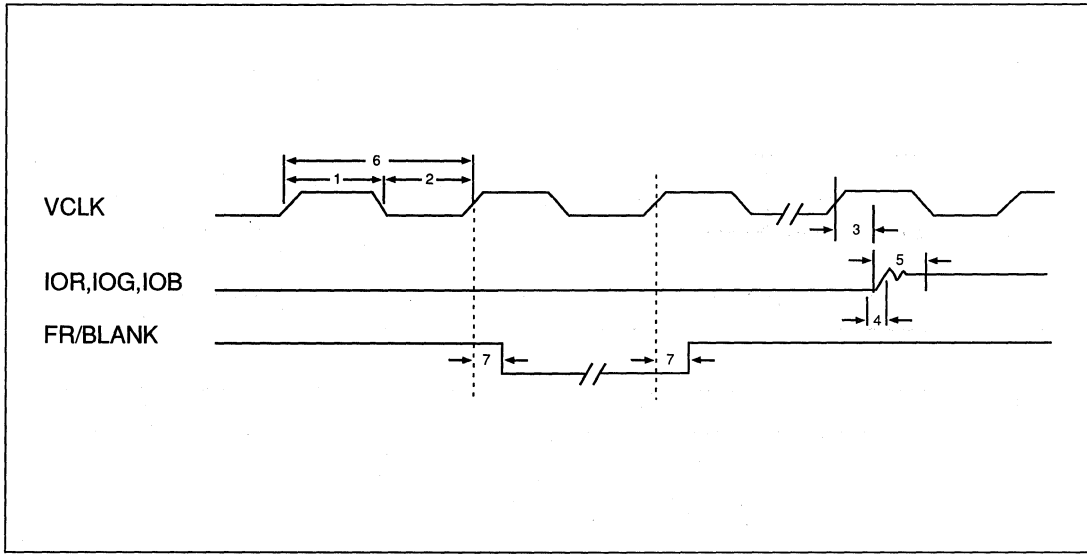

FIGURE C-13. RAMDAC TIMING

NO.	PARAMETER	WD90C20			WD90C20A			UNITS
		MIN.	TYP	MAX	MIN.	TYP	MAX	
1	VCLK Pulse Width High Time	9						ns
2	VCLK Pulse Width Low Time	9						ns
3	Analog Output Delay			30			25	ns
4	Analog Output Rise/Fall Time		3					ns
5	Analog Output Settling Time		20					ns
6	Clock Frequency			45			50	MHz
7	Blanking Delay Time			45				ns

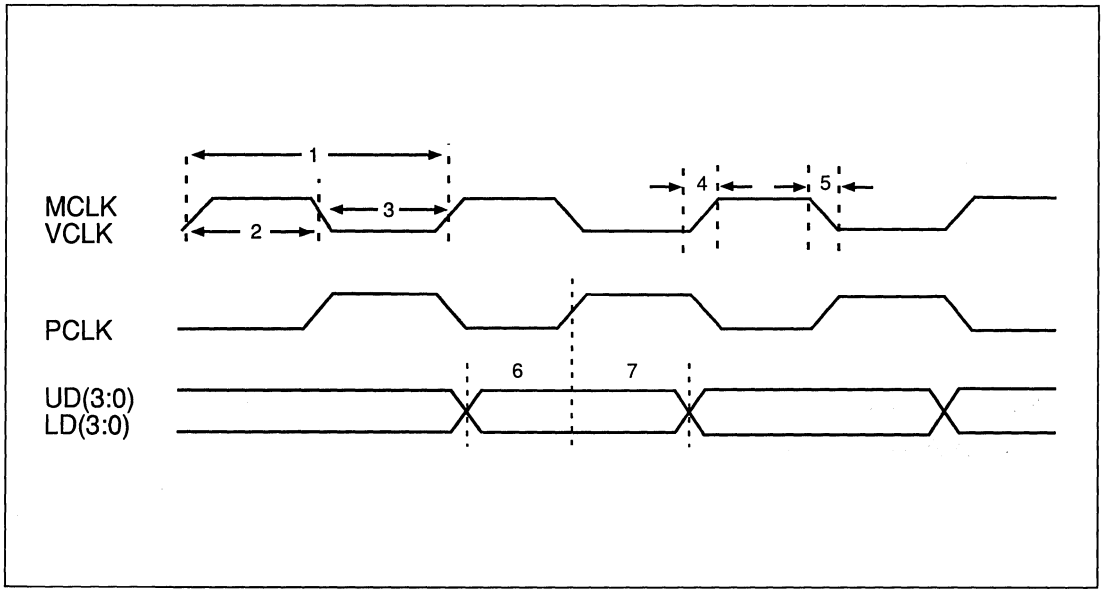

FIGURE C-14. CRT CLOCK TIMING

NO.	PARAMETER	WD90C20		WD90C20A	
		MIN.	MAX	MIN.	MAX
1	Input Clock (VCLK, MCLK)	t	t		
2	Input Clock High Time	40%	60%		
3	Input Clock Low Time	40%	60%		
4	Input Clock Rise Time		3		
5	Input Clock Fall Time		3		
6*	UD(3:0), LD(3:0) setup time to PCLK (high)				
	Mode 0	20			
	Mode 3	10			
	Mode 4	20			
	Mode 12	10			
	Mode 13	15		20	
7*	UD(3:0), LD(3:0) hold time from PCLK (high)				
	Mode 0	10			
	Mode 3	10			
	Mode 4	10			
	Mode 12	10			
	Mode 13	-25		20	

* For external RAMDAC

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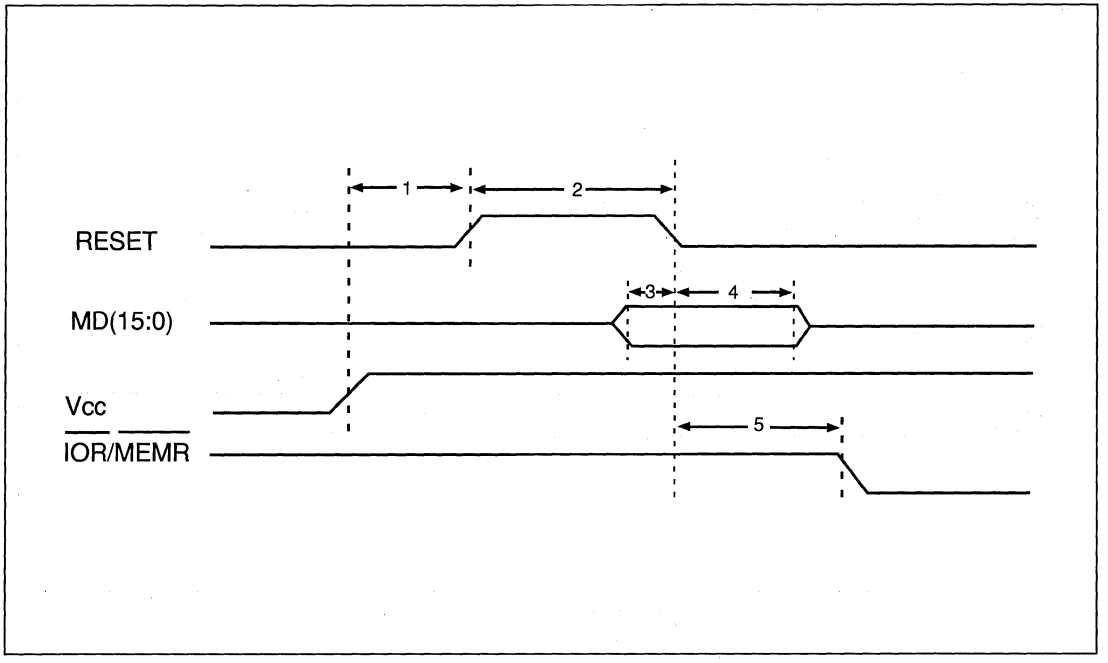

FIGURE C-15. RESET TIMING

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	Vcc	high to	RESET (high)	100ns			
2	RESET	pulse width		100t			
3	MD(15:0)	setup to	RESET (low)	2t			
4	MD(15:0)	hold from	RESET (low)	2t			
5	RESET	to first	$\overline{IOR}/\overline{MEMR}$	10t			

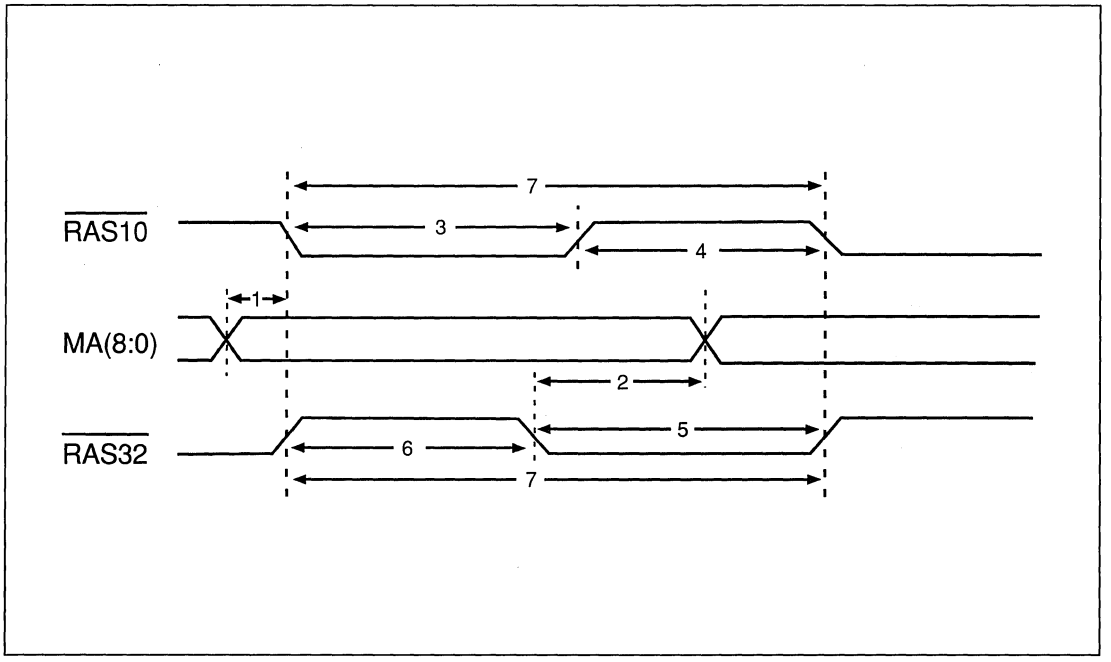

FIGURE C-16. RAS ONLY DRAM REFRESH TIMING

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	MA(8:0)	setup to	$\overline{RAS10}$ active	t			
2	MA(8:0)	hold to	$\overline{RAS32}$ active	t			
3	$\overline{RAS10}$	low time		5t-20	5t+10	5t-15	
4	$\overline{RAS10}$	high time		4t-10	4t+10		
5	$\overline{RAS32}$	low time		5t-20	5t+10	5t-15	
6	$\overline{RAS32}$	high time		4t-10	4t+10		
7	$\overline{RAS}$	cycle time		9t-10	9t+10		

t = 1/MCLK

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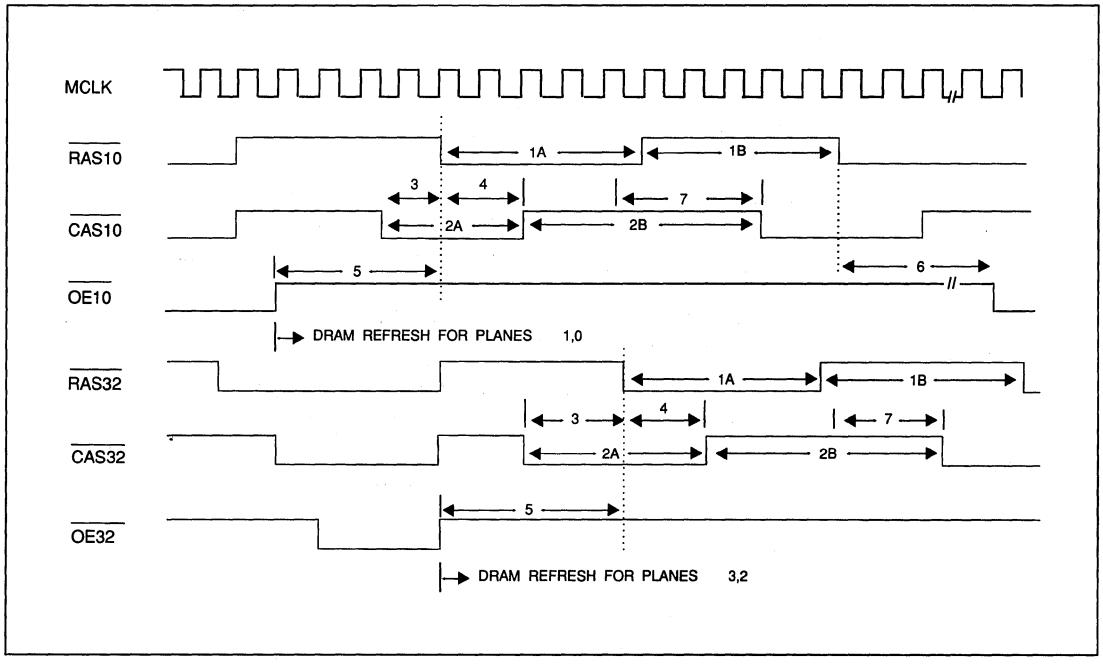

FIGURE C-17. CAS BEFORE RAS DRAM REFRESH TIMING

* (VALID ONLY FOR WD90C20A)

NO.	CAS BEFORE RAS DRAM REFRESH TIMING		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1A	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width low		5t-10	5t+10		
1B	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width high		5t-10	5t+10		
2A	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width low		4t-5	4t+5		
2B	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width high		6t-5	6t+5		
3	$\overline{CAS10}$ ($\overline{CAS32}$) low to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	2t-10	2t+10		
4	$\overline{RAS10}$ (RAS32) low to	$\overline{CAS10}$ ($\overline{CAS32}$) (high)	2t-10	2t+10		
5	$\overline{OE10}$ ($\overline{OE32}$) high to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	4t-8	5t+8		
6	$\overline{RAS10}$ (RAS32) low to	$\overline{OE10}$ ($\overline{OE32}$) (low)	30t			
7	$\overline{RAS10}$ (RAS32) high to (Precharge)	$\overline{CAS10}$ ($\overline{CAS32}$) (low)	3t-5	3t+20		3t+15

t = 1/MCLK

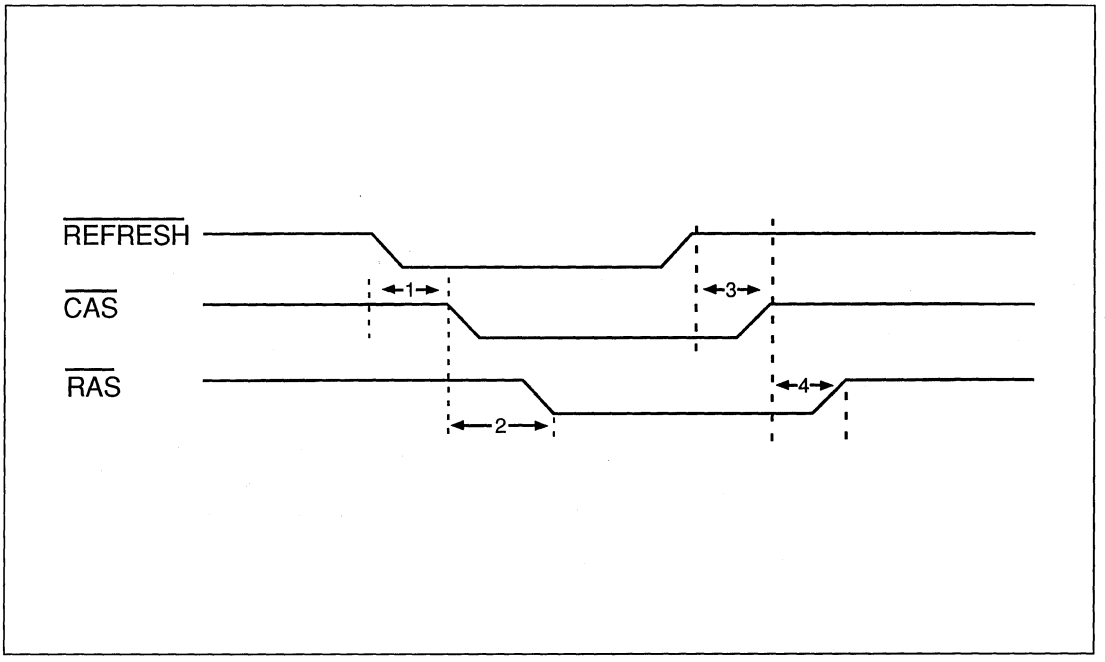

FIGURE C-18. CAS BEFORE RAS REFRESH (Power-Down Mode)

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{CAS}$ low	from	$\overline{REFRESH}$ (low)	20			
2	$\overline{RAS}$ low	from	$\overline{CAS}$ (low)	20			
3	$\overline{CAS}$ high	from	$\overline{REFRESH}$ (high)	15			
4	$\overline{RAS}$ high	from	$\overline{CAS}$ (high)	20			

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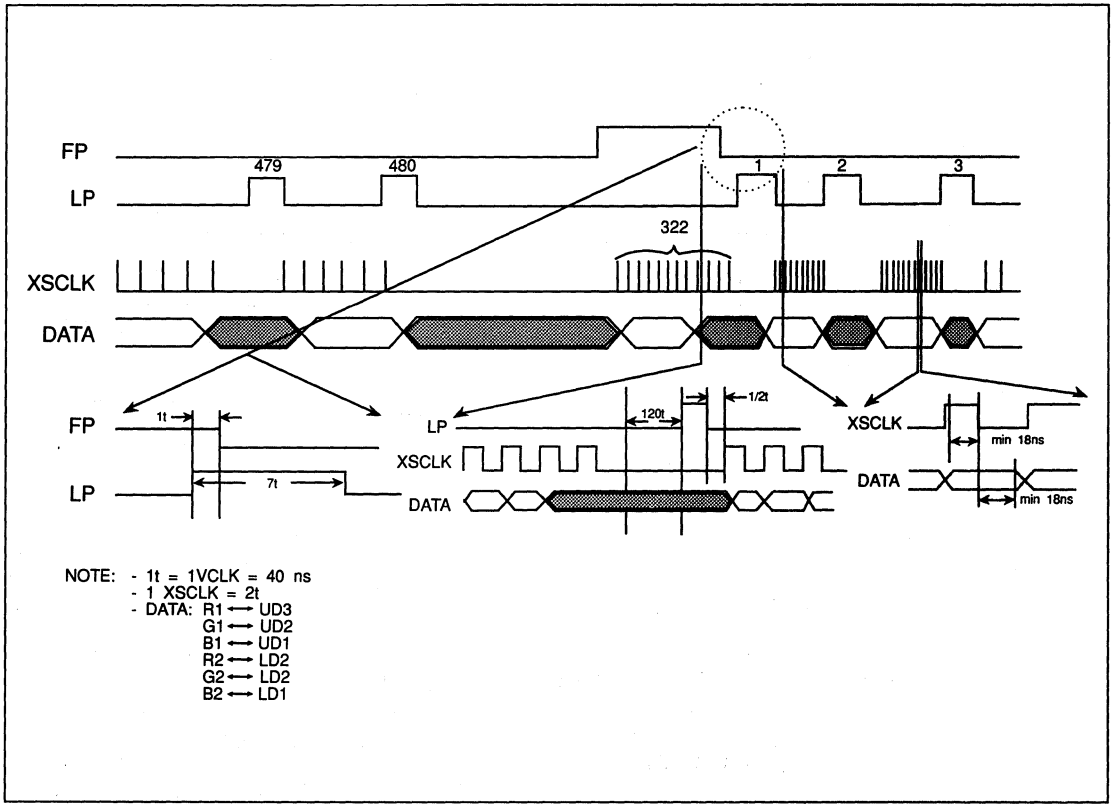

FIGURE C-19. STN COLOR LCD INTERFACE TIMING

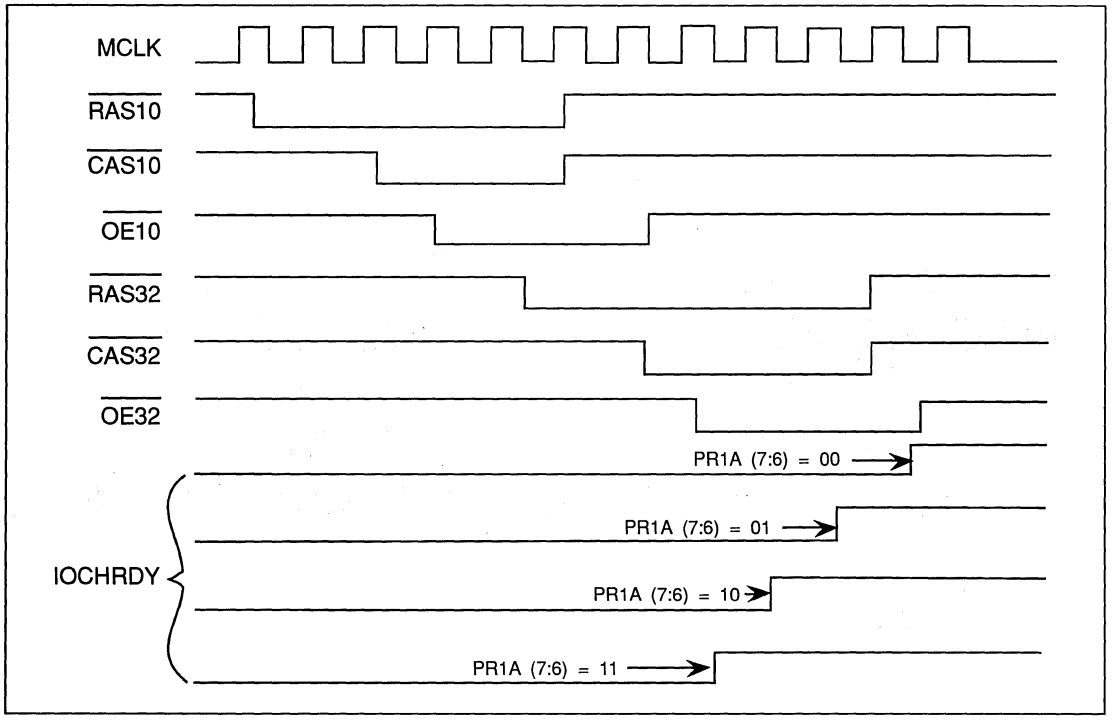

FIGURE C-20. IOCHRDY RELEASE TIMING IN MEMORY READ CYCLE

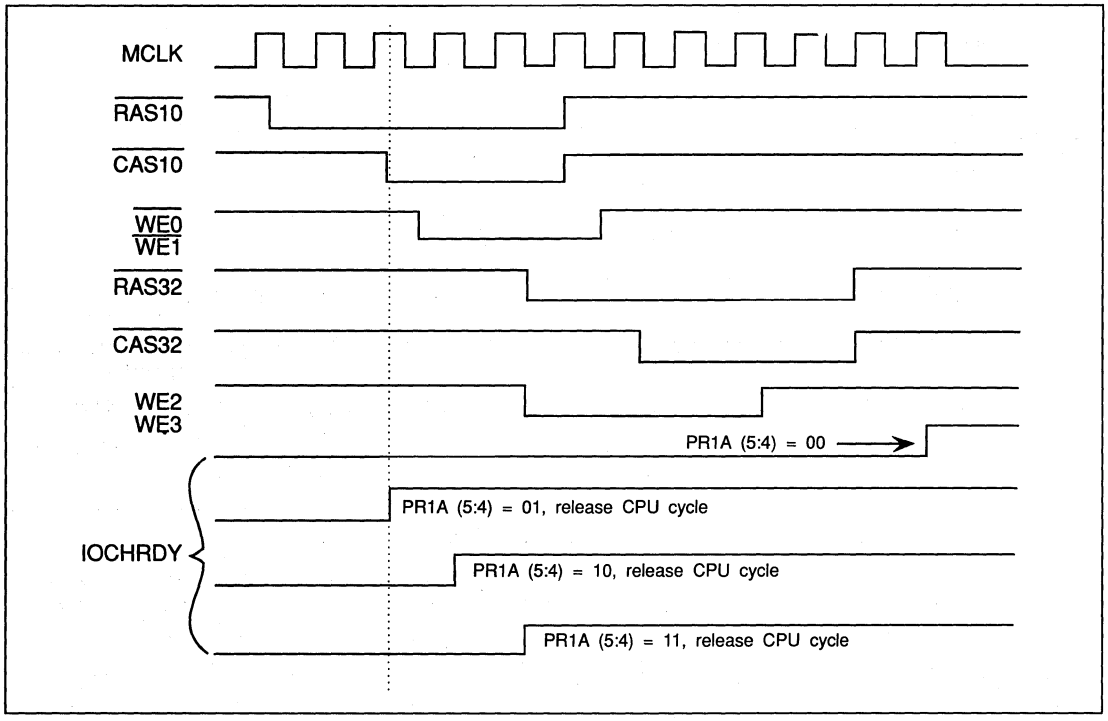

FIGURE C-21. IOCHRDY RELEASE TIMING IN MEMORY WRITE CYCLE

C.1 DC AND RAMDAC SPECIFICATIONS

SUPPLY PINS			
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VCC	4.1V	4.7V	Pins 9, 28, 53, 67, 94
RVCC	4.75V	5.25V	Pin 108
AVCC	4.75V	5.25V	Pin 123

WD90C20 TYPICAL AND MAXIMUM CURRENT/POWER CONSUMPTION						
MODE	**FREQUENCY (MHz)**					
	25 MHz		**28 MHz**		**32 MHz**	
	TYPICAL	**MAX.**	**TYPICAL**	**MAX.**	**TYPICAL**	**MAX.**
DISPLAY ACTIVE	149.4 mA 671.5 mW	179.3 mA 805.8 mW	166.8 mA 750.0 mW	200.2 mA 900.0 mW	182.8 mA 822.2 mW	219.4 mA 986.6 mW
SYSTEM POWERDOWN *	- -	- -	- -	- -	- -	- -
DISPLAY IDLE	22.0 mA 98.3 mW	27.5 mA 122.9 mW	24.3 mA 108.5 mW	30.4 135.6 mW	27.2 mA 121.5 mW	34.0 mA 151.9 mW
GENERAL POWERDOWN W/EXT. CLK CONTROL **	11.0 mA 49.7 mW	14.3 mA 64.6 mW	11.0 mA 49.7 mW	14.3 mA 64.6 mW	11.0 mA 49.7 mW	14.3 mA 64.6 mW
GENERAL POWERDOWN W/INT. CLK CONTROL	22.0 mA 98.4 mW	27.5 mA 123.0 mW	24.8 mA 110.6 mW	31.0 mA 138.3 mW	26.9 mA 120.0 mW	33.6 mA 150.0 mW

Conditions: AVCC (pin 123) = 5.0 volts, MCLK=44.9 MHz
RVCC (pin 108) = 5.0 volts,
DIGITAL VCCs (pins 9, 28, 53, 67, 94) = 4.4 volts
Display type active when measurements taken: LCD.

* - Not available for WD90C20
** - VCLK = 2.0 MHz, MCLK = 6.9 MHz

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WD90C20A TYPICAL AND MAXIMUM CURRENT/POWER CONSUMPTION						
MODE	**FREQUENCY (MHz)**					
	25 MHz		**28 MHz**		**32 MHz**	
	TYPICAL	**MAX.**	**TYPICAL**	**MAX.**	**TYPICAL**	**MAX.**
DISPLAY ACTIVE	74.0 mA 346.0 mW	88.8 mA 415 mW	83 mA 388.0 mW	99.6 mA 465 mW	91.0mA 425.0 mW	109.2 mA 510 mW
SYSTEM POWERDOWN *	4.5 mA 21.0 mW	10.0 mA 46.6 mW	4.5 mA 21.0 mW	10.0 mA 46.6 mW	4.5 mA 21.0 mW	10.0 mA 46.6 mW
DISPLAY IDLE	11.9 mA 56.6 mW	15.5 mA 73.6 mW	13.1 mA 62.5 mW	17.0 mA 81.3 mW	14.7 mA 70 mW	19.1 mA 91.0 mW
GENERAL POWERDOWN W/EXT. CLK CONTROL **	17.5 mA 82.6 mW	21.9 mA 103.3 mW	17.5 mA 82.6 mW	21.9 mA 103.3 mW	17.5 mA 82.6mW	21.9 mA 103.3 mW
GENERAL POWERDOWN W/INT. CLK CONTROL	11.9 mA 56.6 mW	15.5 mA 73.6 mW	13.1 mA 62.5 mW	17.0 mA 81.3 mW	14.7 mA 70 mW	19.1 mA 91.0 mW

Conditions: AVCC (pin 123) = 5.0 volts, MCLK=44.9 MHz
RVCC (pin 108) = 5.0 volts,
DIGITAL VCCs (pins 9, 28, 53, 67, 94) = 4.4 volts
Display type active when measurements taken: LCD.

* - VCLK = MCLK = 0 Hz
** - VCLK = MCLK = 6.9 MHz

INPUT PINS			
PINS	LA17-19, SBHE, MEMEN, $\overline{EIO}$/3C3D0, $\overline{ALE}$, $\overline{MEMR}$/M/$\overline{IO}$, $\overline{PWRDN}$, $\overline{MEMW}$/S0, $\overline{IOR}$/$\overline{S1}$, $\overline{IOW}$/CMD, RESET, $\overline{REFRESH}$, MCLK, VCLK0, SA0-16 (PINS 3-8, 11, 38-44, 98, 99, 117-122, 124-132, 1, 2)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC
PIN	**VREF (PIN 111)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIN ANALOG	-0.5V	2.0V	See RAMDAC specifications
IIL	-10 uA	10 uA	VIN = 0V TO VCC
	-100 uA	100 uA	VIN = 0V TO VCC+0.6V

PIN	MDETECT/FSADJUST (PIN 112)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC

PIN	ALL INPUTS		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
CIN		6 PF	

PINS	IRQ/$\overline{IRQ}$, MA0-8, $\overline{RAS10}$, $\overline{RAS32}$, $\overline{CAS10}$, $\overline{CAS32}$, $\overline{WE0}$, $\overline{WE1}$, $\overline{WE2}$, $\overline{WE3}$, $\overline{OE10}$, $\overline{OE32}$ (PINS 12, 45-52, 55-65)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 3.0mA
VOH	2.4V		IOH = -4.8mA (WD90C20 only)
			IOH = -6.0mA (WD90C20A only)

PINS	$\overline{EBROM}$/$\overline{CDSFDBK}$, HBDIR, LBDIR, LP/HSYNC, FP/VSYNC, FR/BLANK, $\overline{RPLT}$, WPLT/VD9, LD0-3, UD0-3, (PINS 13, 16, 17, 89-93, 100-107)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 1.5mA
VOH	2.4V		IOH = -3.6mA

PINS	MEMCS16\CDS16, IOCHRDY (PINS 14, 15)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 16.0mA
VOH	2.4V		IOH = -8.0mA

TABLE C-2. D.C. TEST SPECIFICATIONS

PINS	RED, GREEN, BLUE (PINS 114-116)		
PARAMETER	MIN	MAX	CONDITIONS
VOUT	-0.5	1.5	See RAMDAC Specification

PIN	$\overline{\text{LCD/CRT}}$ (PIN 110)		
PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

PINS	PCLK, XSCLK, WGTCLK (PINS 86-88)		
PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

I/O PINS			
PINS	VCLK2, VCLK1 (PINS 96, 97)		
PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 1.5 mA
VOH	2.4V		IOH = -3.6mA
IOZ	-50 uA	50uA	VOUT = 0V TO VCC

PINS	SD0-15, MD0-15 (PINS 36-29, 26-19, 84-77, 75-68)		
PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 3.0 mA
VOH	2.4V		IOH = -4.8mA (WD90C20 only)
IOZ	-50 uA	50uA	IOH = -6.0mA (WD90C20A only)
			VOUT = 0V TO VCC

PINS	ALL OUTPUTS AND I/O'S		
PARAMETER	MIN	MAX	CONDITIONS
COUT		30 PF	

TABLE C-2. TEST SPECIFICATIONS (CONTINUED)

PINS	BLUE, GREEN, RED PINS (114-116)			
PARAMETER	**MIN**	**TYP**	**MAX**	**CONDITIONS**
DAC RESOLUTION		6 BITS		
INTEGRAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
DIFFERENTIAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
WHITE LEVEL RELATIVE TO BLACK	13.38mA	14.08mA	14.79mA	VREF = 1.235, RSET = 221 Ohms
BLACK LEVEL	-20uA		20uA	
GRAY SCALE CURRENT RANGE			20mA	
LSB SIZE		223.5 uA		VREF = 1.235, RSET = 221 Ohms
GRAY SCALE ERROR			5.0%	
GLITCH ENERGY			50 pJOULES	
SETTLING TIME			20 NS	R <= 150 Ohms, 100 PF
CLOCK FEED THROUGH			20 pCOULOMB	
DAC TO DAC MATCHING			5%	
OUTPUT COMPLIANCE CURRENT TOLERANCE	-5%		+5%	
OUTPUT COMPLIANCE VOLTAGE RANGE	-0.5V		+1.5V	
VOLTAGE REFERENCE	1.14	1.235	1.26	
VOLTAGE REFERENCE INPUT CURRENT			10 uA	

TABLE C-3. RAMDAC SPECIFICATIONS (WD90C20 ONLY)

D.0 PACKAGE DIMENSIONS AND SPECIFICATIONS

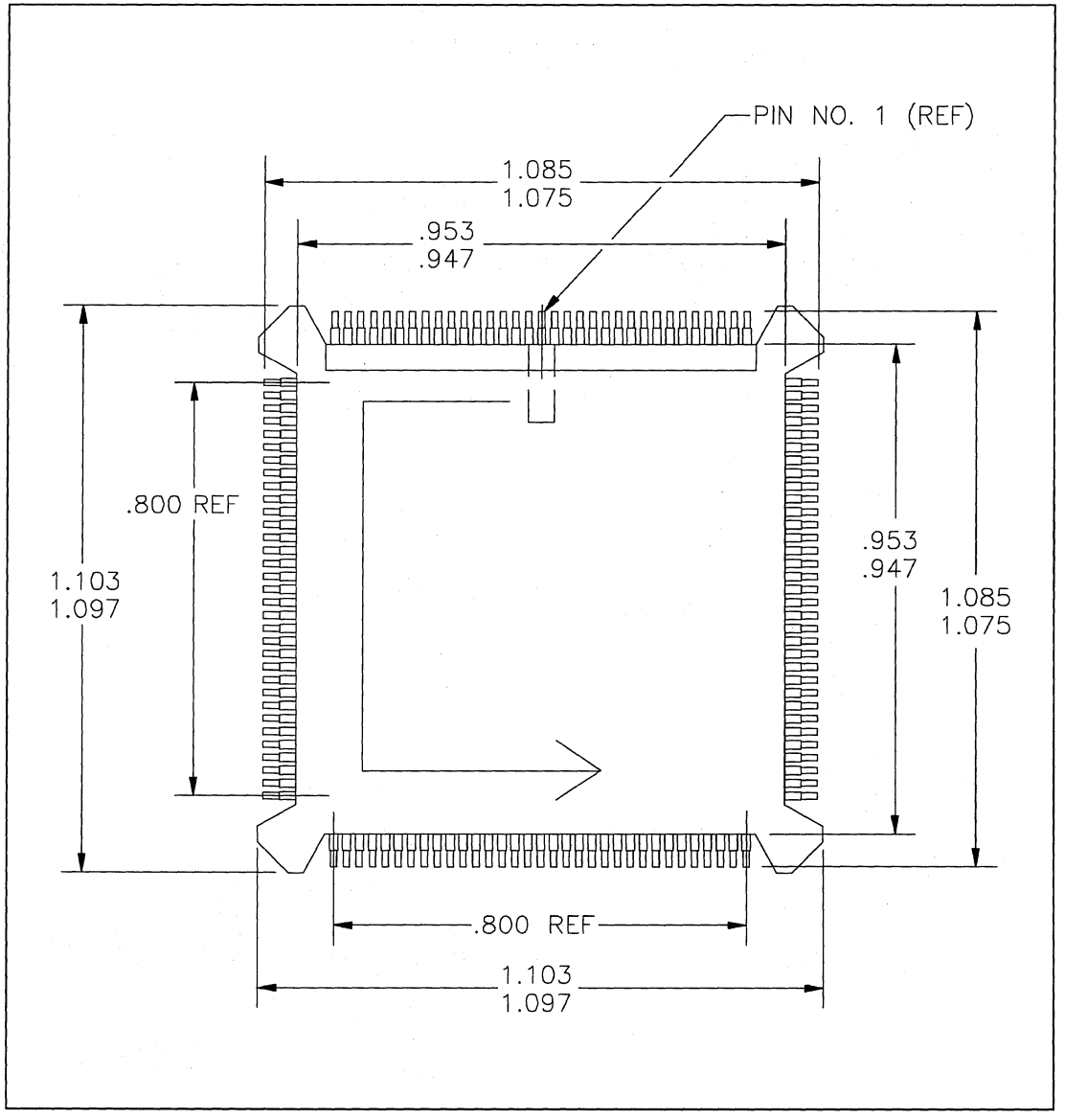
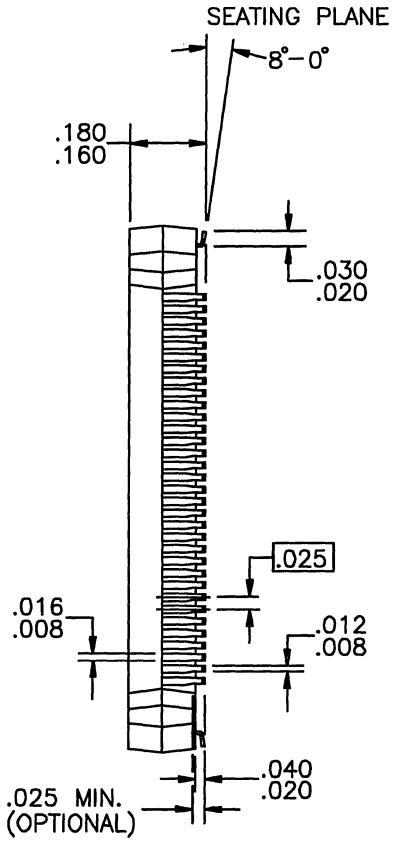
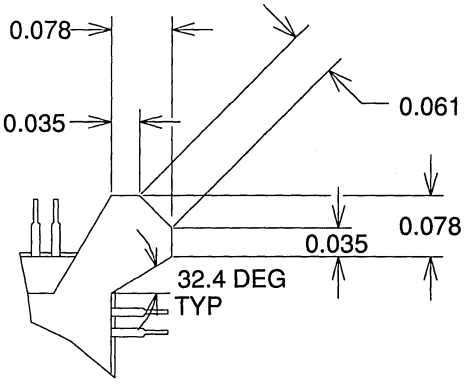


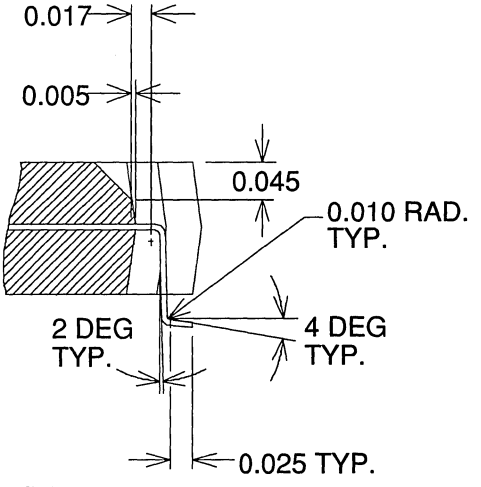
FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE



Side View



Bumper Detail



Detail A

FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE (CONTINUED)

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E.0 MAXIMUM RATINGS

Ambient temperature under bias	$0^{o}C$ to 70^{o} C
Storage temperature	$-40^{o}C$ to $125^{o}C$
Voltage on all inputs and outputs with respect to Vss	-0.3 to 6.5 Volts
Power dissipation	1.2 Watts
Power Supply Voltage	4.1 to 4.7 Volts

NOTE: Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to maximum rating conditions for extended periods may affect product reliability.

F.0 DIFFERENCES BETWEEN WD90C20 AND WD90C20A

The WD90C20A is a 0.9 micron version of the WD90C20 VGA controller chip. The submicron process design delivers reduced power consumption, true hardware vertical expansion, and an enhanced color palette for Super Twisted Nematic (STN) color LCDs.

Since the WD90C20A uses the smaller 0.9 micron geometry, smaller capacitances are required; therefore, a system designed with the WD90C20A uses less power than a comparable system using a 1.25 micron geometry VGA chip. Because the WD90C20A is pin-to-pin compatible with the WD90C20, you can keep your current designs and upgrade them for lower overall power consumption.

F.1 FUNCTIONAL CHANGES

- DC specifications for some of the output buffers have changed. See sections C.1 and F.4 for the WD90C20A DC specifications.
- Internal pullups on the SD bus are eliminated for the WD90C20A.
- The primary output $\overline{\text{MEMCS16}}$ is tristated when PWRDNN=0 and PR35(5)=1 for the WD90C20A.
- The continuous LP pulses during vertical blanking are now selectable on the WD90C20A for color LCDs (in addition to mono LCDs).

F.2 FEATURE ENHANCEMENTS FOR WD90C20A

F.2.1 DAC Enhancement

The WD90C20A DAC shuts off through software. Setting PR18(7)=0 enables the DAC to operate as normal; setting PR18(7)=1 forces the WD90C20A DAC to be shut off.

F.2.2 Micro Channel Interface Enhancement

The WD90C20A has additional support for the Micro Channel interface.If PR39(4)=0, then the default I/O cycle is selected.

If PR39(4)=1, then the synchronous-extended I/O cycle is selected.

F.2.3 Monochrome LCD Contrast Enhancement

Reverse video in text mode only and normal video in graphics mode.

If PR18 (4) = 0, then only normal video displayed.

If PR18 (4) = 1 and PR39 (3) = 0, then reverse video is displayed in both text and graphics modes. The WD90C22 also has this feature.

If PR18 (4) = 1 and PR39 (3) = 1, then reverse video is displayed only in text mode, while normal video is displayed in graphics mode.

PR39 (3)	PR18 (4)	TEXT	GRAPHICS
X	0	Normal	Normal
0	1	Reverse	Reverse
1	1	Reverse	Normal

X= don't care

F.2.4 Plasma Panel Support

Plasma panel support is not available for the WD90C20A.

F.2.5 Color LCD Display Enhancement

The WD90C20A increases the number of display colors from 512 to 4K for STN color LCDs.

The WD90C20A has simultaneous display of both the CRT and single panel color LCDs with vertical expansion and autocentering.

The LCD/CRT polarity is shown as follows:

In the WD90C20

DISPLAY MODE	$\overline{\text{LCD}}$/CRT
CRT only	H
Flat panel only	L

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In the WD90C20A

DISPLAY MODE	$\overline{LCD}$/CRT
CRT only	H
Flat panel only	L
Simultaneous display	L

The WD90C20A has multiplexed outputs for CRT VSYNC and CRT HSYNC.

For bit 2: Enable CRT VSYNC and CRT HYSNC
If PR39 (2) = 0, then LBDIR pin=LBDIR signal and HBDIR pin=HBDIR signal.

If PR39 (2) = 1, then LBDIR pin=CRT VSYNC signal and HBDIR pin=CRT HSYNC signal.
See the following table.

PR39 (2)	LBDIR	HBDIR
0	LBDIR	HBDIR
1	CRT VSYNC	CRT HSYNC

When the TFT panel is enabled, the polarities of CRT VSYNC and CRT HSYNC are now pulsed low, regardless of the values programmed in the Miscellaneous Output Register Bit 7 and Bit 6 in PR11(3).

The WD90C20A has programmable polarities of FP and LP.

For bit 1: FP Polarity Select.
If PR39 (1) = 0, then FP has normal polarity.
If PR39 (1) = 1 then FP has reverse polarity.

For bit 0: LP Polarity Select.
If PR39 (0) = 0, then LP has normal polarity.
If PR39 (0) = 1, then LP has reverse polarity.

PR39(1)	FP	PR39(0)	LP
0	Normal	0	Normal
1	Reverse	1	Reverse

The WD90C20A has software adjustment of HSYNC timings through PR19(7, 1,0). The WD90C20A and WD90C22 have the same timings for these signals.

PR19(7)	PR19(1)	PR19(0)	NUMBER OF VCLK DELAY
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

F.2.6 Power Management Enhancement

The WD90C20A dot clock dithering logic is stopped whenever the on-chip hardware dithering in not required. This can reduce the power dissipation by as much as 100mW.

The panel display data, VUD[3:0] and VLD[3:0], are set to logic low during reset or any of the powerdown modes to avoid potential current drain.

F.3 PERFORMANCE ENHANCEMENTS FOR WD90C20A

F.3.1 DAC Improvements

The WD90C20A's improved RAMDAC was redesigned to do the following:

- reduce power dissipation
- reduce overshoot and undershoot noise
- reduce ampflier gain error
- improve linearity
- increase yield

R_{SET} requires a new value resistor, which reduces both power dissipation and ampflier gain.

The new WD90C20A DAC specifications are in the table on the next page.

AC CHARACTERISTICS				
Parameter	**Min**	**Typ**	**Max**	**Units**
Analog output capacitance		80		pF
DAC switching speed			50	MHz
Output setting time (to ±1/4 LSB)		20		ns
Rise/fall time		3		ns
DC CHARACTERISTICS				
Resolution	6	6	6	bits
Accuracy (each DAC) Integral non-linearity (INL) Differential non-linearity (DNL) Gray scale error Monotonicity		 guaranteed	 ±1/2 ±1/2 ±5	 LSB LSB % full scale
LSB current 37.5 ohm load 50 ohm load		 296 222		 µA µA
Full scale current (each DAC) 37.5 ohm load 50 ohm load		 18.67 14		 mA mA
R_{SET} 37.5 ohm load 50 ohm load		 4320±1% 5760±1%		 ohm ohm
DAC to DAC matching			5	%
P_{TOTAL} (all three DACs) 37.5 ohm load		 230		mW
RECOMMENDED OPERATING CONDITIONS				
Power Supply AV_{DD}	4.5	5.0	5.5	volts
Pixel clock frequency f			50	MHz
Ambient temperature T_A	0		70	degrees C

TABLE F-1. WD90C20A RAMDAC SPECIFICATIONS

$$I_{FULL\ SCALE} = \frac{63 \times 1.036 \times V_{REF}}{R_{SET}}$$

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F.4 WD90C20A DC SPECIFICATIONS

Below are the updated WD90C20A DC specifications.

OUTPUT CAPACITANCE LOADING			
SIGNAL	**TRISTATE (Y/N)**	**MIN**	**MAX**
$\overline{\text{MEMCS16}}$	Yes		70 pF
OICHRDY	Yes		100 pF
$\overline{\text{EBROM}}$	No		40 pF
IRQ	Yes		70 pF
HBDIR	No		40 pF
LBDIR	No		40 pF
MA(7:0)	Yes	40 pF	70 pF
$\overline{\text{RAS10}}$	Yes	40 pF	70 pF
$\overline{\text{RAS32}}$	Yes	40 pF	70 pF
$\overline{\text{WE0}}$	Yes	40 pF	70 pF
$\overline{\text{WE1}}$	Yes	40 pF	70 pF
$\overline{\text{WE2}}$	Yes	40 pF	70 pF
$\overline{\text{WE3}}$	Yes	40 pF	70 pF
$\overline{\text{OE10}}$	Yes	40 pF	70 pF
$\overline{\text{OE32}}$	Yes	40 pF	70 pF
$\overline{\text{WPLT}}$	No		30 pF
$\overline{\text{RPLT}}$	No		30 pF
VUD(0:3)	Yes	20 pF	40 pF
VLD(0:3)	Yes	20 pF	40 pF
FR	Yes		40 pF
FP	Yes		40 pF
LP	Yes		40 pF
XSCLK	No		40 pF
PCLK	No		70 pF
WGTCLK	No		40 pF
$\overline{\text{LCD}}$	No		30 pF
SD(15:0)	Yes		70 pF
MD(15:0)	Yes		70 pF
$\overline{\text{CAS10}}$	Yes	40 pF	70 pF
$\overline{\text{CAS32}}$	Yes	40 pF	70 pF
VCLK1	---		30 pF
VCLK2	---		30 pF

TABLE F-2. WD90C20A DC SPECIFICATIONS

WD90C22

VGA Flat Panel

Display Controller

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

This data sheet describes the WD90C22 video controller. The WD90C22 is a VGA display controller that has been optimized for applications that require flat panel display support. It is an extension of the WD90C00 and as such supports all of the WD90C00's features and modes when driving a standard CRT. The WD90C22's highly integrated design includes a complete Micro Channel or AT compatible bus interface, as well as an on-chip PS/2 compatible RAMDAC with integral monitor detection logic. The controller's 1.25 micron CMOS construction and power management features significantly reduce the power required for the display subsystem.

Flat panel displays supported include all 640 by 480 monochrome and color liquid crystal displays (LCD), as well as plasma displays.

1.2 FEATURES

- On-chip Micro Channel interface
- On-chip 8- or 16-bit AT bus interface
- Direct interface with CRT and flat panel displays (monochrome and color TFT LCDs)
- On-chip frame rate modulation logic
- Supports all functions of WD90C00 VGA chip in CRT mode
- 64-shade gray scale mapping
- Software-selectable vertical screen centering
- Hardware vertical expansion*
- On-chip PS/2 compatible RAMDAC*
- On-chip monitor detection logic
- 32 MHz maximum LCD video clock
- 45 MHz maximum CRT video clock
- Flexible powerdown management features *
- Vcc may be removed in powered system
- 256 out of 4K or 256K color support for DTSN color LCD
  8 or 512 color support for TFT color LCD
- Four powerdown modes

* Patent pending

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2.0 THEORY OF OPERATION

The WD90C22 contains six major functional modules. In addition to the CRT controller, there is a sequencer, a graphics controller, an attribute controller, a flat panel interface, and a RAMDAC. The WD90C22 handles all display buffer management functions, including display refresh cycles, memory refresh cycles, and the arbitration and sequencing of host access cycles.

- **Sequencer**

The sequencer provides the display memory control signals and timing. It also provides the synchronization between the CRT controller and the attribute controller. The sequencer controls the arbitration between the CPU cycle and the CRT cycle, or the CPU cycle and the memory refresh cycle.

- **Graphics Controller**

The graphics controller manages data flow between video memory and the attribute controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the sequencer.

- **Attribute Controller**

The attribute controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video (as well as background or foreground video) in VGA and enhanced VGA BIOS modes.

- **Flat Panel Adapter**

The flat panel adapter section includes color-to-gray scale mapping*, a dithering mapping RAM, a dithering engine, a row buffer*, shading control*, and panel interface logic.
* Patent pending.

- **RAMDAC**

The WD90C22's on-board RAMDAC is a low power, PS/2-compatible device with special power-down modes and PS/2 monitor detection logic.

The RAMDAC's 256 by 18 color look-up table has triple 6-bit D/A converters, a pixel mask register, and composite blank generation on the three channels. It also supports the use of an external voltage reference. Without external buffering the RAMDAC will generate RS-343A-compatible video signals into a doubly terminated 75 Ohm load or a 50 Ohm load. Integral and differential linearity errors are a maximum of ± 1/2 LSB.

2.1 WD90C22 INTERFACES

The WD90C22 has five main system interfaces: the CPU, a display memory, a RAMDAC/CRT, a clock, and a flat panel display. In most implementations, these interfaces eliminate the need for glue logic.

- **CPU Interface**

The WD90C22 host interface supports both the AT and Micro Channel buses with both 8- and 16-bit data path widths. The WD90C22 may also be directly connected to the bus if drive requirements permit. The bus mode is determined by the status of the configuration register bit, CNF(2), which is loaded by the de-assertion of reset. The value that is loaded reflects the status of one of the memory data pins at reset.

I/O transfers to and from the device are 8 bits wide, and display memory transfers are 8 or 16 bits wide, depending on the video mode selected. Because of their architecture, EGA type planar modes are restricted to 8-bit display data transfers. Text and 256 color extended modes allow 16-bit transfers on a 16-bit bus.

The controller generates wait states as required during display memory accesses. Wait states are not generated for I/O or video BIOS ROM accesses. Special I/O ports, such as 46E8H (when in AT bus mode) for setup, and 102H for VGA enable, are internally implemented.

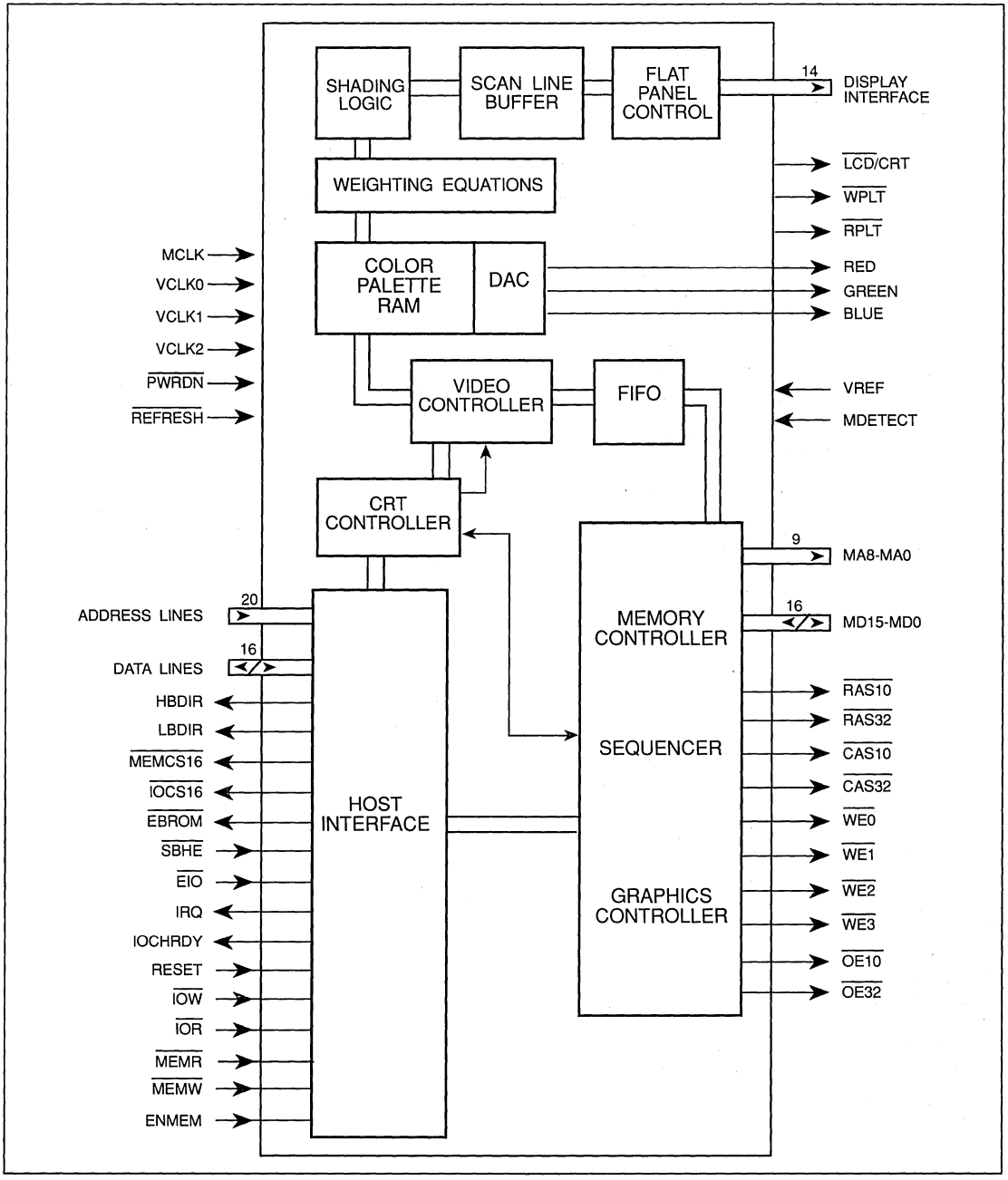

FIGURE 2-1. WD90C22 BLOCK DIAGRAM

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- **Display Memory Interface**

The WD90C22 generates all signals and memory timing required to operate the display memory. It directly controls three display memory sizes, 256 Kbyte, 512 Kbyte, and 1 Mbyte, as follows:

MEMORY SIZE	NUMBER AND TYPE OF DRAM REQUIRED
256 Kbytes	8 64 Kbyte by 4 DRAMs, or 2 64 Kbyte by 16 DRAMs
512 Kbytes	16 64 Kbyte by 4 DRAMs*, or 4 64 Kbyte by 16 DRAMs
1 Mbyte*	8 64 Kbyte by 16 DRAMs, or 8 256 Kbyte by 4 DRAMs

* Requires minimal support logic.

Page mode memories are required for all configurations. With a 36 MHz memory clock (MCLK), 120 ns devices may be used. If 256 color CRT modes are to be supported, 100 ns DRAMs and a 45 MHz MCLK are required. The WD90C22 includes special offset registers that allow the host to address up to 1 Mbyte of display memory.

- **CRT/RAMDAC Interface**

In addition to its internal RAMDAC, the WD90C22 allows the use of an external RAMDAC. This is helpful in specialized applications where a 24-bit wide color lookup table or pixel demultiplexing (to obtain higher video rates) is required. The external RAMDAC interface will support any Bt471/478/476 compatible device.

- **Clock Interface**

The WD90C22 has four clock input signal pins. Three of these (VCLK0, VCLK1, and VCLK2) are normally connected to oscillators. VCLK1 and VCLK2 may be configured to control an external clock multiplexor or clock generator, such as the WD90C61. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 36 MHz for 120 ns DRAMs or 45 MHz for 100 ns DRAMs.

- **Flat Panel Interface**

The WD90C22 is designed to interface with 640 by 480 LCD or Plasma panels. The flat panel interface lines change function to support the specific panel type chosen. Table 2-1 summarizes their use for each mode of operation.

When in LCD mode, with frame rate modulation selected, the controller supplies eight pixels per shift clock (four for the upper panel, and four for the lower). If pulse width modulation is selected, the controller provides two pixels per shift clock (one 4-bit pixel for the upper screen, and one 4-bit pixel for the lower screen).

When in Plasma mode, pulse width modulation is used to provide shading, while the controller supplies one pixel (four bits per pixel) per clock.

When in color STN LCD mode, the controller supplies two pixels per shift clock and uses hardware dithering. Each pixel (three bits, one each for R, G, and B), with dithering, provides 16 colors. The user can select: 256 out of 4K or 256K colors

LCD	PLASMA	CRT
UD (3:0)	VD (3:0)	P (7:4)
LD (3:0)	Reserved	P (3:0)
FR	Reserved	BLANK
FP	VS	VSYNC
LP	HS	HSYNC
XSCLK	XSCLK	Reserved
WGTCLK	ENABLE	Reserved
Reserved	Reserved	PCLK

TABLE 2-1. DISPLAY INTERFACE OUTPUT FUNCTIONS

MONOCHROME LCD	COLOR LCD WD90C22
UD (3)	R1
UD (2)	G1
UD (1)	B1
UD (0)	Border Information
LD (3)	R2
LD (2)	G2
LD (1)	B2
LD (0)	Reserved

TABLE 2-2. LCD DATA BIT ASSIGNMENTS

- **Power Up Configuration**

An internal 8-bit configuration register, CNF, controls the behavior of the major interfaces. Its bits are loaded with the inverted state of memory data lines 0 through 7 at the time RESET is deasserted. Pull-up or pull-down resistors on the MD lines are used to set the configuration.

3.0 FLAT PANEL SUPPORT CONSIDERATIONS

Supporting VGA compatible graphics on flat panel displays involves several non-trivial issues, including:

- Display Timing Differences
- Screen Size Mapping
- Color-to-Gray Scale Mapping
- Shading Mechanics
- Split Screen Refresh

The following paragraphs address each of these issues.

• Display Timing Differences

Typically, flat panel displays have different timing requirements from a CRT. To overcome this problem, the WD90C22 provides a set of hidden display timing registers, which are read/write protected in locked mode.

• Screen Size Mapping

Unlike those of a CRT, the pixels on a flat panel display are real, discrete entities of a fixed size. This can result in problems when different display modes are mapped onto a single panel. The WD90C22 has been designed to support VGA and various backward compatible display modes on a 640 by 480 dot flat panel and it provides integral hardware support to deal with screen size incompatibilities.

In case of backward compatible display modes, such as EGA, which has a maximum resolution of 640 by 350, the vertical resolution of the mode is less than the number of dots of vertical resolution of the panel. This results in an active display area that is smaller than that of the panel and shifted up on the display, as shown in Figure 3-1(A). There are two ways to enhance screen size mapping as described below.

The simplest approach, supported by the WD90C22 is to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel. In the case of an EGA 350 line mode being displayed on a 480 line panel, this would involve shifting the active display area down 65 lines (that is, 480 minus 350, the quantity divided by two). The effect of such a mapping is shown in Figure 3-1(B).

If the goal is to have the active display area fill the panel in all modes, then the active display area can be expanded by double scanning a portion of the active scan lines. Previously available controllers simply double scan lines at regular intervals, every third line in the case of EGA 350 line modes.

The WD90C22 uses an advanced proprietary algorithm that automatically expands to fill all 480 lines*. This algorithm can be used to support better "screen scrolling" when in 350 line modes.

* Patent pending on Hardware Vertical Expansion.

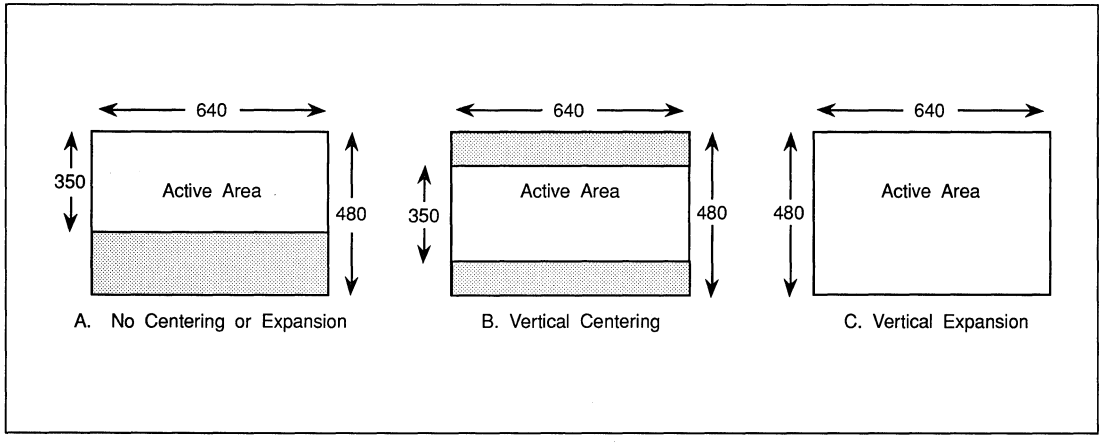

FIGURE 3-1. EXAMPLE OF SCREEN SIZE MAPPING

Under certain display conditions, any expansion scheme can result in undesirable aliasing effects of the displayed data. For this reason the WD90C22 allows the system designer flexibility to choose between vertical expansion or centering.

Horizontal resolution issues involve 720 dot modes such as VGA text and Hercules graphics. In VGA text mode, the 9th dot in each character box is dropped. The net effect is a slight compression in the spacing between characters. Alternatively, a different font may be loaded, although a nonstandard font size may not be fully compatible.

- **Color-to-Gray Scale Mapping**

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following RGB weighting equation:

$$I = .30R + .59G + .11B$$

Unfortunately, many of the currently available panels support at most sixteen shades and some only support two. In order to provide faithful support of all of the standard VGA modes on a flat panel, the WD90C22 provides a range of features to map colors to intensities and control panel shading. Foremost among these is sophisticated logic that converts gray scale values into dithering patterns. Additionally, the device allows software modification of the weighting values used in the gray scale mapping equation. Figure 3-2 gives an overview of the color-to-gray scale support provided by the WD90C22.

- **Shading Mechanics**

The WD90C22 supports shading via either frame rate or pulse width modulation. Pulse width modulation is handled via the display panel. The controller transfers 2, 3, or 4 bits per pixel to the driver logic on the panel, along with a high speed clock signal used to sequence the shading logic. Frame rate modulation, on the other hand, must be implemented in the display controller. The WD90C22 provides support for 2, 4, 8, 16, or 32 shade frame rate modulation with its integrated dithering controller. Any combination of dithering patterns can be selected via the dithering controller's mapping RAM. This design allows the WD90C22 to provide flicker-free frame rate modulation with frame rates as low as 70 Hz.

- **Split Screen Refresh**

The WD90C22 provides complete support for panels that are split into upper and lower panels requiring simultaneous refresh. This type of refresh is typically used by non-active matrix LCDs and plasma panels.

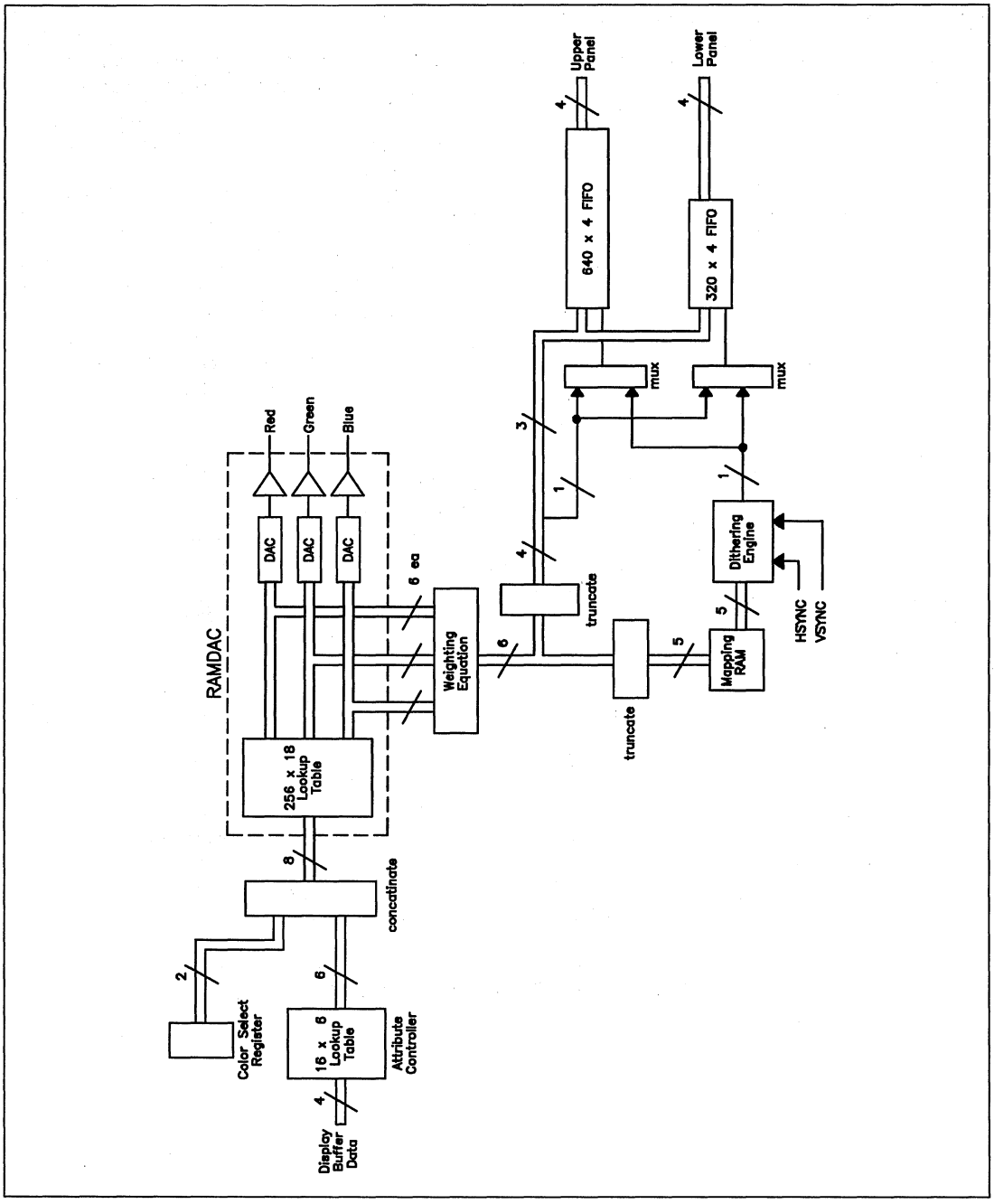

FIGURE 3-2. WD90C22 COLOR MAPPING

4.0 SIGNAL DESCRIPTION

Figure 4-1 illustrates the 132 plastic flat pack (PFP).

Table 4-1 lists all pins referenced in Figure 4-1 and provides a detailed description of each signal.

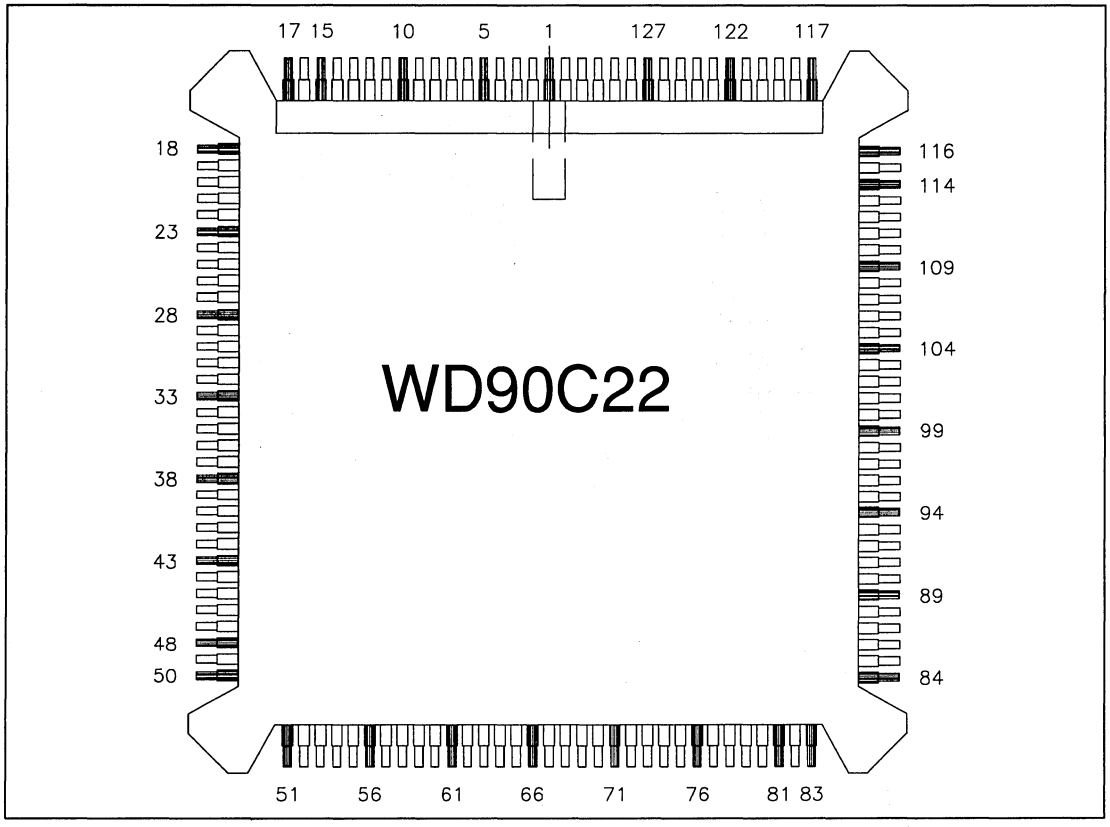

FIGURE 4-1. 132-PIN PFP (TOP VIEW)

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PIN	MNEMONIC	I/O	DESCRIPTION
			POWER ON
42	RESET	I	**Reset** This signal input will reset the WD90C22. MCLK and VCLK0 should be connected to the WD90C22 in order for the WD90C22 to initialize during reset. WD imaging registers, PR1 and CNF, are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/ pull-down resistors. The reset pulse width should be at least ten MCLK clock periods.
			CLOCK SELECTION
96	VCLK2	I/O	**Video Clock 2** This pin can be a third video display clock input or an output to the external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
97	VCLK1	I/O	**Video Clock 1** This pin can be a second video display clock input or an output to the external clock selection module. Pin direction is determined on reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
98	MCLK	I	**Memory Clock** This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system micro-processor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 45.0 MHz for 100 ns DRAMS.
99	VCLK0	I	**Video Clock 0** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
			HOST INTERFACE
1 - 2 117 - 122 124 - 132	SA15 - SA16 SA0 - SA5 SA6 - SA14	I	**Address Bus (SA16-SA0)** These active high inputs form the lower order 17 bits of video memory address. These inputs are directly connected to the system bus.

TABLE 4-1. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
3 - 5	LA17 - LA19	I	**Unlatched Address Bus (LA19 -LA17)** These active high inputs form the high-order three bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
6	SBHE	I	**System Byte High Enable** If SA0 is "0", this signal is used to enable 16-bit data transfer mode when SBHE is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]).
7	ENMEM	I	**Enable Memory** This line is driven by external decode logic. In AT mode, this signal is decoded by LA23 - LA20 and $\overline{\text{REFRESH}}$. In Micro Channel mode, this signal is decoded by LA23 - LA20 and MADE24 ("1" = enable).
8	$\overline{\text{EIO}}$/3C3D0	I	**Enable I/O** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0, and enables video subsystem memory and I/O address decoding ("1" = enable).
11	ALE $\overline{\text{CDSETUP}}$	I	**ALE** In AT mode, this line is ALE; in Micro Channel mode, it is driven by the host to individually select channel connector slots during system configuration and error recovery procedures.
12	IRQ/$\overline{\text{IRQ}}$	O	**Interrupt Request** Programmable processor interrupt request. It is enabled via Bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of the vertical display occurs, this signal goes active, causing an interrupt. It will stay latched until CRTC11 Bit 4 clears it. In an AT system IRQ is not connected, although you may connect it if you desire. $\overline{\text{IRQ9}}$ is used to generate an interrupt in Micro Channel mode. For further details, see the reference literature.
13	$\overline{\text{EBROM}}$ $\overline{\text{CDSFDBK}}$	O	**Enable BIOS ROM** In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). It is not active for access to addresses in the range C60000H-C67FFH, but this address range may be mapped-in by setting PR17 (0) = 0. A write to the WD90C22 internal I/O port address, 46E8H, causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping. In Micro Channel mode, this signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the addresses specified by the host.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

15

PIN	MNEMONIC	I/O	DESCRIPTION
14	$\overline{\text{MEMCS16}}$/ $\overline{\text{CDDS16}}$	O	**Memory Chip Select 16 Bits** In AT mode, this line is used to respond to the host to enable a 16-bit video memory data transfer. In Micro Channel mode, this line provides $\overline{\text{CDDS16}}$ for 16-bit video memory or I/O access.
15	IOCHRDY/ CDCHRDY	O	**Ready** An active high output which signals to the system processor that a memory access is complete. This signal is used only to add wait states to the bus cycles during video memory accesses. It is pulled inactive by the WD90C22 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
16	HBDIR	O	**High Byte Direction** This line is used to control the data direction of an external high byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles.
17	LBDIR	O	**Low Byte Direction** This line is used to control the data direction of an external low byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles.
19 - 26 29 - 36	SD15 - SD8 SD7 - SD0	I/O	**Data Bus (SD15 - SD0)** These bidirectional signals may either be connected directly to a local data bus requiring less than 8 ma. of source/sink, or may be connected through two external bus buffers.
38	$\overline{\text{MEMR}}$/ M/$\overline{\text{IO}}$	I	**Memory Read** In AT mode, this signal is called $\overline{\text{SMEMR}}$ and is an active low memory read strobe. It is asserted in 8-/16-bit memory read cycles. In Micro Channel mode, the signal is called M/$\overline{\text{IO}}$. It distinguishes between memory and I/O cycles. When (M/$\overline{\text{IO}}$) is high, a memory cycle is in process. A low on (M/$\overline{\text{IO}}$) shows that an I/O cycle is in process. For further details, refer to the reference literature.
39	$\overline{\text{MEMW}}$/ $\overline{\text{S0}}$	I	**Memory Write** The active low memory write strobe in AT mode for 8-/16-bit data transfers. In Micro Channel mode, it becomes $\overline{\text{S0}}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with the $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ and $\overline{\text{CMD}}$ signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
43	$\overline{\text{REFRESH}}$	I	**Refresh** This active low input pin is connected to the system $\overline{\text{REFRESH}}$ signal from the I/O bus.
40	$\overline{\text{IOR}}$/ $\overline{\text{S1}}$	I	**I/O Read** Active low I/O read strobe in AT mode. It is asserted in 8-/16-bit I/O read bus cycles. $\overline{\text{S1}}$ is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.
41	$\overline{\text{IOW}}$/ $\overline{\text{CMD}}$	I	**I/O Write** Active low strobe. In AT mode, the strobe signals an I/O write for 8-/16-bit I/O write cycles. In Micro Channel mode it is synonymous with $\overline{\text{CMD}}$; address bus validity is signaled by $\overline{\text{CMD}}$ going low while the rising edge of $\overline{\text{CMD}}$ indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
			DISPLAY MEMORY INTERFACE
45 - 52 55	MA0 - MA7 MA8	O	**Memory Address (MA0 - MA8)** Display memory DRAM address.
56	$\overline{\text{RAS10}}$	O	**Row Address Strobe** Active low Memory Maps 1 and 0 RAS output signal.
57	$\overline{\text{RAS32}}$	O	**Row Address Strobe** Active low Memory Maps 3 and 2 RAS output signal.
58	$\overline{\text{CAS10}}$	O	**Column Address Strobe** Active low Memory Maps 1 and 0 CAS output signal.
59	$\overline{\text{CAS32}}$	O	**Column Address Strobe** Active low Memory Maps 3 and 2 CAS output signal.
60	$\overline{\text{WE0}}$	O	**Write Enable** Active low Memory Map 0 DRAM write enable signal.
61	$\overline{\text{WE1}}$	O	**Write Enable** Active low Memory Map 1 DRAM write enable signal.
62	$\overline{\text{WE2}}$	O	**Write Enable** Active low, Memory Map 2 write enable signal.
63	$\overline{\text{WE3}}$	O	**Write Enable** Active low, Memory Map 3 write enable signal.
64	$\overline{\text{OE10}}$	O	**Output Enable** Active low, Memory Maps 1 and 0 output enable signal.
65	$\overline{\text{OE32}}$	O	**Output Enable** Active low, Memory Maps 3 and 2 output enable signal.
68-75 77-84	MD15 - MD8 MD7 - MD0	I/O	**Data Lines** Lines MD15 through MD0 are the data bus to the video display DRAMS. Data lines MD0 through MD15 are pulled up or down with resistors to provide setup information on power-up (reset) as shown in Table 4-2.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS
44	$\overline{\text{PWRDN}}$	I	**Power Down Selected** This active low input signal is used to disable screen refresh cycle.
110	LCD/$\overline{\text{CRT}}$	O	**LCD or CRT Selected** This active high output is used to power down an external RAM-DAC chip whenever the WD90C22 operates in LCD mode. "1" is CRT mode, and "0" is LCD mode.
			*DISPLAY INTERFACE**
86	PCLK	O	**Pixel Clock** This line is used to clock the video outputs into a RAMDAC in a CRT interface.
87	XSCLK	O	**Shift Clock** In an LCD interface, this signal is used to shift the upper and lower panel's data into the X-driver. In a Plasma interface, this signal is also used as shift clock.
88	WGTCLK	O	**Weight Control Clock** In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "ENABLE VIDEO" signal.
89	LP/HSYNC	O	**Latch Pulse** In an LCD interface, this signal is used to latch all the data in the current scan line. In either a Plasma or a CRT interface, this signal is used for horizontal sync.
90	FP/VSYNC	O	**Frame Pulse** This signal is used to indicate the start of scanning to the Y-driver in an LCD interface. In either a Plasma or a CRT interface, this signal is used for vertical sync.
91	FR/BLANK	O	**Frame Control** In an LCD interface, it is an AC signal which is toggled every frame. In a CRT interface, it is the $\overline{\text{BLANK}}$ signal. Some panels call this signal "M."
103 - 100	LD3 - LD0	O	**Lower Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the lower panel data bus. In a Plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAM-DAC.
107 - 104	UD3 - UD0	O	**Upper Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the upper panel data bus. In a Plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

*The display interface functions are redefined for each display mode – see Table 2-1 on page 4 for details.

PIN	MNEMONIC	I/O	DESCRIPTION
			RAMDAC INTERFACE
92	$\overline{\text{RPLT}}$ /	O	**Read Palette** Video DAC register and color palette read signal. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H. This line is active in both internal and external RAMDAC configurations.
	VD9		**Video Data Bit 9** In color TFT mode, this is the ninth data bit of the LCD interface.
93	$\overline{\text{WPLT}}$	O	**$\overline{\text{Write Palette}}$** Video DAC register and color palette write signal. Active low during an I/O write to addresses 3C6H-3C9H. This line is active in both internal and external RAMDAC configurations.
111	VREF	I	**Voltage Reference Input** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC. Grounding this pin changes the function of pin 112 and disables the internal RAMDAC so that the WD90C22 can be used with an external RAMDAC.
112	MDETECT/	I	**Monitor Detect** When pin 111 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2H Bit 4.
	FSADJUST		**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DAC's.
114	BLUE	O	**Blue Current Output** High impedance current source can directly drive a doubly-terminated 75-ohm coaxial cable.
115	GREEN	O	**Green Current Output** High impedance current source can directly drive a doubly-terminated 75-ohm coaxial cable.
116	RED	O	**Red Current Output** High impedance current source can directly drive a doubly-terminated 75-ohm coaxial cable.
			POWER AND GROUND
9,28, 53, 67, 94	Vcc	-	**Power**
10,18, 27,37,54, 66,76,85, 95	GND	-	**Ground**
123	AVcc	-	**+ 5VDC** - ANALOG (See Figure 4-2)
113	AGND	-	**Ground** - ANALOG (See Figure 4-2)
108	RVcc	-	**RAMDAC power** (See Figure 4-2)
	RGND	-	**RAMDAC ground** (See Figure 4-2)

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

15

WD90C22	
Pin	**Pullup/Pulldown Type**
SD [15:0]	PU
LA [19:17]	
SA [16:0]	PD
MEMEN	PD

PU = 100K Ohm Nominal, PD = 200K Ohm Nominal

MEMORY DATA LINE	POWER-UP FUNCTION	DATA STORED AT NAME	PORT
MD15	EGA SW4 / LCD Select*	PR11(7)**	3?5.2A.7
MD14	EGA SW3	PR11(6)**	3?5.2A.6
MD13	EGA SW2	PR11(5)**	3?5.2A.5
MD12	EGA SW1	PR11(4)**	3?5.2A.4
MD11	ANALOG/TTL Display	PR5(3)**	3CF.0F.3
MD10	–	–	–
MD9	Panel Select Bit 1	PR18(1)**	3?5.31.1
MD8	Panel Select Bit 0	PR18(0)**	3?5.31.0
MD7	General Purpose	PR5(7)***	3CF.0F.7
MD6	General Purpose	PR5(6)***	3CF.0F.6
MD5	General Purpose	PR5(5)***	3CF.0F.5
MD4	General Purpose	PR5(4)***	3CF.0F.4
MD3	VCLK1,2 (I/O)	None**	–
MD2	AT/Micro Channel Mode	None**	–
MD1	–	PR1(1)***	3CF.0B.1
MD0	BIOS ROM Mapping	PR1(0)***	3CF.0B.0

TABLE 4-2. PR REGISTER FUNCTIONS

NOTES:
Data lines MD0 - MD15 are pulled up or down with resistors to provide setup information on power-up (reset) as shown above.

* PR11(7) = 0 : mono LCD, PR11(7) = 1 : color LCD.
** Pullup resistor sets these bits to logic 1.
*** Pulldown resistor sets these bits to logic 1.

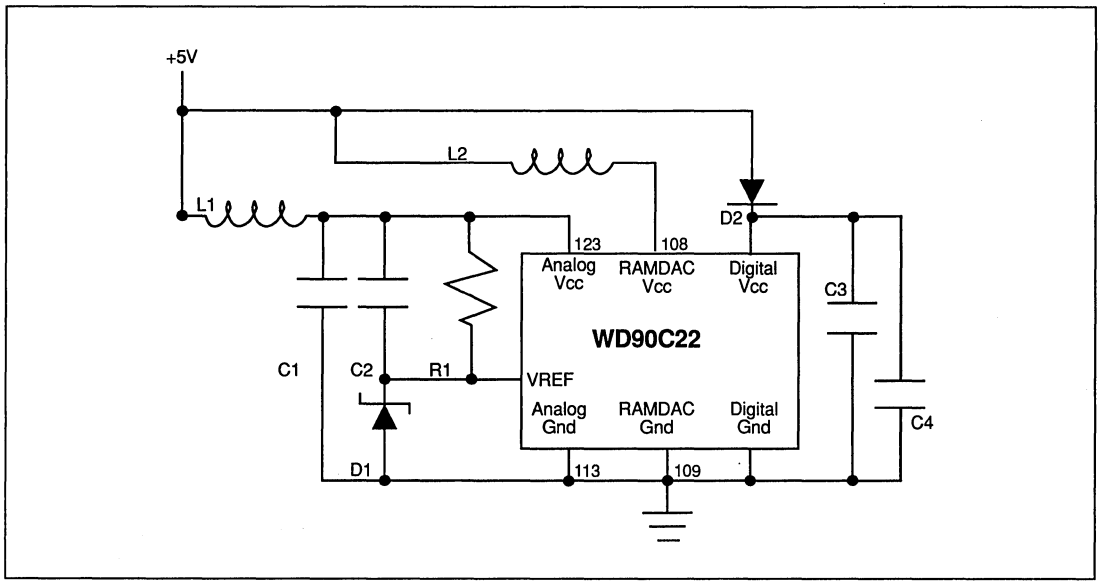

FIGURE 4-2. POWER DISTRIBUTION FOR WD90C22

COMPONENT	RECOMMENDED COMPONENT VALUE	SUGGESTED PART NUMBER/ COMMENTS
C1	0.1 UF	Reduces noise in analog portion of chip.
C2	0.1 UF	Stablizes VREF voltage.
C3	5 by 0.1 UF One each for Pins 9, 28, 53, 67, 94	Reduces noise to the VGA core.
C4	22 UF	Bulk decoupling.
D1	LM385	1.2 volt voltage reference.
D2	MBR150 (MBRL040-SMT) MBR160, or 2 1N5817s in series	Reduces voltage to digital portion of chip (40-50 mA reduction in current)
L1	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to analog portions of WD90C22.
L2	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to RAMDAC. No decoupling capacitor is to be used at Pin 108.

TABLE 4-3. RECOMMENDED COMPONENT VALUE

15

5.0 WD90C22 REGISTERS

All standard IBM registers incorporated in the WD90C22 are functionally equivalent to the VGA implementation, while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards using the 6845 CRT Controller. This section describes the VGA registers (and the differences between VGA and EGA), as well as the PR registers.

5.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
NOTE: *Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Red Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 5-1. VGA REGISTERS SUMMARY

5.2 COMPATIBILITY REGISTERS

FUNCTIONS	RW[1]	MDA[2]	CGA[2]	AT&T[2]	HERCULES[2]
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
CRTC[3]	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 5-2. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. 6845 Mode Registers.

15

5.3 VGA REGISTERS

This section describes the VGA registers.

5.4 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:
1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.4.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

* These bits determine the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz in CRT mode).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz in CRT mode) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

5.4.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

The DAC output currents, I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. The output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

The results of the monitor detection circuitry is readable at port 3C2H Bit 4. (See Figure B-1) It is important that this output signal be read during active video ouput, not during retrace or any other blanking period.

Bit(3:0)

Reserved.

5.4.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register Bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.4.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control.
0 = Vsync output enabled.
1 = Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved.

5.5 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to 0.

5.5.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

5.5.2 Reset Register, Read/Write Port = 3C5, Index = 00H

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

5.5.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01H

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection.
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels wide).

Bit 2

Shift Load. Effective only if Bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

15

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

5.5.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing to Memory Maps (0-3), respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

5.5.5 Character Map Select Register, Read/Write Port = 3C5, Index = 03H

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 Bit 1 is 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. "0" selects character map B. "1" selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5), and Bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A, along with Bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.
The MSB of character map B, along with Bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit(3:2)

Character Map Select A.
Refer to Bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to Bit 4 table.

5.5.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04H

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0

Reserved.

5.6 CRT CONTROLLER REGISTERS

PORT[1]	INDEX	VGA REGISTER NAME	6845 REG NAME[2]
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	See note 3.
3?5	03	End Horizontal Blanking	See note 3.
3?5	04	Start Horizontal Retrace	See note 3.
3?5	05	End Horizontal Retrace	See note 3.
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	See note 3.
3?5	08	Preset Row Scan	See note 3.
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	See note 3.
3?5	14	Underline Location	See note 3.
3?5	15	Start Vertical Blank	See note 3.
3?5	16	End Vertical Blank	See note 3.
3?5	17	CRTC Mode Control	See note 3.
3?5	18	Line Compare	See note 3.

TABLE 5-3. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   ?= B in monochrome modes.
   ?= D in color modes.

2. 6845 Mode Registers are defined and explained in greater in the reference literature.

3. This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

5.6.1 CRT Address Register, Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

5.6.2 Horizontal Total Register, Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the horizontal total period is the total of the character count in the active display plus the character count in the retrace time less 5, per horizontal scan line.

5.6.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total number of displayed characters less one is programmed into this register.

Horizontal overscan begins when the horizontal character counter reaches this character clock value.

5.6.4 Start Horizontal Blanking Register, Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the hexidecimal value in the character clocks in this register. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.5 End Horizontal Blanking, Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

Bit 7

Reserved.

Bit(6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

15

Bit (4:0)

End Horizontal Blanking.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Blanking and the desired width of the horizontal blanking in character clocks. The least significant five bits are programmed into this register, while the sixth most significant bit is the End Horizontal Retrace register (index 05H) Bit 7. When the least significant six bits of the horizontal character counter match these six bits, the horizontal blanking is ended.

5.6.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.7 End Horizontal Retrace Register, Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

Bit 7

MSB (sixth bit) of the End Horizontal Blanking register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Retrace and the desired width of the horizontal retrace in character clocks. The least significant five bits are programmed into this register. When the least significant five bits of the horizontal character counter match these five bits, the horizontal retrace signal is turned off.

5.6.8 Vertical Total Register, Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant 8 bits of a 10-bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) Bit 0 and Bit 5, respectively. In 6845 modes, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H Bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0

Vertical Total Bit 8 (index = 06H).

NOTES:

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register Bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

5.6.10 Preset Row Scan Register, Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

5.6.11 Maximum Scan Line Register, Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4 - 0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is Bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, Bits 5 through 7 are reserved, and Bits 4 through 0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

5.6.12 Cursor Start Register, Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. They contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, Bit 7 is reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value. Bit 6 is not used.

5.6.13 Cursor End Register, Read/Write, Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks; e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, Bits 7 through 5 are reserved and Bits 4 through 0 contain the row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode; i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

5.6.14 Start Address High Register, Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16-bit video memory address used for screen refresh. The low order 8-bit register is at index 0DH. The PR Register PR3 Bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes Bits 6 and 7 are forced to "0" regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

5.6.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

5.6.16 Cursor Location High Register, Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, Bits 6 and 7 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

5.6.17 Cursor Location Low Register, Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

5.6.18 Vertical Retrace Start Register, Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the 10-bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 through 0 as the light pen read back value, and Bits 6 and 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

5.6.19 Vertical Retrace End Register, Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
These bits specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add the number of scan count for "W" to the value of the Vertical Retrace Start register. The least significant four bits of the result are written in the Vertical Retrace End register. When the least significant four bits of the vertical scan line counter match these four bits, the vertical retrace signal is turned off.

5.6.20 Vertical Display Enable End Register, Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower 8 bits)

Bit(7:0)

Vertical Display Enable End Lower 8 Bits.
The lower eight bits of 10-bit register that defines where the active display frame ends.

The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

5.6.21 Offset Register, Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen Width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or doubleword display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

5.6.22 Underline Location Register, Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

5.6.23 Start Vertical Blank Register, Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the 10-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). The 10-bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

5.6.24 End Vertical Blank Register, Read/write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank Inactive Count.
End Vertical Blank is an 8-bit value calculated as follows:

8-bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) +
(value of vertical blank signal width in scan lines).

When the least significant eight bits of the vertical scan line counter match these eight bits, the vertical blank signal is turned off.

5.6.25 CRT Mode Control Register, Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1-bit and the MSB of the address counter appears on the LSB. See the table on the next page.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

* See Bit 5, defining address wrap. This table is applicable only when PR Register PR1 Bits 7 and 6 equal 0, or PR16 Bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) Bit 6 controls addressing. See the following table.

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.

1 = Select MA15 for odd/even mode when 256 Kbyte of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2.

0 = Character clock increments memory address counter.

1 = Character clock divided by 2 increments the address counter.

15

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter Bit 1 as output at MA14 address pin.
1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller Compatibility Mode Support for CGA Operation.

0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

5.6.26 Line Compare Register, Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower 8 Bits.
Lower 8 bits of the 10-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.7 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE: Reserved bits should be set to 0.

5.7.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.7.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) Bit 1 and Bit 0.

5.7.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

5.7.4 Color Compare Register, Read/Write PORT 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.7.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
This specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

5.7.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. This operation has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 and 1 or value 10b or 11 to select the chained maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

5.7.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode Bit 1
0	Write Mode Bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to 6 bits through internal palette and is sent out on the lower 6-bit pins (VID5 - VID0) every dot clock. The remaining two video outputs (VID6, VID7) are determined by Bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 – Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.

The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the 8 bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.7.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0.
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128 Kbyte
0	1	A000:0H-AFFF:FH	64 Kbyte
1	0	B000:0H-B7FF:FH	32 Kbyte
1	1	B800:0H-BFFF:FH	32 Kbyte

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.7.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

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5.7.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

The bit mask operation applies simultaneously to all four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation affects any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.8 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3C0	——	Index Register
3C0	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes.
1 = D in Color Modes.

5.8.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read through address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0, but does not toggle for reads to address 3C1.

5.8.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

BIT	FUNCTION
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

5.8.3 Attribute Mode Control Register, Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line Compare will have no effect on the PEL Panning Register.
1 = Allows a successful Line Compare to disable the PEL Panning Register and also Bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

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Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to 0 for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

5.8.4 Overscan Color Register, Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

5.8.5 Color Plane Enable Register, Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select two out of eight color outputs which can be read by the Input Status Register 1 (port = 03?A) Bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

5.8.6 Horizontal PEL Panning Register, Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 Dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

5.8.7 Color Select Register, Read Port 3C1/Write Port 3C0, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers to create 8-bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

5.9 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.9.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 4

Reserved.

Bit 3

Video Enable.
0 = Video disable.
1 = Video activated.

Bit 2

Reserved.

Bit 1

Port 3BFH Enable.
0 = Prevents setting of Port 3BF Bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh Bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode (should be 1).
0 = High resolution disabled.
1 = High resolution is enabled.

5.9.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its Bits 0 and 1.

5.9.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6,4,2)

Reserved.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF Bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF Bit 0 to switch for the alpha or graphics mode selection.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 3

Video Enable.
0 = Video disable.
1 = Video enable.

Bit 0

High Resolution (should be 1).
0 = High resolution disabled.
1 = High resolution enabled.

5.9.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) Bit 7 selects the displayed memory page address in the graphics mode. When it is reset, Bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) Bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.9.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

5.9.6 CGA Color Select Register, Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

5.9.7 CRT Status Register, MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

5.9.8 CRT Status Register, CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

5.9.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to 0 by reset. This register is enabled by setting Bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

5.10 WD90C22 PR REGISTERS

NAME	RW [1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0A(6:0)	3CF.09	5.10.1
Alternate Address Offset B	RW	PR0B(6:0)	3CF.0A	5.10.1
Memory Size	RW	PR1(7:0)	3CF.0B	5.10.2
Video Select	RW	PR2(7:0)	3CF.0C	5.10.3
CRT Control and Group Locking	RW	PR3(7:0)	3CF.0D	5.10.4
Video Control	RW	PR4(7:0)	3CF.0E	5.10.5
Unlock PR0-PR4	RW	PR5(7:0)	3CF.0F	5.10.6
Unlock PR11 - PR17	RW	PR10(7:0)	3?5.29[4]	5.10.7
EGA Switches	RW	PR11(7:0)	3?5.2A	5.10.8
Scratch Pad	RW	PR12(7:0)	3?5.2B	5.10.9
Interlace H/2 Start	RW	PR13(7:0)	3?5.2C	5.10.10
Interlace H/2 End	RW	PR14(7:0)	3?5.2D	5.10.11
Miscellaneous Control 1	RW	PR15(7:0)	3?5.2E	5.10.12
Miscellaneous Control 2	RW	PR16(7:0)	3?5.2F	5.10.13
Miscellaneous Control 3	RW	PR17(1:0)	3?5.30	5.10.14
Flat Panel Status	RW[5,6]	PR18(7:0)	3?5.31	5.10.15
Flat Panel Control I	RW	PR19(7:0)	3?5.32	5.10.16
Flat Panel Control II	RW	PR1A(7:0)	3?5.33	5.10.17
Flat Panel Unlock	RW	PR1B(7:0)	3?5.34	5.10.18
Mapping RAM Unlock	RW	PR30(7:0)	3?5.35	5.10.19
Mapping RAM Address Counter	RW	PR33(7:0)	3?5.38	5.10.20
Mapping RAM Data	RW	PR34(7:0)	3?5.39	5.10.21
Mapping RAM Control	RW[6]	PR35(1:0)	3?5.3A	5.10.22
LCD Panel Height Select	RW	PR36(7:0)	3?5.3B	5.10.23
Flat Panel Blinking Control	RW	PR37(7:0)	3?5.3C	5.10.24
Color LCD Control	RW	PR39(7:0)	3?5.3E	5.10.25
Vertical Expansion Initial Value	RW	PR41(7:0)	3?5.37	5.10.26
PR43 Unlock Register	WO	PR42(7:0)	3C5.06	5.10.27
Paradise VGA Status	RW	PR43(7:0)	3C5.07	5.10.28
Power-Down Memory Refresh	RW	PR44(7:0)	3?5.3F	5.10.29
CNF Configuration	HARD[6]	–	–	

TABLE 5-4. PR REGISTERS SUMMARY

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = read/Write.
2. In the PR register notation, XXX.YY, XXX is the data port address and YY is the register index.
3. All register addresses are in hex.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. The register bits (1:0) are loaded as CNF (10:9) upon reset.
6. Not all bits are readable.

The WD90C22 has additional features that enhance the performance and function of the Western Digital WD90C00 and basic VGA subsystem.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write-protected at power-up by the hardware reset. In order to load these registers, the appropriate unlock register, PR5 or PR10, must be loaded first with binary XXXXX101; the register remains unlocked until any other value is written to it. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power-up by hardware reset. To read registers PR10 through PR17, load PR10 with 1XXX0XXX. The registers remain readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them shows data to be FFH. Setting PR4 Bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power-on reset except where noted.

5.10.1 Address Offset Registers, PR0A & PR0B

PR0A - Address Offset Register A, Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B, Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C22 can control up to 1 Mbyte of video RAM. However, the memory map for IBM PC and compatibles assigns 128 Kbytes of the available 1 Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. This space is further limited to a 64 Kbyte video memory partition to allow a second video card to co-exist.

The WD90C22 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 Bit 3 is set to 1. PR0A and PR0B provide a 7-bit offset that is added to address Bits A (18:12) of the system address to form a 20-bit address. The arrangement is similar to that of the segment register DS and ES of the 8088/80X86 architecture, with PR0A and PR0B providing 4 Kbyte segments.

In a 64 Kbyte VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), when PR0B is enabled by setting PR1 Bit 3 = 1, PR address offset registers, PR0A and Alternate Offset Address register (PR0B), may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H–AFFF:FH while PR0B is mapped from A000:0H–A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register Bits 3 and 2) and the Alternate Offset register is enabled, PR0A is mapped from B000:0H-BFFF:FH, while PR0B is mapped from A000:0H-AFFF:FH.

5.10.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map Select
3	Enable Alternate Address Offset Register PROB
2	16-Bit Video Memory
1	Reserved
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1 (1:0) are latched internally at power-on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6
Memory Size.
256 Kbyte of available VGA video memory space is divided into four 64 Kbyte maps (0-3), each defining bit planes (0-3). In mode 13, the 4-bit planes are chained to form one large bit plane. The starting address of the 256 Kbyte video memory buffer can be configured to match other video adapters and/or application programs. WD90C22 enhances memory size capability when Bits 6 and 7 are programmed to extend video buffer size to 512 Kbyte or 1024 Kbyte.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64 Kbyte by 4	N/U	256 Kbyte	4 (64 Kbyte Per Plane)
64 Kbyte by 4	BANK SELECT	512 Kbyte	4 (128 Kbyte Per Plane)
256 Kbyte by 4	DRAM PIN A8	1024 Kbyte	4 (256 Kbyte Per Plane)

The DRAM organizations supported by the WD90C22 and its associated video space are shown in the table at the bottom of the page.

When video memory size is 512 Kbyte, and 64 Kbyte by 4 DRAMs are used, two banks of 64 Kbyte form 128 Kbyte per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the CAS10N and CAS32N signals. Four planes form the desired 512 Kbyte video memory space. For 1024 Kbyte video memory size, MA8 is directly connected to the A8 address pin of the 256 Kbyte by 4 DRAMS, and two DRAMS form a 256 Kbyte space per plane. Four planes make the desired 1024 Kbyte video memory space.

PR1 Bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is the same as IBM VGA regardless of PR1 (6) and PR1(7).

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 Kbyte Standard VGA	VGA*
0	1	0	256 Kbyte WDI VGA	PVGA**
1	0	0	512 Kbyte WDI VGA	PVGA
1	1	0	1024 Kbyte WDI VGA	PVGA
X	X	1	Any Of The Above	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
**WDI extended modes can fully utilize up to 256 Kbytes.

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RAM ADDRESSING:

PR1(7) PR1(6)

0 0 256 Kbyte Total; 64 Kbyte Plane; IBM VGA Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(50)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:

PR1(7) PR1(6)

0 1 256 Kbyte Total; 64 Kbyte Plane; WD90C22 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 0 512 Kbyte Total; 128 Kbyte/Plane; WD90C22 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
*						
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 1 1024 Kbyte Total In 4 Planes; 256 Kbyte/Plane; WD90C22 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16) *	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:
1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 Bit 3 or Bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 Bit 5 = 0.

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BIT 5	BIT 4	MEMORY MAP
0	0	VGA Mapping in 64 Kbyte space - A000:0H to BFFF:FH Address Range
0	1	First 256 Kbyte in 1 Mbyte space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 Kbyte in 1 Mbyte space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 Kbyte in greater or equal to 1 Mbyte space - 0000:0H to FFFF:FH Address Range

Bit 3

Enable Alternate Address Offset Register PR0B.

Bit 2

Enable 16-Bit Bus for Video Memory.
When set to 1, DS16N will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have DS16 inactive.

Bit 1

Reserved. Set to 0.

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-up resistor latches 0 after power-up. A pull-up on MD(0) sets this bit to 0 at power-on reset.

5.10.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register and Mode.

Bit 6

0: VGA or EGA mode.
1: Non-VGA (6845) mode.

Bit 5

Character Map Select.
The following functions are overridden by setting PR15(2). This bit, in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected according to the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE: Setting PR15(2) = 1, i.e., selecting "page mode addressing" overrides the "plane selected" table shown above.

Bit(4:3)

Character Clock Period Control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE: The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and Character Map Select.
Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., Programming 1 gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are available. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, setting this bit locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK. Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

5.10.4 PR3 - CRT Lock Control Register, Read/Write Port=3CF, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e., the IBM Vertical Retrace End Register Bit 7 controlled by index register 11). When Bit 7 is 1, CRT controller registers (R0-7) are write protected by VGA definition. Information on the five groups, and their locking schemes, is provided below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1.
CRT Controller Register 00
–Horizontal Total Characters per scan
CRT Controller Register 01
–Horizontal Display Enable End
CRT Controller Register 02
–Start Horizontal Blanking
CRT Controller Register 03
–End Horizontal Blanking
CRT Controller Register 04
–Start Horizontal Retrace
CRT Controller Register 05
–End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1.
CRT Controller Register 07(Bit6)
–Vert. Display Enable End bit 9
CRT Controller Register 07(Bit1)
–Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1.
CRT Controller Register 06
– Vertical Total
CRT Controller Register 07(Bit7)
–Vertical Retrace Start bit 9
CRT Controller Register 07(Bit5)
–Vertical Total bit 9
CRT Controller Register 07(Bit3)
–Start Vertical Blank bit 8
CRT Controller Register 07(Bit2)
–Vertical Retrace Start bit 8
CRT Controller Register 07(Bit0)
–Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1.
CRT Controller Register 09(Bit5)
–Start Vertical Blank bit 9
CRT Controller Register 10
–Vertical Retrace Start
CRT Controller Register 11 [Bits(3:0)]
–Vertical Retrace End
CRT Controller Register 15
–Start Vertical Blanking
CRT Controller Register 16
–End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1.
CRTC mode Control Register 17(Bit2)
–Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 Bit 7.

Bit 6

Lock HSYNC polarity, as programmed in 3C2 Bit 6.

Bit 5

Lock Horizontal Timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 Bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address register values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 Bit 7=1.

Bit 0

Lock Vertical Timing.
1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 Bit 7=0.

5.10.5 PR4- Video Control Register, Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register Control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$.
Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. One of two types of display enable timings can be selected; the choice is determined by PR15(1).

Bit 6

Select PCLK Equal to VCLK.
0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

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Bit 4

Tri-state the Memory Control Outputs.
The memory address bus, MA(8:0), and all ten DRAM control signals, are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" Bit 3 of mode register 3D8, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal Palette and Overscan Registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) Bit 1 is 0) 3C0 register is read/write while 3C1 register is read only, according to the Attribute Controller register definitions.

Bit 0

Shift Register Control.
This bit configures the video shift registers for 256-color mode.

5.10.6 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 through PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register Bits 4 through 8. Setting PR(4) Bit 1 to 1 read protects registers PR0 through PR5.

BIT	FUNCTION
7	CNF(7) [READ ONLY]
6	CNF(6) [READ ONLY]
5	CNF(5) [READ ONLY]
4	CNF(4) [READ ONLY]
3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits are cleared to 0 by reset. They control writing to PR registers PR0 through PR4 as follows:

2	1	0	PR0-PR4
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected

5.10.7 PR10 Unlock PR11-PR17
Read/Write Port = 3?5, Index = 29H

This register is READ/WRITE and cleared to 0 by reset. PR10 can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10 through PR17. Bits 7 and 3 enable register read operation for PR10 through PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for Manufacturing Test

5.10.8 PR11 EGA Switches
Read/Write Port = 3?5, Index = 2AH

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA configuration switches SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	WRITE 3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

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Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible analog) display.

Bit 2

Lock Clock Select.
This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer Screen Control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller and Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during a read operation.

Bit 0

Lock 8/9 Dots.
Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 Bit 0. Although 8 or 9 character timing is locked by setting PR11 Bit 0 to 1, the 3C5.01 Bit 0 appears unlocked to the system processor during reads.

5.10.9 PR12 Scratch Pad
Read/Write Port = 3?5, Index = 2BH

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

Bit 7

DAC Shut-off
Setting this bit to 0 enables the built-in DAC as normal. When this bit is set to 1, the built-in DAC is forced off.

The data in this register is unaffected by hardware reset and undefined at power-up.

5.10.10 PR13 Interlace H/2 Start
Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00). The equation is as follows:

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE: HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.10.11 PR14 Interlace H/2 End
Read/Write Port = 3?5, Index = 2DH

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ.
This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in Micro Channel operation.

Bit 6

Vertical Double Scan.
This bit should be set to 1 when emulating EGA on a PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. The relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is as follows:

$$N=2(n+1)$$

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced Mode.
Setting this bit to 1 selects interlaced mode. Interlaced mode can be used in video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 End Bits (4:0).
Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

5.10.12 PR15 Miscellaneous Control 1
Read/Write Port = 3?5, Index = 2EH

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8H.
This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Low VCLK.
Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ) >2

Bit 5

Latched VCLK1 and VCLK2.
This bit is used only if CNF(3) = 1 (which configures the VCLK1 and VCLK2 pins as outputs). Setting this bit to 1 causes outputs VCLK1 and VCLK2 to equal Bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H, respectively.

Bit 4

Select MCLK as Video Clock.
Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs cannot be selected when this bit is set.

Bit 3

Interlaced Compatibility.
This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.

Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing.
Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory (by 30-40%). Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8 Kbyte memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register, while the map selection is determined by the bits (4:3). A pair of adjacent 8 Kbyte character maps in planes 2 and 3 (adjacent in the sense that they have the same addressing), may be selected by Bit 3 of the attribute code.

The Character attribute Bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE: The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to choose between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0= BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable Border.
Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

5.10.13 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H Register.
Setting this bit to 1 causes EBROMN output to be forced high (inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.
Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64 Kbyte or 128 Kbyte locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512 Kbyte or 1024 Kbyte of video memory in which the CRT controller is limited to only 64 Kbyte or 128 Kbyte locations. Bit PR16(6) should be set to 1 to ensure that the VGA and EGA compatible operation of the address counter is limited to 64 Kbyte locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256 Kbyte
0	1	128 Kbyte
1	X	64 Kbyte

Bit (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively. The 2-bit result defines the starting location of the displayed video buffer at one of the four 64 Kbyte boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping.
Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC Write Strobe (3C6H - 3C9H).
Programming this bit to 1 causes output WPLTN to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C22, is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

5.10.14 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

This 2-bit register can be loaded only if PR10 (3?5.29) contains XXXXX101. It can be read only if PR10 contains 1XXX0XXX, and if both PR1B (7:5) is not 101 and PR30 (6:4) is not 011.

BIT	FUNCTION
(7:2)	Reserved
1	MDA Compatibility
0	Map Out 2 Kbyte From BIOS ROM

Bit (7:2)

Reserved.

Bit 1

MDA Compatibility Enable Bit.
Setting this bit to 1 enables MDA compatibility which will:

1. Disable I/O write to Hercules register 3BF.
2. Force Bit 7 of 3BA to 1.
3. Select underline decode of attribute XXXXX001 (if this bit is 0, underline decode is X000X001).

Reset sets this bit to 0.

Bit 0

Map Out 2 Kbyte of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C6000H – C67FFH. Power-on-reset sets this bit to 1. Clearing this bit to 0 enables access to all 32 Kbyte addresses of the BIOS ROM from CC000H – C7FFFH.

5.10.15 PR18 Flat Panel Status Register Read Write Port = 3?5, Index = 31

Bit 7

Reserved.

Bit 6

Enable Free Running Clock for Plasma or TFT Panel.
0 = Disable free running.
1 = Enable free running.

Bit 5

Enable 256 Kbyte Colors in STN Color LCD.
0 = Select 4 Kbyte colors.
1 = Select 256 Kbyte colors.

Bit 4

Enable Reverse Video in Flat Panel Mode.
This bit is used to reverse the polarity of video output data UD(3:0) and LD (3:0).

If PR18 (4)= 0, then only normal video displayed
If PR18 (4) = 1, then reverse video is displayed
in both text and graphics modes.

PR39 (3)	PR18 (4)	TEXT	GRAPHICS
X	0	Normal	Normal
0	1	Reverse	Reverse
1	1	Reverse	Normal

Bit 3

Enable Highest Contrast Intensity in Text Mode.
0 = Disable.
1 = Enable.

Bit 2

TFT Color LCD Select.
This bit is not readable.
0 = Disable TFT type color LCD panel interface.
1 = Enable TFT type color LCD panel interface.

Bit(1:0)

Panel Select Bit 1 and Bit 0.
These two bits are used to select different sets of parameters which will be loaded into the CRT controller. The parameters should be locked after loading.

PSB (1)	PSB(0)	PANEL TYPE
0	0	Dual Panel LCD Display
0	1	Plasma Display
1	0	EL Display
1	1	Single Panel LCD Display

5.10.16 PR19 Flat Panel Control Register, Read/Write Port = 3?5, Index 32

BIT	FUNCTION
7	Reserved
6	FP Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Autocentering/ Vertical Expansion Select
2	Enable Autocentering and Vertical Expansion
(1:0)	Adjustment of HSYNC Timing

Bit 7

Reserved

Bit 6

FP Timing Select.
This bit is used to select two different frame pulse (FP) timings for different LCD panels.
0 = Select ON time during first horizontal line.
1 = Select ON time during second horizontal line.

Bit 5

CRT Display Enable.
This bit enables CRT to be the display device.
0 = Disable CRT display.
1 = Enable CRT display.

NOTE: Upon hardware reset, PR19 (5) =1.

PR18(1)	PR18(0)	PR19(5)	PR19(4)	CRT Controller (Timing)
0	0	0	1	Based on LCD
0	0	1	0	Based on CRT
0	1	0	1	Based on Plasma
0	1	1	0	Based on CRT
1	0	0	1	Based on EL
1	0	1	0	Based on CRT

Bit 4
Flat Panel Display Enable.
This bit enables the flat panel as the display device.
0 = Disable Flat Panel display.
1 = Enable Flat Panel display.

Notes:
1. Upon hardware reset, PR19 (4) = 0.
2. When the flat panel display is not enabled, the outputs UD (3:0) and LD (3:0) are active and may be used as the pixel address to drive an external RAMDAC.
3. For simultaneous display of CRT and certain flat panel, set PR19 (5:4) = 11. In this case, the display is locked in 8-dot clock mode and the output -LCD/CRT = 0. The following flat panel may be displayed simultaneously with a CRT: plasma, TFT LCD, and color STN LCD.

Bit 3
Screen Auto Centering/Vertical Expansion Select.
0 = Auto-centering (default).
1 = Reserved for Vertical Expansion (set to 0).

Bit 2

Enable Auto-Centering and Vertical Expansion.
0 = Disable (default).
1 = Enable.

NOTE: This is used only for pulse wave modulation on the LCD panel.

Bit (1:0)

Adjustment of HSYNC timing.

PR19(7), PR19(1), and PR19(0) are used to select number of VCLK delays to adjust the HSYNC timing.

PR19(7)	PR19(1)	PR19(0)	Number of VCLK Delay
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.10.17 PR1A Flat Panel Control II Register, Read/Write Port 3?5, Index = 33

BIT	FUNCTION
(7:6)	Select IOCHRDY Release Timing in CPU Memory Read Cycle
(5:4)	Select IOCHRDY Release Timing in CPU Memory Write Cycle
3	Enable CGA Color to Gray Scale Adjustment
2	Shading Method Select
1	Select Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit(7:6)

Select IOCHRDY Release Timing in CPU Memory Read Cycle.

BIT 7	BIT 6	RELEASE TIMING
0	0	1 MCLK delay before CPU complete read cycle
0	1	2 MCLK delay before CPU complete read cycle
1	0	3 MCLK delay before CPU complete read cycle
1	1	4 MCLK delay before CPU complete read cycle

Bit (5:4)

Select IOCHRDY Release Timing in CPU Memory Write Cycle

BIT 5	BIT 4	RELEASE TIMING
0	0	1 MCLK delay before CPU completes write cycle
0	1	2 MCLK delay after CPU wins arbitration
1	0	3 MCLK delay after CPU wins arbitration
1	1	4 MCLK delay after CPU wins arbitration

Bit 3

Enable CGA Color to Gray Scale Adjustment.
This bit is used to add adjustment of weighting equation in CGA mode to get 16 different gray scale codes.
0 = Disable.
1 = Enable.

NOTE: For VGA, bit should be set to 0.

Bit 2

Shading Method Select.
0 = Frame rate modulation (default).
1= Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.
0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.
0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by PR1A(1).

5.10.18 PR1B Flat Panel Unlock Register, Read/Write Port 3?5, Index = 34

This register is used to protect PR18, PR19, PR1A, PR 30, PR36 through PR41, and PR44 from being read from or written into. In order to unprotect (read or write) the above registers, PR1B must be first loaded with 101XXXXX. The above registers remain unprotected until another value is written into PR1B.

PR1B is also used to lock all Shadow registers. To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

Upon hardware reset, PR1B is initialized to 101XX110, and the Shadow registers PR18, PR19, PR1A, PR30, PR36 through PR41, and PR44 are unprotected.

5.10.19 PR30 Mapping RAM Unlock Register, Read/Write Port = 3?5, Index = 35

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with X011XXXX; all mapping RAM registers remain unlocked until another value is written to the PR30 register.

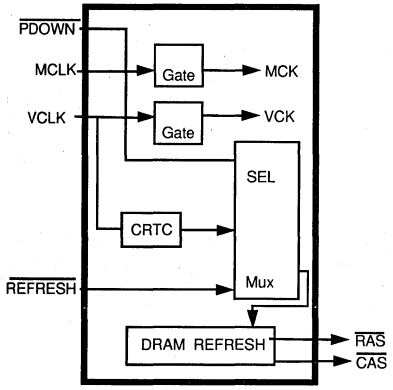
5.10.20 PR33 Mapping RAM Address Counter Register, Read/Write Port = 3?5, Index = 38

This register is used to select the RAM ADDRESS COUNTER register.

NOTE: Any I/O Read or Write to the I/O port 3?5.39H (Mapping RAM Data register) will increment the Mapping RAM Address Counter by one.

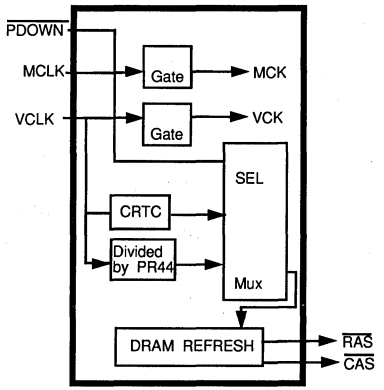
5.10.21 PR34 Mapping RAM Data Register, Read/Write Port = 3?5, Index = 39

This register is used to select the RAM data register for memory read or memory write.



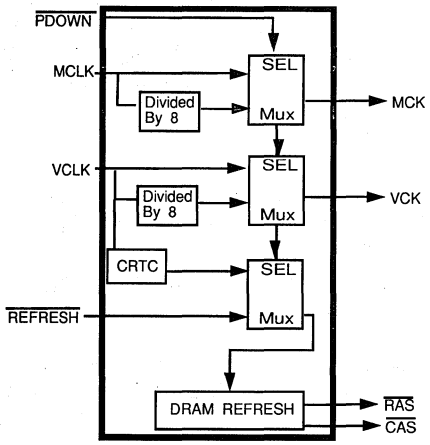
SYSTEM POWER DOWN MODE (SLEEP)

A. RAMDAC is off.
B. Clock inputs are turned off as they enter the chip.
C. CAS before RAS video memory refresh is generated from REFRESH input.
D. Neither video memory or I/O can be accessed in this mode.
E. RAMDAC and Mapping RAM contents are lost and must be reloaded to resume.



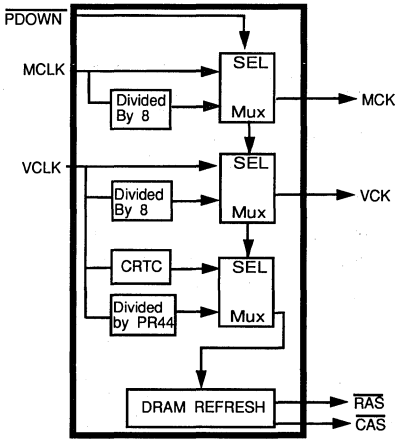
GENERAL POWER DOWN MODE (EXTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are not modified; their speed is reduced by system resources.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS.
D. Video memory and I/O are accessable.



DISPLAY IDLE MODE (SUSPEND/RESUME)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh is CAS before RAS and generated by REFRESH input.
D. I/O is accessable and memory is not accessable.



GENERAL POWER DOWN MODE (INTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS. PR44 can be RAS only.
D. Video memory and I/O are accessable.

FIGURE 5-1. SYSTEM POWER-DOWN MODE DISPLAY IDLE MODE

PR44(7)	PR35(7)	PR35(6)	MODE
0	1	X	System Power-Down Mode: MCLK and VCLK are turned off. Video memory refresh is generated from PDREF. Neither memory nor I/O can be accessed. RAMDAC and Mapping RAM must be reloaded.
0	0	X	Display Idle Mode: MCLK and VCLK are divided by 8 before being distributed across the chip. Video memory refresh is generated from PDREF. Only I/O can be accessed.
1	X	0	General Power-Down (External Clock Used): MCLK and VCLK inputs are used to drive the chip . The assumption is made that MCLK and VCLK have been reduced by some other part of the system. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.
1	X	1	General Power-Down (Internal Clock Used): MCLK and VCLK inputs are divided by 8 before being distributed across the chip. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.

5.10.22 PR35 Mapping RAM and Power-Down Control Register, Read/Write Port = 3?5, Index = 3A

BIT	FUNCTION
7[1]	Select System Power-Down Mode/ Display Idle Mode
6[1]	Select Internal Divided By 8 Clock to Control General Power-Down Mode
5[1]	Host Release Control
4[1]	Reserved; set to 1.
3[1]	Select 64 Gray Scale Levels
2[1]	Enable $\overline{CAS}$ before $\overline{RAS}$ Memory Refresh Cycle
1	Enable Weighting Equation
0	Reserved; set to 1.

[1] Readable only when PR30=X011XXXX.

Bit 7

Select System Power-Down Mode/display Idle Mode. Refer to Figure 5-1. This bit is not readable.

0 = Display idle mode (default).

1 = System power-down mode; MCLK and VCLK turned off.

Bit 6

Select Internal Divided by 8 Clock to Control General Power-Down Mode. This bit is active only when PR44(7) is set at 1. This bit is not readable.

0 = Disable internal clock.

1 = Enable internal clock; clock is divided by 8.

Bit 5

Host Release Control.

This bit is designed to allow another VGA controller in the I/O bus. When PR35(5) is set to 1 and PDOWN input is set to 0, the WD90C22 will not respond to any CPU memory or I/O accesses. All

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output buffers of the system interface are turned off (tristate).

There are four power-down modes. The following conditions are true in each powerdown mode.
1. Video memory is maintained.
2. RAMDAC outputs are turned off.
3. Panel outputs are turned off.

Bit 4

Reserved. This bit is set at 1.

Bit 3

Select 64 Gray Scale Levels
0 = Select disabled; select 32 gray scale levels.
1= Select enabled; select 64 gray scale levels.

Bit 2

Enable CAS before RAS Memory Refresh Cycle.
0 = $\overline{RAS}$ only refresh cycle (default).
1 = $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Bit 1

Enable Weighting Equation.

This bit is used to turn the IBM VGA weighting equation on and off in either color mode or monochrome mode.
0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved. This bit is set at 1.

5.10.23 PR36 Panel Height Select Register, Read/Write Port = 3?5, Index = 3B

This register is loaded with the height, less 1, of a single panel. This information is used to calculate auto-centering, vertical expansion, and related values. In a 640 by 480 dual panel display, this register should be loaded with "EF". (480/2)-1 = 239_{10} = EFH. In a 640 by 400 dual panel display, the equation is: (400/2)-1 = 199_{10} = C7H.

5.10.24 PR37 Flat Panel Blinking Control, Read/Write Port = 3?5, Index = 3C

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

Bit	2	1	0	CURSOR BLINKING RATE SELECT
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
Bit	**5**	**4**	**3**	**CHARACTER BLINKING RATE SELECT**
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
Bit	**6**			**PLASMA SHIFT CLOCK SELECT**
	0			Select falling edge of the clock to latch data
	1			Select rising edge of the clock to latch data
Bit	**7**			**LCD LP SIGNAL SELECT**
	0			LP will be disabled during vertical blanking period
	1			LP will be generated continuously during vertical blanking period (SCLK will be turned off)

5.10.25 PR39 Color LCD Control Register, Read/Write Port = 3?5, Index = 3E

This register is used to support color LCD panel.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Panel
4	Reserved
3	Enable Reverse Video
2	Reserved
1	Reserved
0	Reserved

Bit 7

Enable Border LP Control.
This bit is used to generate a special LP pulse to latch border information (black or white).
0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select.
0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel.
This bit is used to select monochrome LCD or color LCD.
0 = Disable color LCD panel select.
1 = Enable color LCD panel select.

Bit 4

Reserved.

Bit 3

Enable Reverse Video.
See PR18 (4)

Bit(2:0)

Reserved.

5.10.26 PR41 Vertical Expansion Initial Value Register, Read/Write Port = 3?5, Index = 37

Reserved.

5.10.27 PR42 – PR43 Unlock Register, Write Only Port = 3C5, Index = 06

This register locks the PR VGA Status register. In order to read/write to the PR VGA status register (PR43), PR42 must be loaded first with X1X01XXX; PR43 will remain unlocked until another value is written to PR42.

5.10.28 PR43 PR VGA Status Register, Read/Write Port = 3C5, Index = 07

This register is used to indicate the current status of the PR VGA chip and to enhance programming compatibility.

BIT	FUNCTION
(7:4)	Read/Write Scratch Pad Bits
3	Color/Monochrome Emulation Status
2	Mode Type
1	EGA Compatibility Set
0	Display Type

Bit(7:4)

Read/Write Sctatch Pad Bits.
These four bits are available for temporary data storage.

Bit 3

Color/Monochrome Emulation Status.
Read only, Bit 0, of Miscellaneous Output register (3C2).
0 = Monochrome emulation is enabled.
1 = Color graphic emulation is enabled.

Bit 2

Mode Type.
Read only, Bit 6 of PR2.
0 = Either VGA or EGA mode is enabled.
1 = Non-VGA and non-EGA modes are enabled.

Bit 1

EGA Compatibility Set.
Read only of PR4, Bit 1.
0 = EGA compatibility is disabled.
1 = EGA compatibility and the ability to read PR0 – PR5 registers are enabled.

Bit 0

Display Type.
Read only of PR5, Bit 3.
0 = Analog (VGA-compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

5.10.29 PR44 Powerdown Memory Refresh Control Register, Read/Write Port = 3?5, Index = 3F

This register controls two power saving features when in the general powerdown modes. Bit 7 is used with PR35(7:6) to determine which powerdown mode is to be used. With some powerdown modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. PR44(6:0) are loaded with a value that modifies the video memory refresh period during power down.

BIT	FUNCTION
7	General Powerdown Mode Enable
(6:0)	Memory Refresh Cycle Period

Bit 7

General Powerdown Mode Enable Bit.
This bit enables general powerdown mode.
0 = Disables general powerdown.
1 = Enables general powerdown.

Bit(6:0)

Memory Refresh Cycle Period.
These bits are loaded with the value Z, which is used to determine the refresh period when general power down mode is used. Refresh period = VCLK x 8 x (Z+5). For example, assume:

1. Two memory refresh cycles are selected during horizontal blanking period in Flat Panel display mode.
2. Each horizontal line has 96 character clocks.
3. MCLK = 36 MHz, VCLK = 25 MHz.
4. PR44 = 8EH.

When in powerdown mode, POWRDN = 0, MCLK = VCLK = 5 MHz.

1. Z = 14.
2. Refresh Cycle = 200 ns x 8 x (14 + 5).
3. Maximum Refresh Period = 200 ns x 8 x (14 + 5 - 7) = 19.2 µs.
4. Refresh Active Time = MCLK x 9 x 2 (cycle) = 200 ns x 9 x 2 = 3.6µs.

5.11 INTERNAL I/O PORTS

5.11.1 AT Mode, Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused.

Bit 4

Setup.
Puts WD90C22 into setup mode where only I/O port 102H is accessible.

Bit 3

I/O and Memory Accesses.
0 = Disable I/O and memory accesses.
1 = Enable I/O and memory accesses.

Bit(2:0)

Unused Internally.
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4 Kbyte pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4 Kbyte pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

5.11.2 Setup Mode Video Enable, (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C22 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C22 after power on in MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the $\overline{\text{CDSETUP}}$ (ALE) signal pin is active low, the WD90C22 is in setup mode and port 102H can be accessed.

5.12 VIDEO RAMDAC PORTS

The WD90C22 incorporates a complete Micro Channel-compatible RAMDAC, as well as the ability to support an optional external RAMDAC. Selection of the internal or external RAMDAC option is based on the state of the VREF pin when reset is de-asserted.

Data from the internal RAMDAC is always written to the data bus, even when the internal RAMDAC is configured for use with external RAMDAC. RPLT may be used as a gate to send data from an external RAMDAC to the data bus.

There are four operation modes for the built-in video RAMDAC:
– Palette Read Mode
– Palette Write Mode
– PEL Mask Mode
– Palette Status Mode

Which mode is activated depends on two conditions: 1) which I/O port is being addressed, and 2) whether a host write or a host read is being executed.

In other words, the registers, albeit at the same I/O port, may have different meanings, depending on the mode in which the color palette is being accessed. Specifically, the register at 03C7 may contain either PEL address or palette status, depending on whether the access is a read or write operation.

When in the Palette Read Mode, the PEL address is to be written into the 03C7 port. The data can then be read out through the SD bus by three successive read operations from the 03C9 port.

When in the Palette Write Mode, the PEL address is to be written into the 03C8 port. The data can then be written into the palette through the SD bus by three successive write operations into the 03C9 port.

During either Palette Read or Palette Write mode, the 03C7 port can be read to obtain the contents of the Palette Status Register. Please see below for more detail on the palette register.

5.12.1 PEL Mask Register, Read/Write Port = 03C6

The 8-bit PEL Mask Register, along with the eight bits of color information from the combination of the attribute controller and the color select register, are ANDed together and become the index into the color lookup table of the RAMDAC during display refresh. The contents of this register have no effect on host access to the lookup table. The host may access this register at any time without disturbing the contents of the lookup table. The contents of this register are undefined after reset.

5.12.2 Palette Status Register/ Palette-Read-Mode PEL Address Register Read/Write Port = 03C7

Palette Status Register (as a Read Port):
The Palette Status Register can be accessed by reading the 03C7 port (read only). Bits 0 and 1 of this register indicate whether the last active operation to the DAC was in Palette Read Mode or in Palette Write Mode. These bits are both 0 if a host write into the port 03C7 is more recent than a host write into the port 03C8. They are both 1 if a host write into the port 03C8 is more recent than a host write into the port 03C7.

Palette-Read-Mode PEL Address Register (as a Write Port):

DAC ADDRESS	TYPE	REGISTER NAME
3C6H	Read/Write	PEL Mask
3C7H	Read/Write	When written: PEL Address (Read Mode); When read: Palette Status
3C8H	Read/Write	PEL Address (Write Mode)
3C9H	Read/Write	PEL Data Port

The host reads data from the color palette RAM by first writing the index of the first location to be read into this PEL Address Register (write only). When this is done, the RAMDAC loads the RAM data specified by the index into an 18-bit holding register. The contents of this 18-bit register are read out via three reads from the PEL Data Port. The data read during these reads consists of six bits of color information packaged into the six least significant bits of the port. The two most significant bits of data during these reads are set to zero. The color information is delivered in the sequence: read, green, blue. After the three read cycles have completed, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be read by sets of three reads from the PEL Data Port, 03C9.

5.12.3 Pallette-Write-Mode PEL Address Register Read/Write Port = 03C8

The host writes data from the color palette RAM by first writing the index of the first location to be written into this register. Completed PEL data to be written is then loaded into an 18-bit holding register via three writes to the PEL Data Port. This is accomplished by concatenating the six least significant bits of the data from the three writes. The color information is extracted in the sequence: red, green, blue. When this is done, the RAMDAC loads the contents of the holding register into the palette RAM location indexed by the contents of the PEL Address (write mode) register. After the data has been transferred to the RAM, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be written by sets of three writes to the PEL Data Port.

5.12.4 PEL Data Read/Write Port = 03C9

This port is used to transfer 6-bit PEL data values to and from the palette RAM. The 18-bit palette locations are transferred in the order: red, green, blue.

5.13 WD90C22 CONFIGURATION BITS, CNF

The configuration register, CNF, is not a physical register, but a convenient way to reference the state of the video memory data lines which are latched at reset. These data lines–for the sake of convenience, collectively called the configuration register CNF– provide setup parameters to various areas on the chip.

When the WD90C22 is reset, it latches the state of the video memory data lines. This data provides setup parameters to various areas of the chip. In order to easily reference these individual bits, we collectively refer to them as the configuration register, (CNF). Only fifteen data lines are used in the WD90C22; and data line MD10 is not used.

CNF (11)

Color/Mono LCD Panel Select.
This bit is latched internally at power-on-reset from corresponding memory data bus pin MD(15), provided with either pull-up or pull-down external resistors. This bit is read from PR11(7), I/O port 3?5.2A bit 7. This bit is affected by writing to 3?5.2A. Pulling up MD(15) causes CNF(11) to be latched high.

0 = Monochrome LCD panels.
1 = Color LCD panels.

CNF (10:9)

Panel Select Bits.
These bits are latched internally at power-on-reset from corresponding memory data bus pins MD(9:8), provided with either pull up or pull down external resistors. They are read only at I/O port 3?5.31 as bits 1:0 and are unaffected by writing to 3?5.31. Pulling up MD(9:8) data bus pin causes CNF (10:9) to be latched high.

CNF(10)	CNF(9)	DISPLAY TYPE
0	0	Dual Panel LCD Display
0	1	Plasma Display
1	0	EL Display
1	1	Single Panel LCD Display

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CNF (8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). CNF(8) is unaffected by writing to PR5 (3CF.0F).

0 = Analog (VGA - compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

General Purpose Status Bits.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). They are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

Video Clock Source Control.

This bit cannot be written to or read as I/O port. Pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C22 pins VCLK1 and VCLK2 as inputs or outputs.

0= For inputs.
1= For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of the dot clock is by an internal multiplexor. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. VCLK1 and VCLK2 outputs are equal to Bits 2 and 3 of the Miscellaneous output register at 3C2H, respectively, when PR15 Bit 5 is set to 1.

CNF (2)

Bus Architecture Select.
This bit cannot be written to or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.
0 = Micro Channel architecture.
1 = AT BUS architecture.

Selecting CNF(2) will change the pinout definition between AT bus and Micro Channel bus. Refer to the pinout description.

PC AT BUS	I/O	MC	I/O
$\overline{\text{MEMCS16}}$	OUT	$\overline{\text{CDDS16}}$	OUT
IOCHRDY	OUT	CDCHRDY	OUT
$\overline{\text{EBROM}}$	OUT	$\overline{\text{CDSFDBK}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MEMR}}$	IN	M/IO	IN
$\overline{\text{MEMW}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
ALE	IN	$\overline{\text{CDSETUP}}$	IN

5.14 MAPPING RAM – 32 by 6 STATIC RAM

The 32 by 6 SRAM is designed for dithering pattern selecting. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM can be read or written to by the CPU.

During normal operation, the outputs from the weighting equation (6 bits) will be connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (6 bits) are connected to the dithering logic.

To Write:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock the mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load WRITE starting address register with 00.
OUT 3?4, 39H	Program the index register.
OUT 3?5, 0AH	Write 0A directly to the mapping RAM at location 00.
OUT 3?5, 0BH	Write 0B directly to the mapping RAM at location 01.

To Read:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load READ starting address register with 00.
OUT 3?4, 39H	Program the index register.
IN 3?5	Read directly from the mapping RAM at 00.
IN 3?5	Read directly from the mapping RAM at 01.

NOTE: There is a minimum timing requirement between two consecutive RAM reads or writes (4 x VCLK period). If the system is running faster than 16 MHz, a "NOP" instruction should be inserted between consecutive reads and/or writes.

5.15 SHADOW TIMING REGISTERS

The shadow timing registers control the timing in the CRTC. When the regular timing registers are written to, the shadow timing registers, if unlocked (in CRT mode, they are unlocked), receive the same data. Locking the shadow timing registers is controlled by PR1B.

Timing data is always read from the regular timing registers. The WD90C22 never reads from the shadow timing registers.

In Flat Panel mode, the shadow timing registers are loaded once and then locked by PR1B. Once they are locked, data written to the timing registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

There are eleven shadow timing registers. All are indexed in port 03?5.

NAME	INDEX	SAMPLE VALUE*
Horizontal Total	00H	5FH
Start Horizontal Blanking	02H	50H
End Horizontal Blanking	03H	82H
Start Horizontal Retrace	04H	54H
End Horizontal Retrace	05H	80H
Vertical Total	06H	F2H
Overflow **	07H	00H
Vertical Retrace Start	10H	F0H
Vertical Retrace End	11H	02H
Start Vertical Blank	15H	F0H
End Vertical Blank	16H	F2H

* The sample values are for a monochrome dual panel LCD with 640 by 480 pixels.

** Only bits 7, 5, 3, 2 and 0 are locked by PR1B.

6.0 RAMDAC

6.1 GENERAL DESCRIPTION

The on-board RAMDAC was designed specifically for Personal System/2 compatible color graphics in a laptop computer environment. It integrates the functions of a color lookup table, digital-to-analog converters, power saving features and PS/2 compatible monitor detection logic.

The 256 by 18 color lookup table has triple 6 bit video D/A converters. A pixel mask register and composite blank generation on the three channels are provided. The RAMDAC also supports the use of an external voltage reference.

Without external buffering, the RAMDAC will generate RS-343A compatible video signals into a doubly-terminated 75 ohm load, and RS-170 compatible video signals into a singly-terminated 75 ohm load. Integral and differential linearity errors are a maximum of +/- 1/2 LSB.

6.2 FUNCTIONAL DESCRIPTION

The RAMDAC architecture consists of five major modules:

- Address Register
- Pixel Mask Register
- Color Palette RAM
- Powerdown Control
- Digital-to-Analog Converter (with automatic poweron reset)

Color Palette RAM: There are three 256 by 6 color palette RAMs for the red, green and blue polygun. They provide color information to the triple 6-bit D/A converters. The RAMDAC's color palette RAM memory cell is a custom, power saving cell.

Power-Down Control: The RAMDAC supports an intelligent power-down control sequence. When $\overline{\text{PWRDN}}$ input is low, the entire RAMDAC will enter the "IDLE" state; both the DAC and the color palette RAM will be turned off regardless of the CRT/-LCD signal. When $\overline{\text{PWRDN}}$ input is high in CRT mode, the RAMDAC will operate with the DAC and the color palette RAM always enabled. In LCD mode, when $\overline{\text{PWRDN}}$ input is high, the DAC is turned off. The color palette RAM will be enabled only when the MPU is accessing the RAMDAC because of the intelligent "MPU operation auto-detecting" circuit implemented.

Automatic Power-on Reset: The RAMDAC supports an "automatic power-on-reset" circuit that enables its DAC portion to initialize very quickly after power-on. And, since the DAC is totally turned off in LCD mode, a triggered signal will also initialize the "reset operation" of the DAC during the mode change from LCD mode to CRT mode.

See section Appendix E for a description of the RAMDAC registers.

6.3 FEATURES

- Personal System/2 compatible
- Bt471/478 and Bt476 compatible
- Power management features
- On-Chip monitor detection logic
- Video signal output into 37.5 or 50 ohms
- 256 by 18 color palette RAM
- Triple 6-Bit D/A Converters
- Pixel mask register
- Up to 8 bits input per pixel
- RS-343/RS-170 compatible outputs
- 1.25 micron CMOS technology

7.0 POWER-DOWN MODES

7.1 SYSTEM POWER-DOWN MODE

7.1.1 Description of System Power-Down Mode (Sleep Mode)

System Power-down mode is used when the entire system goes to sleep and provides the most power savings. Current requirements for this mode are approximately 4mA. This mode also requires the most system overhead and therefore in addition to being the most miserly in terms of power consumption, it is also the slowest. When the VGA subsystem has been placed in System Power-down mode, the only activity required of the VGA subsystem is saving the contents of the video display buffer which is accomplished by maintaining refresh of the DRAM. In this mode the system CPU has no access to the display memory nor any access to the I/O of the WD90C22 VGA controller.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Turning off the internal MCLK and VCLK signals.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to WD90C22 I/O registers.
6. Denying the CPU access to video memory.

In System Power-down mode only the content of the video display buffer is saved which implies that the rest of the dynamic data contained in the VGA subsystem is corrupted. This includes the color content of the RAMDAC palette and the content of the mapping RAM is lost when in this mode.

7.1.2 Entering System Power-Down Mode

To select System Power-Down mode, load bit PR35(7) with "1" (default value is "0"). The WD90C22 will enter a System Power-Down mode cycle when the motherboard power manager drives the "PDOWN" input of the 90C20 low. After "PDOWN" is driven low, the CPU can not access the WD90C22.

The WD90C22's internal memory and video clocks will automatically be turned off (to save power) after the following time interval: 4 horizontal scan lines PLUS 3 "REFRESH" cycles.

The WD90C22 uses the "REFRESH" input to generate "CAS before RAS" memory refresh cycles which refresh display memory. The internal RAMDAC is also turned off, and display memory refresh is the only WD90C22 activity during this power-down mode. The VCC pins of the WD90C22 must remain powered.

Primary input MCLK may be clocked at the same frequency as VCLK, or may be left at a static "1" or "0". Primary input VCLK must NOT be turned off but may be reduced to as low as 8 KHz. When the VCLK and MCLK frequencies are reduced, they should not be reduced until the following time interval has passed: the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles.

There are several ways to slow down the clocks of the WD90C61. The most effective way is to use the "FCLKIN" input frequency. This is done by driving the "FCLKSEL" input low. "FCLKIN" could be connected to a slow frequency clock which is available on the motherboard.

During the System Power-Down mode, the "OE10", "OE32", "WE0", "WE1", "WE2", "WE3" and MA(8:0) outputs are all driven high. The memory data bus, MD(15:0), will be in an unknown state. Note that all primary inputs must be driven to either VCC or VSS, as required by the system design. No inputs may be left floating.

7.1.3 Exiting System Power-Down Mode

Before returning to normal display mode, the power manager must first return the WD90C22 clock inputs back to their original frequencies (if they were slowed down during the power-down mode). Care must be taken to ensure that the clock inputs to the WD90C22 are stable BEFORE driving the "PDOWN" input high.

To return to normal mode, the power manager drives "PDOWN" high; the WD90C22 returns to normal operation mode after the following time interval; the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles. The screen automatically displays the information in video memory.

The power-up service routine must reload the RAMDAC RAM data and the 32 by 6 Dithering Mapping RAM data after the system returns to normal operation mode.

7.2 DISPLAY IDLE MODE

7.2.1 Description of Display Idle Mode

The Display Idle Mode is used when the user can allow the display to be turned off, for example, when a keyboard key has not been pressed for five minutes. The DAC and LCD panel interfaces are turned off in this mode. Internal clocks are divided by eight from the primary inputs, thus internal logic runs eight times slower. The CPU can access I/O registers of the WD90C22, but it can not access display memory.

Power saving is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing internal WD90C22 clocks by eight.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to video memory.

7.2.2 Entering Display Idle Mode

Register bits PR35(7) and PR44(7) must be set to "0" (default values) to use this mode. The WD90C22 will enter a Display Idle Mode cycle when the motherboard power manager drives the "PDOWN" input of the WD90C22 low.

The WD90C22 will then divide the internal VCLK and MCLK signals by eight. For example, if the input VCLK is 32 MHz and the input MCLK is 44.9 MHz, the internal VCLK will be 4 MHz and the internal MCLK will be 5.61 MHz. Power consumption in this mode is approximately 1/10 of normal consumption. The internal RAMDAC turns off and screen refresh cycles are stopped. The WD90C22 uses the "REFRESH" input to generate "CAS before RAS" cycles to refresh display memory. The CPU will be the only user to access the display memory. There is no arbitration between CPU cycles and CRT cycles, or between CPU cycles and refresh cycles.

While in the Display Idle Mode, the video system continues to run, allowing the user to read/write WD90C22 I/O registers, however, the CPU CAN NOT read/write display memory.

7.2.3 Exiting Display Idle Mode

To return to normal operation mode, the power manager simply drives "PDOWN" high. The screen automatically displays the original picture. External clocks must maintain original frequencies for the Display Idle Mode.

7.3 GENERAL POWER-DOWN MODES

7.3.1 Description of General Power-Down Modes

There are two General Power-Down modes. These modes are used when: 1)the user doesn't need to view the display, 2)he needs to keep the system running, but 3)he can afford to reduce the frequencies of both MCLK and VCLK. Video system performance is reduced in exchange for significant power savings. Another advantage is that activating the WD90C22 PDOWN input is the only software interaction required.

One of the General Power-Down modes is designed to interface with an intelligent clock generator like the WD90C61, which slows down the clocks to the WD90C22 to a selectable frequency during the power-down interval. This is called the General Power-Down mode with External Clock Control.

The other is designed to be independent of the external clock control; the external clock maintains the same frequency during power-down, however internal clock circuitry in the WD90C22 divides the input clock by eight. This is called General Power-Down mode with Internal Clock Control.

Both General Power-Down modes allows the CPU to access BOTH I/O registers and display memory.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing the MCLK and VCLK inputs by a system chosen factor (external) or by eight (internal).

7.3.2 Entering General Power-Down Mode with External Clock Control

To select General Power-Down mode with External Clock Control, load bit PR44(7) with "1" and bit PR35(6) with "0". PR44(6:0) should be pre-loaded with its correct value, based on the power-down clock frequency.

The WD90C22 will enter a General Power-Down mode with External Clock Control cycle when the motherboard power manager drives the "PDOWN" input of the WD90C22 low. At this time the PR44 register will replace the CRTC registers to control memory refresh timing.

7.3.3 Exiting General Power-Down Mode with External Clock Control

Before returning to normal display mode, the power manager must first return the WD90C22 clock inputs back to their original frequencies. Care must be taken to ensure that the clock inputs to the WD90C22 are stable BEFORE driving the "PDOWN" input high.

To return to normal mode, the power manager drives "PDOWN" high; the WD90C22 then returns to normal operation mode and displays the screen that is stored in video memory.

7.3.4 Entering General Power-Down Mode with Internal Clock Control

To enter the General Power-Down mode with the internal clock control, PR44(7) must be set to a "1" and PR35(6) must be set to a "1". PR44(6:0) should be pre-loaded with its correct value based on the VCLK frequency and the PR1A(1:0) value. The PR1A(1:0) is used to select different memory refresh cycles per each horizontal line.

After the input "PDOWN" is driven low by the system, the WD90C22 will enter General Power-Down mode automatically. Register PR44 will replace the CRTC registers to control memory refresh timing.

7.3.5 Exiting General Power-Down Mode with Internal Clock Control

To return to normal mode, the power manager drives "PDOWN" high; the WD90C22 then returns to normal operation mode and returns the internal MCLK and VCLK signals to their normal frequencies. The information stored in video memory is displayed on the screen.

7.3.6 Example Calculations of PR44(6:0) Values

Described below are examples of how to calculate correct values of PR44(6:0) for both General Powerdown modes. Calculation of PR44(6:0) value is based upon the following equation:

7.3.7 Disabling the WD90C22 to Accommodate an Alternate VGA Controller

PR35 Bit 5 allows the WD90C22 to accommodate an alternate VGA controller. When the WD90C22 detects that "PDOWN" is low and PR35(5) is high, the WD90C22 isolates itself from the system I/O bus regardless of the programmed power-down mode. In this case, the CPU CAN NOT access the WD90C22. All outputs and I/Os of the host interface are tri-stated. This feature allows another VGA or graphic controller on the system I/O bus in case the system designer wished to switch display environments.

To return to normal operation mode, the CPU must drive "PDOWN" high.

PR44(6:0) = ((Refresh Rate*PR1A(1:0))/((1/(CLK/8))*Character)) - 5

Where: Refresh Rate = Period defined for Refresh of the DRAMs

CLK = External Clock input for General Power-Down mode with External Clock
VCLK input for General Power-Down mode with Internal Clock.

Example for General Power-Down mode with External Clock Control:

Example A == > How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 0
PR1A(1:0) = 11 (2 memory refresh cycles/horizontal line)
Normal Operation: VCLK = 32 MHz, MCLK = 44.9 MHz
Power-Down Mode: VCLK = 5 MHz, MCLK = 8 MHz (external control)

CALCULATE ==>
15 us x 2 = 30 us (2 refreshes/line)
1/5 MHz x 8 = 200 ns x 8 = 1.6 us (1 character clock in power-down mode)
(30 us / 1.6 us) - 5 = 14 (PR44(6:0) = OE hex)

Example B ==> How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 1 (internal divided by 8 control)
PR1A(1:0) = 01 (1 memory refresh cycle/horizontal line)
Normal Operation: VCLK = 28 MHz, MCLK = 42 MHz
Powerdown Mode: VCLK = 3.5 MHz, MCLK = 5.25 MHz (internal control)

CALCULATE ==>
15 us x 1 = 15 us (1 refresh/line)
285.7 ns x 8 = 2.286 us (1 character clock in power-down mode)
(15 us/ 2.286 us) - 5 = 2 (PR44(6:0) = 02 hex)

The following are descriptions of the output states of all output pins during the four power-down modes. These states are given for both "AT" and "Micro Channel" modes of operation. This information is provided for reference to the system designer.

PC-AT MODE					
OUTPUT STATE					
Pin No.	**Pin**	**System Powerdown Mode**	**Display Idle Mode**	**General Mode w/Ext. Clock**	**General Mode w/Int. Clock**
	SD[15:0]	Z	N	N	N
15	IOCHRDY	Z	N	N	N
12	IRQ	Z	N	N	N
14	$\overline{\text{MEMCS16}}$	Z	N	N	N
13	$\overline{\text{EBROM}}$	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	$\overline{\text{RAS32}}$	N	N	N	N
56	$\overline{\text{RAS10}}$	N	N	N	N
59	$\overline{\text{CAS32}}$	N	N	N	N
58	$\overline{\text{CASA10}}$	N	N	N	N
65	$\overline{\text{OE32}}$	H	N	N	N
64	$\overline{\text{OE10}}$	H	N	N	N
	$\overline{\text{WE}}$[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	$\overline{\text{LCD}}$/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	$\overline{\text{RPLT}}$	H	N	N	N
93	$\overline{\text{WPLT}}$	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tri-state.

NOTES: 1. For on-chip pullups and pulldowns, please see Section 4.0 "Signal Definitions".

MICRO CHANNEL MODE					
OUTPUT STATE					
Pin No.	Pin	System Powerdown Mode	Display Idle Mode	General Mode w/Ext. Clock	General Mode w/Int. Clock
	SD[15:0]	Z	N	N	N
15	IOCHRDY	H	N	N	N
12	IRQ	H	N	N	N
14	$\overline{\text{MEMCS16}}$	H	N	N	N
13	$\overline{\text{EBROM}}$	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	$\overline{\text{RAS32}}$	N	N	N	N
56	$\overline{\text{RAS10}}$	N	N	N	N
59	$\overline{\text{CAS32}}$	N	N	N	N
58	$\overline{\text{CASA10}}$	N	N	N	N
65	$\overline{\text{OE32}}$	H	N	N	N
64	$\overline{\text{OE10}}$	H	N	N	N
	$\overline{\text{WE}}$[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	$\overline{\text{LCD}}$/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	$\overline{\text{RPLT}}$	H	N	N	N
93	$\overline{\text{WPLT}}$	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tristate.

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8.0 LCD PANEL CONTROL

This section describes external power on/off control logic for an LCD panel interface.

8.1 DESCRIPTION OF SIGNALS FOR FIGURE 8-1

Described below are the signals related to the power-on/off control logic in Figure 8-1.

POWER-ON
(General motherboard signal, input to control logic)

Active high signal: indicates that the LCD +5 volt power supply (+VDD_LCD) and the backlight power supply (+VBL) are stable.

$\overline{\text{PDOWN}}$, +PDOWN
(General motherboard signal, input to control logic)

Active low and active high signals, respectively; indicate that the system has entered the POWER-DOWN mode.

RSET
(General motherboard signal, input to control logic)

Active high signal; is generated during power-on or system reset.

$\overline{\text{LCD}}$
(WD90C22 output)

WD90C22 active low output; indicates that the LCD panel is selected as main display.

$\overline{\text{LCDEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable the LCD drivers and DC power.

$\overline{\text{CFLEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable backlight power.

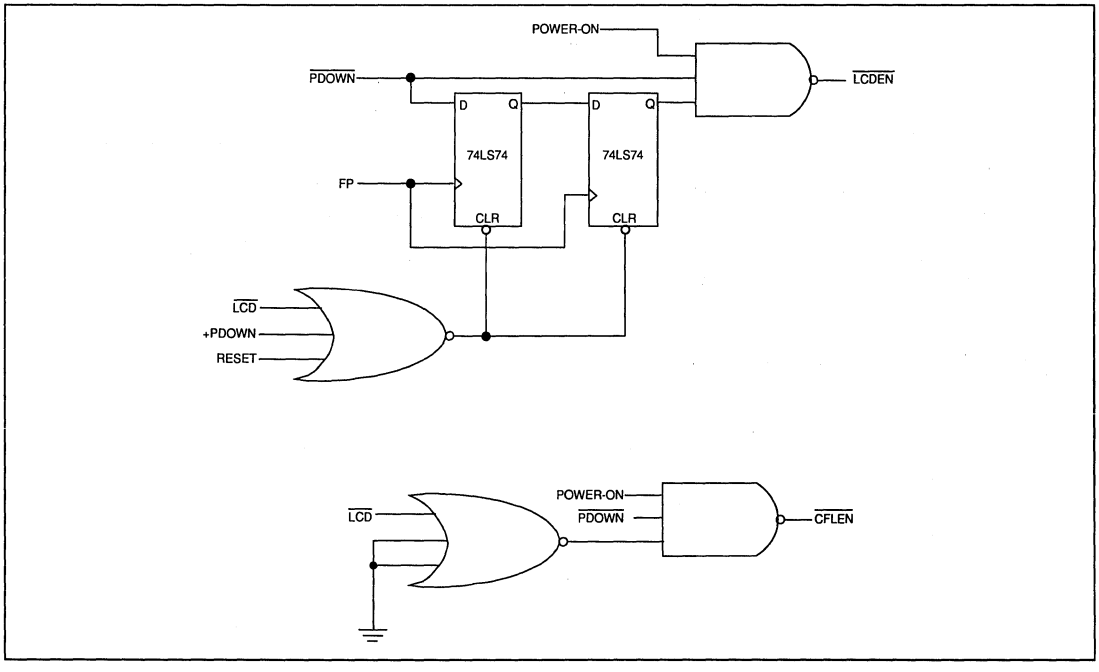

FIGURE 8-1. LCD PANEL CONTROL

9.0 LCD POWER-ON/OFF OPERATIONS DESCRIPTION

9.1 SYSTEM POWER-ON

When main power is turned on, RESET guarantees that "LCDEN" remains high during the power-on interval. This protects the LCD panel from damage. After "RESET" goes inactive, the "LCD" output from the WD90C22 will be a 1, which forces LCDEN high, keeping the LCD panel disabled.

Once the LCD panel has been programmed to be active, two "FP" strobes (one to two vertical frames) after "LCD" goes low, "LCDEN" is driven low, enabling LCD power. "CFLEN" (backlight power) is driven low immediately after "LCD" goes low.

9.2 SYSTEM POWER-OFF

When main power is turned off "POWERON" goes low, forcing both "-LCDEN" and "CFLEN" high, which immediately disables both LCD panel power and backlight power.

9.3 SWITCHING FROM CRT MODE TO LCD MODE

The system must:

1. Reset the CRT mode bit PR19(5) to "0".
2. Read and save the CRTC registers.
3. Load the shadow registers with default values from the table.
4. Lock the shadow registers.
5. Write back the CRTC registers.
6. Enable the LCD mode by setting PR19(4)=1 (which sets "LCD"=0).

Two "FP" strobes (one to two vertical frames) from "LCD" going low, "LCDEN" is driven low, enabling LCD power. "CFLEN" is driven low immediately after "LCD" goes low.

9.4 SWITCHING FROM LCD MODE TO CRT MODE

The system must:

1. Reset the LCD mode bit PR19(4) to "0", thus setting the WD90C22 output "LCD" to a "1" (since "LP" and "FP" are still toggling).
2. Read and save the CRTC registers.
3. Unlock the shadow registers.
4. Write back the CRTC registers.
5. Set the CRT mode bit PR19(5) to a "1".

9.5 ENTERING POWER-DOWN MODE

The system drives "PDOWN" low and "+PDOWN"high to enter a power-down mode. Both "LCDEN" and "CFLEN" are driven high immediately (before "LP" and "FP" stop toggling).

9.6 LEAVING POWER-DOWN MODE

When in LCD Mode: The system drives "PDOWN" high and "+PDOWN" low to leave a power-down mode (to return to normal operation mode). "LCDEN" remains high for two "FP" strobes (one to two vertical frame periods). This guarantees the "LP" and "FP" will be toggling before LCD panel power is turned on.

When in CRT Mode: Because "LCD" is always a "1" when entering and leaving a power-down mode, "LCDEN" and "CFLEN" will also remain high for the entire period, thus leaving the LCD panel power turned off.

A.0 APPLICATIONS APPENDIX

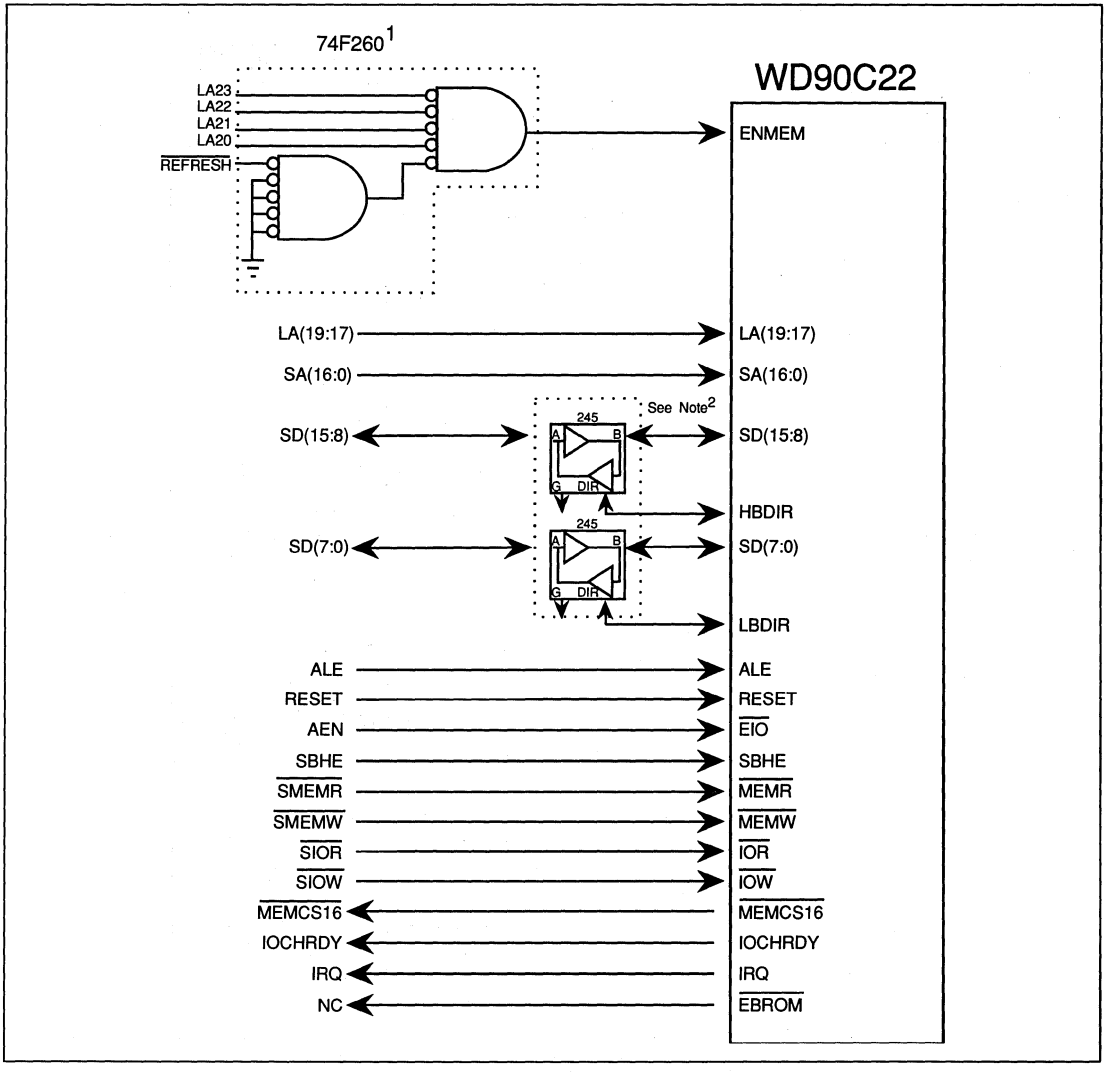

FIGURE A-1. PC/AT INTERFACE

NOTES:

[1] The 74F260 is used to determine if the current address is in the first megabyte. This function is already provided by most core logic chip sets.

[2] The 74245 buffers are only needed if system drive requirements exceed chip capabilities.

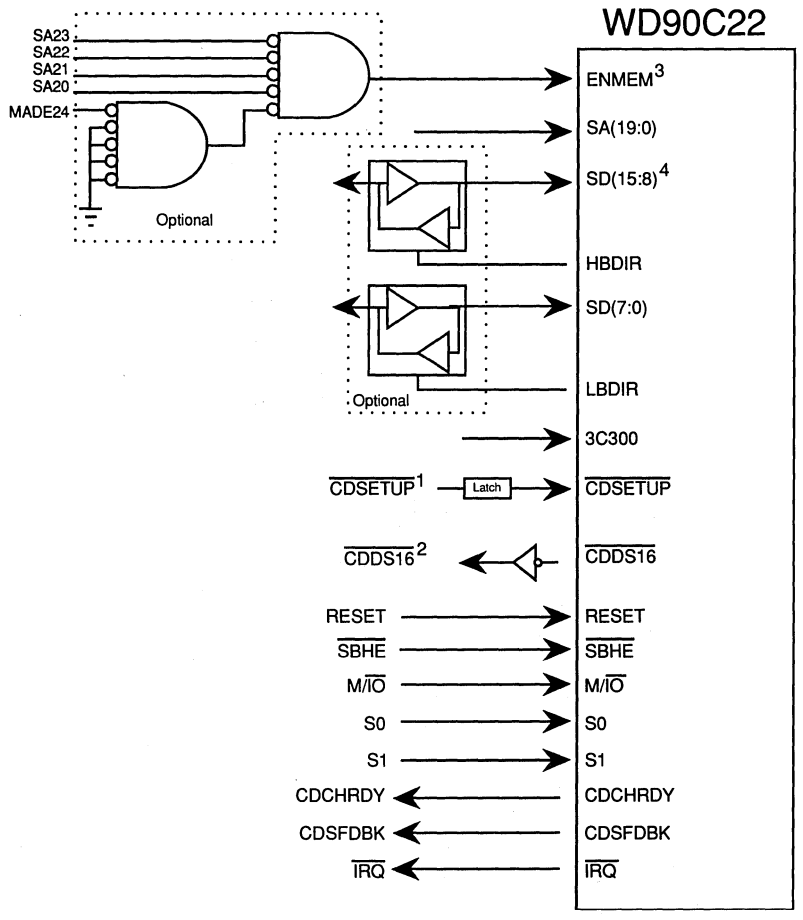

FIGURE A-2. MICRO CHANNEL INTERFACE

NOTES:

1 CDSETUP must be latched if core logic does not already latch it.
2 CDDS16 requires an inverter (changed in future revisions).
3 ENMEN must be qualified for the first megabyte of memory space. This is provided in many core logic designs; the two And Gates are not required.
4 The bidirectional buffers are only needed if the system design requires more current than the WD90C22 can deliver.

15

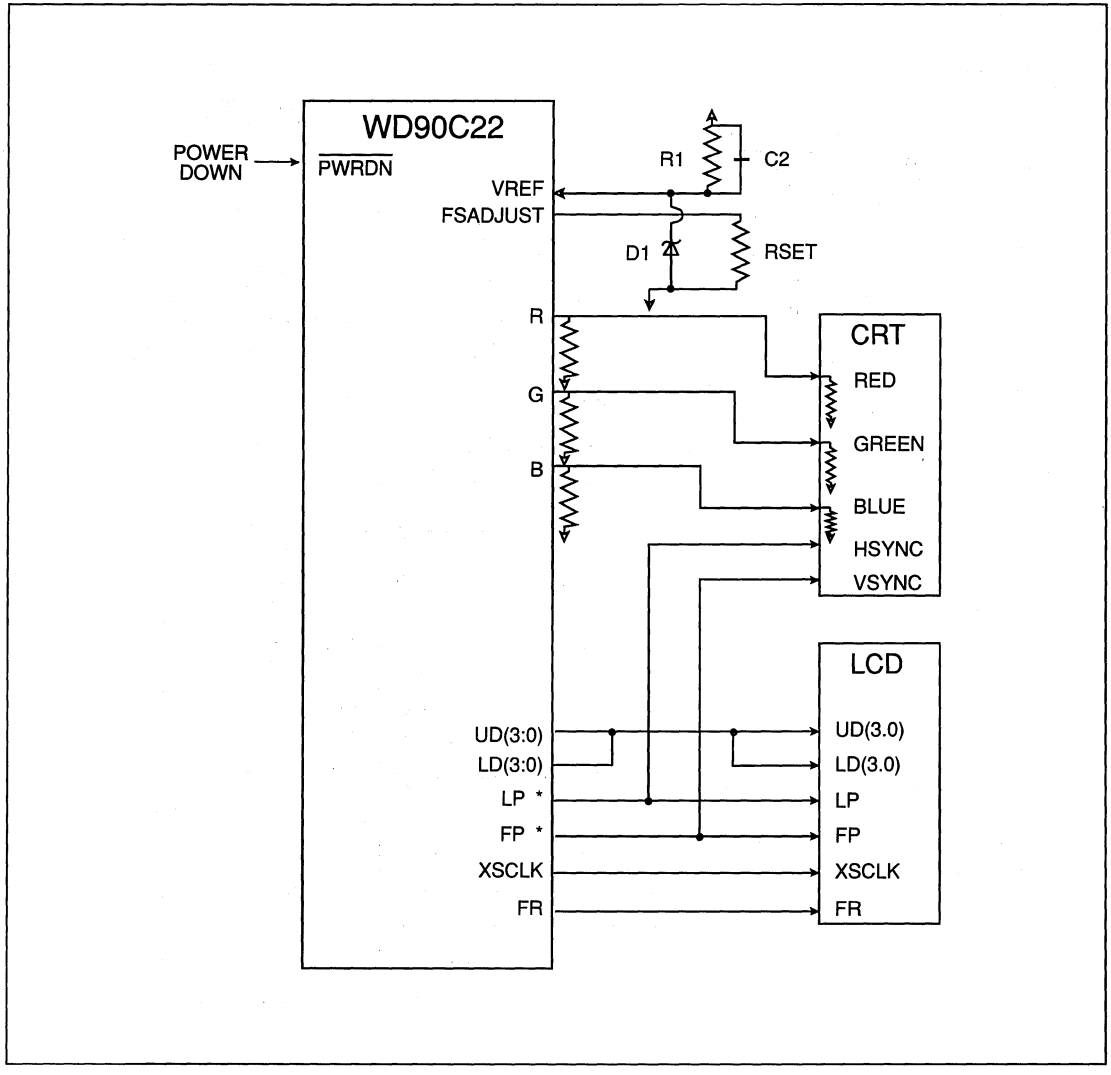

FIGURE A-3. WD90C22 DISPLAY INTERFACE

FULL-SCALE-VOLTAGE CALCULATION EXAMPLE:

$$V_{FULL\ SCALE} = [I_{FULL\ SCALE}] \quad [RLD]$$

$$= \left[\frac{code \times 0.04 \times VREF}{RSET}\right] \quad [RLD]$$

$$= \left[\frac{63 \times 0.04 \times 1.235}{221}\right] \quad [50] = 0.704 \text{ volts}$$

* These signals may require buffering if monitor sinks more than the 6mA drive of the WD90C20.

B.0 EGA MODE APPENDIX

This appendix provides a general description of EGA mode. Details of the actual software implementation are not covered.

For those registers that are the same in both VGA and EGA mode, refer to the VGA description. Only the differences are described in this section. Bits not used should be set to 0 unless otherwise noted.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pullup or pulldown resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
2. Unlock all the PR registers.
3. Program PR2(6) to 0 for EGA mode.
4. Set PR4 Bit 1 to logic 1 for EGA compatibility.
5. Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power-on-reset.)
6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 Bit 4.
7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the steps listed below:
   - Initialize all the registers
   - Lock CRT controller registers
   - Force Clock Control rate of the CRT controller
8. Set EGA emulation mode by programming:
   - PR11(3)=1; Set EGA emulation on PS/2 type display
   - PR14(6)=1; Vertical double scan
   - PR11(2)=1; Lock clock select
   - PR11(0)=1; Lock 8/9 dot timing
   - PR14(7)=1; Enable IRQ (optional)
9. Lock the PR registers PRO-PR5 and PR10-PR17.
10. Read protect PR registers.
11. When EGA is required on a TTL monitor, the suggested steps are:
    - Initialize all the registers
    - Set EGA TTL mode by programming:
      PR11(3)=0;EGA TTL
      PR14(7)=1;Enable IRQ
      PR15(6)=1;Set Low Clock
      PR14(7)=1;Enable IRQ
    - Lock PR registers PRO-PR5 and PR10-PR17
    - Read protect PR registers

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3C4
CRT Controller Data Reg Except the Following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
High Pen High (Index=10)	R	3?5
Light Pen Low (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

TABLE B-1. EGA REGISTERS SUMMARY

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All register addresses are in hex.
3. ? = B in monochrome modes or D in color modes.
4. * = Identical responses from I/O ports 3C0 and 3C1.

B.1 GENERAL REGISTERS

The General Registers and the bit definitions that differ from VGA mode are covered below.

B.1.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Disables internal video drivers.
0 = Activate video drivers.
1 = Disable video drivers.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

B.1.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not Used.

Bit 4

EGA: Information on the four configuration switches stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not Used = 1

B.1.3 Input Status Register 1 (Read Port 3?A)

Bit (7)

EGA: Not Used.

Bit 6

EGA: Not Used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: The following Light Pen Switch definition is applicable:
0 = Light Pen Switch is Closed.
1 = Light Pen Switch is Open.

Bit 1

EGA: The following Light Pen Trigger definition is applicable:
0 = Light Pen Trigger is Reset.
1 = Light Pen Trigger is Set.

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

B.1.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not Used.

B.2 SEQUENCER REGISTERS (PORT 3C5)

B.2.1 Clocking Mode Register, (Index = 01)

Bits (7:4)

EGA: Not Used.

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to Zero.

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

B.2.2 Character Map Select Register, (Index 03)

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Character Map Select A:

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

Bits (1:0)

EGA: Character Map Select B:

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

NOTE: 1. Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

B.2.3 Memory Mode Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha Mode Bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha mode and enables non-Alpha mode.

B.3 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. A "?" implies that a register is mapped into either 3B5 or 3D5 for Monochrome or Color display modes, respectively.

B.3.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Register Address index where the data is to be written.

B.3.2 Horizontal Total Register, (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

B.3.3 End Horizontal Blanking Register, (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: These bits define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

B.3.4 End Horizontal Retrace Register, (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

B.3.5 Vertical Total Register, (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

B.3.6 CRT Controller Overflow Register, (Index = 07)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bit (4:0) definitions in the VGA section.

B.3.7 Preset Row Scan Register, (Index = 08)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register (4:0) definition in the VGA section.

B.3.8 Maximum Scan Line Register, (Index = 09)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

B.3.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

B.3.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not Used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

B.3.11 Vertical Retrace Start Register, (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

B.3.12 Vertical Retrace End Register, (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not Used.

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if Bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

B.3.13 Underline Location Register, (Index = 14)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

B.3.14 End Vertical Blanking Register, (Index = 16)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

B.3.15 Mode Control Register, (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.4 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

B.4.1 Read Map Select Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

B.4.2 Mode Register, (Index = 05)

Bit (7:6)

EGA: Not Used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

B.5 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

B.5.1 Mode Control Register, (Index = 10)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.5.2 Overscan Color Register, (Index = 11)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the 6 bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

B.5.3 Color Plane Enable Register, (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer according to the table below.

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2 (Red)	VID 0 (Blue)
0	1	VID 5 (SRed)	VID 4 (SGreen)
1	0	VID 3 (SBlue)	VID 1 (Green)
1	1	VID 5 (SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

B.5.4 Horizontal PEL Panning Register, (Index = 13)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: These 4 bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, a 9-dots/character image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B.6 MONITOR DETECTION

The DAC output currents I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. The output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

The output signal MDETECT is readable at port 3C2H bit 4. It is important to read during active video ouput, not during retrace or any other blanking period.

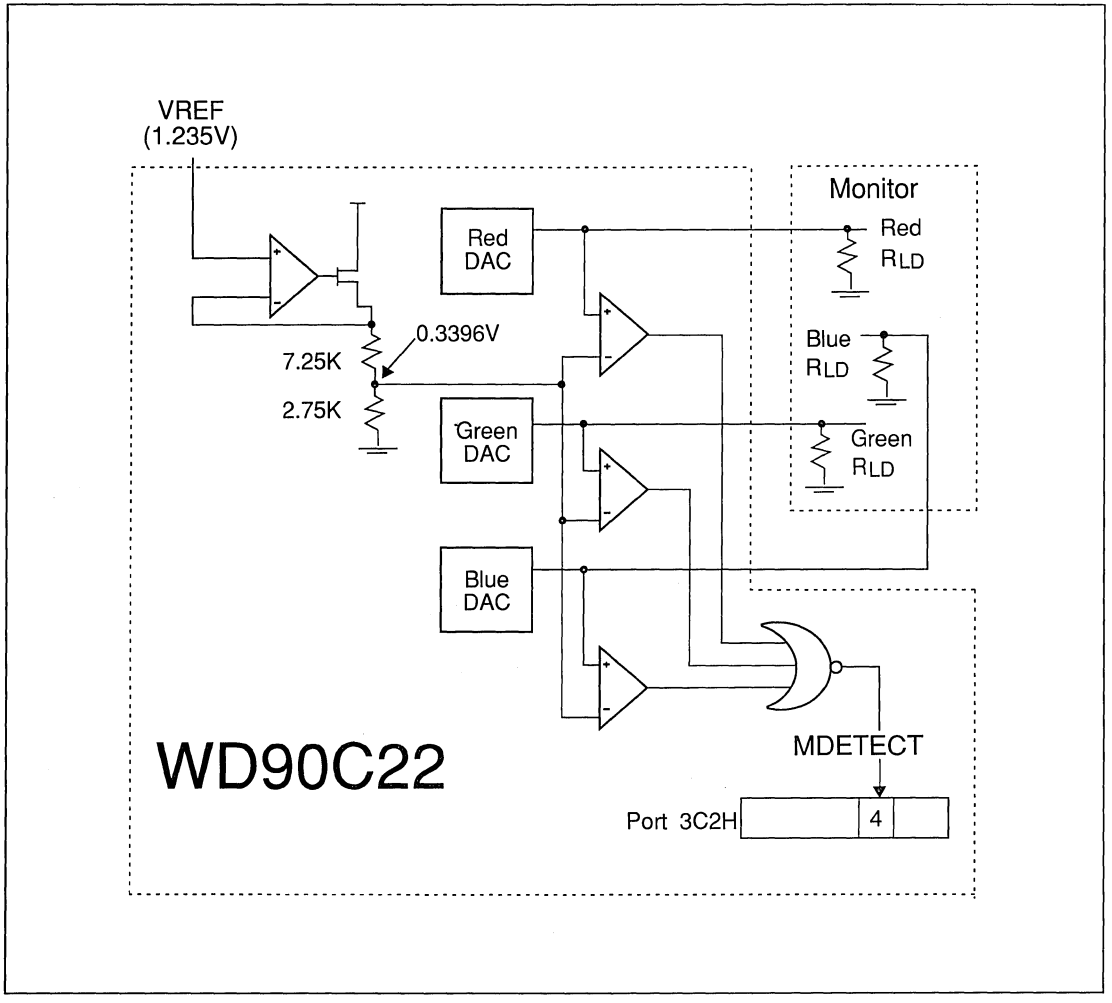

FIGURE B-1. MONITOR DETECTION FOR INTERNAL RAMDAC

C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	I/O Write – AT Mode
C-2	I/O Read – AT Mode
C-3	Memory Write – AT Mode
C-4	Memory Read – AT Mode
C-5	I/O Write – Micro Channel Mode
C-6	I/O Read – Micro Channel Mode
C-7	Memory Write – Micro Channel Mode
C-8	Memory Read – Micro Channel Mode
C-9	CPU Write with Non-Page Mode
C-10	CPU Read Non-Page Mode, CRT Read
C-11	DRAM Page Mode Read Timing
C-12	WD90C22 LCD Timing (t = VCLK)
C-13	RAMDAC Timing
C-14	CRT Clock Timing
C-15	Reset Timing
C-16	RAS OnlyDRAM Refresh Timing
C-17	CAS Before RAS DRAM Refresh Timing
C-18	CAS Before RAS Refresh (Power-Down Mode)
C-19	STN Color LCD Interface Timing
C-20	IOCHRDY Release Timing in Memory Read Cycle
C-21	IOCHRDY Release Timing in Memory Write Cycle

TABLE C-1. TIMING DIAGRAMS

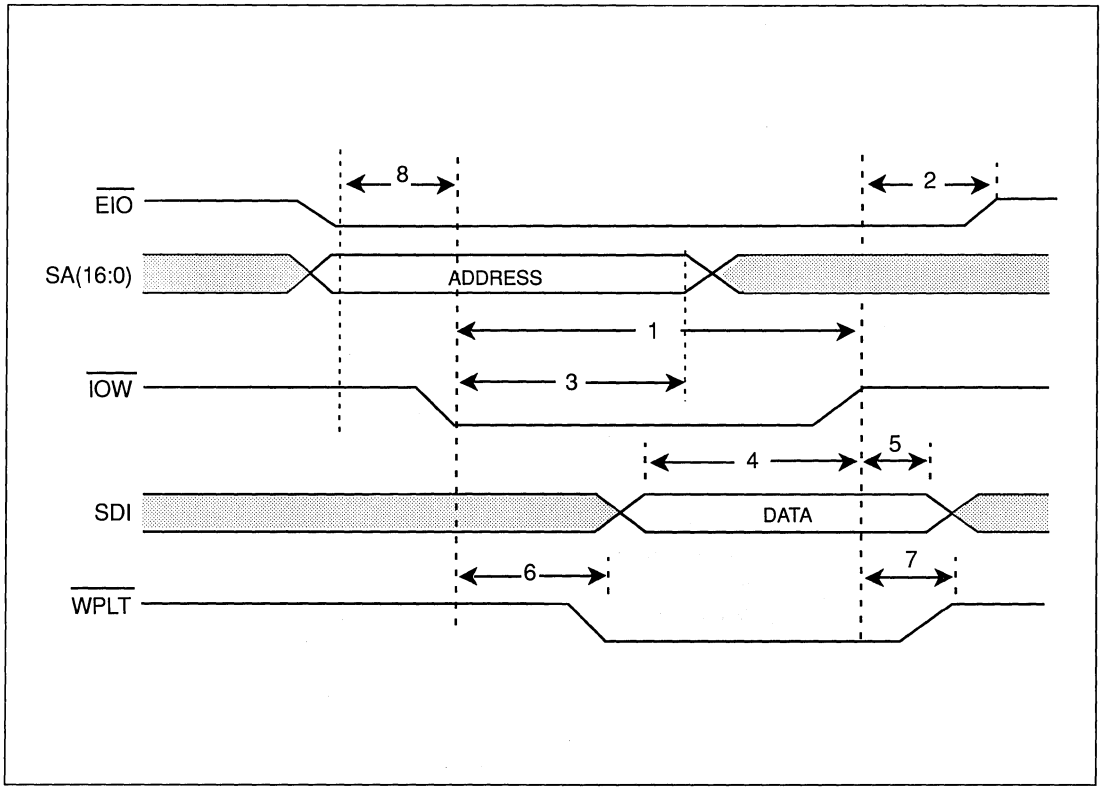

FIGURE C-1. I/O WRITE-AT MODE

NO.	I/O WRITE AT MODE			MIN.	MAX.
1	$\overline{IOW}$	active pulse width		2.5t	
2	$\overline{EIO}$	hold from	$\overline{IOW}$ inactive (high)	10	
3	SA(16:0),	hold from	$\overline{IOW}$ active	25	
4	Write Data SDI	setup to	$\overline{IOW}$ inactive	30	
5	Write Data SDI	hold from	$\overline{IOW}$ inactive	10	
6	$\overline{WPLT}$	active from	$\overline{IOW}$ active (C_L = 15pF)		50
7	$\overline{WPLT}$	inactive from	$\overline{IOW}$ inactive (C_L = 15pF)		50
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOW}$ active	15	

t = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consective I/O transfers.

15

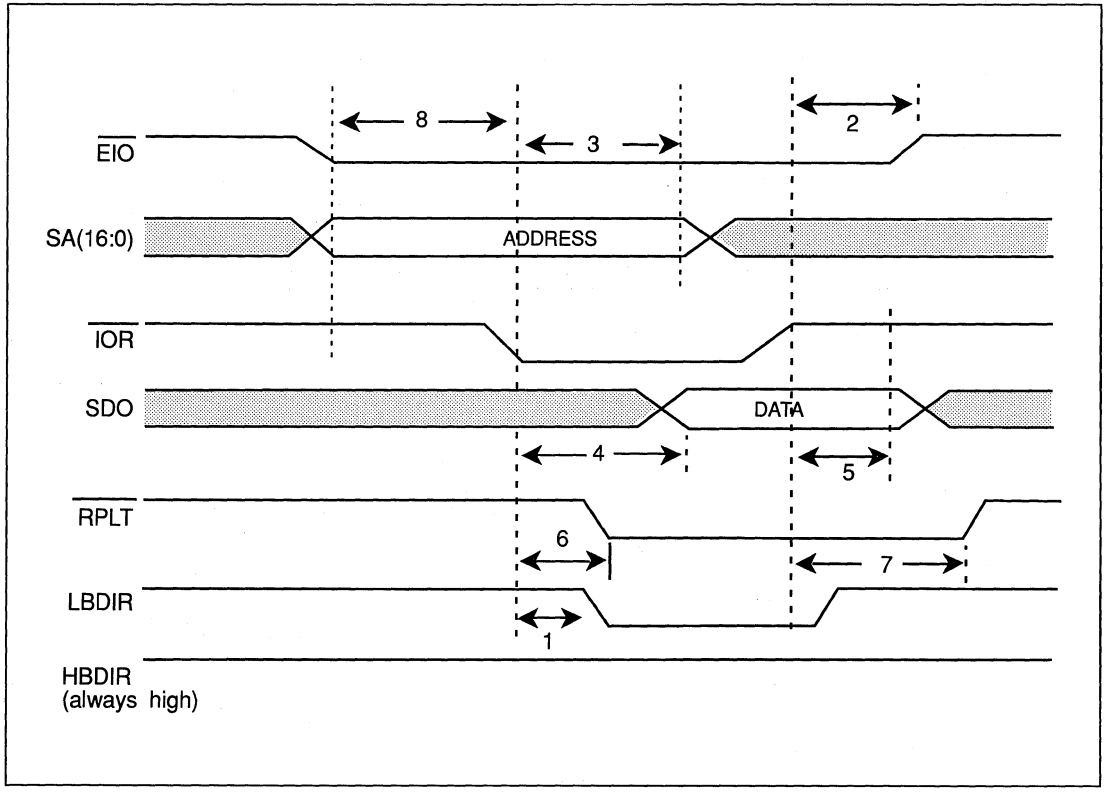

FIGURE C-2. I/O READ-AT MODE

NO.	I/O READ AT MODE			MIN.	MAX.
1	LBDIR	delay from	$\overline{IOR}$		48
2	$\overline{EIO}$	hold from	$\overline{IOR}$ inactive (high)	10	
3	SA(16:0),	hold from	$\overline{IOR}$ active	25	
4	Read Data SDO	valid from	$\overline{IOR}$ active	.5T	1.5T+65
5	Read Data SDO	hold from	$\overline{IOR}$ inactive	10	40
6	$\overline{RPLT}$	active from	$\overline{IOR}$ active (C_L = 15pF)		50
7	$\overline{RPLT}$	inactive from	$\overline{IOR}$ inactive (C_L = 15pF)		50
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOR}$ active	15	

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consective I/O transfers.

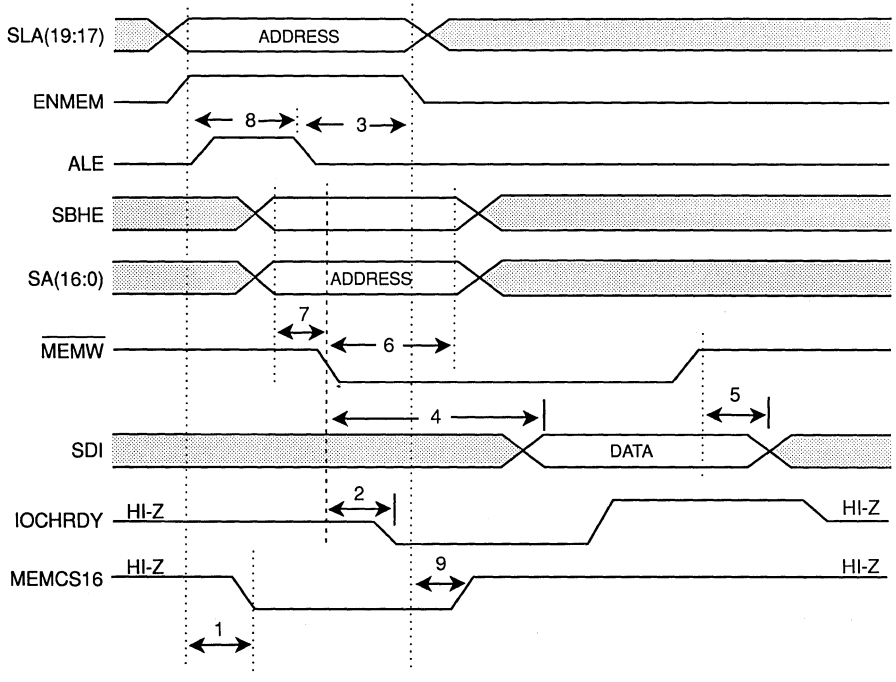

FIGURE C-3. MEMORY WRITE - AT MODE

NO.	MEMORY WRITE AT MODE			MIN.	MAX.
1	$\overline{\text{MEMCS16}}$	valid from	SLA (19:17) ENMEM valid		21
2	IOCHRDY	inactive from	$\overline{\text{MEMW}}$ active	24	
3	SLA(19:17), ENMEM	hold from	ALE inactive	5	
4	Data SDI	valid from	$\overline{\text{MEMW}}$ active	30	
5	Data SDI	hold from	$\overline{\text{MEMW}}$ inactive	5	
6	SA(16:0), SBHE	hold from	$\overline{\text{MEMW}}$ active	20	
7	SA(16:0), SBHE	setup to	$\overline{\text{MEMW}}$ active	25	
8	SLA(19:17), ENMEM	setup to	ALE inactive	25	
9	$\overline{\text{MEMCS16}}$	invalid from	SLA (19:17) ENMEM invalid		30

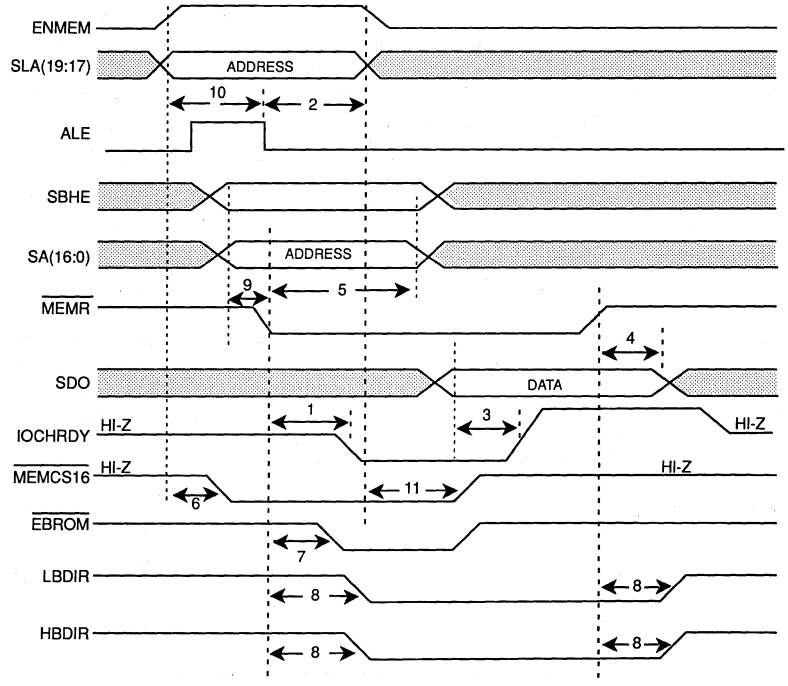

FIGURE C-4. MEMORY READ - AT MODE

NO.	MEMORY READ – AT MODE			MIN.	MAX.
1	IOCHRDY	inactive from	$\overline{\text{MEMR}}$ active		26
2	SLA(19:17), ENMEM	hold from	ALE inactive	30	
3	Data SDO	valid setup to	IOCHRDY active	2t	
4	Data SDO	hold from	$\overline{\text{MEMR}}$	20	50
5	SA(16:0), SBHE	hold from	$\overline{\text{MEMR}}$ active	20	
6	$\overline{\text{MEMCS16}}$	valid from	SLA(19:17) ENMEM valid		24
7	$\overline{\text{MEMR}}$	active to	$\overline{\text{EBROM}}$ active		30
8	LBDIR HBDIR	delay from	$\overline{\text{MEMR}}$		48
9	SA(16:0), SBHE	setup to	$\overline{\text{MEMR}}$ active	25	
10	SLA(19:17), ENMEM	setup to	ALE inactive	25	
11	$\overline{\text{MEMCS16}}$	invalid from	SLA(19:17) ENMEM invalid		30

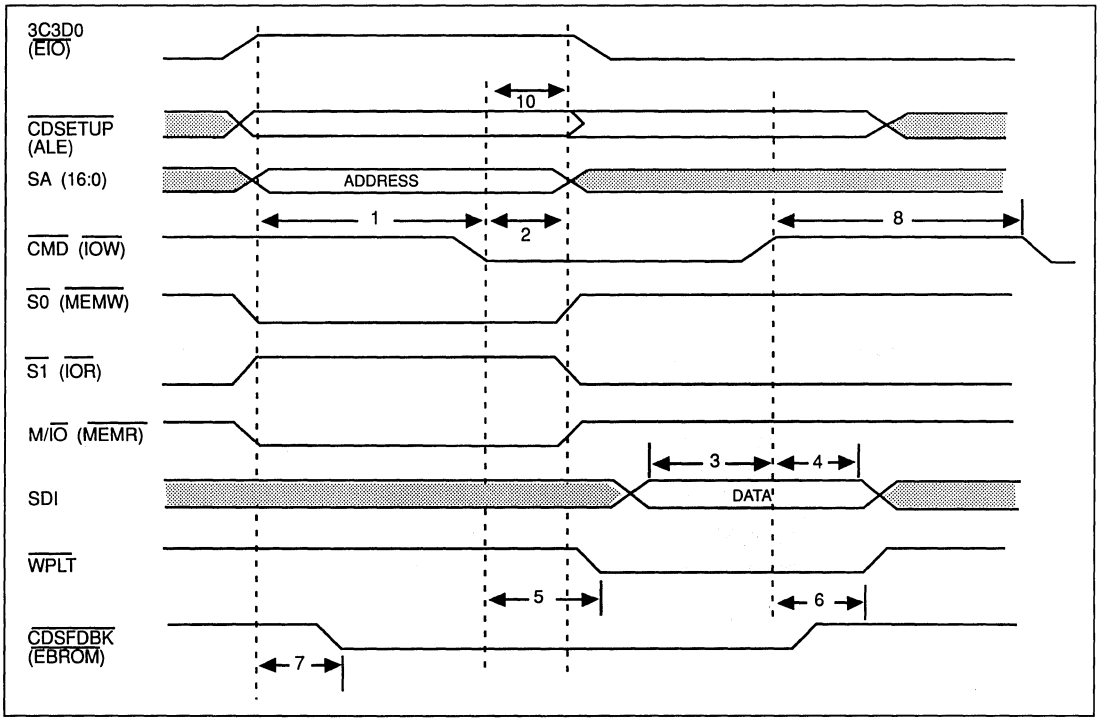

FIGURE C-5. I/O WRITE-MICRO CHANNEL MODE

NO.	I/O WRITE – MC MODE			MIN.	MAX
1	SA(16:0), $\overline{S0}$, $\overline{S1}$ 3C3D0, $\overline{CDSETUP}$, M/$\overline{IO}$	setup to	$\overline{CMD}$ active (low)	15	
2	SA(16:0), $\overline{S0}$, $\overline{S1}$ 3C3D0, M/$\overline{IO}$	hold from	$\overline{CMD}$ active	30	
3	Write data SDI	setup to	$\overline{CMD}$ inactive	30	
4	Write data SDI	hold from	$\overline{CMD}$ inactive	10	
5*	$\overline{WPLT}$	active from	$\overline{CMD}$ active		50
6*	$\overline{WPLT}$	inactive from	$\overline{CMD}$ inactive		50
7	$\overline{CDSFDBK}$	active from	Address Valid		58
8	$\overline{CMD}$	inactive pulse width		2t	
9	$\overline{CMD}$	active pulse width		2.5t	
10	$\overline{CDSETUP}$	hold from	$\overline{CMD}$ active (low)	30	

* C_L = 15pF
t = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consective I/O transfers.

15

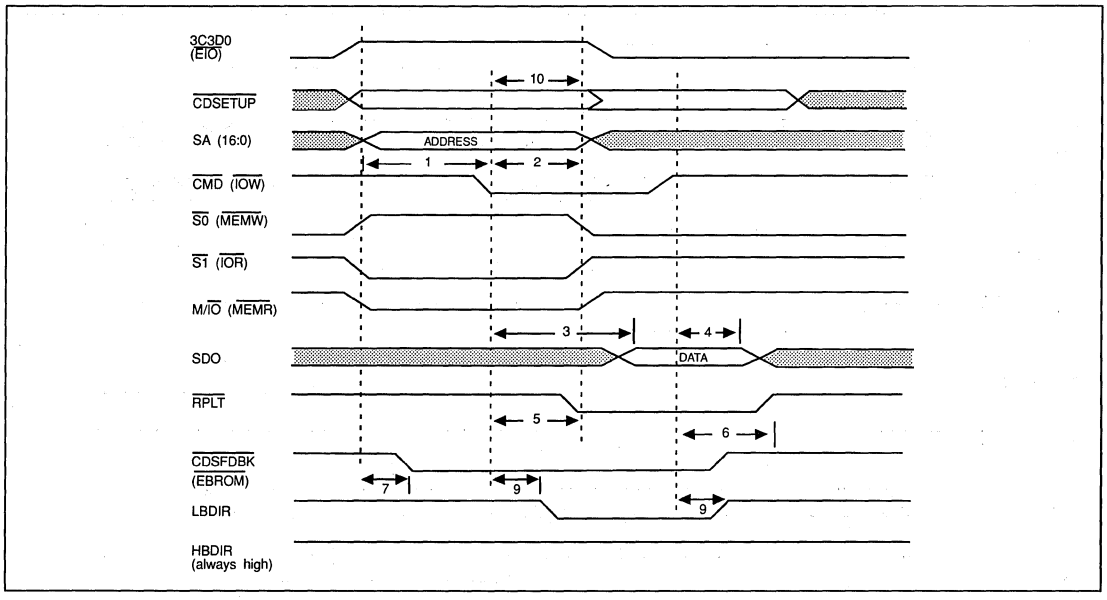

FIGURE C-6. I/O READ - MICRO CHANNEL MODE

NO.	I/O READ MC MODE			MIN.	MAX.
1	SA(16:0), S0, S1, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	15	
2	SA(16:0), S0, S1, 3C3D0, M/IO	hold from	CMD active	30	
3	Read data SDO	valid from	CMD active	.5T	1.5T+65
4	Read data SDO	hold from	CMD inactive	10	40
5	RPLT	active from	CMD active (C_L = 15pF)		50
6	RPLT	inactive from	CMD inactive (C_L = 15pF)		50
7	CDSFDBK	active from	Address Valid		58
8a 8b	CMD CMD	active pulse width active pulse width mapping RAM only		130 4t+30	
9	LBDIR	delay from	CMD		48
10	CDSETUP	hold from	CMD active (low)	30	48

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consective I/O transfers.

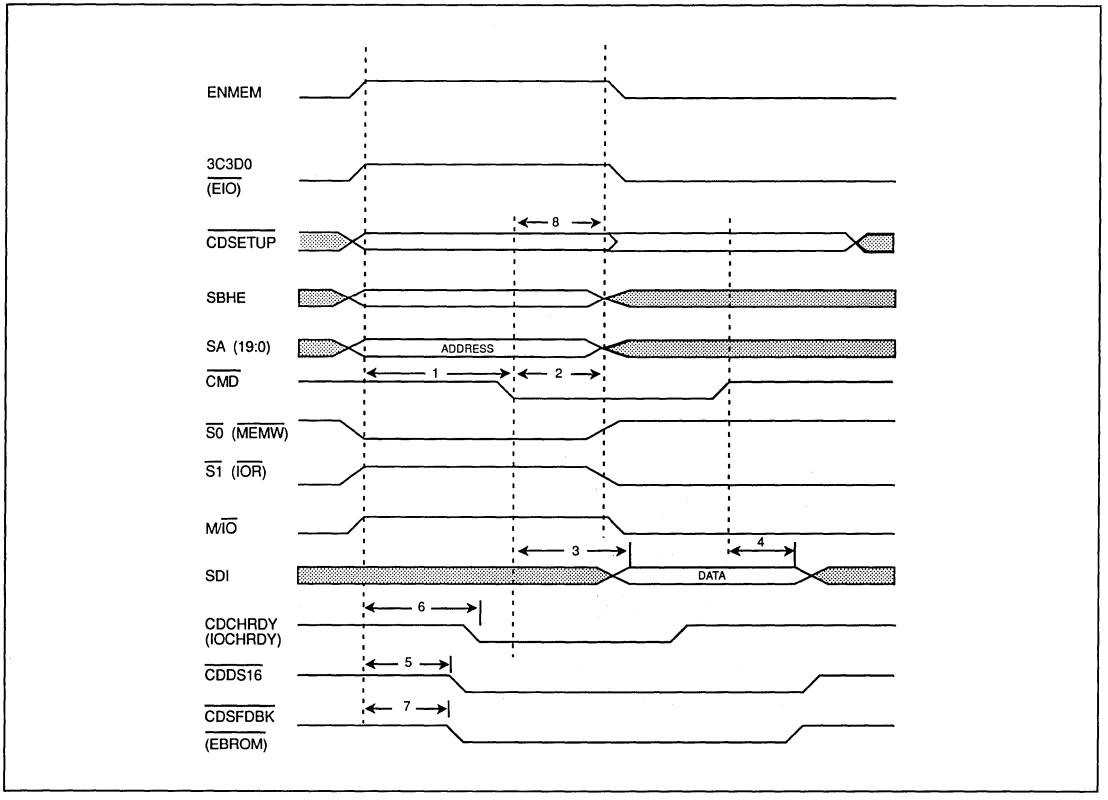

FIGURE C-7. MEMORY WRITE-MICRO CHANNEL MODE

NO.	MEMORY WRITE MC MODE			MIN.	MAX.
1	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	25	
2	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, M/IO	hold from	CMD active	30	
3	Data SDI	valid from	CMD active		25
4	Data SDI	hold from	CMD inactive	0	
5*	CDDS16	valid from	SA(19:0) ENMEM valid		45
6	SA(19:10) S0, S1	valid to	CDCHRDY inactive (low)		40
7	CDSFDBK	active from	Address Valid		58
8	CDSETUP	hold from	CMD active (low)	30	

* NOTE: CDDS16 active low.

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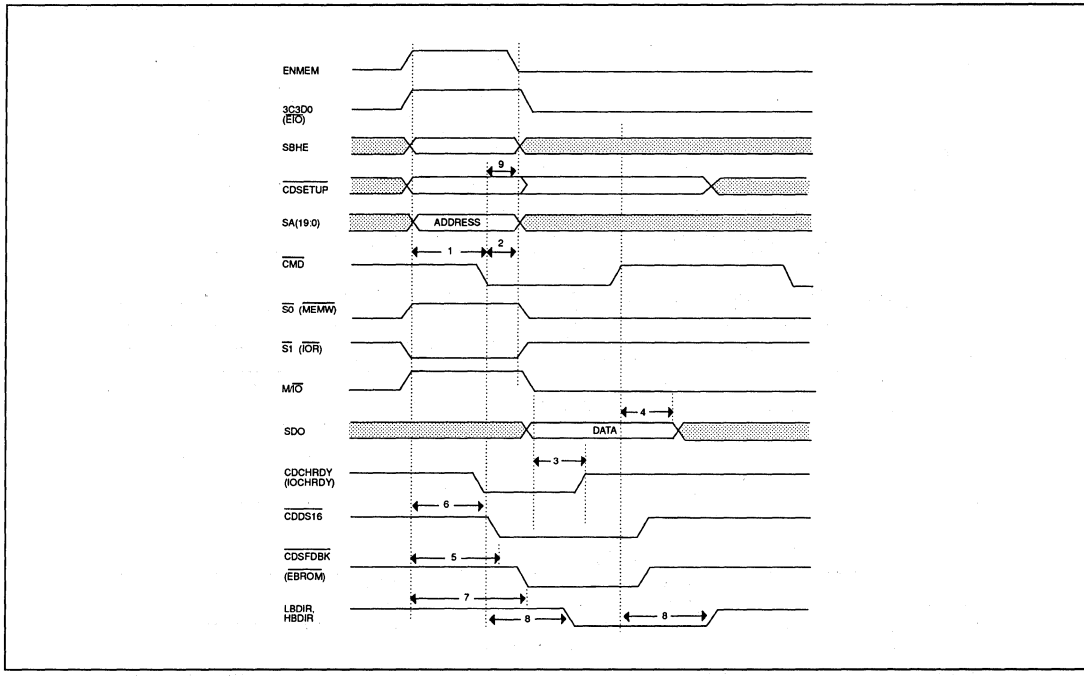

FIGURE C-8. MEMORY READ-MICRO CHANNEL MODE

NO.	MEMORY READ MC MODE			MIN.	MAX.
1	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	25	
2	SA(19:0), S0, S1 ENMEM, SBHE, 3C3D0, M/IO	hold from	CMD active	30	
3*	Read data SDO valid	setup to	CDCHRDY active (high)	2t	
4	Read data SDO	hold from	CMD inactive	20	50
5**	CDDS16	valid from	SA(19:0) ENMEM valid		45
6	SA(19:0) S0, S1	valid to	CDCHRDY inactive (low)		40
7	CDSFBK	active from	Address Valid		58
8	HBDIR, LBDIR	delay from	CMD		48
9	CDSETUP	hold from	CMD active (low)	30	

NOTES: * PR1A (7:6) = 00
** CDDS16 active low

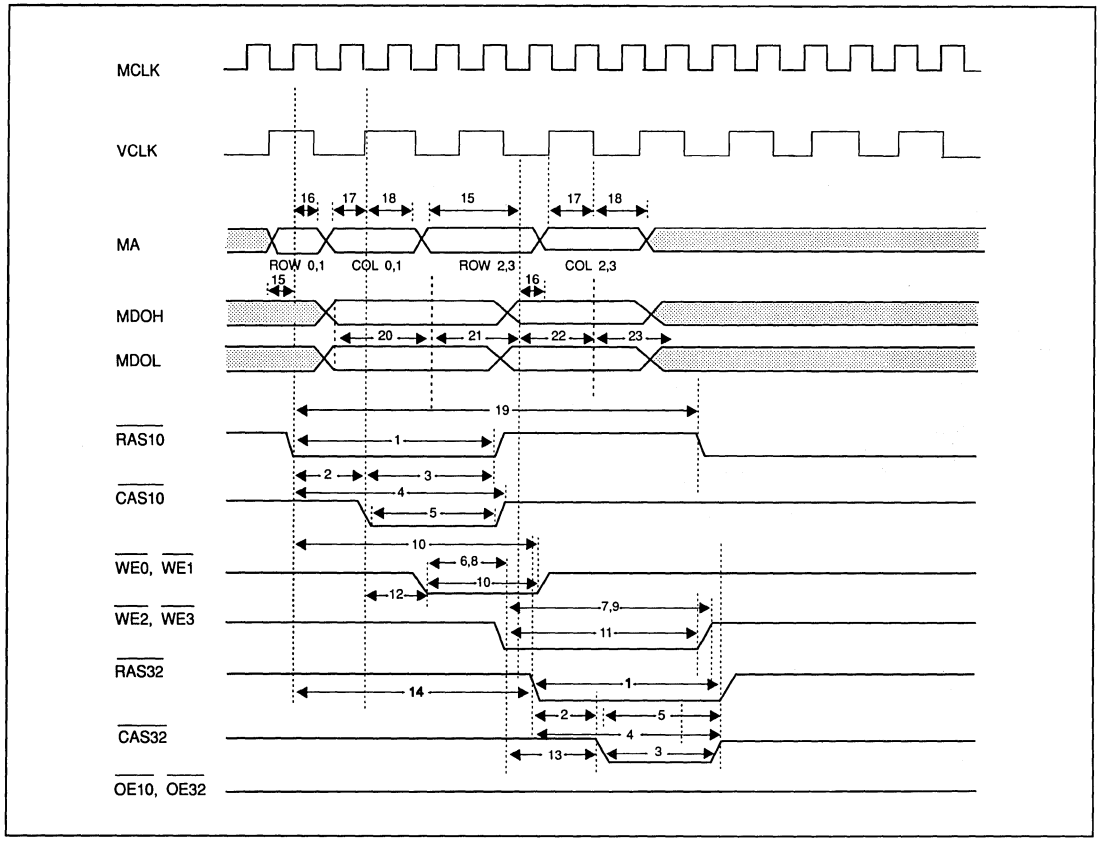

FIGURE C-9. CPU WRITE WITH NON-PAGE MODE

NO.	CPU WRITE MCLK = 45.046 MHz			MIN.	MAX.
1	$\overline{RAS10}$ ($\overline{RAS32}$)	pulse width low		5t-25	5t
2	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$) (low)	2t-11	2t+2
3	$\overline{CAS10}$ ($\overline{CAS32}$)	low to	$\overline{RAS10}$ ($\overline{RAS32}$) (high)	3t-20	3t+10
4	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$) (high)	5t-25	5t
5	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-25	3t
6	$\overline{WE0}$, $\overline{WE1}$	low to	$\overline{CAS10}$ (high)	2.5t-20	2.5t
7	$\overline{WE2}$, $\overline{WE3}$	low to	$\overline{CAS32}$ (high)	5t-20	5t
8	$\overline{WE0}$, $\overline{WE1}$	low to	$\overline{RAS10}$ (high)	2.5t-20	2.5t+2
9	$\overline{WE2}$, $\overline{WE3}$	low to	$\overline{RAS32}$ (high)	5t-20	5t+2
10	$\overline{WE0}$, $\overline{WE1}$	pulse duration		3t-20	3t
11	$\overline{WE3}$, $\overline{WE2}$	pulse duration		5t-20	5t
12	$\overline{WE0}$, $\overline{WE1}$	low from	$\overline{CAS10}$ (low)	0.5t-5	0.5t+6

t = 1/MCLK

15

NO.	CPU WRITE MCLK = 45.046 MHz (Continued)			MIN.	MAX.
13	$\overline{WE2}$, $\overline{WE3}$	low to	$\overline{CAS32}$ (low)	2t-10	2t
14	$\overline{RAS10}$	low to	$\overline{RAS32}$ (low)	4.5t-7	4.5t+7
15	Row address	setup to	$\overline{RAS10}$, $\overline{RAS32}$ (low)	t-15	t+15
16	Row address	hold from	$\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15
17	Column address	setup to	$\overline{CAS10}$, $\overline{RAS32}$ (low)	t-25	t+10
18	Column address	hold from	$\overline{CAS10}$, $\overline{CAS32}$ (low)	1.5t-5	1.5t+20
19	Random Write Cycle			9t	
20	Write Data	setup to	$\overline{WE0}$, $\overline{WE1}$ (low)	t-10	
21	Write Data	hold from	$\overline{WE0}$, $\overline{WE1}$ (low)	2t-5	
22	Write Data	setup to	$\overline{CAS32}$ (low)	2t-5	
23	Write Data	hold from	$\overline{CAS32}$ (low)	t-5	

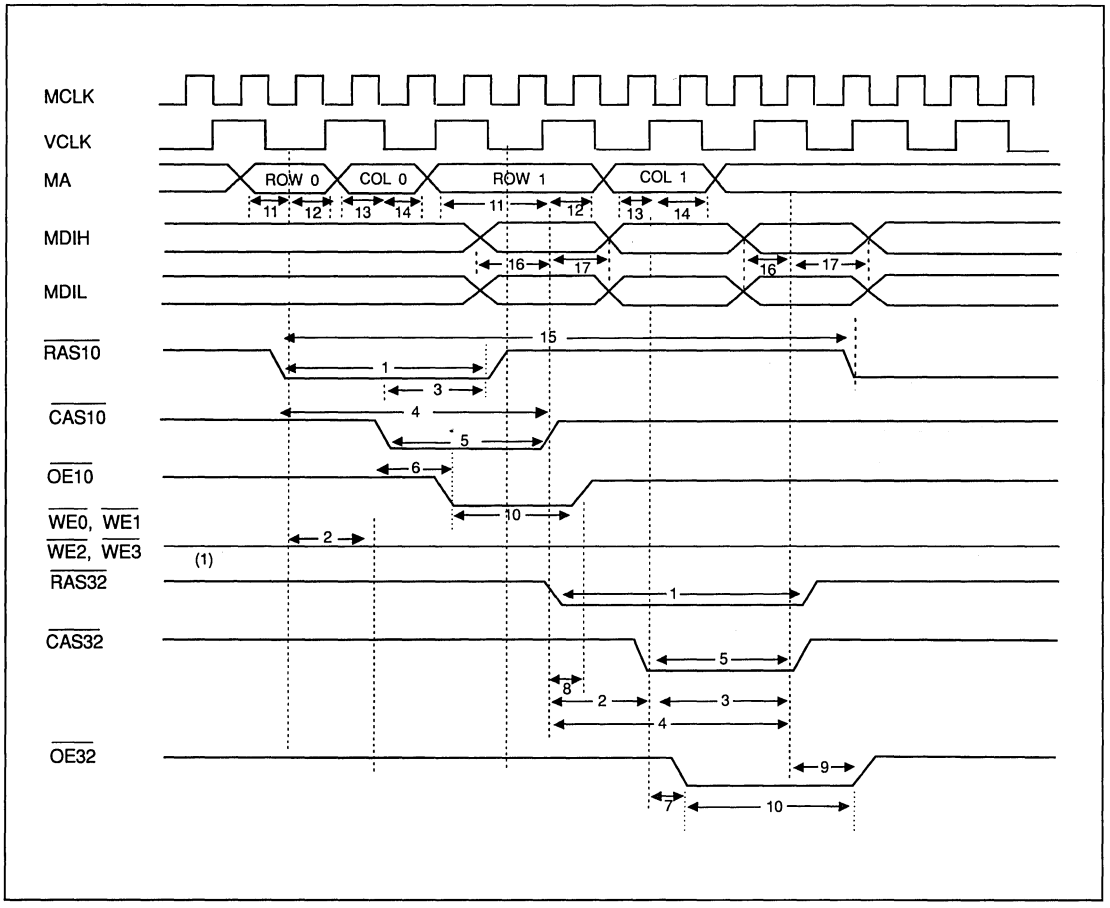

FIGURE C-10. CPU READ NON-PAGE MODE, CRT READ

NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz			MIN.	MAX.
1	$\overline{RAS10}$ ($\overline{RAS32}$)	pulse width low		5t-25	5t
2	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$) (low)	2t-11	2t+2
3	$\overline{CAS10}$ ($\overline{CAS32}$)	low to	$\overline{RAS10}$ ($\overline{RAS32}$) (high)	3t-15	3t+10
4	$\overline{RAS10}$ ($\overline{RAS32}$)	low to	$\overline{CAS10}$ ($\overline{CAS32}$) (high)	5t-20	5t
5	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-20	3t
6	$\overline{CAS10}$	low to	$\overline{OE10}$ (low)	t-6	t+5
7	$\overline{CAS32}$	low to	$\overline{OE32}$ (low)	t-6	t+5
8	$\overline{CAS10}$	high to	$\overline{OE10}$ (high)	t-6	t+5

t = 1/MCLK

15

NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz (Continued)			MIN.	MAX.
9	$\overline{CAS32}$ high	to	$\overline{OE32}$ (high)	t-6	t+5
10	$\overline{OE10}$, $\overline{OE32}$	pulse width low		3t-20	3t
11	Row address	setup to	$\overline{RAS10}$, $\overline{RAS32}$ (low)	t-12	t+10
12	Row Address	hold from	$\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15
13	Column Address	setup to	$\overline{CAS10}$, $\overline{CAS32}$ (low)	t-12	t+10
14	Column Address	hold from	$\overline{CAS10}$,$\overline{CAS32}$ (low)	1.5t	1.5t+25
15	Random Read Cycle			9t-2	
16	Read Data	setup to	$\overline{CAS10}$, $\overline{CAS32}$ (high)	10	
17	Read Data	hold from	$\overline{CAS10}$, $\overline{CAS32}$ (high)	15	

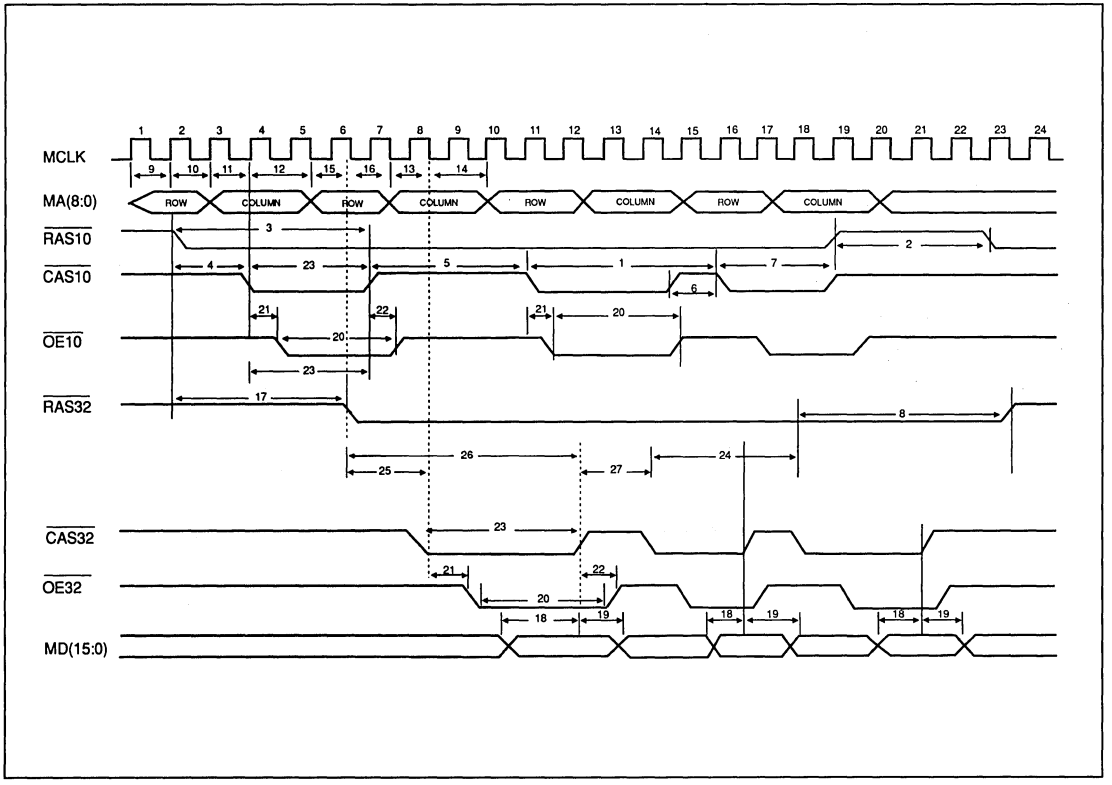

FIGURE C-11. DRAM PAGE MODE-READ TIMING

NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz			MIN.	MAX.
1*	Page mode	cycle time	$\overline{CAS10}$ low to CAS low	5t-2	
2	$\overline{RAS10}$	Precharge		4t-6	4t+14
3	$\overline{RAS10}$	low to	$\overline{CAS10}$ high (first)	5t-20	5t-2
4	$\overline{RAS10}$	low to	$\overline{CAS10}$ low	2t-11	2t+2
5	First $\overline{CAS10}$	pulse width high		4t-10	4t+10
6	$\overline{CAS10}$	pulse width high		2t-10	2t+10
7	$\overline{CAS10}$	low to	$\overline{RAS10}$ high	3t-15	3t+4
8	$\overline{CAS32}$	low to	$\overline{RAS32}$ high	5t-15	5t+4
9	Row address	setup to	$\overline{RAS10}$ low	t	t+16
10	Row address	hold from	$\overline{RAS10}$ low	t-5	t+5
11	Column address	setup to	$\overline{CAS10}$ low	t-15	t+1
12	Column address	hold from	$\overline{CAS10}$	1.5t	1.5t+18
13	Column address	setup to	$\overline{CAS32}$	t-15	t+8

* First cycle is +2t longer than this spec
t = 1/MCLK

NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz (Continued)			MIN.	MAX.
14	Column address	hold from	$\overline{CAS32}$ low	1.5t-15	1.5t+2
15	Row address	setup to	$\overline{RAS32}$ low	t-15	t+5
16	Row address	hold from	$\overline{RAS32}$ low	t-8	t+5
17	$\overline{RAS32}$	low from	$\overline{RAS10}$ low	4.5t-7	4.5t+7
18	Read data	setup to	CAS high	10	
19	Read data	hold from	CAS high	15	
20	$\overline{OE10}$ ($\overline{OE32}$)	pulse width low		3t-20	3t
21	$\overline{OE10}$ ($\overline{OE32}$)	low after	$\overline{CAS10}$ low ($\overline{CAS32}$)	t-6	t+6
22	$\overline{OE10}$ ($\overline{OE32}$)	high after	$\overline{CAS10}$ high ($\overline{CAS32}$)	t-6	t+6
23	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-20	3t
24	Page mode	cycle time	$\overline{CAS32}$ low to $\overline{CAS32}$ low	5t-2	
25	$\overline{RAS32}$	low to	$\overline{CAS32}$ high (first)	5t-22	5t
26	$\overline{RAS32}$	low to	$\overline{CAS32}$ low	2t-11	2t+2
27	First $\overline{CAS32}$	pulse width high		2t-11	2t+11

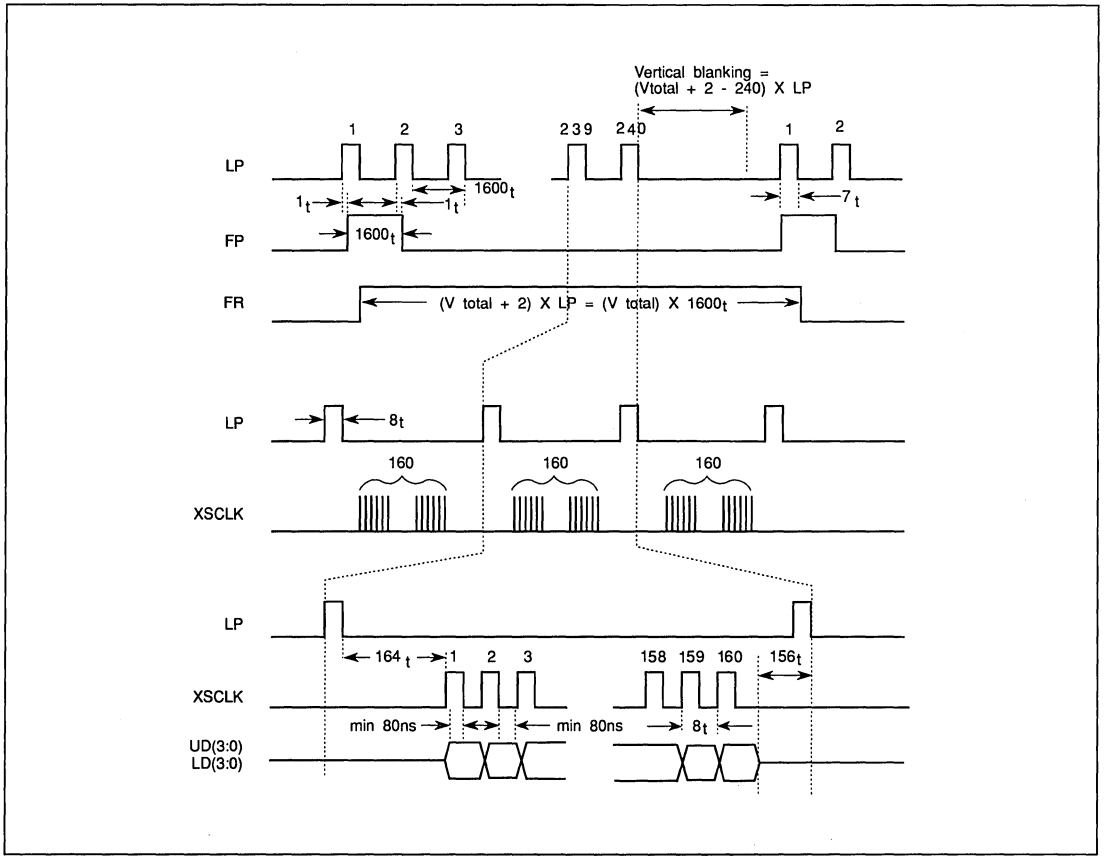

FIGURE C-12. WD90C22 LCD TIMING DIAGRAM (t=VCLK)

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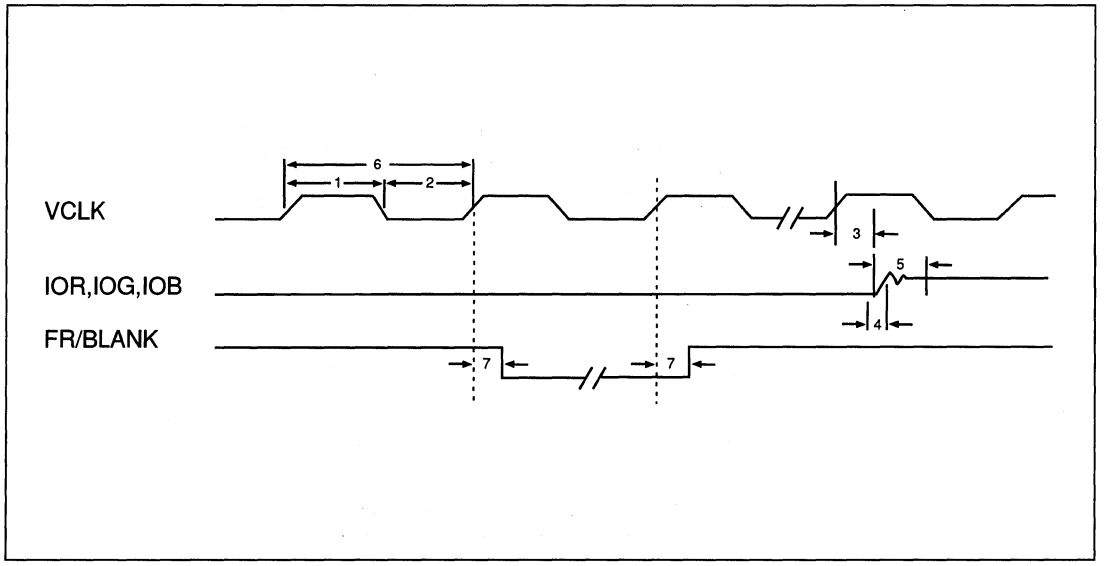

FIGURE C-13. RAMDAC TIMING

NO.	PARAMETER	MIN.	TYPICAL	MAX	UNITS
1	VCLK Pulse Width High Time	9			ns
2	VCLK Pulse Width Low Time	9			ns
3	Analog Output Delay			30	ns
4	Analog Output Rise/Fall Time		3		ns
5	Analog Output Settling Time		20		ns
6	Clock Frequency			45	MHz
7	Blanking Delay Time			30	ns

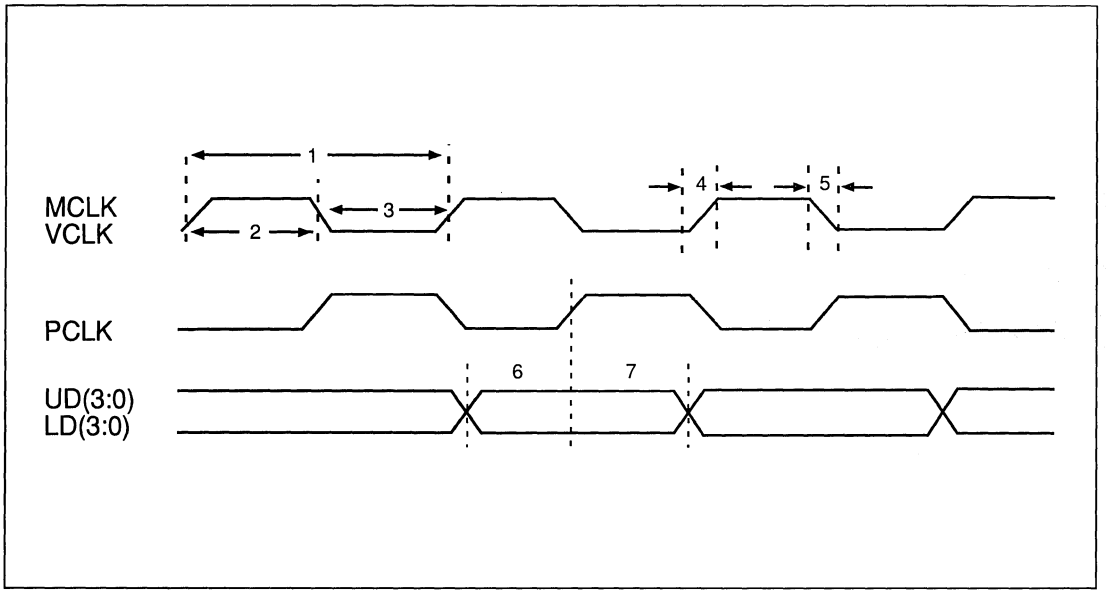

FIGURE C-14. CRT CLOCK TIMING

NO.	PARAMETER	MIN.	MAX
1	Input Clock (VCLK, MCLK)	t	t
2	Input Clock High Time	40%	60%
3	Input Clock Low Time	40%	60%
4	Input Clock Rise Time		3
5	Input Clock Fall Time		3
6*	UD(3:0), LD(3:0) setup time to PCLK (high)		
	Mode 0	20	
	Mode 3	10	
	Mode 4	20	
	Mode 12	10	
	Mode 13	20	
7*	UD(3:0), LD(3:0) hold time from PCLK (high)		
	Mode 0	10	
	Mode 3	10	
	Mode 4	10	
	Mode 12	10	
	Mode 13	2	

* For external RAMDAC

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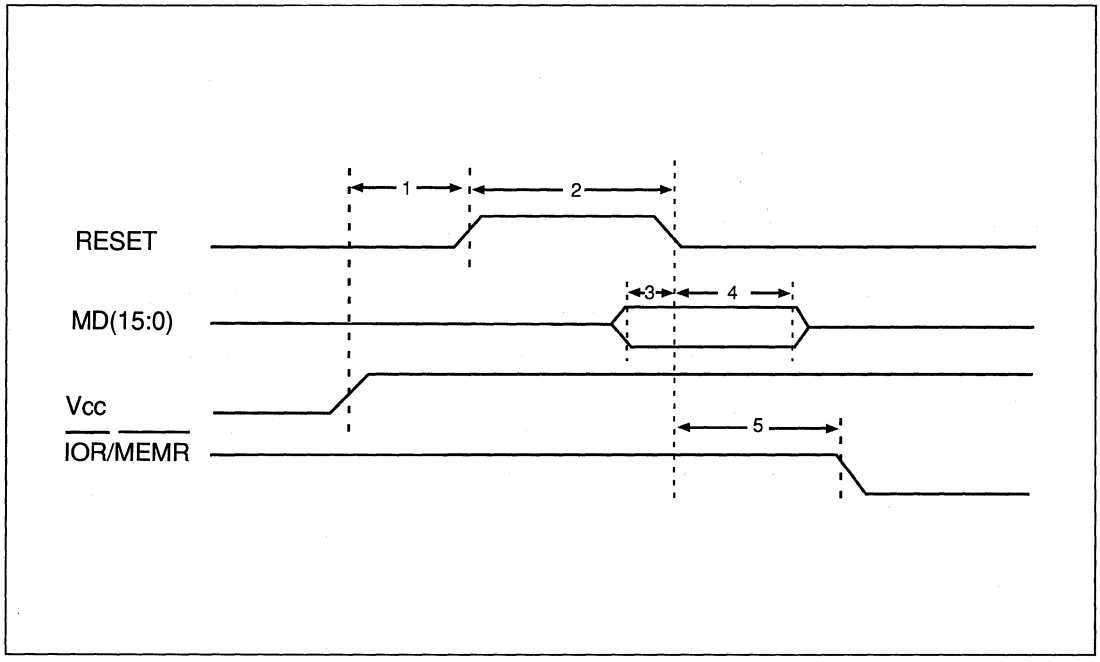


FIGURE C-15. RESET TIMING

NO.	PARAMETER			MIN.	MAX.
1	Vcc	high to	RESET (high)	100ns	
2	RESET	pulse width		100t	
3	MD(15:0)	setup to	RESET (low)	2t	
4	MD(15:0)	hold from	RESET (low)	2t	
5	RESET	to first	$\overline{IOR}/\overline{MEMR}$	10t	

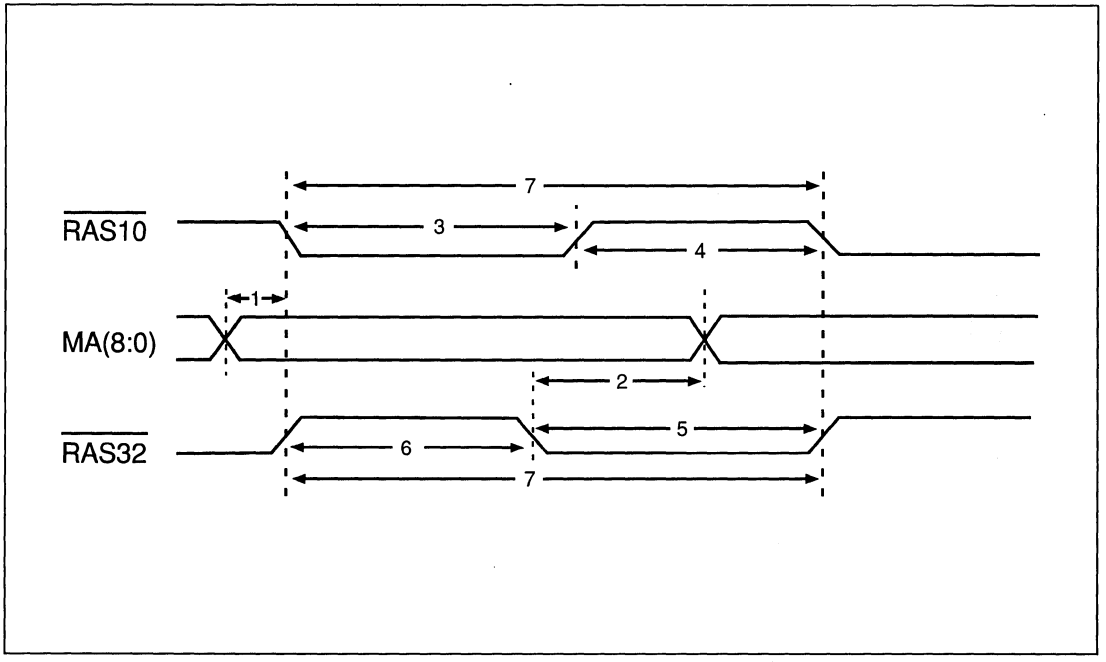


FIGURE C-16. RAS ONLY DRAM REFRESH TIMING

NO.	PARAMETER			MIN.	MAX.
1	MA(8:0)	setup to	$\overline{RAS10}$ active	t	
2	MA(8:0)	hold to	$\overline{RAS32}$ active	t	
3	$\overline{RAS10}$	low time		5t-20	5t+10
4	$\overline{RAS10}$	high time		4t-10	
5	$\overline{RAS32}$	low time		5t-20	
6	$\overline{RAS32}$	high time		4t-10	4t+10
7	$\overline{RAS}$	cycle time		9t-10	9t+10

t = MCLK

15

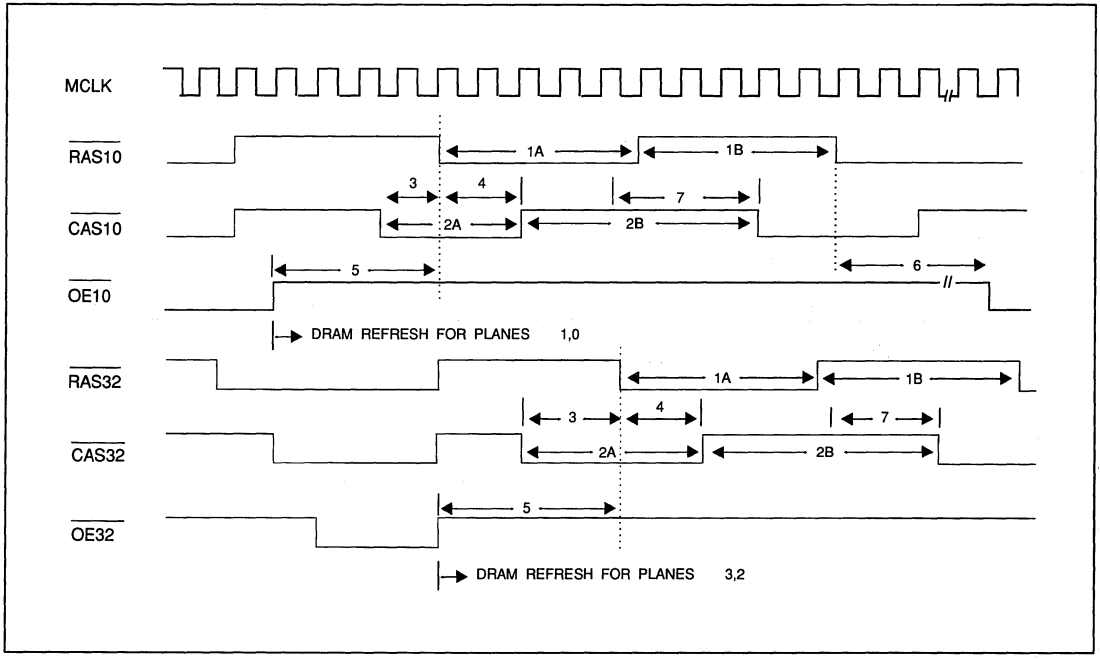


FIGURE C-17. CAS BEFORE RAS DRAM REFRESH TIMING

NO.	CAS BEFORE RAS DRAM REFRESH TIMING		MIN.	MAX.
1A	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width low		5t-10	5t+10
1B	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width high		5t-10	5t+10
2A	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width low		4t-5	4t+5
2B	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width high		6t-5	6t+5
3	$\overline{CAS10}$ ($\overline{CAS32}$) low to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	2t-10	2t+10
4	$\overline{RAS10}$ (RAS32) low to	$\overline{CAS10}$ ($\overline{CAS32}$) (high)	2t-10	2t+10
5	$\overline{OE10}$ ($\overline{OE32}$) high to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	4t-8	5t+8
6	$\overline{RAS10}$ (RAS32) low to	$\overline{OE10}$ ($\overline{OE32}$) (low)	30t	
7	$\overline{RAS10}$ (RAS32) high to (Precharge)	$\overline{CAS10}$ ($\overline{CAS32}$) (low)	3t-5	3t+20

t = 1/MCLK

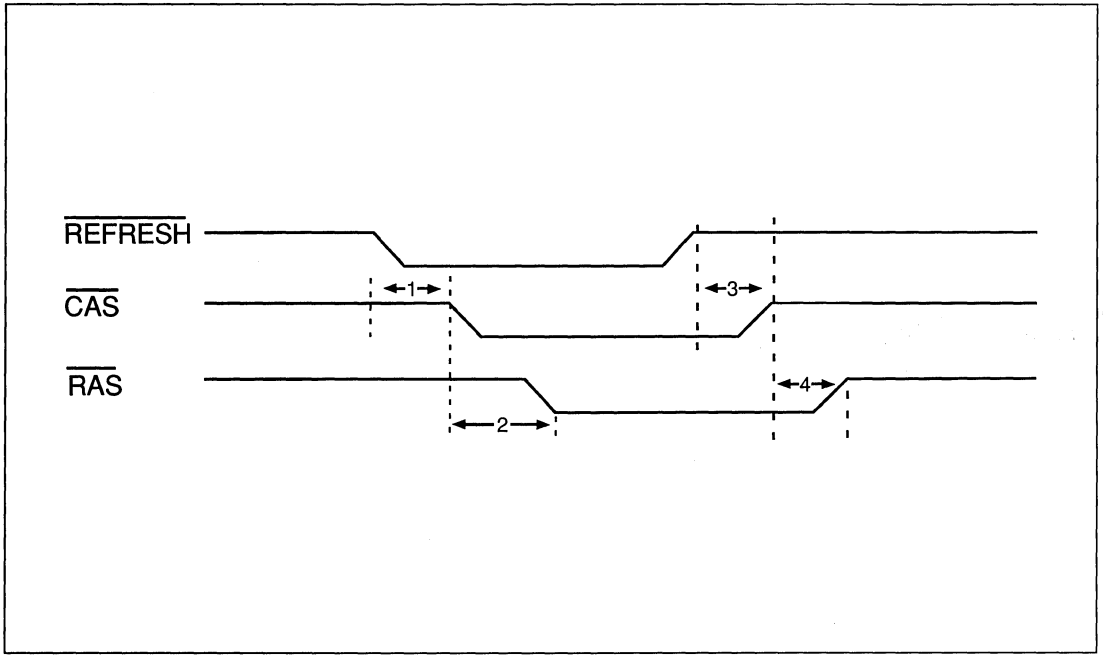
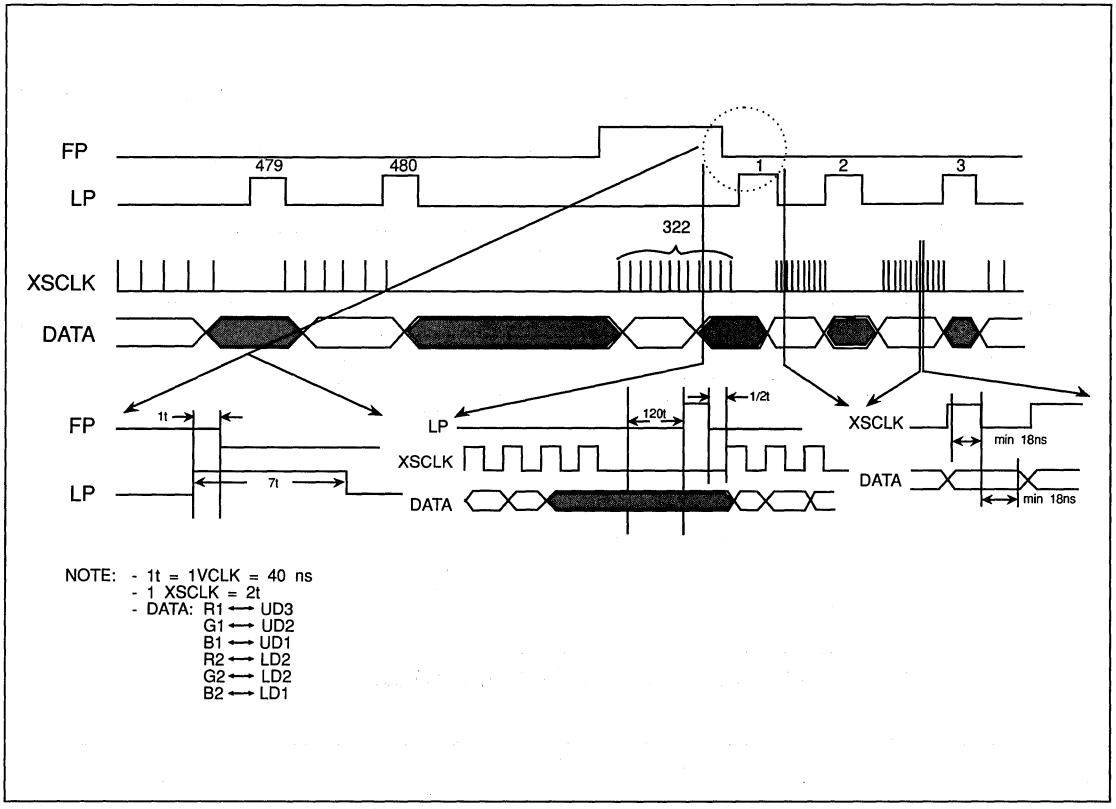


FIGURE C-18. CAS BEFORE RAS REFRESH (Power-Down Mode)

NO.	PARAMETER			MIN.	MAX.
1	$\overline{CAS}$ low	from	$\overline{REFRESH}$ (low)	20	
2	$\overline{RAS}$ low	from	$\overline{CAS}$ (low)	30	
3	$\overline{CAS}$ high	from	$\overline{REFRESH}$ (high)	20	
4	$\overline{RAS}$ high	from	$\overline{CAS}$ (high)	30	

15



NOTE: - 1t = 1VCLK = 40 ns
- 1 XSCLK = 2t
- DATA: R1 ⟷ UD3
G1 ⟷ UD2
B1 ⟷ UD1
R2 ⟷ LD2
G2 ⟷ LD2
B2 ⟷ LD1

FIGURE C-19. STN COLOR LCD INTERFACE TIMING

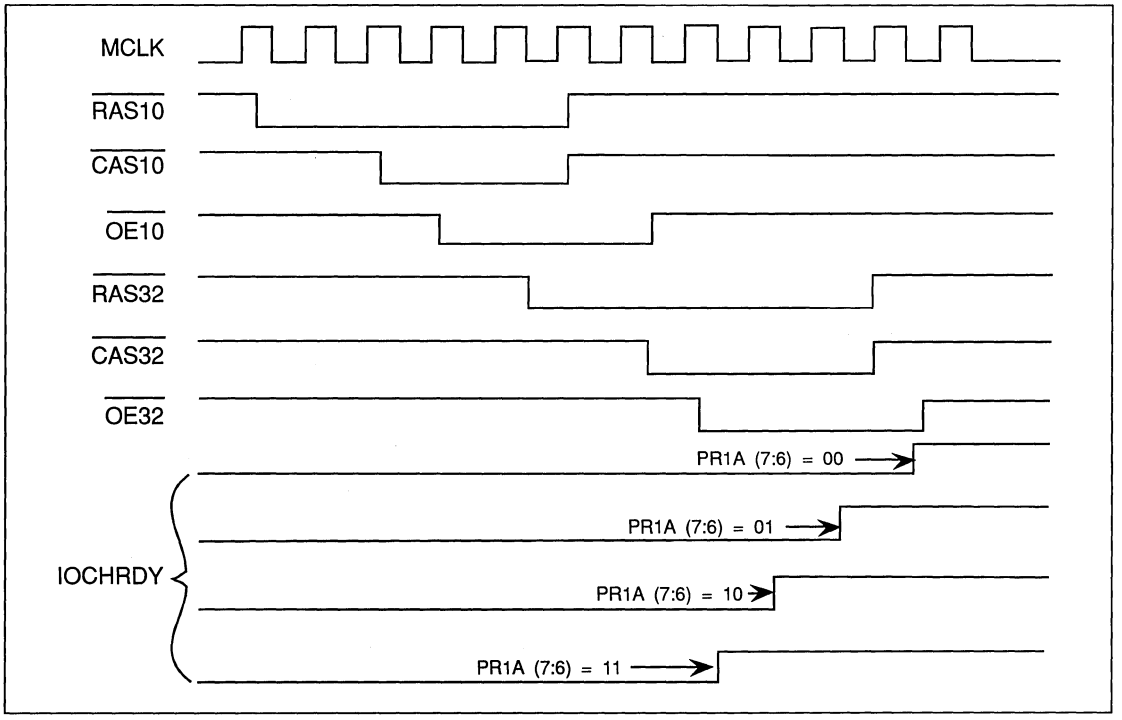


FIGURE C-20. IOCHRDY RELEASE TIMING IN MEMORY READ CYCLE

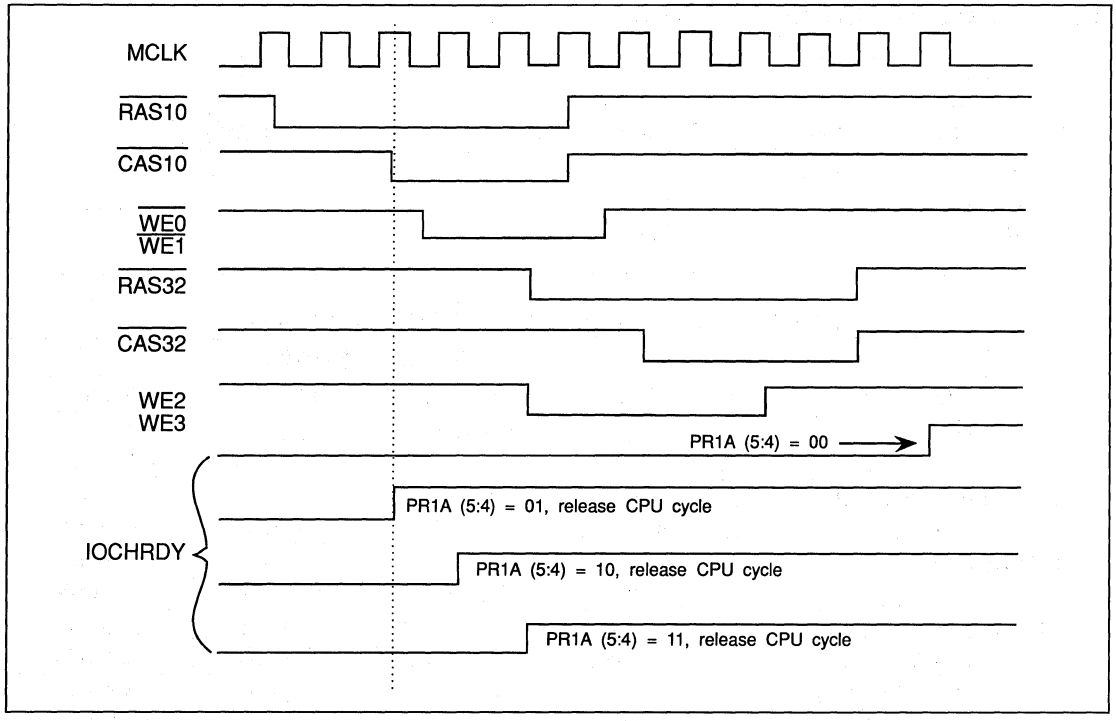


FIGURE C-21. IOCHRDY RELEASE TIMING IN MEMORY WRITE CYCLE

C.1 DC and RAMDAC SPECIFICATIONS

SUPPLY PINS			
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VCC	4.1V	4.7V	Pins 9, 28, 53, 67, 94
RVCC	4.75V	5.25V	Pin 108
AVCC	4.75V	5.25V	Pin 123

WD90C22 TYPICAL CURRENT/POWER CONSUMPTION				
	FREQUENCY (MHz)			
MODE	**25 MHz**	**28 MHz**	**32 MHz**	**36 MHz**
DISPLAY ACTIVE	149.4 mA 671.5 mW	166.8 mA 750.0 mW	182.8 mA 822.2 mW	197.9 mA 890.3 mW
SYSTEM POWERDOWN *	2.0 mA 9.4 mW	2.0 mA 9.4 mW	2.0 mA 9.4 mW	2.0 mA 9.4 mW
DISPLAY IDLE	16.0 mA 72.0 mW	18.0 mA 80.5 mW	20.5 mA 91.5 mW	21.5mA 96.0 mW
GENERAL POWERDOWN W/EXT. CLK CONTROL **	25.0 mA 113.0 mW	25.0 mA 113.0 mW	25.0 mA 113.0mW	25.0 mA 113.0 mW
GENERAL POWERDOWN W/INT. CLK CONTROL	16.0 mA 72.0 mW	18.0mA 80.5 mW	20.5 mA 91.5 mW	21.5 mA 96.0 mW

Conditions: AVCC (pin 123) = 5.0 volts
RVCC (pin 108) = 5.0 volts,
DIGITAL VCCs (pins 9, 28, 53, 67, 94) = 4.4 volts
Display type active when measurements taken: LCD.

* - VCLK frequency is 32 KHz
** - VCLK frequency is 2.0 MHz

INPUT PINS			
PINS	LA17-19, SBHE, MEMEN, $\overline{\text{EIO}}$/3C3D0, $\overline{\text{ALE}}$, $\overline{\text{MEMR}}$/M/$\overline{\text{IO}}$, $\overline{\text{PWRDN}}$, $\overline{\text{MEMW}}$/S0, $\overline{\text{IOR}}$/S1, $\overline{\text{IOW}}$/CMD, RESET, $\overline{\text{REFRESH}}$, MCLK, VCLK0, SA0-16 (PINS 3-8, 11, 38-44, 98, 99, 117-122, 124-132, 1, 2)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC

TABLE C-2. D.C. TEST SPECIFICATIONS

15

PIN	VREF (PIN 111)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIN ANALOG	-0.5V	2.0V	
IIL	-10 uA	10 uA	VIN = 0V TO VCC
	-100 uA	100 uA	VIN = 0V TO VCC+0.6V

PIN	MDETECT/FSADJUST (PIN 112)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC

PIN	ALL INPUTS		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
CIN		6 PF	

PINS	IRQ/$\overline{\text{IRQ}}$, MA0-8, $\overline{\text{RAS10}}$, $\overline{\text{RAS32}}$, $\overline{\text{CAS10}}$, $\overline{\text{CAS32}}$, $\overline{\text{WE0}}$, $\overline{\text{WE1}}$, $\overline{\text{WE2}}$, $\overline{\text{WE3}}$, $\overline{\text{OE10}}$, $\overline{\text{OE32}}$ (PINS 12, 45-52, 55-65)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 3.0mA
VOH	2.4V		IOH = -4.8mA

PINS	$\overline{\text{EBROM}}$/$\overline{\text{CDSFDBK}}$, HBDIR, LBDIR, LP/HSYNC, FP/VSYNC, FR/BLANK, $\overline{\text{RPLT}}$, WPLT/VD9, LD0-3, UD0-3, (PINS 13, 16, 17, 89-93, 100-107)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 1.5mA
VOH	2.4V		IOH = -3.6mA

PINS	MEMCS16\CDS16, IOCHRDY (PINS 14, 15)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 16.0mA
VOH	2.4V		IOH = -8.0mA

TABLE C-2. D.C. TEST SPECIFICATIONS (CONTINUED)

PINS	RED, GREEN, BLUE (PINS 114-116)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOUT	-0.5	1.5	See RAMDAC Specification

PIN	$\overline{\text{LCD/CRT}}$ (PIN 110)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

PINS	PCLK, XSCLK, WGTCLK (PINS 86-88)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

I/O PINS			
PINS	**VCLK2, VCLK1 (PINS 96, 97)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 1.5 mA
VOH	2.4V		IOH = -3.6mA
IOZ	-50 uA	50uA	VOUT = 0V TO VCC

PINS	SD0-15, MD0-15 (PINS 36-29, 26-19, 84-77, 75-68)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 3.0 mA
VOH	2.4V		IOH = -4.8mA
IOZ	-50 uA	50uA	VOUT = 0V TO VCC

PINS	ALL OUTPUTS AND I/O'S		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
COUT		30 PF	

TABLE C-2. TEST SPECIFICATIONS (CONTINUED)

15

PINS	BLUE, GREEN, RED PINS (114-116)			
PARAMETER	**MIN**	**TYP**	**MAX**	**CONDITIONS**
DAC RESOLUTION		6 BITS		
INTEGRAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
DIFFERENTIAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
WHITE LEVEL RELATIVE TO BLACK	13.38mA	14.08mA	14.79mA	VREF = 1.235, RSET = 221 Ohms
BLACK LEVEL	-20uA		20uA	
GRAY SCALE CURRENT RANGE			20mA	
LSB SIZE		223.5 uA		VREF = 1.235, RSET = 221 Ohms
GRAY SCALE ERROR			5.0%	
GLITCH ENERGY			50 pJOULES	
SETTLING TIME			20 NS	R <= 150 Ohms, 100 PF
CLOCK FEED THROUGH			20 pCOULOMB	
DAC TO DAC MATCHING			5%	
OUTPUT COMPLIANCE CURRENT TOLERANCE	-5%		+5%	
OUTPUT COMPLIANCE VOLTAGE RANGE	-0.5V		+1.5V	
VOLTAGE REFERENCE	1.14	1.235	1.26	
VOLTAGE REFERENCE INPUT CURRENT			10 uA	

TABLE C-3. RAMDAC SPECIFICATIONS

D.0 PACKAGE DIMENSIONS AND SPECIFICATIONS

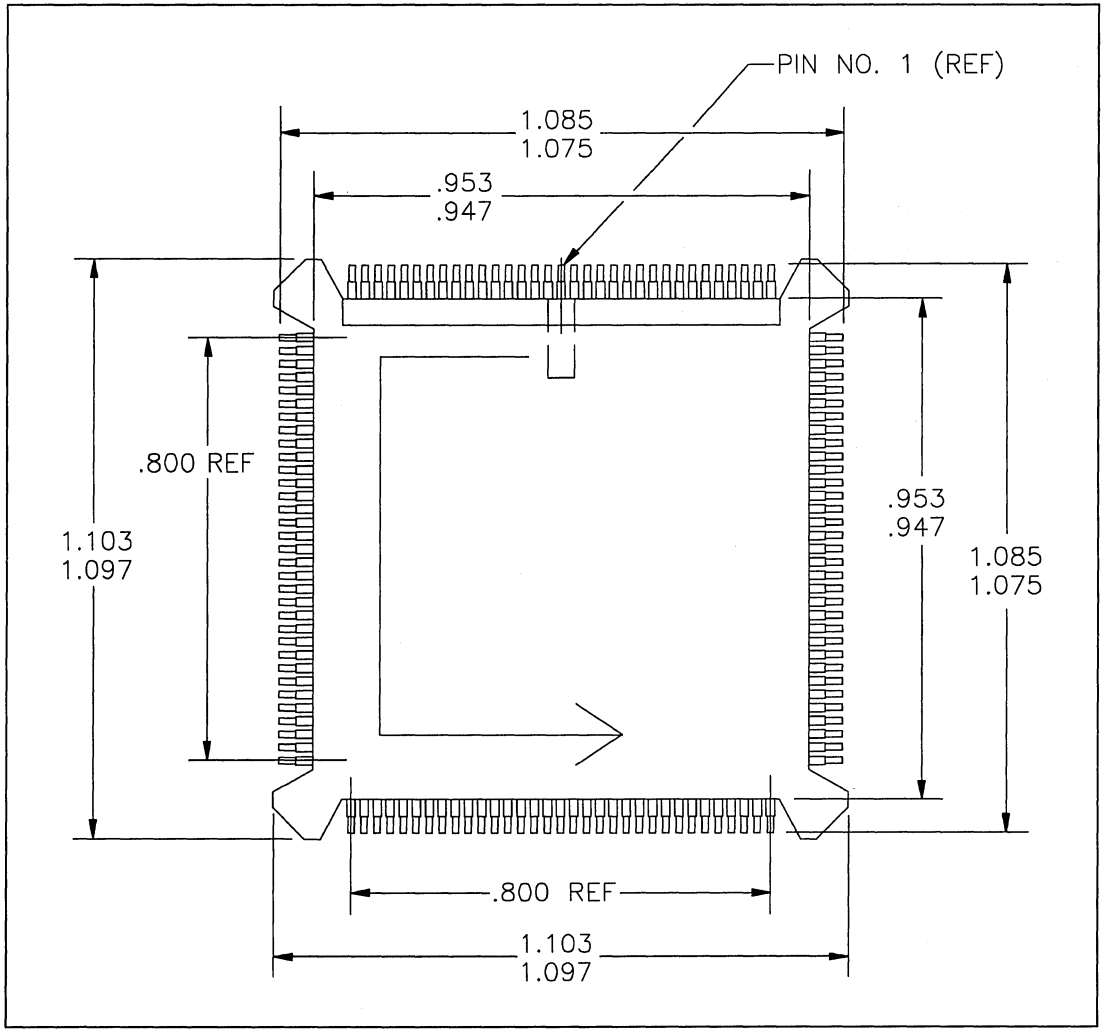
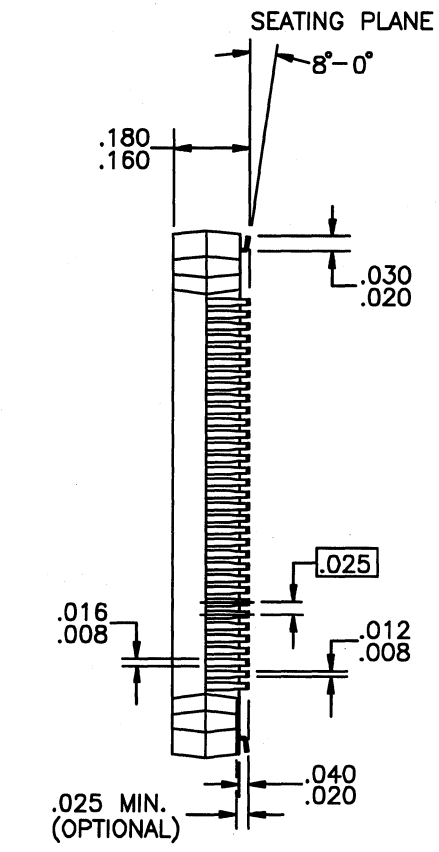
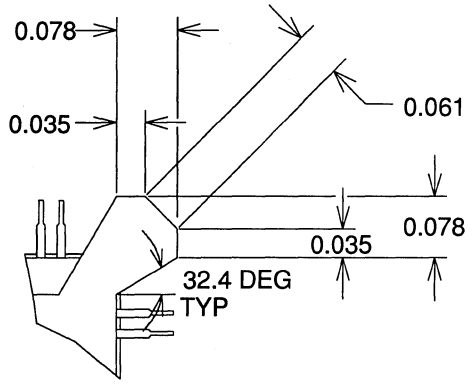


FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE

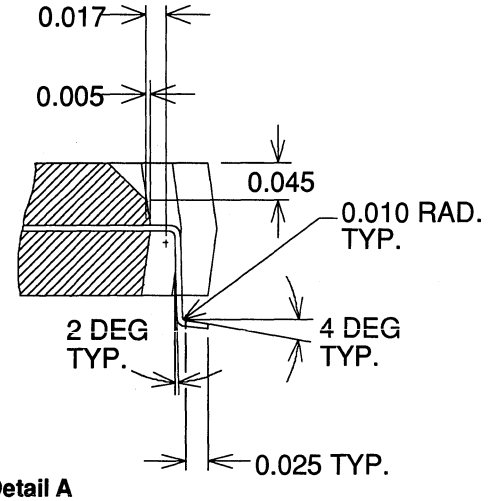
15



Side View



Bumper Detail



Detail A

FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE (CONTINUED)

E.0 MAXIMUM RATINGS

Ambient temperature under bias	$0^{o}C$ to $70^{o}C$
Storage temperature	$-40^{o}C$ to $125^{o}C$
Voltage on all inputs and outputs with respect to Vss	-0.3 to 6.5 volts
Power dissipation	1.2 watt
Power Supply Voltage	4.1 to 4.7 volts

NOTE: Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to maximum rating conditions for extended periods may affect product reliability.

WD90C26

VGA Flat Panel

Display Controller

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

This introduction contains the following information:

- Product Scope
- Product Features
- General Description

1.1 SCOPE

The WD90C26 VGA Laptop Display Controller allows control of a flat-panel display, along with simultaneous display on a traditional CRT. The WD90C26 supports all of today's mono and color flat-panel technologies.

The WD90C26 has improved power management capabilities and a performance-scaling capability that makes it an ideal video solution for low battery drain portable computer applications.

1.2 FEATURES

- True 64-gray scale in including 640 by 480 by 256 mode
- Simultaneous display (with all types of flat-panels)*
- 'WD90C26LV' low voltage version available
- On-board VGA compatible RAMDAC
- Zero wait-state performance
- Adjustable video FIFO depth and fast page mode memory timing
- System interface write buffering
- Flexible display memory configuration (2, 3 or four 256K by 4 DRAMs or one 256K by 16 DRAM)
- 8- or 16-bit I/O and memory interface
- True 16-bit CPU to display memory data transfer in all modes
- 27K colors on 9-bit TFT color LCD panel, 256K colors on 9-bit STN LCD panel, and 4K undithered direct colors on 12-bit TFT color LCD panel
- Full screen presentation in simultaneous display mode
- Hardware auto-centering and vertical expansion
- Up to 16 loadable fonts
- Supports 800 by 600 by 256 and 1024 by 768 by 16 non-interlaced modes on CRT display
- Hidden register support for 100% hardware compatibility with IBM's VGA standards
- 100% compatibility with CGA, MDA, Hercules Graphics
- Typical power dissipation of 450 mW at 5V operation
- Up to 65 MHz maximum video clock rate on CRT display
- Up to 45 MHz maximum video clock rate on LCD display
- Up to 45 MHz maximum memory clock rate
- On-chip 8/16-bit ISA Bus (AT bus) interface
- On-chip 8- or 16-bit Micro Channel interface
- I/O mapping improves board level testability
- Enhanced power down management modes
- 144-pin EIAJ package
- Compatible with WD90C55 color STN LCD interface

* Patent pending

1.3 GENERAL DESCRIPTION

The Western Digital WD90C26 is a 0.9 micron CMOS VGA controller designed to simultaneously drive a flat-panel display and the traditional analog CRT with a minimum of external components. The only additional components required for a complete flat-panel VGA subsystem are 1, 2, 3, or 4 DRAMs and video/memory clock sources. Contained on-board are a RAMDAC and a flat-panel interface. The full-featured RAMDAC is capable of directly driving P/S2 style analog color or monochrome

monitors. The full-featured flat-panel interface is capable of supporting LCD, plasma, and EL and other flat-panel technologies.

The WD90C26's scalable architecture allows it to be used with either 2, 3, or 4 external 256K by 4 DRAMs or one 256K by 16 DRAM. Basic VGA performance is available with the minimum 2 DRAM configuration or the single 256K by 16 DRAM con-fig-uration. Added panel support and enhanced VGA modes are available using 3 or 4 256K by 4 DRAMs. 16-bit video memory performance is also available using the 4 256K by 4 DRAM configuration or the single 256K by 16 DRAM configuration. DRAM utilization is firmware controllable, allowing the scaling of DRAM power consumption or increasing performance.

Western Digital's superior orthogonal 64-gray scale to 64-gray scale mapping technology allows system developers to 'hand tune' each of the shades in the 64-gray scale to provide the most realistic linear gray scale shading for a particular panel. This is achieved through use of a firmware programmable 64-word gray scale lookup table on-board the WD90C26.

As with all Western Digital VGA offerings, the WD90C26 is 100% compatible with IBM VGA, CGA, MDA, and Hercules video systems. Through the use of its hidden, or 'shadow' registers, the WD90C26 can be programmed to support fixed-LCD screen sizes, yet appear to the host as capable of displaying the variety of screen pitches available with analog monitors. System routine modifications to video system registers, thus shadowed or hidden, do not destroy the WD90C26's ability to display the desired information on a flat-panel display as well.

The WD90C26's auto-centering and vertical expansion features provide full-screen flat-panel displays even in video modes with lower resolutions than those of the panel. A unique expansion algorithm provides for realistic appearance of both text and graphics on expanded displays, without requiring the use of special expanded display fonts.

Advanced power management features include:

- Separate supply pins for certain functions so that parts of the chip may be externally powered off
- The capability to slow down internal clocks to conserve power and to deactivate or tri-state I/O pins during power-down and reset modes
- Power sequencing that can be used to control power supply and interface signals, and to prevent panel burnout

Also included in the WD90C26 is an advanced TFT support circuit that allows display from a palette of 27K colors on 9-bit interface color panels.

The WD90C26 directly supports TFT displays with 12-bit interfaces with undithered 12-bit direct colors from a 4K palette for optimum 12-bit display performance.

2.0 ARCHITECTURE

This section describes the architecture of the WD90C26. A block diagram of the architecture is shown in Figure 2-1. The components described are:

- System Interface Logic
- CRT Controller
- Video Sequencer
- Video Graphics Controller
- Video Attribute Controller
- RAMDAC
- Flat Panel Adapter
- Display Memory Interface
- Power-Down Control

2.1 SYSTEM INTERFACE LOGIC

The WD90C26 includes a host system interface for direct connection to an ISA standard bus or IBM compatible Micro Channel. The interface allows the following features:

- Full 16-bit I/O and memory cycles
- Zero wait-state performance capability
- 16-bit to 8-bit data path conversion
- Full decoding of 16 MBytes of memory space for mapping of video memory, without requiring external decode logic
- Internal buffering of system operations to speed performance
- External video BIOS ROM

2.2 CRT CONTROLLER

A VGA-compatible CRT controller includes the following functions:

- Generates video buffer addresses for screen refresh operations
- Generates monitor synchronization signals
- Controls an alpha-numeric cursor
- May be set with remapped register locations to operate as a CGA, MDA, or Hercules
- Register shadowing

2.3 VIDEO SEQUENCER

The VGA compatible video sequencer is the central timing and memory control section of the WD90C26. Its functions include the following:

- Generation of memory handshake signals
- Control of CRT controller timings
- Provision of general interface timing and control signals to the balance of the WD90C26

2.4 VIDEO GRAPHICS CONTROLLER

The VGA video graphics controller performs VGA graphics operations on video data such as AND, OR, XOR, rotate, and color comparison functions.

2.5 VIDEO ATTRIBUTE CONTROLLER

The WD90C26's video attributes are added to display data by the Video Attribute Controller. Data added includes:

- Standard text attributes
- VGA graphics mode attributes
- Cursor display
- Screen border color

The Video Attribute Controller also performs data conversion from modes like packed pixel, planar, or text mode into video data to be presented to the RAMDAC.

2.6 RAMDAC

Integrated into the WD90C26 is a fully VGA-compatible high-speed 18-bit RAMDAC. This RAMDAC directly drives VGA and super-VGA color or monochrome analog monitors.

2.7 FLAT-PANEL ADAPTER

The flat-panel adapter takes video information from the WD90C26's internal RAMDAC color palette RAM and converts it into the format appropriate for the type of panel to be attached.

The following functions occur in the flat-panel adapter:

- "Digital DAC" color to monochrome gray scale conversion
- Gray scale mapping
- Gray shade dithering
- Color STN LCD panel dithering circuitry
- Row buffering
- Frame buffering
- Panel format conversion

2.7.1 Color to Gray Scale Conversion

For monochrome flat-panel display of what normally would be a color analog video output, a digital equivalent of the RAMDAC function is required to sum color information together into video signals. This function is accomplished through use of a digital equivalent of the DAC function, which takes the RGB color to gray scale weighting color palette RAM outputs and converts them to their digitally weighted monochrome equivalent. Weighting is performed using NTSC standard algorithms, and may be disabled for Monochrome Display Adapter emulation applications.

2.7.2 Gray Scale Mapping

The WD90C26's flat-panel adapter circuitry incorporates an orthogonal 64-word by 64 gray-scale to gray-shade mapping RAM. This mapping RAM serves as a firmware-programmable lookup table that may be configured to map gray scale value from color-to-gray scale conversion into the dithered gray-scale shades best suited to a particular panel model.

Maximum flexibility in 'tuning' the WD90C26 to work with a particular panel model's characteristics is possible via this mapping RAM. Its size also allows finer control when selecting dithering patterns from the 64-shade monochrome dithering circuitry, allowing any monochrome panel to perform to its best in displaying visually accurate gray scales.

Control of gray scale selection is facilitated by the WD OEM User Utility. Please refer to the application note for details.

2.7.3 Gray Shade Dithering

Monochrome gray shade dithering circuitry provides a total of 64 shades of gray on monochrome flat-panel displays. All 64 shades may be simultaneously displayed. Simultaneous display of 64 shades in VGA modes is possible in 256 color modes only.

2.7.4 Color STN Dithering

For color 4-bit interface STN panels, the WD90C26 dithering circuitry supports color display from the full 256K VGA palette.

2.7.5 Color TFT Panel Dithering Circuitry

For Color TFT panels, dithering circuitry supports a total of 27K colors 9-bit interface panels.

2.7.6 Direct 12-bit TFT Panel Support

The WD90C26 drives 12-bit TFT panels with direct undithered color for a palette of 4K colors.

2.7.7 Row Buffering

Monochrome dual-panel displays (most monochrome LCDs) can be directly supported by the WD90C26 due to its capability to internally buffer alternate panel rows.

When simultaneous display on CRT and monochrome dual panel displays is not required, no external frame buffer memory is needed to support a monochrome dual-panel style LCD.

2.7.8 Frame Buffering

The WD90C26 includes a frame buffering capability that allows simultaneous display on a CRT and on a dual-panel monochrome display. This function requires that a 256K by 4 DRAM be attached to the Bank B memory interface.

When simultaneous display is not required, the WD90C26's internal row buffering provides all the required support for a dual-panel display.

2.7.9 Panel Format Conversion

The internal panel format conversion circuit provides the flexibility to reformat color or monochrome panel data into the particular pixel grouping required.

2.8 DISPLAY MEMORY INTERFACE

The display memory interface that maps videomemory DRAM is controlled by two separate external memory buses. These buses allow the accommodation of the changing needs of peformance, support feature, and power conservation. Descriptions of these buses follow.

The Bank A bus is used for interfacing to 8-bit video memory configurations, or as the lower byte 16-bit video memory configurations.

The Bank B bus is used as the frame buffer interface when simultaneous display on a CRT and a dual-panel display is desired.

When simultaneous display with a dual-panel display is not required, the Bank B bus can either be used to access the upper byte of a 16-bit video memory, or shut down to conserve power.

2.9 POWER-DOWN CONTROL

The WD90C26's ability to control power consumption allows it to work successfully in portable applications. Power consumption is managed by the power-down control block, which performs the following functions:

- Turns off clocks to unused portions of the WD90C26
- Provides refresh signals to video memory when normal refresh functions are shut down
- Controls wakeup/sleep cycling
- Reduces chip power during power-down mode
- Sequences chip reset operations

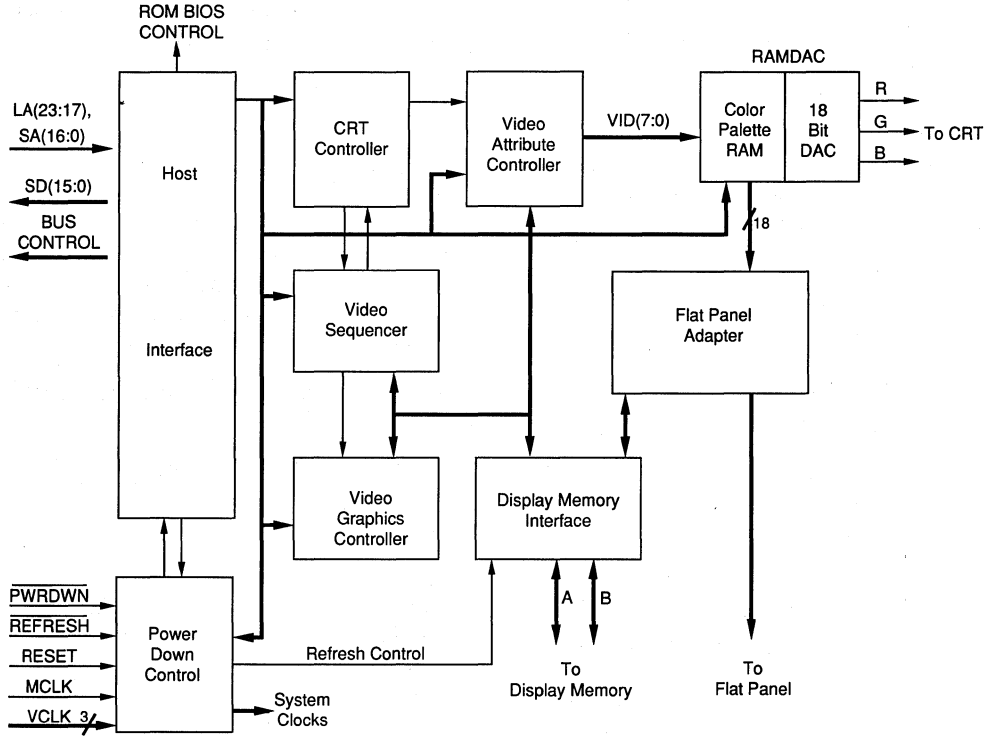


FIGURE 2-1. WD90C26 BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

This section describes the following WD90C26 interfaces:

- System Interface - Allows the WD90C26 to directly interface to ISA bus-based systems or to Micro Channel-based systems
- BIOS Support Interface - Allows the WD90C26 to provide an enable output for external video BIOS memory
- Video Memory Interface - Allows connection of either 2, 3, or 4 256K by 4 DRAMS or one 256K by 16 DRAM
- Video Interface - Alllows direct connection to most PC-compatible CRTs and to a wide range of industry-standard flat-panel types
- Clock Interface - Controls clock oscillators or allows up to four separate frequency inputs
- Power Management Interface - Allows control of chip power consumption

3.2 SYSTEM INTERFACE

The WD90C26 is designed to directly interface to ISA bus based systems or to Micro Channel based systems.

System interface selection is done by pulling high or low a video memory data line at time of chip reset.

For both Micro Channel and ISA Bus operations, the WD90C26 is mapped into the system I/O address space as the standard set of video I/O registers for the particular video system being emulated.

Four extensively indexed registers at locations 3B5h/3D5h and 3C5h and 3CFh are used to control the vast amount of features beyond those of standard VGA operation.

The WD90C26 has a 1-1/2 word write buffer which operates as a 2-cycle write buffer. This allows the WD90C26 to operate with a very high percentage of true zero wait state performance.

The WD90C26 is designed to be a portable computing device where driving a large capacitive bus, such as found in traditional PCs, is not a factor. To reduce power consumption, the WD90C26's system interface has been designed to drive typical loadings found in laptop applications where bus devices are few and closely grouped.

3.2.1 ISA Bus Interface

The WD90C26 interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The WD90C26 supports full 16-bit memory and I/O transfers. Support of 16-bit memory transfers is independent of whether the WD90C26 has an 8-bit or 16-bit video memory path, although increased performance occurs when a 16-bit video memory is available.

The following ISA Bus signals are directly supported by the WD90C26:

LA[23:17]	$\overline{\text{IOW}}$
SA [16:0]	$\overline{\text{MEMCS16}}$
$\overline{\text{BALE}}$	IOCS16
$\overline{\text{SBHE}}$	IOCHRDY
AEN	$\overline{\text{SRDY (OWS)}}$
$\overline{\text{SD[15:0]}}$	REFRESH
$\overline{\text{MEMR}}$	RESET
$\overline{\text{MEMW}}$	IRQ
$\overline{\text{IOR}}$	

LA addresses are latched internal to the WD90C26 by the ALE signal to eliminate bus timing problems in some common system implementations.

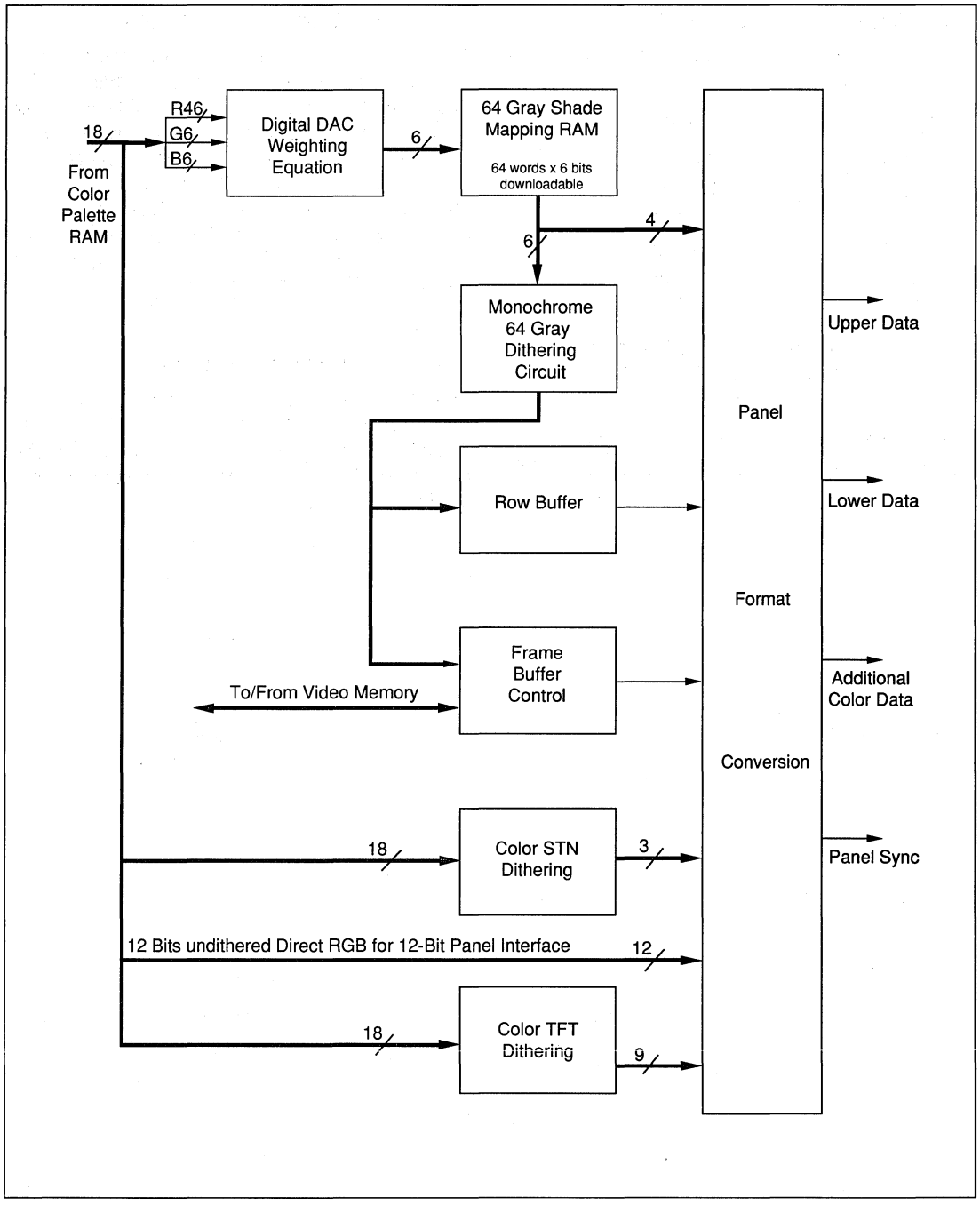


FIGURE 2-2. 90C26 BLOCK DIAGRAM, FLAT PANEL ADAPTER SECTION

3.3 MICROCHANNEL INTERFACE

The WD90C26 directly supports the following Micro Channel interface signals:

A[23:0]	SBHE
ADL	S0
CDSFDBK	S1
M/IO	IRQ
D[15:0]	CDSETUP
CDDS16	CHRESET
CDCHRDY	REFRESH
CMD	MADE24

In addition, the WD90C26 supports both an internal and external decode of I/O address 3C3 bit 0 as a video memory and I/O decode enable.

For full Micro Channel compatibility, only the lower 16 bits of system address bus are decoded for I/O accesses.

3.4 BIOS SUPPORT INTERFACE

The WD90C26 can be configured to provide an enable output for external video BIOS memory. The WD90C26 can support 8- or 16-bit BIOS widths and can be configured to automatically map this external BIOS in to the system memory map at time of reset, and then selectively map it in or out thereafter. Decodes of the 32K of VGA video BIOS address space as defined in the VGA architecture are provided, with an ability to dynamically map out the highest 2K of the 32K space.

3.5 VIDEO MEMORY INTERFACE

The WD90C26 is designed to operate with either 2, 3, or 4 256K by 4 DRAMs or a single 256K by 16 DRAM, with a variety of performance available at each step. The figure on the next page illustrates this implementation.

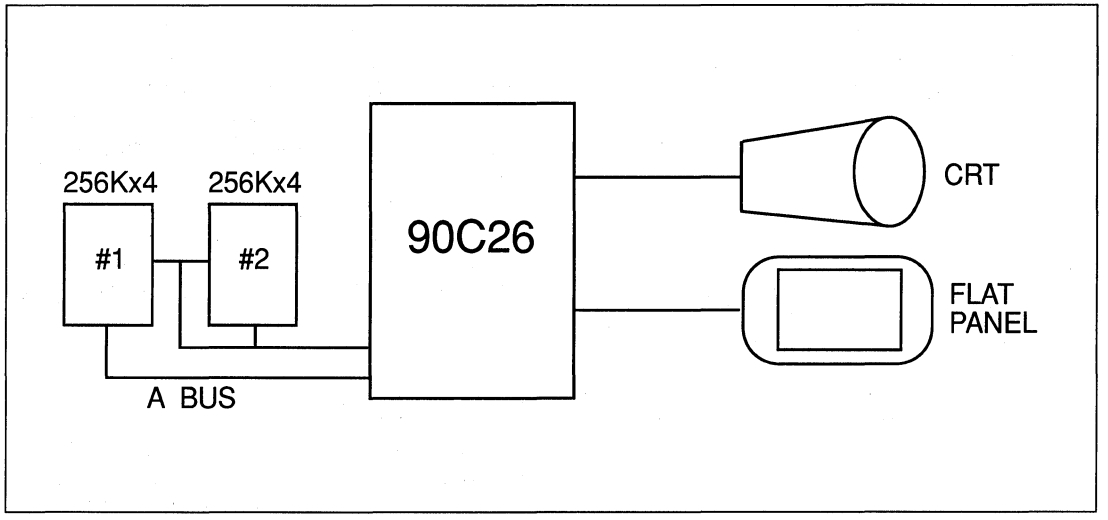


FIGURE 3-1. 2 DRAM IMPLEMENTATION

3.5.1 2 DRAM Implementation

In this implementation, the WD90C26 can support the following:

- simultaneous display on a CRT and any non-dual-panel flat-panel display such as active matrix (TFT), multiplexed (STN) color, plasma, and EL.
- non-simultaneous display with a dual-panel multiplexed (STN) LCD or mono.
- 256 color mode in a 640 by 400 resolution display.

This memory configuration provides for the lowest active power utilization since only two external DRAMs are active. During this time, Bus B memory connections are held static or tri-stated for minimum power dissipation.

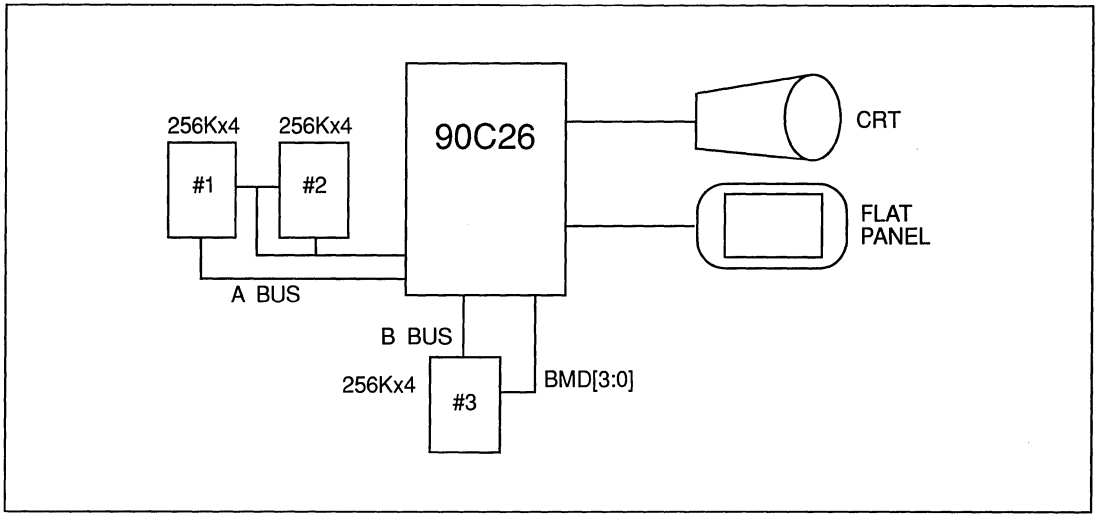


FIGURE 3-2. 3 DRAM IMPLEMENTATION

3.5.2 3 DRAM Implementation

When 3 DRAMs are used, the WD90C26 can additionally support the following:

- simultaneous display of a CRT and a dual-panel multiplexed(STN) LCD display.

The upper nibble of the B bus memory data BMD[7:4] remains tri-stated during the three DRAM mode.

DRAM #3 may be disabled under firmware control when this simultaneous display feature is not needed, allowing power savings when the two displays are not simultaneously connected or when the flat-panel is not a dual-panel type.

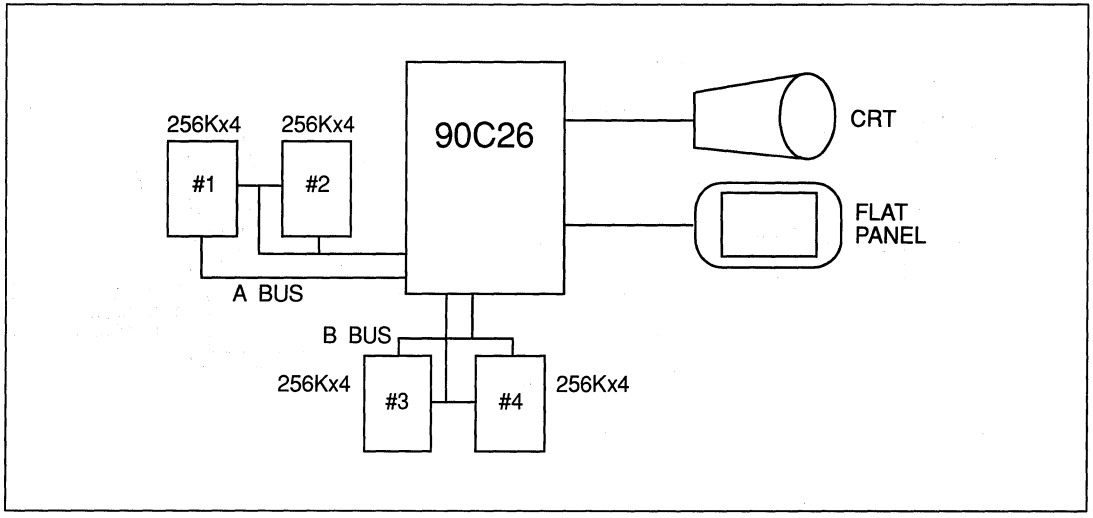


FIGURE 3-3. 4 DRAM IMPLEMENTATION

3.5.3 4 DRAM Implementation

In addition to the features of the 2 DRAM and 3 DRAM modes, the following feature is supported:

- the ability to use 16-bit 512K video RAM except in those occasional times when a dual panel multiplexed display and a CRT are used simultaneously.

Bank B of DRAM may also be disabled by firmware for power reduction, and as before DRAM #3 may be used alone for simultaneous display support of a dual panel display and CRT, while DRAM #4 is disabled.

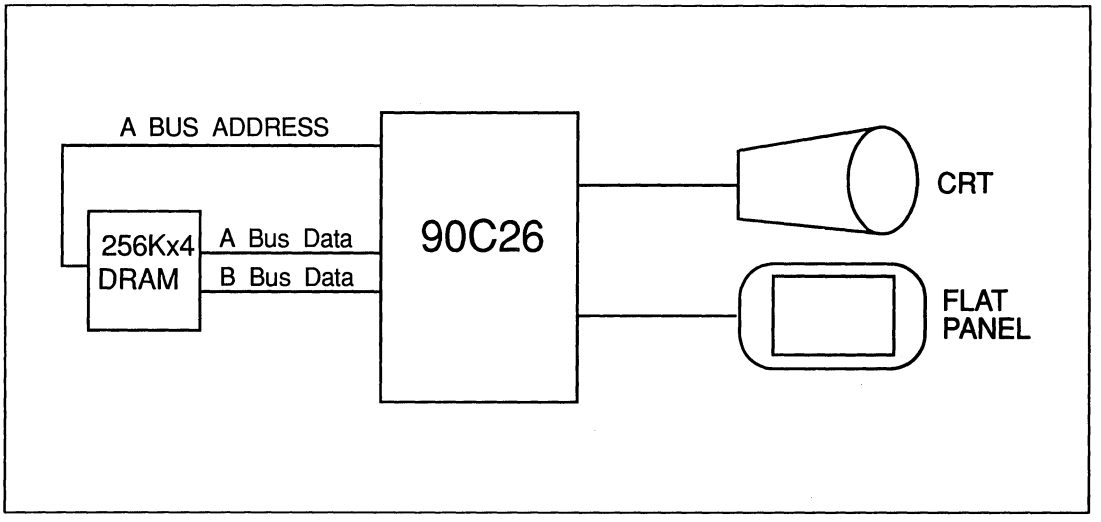


FIGURE 3-4. SINGLE 256K BY 16 IMPLEMENTATION

3.5.4 Single 256K by 16 DRAM Implementation

The WD90C26 may be used with a single 2 CAS 256K by 16 DRAM, providing 512K of video memory and 16-bit memory performance. Simultaneous display operation with all flat-panel types except dual-panel LCD's Is allowed.

3.6 VIDEO INTERFACE

The WD90C26 supports a number of video interfaces allowing it to directly connect to most PC compatible CRTs and to a wide range of industry-standard flat-panel types. This support is achieved through configurable CRT and flat-panel interfaces.

3.6.1 Flat Panel Interface

One of the key features of the WD90C26 is a configurable video output port designed for support of a number of flat-panel technologies. This port is designed to directly support the following flat-panel types without requiring external interface formatting circuitry:

- Monochrome STN multiplexed dual panel LCD displays with one upper panel pixel and one lower panel pixel per clock, one bit per pixel interfaces.
- Monochrome plasma panel displays with one pixel per clock, 4 bits per pixel interfaces.
- Monochrome EL panel displays with one pixel per clock, 4 bits per pixel interfaces.
- Monochrome TFT panel displays with one pixel per clock, 4 bits per pixel interfaces
- Color STN single panel multiplexed LCD displays with one pixel triad per clock, 3 bits per pixel triad (one red, one green, one blue) interfaces.
- Color single panel active matrix TFT LCD displays with one pixel per clock, 3 bits per pixel interfaces.
- Color single panel active matrix TFT LCD displays with one pixel per clock, 4 bits per pixel interfaces.

Programmable flat-panel timing signals allow wide degrees of flexibility in configuring panel interfaces, making the WD90C26 usable with most popular flat-panel designs for PC applications.

For flat panel designs with more unique timing requirements, the WD90C26 is designed to directly interface with the WD90C55 Color Interface Device.

3.6.2 Analog CRT Interface

The WD90C26 includes a complete VGA compatible CRT interface with on-board 256 by 18-bit RAMDAC, which can directly drive analog VGA compatible color or monochrome displays.The interface is also capable of driving older EGA or monochrome compatible displays.

3.6.3 External RAMDAC Interface

For applications where use of an external RAMDAC or equivalent external function is desired, the WD90C26's flat-panel interface can be configured as an industry-standard RAMDAC interface instead of flat-panel pixel data. This allows the WD90C26 to be used in applications where a 24-bit RAMDAC is needed or where special panel pixelization techniques are required.

3.7 CLOCK INTERFACE

The WD90C26 has four clock input signal pins:

- VCLK0
- VCLK1
- VCLK2
- VCLK3

Three of these (VCLK 2, 1, and 0) are normally connected to oscillators. VCLK1 and VCLK2 may be configured to control an external clock multiplexor or clock generator. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 45 MHz for 70nsec DRAMs.

3.8 POWER MANAGEMENT INTERFACE

The WD90C26's power management interface controls power-down mode operations including DRAM refresh modes and four power reduction modes are available providing a range of function and power savings.

4.0 SIGNAL DESCRIPTIONS

4.1 INTRODUCTION

This section contains a pin diagram, a pin table, and a signal description summary for the following groups of pins:

System Interface Pins

EBROM	SD[15:8]
MEMW/S0	MEMR/M/IO
IOCS16/CDSETUP	MEMCS16/CDDS16
SBHE	BALE/MADE24
IRQ/IRQ	IOR/S1
IOW/CMD	AEN/3C3D0
SD[7:0]	OWS/CDSFBK
IOCHRDY/CDCHRDY	LA[19:17]
SA[16:0]	LA22/R3
LA23/BLW1M	LA20/B3
LA21/G3	IRQ/IRQ

Display Buffer Memory Interface Pins

BMA[8:0]	BRAS
BWE	ACAS
AOE	AMA[8:0]
ARAS	BCAS
AWE	BOE

Internal DAC Analog Interface

ANARED	ANAGRN
ANABLU	PNLOFF/WPLT
FSADJ/MDET	VREF/DACDISA

Clock Generation Interface

VCLK0/VCKIN
VCLK1/VCSLD/VCSEL1
MCLK
VCLK2/VCSEL/VCSELH

Panel Interface

HSYNC	VSYNC
FR/BLANK	XSCLK
ENDATA	LP
FP	PNLENA

Power Down Control Pins

PWRDWN	RESET
REFRESH	

Power Pins

VDD	VSS
PVDD	BVDD
AVDD	AVSS
RVDD	RVSS
BVDD	BVSS

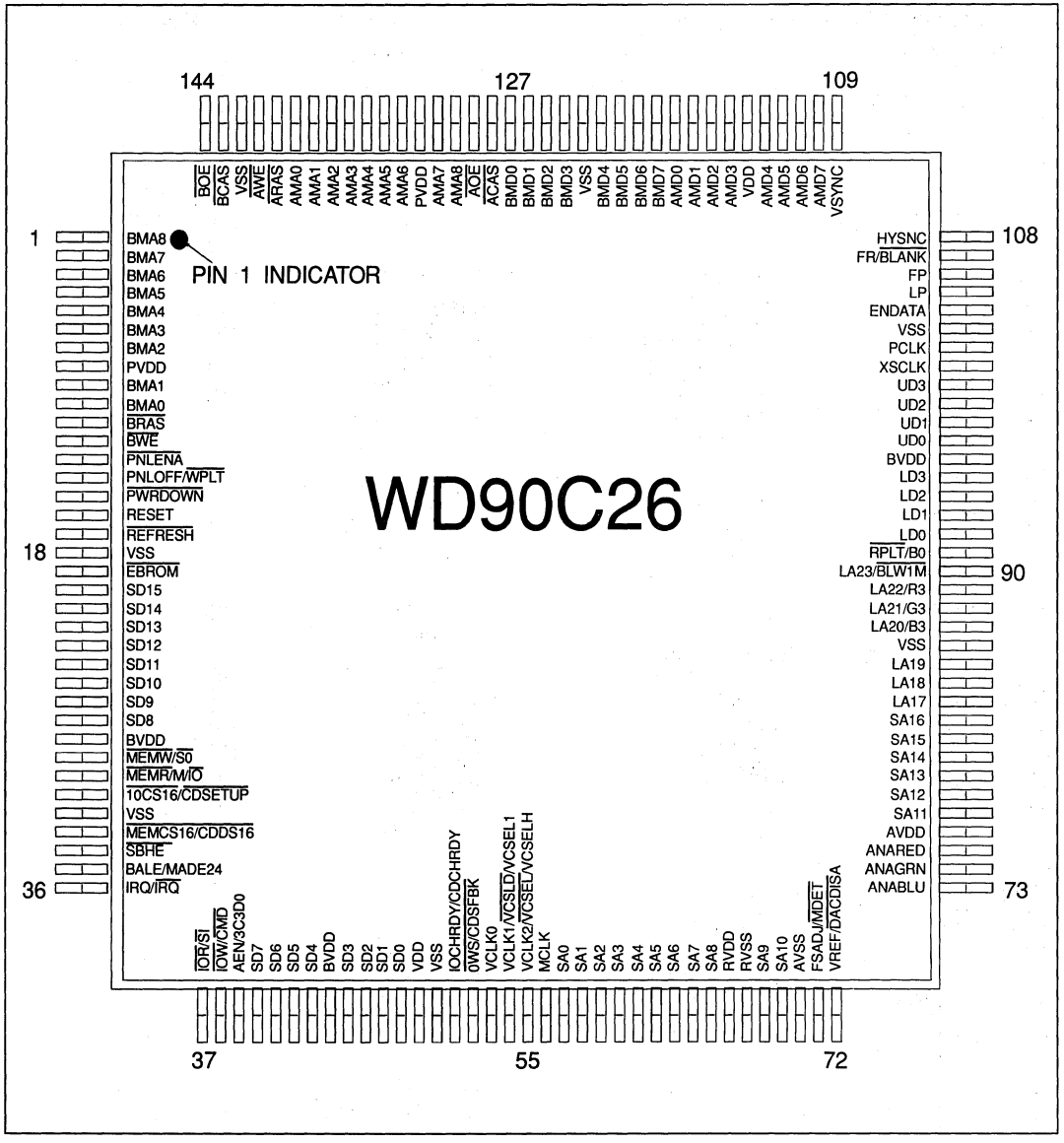


FIGURE 4-1. WD90C26 PIN DIAGRAM, 144-PIN JEDEC PQFP PACKAGE

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - BMA8	38 - IOW/CMD	75 - ANARED	112 - AMD5
2 - BMA7	39 - AEN/3C3D0	76 - AVDD	113 - AMD4
3 - BMA6	40 - SD7	77 - SA11	114 - VDD
4 - BMA5	41 - SD6	78 - SA12	115 - AMD3
5 - BMA4	42 - SD5	79 - SA13	116 - AMD2
6 - BMA3	43 - SD4	80 - SA14	117 - AMD1
7 - BMA2	44 - BVDD	81 - SA15	118 - AMD0
8 - PVDD	45 - SE3	82 - SA16	119 - BMD7
9 - BMA1	46 - SD2	83 - LA17	120 - BMD6
10 - BMA0	47 - SD1	84 - LA18	121 - BMD5
11 - BRAS	48 - SD0	85 - LA19	122 - BMD4
12 - BWE	49 - VDD	86 - VSS	123 - VSS
13 - PNLENA	50 - VSS	87 - LA20/B3	124 - BMD3
14 - PNLOFF/WPLT	51 - IOCHRDY/ CDCHRDY	88 - LA21/G3	125 - BMD2
15 - PWRDOWN	52 - OWS/CDSBFK	89 - LA22/R3	126 - BMD1
16 - RESET	53 - VCLK0	90 - LA23/BLW1M	127 - BMD0
17 - REFRESH	54 - VCLK1/ VCSLD/ VCSEL1	91 - RPLT/B0	128 - ACAS
18 - VSS	55 - VCLK2/ VCEL/ VCSELH	92 - LD0	129 - AOE
19 - EBROM	56 - MCLK	93 - LD1	130 - AMA8
20 - SD15	57 - SA0	94 - LD2	131 - AMA7
21 - SD14	58 - SA1	95 - LD3	132 - PVDD
22 - SD13	59 - SA2	96 - BVDD	133 - AMA6
23 - SD12	60 - SA3	97 - UD0	134 - AMA5
24 - SD11	61 - SA4	98 - UD1	135 - AMA4
25 - SD10	62 - SA5	99 - UD2	136 - AMA3
26 - SD9	63 - SA6	100 - UD3	137 - AMA2
27 - SD8	64 - SA7	101 - XSCLK	138 - AMA1
28 - BVDD	65 - SA8	102 - PCLK	139 - AMA0
29 - MEMW/SO	66 - RVDD	103 - VSS	140 - ARAS
30 - MEMR/M/IO	67 - RVSS	104 - ENDATA	141 - AWE
31 - IOCS16/ CDSETUP	68 - SA9	105 - LP	142 - VSS
32 - VSS	69 - SA10	106 - FP	143 - BCAS
33 - MEMCS16/ CDDS16	70 - AVSS	107 - FR/BLANK	144 - BOE
34 - SBHE	71 - FSADJ/MDET	108 - HSYNC	145 - N/A
35 - BALE/MADE24	72 - VREF/DACDISA	109 - VSYNC	
36 - IRQ/IRQ	73 - ANABLU	110 - AMD7	
37 - IOR/S1	74 - ANAGRN	111 - AMD6	

TABLE 4-1. PIN ASSIGNMENTS

4.2 SYSTEM INTERFACE PINS

The following table describes each System Interface pin on the WD90C26. The WD90C26 system interface can be configured for either ISA bus or Micro Channel interface support by setting DCONF/2 high or low by pulling high or low the AMD2 pin at reset. Other configuration options may also be selected by setting configuration bits high or low at reset through pulling memory data lines high or low.

PIN	MNEMONIC	I/O	DESCRIPTION
16	RESET	I	**WD90C26's Initialization Signal** Typical usage in ISA Bus based system: connected to ISA Bus RESET signal.Typical usage in Micro Channel based system: connected to Micro Channel RESETDRV signal.
17	$\overline{\text{REFRESH}}$	I	**Input Active Low DRAM Refresh** The WD90C26 uses this input to initiate refresh operations to its video buffer memory. It also uses this signal as a negative qualifier for memory read operations.
19	$\overline{\text{EBROM}}$	O	**Enable BIOS ROM** In BIOS ROM Map-in mode, where CONF(0)=0 the WD90C26 drives this output low when it decodes system accesses to video BIOS ROM and a memory read operation is requested from an address range identified within the WD90C26 as a video BIOS ROM address. If CONF(0)=1 this pin remains inactive high.
29	$\overline{\text{MEMW}}$/$\overline{\text{S0}}$	I	**Memory Write** $\overline{\text{MEMW}}$ if CONF(2)=1 (ISA Bus Mode). Memory write input from ISA bus. **Decode MicroChannel Bus Cycles** $\overline{\text{S0}}$ if CONF(2)=0 (Micro Channel Mode). When the WD90C26 is in ISA Bus mode. This pin is the industry standard $\overline{\text{MEMW}}$ bus signal, and indicates to the WD90C26 that a memory write bus cycle is occurring. When the WD90C26 is in Micro Channel mode, this pin is the Micro Channel $\overline{\text{S0}}$ channel status input, which the WD90C26 uses, along with S1, M/$\overline{\text{IO}}$, and $\overline{\text{CMD}}$, to decode Micro Channel bus cycles.

TABLE 4-2. SYSTEM INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
30	MEMR/M/IO	I	**Memory Read** MEMR if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus mode, this pin is the industry-standard MEMR bus signal. This indicates to the WD90C26 that a memory read bus cycle is occurring. Because MEMR may also be active during refresh cycles, the WD90C26 internally gates MEMR with REFRESH. **Memory/IO Cycle** M/IO if CONF(2)=0 (Micro Channel Mode) When the WD90C26 is in Micro Channel mode, this pin is the M/IO signal from the Micro Channel bus. A high input at this pin is interpreted by the WD90C26 as a Micro Channel Bus Memory cycle. A signal at this pin indicates a Micro Channel Bus I/O cycle to the WD90C26.
31	IOCS16/CDSETUP	I/O O.C.	**I/O Chip Select 16** IOCS16 if CONF(2)=1 (ISA Bus Mode). Open collector Indicates the WD90C26 supports 16-bit I/O operations at the "current"I/O address. In ISA Bus mode, pin 31 becoming active low is an indication to the ISA Bus that it supports 20-bit I/O transfers at the 16-bit I/O address being presented to it. Otherwise this pin is in a high-impedance state. IOCS16 is not gated by any other signals. Its function is independent of other bus control lines, bus modes, or register settings. IOCS16 is not affected by AEN. **Card Setup** CDSETUP if CONF(2)=0 (Micro Channel Mode). In Micro Channel mode, this pin is the card setup input indicating to the WD90C26 to perform setup functions.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
33	MEMCS16/ CDDS16	O O.C.	**Memory Chip Select 16** MEMCS16 if CONF(2)=1 (ISA Bus Mode). In ISA bus mode, pin 33 is an indication to the system that the WD90C26 supports 16-bit memory transfers at the system address being presented. In ISA Bus applications, pin 33 is typically connected to the ISA Bus MEMCS16 signal. **Card Data Size 16** CDDS16 if CONF(2)=0 (Micro Channel Mode) In Micro Channel applications pin 33 indicates a 16-bit resource available at the address.
34	SBHE	I	**System Byte Hi Enable** SBHE indicates to the WD90C26 the mapping of bytes into high or low registers on write operations and the ordering of high and low bytes during read operations.
35	BALE/MADE24	I	**Address Latch Enable** BALE if CONF(2)=1 (ISA Bus Mode) Typical usage in ISA Bus based system: connected to ISA Bus BALE signal. When the WD90C26 is in ISA Bus mode this pin is the industry standard BALE signal input to the WD90C26. A high level is interpreted by the WD90C26 as an indication that the system address is setting up on its SA bus inputs to be latched on the falling edge of this signal. To ensure compatibility across a variety of platforms, the WD90C26 latches LA17-LA23 with the fall of BALE. **Memory Address Enable 24** MADE24 if CONF(2)=0 (Micro Channel Mode). When the WD90C26 is in Micro Channel mode, this pin is the Micro Channel MADE24 input to the WD90C26 and is used by the WD90C26 as an indication that the system address is in the below-16 MByte range.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
36	IRQ/$\overline{IRQ}$	O	**Interrupt Request** Active high if CONF(2)=1 (ISA Bus Mode), Active Low if in Micro Channel mode. Open Collector in Micro Channel mode. Description of function of IRQ in both ISA and Micro Channel Modes is as follows: When bit 5 of the VGA Vertical Retrace End Register (I/O Address 3?5h index 11) is set to 0, this signal is set active at the occurrence of the end of vertical display of a frame of active video. IRQ stays active until cleared by momentarily setting bit 4 of the Vertical Retrace End Register to 0 and then back to 1. When bit 5 of the VGA Vertical Retrace End Register is set to 0 the activation of this pin is disabled, forcing its output to be low in ISA bus mode or high impedance in Micro Channel mode. NOTE: This pin can only be configured or the interrupt cleared if the Vertical Retrace End Register is unlocked by setting PR3 bit 0 high.
37	$\overline{IOR}$/$\overline{S1}$	I	**$\overline{I/O}$ Read** $\overline{IOR}$ if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus Mode, this pin indicates to the WD90C26 that an I/O read bus cycle is to occur. $\overline{IOR}$ may also be active during DMA cycles and is therefore internally qualified by AEN. **$\overline{S1}$ Cycle Decode** $\overline{S1}$ if CONF(2)=0(Micro Channel Mode). When the WD90C26 is in Micro Channel mode (AMD2 low at reset), this pin is the Micro Channel $\overline{S1}$ channel status input, which the WD90C26 uses, along with $\overline{S0}$, M/$\overline{IO}$, and $\overline{CMD}$, to decode Micro Channel bus cycles.
38	$\overline{IOW}$/$\overline{CMD}$	I	**$\overline{I/O}$ Write** $\overline{IOW}$ if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus mode, this pin indicates to the WD90C26 that an I/O read bus cycle is to occur. The WD90C26 internally qualifies $\overline{IOW}$ write requests with AEN. **$\overline{Command}$** $\overline{CMD}$ if CONF(2)=0 (Micro Channel Mode) When the WD90C26 is in Micro Channel mode, this pin is interpreted by the WD90C26 as the $\overline{CMD}$ signal from a Micro Channel bus. The WD90C26 uses this signal to properly decode cycle types.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

16

PIN	MNEMONIC	I/O	DESCRIPTION
39	AEN/3C3D0	I	**Address Enable** AEN if CONF(2)=1 (ISA Bus Mode). When active high, this signal disables the WD90C26 from performing ISA bus read or write accesses. When low, system accesses to the WD90C26 are enabled. **Video Subsystem Enable Port, Data Bit 0 Input** 3C3D0 if CONF(2)=0 (Micro Channel Mode). This signal typically comes from bit 0 of I/O port 3C3h. A high input at this pin enables the WD90C26's ability to respond to Micro Channel bus accesses. In Micro Channel mode, I/O writes to the WD90C26 of a '1' to I/O port 3C3 bit 0 also enables the WD90C26.
51	IOCHRDY/ CDCHRDY	O O.C.	**I/O Channel Ready Status** IOCHRDY if CONF(2)=1 (ISA Bus Mode). I/O Channel Ready status when active high. When the WD90C26 is in ISA Bus Mode (see section on configuration bits for description of use of AMD2 as a mode configuration pin), pin 51 is the industry-standard IOCHRDY bus signal, and indicates readiness of the WD90C26 in responding to ISA bus read and write cycles. When the WD90C26 cannot complete the desired bus cycle within the standard or 0 wait cycle times, it will de-assert IOCHRDY until it is ready to complete the transfer. **Channel Ready** CDCHRDY if CONF(2)=1 (Micro Channel Mode). When the WD90C26 is in Micro Channel Mode, CONF(2)=0), pin 51 is the CDCHRDY signal to a Micro Channel bus. The WD90C26 drives this pin low when additional cycle time is required. In Micro Channel mode, CDCHRDY is brought to its high-impedance inactive state by the rising edge of the signal to pin 48, $\overline{CMD}$. Under typical conditions of video memory speeds and bus rates, the WD90C26 does not cause IOCHRDY or CDCHRDY to go inactive low or cause CDCHRDY to occur later than the minimum requirement, except in certain instances when a write operation results in an internal write data buffer overflow.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
52	$\overline{0WS}$ $\overline{CDSFBK}$	O O.C.	**$\overline{Zero}$ Wait State** $\overline{0WS}$ if ISA Bus Mode CONF(2)=1 (ISA Bus Mode). This pin is the WD90C26's indication of readiness to support zero wait state option. The description of PR32 includes information on how to configure the WD90C26's support of $\overline{0WS}$. The WD90C26 drives this signal low when 0 wait cycles can be supported. Otherwise this signal is tri-stated. **$\overline{Card\ Selected}$ Feedback** $\overline{CDSFBK}$ if CONF(2)=1 (Micro Channel Mode). Feedback to the Micro Channel interface of CD status. Driven active low by the WD90C26 as an acknowledgment of its selection. Does not go active if $\overline{CDSETUP}$ is active low. It is tri-stated when not being driven active low.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

4.2.1 System Interface Data Signals

PIN	MNEMONIC	I/O	DESCRIPTION
SD15 is the MSB and SD0 is the LSB of the 16-bit system data bus in ISA bus and Micro Channel bus architectures. The WD90C26's system data signals may be directly connected to the host system data bus, provided the WD90C26 drivers are adequate when host system data bus loading considerations are made. The full data sheet provides specifics about bus drive capabilities.			
20	SD15	I/O	System Data 15
21	SD14	I/O	System Data 14
22	SD13	I/O	System Data 13
23	SD12	I/O	System Data 12
24	SD11	I/O	System Data 11
25	SD10	I/O	System Data 10
26	SD9	I/O	System Data 9
27	SD8	I/O	System Data 8
40	SD7	I/O	System Data 7
41	SD6	I/O	System Data 6
42	SD5	I/O	System Data 5
43	SD4	I/O	System Data 4
45	SD3	I/O	System Data 3
46	SD2	I/O	System Data 2
47	SD1	I/O	System Data 1
48	SD1	I/O	System Data 0

TABLE 4-3. SYSTEM INTERFACE DATA SIGNALS

4.2.2 System Interface Address Signals

PIN	MNEMONIC	I/O	DESCRIPTION
SA9-SA0 are used by the WD90C26 as the I/O address during ISA bus or Micro Channel I/O cycles. SA16-SA0 are used as the lower 17 bits of the WD90C26's 24-bit memory address during ISA bus or Micro Channel memory cycles. SA16 is the MSB and SA0 is the LSB of the 17-bit system address bus.			
57	SA0	I	System Address 0
58	SA1	I	System Address 1
59	SA2	I	System Address 2
60	SA3	I	System Address 3
61	SA4	I	System Address 4
62	SA5	I	System Address 5
63	SA6	I	System Address 6
64	SA7	I	System Address 7
65	SA8	I	System Address 8
68	SA9	I	System Address 9
69	SA10	I	System Address 10
77	SA11	I	System Address 11
78	SA12	I	System Address 12
79	SA13	I	System Address 13
80	SA14	I	System Address 14
81	SA15	I	System Address 15
82	SA16	I	System Address 16
LA19-LA17 are additional latchable system address signals. LA19 is the MSB of the 20 bit below-1-megabyte memory address bus in ISA bus and Micro Channel bus architectures, formed by using LA19-LA17 and SA16-SA0. The WD90C26 uses the resulting memory address, along with either the BLW1M signal or decodes of LA23-LA20, for accesses to its video memory buffer DRAM. In certain other modes, the WD90C26 uses the address formed by LA19-SA0, along with a 1MB block decode from LA23-LA20, to access the WD90C26's DRAM video buffer as above-1-megabyte memory. In ISA bus mode CONF(2)=1), LA19-LA17 are inputs to a transparent latch internal to the WD90C26 that allows LA19-LA17 to propagate in, while BALE is active high. LA19-LA17 are then captured when BALE goes inactive low. In Micro Channel Mode CONF(2)=0), LA19-LA17 are also address inputs.			

TABLE 4-4. SYSTEM INTERFACE ADDRESS SIGNALS

PIN	MNEMONIC	I/O	DESCRIPTION
83	LA17	I	Latchable System Address 17
84	LA18	I	Latchable System Address 18
85	LA19	I	Latchable System Address 19
87	LA20/B3	I/O	**Latchable System Address Bit 20** LA20 if pull-up on MD 7 (Full Decode Mode). Blue MSB for 12-bit panel interface. B3 if pull-down on MD7 and in 12-bit panel mode.
88	LA21/G3	I/O	**Latchable System Address Bit 21** LA21 if pull-up on MD 7 (Full Decode Mode). Green MSB for 12-bit panel interface. G3 if pull-down on MD7 and in 12-bit panel mode.
89	LA22/R3	I/O	**Latchable System Address Bit 22** LA22 if CONF(7)=1 (Full Decode Mode). Red MSB for 12-bit panel interface. R3 if pull-down on MD7 and in 12-bit panel mode.
90	LA23/$\overline{\text{BLW1M}}$	I	**Latchable System Address Bit 23** LA23 if MSB of the 24-bit system address formed by LA(23:17) and SA(16:0). **Below 1 megabyte Address Decode** $\overline{\text{BLWIM}}$ if CONF(7)=1 (12-bit I/F mode). Active low input from external decode indicating that the system address is in the below-1-megabyte address range of 000000h to FFFFFFh.

TABLE 4-4. SYSTEM INTERFACE ADDRESS SIGNALS (Continued)

4.3 DISPLAY BUFFER MEMORY INTERFACE PINS

The display memory interface is designed for connection of up to four 256K by 4 or one 256K by 16 fast-page-mode DRAMs. This section is divided into the following subsections, which provide tables describing the data signals below:

- Bank A Video Memory Data Bus Signals
- Bank B Video Memory Data Bus Signals

4.3.1 Bank A Video Memory Signals

PIN	MNEMONIC	I/O	DESCRIPTION
		BANK A VIDEO MEMORY DATA BITS	
110	AMD7	I/O	Bank A Memory Data Bit 7
111	AMD6	I/O	Bank A Memory Data Bit 6
112	AMD5	I/O	Bank A Memory Data Bit 5
113	AMD4	I/O	Bank A Memory Data Bit 4
115	AMD3	I/O	Bank A Memory Data Bit 3
116	AMD2	I/O	Bank A Memory Data Bit 2
117	AMD1	I/O	Bank A Memory Data Bit 1
118	AMD0	I/O	Bank A Memory Data Bit 0
		BANK A VIDEO MEMORY ADDRESS BITS	
130	AMA8	O	Bank A Memory Address Bit 8
131	AMA7	O	Bank A Memory Address Bit 7
133	AMA6	O	Bank A Memory Address Bit 6
134	AMA5	O	Bank A Memory Address Bit 5
135	AMA4	O	Bank A Memory Address Bit 4
136	AMA3	O	Bank A Memory Address Bit 3
137	AMA2	O	Bank A Memory Address Bit 2
138	AMA1	O	Bank A Memory Address Bit 1
138	AMA0	O	Bank A Memory Address Bit 0
Primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			
128	$\overline{\text{ACAS}}$	O	**CAS Bank A** Column address strobe for video memory buffer DRAM bank A, consisting of 256K by 4 DRAMs #1 and #2. When 256K by 16 DRAM is used, this is the lower CAS strobe output and the BCAS signal is the upper CAS strobe input.
129	$\overline{\text{AOE}}$	O	**Output Enable Bank A** Output Enable control for video memory buffer DRAM bank A. When 256K by 16 DRAM is used, this is the DRAM output enable strobe.

TABLE 4-5. BANK A VIDEO MEMORY SIGNALS

PIN	MNEMONIC	I/O	DESCRIPTION
140	$\overline{\text{ARAS}}$	O	**RAS Bank A** Row address strobe for video memory buffer DRAM banks A, consisting of 256K by 4 DRAMs #1 and #2. When a 256K by 16 DRAM is used, this is the DRAM $\overline{\text{RAS}}$ strobe output.
141	$\overline{\text{AWE}}$	O	**Write Enable Bank A** Write Enable control for video memory buffer DRAM bank A. When a 256K by 16 DRAM is used this is the DRAM write enable output.

TABLE 4-5. BANK A VIDEO MEMORY SIGNALS (Continued)

4.3.2 Bank B Video Memory Signals

PIN	MNEMONIC	I/O	DESCRIPTION
BANK B VIDEO MEMORY DATA BITS			
119	BMD	I/O	Bank B Memory Data Bit 7
120	BMD	I/O	Bank B Memory Data Bit 6
121	BMD	I/O	Bank B Memory Data Bit 5
122	BMD	I/O	Bank B Memory Data Bit 4
124	BMD	I/O	Bank B Memory Data Bit 3
125	BMD	I/O	Bank B Memory Data Bit 2
126	BMD	I/O	Bank B Memory Data Bit 1
127	BMD	I/O	Bank B Memory Data Bit 0
BANK B VIDEO MEMORY ADDRESS BITS			
1	BMA	O	Bank B Memory Address Bit 8
2	BMA	O	Bank B Memory Address Bit 7
3	BMA	O	Bank B Memory Address Bit 6
4	BMA	O	Bank B Memory Address Bit 5
5	BMA	O	Bank B Memory Address Bit 4
6	BMA	O	Bank B Memory Address Bit 3
7	BMA	O	Bank B Memory Address Bit 2
9	BMA	O	Bank B Memory Address Bit 1
10	BMA	O	Bank B Memory Address Bit 0
11	$\overline{\text{BRAS}}$	O	**RAS Bank B** Row address strobe for video memory buffer DRAM bank B, consisting of 256K by 4 DRAM #3 or 256K by 4 DRAMs #3 and #4.
12	$\overline{\text{BWE}}$	O	**Write Enable Bank B** Write Enable control for video memory buffer DRAM bank B.
143	$\overline{\text{BCAS}}$	O	**CAS Bank B** Column address strobe for video memory buffer DRAM bank B, consisting of 256K by 4 DRAM #3 or 256K by 4 DRAMs #3 and #4. When a 256K by 16 DRAM is used, this is the upper $\overline{\text{CAS}}$ strobe output.
144	$\overline{\text{BOE}}$	O	**Output Enable Bank B** Output Enable control for video memory buffer DRAM bank B.

TABLE 4-6. BANK B VIDEO MEMORY SIGNALS

4.4 CRT INTERFACE SIGNALS

Internal DAC analog interface pins are described in the following table.

PIN	MNEMONIC	I/O	DESCRIPTION
75	ANARED	O Analog	CRT Red Drive
74	ANAGRN	O Analog	CRT Green Drive
73	ANABLU	O Analog	CRT Blue Drive
72	VREF/ DACDISA	I	**Attach External Precision Reference Input** VREF if above Vss DAC reference voltage. The input for attachment of an external precision reference used by the WD90C26's internal DAC for regulation purposes. **Disable Internal DAC** DACDISA if tied to Vss. If the internal DAC is not needed to drive a CRT, this input may be grounded to disable the internal DAC.
71	FSADJ/ MDET	I A/D	**DAC Full-Scale Adjustment** FSADJUST if pin 72 is above Vss. **Monitor Detect Input** MDET if pin 72 is tied to Vss. If pin 72 is above Vss, this pin serves as the input for a DAC full-scale current adjust external resistor or potentiometer. If pin 72 is tied to Vss, this pin is a digital input to which may be connected an external monitor detect circuit as part of an external RAMDAC support. A low level at this pin causes bit 4 of the VGA input status register 0, at 3C2h as detection of monitor connection to the VGA subsystem.

TABLE 4-7. DAC ANALOG INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
91	$\overline{\text{RPLT}}$/B0	O	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit. **Blue Data Bit 0** If the WD90C26 has been configured for a 9- or 12-bit color TFT interface, this pin is the low-order blue video data output to a panel. This output is static low if the external panel is not enabled or if the panel is not a color interface. The setting of bit 2 determines whether the WD90C26 is configured for a TFT interface.
108	HSYNC	O	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. This pin is inactive when the WD90C26 is in power-down modes or CRT display is not enabled. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.
109	VSYNC	O	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. This pin is inactive when the WD90C26 is in power-down modes or CRT display is not enabled. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.

TABLE 4-7. DAC ANALOG INTERFACE PINS (Continued)

4.5 CLOCK GENERATION INTERFACE PINS

Clock generation interface pins are described in the following table.

PIN	MNEMONIC	I/O	DESCRIPTION
53	VCLK0/VCLKN	I	**Video Clock 0** VCLK0 if CONF(3)=1. The primary of four possible video clock inputs to the WD90C26. VCLK0 is the main video clock to the WD90C26. **Video Clock Input** VCLKN if CONF(3)=0 If AMD[3] is high while RESET is active, this pin is VCLKN, the video clock input from an external frequency source or multiplexer, whose frequency is controlled by Miscellaneous Write Register bit 2, and depending on PR15 bit 5, bit 3, of the Miscellaneous Write Register. Selection of the video shift clock is internally overridden if MCLK has been selected by the setting of PR15 bit 4.
54	VCLK1/ VCSLD/ VCSELL	I/ O/ O	**Video Clock 1** VCLK1 if f pulldown on AMD[3]. If AMD[3] is low while RESET is active, pin 54 is the VCLK1 signal, VCLK1 is the second of four possible video clock inputs to the WD90C26, which are internally selected to provide video shift clock rates for various screen formats and display types. **Video Clock Select Load** VCSLD if CONF(3)=0. This signal is typically used as a video clock select load control line to an external multiple video frequency source. **Video Clock Select Low** VCSELL if CONF(3)=0 and PR15(5)=1 The lower order signal of VCSELL. VCSELL are outputs used as select lines to an external video clock source multiplexer.

TABLE 4-8. CLOCK GENERATION INTERFACE PIN TABLE

PIN	MNEMONIC	I/O	DESCRIPTION
55	VCLK2/ VCSEL/ VCSELH	I/ O/ O	**Video Clock 2** VCLK2 if CONF(3)=1. The third of four possible video clock inputs to the WD90C26, which are internally selected to provide video shift clock rates for various screen formats and display types. **Video Clock Select** VCSEL if CONF(3)=0 and PR15(5)=0. VCSEL is typically used as a video clock select control link to an external multiple video frequency source. Its output follows the setting of WD90C26 register PR2 bit 1. **Video Clock Select High** VCSELH if CONF(3)=0 and PR15(5)-1. The higher order signal of VCSELH, VCSELL, which are outputs used as select lines to an external video clock source multiplexer.
56	MCLK	I	**Memory Timing Clock Input** This signal is the memory timing clock input to the WD90C26. Its speed dictates video memory access timing and speeds as well as system I/O timing. MCLK may also serve as one of four possible sources of video shift clock.

TABLE 4-8. CLOCK GENERATION INTERFACE PIN TABLE (Continued)

4.6 PANEL INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
13	$\overline{\text{PNLENA}}$	O	**LCD Enable** $\overline{\text{PNLENA}}$ is intended to be used to control the attached panel's power supply.
14	PNLOFF/$\overline{\text{WPLT}}$	O	**Panel Power Off** PNLOFF if PR57 bit 2 is '0'. The Power-Off active high signal to an LCD panel's bias supply circuit. The PNLOFF signal is used as a power enable/disable to a control panel, and is tied to the WD90C26's power management circuitry. The WD90C26 sequences this signal as part of the panel power/power-down procedures designed to protect panel circuitry. A high at this output indicates power-off to the panel and a low power-on. **Write Palette** $\overline{\text{WPLT}}$ if PR57 bit 2 is '1'. If the WD90C26 has been configured for external DAC mode, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
102	PCLK	O	**Pixel Clock** This pin serves as a pixel clock output which may be used to latch pixel data from the WD90C26's video output bus into an external RAMDAC. Pixel data from the WD90C26 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC by the falling edge of PCLK.
107	FR/$\overline{\text{BLANK}}$	O	**Frame Rate Signal** FR if operation in any LCD modes. FR is a free-running clock which is intended to be connected to FR frame rate inputs on some LCD panels. Frequency of its signal is programmable. **Blanking Control Signal** $\overline{\text{BLANK}}$ is the standard analog VGA RAMDAC blanking signal. Output when the WD90C26 is not operating in any ICD modes.

TABLE 4-9. PANEL INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
100 99 98 97	UD3 UD2 UD1 UD0	O	**Upper Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the upper panel data bus. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.
95 94 93 92	LD3 LD2 LD1 LD0	O	**Lower Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the lower panel data bus. In a plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAMDAC.
101	XSCLK	O	**X Driver Shift Clock** In a dual panel interface, this signal is used to shift the upper and lower panel's data into the X-driver.
104	ENDATA	O	**Weight Control Clock** In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "enable video" signal.
106	FP	O	**Frame Pulse** FP is used as an indication to attached panels that a new frame has begun.
105	LP	O	**Latch Pulse** The LP output is intended to be used to latch all the current panel data into the current scan line of the panel.

TABLE 4-9. PANEL INTERFACE PINS (Continued)

4.7 POWER-DOWN CONTROL PINS

PIN	MNEMONIC	I/O	DESCRIPTION
15	PWRDWN	I	**Input Active Low Power Down Control** When active low, this pin causes flat-panel and CRT display update circuitry to halt. PNLENA goes inactive, PNLOFF goes active, and BLANK goes active. The internal RAMDAC's outputs are shut off. Flat-panel and CRT timing signals are halted. Video buffer memory and WD90C26 registers are still accessible when PWRDWN is active.

TABLE 4-10. POWER-DOWN CONTROL PINS

4.8 POWER PINS

PIN	MNEMONIC	I/O	DESCRIPTION
8, 132	PVDD	Power	Power-down section V_{DD} supply.
18, 32, 50, 86, 103, 123, 142	VSS	Ground	Ground V_{SS} = 0V.
28, 44, 90	BVDD	Power	Bus interface V_{DD} supply for system bus, panel, CRT, and clock interfaces.
49, 114	VDD	Power	WD90C26 main V_{DD} supply to core and memory data buses.
66	RVDD	Power	RAM filtered palette V_{DD} supply.
67	RVSS	Ground	RAM palette V_{SS} connection.
70	AVSS	Ground	Internal DAC V_{SS} connection.
77	AVDD	Power	Filtered internal DAC V_{DD} power connection.

TABLE 4-11. POWER PINS

WD90C30

High Performance

Video Controller

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

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ADDITIONAL REFERENCES

IBM Personal Computer Hardware User Guide (IBM # 6322510)
IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
IBM Personal Computer AT Hardware User Guide (IBM # 6280066)
IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
IBM PC Options and Adapters Technical Reference Manual (IBM # 6322509)
IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
Personal Computer Reference Manual (IBM # 6025005)

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1.0 INTRODUCTION

The Western Digital Imaging WD90C30 is a 0.9 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. A major advantage of the WD90C30 is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C30 supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C30 also supports 132-column text mode and 6-16 pixel fonts.

This data book supplies a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information, and associated references.

1.1 FEATURES

- Provides single chip video graphics solution for IBM PC, XT, AT, and PS/2 compatible systems.
- Supports two, four or eight 64 Kbyte by 16 DRAMs; four or eight 256 Kbyte by 4 DRAMs; and one or two 256 Kbyte by 16 DRAMs.
- Pin compatible with the WD90C31.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
- Supports all IBM VGA modes with two 64K by 16 DRAMs or only one 256K by 16 DRAM.
- With more DRAMS installed it can support 256 colors at the following resolutions: 640 by 400, 640 by 480, 800 by 600, and 1024 by 768.
- Supports 132-column text.
- Write buffer for zero wait state CPU write performance.
- 8-bit or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate.
- Up to 50 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6-16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC, and overscan registers.
- Special CRTC shadow registers for support of non-standard monitors.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- 132-pin JEDEC (Joint Electronic Device Engineering Council) PQFP (Plastic Quad Flat Package).
- 144-pin EIAJ (Electrical Industry Association of Japan) PQPF.
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for PC/XT/AT, and Micro Channel with minimum external component support.
- Programmable memory mapping register to map WD90C30 into any CPU memory address space.
- Eight-bit CPU address offset register to support 1 Mbyte memory segmentation.

2.0 WD90C30 ARCHITECTURE

The WD90C30 contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C30 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

An internal four-level write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode. The sequencer arbitrates between video display refresh, memory refresh and CPU access of the video memory. The sequencer also provides write buffer control.

The Graphics Controller manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles.

The Attribute Controller serializes the video memory data into video data stream, according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.

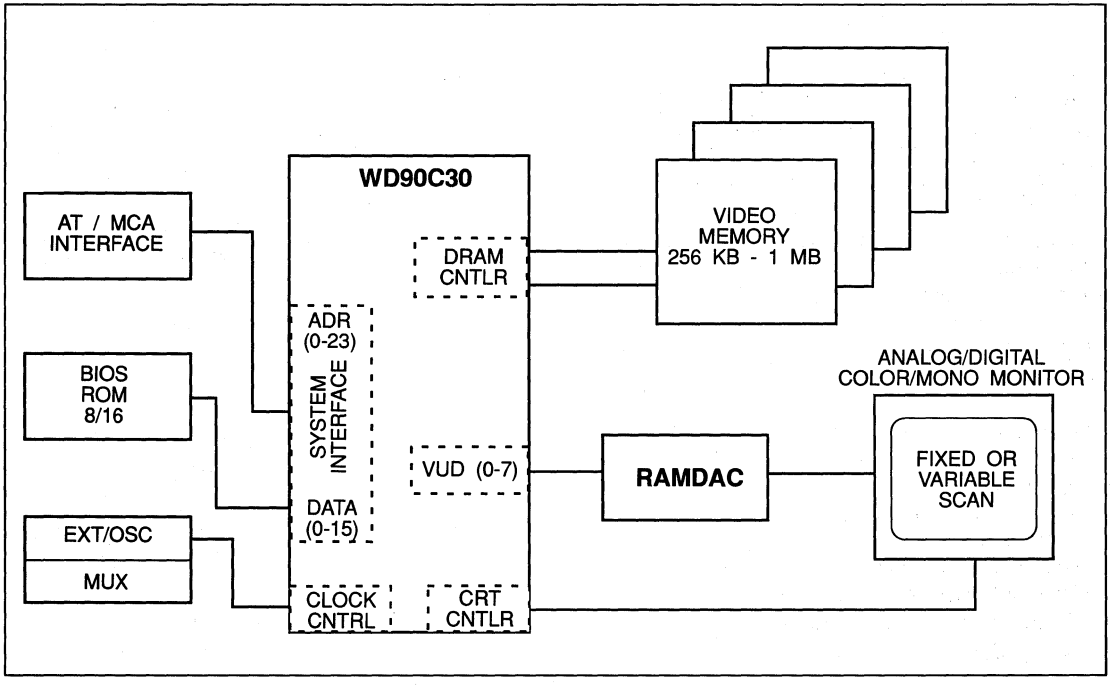

FIGURE 1. SYSTEM BLOCK DIAGRAM

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3.0 WD90C30 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C30 is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C30 Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C30 operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C30 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8-bit or 16-bit data path modes. WD90C30 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM.

The I/O data path can be programmed to be either 16-bit or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C30.

The WD90C30 has a display memory write buffer which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C30 provides the necessary wait states for CPU accesses to the video memory, if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT (or 03C3H for Micro Channel) for setup, and 102H for VGA enable, have been implemented internally in the WD90C30.

3.2 DRAM INTERFACE

The WD90C30 has a very flexible DRAM interface. It can work with two, four, or eight 64Kbyte by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs and one 256 Kbyte by 16 DRAM with a 16-bit memory interface. Other possible configurations are eight 256 Kbyte by 4 DRAMS or two 256Kbyte by 16 DRAMS with a 32-bit memory interface. In all cases the WD90C30 uses the DRAM fast page mode to optimize performance.

The WD90C30 can support all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has internal write buffer, the WD90C30 can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed, the WD90C30 is capable of supporting high resolution video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C30 is designed to support DRAM (60 ns, 70 ns, 80 ns, and 100 ns) with the dedicated MCLOCK which can operate from 32 MHz to 50 MHz maximum.

The WD90C30 generates fast page DRAM timing for all the CPU accesses, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes).

The WD90C30 also generates CAS before RAS DRAM refresh for the display memory.

3.3 VIDEO INTERFACE

The WD90C30 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C30 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and

depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C30 can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C30. The WD90C30 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C30 has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock.

3.5 WD90C30 POWER-UP CONFIGURATION

The WD90C30 uses the memory data pins to configure an internal configuration register upon power-up-reset. CNF(2) determines whether the WD90C30 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C30 at power-up-reset are used as status bits or for clock source control. For more information on WD90C30 power-up configuration, refer to Section 7.10, Configuration Bits.

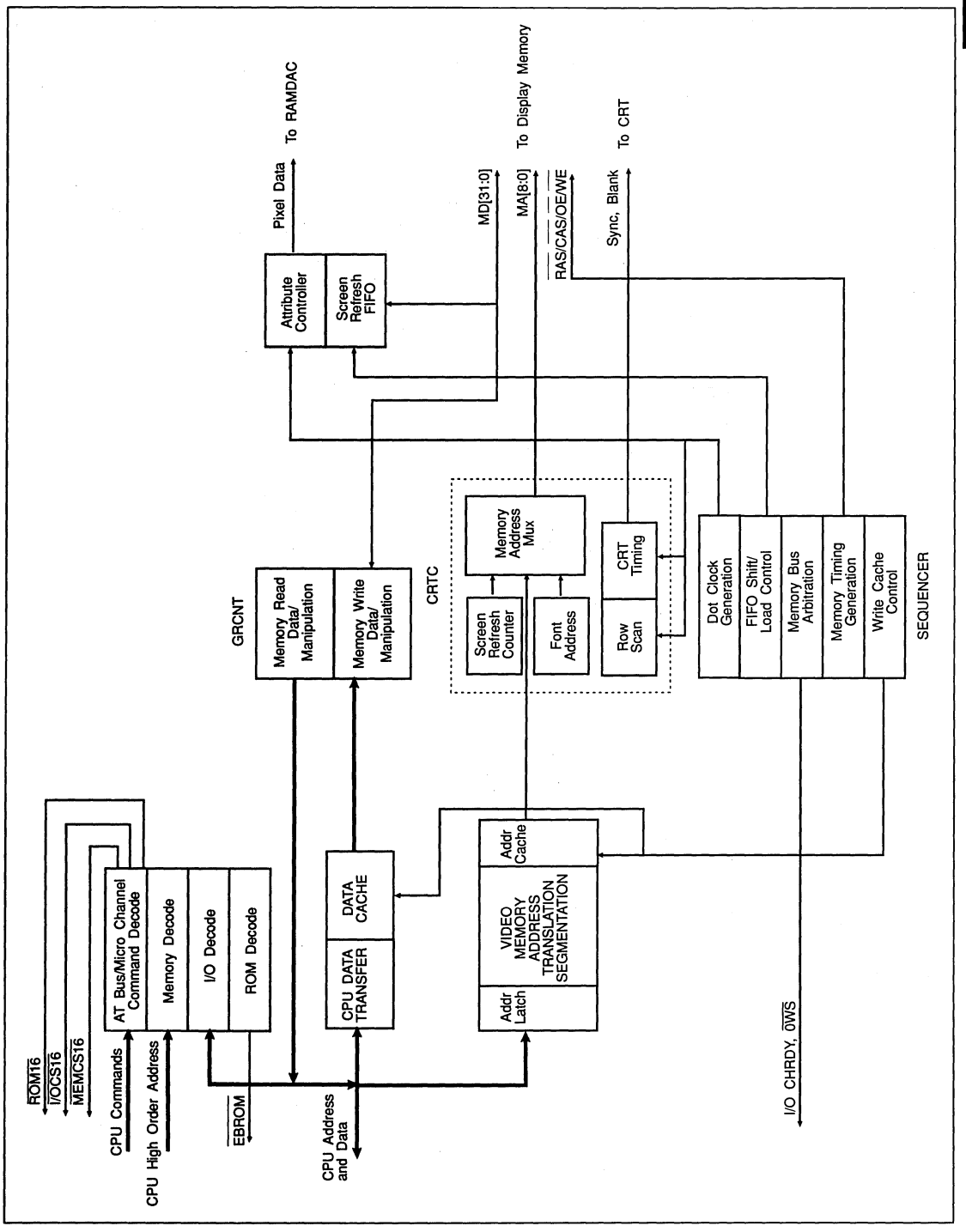

FIGURE 2. WD90C30 BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTION

Table 1 provides a list of pin assignments for the 132-pin JEDEC package. Table 2 provides a list of pin assignments for the 144-pin EIAJ package. Table 3 provides a description of the signals controlled by the WD90C30, and both the JEDEC and EIAJ pins are identified. The WD90C30 mnemonics are used.

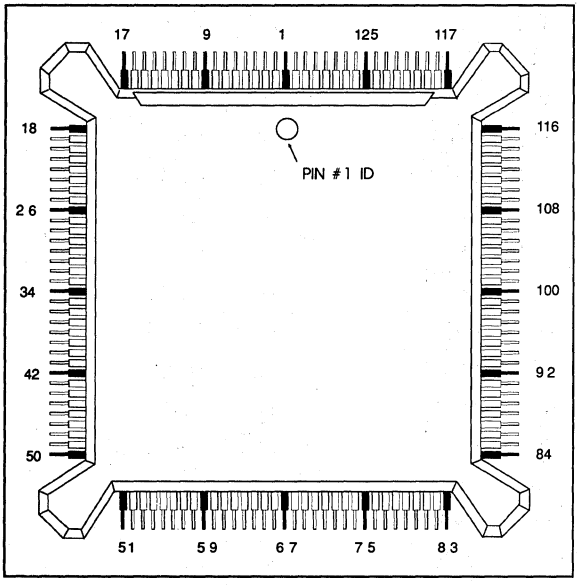

FIGURE 3. 132-PIN JEDEC PACKAGE

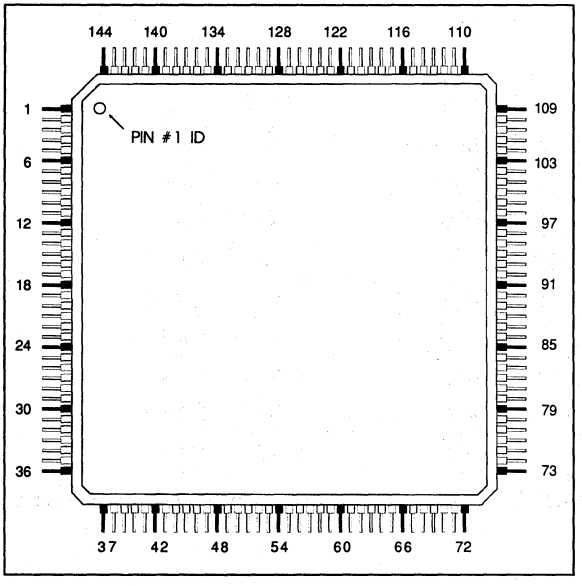

FIGURE 4. 144-PIN EIAJ PACKAGE

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PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	MDET	34	MD12	67	VSS	100	DIR
2	USR1	35	MD11	68	A22	101	DA7
3	USR0	36	MD10	69	A23	102	DA6
4	MCLK	37	MD9	70	$\overline{\text{IOCS16}}$	103	DA5
5	VSS	38	MD8	71	$\overline{\text{MEMCS16}}$	104	DA4
6	$\overline{\text{OE}}$	39	$\overline{\text{RAS}}$	72	$\overline{\text{BHE}}$	105	DA3
7	$\overline{\text{WE3}}$	40	VSS	73	ALE	106	DA2
8	MD31	41	$\overline{\text{CAS}}$	74	IRQ	107	DA1
9	MD30	42	MD7	75	EMEM	108	DA0
10	MD29	43	MD6	76	$\overline{\text{IOR}}$	109	$\overline{\text{EDBUFL}}$
11	MD28	44	MD5	77	$\overline{\text{IOW}}$	110	VSYNC
12	MD27	45	MD4	78	$\overline{\text{MRD}}$	111	HSYNC
13	MD26	46	MD3	79	$\overline{\text{MWR}}$	112	$\overline{\text{BLANK}}$
14	MD25	47	MD2	80	RESET	113	$\overline{\text{HTL}}$
15	MD24	48	MD1	81	$\overline{\text{0WS}}$	114	$\overline{\text{WPLT}}$
16	$\overline{\text{WE2}}$	49	MD0	82	IOCHRDY	115	$\overline{\text{RPLT}}$
17	VSS	50	VCC	83	VSS	116	VCC
18	VCC	51	VSS	84	VCC	117	VSS
19	MD23	52	$\overline{\text{WE0}}$	85	$\overline{\text{EIO}}$	118	PCLK
20	MD22	53	MA0	86	$\overline{\text{ROM16}}$	119	VID0
21	MD21	54	MA1	87	$\overline{\text{EBROM}}$	120	VID1
22	MD20	55	MA2	88	$\overline{\text{EDBUFH}}$	121	VID2
23	MD19	56	MA3	89	A16	122	VID3
24	MD18	57	MA4	90	DA15	123	VID4
25	MD17	58	MA5	91	DA14	124	VID5
26	MD16	59	MA6	92	DA13	125	VID6
27	$\overline{\text{RAS4}}$	60	MA7	93	DA12	126	VID7
28	$\overline{\text{RAS3}}$	61	MA8	94	DA11	127	VSS
29	VSS	62	A17	95	DA10	128	VCLK0
30	$\overline{\text{WE1}}$	63	A18	96	DA9	129	VCLK1
31	MD15	64	A19	97	DA8	130	VCLK2
32	MD14	65	A20	98	$\overline{\text{EABUF}}$	131	$\overline{\text{EXPCLK}}$
33	MD13	66	A21	99	VSS	132	$\overline{\text{EXVID}}$

TABLE 1. WD90C30 132-PIN JEDEC ASSIGNMENTS

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	N.C.	37	N.C.	73	N.C.	109	N.C.
2	VCC	38	VSS	74	VCC	110	VSS
3	MD23	39	$\overline{WE0}$	75	$\overline{EIO}$	111	PCLK
4	MD22	40	MA0	76	$\overline{ROM16}$	112	VID0
5	MD21	41	MA1	77	$\overline{EBROM}$	113	VID1
6	MD20	42	MA2	78	$\overline{EDBUFH}$	114	VID2
7	MD19	43	MA3	79	A16	115	VID3
8	MD18	44	MA4	80	DA15	116	VID4
9	MD17	45	MA5	81	DA14	117	VID5
10	MD16	46	MA6	82	DA13	118	VID6
11	$\overline{RAS4}$	47	MA7	83	DA12	119	VID7
12	$\overline{RAS3}$	48	MA8	84	DA11	120	VSS
13	VSS	49	A17	85	DA10	121	VCLK0
14	$\overline{WE1}$	50	A18	86	DA9	122	VCLK1
15	MD15	51	A19	87	DA8	123	VCLK2
16	MD14	52	A20	88	$\overline{EABUF}$	124	$\overline{EXPCLK}$
17	MD13	53	A21	89	VSS	125	$\overline{EXVID}$
18	N.C.	54	N.C.	90	N.C.	126	N.C.
19	MD12	55	VSS	91	DIR	127	MDET
20	MD11	56	A22	92	DA7	128	USR1
21	MD10	57	A23	93	DA6	129	USR0
22	MD9	58	$\overline{IOCS16}$	94	DA5	130	MCLK
23	MD8	59	$\overline{MEMCS16}$	95	DA4	131	VSS
24	RAS	60	$\overline{BHE}$	96	DA3	132	$\overline{OE}$
25	VSS	61	ALE	97	DA2	133	$\overline{WE3}$
26	$\overline{CAS}$	62	IRQ	98	DA1	134	MD31
27	MD7	63	EMEM	99	DA0	135	MD30
28	MD6	64	$\overline{IOR}$	100	$\overline{EDBUFL}$	136	MD29
29	MD5	65	$\overline{IOW}$	101	VSYNC	137	MD28
30	MD4	66	$\overline{MRD}$	102	HSYNC	138	MD27
31	MD3	67	$\overline{MWR}$	103	$\overline{BLANK}$	139	MD26
32	MD2	68	RESET	104	$\overline{HTL}$	140	MD25
33	MD1	69	$\overline{OWS}$	105	$\overline{WPLT}$	141	MD24
34	MD0	70	IOCHRDY	106	$\overline{RPLT}$	142	$\overline{WE2}$
35	VCC	71	VSS	107	VCC	143	VSS
36	N.C.	72	N.C.	108	N.C.	144	N.C.

TABLE 2. WD90C30 144-PIN EIAJ ASSIGNMENTS

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
POWER ON			
80 - 68	RESET	I	**RESET:** This signal input resets the WD90C30. MCLK and VCLK0 should be connected to WD90C30 in order for the WD90C30 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
CLOCK SELECTION			
4 - 130	MCLK	I	**MEMORY CLOCK:** This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
128 - 121	VCLK0	I	**VIDEO CLOCK 0:** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
129 - 122	VCLK1	I/O	**VIDEO CLOCK 1:** This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on Pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, Bit 2). Refer to the Configuration Register and PR15 Register, Bit 5 description.
130 - 123	VCLK2	I/O	**VIDEO CLOCK 2:** A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of Bit PR2(1) (or it reflects the contents of 03C2H, Miscellaneous Register, Bit 3) if CNF(3) is set to "1". See the Configuration Register and PR15 Register, Bit 5 description.

TABLE 3. SIGNAL DESCRIPTION

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
HOST INTERFACE			
69 - 57 68 - 56 66 - 53 65 - 52 64 - 51 63 - 50 62 - 49	A23 A22 A21 A20 A19 A18 A17	I I I I I I I	**ADDRESS BUS (A23 - A17):** These address bits should be connected to address bus SA23 - 17 in Micro Channel mode. In AT mode A23-17 should be connected to A23-17 of the AT address bus.
89 - 79	A16	I	**ADDRESS BUS (A16):** Bit SA16 of CPU address bus
73 - 61	ALE	I	**ADDRESS LATCH ENABLE:** In AT mode, A23-17 are latched internally at the falling edge of the ALE. In Micro Channel mode, ALE should not be used and should be connected to VSS.
90 - 80 91 - 81 92 - 82 93 - 83 94 - 84 95 - 85 96 - 86 97 - 87 101 - 92 102 - 93 103 - 94 104 - 95 105 - 96 106 - 97 107 - 98 108 - 99	DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**ADDRESS /DATA BUS:** This is the multiplexed CPU address and data bus. $\overline{EABUF}$ = 0: Enables the external address buffer. $\overline{EDBUFL}$ = 0 or $\overline{EDBUFH}$ = 0: Enables the external bi-directional data buffers. DIR controls the data flow for the data buffer.
82 - 70	IOCHRDY	O	**READY**: This active high output signal indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C30 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.

TABLE 3. SIGNAL DESCRIPTION (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
74 - 62	IRQ/(IRQ)	O	**INTERRUPT REQUEST:** Programmable processor interrupt request. It is enabled via Bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will be active, causing the interrupt. It will stay active until CRTC11 Bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. IRQ is used to generate interrupt, usually in the Micro Channel mode.
71 - 59	MEMCS16/ (CDDS16)	O	**MEMORY CHIP SELECT 16 BITS:** In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
85 - 75	EIO (3C3D0)	I	**ENABLE I/O:** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line comes from I/O port 3C3H Bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
87 - 77	EBROM	O	**ENABLE BIOS ROM:** This is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A write to WD90C30 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
113 - 104	HTL	O	**ENABLE HIGH-TO-LOW:** (for 16-bit BIOS) If only an eight-bit CPU interface is used, this output enables a data buffer to allow reading of the upper byte of ROM data on the lower data bus when two ROMs (16-bit) are supported.
75 - 63	EMEM	I	**ENABLE MEMORY:** This signal enables memory decoding when high. It is normally connected to the Refresh signal.
72 - 60	BHE	I	**BYTE HIGH ENABLE:** BHE should be connected to BHE of the AT or Micro Channel bus. BHE, SA0 = 00 - Word transfer = 01 - High byte transfer = 10 - Low byte transfer = 11 - Illegal

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
81 - 69	$\overline{0WS}$	O	**ZERO WAIT STATE:** This active low signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33 register, bits 7 and 6 in the following ways: $\overline{0WS}$ = 0 if write cache is not full. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full. In this case $\overline{0WS}$ = 0 should be ANDed externally with $\overline{MWR}$ to generate zero wait state strobe. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full AND $\overline{MWR}$ is active. $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full and $\overline{MWR}$ is active; OR if valid I/O address decode and $\overline{IOW}$ is active.
78 - 66	$\overline{MRD}$/(M/$\overline{IO}$)	I	**MEMORY READ:** In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
79 - 67	$\overline{MWR}$/($\overline{S0}$)	I	**MEMORY WRITE:** The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
76 - 64	$\overline{IOR}$/($\overline{S1}$)	I	**I/O READ:** Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
77 - 65	$\overline{IOW}$/($\overline{CMD}$)	I	**I/O WRITE:** Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$. Address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
70 - 58	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	**I/O CHIP SELECT 16 BITS:** In AT mode, this signal is used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, this signal is driven by the host to individually select channel connector slots during system configuration.

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
100 - 91	DIR	O	**DIRECTION CONTROL:** Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C30 will then drive DIR high to change the direction of the data buffers.
88 - 78	$\overline{\text{EDBUFH}}$	O	**ENABLE DATA BUFFER HIGH:** Active low signal that allows control of an external data buffer for data bits D8 through D15.
109 - 100	$\overline{\text{EDBUFL}}$	O	**ENABLE DATA BUFFER LOW:** Active low signal that allows control of an external data buffer for data bits D0 through D7.
98 - 88	$\overline{\text{EABUF}}$	O	**ENABLE ADDRESS BUFFER:** Active low signal that allows control of an external address buffer.
86 - 76	$\overline{\text{ROM16}}$/($\overline{\text{CSFB}}$)/ $\overline{\text{EXBLANK}}$	I/O	**BIOS ROM SELECT 16 BITS:** (AT Mode) Active low output. This signal decodes the ROM address LA(23-17) for space 0C0000 - 0DFFFF. It may be combined with SA15 and SA16 externally to control $\overline{\text{MCS16}}$ for the address space C0000 - C7FFF. If CNF(17) is set to 0 at power up reset, the ROM16 address decoding is disabled. ROM16 then reflects the status of PR1_1 bit. **CARD SELECT FEEDBACK:** (Micro Channel mode) Active low output. This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. **EXTERNAL BLANK:** (AT or Micro Channel Mode) If CNF (18) is set to zero (MD18 = 0 at power-up reset), this signal becomes an active low input. $\overline{\text{EXBLANK}}$ = 1: enables BLANK, VSYNC, and HSYNC output. $\overline{\text{EXBLANK}}$ = 0: tri-state BLANK, VSYNC, and HSYNC output.

TABLE 3. SIGNAL DESCRIPTION (Continued)

NOTE:
( ) Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
DISPLAY MEMORY INTERFACE			
41 - 26	$\overline{CAS}$	O	**COLUMN ADDRESS STROBE:** Active low CAS output signal (for both two, four and eight DRAM configurations).
39 - 24	$\overline{RAS}$	O	**ROW ADDRESS STROBE:** This active low RAS output signal is the strobe for the 256 Kbyte by 4 or 256 Kbyte by 16 DRAM interface. If 64 Kbyte by 16 DRAMS are used, then this signal is the RAS strobe for the first 256 Kbyte memory bank.
28 - 12	$\overline{RAS3}$	O	**ROW ADDRESS STROBE:** This active low RAS strobe is used only if eight 64 Kbyte by 16 DRAMs are used. It controls the third 256 Kbyte memory bank.
27 - 11	$\overline{RAS4}$	O	**ROW ADDRESS STROBE:** This active low RAS strobe is used only if eight 64 Kbyte by 16 DRAMs are used. It controls the fourth 256 Kbyte memory bank.
6 - 132	$\overline{OE}$	O	**OUTPUT ENABLE:** Active low DRAM output enable signal (for both two, four and eight DRAM configurations).
52 - 39	$\overline{WE0}$	O	**WRITE ENABLE:** Active low write enable signal for MD7 through 0.
30 - 14	$\overline{WE1}$	O	**WRITE ENABLE:** Active low write enable signal for MD15 through 8.
16 - 142	$\overline{WE2}$	O	**WRITE ENABLE:** Active low write enable signal for MD23 through 16.
7 - 133	$\overline{WE3}$	O	**WRITE ENABLE:** Active low write enable signal for MD31 through 24.
PROGRAMMABLE OUTPUTS			
3 - 129	USR0	O	May be used to control special card or system features (see PR32 register).
2 - 128	USR1	O	May be used to control special card or system features (see PR32 register).

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
VIDEO MEMORY DATA			
31 - 15	MD15	I/O	**DISPLAY MEMORY DATA (MD15 through 0):** These lines are the data bus to the video display DRAMS. The MD0-18 data lines are pulled up by internal 50K ohm resistors or may be pulled down by external 4.7 Kohm resistors to provide setup information on power-up (reset) as follows:
32 - 16	MD14	I/O	
33 - 17	MD13	I/O	
34 - 19	MD12	I/O	
35 - 20	MD11	I/O	
36 - 21	MD10	I/O	
37 - 22	MD9	I/O	
38 - 23	MD8	I/O	**MD — POWER-UP FUNCTION — REGISTER (BIT)**
42 - 27	MD7	I/O	
43 - 28	MD6	I/O	18 Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ — CNF(18)+
44 - 29	MD5	I/O	
45 - 30	MD4	I/O	16 64K by 16 or 256K by 4 DRAM Select — CNF(16)+
46 - 31	MD3	I/O	
47 - 32	MD2	I/O	15 EGA SW4/General Purpose — PR11 (7) +
48 - 33	MD1	I/O	14 EGA SW3/General Purpose — PR11 (6)+
49 - 34	MD0	I/O	13 EGA SW2/General Purpose — PR11 (5) +
8 - 134	MD31	I/O	12 EGA SW1/General Purpose — PR11 (4) +
9 - 135	MD30	I/O	11 ANALOG/TTL Display — CNF(8) *
10 - 136	MD29	I/O	10 Set 16-bit ROM — [CNF(10)]*
11 - 137	MD28	I/O	9 3C3H or 46E8H I/O port for wake up — [CNF(9)] +
12 - 138	MD27	I/O	
13 - 139	MD26	I/O	8 A23-A20 connection — [CNF(11)]+
14 - 140	MD25	I/O	7 General Purpose — CNF(7) *
15 - 141	MD24	I/O	6 General Purpose — CNF(6) *
19 - 3	MD23	I/O	5 General Purpose — CNF(5) *
20 - 4	MD22	I/O	4 General Purpose — CNF(4) *
21 - 5	MD21	I/O	3 VCLK1,2 I/O — CNF(3) +
22 - 6	MD20	I/O	2 AT/Micro Channel Mode — CNF(2)+
23 - 7	MD19	I/O	1 1 or 2 ROMs — CNF(1) *
24 - 8	MD18	I/O	0 BIOS ROM Mapping — PR1(0) *
25 - 9	MD17	I/O	NOTES:
26 - 10	MD16	I/O	"*" Pulldown resistor sets these bits to logic 1. "+" Pulldown resistor sets these bits to logic 0. For more details refer to PR and Configuration Registers.

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
VIDEO MEMORY ADDRESS			
61 - 48 60 - 47 59 - 46 58 - 45 57 - 44 56 - 43 55 - 42 54 - 41 53 - 40	MA8/$\overline{RAS2}$ MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	**MEMORY ADDRESS (MA0 through MA8):** Display memory DRAM address. For testing purposes, these pins can be tri-stated by setting Register PR4(4)=1. MA8/$\overline{RAS2}$ is an active low RAS strobe for the second 256 Kbyte memory bank if four 64K by 16 DRAMs are used.
RAMDAC INTERFACE			
126 - 119 125 - 118 124 - 117 123 - 116 122 - 115 121 - 114 120 - 113 119 - 112	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	O O O O O O O O	**VIDEO (VD0-VD7):** Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
115 - 106	$\overline{RPLT}$	O	**READ PALETTE:** Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
114 - 105	$\overline{WPLT}$	O	**WRITE PALETTE:** Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H through 3C9H.
118 - 111	PCLK	O	**PIXEL CLOCK:** Video pixel clock output used by the DAC to latch video signals VID0 through 7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output Register.
CRT CONTROL			
112 - 103	$\overline{BLANK}$	O	**BLANK:** Active low display monitor blank pulse to external RAMDAC.
111 - 102	HSYNC	O	**HORIZONTAL SYNC:** Display monitor horizontal synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
110 - 101	VSYNC	O	**VERTICAL SYNC:** Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	TYPE	DESCRIPTION
1 - 127	MDET	I	**MONITOR DETECT:** This pin is used when the RAM-DAC is external. It is used to determine the monitor type and can be read at port 3C2H Bit 4.
FEATURE CONNECTOR SUPPORT			
132 - 125	$\overline{\text{EXVID}}$	I	**ENABLE EXTERNAL VIDEO DATA:** A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided.
131 - 124	$\overline{\text{EXPCLK}}$	I	**ENABLE EXTERNAL PIXEL CLOCK:** A Feature Connector input. A low tri-states the PCLK output. An internal pullup resistor is provided.
POWER AND GROUND			
18 - 2	VCC	-----	+5VDC
50 - 35	VCC	-----	+5VDC
84 - 74	VCC	-----	+5VDC
116 - 107	VCC	-----	+5VDC
5 - 13	VSS	-----	Ground
17 - 25	VSS	-----	Ground
29 - 38	VSS	-----	Ground
40 - 55	VSS	-----	Ground
51 - 71	VSS	-----	Ground
67 - 89	VSS	-----	Ground
83 - 110	VSS	-----	Ground
99 - 120	VSS	-----	Ground
117 - 131	VSS	-----	Ground
127 - 143	VSS	-----	Ground
- 1 - 18 - 36 - 37 - 54 - 72 - 73 - 90 - 108 - 109 - 126 - 144			These pins are not connected in the 144-pin EIAJ package

TABLE 3. SIGNAL DESCRIPTIONS (Continued)

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts
Power Dissipation	140 mA

5.2 DC CHARACTERISTICS

The WD90C30 outputs have 4.0 mA maximum source and sink capability (see Table 4), except as follows:

IRQ, IOCHRDY, $\overline{0WS}$,
$\overline{MEMCS16}$, $\overline{IOCS16}$ = 24 mA sink.

PCLK, VID7:0, $\overline{BLANK}$ = 10 mA source/sink.

DRAM Interface = 4 mA source/sink
(RAS, CAS, $\overline{WE}$, $\overline{OE}$, MA, MD)

HSYNC, VSYNC, DA15:0 = 6 mA sink.

$\overline{ROM16}$ = 16 mA SINK.

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz
CI/O	I/O Pin Capacitance	--	12	pF	FC=1 MHz

TABLE 4. DC CHARACTERISTICS

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

- All units are in nanoseconds.
- C_L = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the spec number in column 1 of the same table.

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK (For configuration at power up.)
2	MD Setup to RSET low	50		
3	MD Hold from RSET low	30		
4	RSET low to first $\overline{IOW}$	10t		
	CLOCK TIMING			
1 *	VCLK Period	12.5	72.0	
2	VCLK high	5		@ 1/2 VDD
3	VCLK low	5		@ 1/2 VDD
4 *	Clock Rise Time		2	1V - (VDD - 1V)
5 *	Clock Fall Time		2	1V - (VDD - 1V)
6	VCLK to PCLK Delay	8	20	45 ns @ 120 pF load
7a	VCLK to HSYNC Delay	8	25	
7b	VCLK to VSYNC Delay	8	25	
7c	VCLK to $\overline{BLANK}$ Delay	8	20	
7d	VCLK to VID(7:0) Delay	8	20	45 ns @ 120 pF load up to 30 MHz
8 **	MCLK period	20	30	Max 50 MHz, min 33.3 MHz
9	MCLK high	8		@ 1/2 VDD
10	MCLK low	8		@ 1/2 VDD
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

TABLE 5. AC TIMING CHARACTERISTICS

* Apply to both VCLK and MCLK.

** VCLK0 and MCLK use CMOS level input buffers. $V(IL)_{max}$ = 1.5V, $V(IH)_{min}$ = VDD - 1.5V

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	10		
3a	A(23:17) setup to ALE low	20		
3b	$\overline{BHE}$, DA(15:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	18		
4a	A(23:17) hold from ALE low	10		
4b	DA(15:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	10		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	10		
7a	$\overline{EABUF}$ high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low	9	25	
7b	$\overline{EDBUF}$ low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low	13.5	35	
7c	$\overline{HTL}$ low from $\overline{MRD}$ low		25	
8a	$\overline{EABUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	14.5	35	
8b	$\overline{EDBUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	8.5	25	
8c	$\overline{HTL}$ high from $\overline{MRD}$ high		25	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		20	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		20	
11	DA(15:0) write data setup to $\overline{IOW}$, $\overline{MWR}$ high	20		
12a	DA(15:0) read data hold from $\overline{IOR}$ high or $\overline{MRD}$ high	10		
12b	DA(15:0) write data hold from $\overline{IOW}$, $\overline{MWR}$ high	10		
13	DA(15:0) read data valid after $\overline{IOR}$ low		70	
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15	Memory read data valid from RDY high		40	Note 1
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	20	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		37	
20b	RPLT low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high	9	15	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high	9	20	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H Port)		1t + 20	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H Port)		25	
24	VCLK1 low from $\overline{IOW}$ low (3C2H Port)		1t + 24	

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
25	VCLK1 high from $\overline{IOW}$ high (3C2H Port)		15	
26	A(15:0) valid to $\overline{IOCS16}$ low		35	C_L = 100pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		20	C_L = 100pF
28	A(23:17) valid to $\overline{MEMCS16}$ or $\overline{ROM16}$ low		39	C_L = 100pF
29	$\overline{MEMCS16}$ tristate from the next active ALE		39	C_L = 100pF
30a	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ high	2t + 15		t = ^{1}/MCLOCK Note 2
30b	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ low	2t		t = ^{1}/MCLOCK (Note 3)
30c	ALE pulse width	30		
31	$\overline{OWS}$, low from $\overline{IOW}$, $\overline{MWR}$ low		15	C_L = 100pF

Note 1: Depends on setting of PR31 (3C5H, index 11H) bits 4, 3. t = ^{1}/MCLOCK
00 - Max 40
01 - Max 40 + 1t
10 - Max 40 + 2t
11 - Max 40 - 1t

Note 2: Minimum of #30a should be the greater of 2t + 15 or (#8a + #3b + delay on the external address buffer)

Note 3: Minimum of #30b should be the greater of 2t or (#7b + #11 + delay on the external data buffer)

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	10		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low	13.5	35	
7b	$\overline{EABUF}$ high from $\overline{CMD}$ low	9	25	
8a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high	8.5	25	
8b	$\overline{EABUF}$ low from $\overline{CMD}$ high	14.5	35	
9	DIR active from $\overline{CMD}$ low		20	
10	DIR inactive from $\overline{CMD}$ high		20	
11	$\overline{CSFB}$ delay from valid address/status		30	C_L = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	DA(15:0) write data setup to $\overline{CMD}$ high	20		
17	DA(15:0) Write data hold after $\overline{CMD}$ high	10		
18	DA(15:0) I/O Read data valid from $\overline{CMD}$ low		70	
19	RDY high delay from $\overline{CMD}$ low	0	2.45 µs	
20	DA(15:0) Memory Read Data valid from RDY high		40	Note 1
21a	$\overline{CMD}$ high (inactive)	2t + 15		Note 2
21b	$\overline{CMD}$ low	2t		Note 3
22	RDY low delay from valid address/status		30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low	9	20	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high	9	20	
27	VCLK1 low from $\overline{CMD}$ low (3C2H Port)		1t + 30	
28	VCLK1 high from $\overline{CMD}$ high (3C2H Port)		25	

Note 1: Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

Note 2: Minimum of #21a is the greater of 2t + 5 or (#8b + #1 + delay on external address buffer)

Note 3: Minimum of #21b is the greater of 2t or (#7a + #16 + delay on external data buffer)

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING (256K by 4, 256K by 16)			
1	$\overline{RAS}$ cycle time	*6t		
2	$\overline{RAS}$ pulse width low	*3.5t - d		
3	$\overline{RAS}$ high time (precharge)	*2.5t + d		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*2.5t - 9	2.5t - d	
5	$\overline{CAS}$ cycle time	2t		
6	$\overline{CAS}$ pulse width low	*1t + d		
7	$\overline{CAS}$ high time (precharge)	*1t - d		
8	Row address setup to $\overline{RAS}$ low	1t - 10		
9	Row address hold time from $\overline{RAS}$ low	1t		
10	Column address setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	3		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup $\overline{CAS}$ low	1t- 5	1t + 5	
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as $\overline{CAS}$ low		
18	$\overline{OE}$ high before $\overline{WE}$ low	2t - 10		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	1t - 10		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t + 10		

Notes:
The timing is the result of setting PR33 (3C5H, Index = 13H) = XXX00000
* Timings are adjustable by PR33.
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 1.
t = ^{1}/MCLK
(MCLK = 37.5 MHz for 80 ns DRAM)
(MCLK = 40 MHz for some faster 80 ns DRAM)
(MCLK = 44.4 MHz for 70 ns DRAM)
(MCLK = 49.5 MHz for 60 ns DRAM)
} Maximum MCLK frequency
d = Delay with a min of 4 ns and a max of 7 ns.

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING (64K by 16)			
1	$\overline{RAS}$ cycle time	*5t		
2	$\overline{RAS}$ pulse width low	*3t		
3	$\overline{RAS}$ high time (precharge)	*2t		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*1.5t	1.5t	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	* 1t + 2d		
7	$\overline{CAS}$ high time (precharge)	* 1t - 2d		
8	Row address setup to $\overline{RAS}$ low	1t		
9	Row address hold time from $\overline{RAS}$ low	1/2t		
10	Column adress setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup before $\overline{CAS}$ low	1t - 10		
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as $\overline{CAS}$ low		
18	$\overline{OE}$ high before $\overline{WE}$ low	1t + 2		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	0.5t		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t		

MCLK edge to $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns.

NOTES:
The timing is the result of setting PR33 (3C5H, Index = 13H) = xxx01110
* Timings are adjustable by PR33
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 0.
t = ^{1}/MCLK (MCLK = 36 MHz for 80 ns, 64K by 16 DRAM)
d = Delay with a min of 4 ns and a max of 7 ns.

TABLE 5. AC TIMING CHARACTERISTICS (Continued)

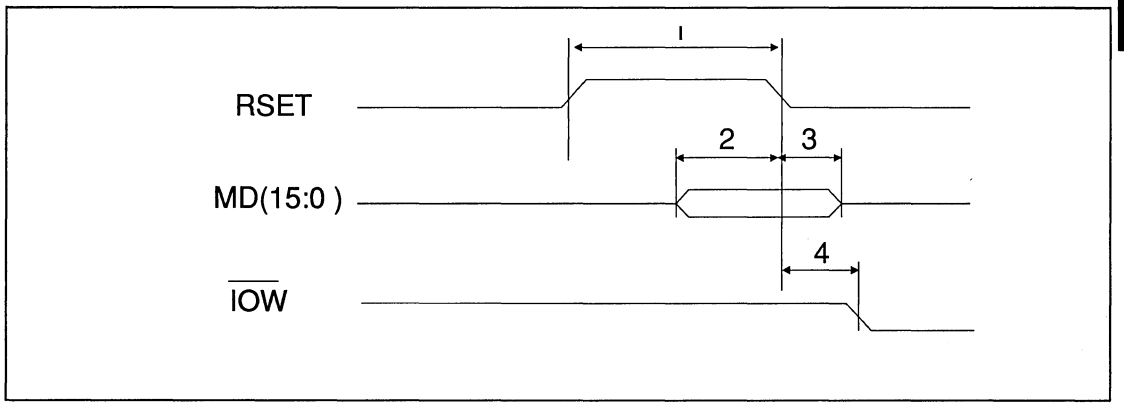

FIGURE 5. RESET TIMING

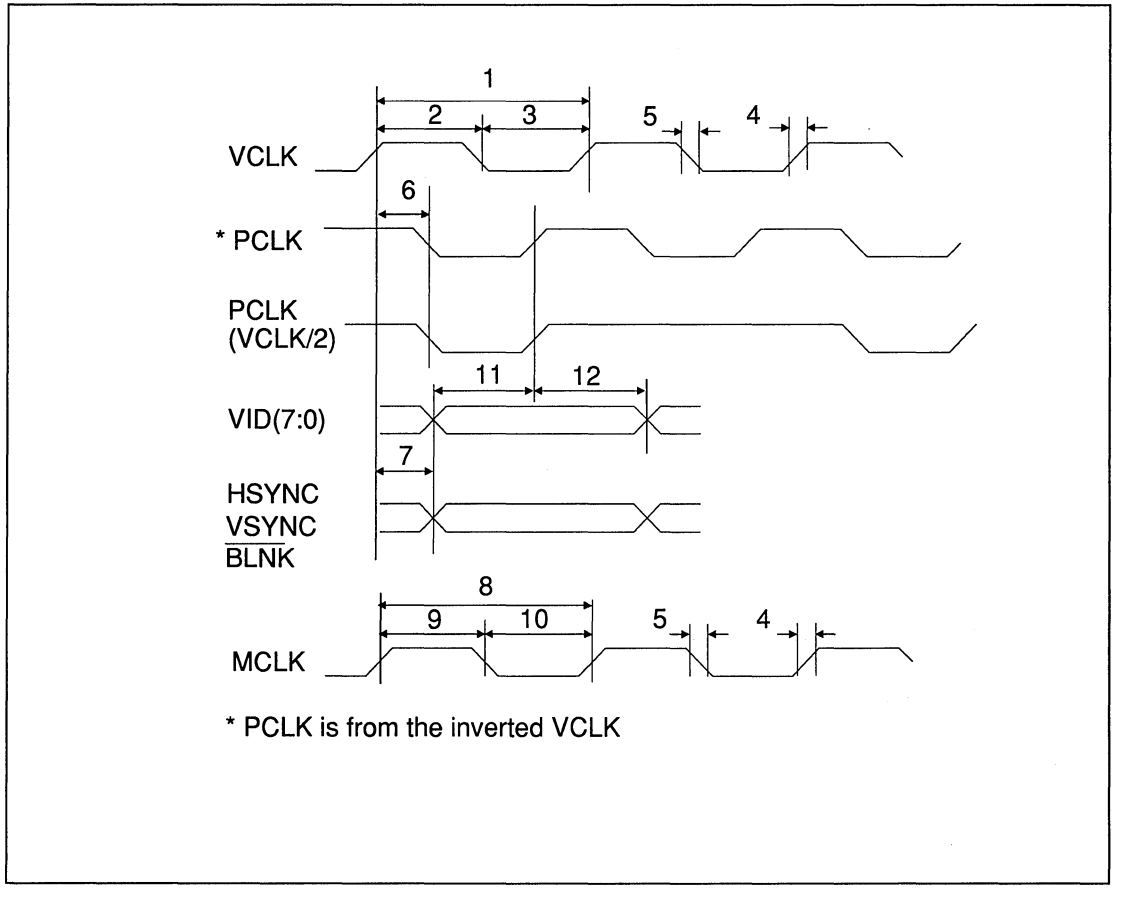

FIGURE 6. CLOCK AND VIDEO TIMING

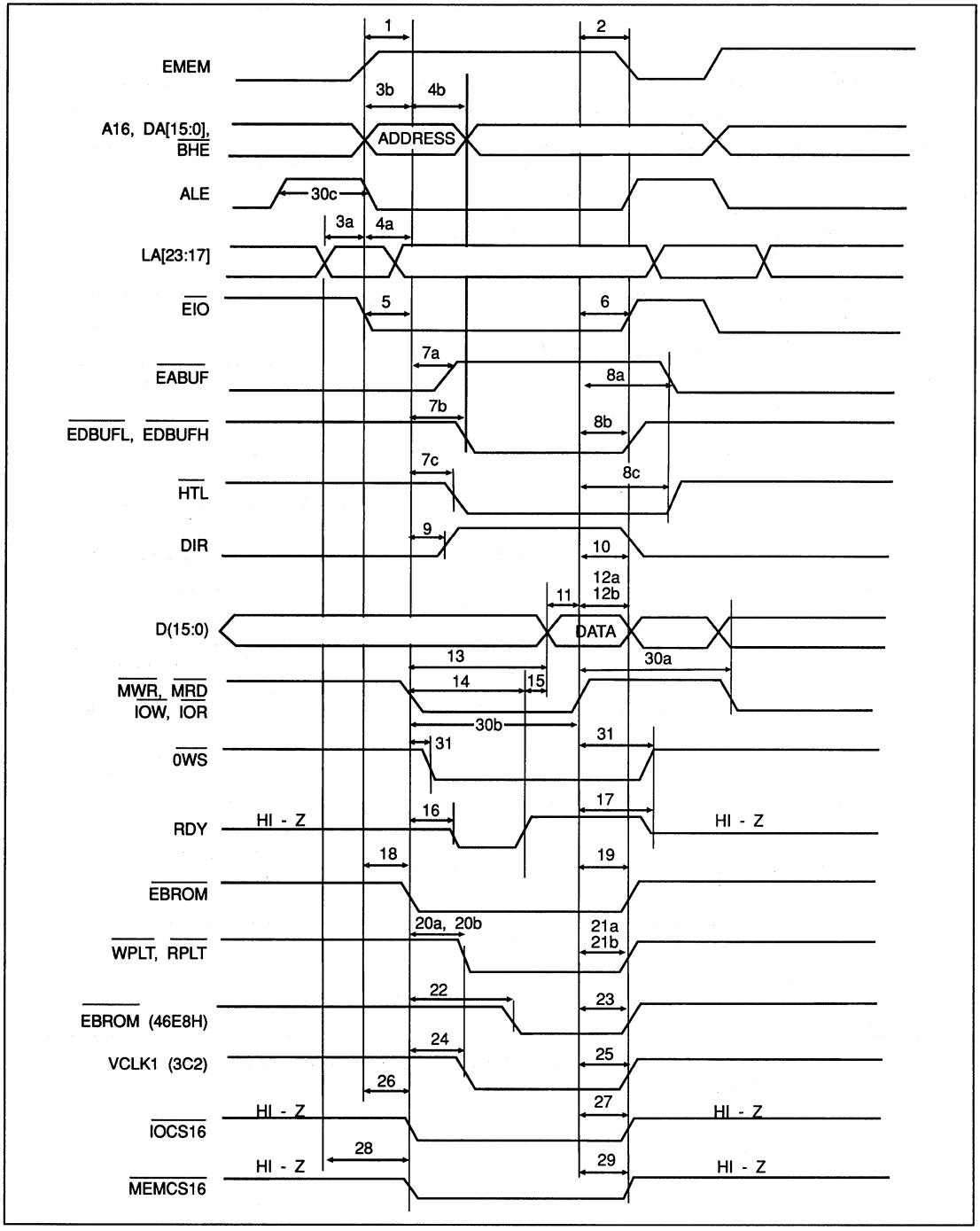

FIGURE 7. AT MODE BUS TIMING

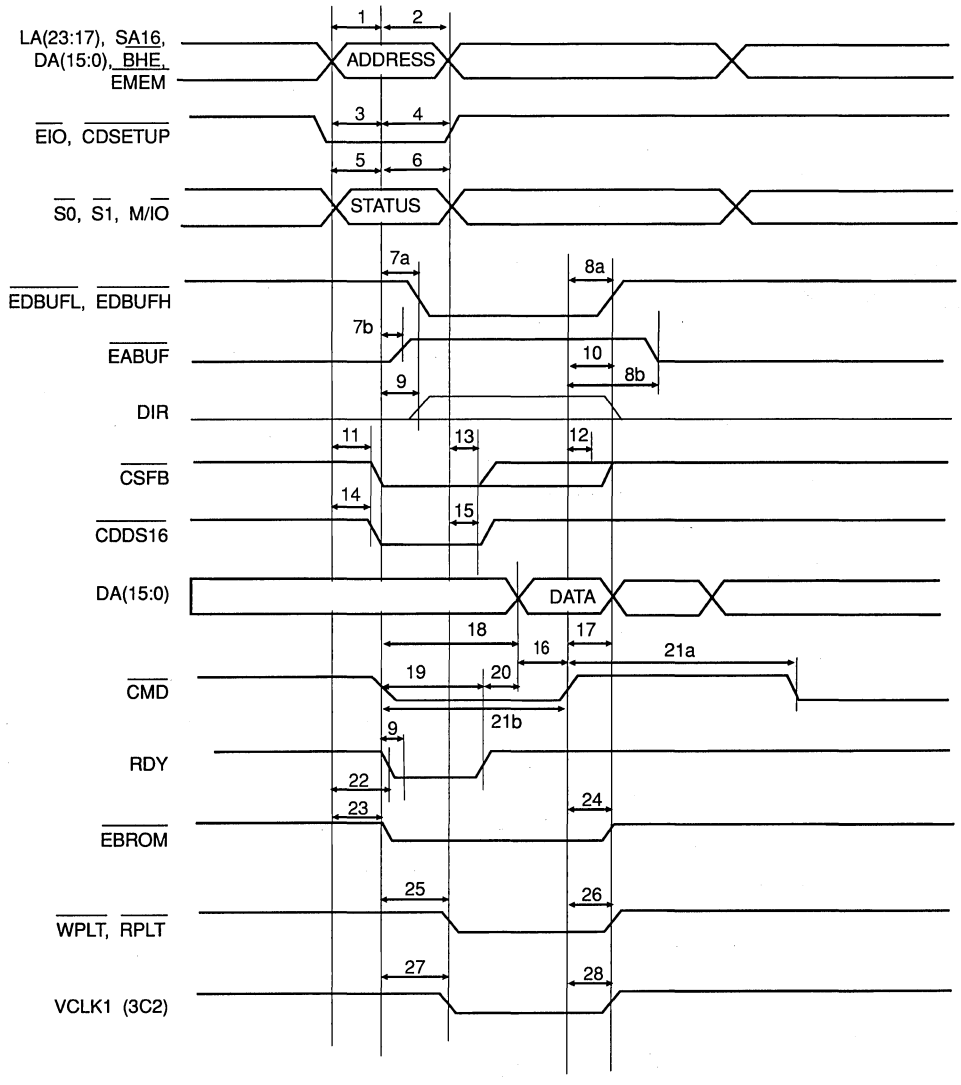

FIGURE 8. MICRO CHANNEL MODE BUS TIMING

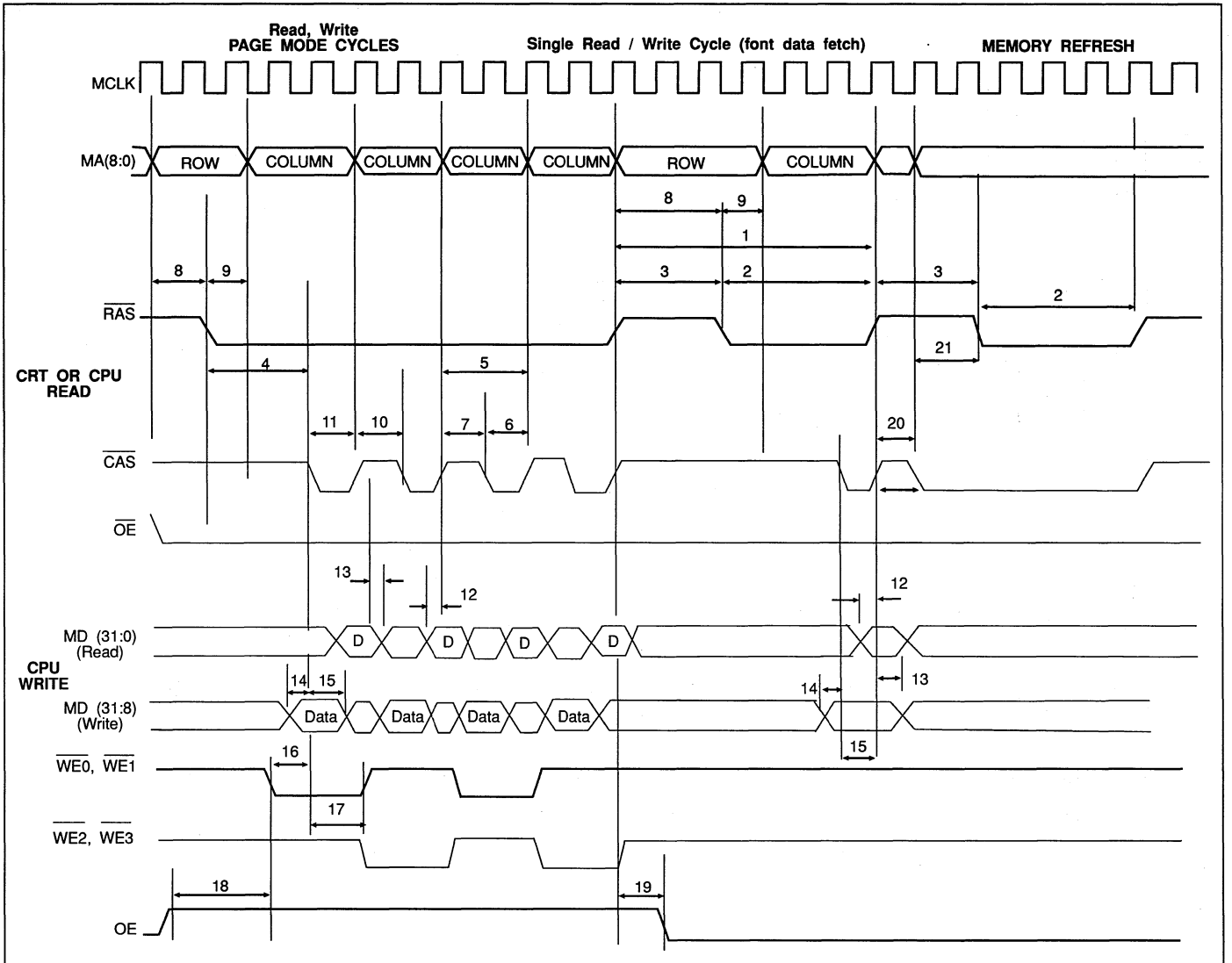

FIGURE 9. DRAM TIMING

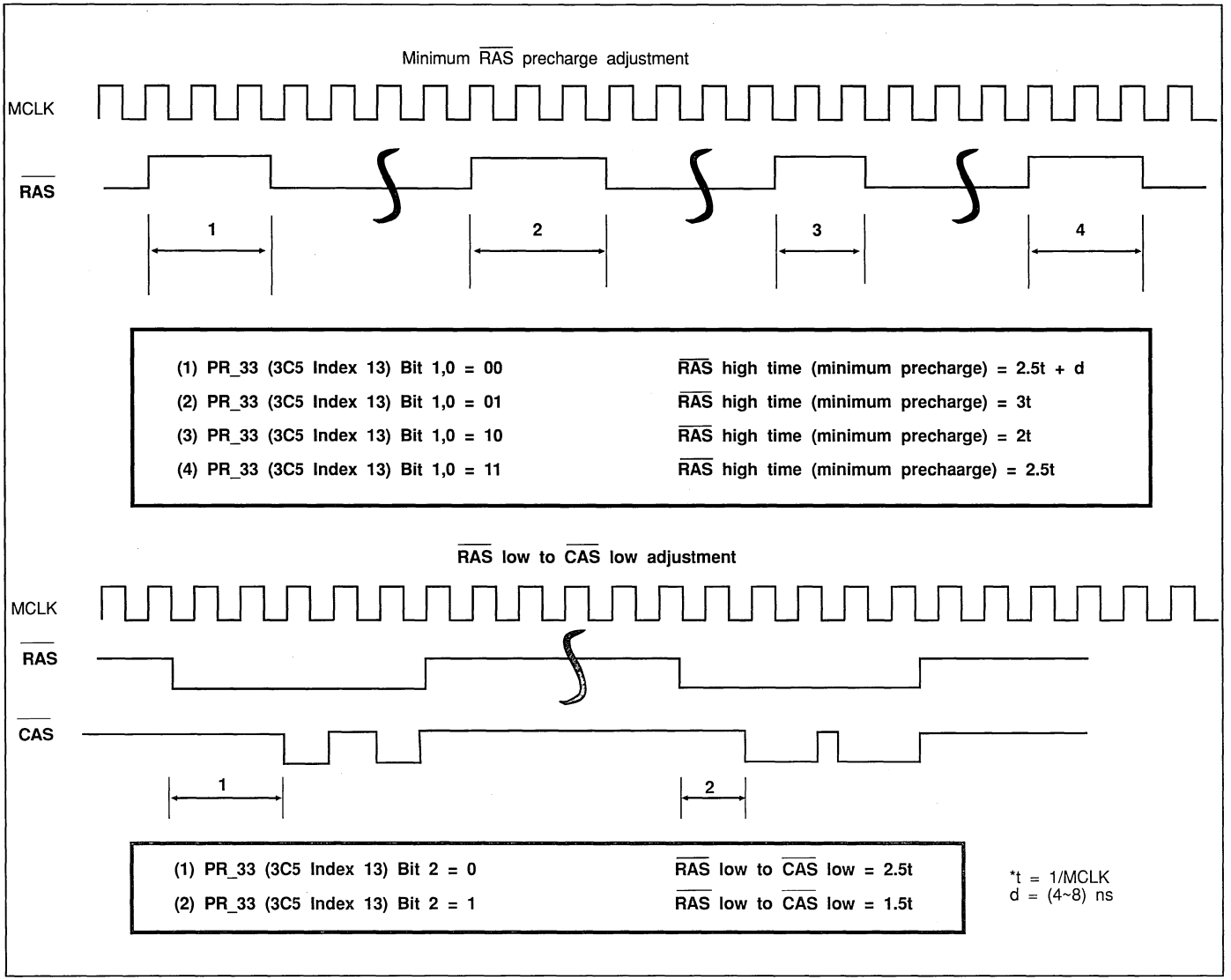

FIGURE 10. DRAM TIMING ADJUSTMENT

DRAM Timing Adjustment: The $\overline{RAS}$, $\overline{CAS}$ timing can be adjusted by register PR33 (3C5H, Index 3H) bits 4 through 0. Only the following timing may be affected: (See Figures 9 and 10).

3 $\overline{RAS}$ high time (precharge)
4 $\overline{RAS}$ low to CAS low
6 $\overline{CAS}$ pulse width

$\overline{CAS}$ pulse width adjustment: $\overline{CAS}$ cycle time is always equal to 2t {t = 1/MCLK}, {d = (4~ 8) ns}.

PR33 (Bits 4 through 3) =
00, $\overline{CAS}$ low = 1t + d; $\overline{CAS}$ high = 1t - d
01, $\overline{CAS}$ low = 1t + 2d; $\overline{CAS}$ high = 1t - 2d
1X, $\overline{CAS}$ low = 1.5t; $\overline{CAS}$ high = $^1/2$t

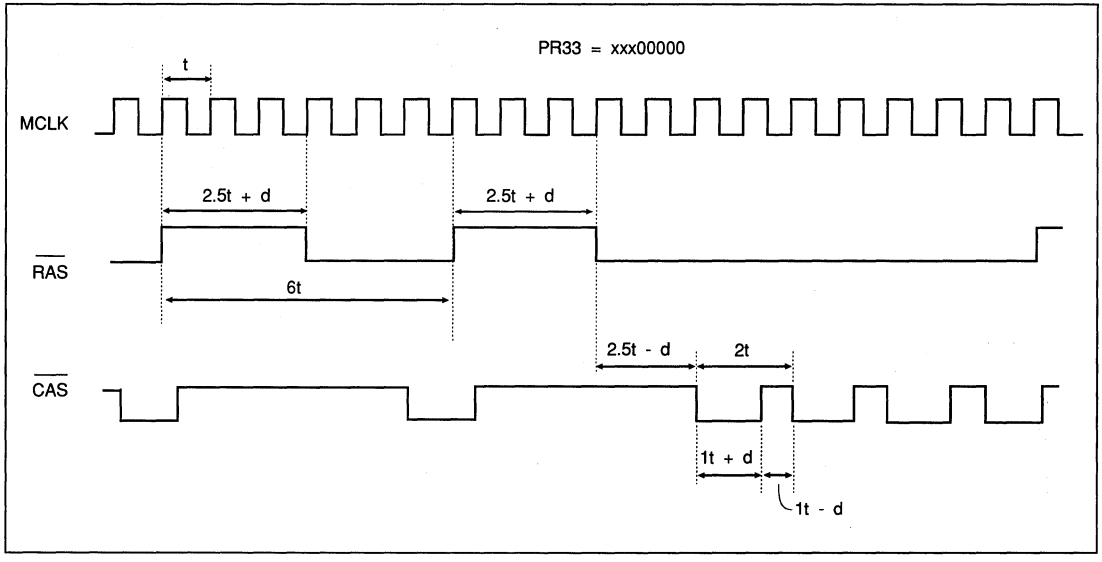

FIGURE 11. 256K BY 4 DRAM TIMING

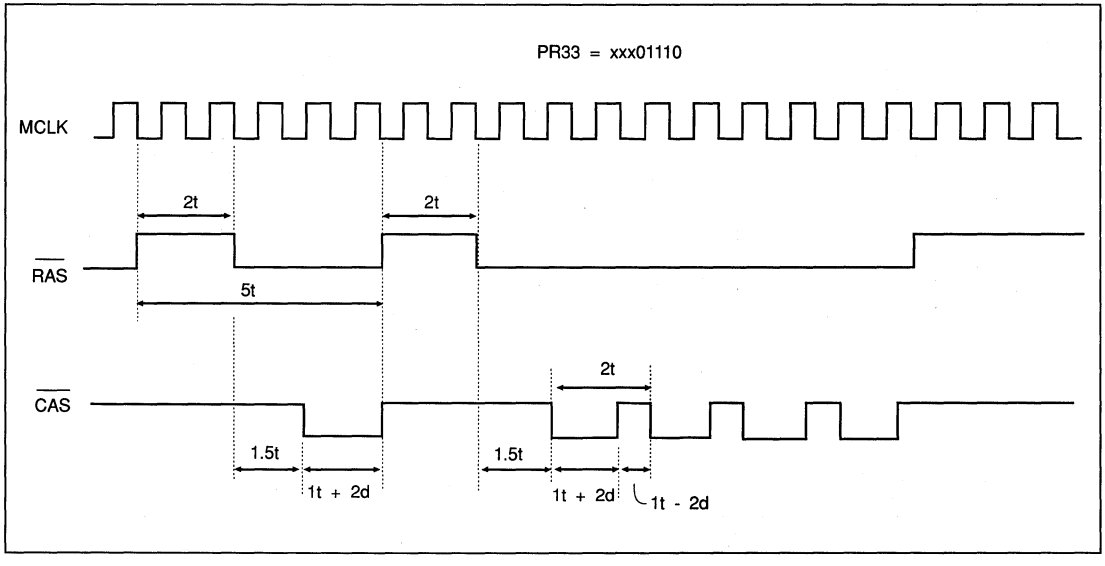

FIGURE 12. 64K BY 16 DRAM TIMING

7.0 WD90C30 REGISTERS

All the standard IBM registers incorporated inside the WD90C30 are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Register	W			3C2
	R			3CC
Input Status Register 0	RO			3C2
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable Register	RW			3C3
* I/O Port 3C3H can be used to replace 46E8H [if CNF(9) = 0] for setup in AT mode. In Micro Channel mode, writes to 3C3H, Bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Register	RW			3C4
Sequencer Data Register	RW			3C5
CRT CONTROLLER REGISTERS				
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Register	RW			3CE
Other Graphics Registers	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Register	RW			3C0
Attribute Controller Data Register	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hexidecimal

TABLE 6. VGA REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3B5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
Reserved 3X5.31- 3X5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3D5.3C
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.8	3C5.8
PR23 Scratch Pad	RW	3C5.9	3C5.9
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and Zero Wait State Control Registers	RW	3C5.13	3C5.13
PR34 Video Memory Mapping Register	RW	3C5.14	3C5.14
PR35 USR0, USR1 Output Select Register	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers description for more details.

TABLE 7. PR REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

TABLE 8. COMPATIBILITY REGISTERS SUMMARY

7.1 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

7.1.1 Miscellaneous Output Register, Read Port = 3CCH, Write Port = 3C2H

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bits (3:2)

Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register Bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4H and 3B5H), or Color (3D4H and 3D5H) mode. Bit 0 also maps Input Status Register 1 at MDA (3BAH) or CGA (3DAH).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

7.1.2 Input Status Register 0, Read Only Port = 3C2H

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bits (6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode.
DA15 monitor status (Pin 20) is sampled and can be read from this bit.

Bits (3:0)

Reserved.

7.1.3 Input Status Register 1, Read Only Port = 3?AH

BIT	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2:1	Reserved
0	Display Enable

Bits (7:6)

Reserved.

Bits (5:4)

Color Plane Diagnostics.
These bits allow the processor to select two of eight colors by activating the Attribute Controller's Color Plane Enable Register Bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bits (2:1)

Reserved.

Bit 0

Display Enable Status.

0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.1.4 Feature Control Register, Read Port = 3CAH, Write Port = 3?AH

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits (7:4)

Reserved

Bit 3

Vertical Sync Control.

0 = VSYNC output enabled.
1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

Bits (2:0)

Reserved

7.2 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

7.2.1 Sequencer Index Register, Read/Write Port = 3C4H

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/Index Bits

Bits (7:5)

Reserved.

Bits (4:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer Register to be accessed. Sequencer extension registers are also indexed by this register.

7.2.2 Reset Register, Read/Write Port = 3C5H, Index = 00H

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits (7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

7.2.3 Clocking Mode Register, Read/Write Port = 3C5H, Index = 01H

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits (7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if Bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate an 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

7.2.4 Map Mask Register, Read/Write Port = 3C5H, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits (7:4)

Reserved.

Bits (3:0)

Controls Writing to Memory Maps (3-0), respectively.
0 = Writing to maps (3-0) disallowed.
1 = Maps (3-0) accessible.

7.2.5 Character Map Select Register, Read/Write Port = 3C5H, Index = 03H

BIT	FUNCTION
7:6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4, Bit 1 = 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. A "0" selects Character Map B. A "1" selects character map A. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and Bit 4 of the attribute code.

Bits (7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of Character Map A along with Bits 3 and 2, select the location of Character Map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of Character Map B along with Bits 1 and 0, select the location of Character Map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bits (3:2)

Character Map Select A.
Refer to Bit 5 table.

Bits (1:0)

Character Map Select B.
Refer to Bit 4 table.

7.2.6 Memory Mode Register, Read/Write Port = 3C5H, Index = 04H

BIT	FUNCTION
7:4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits (7:4)

Reserved.

Bit 3

Chains Four Maps.

0 = Processor sequentially accesses data using map mask register.

1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.

0 = Even processor addresses to access Maps 0 and 2. Odd processor addresses to access Maps 1 and 3.

1 = Sequential processor access as defined by Map Mask Register.

Bit 1

Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/EGA modes.

Bit 0

Reserved.

PORT	INDEX	VGA REGISTER NAME	*6845 REGISTER NAME
3?4	---	CRT Controller Address Register	CRTC Address Register
3?5	00	Horizontal Total	HorizontalTotal
3?5	01	Horizontal Display Enable End	Horizontal Display
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Display
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Maximum Scan Line Address
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Address High
3?5	0D	Start Address Low	Start Address Low
3?5	0E	Cursor Location High	Cursor Location High
3?5	0F	Cursor Location Low	Cursor Location Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TEXT = 1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes
2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.
3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.
5. Port addresses are in hex.

TABLE 9. CRT CONTROLLER REGISTERS

7.3 CRT CONTROLLER REGISTERS

7.3.1 CRT Address Register, Read/Write Port = 3?4H

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bits (7:5)

Reserved.

Bits (4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed in hexidecimal.

7.3.2 Horizontal Total Register, Read/Write Port = 3?5H, Index = 00H

BIT	FUNCTION
7:0	Horizontal Total Period

Bits (7:0)

Count Plus Retrace Less Five.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.3.3 Horizontal Display Enable End Register, Read/Write Port = 3?5H, Index 01H

BIT	FUNCTION
7:0	Displayed Characters per Scan Line

Bits (7:0)

This register contains the total number of displayed characters less one. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.4 Start Horizontal Blanking Register, Read/Write Port = 3?5H, Index = 02H

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.5 End Horizontal Blanking Read/Write Port = 3?5H, Index = 03H

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

Bit 7

Reserved

Bits (6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

End Horizontal Blanking.
Start blanking register plus the width of the horizontal blank in character clocks. The least significant five bits are programmed in this register,

while the most significant bit is the End Horizontal Retrace Register (Index 05H) Bit 7. When the least significant five bits of the horizontal character counter matches these six bits, the horizontal blanking ends.

7.3.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5H, Index = 04H

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits (7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.7 End Horizontal Retrace Register, Read/Write Port = 3?5H, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

This register is locked if the PR Register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

Bit 7

MSB (Sixth Bit) of End Horizontal Blanking Register.

Bits (6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace.
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

7.3.8 Vertical Total Register, Read/Write Port = 3?5H, Index = 06H

BIT	FUNCTION
7:0	Vertical Total Scan Lines

Bits (7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of an eleven bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus two. Time for vertical retrace, and vertical sync are also included. The eighth and nineth bits of this count are loaded into the Vertical Overflow Register (Index = 07H) as Bit 0 and Bit 5, respectively. Bit 10 of this count is in the 3?5H, index 3EH, bit 0. In 6845 modes, total vertical display time in rows is programmed into Bit 6 - Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09H Bits 4 through 0). This register is locked if the PR Register PR3(0) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.9 Overflow Vertical Register, Read/Write Port = 3?5H, Index = 07H

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (Index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (Index = 12H).

++Bit 5

Vertical Total Bit 9 (Index = 06H).

Bit 4

Line Compare Bit 8 (Index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (Index =15H).

++Bit 2

Start Vertical Retrace Start Bit 8 (Index = 10H).

++ Bit 1

Vertical Total Bit 8 (Index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register Bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

7.3.10 Preset Row Scan Register, Read/Write Port = 3?5H, Index = 08H

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits (6:5)

Byte Panning Control.
These bits allow up to three bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bits (4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.3.11 Maximum Scan Line Register, Read/Write Port = 3?5H, Index = 09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is Bit 9 of the Line Compare Register (Index = 18H).

Bit 5

Start Vertical Blank.
This is Bit 9 of the Start Vertical Blank Register (Index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bits (4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus one. In 6845 mode, Bits 5 through 7 are reserved, and Bits 4 through 0 are programmed with the maximum scan line count less one for non-interlace mode. Interlaced mode is not supported.

7.3.12 Cursor Start Register, Read/Write Port = 3?5H, Index = 0AH

BIT	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bits (7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bits (4:0)

Cursor Start Scan Line.
These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less one. If this value is programmed with a value greater than the Cursor End Register (Index = 0BH), no cursor is generated. For 6845 modes, Bit 7 is reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value. Bit 6 is not used.

7.3.13 Cursor End Register, Read/Write Port = 3?5H, Index = 0BH

BIT	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

Bit 7

Reserved.

Bits (6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks, e.g., one character clock skew moves the cursor right by one position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

Cursor End Scanline.
These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, Bits 7 through 5 are reserved and Bits 4 through 0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode, i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.3.14 Start Address High Register, Read/Write Port = 3?5H, Index = 0CH

BIT	FUNCTION
7:0	Start Address High Byte

Bits (7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16-bit video memory address, used for screen refresh. The low order 8-bit register is at Index 0DH. The PR Register PR3 Bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes Bits 6 and 7 are forced to "0", regardless of this register's contents, while the lower order eight bits are at Index register 0DH.

7.3.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7:0	Start Address Low Byte

Bits (7:0)

Start Address Low Byte.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

7.3.16 Cursor Location High Register, Read/Write Port = 3?5H, Index = 0EH

BIT	FUNCTION
7:0	Cursor Location High Byte

Bits (7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of the 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at Index 0FH. In VGA mode, the PR Register PR3 Bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, Bits 6 and 7 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

7.3.17 Cursor Location Low Register, Read/Write Port = 3?5H, Index = 0FH

BIT	FUNCTION
7:0	Cursor Location Low Byte

Bits (7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

7.3.18 Vertical Retrace Start Register, Read/Write Port = 3?5H, Index = 10H

BIT	FUNCTION
7:0	Vertical Retrace Start (Lower eight bits)

Bits (7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the 11-bit Vertical Retrace Start Register. Bits 8 and 9 are located in the Overflow Register (Index = 07H). Bit 10 is located in 3?5H, Index 3EH, bit 2. In 6845 compatible mode, this register shows the high order six bits in positions 5 through 0 as the light pen read back value, and Bits 6 and 7 are reserved. The lower order eight bits of the Light Pen Read Back Register are at the Index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3(0) = 1.

7.3.19 Vertical Retrace End Register, Read/Write Port = 3?5H, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller Index registers in the range of index 00H-07H. Line Compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates three refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates five DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enable vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a "0" to) an internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bits (3:0)

Vertical Retrace End.
Specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The four-bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.3.20 Vertical Display Enable End Register, Read/Write Port = 3?5H, Index = 12H

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bits (7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of this 11-bit register defines where the active display frame ends. The programmed count is in scan lines minus one. Bits 8 and 9 are in the Overflow Register (Index 07H) at positions 1 and 6, respectively. Bit 10 is in 3?5H, Index 3EH, Bit 10

7.3.21 Offset Register, Read/Write Port = 3?5H, Index = 13H

BIT	FUNCTION
7:0	Logical Line Screen Width

Bits (7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

7.3.22 Underline Location Register, Read/Write Port = 3?5H, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count by Four for Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by four.

Bits (4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where underline is to be displayed. Load a value one less than the desired scan line number.

7.3.23 Start Vertical Blank Register, Read/Write Port = 3?5H, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7:0	Start Vertical Blank (Lower eight bits)

Bits (7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the 11-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (Index = 07H) and Bit 9 is in the Maximum Scan Line Register (Index = 09H). Bit 10 is 3?5H; Index 3EH, Bit 3. The eleventh bit value is reduced by one from the desired scan line count where the vertical blanking signal starts.

7.3.24 End Vertical Blank Register, Read/Write Port = 3?5H, Index = 16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7:0	End Vertical Blank

Bits (7:0)

Vertical Blank Inactive Count.
End Vertical Blank is an eight-bit value calculated as follows:
Eight-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

7.3.25 CRT Mode Control Register, Read/Write Port = 3?5H, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB. See the Table 10.
1 = Byte address mode.

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256 Kbytes of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by two increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by two.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter Bit 1 as output at MA14 address pin.
1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller Compatibility Mode Support for CGA Operation.
0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.
1 = Enable memory address Pin 13 to be output at MA13 address pin.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLE WORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See Bit 5, defining address wrap. This table is only applicable when PR Register PR1 Bits 7 and 6 equal zero, or PR16 Bit 1 equals one.

The CRT Underline Location Register (Index = 14H) Bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (Index 17H) Bit 6 controls addressing.

TABLE 10. WORD OR BYTE MODE

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7.3.26 Line Compare Register, Read/Write Port = 3?5H, Index = 18H

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bits (7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (Index = 07H) and Bit 9 is in the Maximum Scan Line Register (Index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.4 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

7.4.1 Graphics Index Register, Read/Write Port = 3CEH

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits (7:4)

Reserved.

Bits (3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.4.2 Set/Reset Register, Read/Write Port = 3CFH, Index = 00H

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (Index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight-bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (Index = 05H) Bit 1 and Bit 0.

7.4.3 Enable Set/Reset Register, Read/Write Port = 3CFH, Index = 01H

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to "0", disable the Set/Reset Register (Index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (Index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.4.4 Color Compare Register, Read/Write Port = 3CFH, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Color Compare.

The color compare bit contains the value to which all eight bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with Bit 3 = 0 for the Graphics Mode Register (Index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.4.5 Data Rotate Register, Read/Write Port = 3CFH, Index = 03H

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits (7:5)

Reserved.

Bits (4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (Index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches
Note: "Data" refers to CPU data that has gone through data rotation. The latches contain the data from the last memory read operation.		

Bits (2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (Index = 05H).

7.4.6 Read Map Select Register, Read/Write Port = 3CFH, Index = 04H

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits (7:2)

Reserved.

Bits (1:0)

Map Select.
These bits select memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained Maps 0 and 1 or value 10b or 11b to select the chained Maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.4.7 Graphics Mode Register, Read/Write Port = 3CFH, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four-bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by Bits 2 and 3 of the Color Select Register located at Index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256-color mode.

Bit 5

Shift Register.

Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 through Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the Sequencer Memory Mode Register (Index = 04H). Even system addresses access Maps 0 or 2 and odd system addresses access Maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (Index 04H). This setting will have no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bits (1:0)

Write Mode.

Table 11 defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	**Write Mode 0.** If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is rotated right by the number of bits defined in the Data Rotate Register (with the old LSB now the new MSB).
0	1	**Write Mode 1.** This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2.** Memory maps (3:0) are filled with the eight-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3.** Eight bits of the value contained in the Set/Reset Register (Index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (Index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an eight-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

TABLE 11. WRITE MODES

7.4.8 Miscellaneous Register, Read/Write Port = 3CFH, Index = 06H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits (7:4)

Reserved.

Bits (3:2)

Memory Map 1, 0.
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address Bit A0 is the memory address Bit MA0.
1 = CPU address Bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects Map 0 or 2, while A0 = 1 selects Map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

7.4.9 Color Don't Care Register, Read/Write Port = 3CFH, Index = 07H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits (7:4)

Reserved.

Bits (3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

7.4.10 Bit Mask Register, Read/Write Port = 3CFH, Index = 08H

BIT	FUNCTION
7:0	Bit Mask

Bits (7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.
0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

7.5 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:

1. The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (Port = 3?AH) clears the flip-flop and selects the Address Register, which is read through address 3C1H and written at address 3C0H. Once the Address Register has been loaded with an index, the next write operation to 3C0H will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0H, but does not toggle for reads to address 3C1H.
2. Attribute register data is written at 3C0H and register data is read from address 3C1H.
3. Reserved bits should be set to zero.

7.5.1 Attribute Index Register, Read/Write Port = 3C0H

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits (7:6)

Reserved.

Bit 5

Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (Index 00 - 0FH).

1 = Enable internal color palette and normal video translation.

Bits (4:0)

Attribute Controller Index Register Address Bits.

7.5.2 Palette Registers 00-0FH, Read Port = 3C1H/Write Port = 3C0H

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:6)

Reserved.

Bits (5:0)

Palette Pixel Colors.

They are defined as follows:

0 = Current pixel color deselected.

1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

7.5.3 Attribute Mode Control Register, Read Port = 3C1H/Write Port = 3C0H, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.

0 = VID5 and VID4 palette register outputs are selected.

1 = Color Select Register (Index 14H) Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.

1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also Bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

7.5.4 Overscan Color Register, Read Port = 3C1H/Write Port = 3C0H, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:0)

Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to "0". Border colors are set as shown above.

7.5.5 Color Plane Enable Register, Read Port = 3C1H/Write Port = 3C0H, Index = 12H

BIT	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bits (7:6)

Reserved.

Bits (5:4)

Video Status Control.
These bits select two out of eight color outputs which can be read by the Input Status Register 1 (Port = 03?AH) Bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bits (3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

7.5.6 Horizontal Pel Panning Register, Read Port = 3C1H/Write Port = 3C0H, Index = 13H

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits (7:4)

Reserved.

Bits (3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For nine dots/character modes, up to eight pixels can be shifted horizontally to the left. Likewise, for eight dots/character up to seven pixels can be shifted horizontally to the left. For 256 color, up to three position pixel shifts can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.5.7 Color Select Register, Read Port = 3C1H/Write Port = 3C0H, Index = 14H

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bits (7:4)

Reserved.

Bits (3:2)

Color Value MSB.
Two most two significant bits of the eight-digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bits (1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight-bit color value. They are selected by the Attribute Controller Mode Control Register (Index = 10H).

7.6 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes

7.6.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode.
If Bit 1=1 and Port 3BFH Bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video Enable.
0 = Video Disabled
1 = Video Activated

Bit 2

Reserved.

Bit 1

Port 3BFH Enabled.
0 = Prevents setting of Port 3BFH Bits 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFH Bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode.
Should be set to "1".
0 = High resolution disabled.
1 = High resolution is enabled.

7.6.2 Hercules Registers

The Hercules Mode Register is a two-bit write only register located at I/O port address 3BFH. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8H overrides the write Port 3BFH functions defined by its Bits 0 and 1. The associated details are shown below.

7.6.3 Enable Mode Register 3B8H

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bits (6:2,0)

Reserved.

Bit 1

Port 3BFH Bit 0 Override.
0 = Prevents setting of Port 3BFH Bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFH Bit 0 to switch for the alpha or graphics mode selection.

7.6.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8H) Bit 7 selects the displayed memory page address in the graphics mode. When it is reset, Bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8H) Bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

7.6.5 Color CGA Operation Register, Write Only Port = 3D8H

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bits (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

7.6.6 CGA Color Select Register, Write Only Port = 3D9H

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bits (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA (two bits per pixel).
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 2

Red Border/Background
Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

7.6.7 CRT Status Register, MDA Operation, Read Only Port = 3BAH

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BXH).

Bits (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bits (2:1)

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

7.6.8 CRT Status Register, CGA Operation, Read Only Port = 3DAH

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

7.6.9 AT&T/M24 Register, Write Only Port = 3DEH

This is a write only, eight-bit register located at address 3DEH. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting Bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5:4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bits (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode, 400-line mode.
A 400-line monitor is required for this mode.
0 = 200-line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400-line graphics.

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3B5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
Reserved 3X5.31- 3X5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3B5.3C
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.8	3C5.8
PR23 Scratch Pad	RW	3C5.9	3C5.9
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and zero Wait State Control Registers	RW	3C5.13	3C5.13
PR34 Video Memory Mapping Register	RW	3C5.14	3C5.14
PR35 USR0, USR1 Output Select Register	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected.

TABLE 12. PR REGISTERS SUMMARY

7.7 WD90C30 PR REGISTERS

The WD90C30 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C30 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5H means that the register is mapped into either 3B5H in monochrome mode or 3D5H in color modes.
2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index, e.g., 3CF.0F implies 0F → 3CEH (Select Index register) followed by (Data byte) → 3CFH (Data Port).

Registers PR0 through PR4 and PR11 through PR1A are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101. A register remains unlocked until another value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 Bit 1 to "1" does not read protect registers PR10 through PR17. PR21-PR23 and PR30-PR35 are R/W protected by PR20. PR20 must be loaded with 48H to make it possible to read or write to PR21-PR23 and PR30-PR35. All PR registers are set to "0" at power on reset except where noted.

7.7.1 Address Offset Registers PROA And PROB

PROA - Address Offset Register A, Read/Write Port = 3CFH, Index = 09H

BIT	FUNCTION
7:0	Primary Address Offset Bits

PROB - Address Offset Register B, Read/Write Port = 3CFH, Index = 0AH

BIT	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C30 can control up to 1 Mbyte of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C30 has two CPU address offset registers PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PROA (Bits 6:0) or PROB (Bits 6:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture. PROA and PROB will then provide four Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a four Kbyte segment to another four Kbyte segment of the display memory.)

PROA and PROB are all set to zero at power-on-reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 0.**
  When PR1-3 = 0, then PR0A is always selected as the CPU address offset register.

  When PR1-3 = 1 and if the display memory is mapped into A000 - BFFFF (128 Kbytes), PR0A offset CPU address range is B0000 - BFFFF; the PR0B offset CPU address range is A0000 - AFFFF. (If CPU address bit A16 = 1, select PR0A. Otherwise PR0B is selected.)

  When PR1-3 = 1 and if the display memory is mapped into A0000 - AFFFF (64 Kbytes) or B0000 - B7FFF or B800 - BFFFF (32 Kbytes), then PR0B offset CPU address range is A0000 - A7FFF or B0000 - B7FFF. PR0A offset CPU address range is A8000 - AFFFF or B8000 - BFFFF. (If CPU address bit A15 = 1, select PR0A. Otherwise PR0B is selected.)
- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 1.**
  Both PR0A and PR0B are enabled. A CPU memory write will select PR0B as the offset register. Otherwise, PR0A is selected as the offset register.

7.7.2 PR1 - Memory Size, Read/Write Port = 3CFH, Index = 0BH

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate Address Offset Register PR0B
2	16-Bit System Interface
1	16-bit BIOS ROM
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1(1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits (7:6)

Memory Size.
These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16(1) select the way memory is mapped into the CPU address space. IF PR16(1) is set to "1", the memory mapping will be set identical to the IBM VGA, regardless of PR1(7), PR1(6).

Tables 13 through 16 list the different settings on these two bits for different memory organizations.

PR1(7) = 0 PR1(6) = 0 256K TOTAL; IBM VGA MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	BYTE CPU	CRT	WORD CPU	CRT	DBL WORD CPU	CRT
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(14) or[3] XRN(5)	CA(15) or[4] CA(14)	A(14)	CA(12)

TABLE 13. IBM COMPATIBLE MEMORY ORGANIZATION

PR1 (7) = 0 PR1 (6) = 1 256K TOTAL; 64K/PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	BYTE CPU	CRT	WORD CPU	CRT	DBL WORD CPU	CRT
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16) or[3] XRN(5)	CA(15)	A(16)	CA(14)

TABLE 14. WD90C30 MEMORY ORGANIZATION - 256 KBYTES

PR1(7) = 1, PR1(6) = 0 512K TOTAL;128K/PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	PA	PA	PA	PA	PA	PA
MA(16)	A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16) or[3] XRN (5)	CA(15)	A(16)	CA(14)

TABLE 15. WD90C30 MEMORY ORGANIZATION - 512 KBYTES

PR1 (7), PR1 (6) = 1 1M TOTAL; 256K PLANE; WD90C30 MEMORY ORGANIZATION						
VIDEO RAM ADDR BIT	**BYTE CPU**	**CRT**	**WORD CPU**	**CRT**	**DBL WORD CPU**	**CRT**
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
MA(13)	A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)
----	----	----	----	----	----	----
----	----	----	----	----	----	----
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(16) or[3] XRN (5)	CA(15)	A(18)	CA(16)

TABLE 16. WD90C30 MEMORY ORGANIZATION - 1 MBYTE

NOTES:

1. A(19:0) are WD90C30 internally modified system Addresses (CPU address + offset address).
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted Bit 5. XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. In IBM compatible memory mapping, 3C5.4, Bit 1 = 1 will select XRN(5) to replace CPU address bits. In other memory mapping schemes (PR1(7,6) ≠ 00, 3C5.4H, Bit 1 = 1 and PR16_2 = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as MA(0) if CRTC Mode Register 17, Bit 5 = 1 in word addressing modes.
5. PA is the memory plane select bit when DRAM interface is set for 16 bits.
   PA = 0 selects Plane 1,0
   PA = 1 selects Plane 2,3
6. MA 17-0 are divided into $\overline{RAS}$, $\overline{CAS}$ addresses as follows:

For 2256K by 4 DRAM or 256K by 16 DRAM	MA(16) - MA (8) ⇒ MA(17), M(7) - MA(0) ⇒	$\overline{RAS}$(8) - $\overline{RAS}$(0) $\overline{CAS}$(8) - $\overline{CAS}$(0)
For 64K by 16 DRAM	MA(15) - MA(8) ⇒ MA(7) - MA(0) ⇒	$\overline{RAS}$(7) - $\overline{RAS}$(0) $\overline{CAS}$(7) - $\overline{CAS}$(0)
MA(17,16) = 00 01 10 11	Select 1st 64K bank Select 2nd 64K bank Select 3rd 64K bank Select 4th 64K bank	

Bits (5:4)

PRI(5,4) Memory Map Select.

0	0	IBM VGA mapping. CPU addresses are decoded from 0A0000H - 0BFFFFH from the lowest 1 Mbyte CPU address space (depending on 3CF.06H bits 2 and 3).
0	1	First 256 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X3FFFFH)
1	0	First 512 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X7FFFFH)
1	1	In any 1Mbyte CPU address space (X00000H - XFFFFFH)

*PR34(3C5.14H) Bits 3-0 control to which 1 Mbyte of CPU address space the WD90C30 is mapped.

Bit 3

Enable Alternate Address Offset Register PROB.

Bit 2

Enable 16 bit system interface bus.
When set to "1", $\overline{MEMCS16}$ will be active low for all of the video memory cycles.

Bit 1

16-bit BIOS ROM.
When set to "1", the BIOS ROM has a 16 bit data path ($\overline{ROM16}$ will respond to ROM access). Otherwise, the BIOS ROM has an eight-bit data path.

A pull-down resistor on MD(10) will set this bit to "1" after power-on reset. This bit can also be set to "1" by an I/O write cycle only if the CNF(1) = 1.

Bit 0

BIOS ROM Map Out.
If set to "1", the BIOS ROM is mapped out. A pull-down resistor on MD(0) sets this bit to "1" at power-on-reset.

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7.7.3 PR2-Video Select Register, Read/Write Port = 3CFH, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register and Mode.

Bit 6

6845 Compatibility.
0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select.
The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from Planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1, i.e., selecting page mode addressing overrides plane selected table shown above.

Bits (4:3)

Character clock period control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132-character text mode only)
1	0	9 dots
1	1	6 dots if PR17(5) = 0; 10 dots if PR17(5) = 1.

NOTE:
The character clock period control functions have no effect in graphics modes (Graphics Mode always uses eight dots).

Bit 2

Underline and character map select.
Setting this bit to "1" enables underline for all odd values of attribute codes, e.g., programming "1" gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to "0". Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

Third Clock Select Line.
This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to "1". When CNF(3) is set to "0", it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when Sequencer Register 1, Bit 3, is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.7.4 PR3 - CRT Lock Control Register, Read/Write Port = 3CFH, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7

Lock VSYNC polarity as programmed at 3C2H Bit 7.

Bit 6

Lock HSYNC polarity as programmed at 3C2H Bit 6.

Bit 5

Lock Horizontal Timing.
Locks CRTC registers of Group 0 and 4. Prevents attempts by applications software to unlock Group 0 registers by setting 3?5.11H Bit 7 = 0.

Bit 4

Bit 9 Control.
Bit 9 of CRT Controller Start Memory Adress High Register 3?5.0CH and Bit 9 of Cursor Location High 3?5.0EH. This bit corresponds to Character Address CA(17).

Bit 3

Bit 8 Control.
Bit 8 of CRT Controller Start Memory Address High Register 3?5.0CH and Bit 8 of Cursor Location High 3?5.0EH. This bit corresponds to Character Address CA(16).

Bit 2

Cursor Control.
Cursor Start, Stop, Preset Row Scan, and Maximum Scan Line Address registers values multiplied by two.

Bit 1

Lock Prevention.
Bit 1 = 1 prevents attempts by applications software to lock registers of Group 1 by setting 3?5.11H, Bit 7 = 1.

Bit 0

Lock vertical timing.
Bit 0 = 1 locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by setting 3?5.11H, Bit 7 = 0.

7.7.5 WD90C30 CRT Controller Register Locking

Register locking is controlled by four bits. They are PR3 (5,1,0) and 3?5.11H(7) (i.e. IBM Vertical Retrace End Register Bit 7 controlled by Index register 11). When 3?5.11H Bit 7 is "1", CRT controller registers (R0-7) are write-protected per VGA definition. For more information on the five groups and their locking schemes, refer to the following sections.

All Port and Index addresses are in hex.

- **Group 0**

  These registers are locked if PR3(5) = 1 OR 3?5.11(7) = 1.

  3?5 Index 00 - Horizontal Total Characters per scan

  3?5 Index 01 - Horizontal Display Enable End

  3?5 Index 02 - Start Horizontal Blanking

  3?5 Index 03 - End Horizontal Blanking

  3?5 Index 04 - Start Horizontal Retrace

  3?5 Index 05 - End Horizontal Retrace

- **Group 1**

  These registers are locked if PR3(1) = 0 AND 3?5.11(7) = 1.

  3?5 Index 07 (Bit 6) - Vertical Display Enable End Bit 9

3?5 Index 07 (Bit 1) - Vertical Display Enable End Bit 8

3?5 Index 0E (Bit 1) - Vertical Display Enable End Bit 10

- **Group 2**

  These registers are locked if PR3(0) = 1 OR 3?5.11(7) = 1.

  3?5 Index 06 - Vertical Total

  3?5 Index 07 (Bit 7) - Vertical Retrace Start Bit 9

  3?5 Index 07 (Bit 5) - Vertical Total Bit 9

  3?5 Index 07 (Bit 3) - Start Vertical Blank Bit 8

  3?5 Index 07 (Bit 2) - Vertical Retrace Start Bit 8

  3?5 Index 07 (Bit 0) - Vertical Total Bit 8

  3?5 Index 09 (Bit 5) - Start Vertical Blank Bit 9

  3?5 Index 3E (Bit 0) - Vertical Total Bit 10

  3?5 Index 3E (Bit 2) - Vertical Retrace Start Bit 10

  3?5 Index 3E (Bit 3) - Start Vertical Blank Bit 10

- **Group 3**

  These registers are locked if PR3(0) = 1.

  3?5 Index 10 - Vertical Retrace Start

  3?5 Index 11 [Bits(3:0)] - Vertical Retrace End

  3?5 Index 15 - Start Vertical Blanking

  3?5 Index 16 - End Vertical Blanking

- **Group 4**

  This register is locked if PR3(5) = 1.

  CRTC mode control register 17(Bit 2) - Selects divide-by-two vertical timing.

7.7.6 PR4 - Video Control Register, Read/Write Port = 3CFH, Index = 0EH

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$ / Display Enable
6	PCLK=VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256-color Shift Register Control

Bit 7

$\overline{\text{BLANK}}$ / Display Enable.
This bit controls the output signal $\overline{\text{BLANK}}$. Normally in the VGA mode, $\overline{\text{BLANK}}$ is used by the external video DAC to generate blanking. If this Bit = 1, the $\overline{\text{BLANK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tristate outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLANK}}$.

Bit 4

Tri-state memory control outputs.
The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to "1".

Bit 3

Override CGA Enable Video Bit.
Overrides the CGA "enable video" Bit 3 of mode register 3D8H, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to "1". Power-on-reset causes no override.

Bit 2

Set to 1 to lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode.
It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3COH/3C1H change to write-only mode if the EGA compatibility bit is set. Setting this bit to "1" also disables reading PR0 through PR5. In VGA mode [PR(4) Bit 1 is zero] 3C0 register is read/write while 3C1H register is read only, per the Attribute Controller Register's definitions.

Bit 0

Extended Shift Register Control.
This bit should be set to "1" to select for extended 256-color modes (IBM Mode 13 is not included).

7.7.7 PR5 - General Purpose Status Bits, Read/Write Port = 3CFH, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are read/write bits and cleared to zero by reset. They provide lock or unlock capability for PR registers PR0 through PR4. The PR0 through PR4 registers are unlocked when "X5H" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register Bits 4 through 8. Setting PR(4) Bit 1 to "1", read protects registers PR0 through PR5.

Bit 7	CNF(7) [READ ONLY]
Bit 6	CNF(6) [READ ONLY]
Bit 5	CNF(5) [READ ONLY]
Bit 4	CNF(4) [READ ONLY]
Bit 3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to zero by reset. They control writing to PR registers PR0 through PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected
1 0 1	Write enabled

7.7.8 PR10 Unlock PR11-PR1A Read/Write Port = 3?5H, Index = 29H

This register is read/write and cleared to zero by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10-PR1A. Bits 7 and 3 enable register read operation for PR10 - PR1A. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR1A.

BIT	FUNCTION
7	PR10-PR1A - Read Enable Bit 1
6:4	PR10(6:4) - Scratch Pad
3	PR10-PR1A - Read Enable Bit 0
2:0	PR11-PR1A - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

7.7.9 PR11 EGA Switches, Read/Write Port = 3?5H, Index = 2AH

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4/General Purpose
6	EGASW3/General Purpose
5	EGASW2/General Purpose
4	EGASW1/General Purpose
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA Configuration Switches SW4-SW1.
These read/write bits from corresponding memory data bus pins MD(15:12) are latched internally at power-on-reset with either pull-up or pull-down external resistors. Pulling-up MD(15:12) causes PR11(7:4) to be latched high. These bits can be read as Bit 4 of Port 3C2H if the EGA compatibility bit [PR4(1)] has been set to "1". Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows. These bits can be used as General Purpose scratch bits.

WRITE		READ
3C2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are read/write and cleared to zero at power-on-reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select.
This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer Screen Control.
Setting PR11(1) to "1" prevents modification of the following bits in the Graphics Controller as well as the Sequencer:

Graphics Controller	3CF.05H bits (6:5)
Sequencer	3C5.01H bits (5:2)
Sequencer	3C5.03H bits (5:0)

Although the internal functions selected by the graphics controller and sequencer bits are locked by setting PR11 Bit 1 to "1", they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 Dots.
Setting this bit to "1" prevents modification of the Clocking Mode Sequencer Register 3C5.01H, Bit 0. Although eight or nine character timing is locked by setting PR11 Bit 0 to "1", the 3C5.01H Bit 0 appears unlocked to the system processor during read operations.

7.7.10 PR12 Scratch Pad, Read/Write Port = 3?5H, Index = 2BH

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

7.7.11 PR13 Interlace H/2 Start, Read/Write Port = 3?5H, Index = 2CH

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to "1". All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04H) and Horizontal Total Register (3?5.00H):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05H).

7.7.12 PR14 Interlace H/2 End, Read/Write Port = 3?5H, Index = 2DH

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to "0" by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bit 7

Enable IRQ.
This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to "0". This bit should not be set to "1" in MICRO CHANNEL operation.

Bit 6

Vertical Double Scan.
This bit should be set to "1" when emulating EGA on PS/2 display. Setting this bit to "1" causes the CRTC's Vertical Displayed Line Counter and Row Scan Counter to be clocked by divide-by-two horizontal timing, if vertical sync polarity (3C2H Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: N=2(n+1).

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced Mode.
Setting this bit to "1" selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09H] = 0XX00000. Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 End Bits (4:0).
Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

7.7.13 PR15 Miscellaneous Control 1, Read/Write Port = 3?5H, Index = 2EH

BIT	FUNCTION
7	Read 46E8 Enable
6	High VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8H.
This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to "1" enables I/O Port 46E8H to be read, regardless of the state of its own Bits 3 and 4 and of Port 102H, Bit 0 (sleep bit). Only Bits (4:0) of Port 46E8H are readable; Bits (7:5) are "0".

Bit 6

High VCLK.
Setting this bit to "1" adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency. This bit should be set to "1" if: (MCLK in MHz / VCLK in MHz) equal to 1.5. This bit also should be set to "1" in all extended 256-color modes.

Bit 5

Latched VCLK1 and VCLK2.
This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to "1" causes outputs VCLK1 and VCLK2 to equal Bits 2 and 3 of I/O write register (Miscellaneous Output Register) at 3C2H, respectively.

Bit 4

Select MCLK as Video Clock.
Setting this bit to "1" causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility.
This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to "1" if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to "1" causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing. Setting this bit to "1" also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing.
Setting this bit to "1" forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to "1" if 132 character mode timing is selected (see description of PR2). Setting this bit to "1" in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to "1", it redefines the Character Map Select Register (3C5.03H). One of eight 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by Bits (2:0) of this register while the map selection is determined by the Bits (4:3). A pair of adjacent 8K character maps in Planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by Bit 3 of the attribute code.
The character attribute, Bit 3, in conjunction with Bits 3 and 4 of the Character Map Select Register (3C5.03H), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE:
The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to "1" before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to "1" internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to select between two types of display enable timings available at output pin $\overline{\text{BLANK}}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0 = $\overline{\text{BLANK}}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{\text{BLANK}}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable Border.
Setting this bit to "1" forces the video outputs to "0" during the interval when border (overscan) color would be active.

7.7.14 PR16 Miscellaneous Control 2, Read/Write Port = 3?5H, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7

Lock External 46E8H Register.
Setting this bit to "1" causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to port 46E8H.

Bits (6:5)

CRTC Address Counter Width.
Power on reset clears these bits to "0". These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set "1" to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bits (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter Bits CA(17) and CA(16), respectively, and the two-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06H(1) to "1", setting 3C5.04H(1) to "1", selecting extended memory, and setting 3C5.04H(3) to "0" to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2H(5)] to select between two pages of memory, by controlling video RAM address "0", regardless of the Memory Size Bits PR1(7:6).

17

Bit 1

VGA Memory Mapping.
Setting this bit to "1", selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size Bits PR1(7:6).

Bit 0

Lock RAMDAC Write Strobe (3C6H - 3C9H).
0 = Normal operation.
1 = Output $\overline{WPLT}$ to be forced to "1", disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C30, is also protected from the modification, but may still be read at the Port 3C7H.

7.7.15 PR17 Miscellaneous Control 3, Read/Write Port = 3?5H, Index = 30H

BIT	FUNCTION
7:6	Reserved
5	Character Clock Period Select
4	PCLK = $^{VCLK}/_{2}$
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bits (7:6)

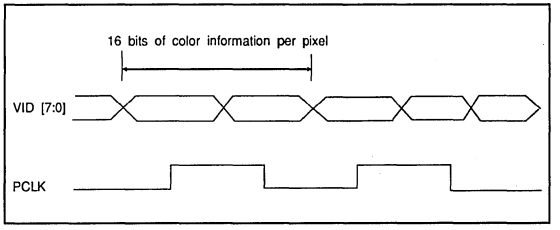
Reserved.

Bit 5:

Character Clock Period Select.
When PR2 (3CF.0CH), Bits 4:3 = "11", then setting this bit to "0" selects the six-dot font. Setting this bit to "1" selects the ten-dot font. Otherwise, this bit has no effect.

Bit 4

PCLK = $^{VCLK}/_{2}$.
Setting this bit to "1" forces PCLK = $^{VCLK}/_{2}$. This control is useful for interface with high color RAM-DAC as follows:



Bit 3

Map Out 4K of BIOS ROM.
Setting this bit to "1" disables access of the BIOS ROM in the system address range C600:0H through C6FF:FH. Power on reset sets this bit to "0".

Bit 2

Enable 64K BIOS ROM.
Setting this bit to "1" enables access of the BIOS ROM in the system address range C000:0H through CFFF:FH. Power on reset sets this bit to "0".

Bit 1

Hercules Compatibility.
Setting this bit to a "1" locks Hercules compatibility register (I/O Port 3BFH). Power on reset sets this bit to "0".

Bit 0

Map Out 2K of BIOS ROM.
Setting this bit to "1" disables access of the BIOS ROM in the system address range C600:0H through C67F:FH. Power-on-reset sets this bit to "0".

7.7.16 PR18 CRTC Vertical Timing Overflow, Read/Write Port = 3?5H, Index = 3EH

These bits combined with other vertical timing overflow bits in CRTC constitutes an 11-bit vertical timing control. These bits are set to zero at power-on-reset.

BIT	FUNCTION
7:5	Reserved
4	Line compare Bit 10
++3	Start vertical blank Bit 10
++2	Start vertical retrace Bit 10
**1	Vertical display enable end Bit 10
++0	Vertical total Bit 10
Note: ++ The bit is locked if PR3(0) = 1 OR the 3?5H Index 11H Bit 7 = 1 ** The bit is locked if PR3(1) = 0 AND the 3?5H Index 11H Bit 7 = 1	

7.7.17 PR19 Video Signature Analyzer Control Read/Write Port = 3?5H, Index = 3FH

BIT	FUNCTION
7:4	Reserved
3	Signature read enable
2	Enable video input
1	Preload control
0	Enable/Status bits

Bits (7:4)

Reserved

Bit 3

Signature Read Enable.
Set this bit to "1" in order to read signature analyzer results from 3?5H, Index 20H and 21H.

Bit 2

Enable Video Input.
This bit is used for self-test. Set this bit to "1" for self-testing. The video input to the signature analyzer is disabled. Set this bit to "0" to enable video input for signature analyzer.

Bit 1

Preload Control.
Setting this bit to "0" will preload the Signature Analyzer Result Register (3?5H, Index 20H and 21H) with 0001H. Set this bit to "1" for normal operation.

Bit 0

Enable/Status Bits.
Setting this bit to "1" will enable the signature analyzer to collect signature on video input. This bit indicates the status when read back.
0 = Finished (or not enabled)
1 = Busy

7.7.18 PR1A Shadow Register Control, Read/Write Port = 3?5H, Index = 3DH

Bits (7:4)

Reserved.

Bits 3

I/O Read Select.
0 = Select actual CRTC registers for read
1 = Select shadow CRTC registers for read

Bits (2:0)

Shadow Lock.
Setting Bits 2:0 = "101" will lock all the shadowed register bits. This lock overrides any locks. Please refer to the shadow register description for details.

7.7.19 PR20 Unlock Sequencer Extended Registers, Read/Write Port 3C5H, Index = 6H, (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer Index reads as six bits.

7.7.20 PR21 Display Configuration Status and Scratch Pad Bits Register, Bits 7:4 Read/Write Bits 3:0 Read Only, Port 3C5H, Index = 7H

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2H Bit 0
2	Status of PR2 Bit 6
1	Status of PR4 Bit 1
0	Status of PR5 Bit 3

Bits (7:4)

Scratch Pad Bits.
Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is "1111".

Bit 3

Status of 3C2H Bit 0.
Reflects the setting of the I/O address select bit in the Miscellaneous Output Register. A "1" indicates CGA (3Dx) addresses have been selected by this read-only bit, while a "0" indicates MDA (3Bx) addresses have been selected.

Bit 2

Status of PR2 Bit 6.
Reflects the setting of the VGA/6845 select bit in PR2 (3CFH Index CH). A "1" indicates 6845 compatibility has been selected by this read-only bit, while a "0" indicates VGA or EGA compatibility has been selected.

Bit 1

Status of PR4 Bit 1.
Reflects the setting of the VGA/EGA select bit in PR4 (3CFH Index EH). A "1" indicates EGA compatibility has been selected by this read-only bit, while a "0" indicates VGA was selected.

Bit 0

Status of PR5 Bit 3.
Reflects the setting of the Analog/TTL status bit in PR5 (3CFH Index FH). A "0" indicates an analog monitor was selected by this read-only bit, while a "1" indicates a TTL-type monitor was selected.

7.7.21 PR22 Scratch Pad Register, Read/Write Port = 3C5H, Index = 8H

Bits (7:0)

Scratch pad bits.

7.7.22 PR23 Scratch Pad Register, Read/Write Port = 3C5H, Index = 9H

Bits (7:0)

Scratch pad bits.

7.7.23 PR30 Memory Interface, Write Buffer and FIFO Control Register, Read/Write Port = 3C4H, Index 10H

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7:6	Write Buffer Control
5	32-bit or 16-bit Memory Data Path
4	Disable 16-bit CPU Interface for Unchain Mode
3	Two-level FIFO
2	Four or Eight-level FIFO
1:0	Display FIFO control

Bits (7:6)

Write Buffer Control.
Bits 6 and 7 determine the depth of the write buffer. PR31 Bit 2 must be set to "1" for these two bits to have any effect.

BITS 7 6	FUNCTION
00	Write buffer is one level deep
01	Write buffer is two levels deep
10	Write buffer is three levels deep
11	Write buffer is four levels deep

Bit 5

Memory Data Path.
When set to "1", the display memory data path becomes 16-bits wide. Otherwise, the data path is 32-bits wide.

Bit 4

0 = Normal conditions
1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3

Two-level FIFO.
0 = The FIFO is four or eight levels deep, depending on Bit 2 of this register.
1 = The FIFO is two levels deep, regardless of Bit 2.

Bit 2

Four or Eight-Level FIFO.
0 = FIFO set to eight levels deep.
1 = FIFO set to four levels deep.

Bits (1:0)

Display FIFO Control
These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to "01" to accommodate most applications. These bits have no effect in any text mode. They are locked into "00" internally when a text mode is set.

BIT	FUNCTION	
00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

7.7.24 PR31 System Interface Control, Read/Write Port = 3C5H, Index = 11H, Reset State = 00

This register provides the control bits for the system interface. This register should be set during the post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

Read/Write Offset Enable.
0 = Normal (Refer to PR0A and PR0B definitions).
1 = The offset register PR0-A will be added to CPU address for read cycles, while PR0-B will be added for write cycles.

Bit 6

Turbo Mode for Blanked Lines.
1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.
0 = Normal.

Bit 5

Turbo Mode for Text.
1 = For improved text mode performance.
0 = Normal.

Bits (4:3)

CPU Read RDY Release Controls 1,0.
These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it takes longer to complete the read cycle.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle
01 = RDY is inserted 1MCLK before the end of a CPU memory cycle.
10 = RDY is inserted 2MCLK before the end of a CPU memory cycle.
11 = RDY is inserted 1MCLK after the end of a CPU memory cycle.

For 10 MHz or slower systems, the "01" setting is recommended. For 12 MHz or faster systems, the "11" setting is recommended.

Bit 2

Enable Write Buffer.
1 = Write buffer is enabled. This will greatly reduce the number of wait states for CPU writes to display memory.
0 = Write buffer disabled.

Bit 1

Enable 16-bit I/O Attribute Controller.
If Bit 1 and Bit 0 are both set to "1", then the Attribute Controller (3C0H/3C1H) is configured for 16-bit access. The index is at 3C0H, while the data is at 3C1H, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for eight-bit cycles. $\overline{IOCS16}$ is asserted for all cycles to 3C0H or 3C1H.

Bit 0

Enable 16-bit I/O Operations.
1 = Enables 16-bit access to the CRTC (3?4H/3?5H), Sequencer (3C4H/3C5H), and Graphics Controller (3CEH/3CFH). The output $\overline{IOCS16}$ will be active for any I/O read or write to these addresses.
0 = The VGA I/O is eight-bits.

7.7.25 PR32 Miscellaneous Control 4, Read/Write Port = 3C5H, 3C5H Index = 12H, Reset State = 00

This register provides control for several different features. Some of these features help to support Genlock of the WD90C30 to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow Read Back in Backward compatible Modes
0	Force Standard CPU Addressing in 132-column Mode

Bit 7

Enable External Sync Mode.
0 = Normal operation mode.
1 = $\overline{EXVID}$ is configured to input external Horizontal Sync, and $\overline{EXPCLK}$ inputs external Vertical Sync. The external $\overline{HSYNC}$ signal also synchronizes the character clock timing. In this configuration, $\overline{EXVID}$ and $\overline{EXPCLK}$ do not control the VID 7:0 and PCLK output buffers, but they are used to genlock the WD90C30 to another display controller.

Bit 6

Disable Cursor Blink.
0 = Blink enabled
1 = The text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

USR1 Function Select.
0 = Causes the USR1 output to reflect the state of Bit 4, which can be used to control new features that the system board designer may wish to add.
1 = The USR1 output is slected by PR35 Bits 5, 4, and 3. See PR35 description.

Bit 4

USR1 Control.
Controls the USR1 output when selected by Bit 5.

Bit 3

USR0 Function Select.
0 = Causes the USR0 output to reflect the state of Bit 2, which can be used to control new features that the system board designer may wish to add.
1 = The USR0 output is selected by PR35 Bits 2, 1, and 0. See PR35 description.

Bit 2

USR0 Control.
Controls the USR0 output when selected by Bit 3.

Bit 1

Read Backward in Compatible Modes.
When set to "1", this bit allows reading of those registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

132-Column Mode.
When set to "1", the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

7.7.26 PR33 DRAM Timing and Zero Wait State Control Register, Read/Write Port = 3C5H, Index = 13H

Bits (7:6)

These two bits control the operation of the $\overline{0WS}$ output pin. $\overline{OWS}$ is disabled if PR31 bit 2 = 0 (Write Buffer is off).

BIT 7	BIT 6	FUNCTION
0	0	$\overline{0WS}$ = 0 if the internal write is buffer-ready.
0	1	$\overline{0WS}$ = 0 if the internal write buffer is ready AND the memory address is decoded.
1	0	$\overline{0WS}$ = 0 if the internal write buffer is ready AND memory address is decoded AND $\overline{MWR}$ = 0.
1	1	$\overline{0WS}$ = 0 if the condition "10" is true OR I/O write to the WD90C30 is occurring.

Bit 5

Reserved

Bits (4:3)

These two bits control the $\overline{CAS}$ timing.

BIT	VALUE	FUNCTION
4-3	00	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (4-7) ns. $\overline{CAS}$ high is 1 Mclock - (4-7) ns.
4-3	01	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (8-14) ns. $\overline{CAS}$ high is 1 Mclock - (8-14) ns.
4-3	10	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1.5 Mclocks. $\overline{CAS}$ high is 0.5 Mclocks.
4-3	11	Reserved.

Bit 2

BIT	VALUE	FUNCTION
2	0	$\overline{CAS}$ cycle starts 2.5 Mclocks after $\overline{RAS}$ low.
2	1	$\overline{CAS}$ cycle starts 1.5 Mclocks after $\overline{RAS}$ low.

Bits (1:0)

These two bits control $\overline{RAS}$ precharge. Refer to DRAM timing adjustments in Section 6.0.

BIT	VALUE	FUNCTION
1-0	00	$\overline{RAS}$ high is 2-1/2 mclocks plus a 4-7 ns. delay.
1-0	01	$\overline{RAS}$ high is 3 Mclocks wide.
1-0	10	$\overline{RAS}$ high is 2 Mclocks wide.
1-0	11	$\overline{RAS}$ high is 2-1/2 Mclocks.

7.7.27 PR34 Video Memory Mapping Register, Read/Write Port = 3C5H, Index = 14H

Bits (7:0)

BITS	FUNCTION
7-4	Reserved.
3-0	These four bits are compared with the CPU address A_[23:20] as part of the video memory address decoding. This allows the VGA to be mapped into any 1 Mbyte CPU memory space. This register will not affect the $\overline{EBROM}$ and $\overline{ROM16}$ decoding. $\overline{EBROM}$ and $\overline{ROM16}$ will still decode at A_[23:20] = 0H. Used with the correct setting of PR1, Bits 5 and 4, this register supports virtual VGA applications. These four bits are set to "0" at power-on reset.

7.7.28 PR35 USR0, USR1 Output Select Register, Read/Write Port = 3C5H, Index = 15H

This register determines which internal signals can be observed through USR0 and USR1 output pins. This is for debug purposes and may be useful for using internal signals to control external functions. PR35, Bits 5 and 3, must be set to "1" for this register to have any effect.

Bits (7:6)

Reserved.

Bits (5:3)

5, 4, 3	USR1 =
0 0 0	"1", if WD90C30 is fetching fonts from DRAM
0 0 1	"1", if WD90C30 is fetching graphics data from DRAM
0 1 0	"1", if the internal write buffer is ready
0 1 1	"1", if a CPU write cycle is occurring
1 0 0	"0", if a CPU write cycle is not caused by write buffer
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

Bits (2:0)

2, 1, 0	USR0 =
0 0 0	"1", if I/O address is decoded
0 0 1	"1", if WD90C30 is fetching character attributes from DRAM
0 1 0	"0", if the internal write buffer is not empty
0 1 1	"1", if CPU read cycle is occurring
1 0 0	"0", if a write buffer cycle is occurring
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

7.8 INTERNAL I/O PORTS

7.8.1 AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7:5	Unused
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bits (7:5)

Unused.

Bit 4

Setup.
Puts WD90C30 into setup mode where only I/O Port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses.

Bits (2:0)

BIOS ROM Page Select.
On I/O accesses to 46E8H, $\overline{\text{EBROM}}$ becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C30 also provides an alternative Port 3C3H instead of Port 46E8H. If a pull-down resistor is connected to MD(9) during power on reset (CNF9 = 0), then Port 3C3H will be decoded instead of Port 46E8H to support the same functions described above. Otherwise, Port 46E8H is selected and decoded.

7.8.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7:1	Unused
0	Wakeup VGA

Bits (7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower three address bits are decoded for this port and WD90C30 must be in Setup mode. VGA Enable Sleep bit or Programmable Option Select (POS) Register 102H Bit 0 is used to awaken the WD90C30 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, Bit 4 of the partially decoded internal I/O Port 46E8H is set to "1" before accessing the I/O Port 102H. In MCA mode, when the VGASETUP ($\overline{\text{EIO}}$) signal pin is active low, the WD90C30 is in setup mode and Port 102H can be accessed.

7.9 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C30. However, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals required by the RAMDAC are provided by the WD90C30. Setting PR(16) Bit 0 to a "1" forces $\overline{\text{WPLT}}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL Address Port (Write)	Read/Write Port
3C7H	PEL Address Port (Read)	Read Only Port
*3C7H	*DAC State (Read Only)	* If Bits 0/1 = 1, DAC in read operation. When Bits 0/1 = 0, DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL Mask (Read/Write)	Not to be written by application code or color look-up table will be changed.
3C9H	PEL Data Register (Read/Write)	Three successive read/write bytes.

* This port is internal to the WD90C30.

TABLE 17. VIDEO RAMDAC PORTS

7.10 WD90C30 CONFIGURATION REGISTER BITS CNF(18:0)

Memory Data Lines (18:0) are used to input configuration data at power-on reset (RST) by pull-up or pull-down resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on. All MD(18:0) are internally pulled up by 50 ohm resistors. The following table lists the non-writable configuration bits.

BIT	FUNCTION
18	Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ input
17	
16	64K by 16 or 256 K by 4 DRAM select
15 -12	EGA Switches
11	A23 - A20 Connection Select
9	46E8H/3C3H Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	AT/MCA Bus Select

CNF(18)

A 4.7K pull-down resistor on Pin MD(18) sets CNF(18) = 0. Otherwise the internal pull-up will set CNF(18) = 1.

0 = $\overline{\text{ROM16}}$ configured as $\overline{\text{EXBLANK}}$ input.

1 = Normal $\overline{\text{ROM16}}$ operation. $\overline{\text{ROM16}}$ is an output.

CNF(16)

A 4.7K pull-down resistor on pin MD(16) sets CNF(16) = 0. Otherwise, the internal pull-up will set CNF(16) = 1.

0 = WD90C30 is interfacing with a 64K by 16 DRAM.

1 = WD90C30 is interfacing with a 256K by 4 or 256K by 16 DRAM.

CNF(15:12)

EGA configuration switches SW4-SW1.
Pulling up MD(15:12) causes PR11(7:4) to be latched high. Pulling down MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as Bit 4 of Port 3C2H (as on a standard EGA) if the EGA compatibility bit [PR4(1)] has been set to "1". Selection of which bit to read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows.

WRITE		READ
3C2 Bit 3	3C2 Bit 2	3C2 Bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF(11)

A 4.7K pull-down resistor on the Pin MD8 sets CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C30 to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).

If there is no pull-down resistor on MD8, the CNF(11) will be set to "1" by the internal pull-up. Pins A(23:17) should be connected to AT bus signals LA(23:17). LA(23:17) are internally latched by ALE signal.

CNF(10)

A 4.7K pull-down on Pin MD10 sets CNF(10) = PR1(1) = 1. Upon power-up, the pin ROM16 is enabled for 16-bit BIOS ROM decoding. Otherwise, the internal pull-up will set CNF(10) = PR1(1) = 0. To enable the 16-bit BIOS, PR1(1) must be set to "1" by writing to Port 3CFH (Index 0BH) bit 1 and at the same time the CNF(1) must be "1". This bit is read/write at PR1(1).

CNF(9)

A 4.7K pull-down on Pin MD9 sets CNF(9) = 0. Then Port 03C3H will be selected as the VGA setup and enable register instead of Port 46E8H in the AT interface. Otherwise, the internal pull-up will set CNF(9) = 1. Port 46E8H will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

CNF(8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power-on-reset from memory data bus Pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0FH). Also, CNF(8) is unaffected by writing to PR5 (3CF.0FH). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF(7:4)

General Purpose Status Bits.
Bits CNF(7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0FH) positions (7:4). These bits are unaffected by writing to PR5(3CF.0FH). Pulling down MD(7:4) causes CNF(7:4) to be latched high.

CNF(3)

Video Clock Source Control.
This bit cannot be written or read as I/O port. Pulling up MD(3) causes CNF(3) to be latched high. It configures WD90C30 pins VCLK1 and VCLK2 as inputs or outputs.

0 = For inputs.
1 = For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to Port 3C2H. This load pulse may be inhibited by setting PR11(2) = 1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs are equal to Bits 2 and 3 of the Miscellaneous Output Register at 3C2H when PR15 Bit 5 is set to "1".

CNF (2)

Bus Architecture Select.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0 = Micro Channel architecture
1 = AT BUS architecture

Selecting CNF(2) will change pinout definition between AT BUS and Micro Channel bus. (See Signal Description.)

PC-AT BUS	I/O	MICRO CHANNEL	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0H	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF (1)

ROM Configuration.
When set to "0", the WD90C30's data bus buffer controls are configured for one ROM (eight bits). An internal pull-up on MD(1) sets this bit to "0" at power-on-reset.

0 = PR1(1) can not be set high. This bit can not be written or read.

1 = The WD90C30's data bus buffer controls are configured for 16-bits (as with two ROMs). Setting CNF(1) to 1 enables the $\overline{\text{HTL}}$ output pin. With an 8-bit system interface, address bit A(0) = 0, selects the even ROM and A(0)=1 selects the odd ROM. With a 16-bit system interface, CNF(1) and PR1(1) must be set to one to enable $\overline{\text{ROM16}}$.

CNF (0)

BIOS ROM Mapping.
If set to "1", the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 Kohm pull-down resistor may be used to set this bit to "1" on power-on-reset.

This bit is read/write at PR1(0).

A.0 APPENDIX A - EGA MODE

A.1 EGA MODE ENTRY

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. "Not Used" bits should be set to "0" unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register Bit 8. Select logic "0" for a VGA-compatible PS/2 display or logic "1" for an EGA-compatible TTL monitor by using the appropriate pull-up or pull-down resistor on MD(11). (A pull-up resistor on MD11 causes CNF(8) to be latched with logic "0" for analog PS/2 compatible displays.) This status information signifies the type of monitor attached to the system and is available to the BIOS or application.
- Unlock all the PR registers.
- Program PR2(6) to "0" for EGA mode.
- Set PR4 Bit 1 to logic "1" for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on Pins MD(15:12). (A pull-up resistor causes logic "1" to be latched after power-on-reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O Port 3C2H Bit 4.
- If EGA mode is to be emulated on an IBM PS/2 analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force clock control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional).
  - Lock the PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3)=0; EGA TTL
    PR14(7)=1; Enable IRQ
    PR15(6)=1; Set Low Clock
    PR14(7)=1; Enable IRQ
  - Lock PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register Write, Port = 3C2H

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

REGISTERS	EGA	I/O PORT HEX
General Registers:		
Miscellaneous Output Register	WO	3C2
Input Status Register 0	RO	3C2
Input Status Register 1	RO	3?A
Feature Control Register	WO	3?A
Sequencer Registers:		
Sequencer Index Register	WO	3C4
Sequencer Data Register	WO	3C5
CRT Controller Registers:		
Index Register	WO	3?4
CRT Controller Data Register, except the following:	WO	3?5
Start Address High (Index=0CH)	RW	3?5
Start Address Low (Index=0DH)	RW	3?5
Cursor Location High (Index=0EH)	RW	3?5
Cursor Location Low (Index=0FH)	RW	3?5
Light Pen High, (Index=10H)	R	3?5
Light Pen Low, (Index=11H)	R	3?5
Graphics Controller Registers:		
Index Register	WO	3CE
Other Graphics Register	WO	3CF
Attribute Controller Registers:		
Index Register	WO	3CO*
Attribute Controller Data Register	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.

TABLE 18. EGA REGISTERS SUMMARY

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is "0".
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is "0".
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is "0".

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0, Read Port = 3C2H

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used.

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to "1".

Bits (3:0)

EGA: Not used = 1.

A.2.3 Input Status Register 1, Read Port = 3?AH

Bit 7

EGA: Not used.

Bit 6

EGA: Not used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1.

Bit 1

EGA: Not used.

Bit 0

EGA: Same as Input Status Register 1 Bit 0 definition in the VGA section.

A.2.4 Feature Control Register, Write Port = 3?AH

Bits (7:0)

EGA: Not used.

A.3 SEQUENCER REGISTERS, PORT = 3C5H

A.3.1 Clocking Mode Register, Index = 01H

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to zero.

Bit 0

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register, Index = 03H

Bits (7:4)

EGA: Not used.

Bits (3:2)

EGA: Character Map Select A.

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)

EGA: Character Map Select B.

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:
Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

A.3.3 Memory Mode Register, Index = 04H

Bits (7:3)

EGA: Not used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2:1) definition in the VGA section.

Bit 0

EGA: Alpha Mode Bit.
A logic "1" shows that Alpha mode is active and character map selection is enabled. A logic "0" disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS, PORT = 3?5H

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5H or 3D5H, for Monochrome or Color display modes, respectively.

A.4.1 Index Register, Port = 3?4H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address Index where the data is to be written.

A.4.2 Horizontal Total Register, Index = 00H

Bits (7:0)

EGA: Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register, Index = 03H

Bit 7

EGA: Not used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register, Index = 05H

Bit 7

EGA: This bit defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register, Index = 06H

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register, Index = 08H

Bits (7:5)

EGA: Not used.

Bits (4:0)

Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

A.4.7 Maximum Scan Line Register, Index = 09H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.8 Cursor Start Register, Index = 0AH

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor End Register, Index = 0BH

Bit 7

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.10 Vertical Retrace Start Register, Index = 10H - Write

(Light Pen High register, Index = 10H - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.11 Vertical Retrace End Register, Index = 11H - Write

(Light Pen Low register, Index = 11H - Read)

Bits (7:6)

EGA: Not used.

Bit 5

EGA: This bit enables the IRQ output buffer control if logic "0" is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic "1", the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic "0", the IRQ latch is reset and cleared to "0" if Bit 5 = 0. If it is logic '1", the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.12 Underline Location Register, Index = 14H

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.13 End Vertical Blanking Register, Index = 16H

Bits (7:5)
EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.14 Mode Control Register, Index = 17H

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS, PORT = 3CFH

A.5.1 Read Map Select Register, Index = 04H

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

BIT 2	BIT 1	BIT 0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register, Index = 05H

Bit (7:6)

EGA: Not used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS, PORTS = 3C0H/3C1H

A.6.1 Palette Registers, Index = 00H through 0FH

BIT	FUNCTION
7:6	Not used
5:0	Dynamic color selection

Bits (7:6)

EGA: Not used.

Bits (5:0)

EGA: Dynamic color selection. Logic "0" = Color deselection, and Logic "1" = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register, Index = 10H

BIT	FUNCTION
7:4	Not used
3:0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register, Index = 11H

BIT	FUNCTION
7:6	Not used
5:0	Overscan color for border

Bits (7:6)

EGA: Not used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic "0". The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register, Index = 12H

BIT	FUNCTION
7:6	Same as Color Plane Enable - VGA
5:4	Video Status Multiplexer
3:0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer as shown below:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register, Index = 13H

BIT	FUNCTION
7:4	Not used
3:0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (nine dots/character) image can be shifted by nine pixels. For all other graphics or alpha numeric modes, a maximum left shift of eight pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B .0 APPENDIX B - WD90C30 INTERFACES

The WD90C30 applications section is divided into various interfaces: processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes and technical briefs at the end of this data book will supplement the information provided in this section.

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B.1 WD90C30 INTERFACES

Figure 13 highlights the WD90C30 interfaces.

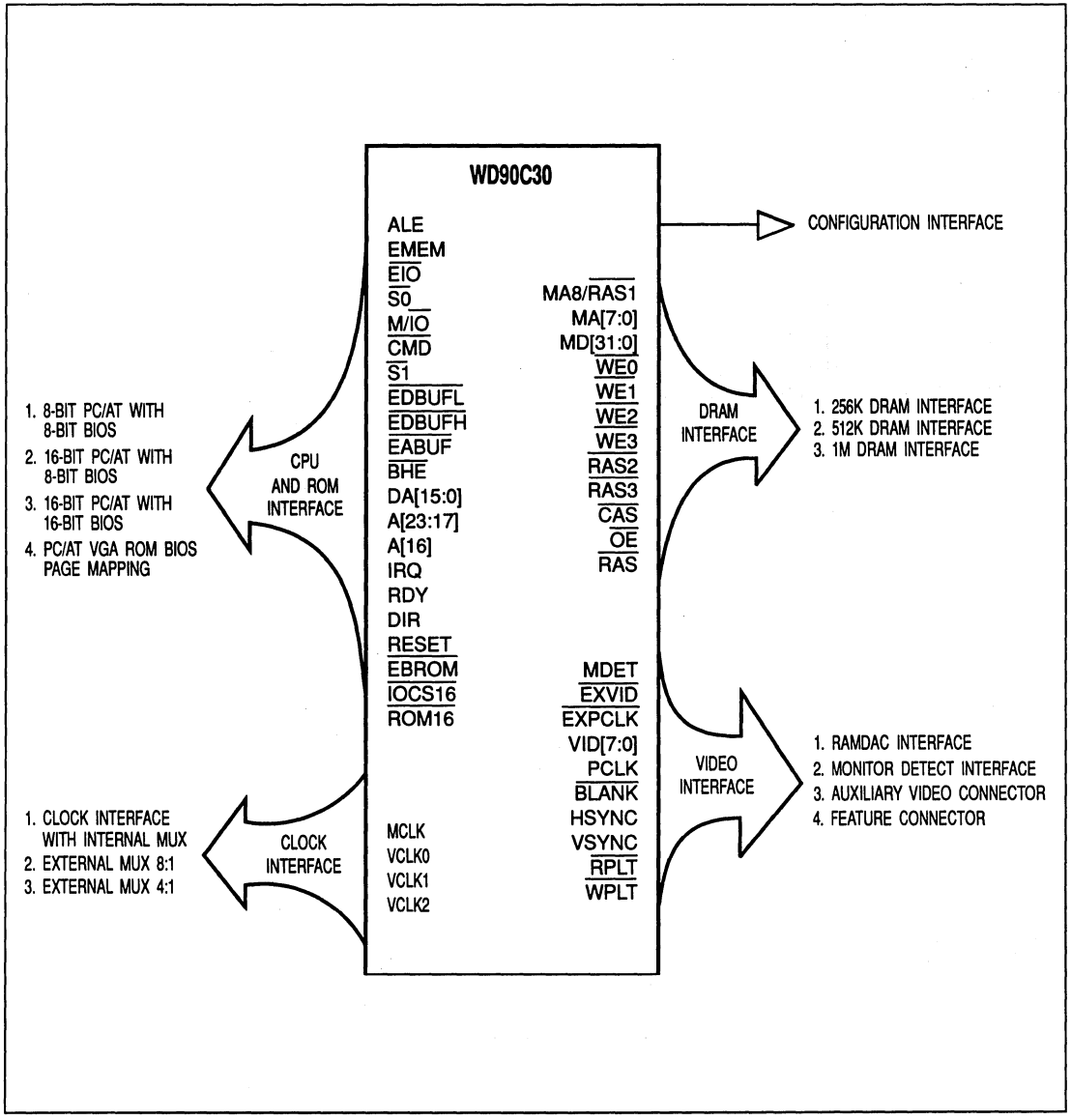

FIGURE 13. WD90C30 INTERFACES

B.2 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 14 shows a block diagram of the WD90C30 with eight-bit PC/AT interface using eight-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

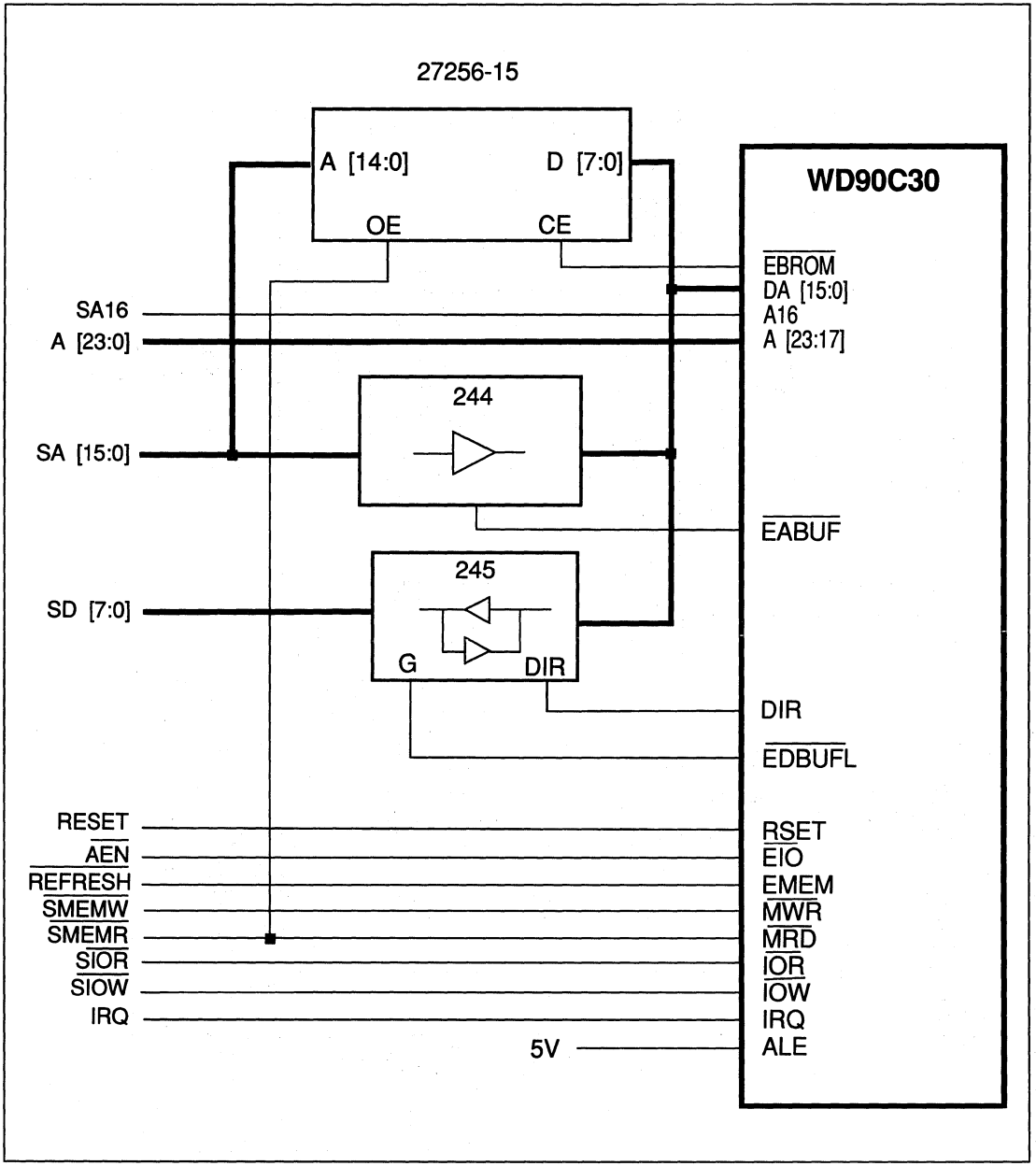

FIGURE 14. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

B.3 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 15 illustrates 16-bit PC/AT interface with an eight-bit BIOS using WD90C30. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown.

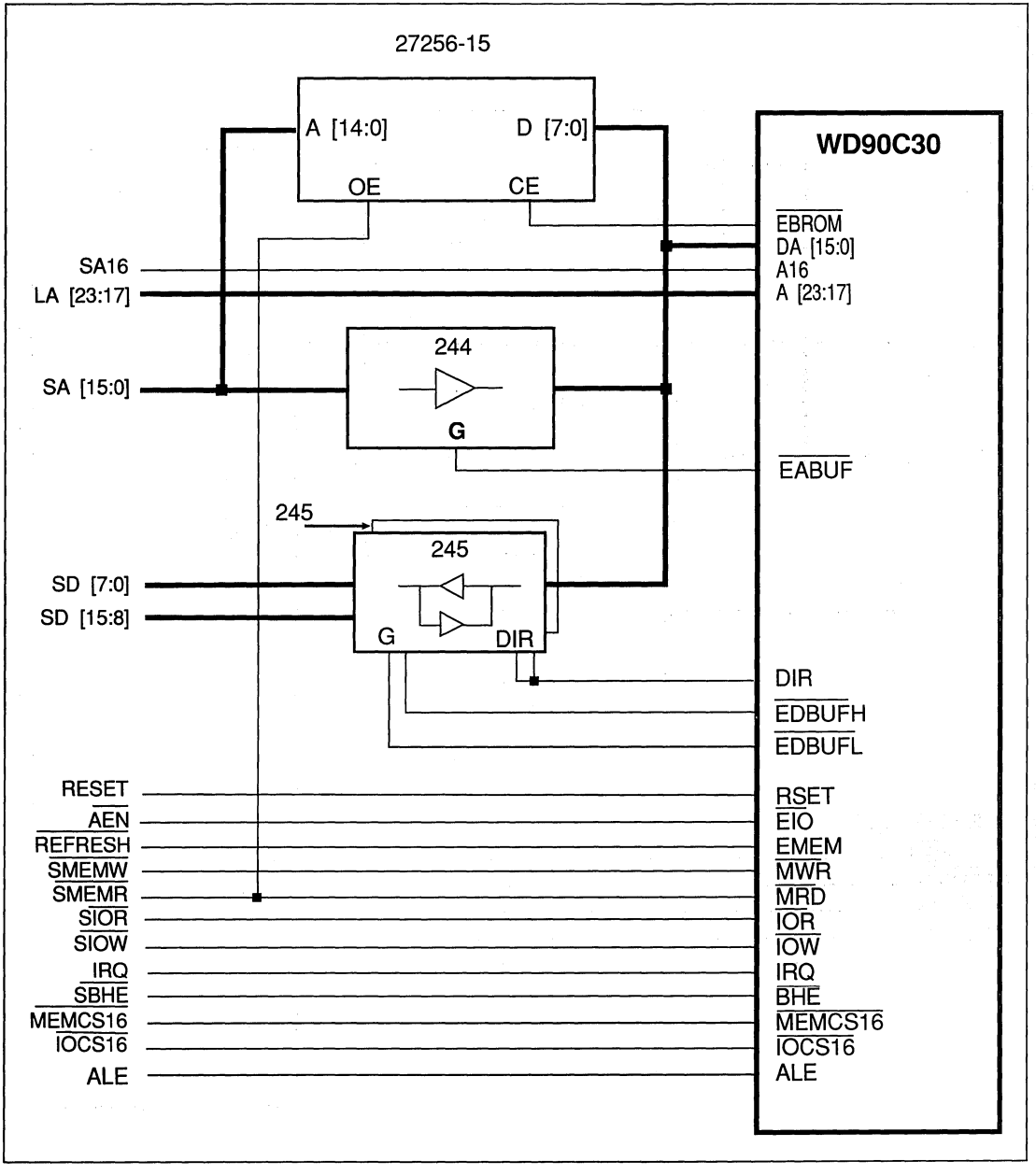

FIGURE 15. 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

B.4 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

Figure 16 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C30. The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds since SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 18 for 286-based systems.

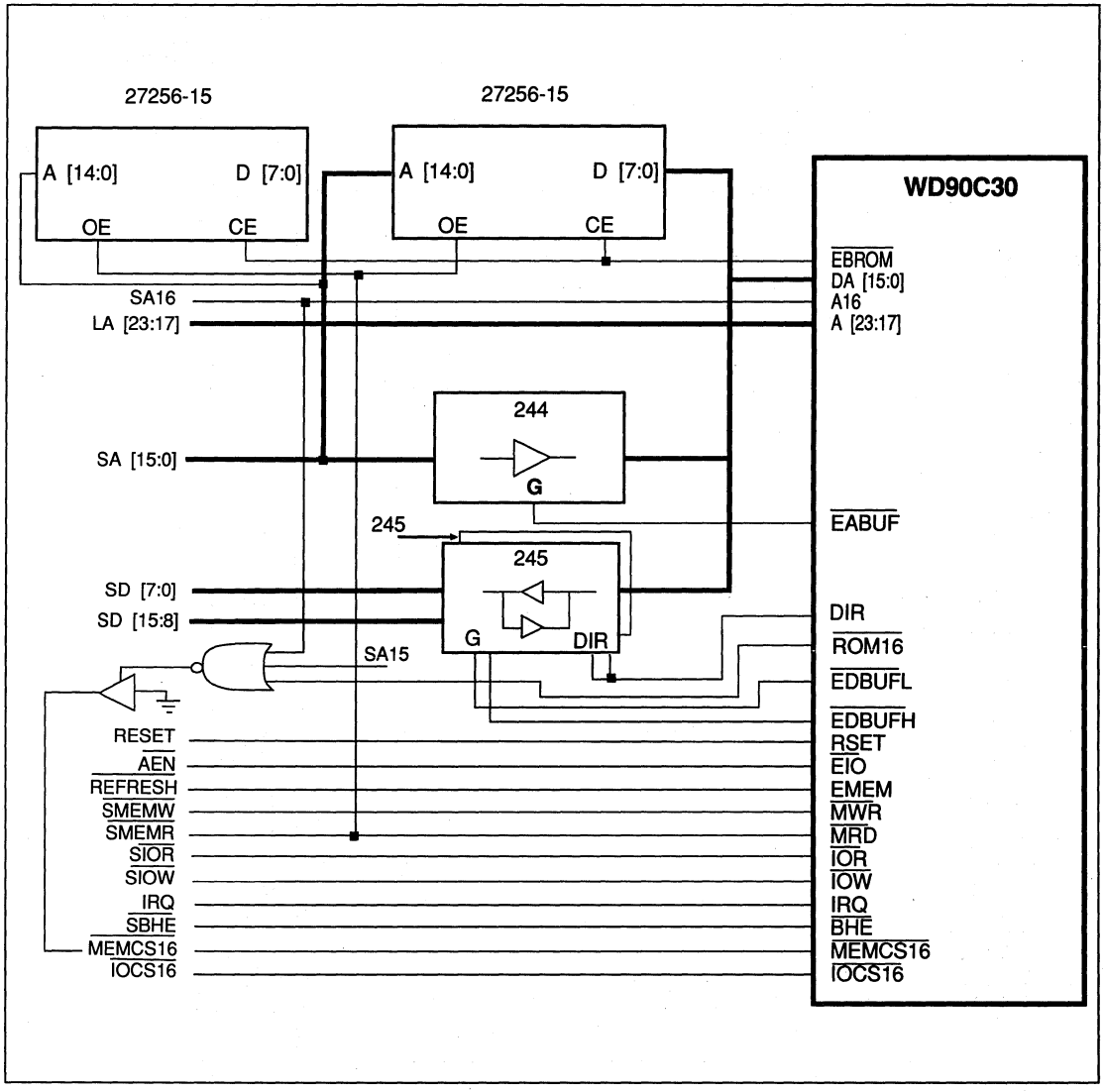

FIGURE 16. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

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B.5 16-BIT MICRO CHANNEL

Figure 17 illustrates the WD90C30 and 16-bit Micro Channel interface. 3C3.D0H is output of Port 3C3H Bit 0 VGA Subsystem Enable Register.

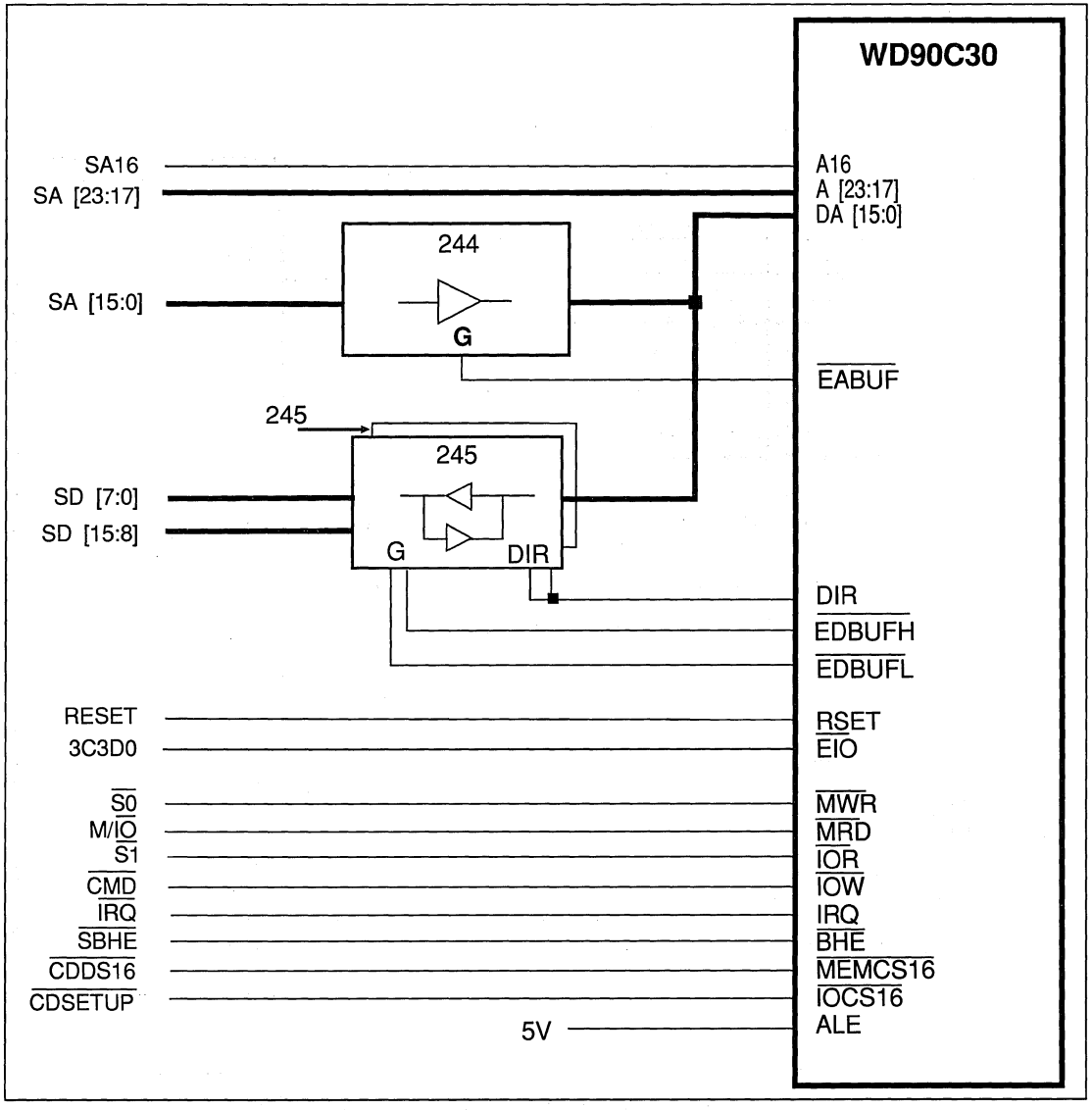
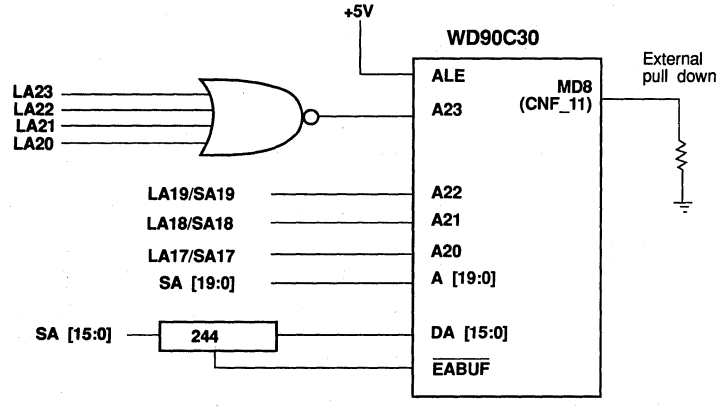


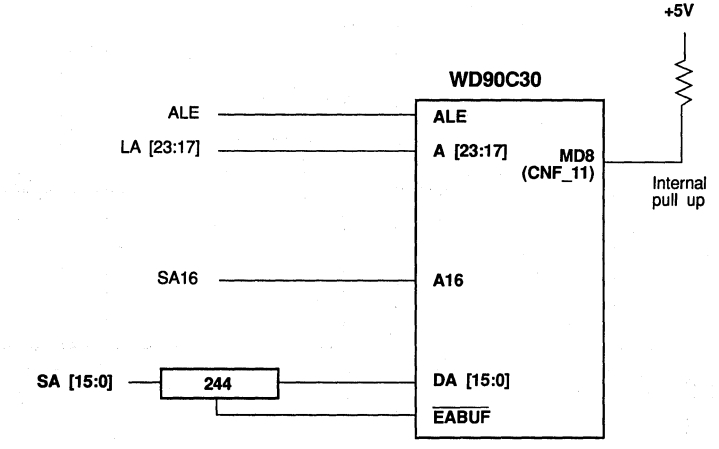
FIGURE 17. 16-BIT MICRO CHANNEL INTERFACE

B.6 WD90C30 INTERFACE FOR 286 OR 386 BASED SYSTEMS

For systems that do not meet the hold time of LA address valid from the falling edge of MEMR or MEMW, pull MD8 down and connect LA addresses and SA addresses as shown in the upper half of Figure 18. This applies to most 286 systems. Otherwise, connect LA addresses and SA addresses as shown in the lower half of Figure 18. This applies to most 386 systems.



Note: MD8 (CNF_11 is pulled down at power-on-reset. This configuration is recommended for interfacing with 8-bit and 16-bit AT buses. For an 8-bit interface, A23 should be connected to SA [19:17] on the AT bus. For a 16-bit interface, LA [23:17] must be connected to generate MEMCS16.



Note: MD8 (CNF_11) is pulled up internally at power-on-reset. This configuration is recommended for interface with a 16-bit AT bus only. LA [23:17] is internally latched by ALE.

FIGURE 18. WD90C30 INTERFACE FOR 286 OR 386-BASED SYSTEMS

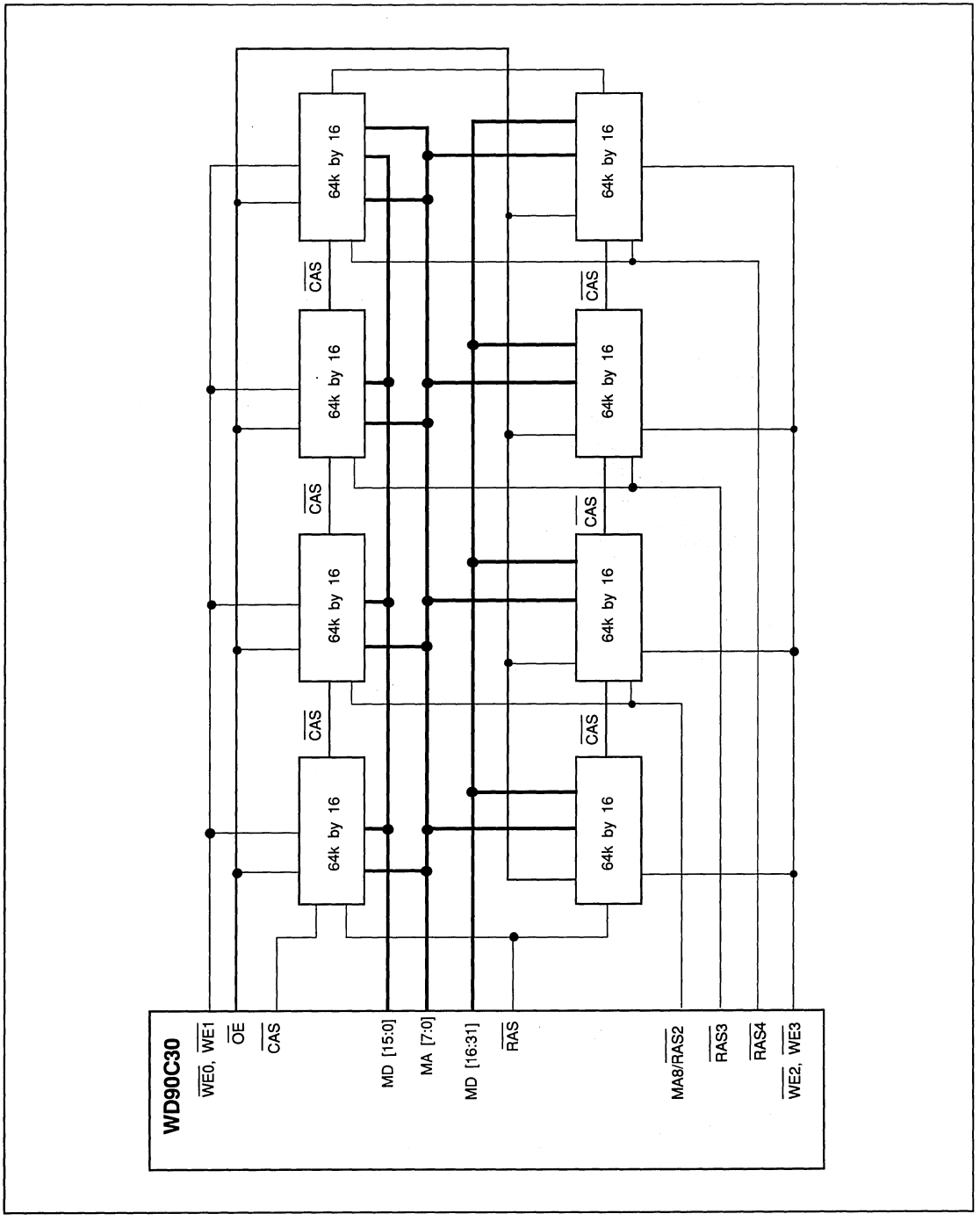
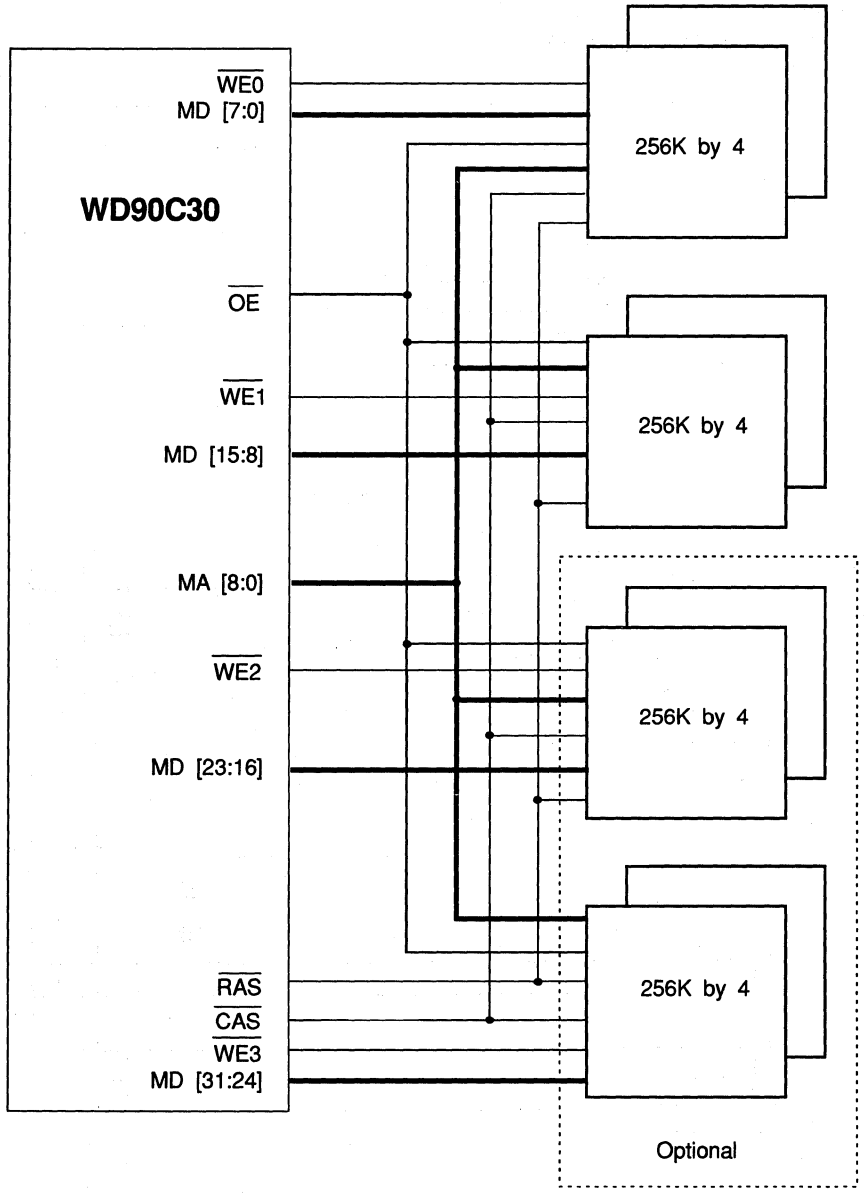


FIGURE 19. TWO, FOUR OR EIGHT 64K BY 16 DRAM INTERFACE



Note: Only MD [15:0] will be used if four 25K by 4 DRAMs are installed.

FIGURE 20. FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

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B.7 WD90C30 WITH RAMDAC INTERFACE

Figure 21 illustrates the WD90C30 and RAMDAC (WD90C50) interface block diagram for analog monitors.

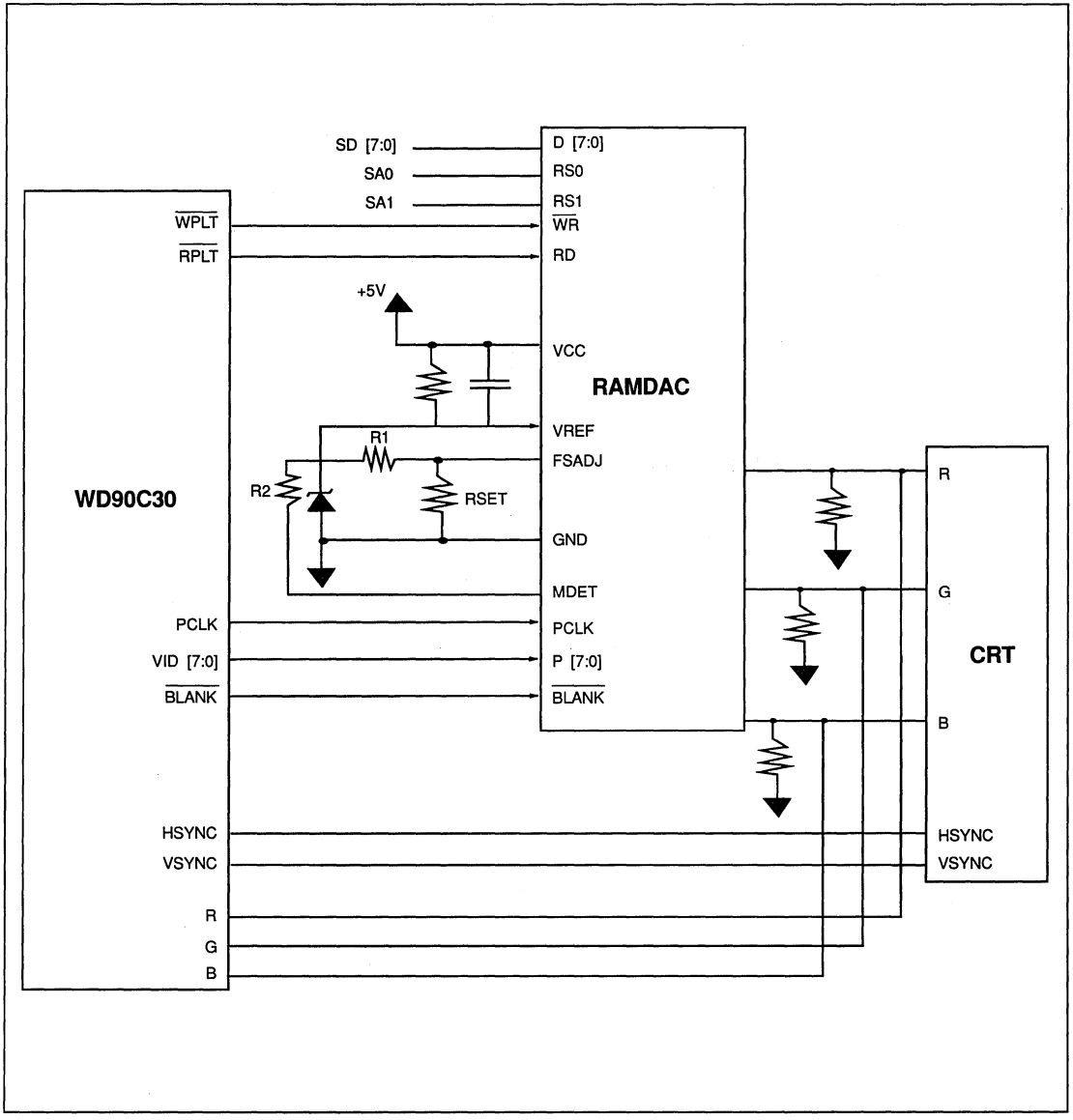

FIGURE 21. WD90C30 WITH RAMDAC INTERFACE

B.8 WD90C30 AND TTL MONITOR CONNECTIONS

Figure 22 illustrates the WD90C30 and TTL monitor connections

NOTE:

- VGA/TTL switch may be used to disable HSYNC and VSYNC for analog or TTL Video connector.
- MD(15:12) may also be connected as the EGA switches if desired. See PR Register and Pinout sections for more detail.
- For AT applications using the WD90C30, install the IRQ9 resistor.
- Transistor 2N2222A is used to emulate a monochrome and color display connection.

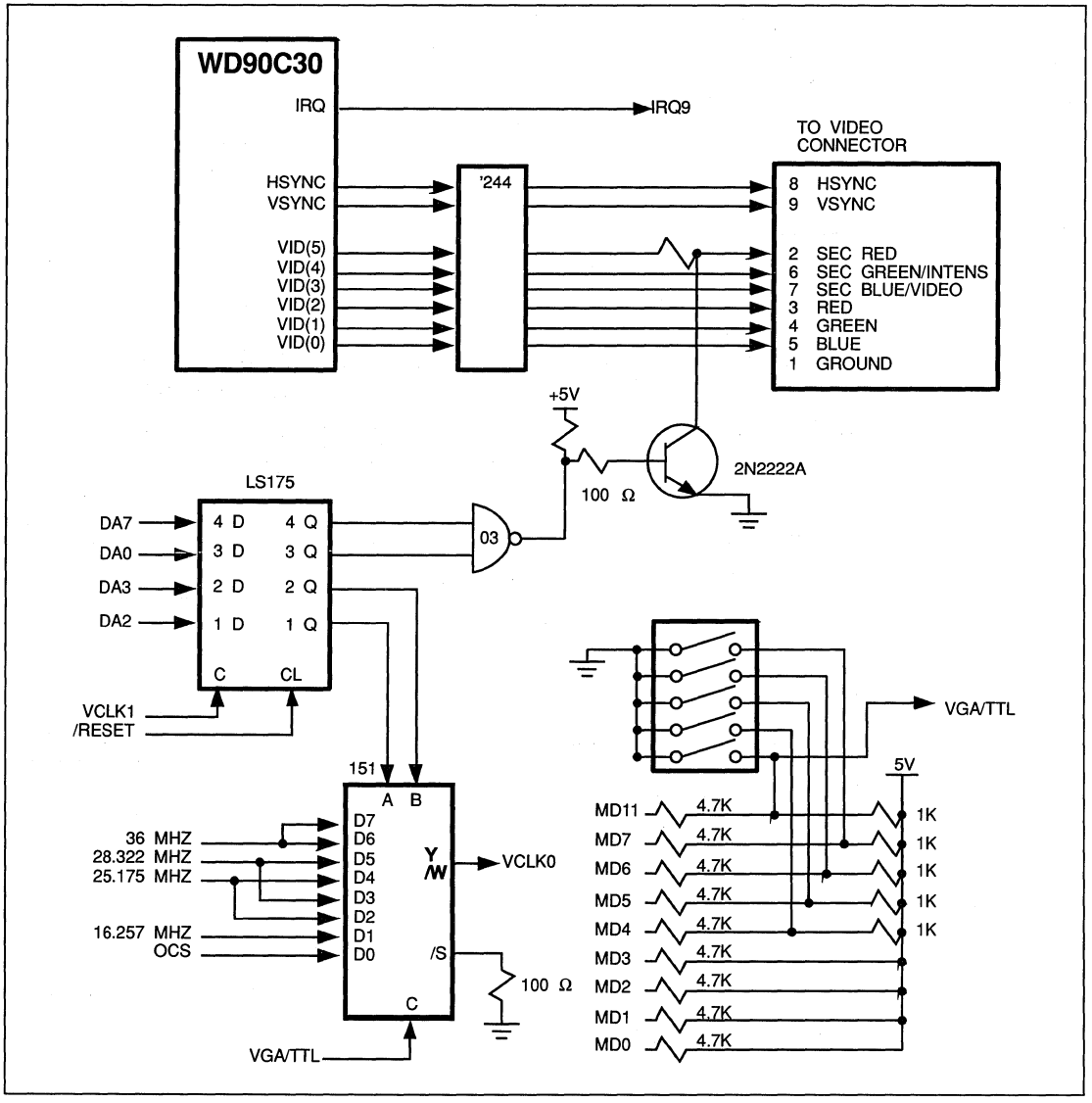

FIGURE 22. WD90C30 AND TTL MONITOR CONNECTIONS

B.9 CLOCK INTERFACE

Figure 23 illustrates the WD90C30 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H Bit 3 and Bit 2 and is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C30 signal pins (VCLK1, VCLK2) inputs.

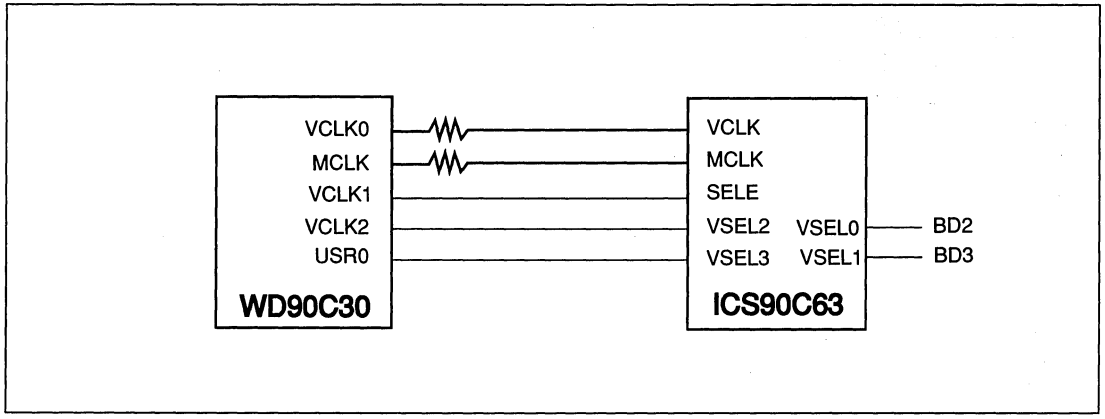

FIGURE 23. CLOCK INTERFACE

C.0 APPENDIX C - SHADOW REGISTER IMPLEMENTATION

The Shadow Register has been implemented on some of the CRTC registers. The purpose of using the shadow register is to have one CRTC register that is writable and readable all the time by application programs without actually changing CRTC timing. The actual CRTC timing registers are initialized and locked while using the shadow register for compatibility.

Registers are added to the following CRTC registers. The shadowed registers can be locked by writing "XXXXX101" to PR1A(3?5.3DH). This lock overrides any other locks. Then by setting PR1A Bit 3 = 1, this will select the shadow register for read.

HORIZONTAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.00	7:0	Group 0	Horizontal Total
3?5.02	7:0	Group 0	Start Horizontal Blanking
3?5.03	4:0	Group 0	End Horizontal Blanking
3?5.05	7	Group 0	Bit 6 of EHB
3?5.04	7:0	Group 0	Start Horizontal Retrace
3?5.05	4:0	Group 0	End Horizontal Retrace
3?5.03	6:5	Group 0	Display Enable Skew
3?5.05	6:5	Group 0	Horizontal Retrace Skew
VERTICAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.06	7:0	Group 2	Vertical Total
3?5.07	5,0	Group 2	Bits 9, 8 of VT
3?5.10	7:0	Group 3	Vertical Retrace Start
3?5.07	7,2	Group 2	Bits 9, 8 of VRS
3?5.11	3:0	Group 3	Vertical Retrace Start
3?5.15	7:0	Group 3	Start Vertical Blank
3?5.07	3	Group 2	Bit 8 of SVB
3?5.09	5	Group 2	Bit 9 of SVB
3?5.16	7:0	Group 3	End Vertical Blank

Note:
Group 0: Registers will be locked if PR3(5) = 1 or 3?5.11H bit 7 = 1
Group 2: Registers will be locked if PR3(0) = 1 or 3?5.11H bit 7 = 1
Group 3: Registers will be locked if PR3(0) = 1
Group 0, 2, 3 registers listed above will be locked if PR1A = "xxxxx101", regardless of the contents of PR3.
The Horizontal Display End and the Vertical Display End registers are not shadowed.

TABLE 19. SHADOW REGISTER IMPLEMENTATION

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D.0 APPENDIX D - SIGNATURE ANALYZER

A signature analyzer was designed for use in the WD90C30. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

D.1 DESCRIPTION

The basis of the signature analyzer is a linear feedback shift register (LFSR). The inputs to the LFSR tap onto the VID_[0:7] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately $1/2^n$, where n is the length of the shift register. A 16-bit signature register is used on the WD90C30. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$) has been implemented on the WD90C30. It was modified for multiple inputs as shown in the block diagram.

D.2 OPERATION

The signature analyzer was designed to collect signature of the VID_[0:7] outputs over one vertical frame. The signal path of the VID_[0:7] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3FH). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 Bits 2 through 0. PR10 also serves as the lock for other registers.

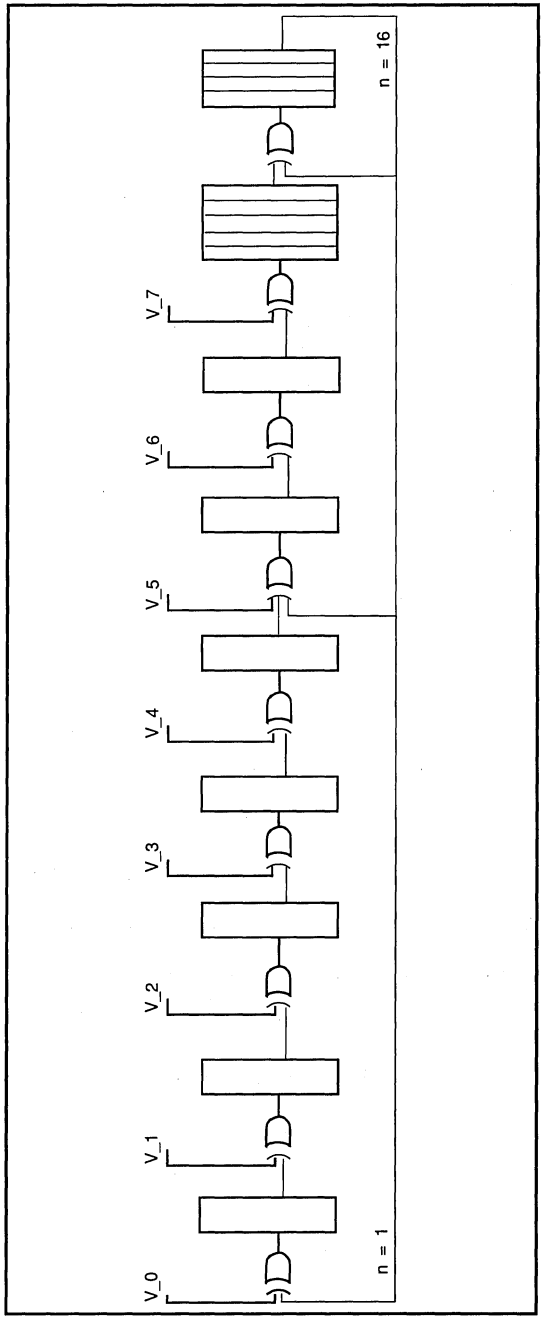

FIGURE 24. LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/WRITE	DESCRIPTION
BIT 0	Start/status	R/W	Writing "1" to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. 1: Busy 0: Finished or not enabled
BIT 1	Clear	R/W	Writing "0" to this bit position preloads the LFSR with 0001H. This bit must be set to operate the signaure analyzer. 1: Normal operation 0: Preload LFSR
BIT 2	Disable Video input	R/W	This bit is used in a self-test mode. A fixed signature will be generated for any given mode (independent of video memory data). 1: Disable video inputs 0: Enable video inputs
BIT 3	Lock Read Port	R/W	This bit must be set in order to read the signature and status. 1: Enable read of LFSR (addresses 3?5.20H and 3?5.21H). 0: Disable reads of LFSR

TABLE 20. CONTROL REGISTER PR19

The following programming steps highlight the sequence that will setup, check, and read the signature.

Step 1) 85H-> 3?5.29H; release control register (PR10) read and write lock

Step 2) 00H-> 3?5.3FH; clear signaure analyzer

Step 3) 03H-> 3?5.3FH; enable signature analyzer to collect signature

Step 4) read 3?5.3FH; check status for busy
if LSB = 1 repeat step 4
if LSB = 0 signature is collected, proceed to step 5

Step 5) OAH-> 3?5.3FH; enable signature analyzer read port

Step 6) read 3?5.20H; read low byte of signature

Step 7) read 3?5.21H; read high byte of signature

Step 8) 00H-> 3?5.3FH; clear signaure analyzer and lock read port.

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E.0 APPENDIX E - I/O MAPPING

E.1 INTRODUCTION

The I/O Mapping was designed for use in the WD90C30 to isolate board level solder defects. The I/O Mapping allows the IC to enter a test mode where all of pins in the IC are divided into various groups as inputs and output. The path from PCB trace through inputs, IC, output and PCB trace can be treated as a simple path. With test points on board, test for opens and shorts can be performed quickly.

E.2 TEST MODE

There are four requirements to meet for the WD90C30 to enter the I/O mapping test mode .

- $\overline{MWR}$ is LOW
- $\overline{IOR}$ is LOW
- CONFIGURATION SWITCH 2 is HIGH (MD2 is pulled high)
- RESET is HIGH

If both $\overline{MWR}$ and $\overline{IOR}$ are low at the same time, it becomes an illegal condition in AT machines and a reserved condition in the PS/2 machines. Configuration switch 2 high will ensure that WD90C30 is in AT mode. Reset controls a transparent latch as shown in Figure 25. Reset can be dropped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

E.3 PIN GROUPINGS

The following pin groupings are done to minimize routing overhead of I/O pin mapping. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the pin name that corresponds to the input pin(s).

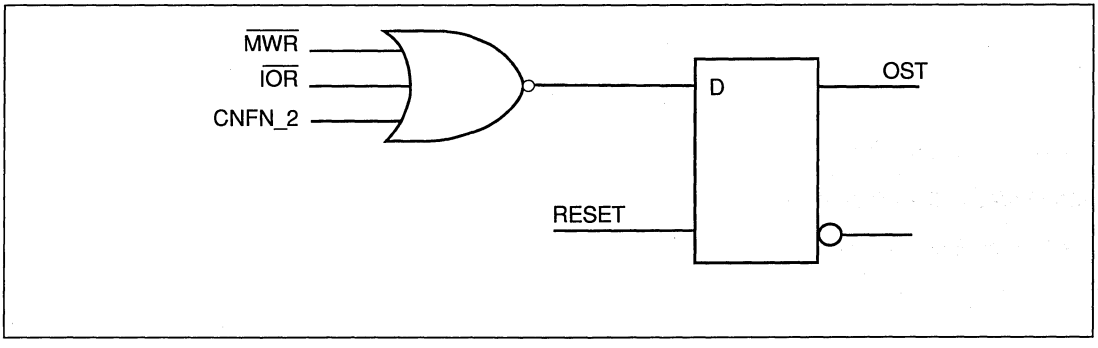

FIGURE 25. TEST MODE CIRCUIT

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
P1	MDET	P123	VID4
P4	MCLK	P124	VID5
P8	MD31	P125	VID6
P9	MD30	P126	VID7
P10 + P13	MD29 + MD26	P2	USR1
P11 + P14	MD28 + MD25	P3	USR0
P12	MD27	P7	$\overline{WE3}$
P15	MD24	P6	$\overline{OE}$
P19 + P24 + P31	MD23 + MD18 + MD15	P27	$\overline{RAS4}$
P20	MD22	P16	$\overline{WE2}$
P21 + P25 + P32	MD21 + MD17 + MD14	P28	$\overline{RAS3}$
P22 + P26 + P33	MD20 + MD16 + MD13	P30	$\overline{WE1}$
P23 + P34 + P43	MD19 + MD12 + MD6	P39	$\overline{RAS}$
P35 + P38	MD11 + MD8	P52	$\overline{WE0}$
P36 + P41	MD10 + $\overline{CAS}$	P53	MA0
P37 + P42 +P46	MD9 + MD7 + MD3	P54	MA1
P44 + P47	MD5 + MD2	P55	MA2
P45 + P49	MD4 + MD0	P56	MA3
P48 + P62	MD1 + A17	P57	MA4
P63 + P68	A18 + A22	P59	MA6
P64 + P69 + P72	A19 + A23 + $\overline{BHE}$	P58	MA5
P65	A20	P60	MA7
P66 + P73 + P86	A21 + ALE + $\overline{ROM16}$	P61	MA8
P70 + P77 + P80	$\overline{IOCS16}$ + $\overline{IOW}$ + RESET	P74	IRQ
P90 + P93 + P95 P79 + P89	DA15 + DA12 + DA10 + $\overline{MWR}$ + A16	P71	$\overline{MEMCS16}$
P75 + P78 + P88	EMEM + $\overline{MRD}$ + $\overline{EDBUFH}$	P82	IOCHRDY
P85 + P92	$\overline{EIO}$ + DA13	P81	$\overline{0WS}$
P91 + P94	DA14 + DA11	P87	$\overline{EBROM}$
P76 + P77	$\overline{IOR}$ + $\overline{IOW}$	P100	DIR**
P96 + P101	DA9 + DA7	P115	$\overline{RPLT}$
P97 + P102	DA8 + DA6	P114	$\overline{WPLT}$
P98 + P103	$\overline{EABUF}$ + DA5	P113	$\overline{HTL}$
P104 + P109	DA4 + $\overline{EDBUFL}$	P112	$\overline{BLANK}$
P105 + P107	DA3 + DA1	P110	VSYNC
P106 + P108	DA2 + DA0	P111	HSYNC

Note:
A "+" in the input column indicates an OR function for the test input pins only.
** This mapping for DIR output is valid only during RESET HIGH.

TABLE 21. WD90C30 PIN SCAN MAP FOR 132-PIN PACKAGE

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P128	VCLK0	P118	PLCK
P129	VCLK1	P119	VID0
P130	VCLK2	P120	VID1
P131	$\overline{\text{EXPCLK}}$	P121	VID2
P132	$\overline{\text{EXVID}}$	P122	VID3

TABLE 21. WD90C30 PIN SCAN MAP FOR 132-PIN PACKAGE (Cont.)

Refer to Table 3 for the comparable pin number for a 144-pin package.

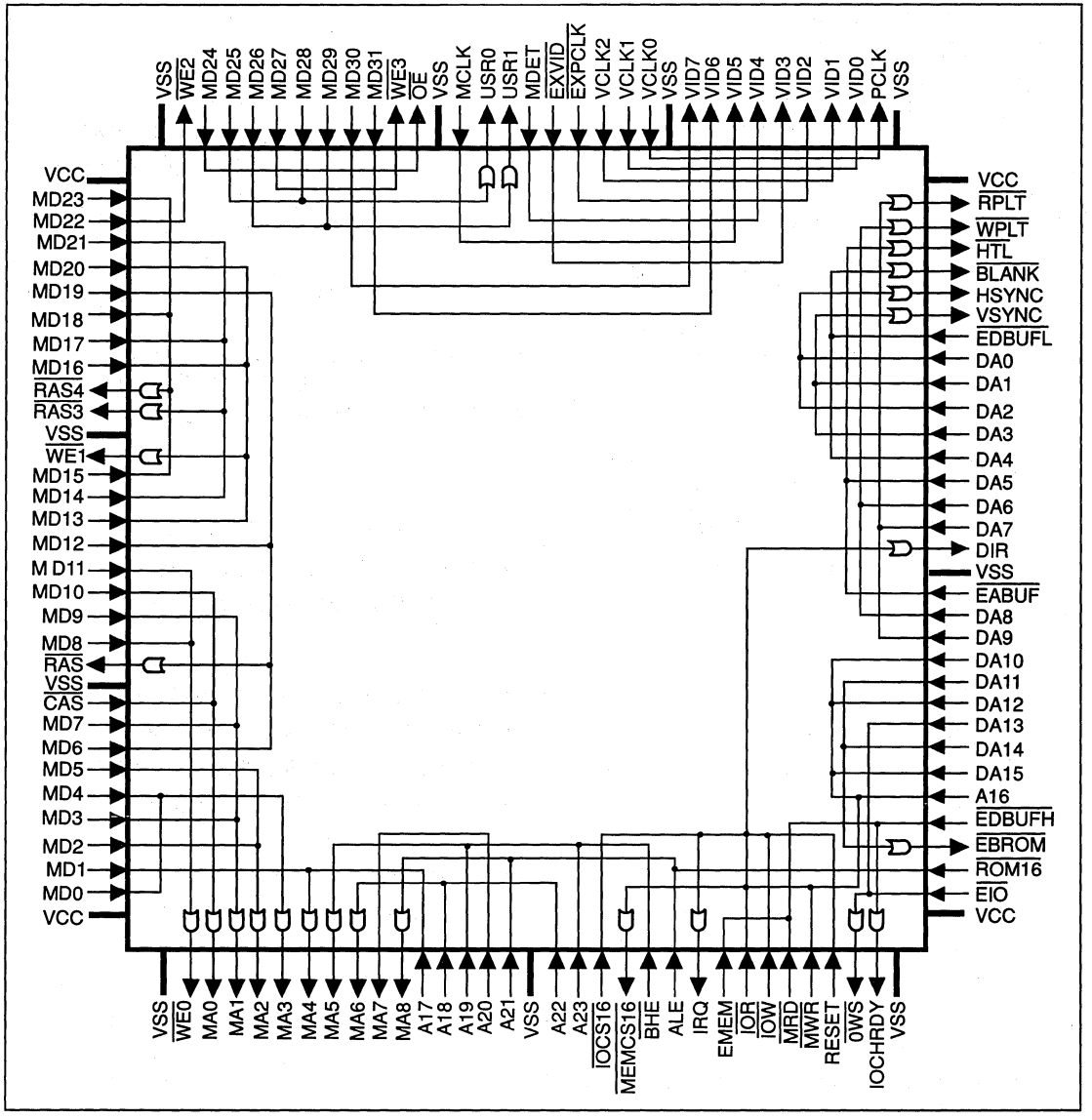

FIGURE 26. WD90C30 PIN SCAN MAP FOR A 132-PIN PACKAGE

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F.0 APPENDIX - F

The WD90C30 design is based on the popular WD90C11 design. Please refer to the WD90C11 data sheet for more informaton. This appendix highlights the major differences between the two devices.

F.1 REGISTER DIFFERENCES BETWEEN WD90C30 AND WD90C11

PR30 Write Buffer and FIFO Control Register, Read/Write Port = 3C5H, Index = 10H

The register also exists in WD90C11. In the WD90C30 chip, the definition of this register is the same except for Bits 7, 6, 5, and 3. All bits are reset to zero at Power-On-Reset (POR).

Bit (7:6)

BIT	VALUE	FUNCTION
7-6	00	One-level write buffer
7-6	01	Two-level write buffer
7-6	10	Three-level write buffer
7-6	11	Four-level write buffer

NOTE: Write buffer is turned on by setting PR31 (3C5H INDEX 11H) Bit 2 = 1. Otherwise, these two bits have no effect.

WD90C30 - FEATURES	WD90C11 - FEATURES
• Multiplexed CPU address and data	• Separated CPU address and data buses.
• Programmable CPU address decoding to map VGA anywhere in the CPU address space.	• Fixed CPU address decoding (0A000 - 0BFFF)
• 16-bit or 32-bit video memory interface	• 8 or 16-bit video memory interface
• Support for 1 Mbyte of memory	• Support for 512 Kbytes of memory
• Support for four or eight 256K by 4 DRAM	• Support for two or four 256K by 4 DRAMs
• 1024 by 768 resolution in 256 colors	• 800 by 600 resolution in 256 colors
• Four levels of CPU write cache	• One level of CPU write cache
• 11-bit vertical counter	• 10-bit vertical counter
• Support for 6 to 16 pixel-wide fonts	• Support for 6 to 8 pixel-wide fonts
• Support for two, four or eight 64K by 16 DRAMs	
• Zero wait state generation	
• CRTC shadow registers	
• Video output signature and pin mapping for system level testing	

TABLE 22. WD90C30 FEATURES / WD90C11 FEATURES

Bit 5

BIT	VALUE	FUNCTION
5	0	32-bit display memory interface.
5	1	16-bit display memory interface.

Bit 4

BIT	VALUE	FUNCTION
4	0	Enable word transfer in planar modes.
4	1	Disable word transfer in planar modes.

Bit 3

BIT	VALUE	FUNCTION
3	0	8-Level or 4-level screen refresh FIFO, depending on Bit 2.
3	1	2-level screen refresh FIFO regardless of bit 2.

Bit 2

BIT	VALUE	FUNCTION
2	0	8-level screen refresh FIFO.
2	1	4-level screen refresh FIFO.

Bits (1:0)

BIT	VALUE	FUNCTION
1-0	00	Generate FIFO request when FIFO is one level empty.
1-0	01	Generate FIFO request when FIFO is two levels empty.
1-0	10	Generate FIFO request when FIFO is three levels empty.
1-0	11	Generate FIFO request when FIFO is four levels empty.

F.2 PR33 DRAM TIMING AND ZERO WAIT STATE CONTROL REGISTER, READ/ WRITE PORT = 3C5H, INDEX = 13H

This is a new register in the WD90C30.

Bits (7:6)

BIT 7	BIT 6	FUNCTION
0	0	$\overline{0WS}$ = 0 if the internal write cache is ready.
0	1	$\overline{0WS}$ = 0 if the internal write cache is ready AND memory address is decoded.
1	0	$\overline{0WS}$ = 0 if the internal write buffer is ready AND memory address is decoded AND MWR = 0.
1	1	$\overline{0WS}$ = 0 if the condition "1, 0" is true OR I/O address is decoded.

Bit 5

Reserved

Bits (4:3)

BIT	VALUE	FUNCTION
4-3	00	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (4-7) ns. $\overline{CAS}$ high is 1 Mclock - (4-7) ns.
4-3	01	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1 Mclock + (8-14) ns. $\overline{CAS}$ high is 1 Mclock - (8-14) ns.
4-3	10	$\overline{CAS}$ cycle is 2 Mclocks. $\overline{CAS}$ low is 1.5 Mclocks. $\overline{CAS}$ high is 0.5 Mclocks.
4-3	11	Reserved.

Bit 2

BIT	VALUE	FUNCTION
2	0	$\overline{CAS}$ cycle starts 3 Mclocks after $\overline{RAS}$ low.
2	1	$\overline{CAS}$ cycle starts 2 Mclocks after $\overline{RAS}$ low.

Bits (1:0)

BIT	VALUE	FUNCTION
1-0	00	$\overline{RAS}$ high is two and half Mclocks plus a 4-7 ns delay.
1-0	01	$\overline{RAS}$ high is three Mclocks wide.
1-0	10	$\overline{RAS}$ high is two Mclocks wide.
1-0	11	$\overline{RAS}$ high is two and a half Mclocks.

F.3 PR34 VIDEO MEMORY MAPPING REGISTER, READ/WRITE PORT = 3C5H, INDEX = 14H

Bits (7:0)

BITS	FUNCTION
7-4	Reserved.
3-0	The contents of these four bits are compared with the CPU address A_[23:20] as part of the video memory address decoding. This will allow the VGA to be mapped out of the lowest 1Mbyte of CPU memory space. This register will not affect the $\overline{ROM16}$ decoding. $\overline{ROM16}$ will still decode at A_[23:20] = 0H.

F.4 PR1 MEMORY SIZE REGISTER, READ/WRITE PORT = 3CFH, INDEX = 0BH

Bits (7:6)

BIT	VALUE	FUNCTION
7-6	00	Same as 1C.IBM 256 Kbyte VGA.
7-6	01	Same as 1C.256 Kbyte Paradise VGA.
7-6	10	Same as 1C.512 Kbyte Paradise VGA.
7-6	11	1024 Kbyte Paradise VGA.

Bits (5:4)

BIT	VALUE	FUNCTION
5-4	00	IBM memory mapping. Decode memory address range is from A0000H - BFFFFH depending on register Bits 3 and 2 (3CFH Index 06H).
5-4	01	Decode memory address range from 00000H - 3FFFFH (256K total).
5-4	10	Decode memory address range from 0000H - 7FFFFH (512K total).
5-4	11	Decode memory address range from 00000H - FFFFFH (1 M total).

Bits (3:0)

BITS	FUNCTION
3	Enable Alternate Address Offset Register PROB.
2	16-Bit Video Memory.
1	ROM Data Width.
0	BIOS ROM Map Out.

Bit 3

Enable Alternate address Offset Register PROB

Bit 2

Enable 16-bit bus for Video Memory. When set to 1, $\overline{\text{MEMCS16}}$ is asserted for all video memory cycles.

Bit 1

0 = BIOS ROM has an 8-bit data path.

1 = BIOS ROM has a 16-bit data path from C000:0H - DFFF:FH, if bit 0 = 0. ($\overline{\text{ROM16}}$ responds to ROM access).

A pull-down resistor on MD(10) sets this bit to 1 after power-on-reset. This bit can also be set to 1 by an I/O write to PR1 register if CNF(1) = 1 (2 ROMs).

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches bit 0 after power-up. A pull-up on MD(0) sets this bit to 0 at power-on-reset.

F.5 PR22 SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 8H

This is a new register in the WD90C30.

Bits (7:0)

Scratch Bits

F.6 PR23 SCRATCH PAD REGISTER, READ/WRITE PORT = 3C5H, INDEX = 9H

This is a new register in the WD90C30.

Bits (7:0)

Scratch Bits

F.7 PROA AND PROB ADDRESS OFFSET REGISTERS, READ/WRITE PORT = 3CFH, INDEX = 09H AND 0AH

Bit 7

This bit is the 7th memory address offset bit.

Bits (6:0)

Primary/Alternate Address Offset Bits.

The WD90C30 is capable of controlling up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes of total memory space for the display memory, starting at A0000H and ending at BFFFFH. For VGA to reach the memory beyond this range, the WD90C30 has two CPU address offset registers, PROA and PROB. These registers can be used to support more than 128 Kbytes of linear display memory address space.

The Contents of PROA (bits 6:0) or PROB (bits 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This is similar to the segment registers DS and ES in the 8088/80X86 architecture. PROA and PROB provide a 4 Kbyte segmentation of the display memory. Increment PROA or PROB by one of its equivalents to jump a 4 Kbyte segment to another 4 Kbyte segment of the display memory.

Both PROA and PROB are set to zero at power-on-reset.

There are two ways to control whether PROA or PROB get added into the CPU address.

1. **Sequencer Extention Register 3C5H Index 11H bit 7 = 0.**

PROA is the primary offset register being added to the CPU address. PR1, bit 3 enables PROB which becomes the secondary offset register.

If Graphics Controller Index 6H bits 3:2 = 00, A000:0H for 128K, and PR1 bit 3 = 1, then PROA offsets the CPU address from B000:0H to BFFF:FH while PROB offsets the CPU address from A000:0H to AFFF:FH.

If Graphics Controller Index 6H, bits 3:2 = 01 (A000:0H for 64K), and PR1 bit 3 = 1, then PROA offsets the CPU address from A800:0H to AFFF:FH, while PROB offsets the CPU address from A000:0H - A7FF:FH.

2. Sequencer Extention Register 3C5H Index 11H bit 7 = 1.

Both PROA and PROB are enabled. PROA is selected as the offset register unless a CPU memory write selects PROB as the offset register.

F.8 PR17 MISCELLANEOUS CONTROL REGISTER, READ/WRITE PORT = 3?5H, INDEX = 30H

Bits (7:6)

Reserved.

Bit 5

BIT	VALUE	FUNCTION
5	0	No effect.
5	1	In text mode, if PR2 Bits 2 and 3 = 11, then the 10-dot font is selected. Otherwise, it has no effect.

Bit 4

BIT	VALUE	FUNCTION
4	0	No effect.
4	1	PCLK is divided by two.

Bits (3:0)

BITS	FUNCTION
3	Map Out 4K BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map Out 2K of BIOS ROM.

Bit 3

Map out 4K of BIOS ROM.

Setting this bit to 1 disables access to the BIOS ROM in the system address range C600:0H - C6FF:FH.

Power on reset sets this bit to 0.

Bit 2

Enable 64K BIOS ROM.

Setting this bit to 1 enables access to the BIOS ROM in the system range C000:0H - CFFF:FH.

Power on reset sets this bit to 0.

Bit 1

Setting this bit to 1 locks Hercules compatibility register (I/O Port 3BFH).

Power on reset sets this bit to 0.

Bit 0

Map out 2K of BIOS ROM.

Setting this bit to 1 disables access to the BIOS ROM in the system address range C600:0H - C67F:FH.

Power on reset sets this bit to 0.

F.9 PR18 VERTICAL TIMING OVERFLOW REGISTER, READ/WRITE PORT = 3?5H, INDEX = 3EH

Bits (7:0)

BITS	FUNCTION
7:5	Reserved
4	Line compare Bit 10.
3	Start vertical blank Bit 10.
2	Start vertical retrace Bit 10.
1	Vertical display enable end Bit 10.
0	Vertical total Bit 10.

F.10 WD90C30 - NEW CONFIGURATION BITS

The WD90C30 provides three new bits in addition to the configuration bits that are standard with the WD90C11. The following configuration bits are set during power-on-reset. A pull-down resistor on the corresponding MD bits will cause a configuration bit to be set low. Otherwise, configuration bits are high.

Configuration Bit 18

0 = The $\overline{\text{ROM16}}$ pin is an input. $\overline{\text{ROM16}}$ becomes EXBLANK.

1 = The $\overline{\text{ROM16}}$ pin is an output pin.

Configuration Bit 16

0 = 64K by 16 DRAM

1 = 256K by 4 or 256K by 16 DRAM

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G.0 PACKAGE DIMENSIONS

Figure 27 illustrates the 132-pin JEDEC package showing the dimensions in inches. Figure 28 illustraes the 144-pin EIAJ package showing the dimensions in millimeteres and inches.

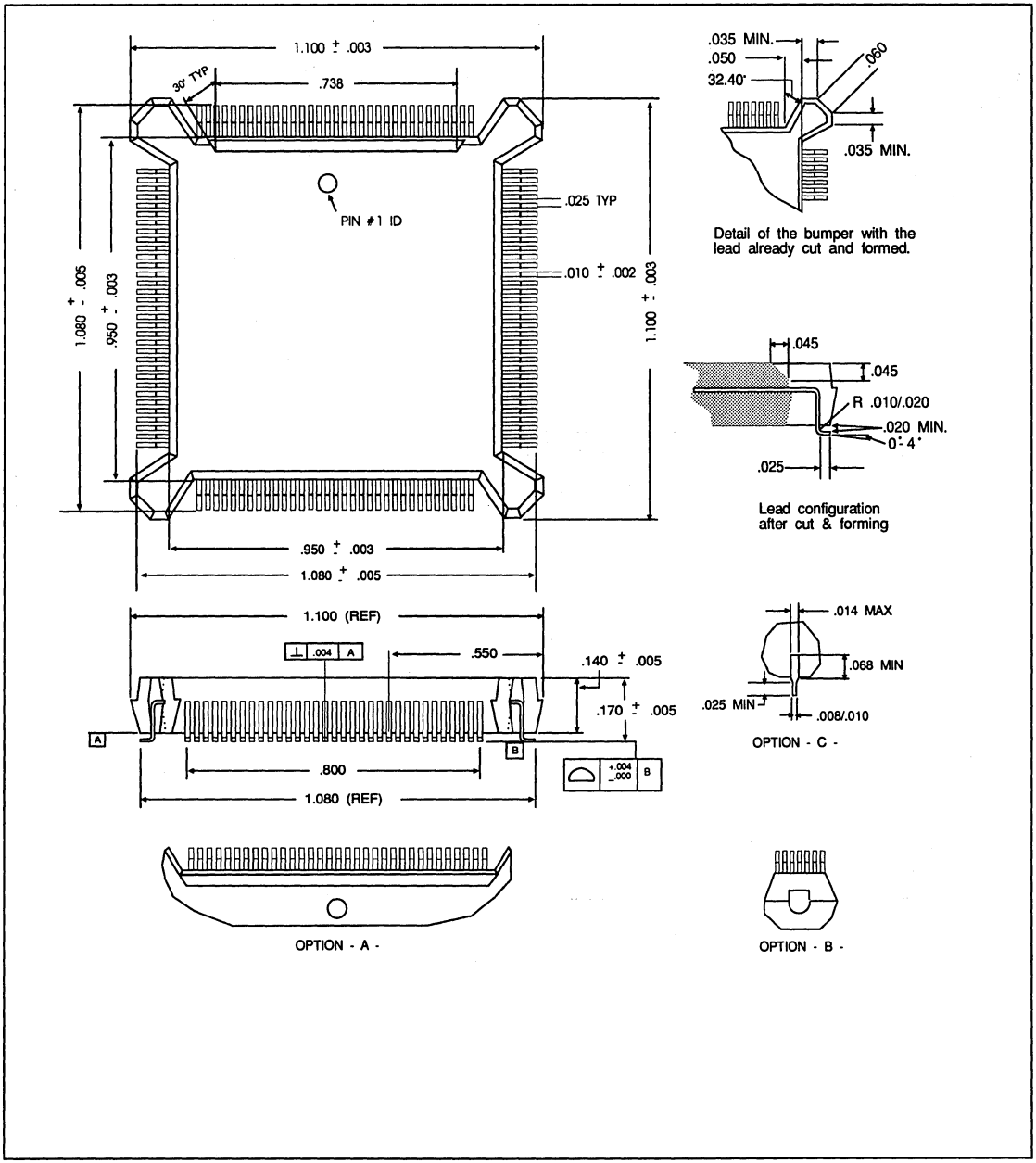


FIGURE 27. 132-PIN JEDEC PACKAGE

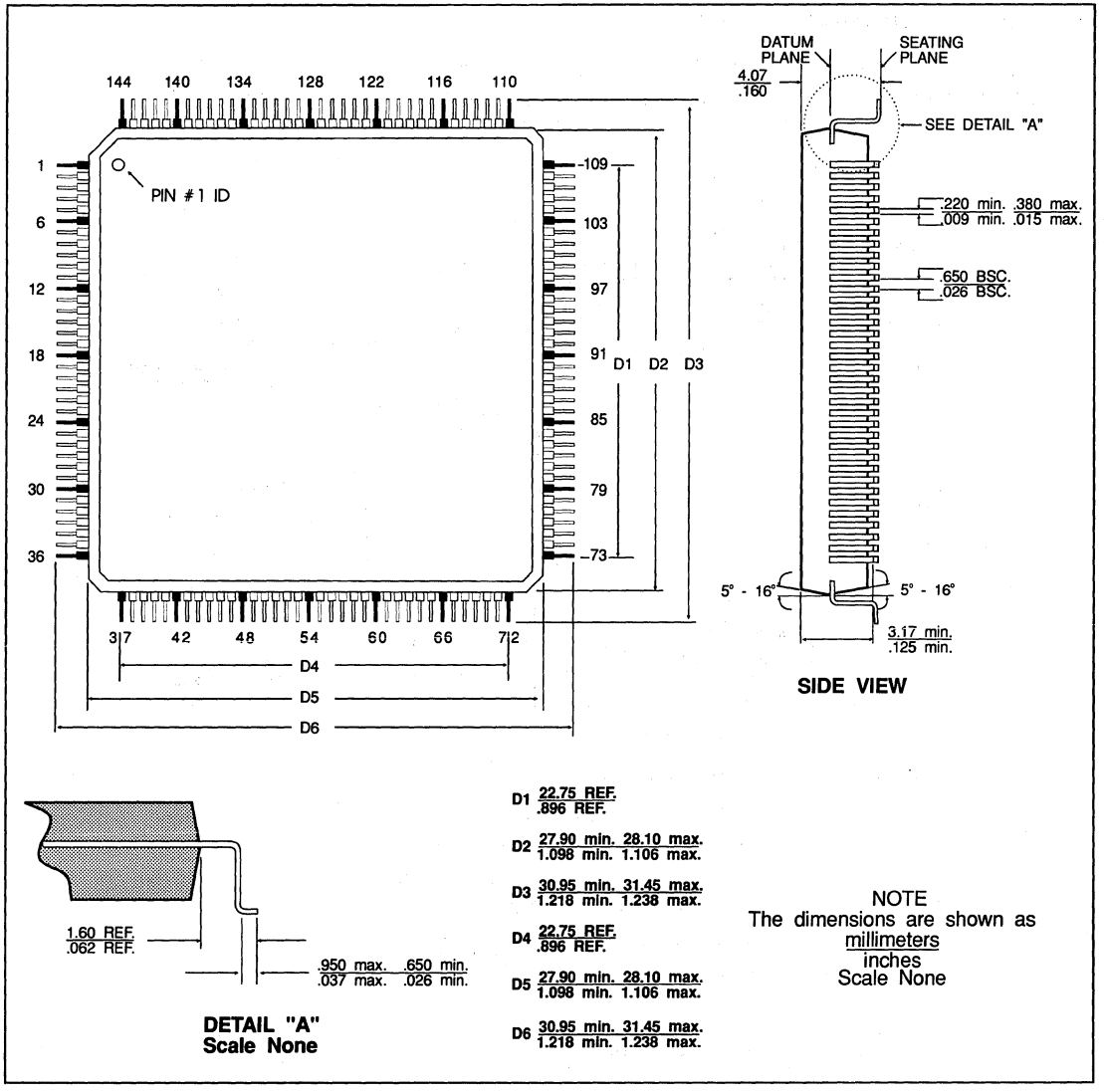
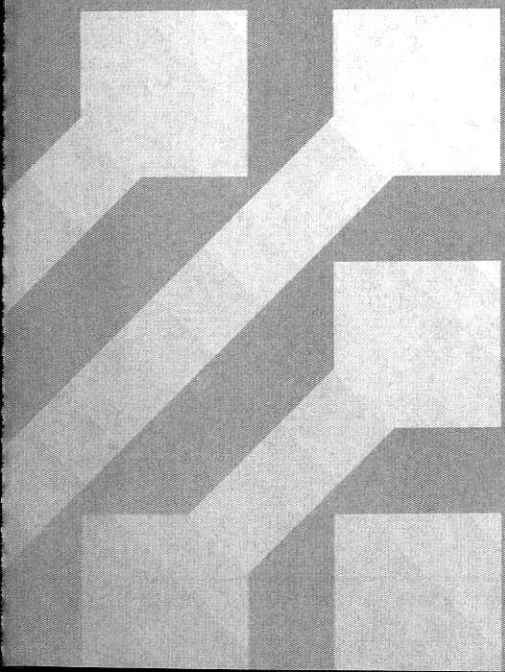


FIGURE 28. 144-PIN EIAJ PACKAGE

WD90C31

High Performance Video Controller with Windows Accelerator



WESTERN DIGITAL

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LIST OF TABLES

LIST OF ILLUSTRATIONS

ADDITIONAL REFERENCES

IBM Personal Computer Hardware User Guide (IBM # 6322510)
IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
IBM Personal System 2 Model 30 Hardware User Guide (IBM # 63x2230)
IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 63x2201)
IBM PC Options And Addapters Technical Reference Manual (IBM # 6322509)
IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)

1.0 INTRODUCTION

The WD90C31 VGA Controller is a 0.9 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with either the PC/XT/AT bus or the IBM Micro Channel bus, while maintaining backward compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. A major advantage of the WD90C31 is that designs implementing this graphics controller are able to run applications requiring VGA hardware and BIOS compatibility and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C31 supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C31 also supports 132-column text mode and 6-16 pixel fonts.

This document supplies a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information and associated references.

1.1 FEATURES

- Provides single chip video graphics solution for IBM AT and PS/2 compatible systems.
- Supports two, four or eight 64 Kbyte by 16 DRAMs; four or eight 256 Kbyte by 4 DRAMs; and one or two 256 Kbyte by 16 DRAMs.
- Pin compatible with the WD90C30.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics and AT&T Model 6300 compatible.
- Supports all IBM VGA modes with two 64K by 16 DRAMs or only one 256K by 16 DRAM.
- With more DRAMS installed it can support 256 colors at the following resolutions: 640 by 400, 640 by 480, 800 by 600 and 1024 by 768.
- Supports 132-column text.
- Write buffer for zero wait state CPU write performance.
- 8-bit or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate.
- Up to 50 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6-16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC and overscan registers.
- Special CRTC shadow registers for support of non-standard monitors.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- Low power 0.9 micron CMOS technology.
- 132-pin JEDEC (Joint Electronic Device Engineering Council) PQFP (Plastic Quad Flat Package).
- 144-pin EIAJ (Electrical Industry Association of Japan) MQFP (Metric Quad Flat Package).
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for PC/XT/AT and Micro Channel with minimum external component support.
- Programmable memory mapping register to map WD90C31 into any CPU memory address space.
- Eight-bit CPU address offset register to support 1 Mbyte memory segmentation.
- A full-function VGA controller optimized for windows.
- Hardware Cursor.
- Up to 64 by 64 pixels.
- Inversion and transparency.
- Two color and three color modes.
- Hardware BITBLT.
- Raster operations.
- Transparency.
- Color expansion for text support.
- Rectangular and linear addressing.
- Filled rectangles.
- Transfers to and from the Host.

1.2 GENERAL DESCRIPTION

This document describes the WD90C31 VGA controller specifically designed for the Microsoft Windows marketplace. The WD90C31 incorporates numerous advanced features that Windows drivers may take advantage of for increased performance.

The WD90C31 is fully compatible with the WD90C30 making it possible to utilize the additional features of the WD90C31 by only upgrading the BIOS and software drivers.

1.2.1 Hardware Cursor

The WD90C31 supports a hardware cursor with a user-defined pattern of up to 64 by 64 pixels at two bits per pixel. The cursor pattern is stored in off-screen display memory. A programmable origin is provided, and cursors may be displayed with any two or three desired colors.

1.2.2 Hardware BITBLT

The WD90C31 provides hardware accelerated Bit Block Transfers (BITBLT) of data between regions of display memory, or between display memory and a fixed I/O port. Display memory regions may be rectangular or linear.

The BITBLT hardware supports text modes as well as monochrome, 4-bit (16-color) and 8-bit (256 color) modes.

A full complement of raster operations and transparency are available, as well as 8 by 8 color patterns. Color expansion, useful for accelerating text modes is supported. Plane masking is also supported.

2 .0 WD90C31 ARCHITECTURE

The WD90C31 contains six major internal modules, the CRT Controller, the Sequencer, the Graphics Controller, Hardware Cursor Controller, BITBLT Controller and the Attribute Controller. The WD90C31 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

An internal four-level write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates a horizontal sync (HSYNC), vertical sync (VSYNC) and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode and the dot clock in the graphics mode. The sequencer arbitrates between video display refresh, memory refresh and CPU access of the video memory. The sequencer also provides write buffer control.

The Graphics Controller manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles.

The Attribute Controller serializes the video memory data into video data stream according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video and background or foreground color in all display modes.

The Hardware Cursor Controller reads in each line of the cursor pattern during the horizontal retrace immediately preceding the scan line on which that line of the cursor pattern is to be displayed. It then merges the cursor pattern into the video stream for the scan line.

The BITBLT Controller generates addresses and data for BITBLT operations, including pattern, rectanlge and system-to-display memory operation.

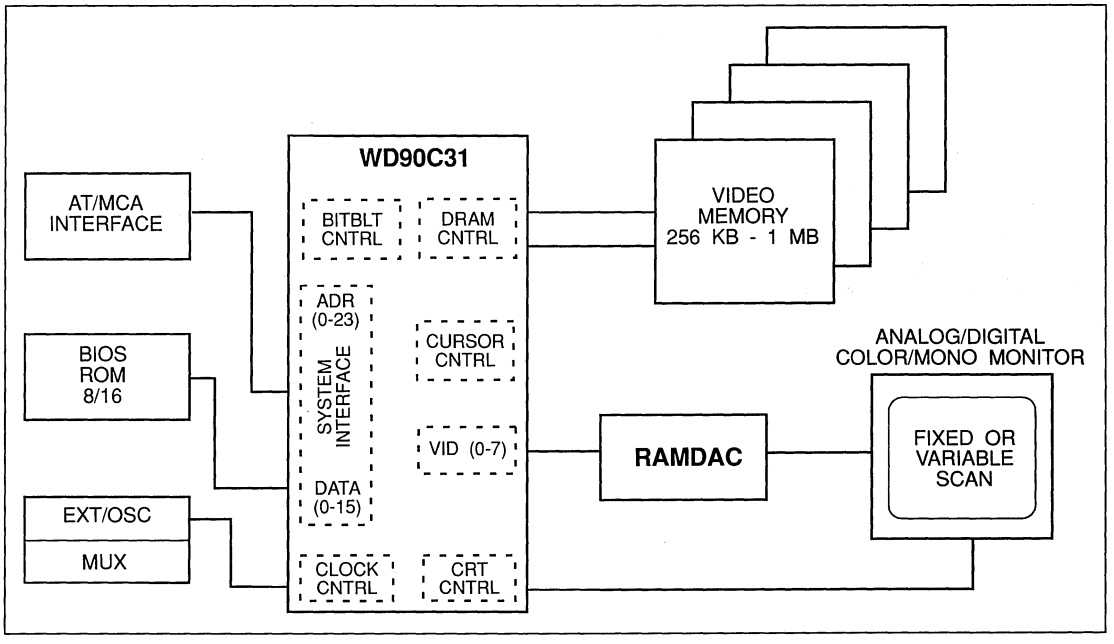

FIGURE 2-1. SYSTEM BLOCK DIAGRAM

3.0 WD90C31 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C31 is designed to operate in both the AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of the Configuration Register bit CNF(2), which is determined upon power-up/reset and is described in Section 7.10, WD90C31 Configuration Register Bits CNF(18:0).

Whether configured for AT or Micro Channel operation, the WD90C31 operates functionally in a manner conducive to AT or Micro Channel interfacing. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C31 provides all the signals and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus in 8-bit or 16-bit data path modes. WD90C31 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, it is possible to implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM.

The I/O data path can be programmed to be either 16-bit or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C31 to indicate a 16-bit operation.

The WD90C31 has a display memory write buffer which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C31 provides the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT (or 03C3H for Micro Channel) for setup and 102H for VGA enable, have been implemented internally in the WD90C31.

3.2 DRAM INTERFACE

The WD90C31 has a very flexible DRAM interface. It can work with two, four, or eight 64K by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs and one 256 Kbyte by 16 DRAM with a 16-bit memory interface. Other possible configurations are eight 256 Kbyte by 4 DRAMS or two 256Kbyte by 16 DRAMS with a 32-bit memory interface. In all cases the WD90C31 uses the DRAM fast page mode to optimize performance.

The WD90C31 can support all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has internal write buffer, the WD90C31 can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed the WD90C31 is capable of supporting high resolution color video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C31 is designed to support 60 ns, 70 ns, 80 ns and 100 ns DRAMs with the dedicated MCLOCK which can operate from 32 MHz to 50 MHz maximum.

The WD90C31 generates fast page DRAM timing for all BITBLT, cursor and CPU accesses, graphics display and text display. A choice of page mode and non-page mode operation is provided to access fonts in text modes.

The WD90C31 also generates CAS before RAS DRAM refresh for the display memory.

3.3 VIDEO INTERFACE

The WD90C31 is optimized to connect to an analog CRT monitor through a RAMDAC but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C31 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors such as multifrequency monitors, are less

stringent because of the many sync frequencies available. The WD90C31 can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C31. The WD90C31 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C31 has four clock input signals, Memory Clock, MCLK, which drives the DRAM and bus interface timing, and the three Video Clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. MCLK can also be selected as a memory clock or video clock.

3.5 WD90C31 POWER-UP CONFIGURATION

The WD90C31 uses the memory data pins to configure an internal configuration register upon power-up-reset. CNF(2) determines whether the WD90C31 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C31 at power-up-reset are used as status bits or for clock source control. For more information on WD90C31 power-up configuration, refer to Section 7.10, Configuration Bits.

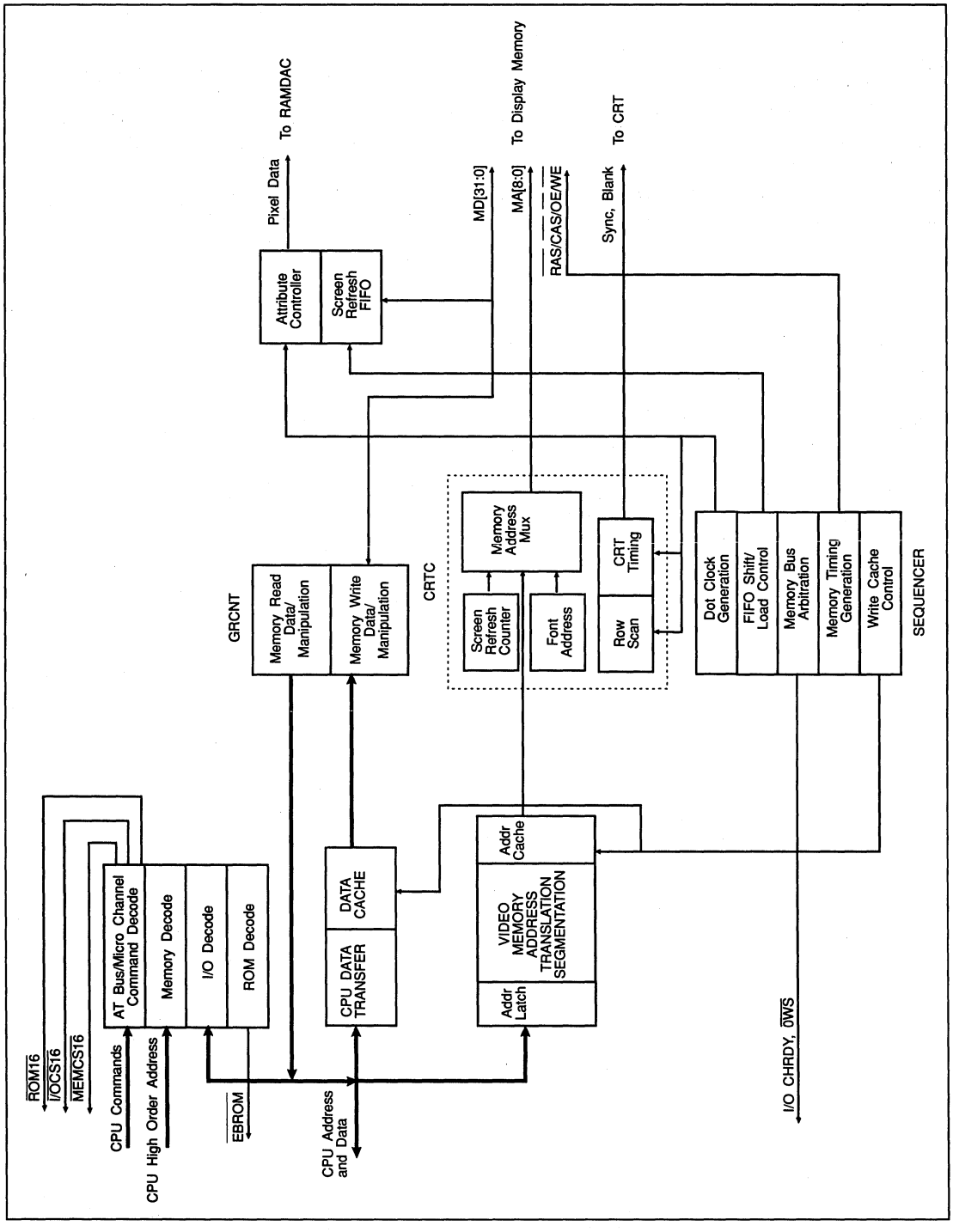

FIGURE 3-1. WD90C31 BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTION

Table 4-1 provides a list of pin assignments for the 132-pin JEDEC package. Table 4-2 provides a list of pin assignments for the 144-pin EIAJ package. Table 4-3 provides a description of the signals controlled by the WD90C31, and both the JEDEC and EIAJ pins are identified. The WD90C31 mnemonics are used.

18

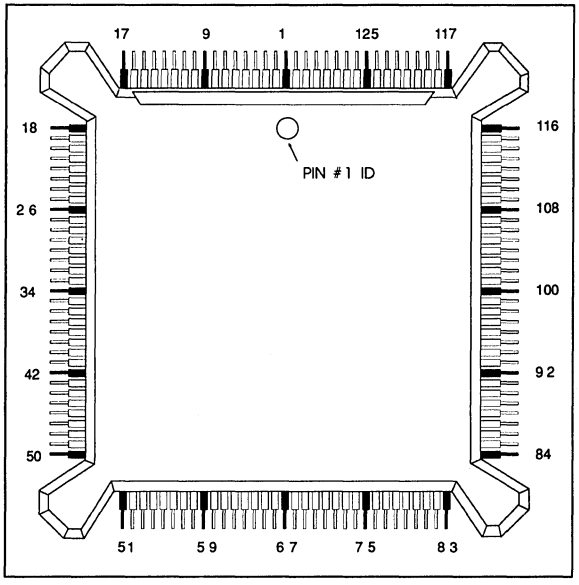

FIGURE 4-1. 132-PIN JEDEC PACKAGE

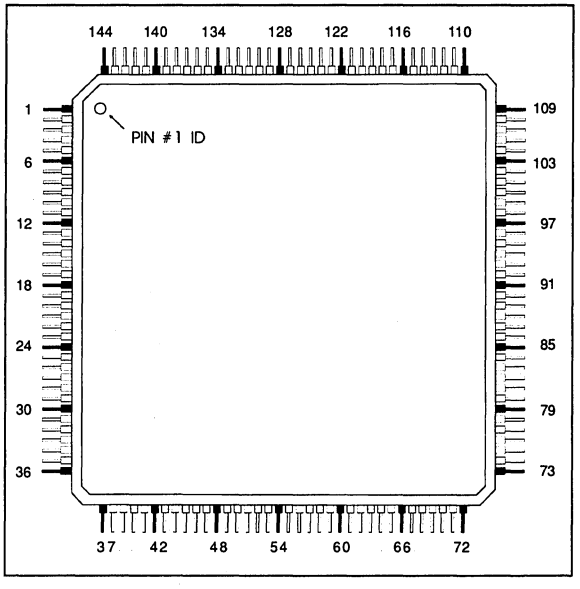

FIGURE 4-2. 144-PIN EIAJ PACKAGE

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	MDET	34	MD12	67	VSS	100	DIR
2	USR1	35	MD11	68	A22	101	DA7
3	USR0	36	MD10	69	A23	102	DA6
4	MCLK	37	MD9	70	$\overline{\text{IOCS16}}$ (CDSETUP)	103	DA5
5	VSS	38	MD8	71	$\overline{\text{MEMCS16}}$ (CDDS16)	104	DA4
6	$\overline{\text{OE}}$	39	$\overline{\text{RAS}}$	72	$\overline{\text{BHE}}$	105	DA3
7	$\overline{\text{WE3}}$	40	VSS	73	ALE	106	DA2
8	MD31	41	$\overline{\text{CAS}}$	74	IRQ($\overline{\text{IRQ}}$)	107	DA1
9	MD30	42	MD7	75	EMEM	108	DA0
10	MD29	43	MD6	76	$\overline{\text{IOR}}$($\overline{\text{S1}}$)	109	$\overline{\text{EDBUFL}}$
11	MD28	44	MD5	77	$\overline{\text{IOW}}$($\overline{\text{CMD}}$)	110	VSYNC
12	MD27	45	MD4	78	$\overline{\text{MRD}}$(M/$\overline{\text{IO}}$)	111	HSYNC
13	MD26	46	MD3	79	$\overline{\text{MWR}}$($\overline{\text{S0}}$)	112	$\overline{\text{BLANK}}$
14	MD25	47	MD2	80	RESET	113	$\overline{\text{HTL}}$
15	MD24	48	MD1	81	$\overline{\text{0WS}}$	114	$\overline{\text{WPLT}}$
16	$\overline{\text{WE2}}$	49	MD0	82	IOCHRDY	115	$\overline{\text{RPLT}}$
17	VSS	50	VCC	83	VSS	116	VCC
18	VCC	51	VSS	84	VCC	117	VSS
19	MD23	52	$\overline{\text{WE0}}$	85	$\overline{\text{EIO}}$(3C3B0)	118	PCLK
20	MD22	53	MA0	86	$\overline{\text{ROM16}}$($\overline{\text{CSFB}}$)	119	VID0
21	MD21	54	MA1	87	$\overline{\text{EBROM}}$	120	VID1
22	MD20	55	MA2	88	$\overline{\text{EDBUFH}}$	121	VID2
23	MD19	56	MA3	89	A16	122	VID3
24	MD18	57	MA4	90	DA15	123	VID4
25	MD17	58	MA5	91	DA14	124	VID5
26	MD16	59	MA6	92	DA13	125	VID6
27	$\overline{\text{RAS4}}$	60	MA7	93	DA12	126	VID7
28	$\overline{\text{RAS3}}$	61	MA8/$\overline{\text{RAS2}}$	94	DA11	127	VSS
29	VSS	62	A17	95	DA10	128	VCLK0
30	$\overline{\text{WE1}}$	63	A18	96	DA9	129	VCLK1
31	MD15	64	A19	97	DA8	130	VCLK2
32	MD14	65	A20	98	$\overline{\text{EABUF}}$	131	$\overline{\text{EXPCLK}}$
33	MD13	66	A21	99	VSS	132	$\overline{\text{EXVID}}$

TABLE 4-1. WD90C31 132-PIN JEDEC ASSIGNMENTS

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	N.C.	37	N.C.	73	N.C.	109	N.C.
2	VCC	38	VSS	74	VCC	110	VSS
3	MD23	39	$\overline{WE0}$	75	$\overline{EIO}$(3C3B0)	111	PCLK
4	MD22	40	MA0	76	$\overline{ROM16}$($\overline{CSFB}$)	112	VID0
5	MD21	41	MA1	77	$\overline{EBROM}$	113	VID1
6	MD20	42	MA2	78	$\overline{EDBUFH}$	114	VID2
7	MD19	43	MA3	79	A16	115	VID3
8	MD18	44	MA4	80	DA15	116	VID4
9	MD17	45	MA5	81	DA14	117	VID5
10	MD16	46	MA6	82	DA13	118	VID6
11	$\overline{RAS4}$	47	MA7	83	DA12	119	VID7
12	$\overline{RAS3}$	48	MA8/$\overline{RAS2}$	84	DA11	120	VSS
13	VSS	49	A17	85	DA10	121	VCLK0
14	$\overline{WE1}$	50	A18	86	DA9	122	VCLK1
15	MD15	51	A19	87	DA8	123	VCLK2
16	MD14	52	A20	88	$\overline{EABUF}$	124	$\overline{EXPCLK}$
17	MD13	53	A21	89	VSS	125	$\overline{EXVID}$
18	N.C.	54	N.C.	90	N.C.	126	N.C.
19	MD12	55	VSS	91	DIR	127	MDET
20	MD11	56	A22	92	DA7	128	USR1
21	MD10	57	A23	93	DA6	129	USR0
22	MD9	58	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	94	DA5	130	MCLK
23	MD8	59	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	95	DA4	131	VSS
24	$\overline{RAS}$	60	$\overline{BHE}$	96	DA3	132	$\overline{OE}$
25	VSS	61	ALE	97	DA2	133	$\overline{WE3}$
26	$\overline{CAS}$	62	IRQ	98	DA1	134	MD31
27	MD7	63	EMEM	99	DA0	135	MD30
28	MD6	64	$\overline{IOR}$($\overline{S1}$)	100	$\overline{EDBUFL}$	136	MD29
29	MD5	65	$\overline{IOW}$($\overline{CMD}$)	101	VSYNC	137	MD28
30	MD4	66	$\overline{MRD}$(M/$\overline{IO}$)	102	HSYNC	138	MD27
31	MD3	67	$\overline{MWR}$($\overline{S0}$)	103	$\overline{BLANK}$	139	MD26
32	MD2	68	RESET	104	$\overline{HTL}$	140	MD25
33	MD1	69	$\overline{OWS}$	105	$\overline{WPLT}$	141	MD24
34	MD0	70	IOCHRDY	106	$\overline{RPLT}$	142	$\overline{WE2}$
35	VCC	71	VSS	107	VCC	143	VSS
36	N.C.	72	N.C.	108	N.C.	144	N.C.

TABLE 4-2. WD90C31 144-PIN EIAJ ASSIGNMENTS

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			POWER ON
80 - 68	RESET	I	**RESET:** This signal resets the WD90C31. To initialize the WD90C31 during reset, MCLK and VCLK0 must be connected to the WD90C31. Western Digital configuration bits are initialized at power-up reset, based on the logic level on the MD15-MD0 bus, as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
4 - 130	MCLK	I	**MEMORY CLOCK:** This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
128 - 121	VCLK0	I	**VIDEO CLOCK 0:** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. VCLK0 is selected as clock when VCLK1 and VCLK2 are used as inputs and both Miscellaneous Output Register bits 2 and 3 set to 0.
129 - 122	VCLK1	I/O	**VIDEO CLOCK 1:** VCLK1 can be a second video display clock input or an output to an external clock selection module. The direction is determined at Reset by a pull-up/down resistor on MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. As an output, VCLK1 is an active low pulse during I/O writes to port 3C2H, or reflects the contents of 03C2H, Miscellaneous Register Bit 2. Refer to the Configuration Register and PR15 Register, Bit 5 description.
130 - 123	VCLK2	I/O	**VIDEO CLOCK 2:** VCLK2 is a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. VCLK2 performs as a user-defined external clock input, an output reflecting the state of Bit PR2(1) or represents the state of 03C2H, Miscellaneous Register, Bit 3, when CNF(3) is set to 1. See the Configuration Register and PR15 Register, Bit 5 description.

TABLE 4-3. SIGNAL DESCRIPTION

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
69 - 57 68 - 56 66 - 53 65 - 52 64 - 51 63 - 50 62 - 49	A23 A22 A21 A20 A19 A18 A17	I I I I I I I	**ADDRESS BUS (A23 - A17):** In Micro Channel mode, A23-A17 should be connected to address bus SA23 - SA17. In AT mode, A23-17 should be connected to LA23-LA17 of the AT address bus.
89 - 79	A16	I	**ADDRESS BUS (A16):** Bit SA16 of CPU address bus.
73 - 61	ALE	I	**ADDRESS LATCH ENABLE**: In AT mode, A23-A17 are latched internally at the falling edge of the ALE. In Micro Channel mode, ALE is not used and should be connected to VSS.
90 - 80 91 - 81 92 - 82 93 - 83 94 - 84 95 - 85 96 - 86 97 - 87 101 - 92 102 - 93 103 - 94 104 - 95 105 - 96 106 - 97 107 - 98 108 - 99	DA15 DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	**DATA/ADDRESS BUS:** This is the multiplexed CPU data and address bus. $\overline{\text{EABUF}}$ = 0: Enables the external address buffer. $\overline{\text{EDBUFL}}$ = 0 or $\overline{\text{EDBUFH}}$ = 0: Enables the external bidirectional data buffers. DIR controls the data flow for the data buffer.
82 - 70	IOCHRDY	O	**IO CHANNEL READY**: IOCHRDY indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C31 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.

TABLE 4-3. SIGNAL DESCRIPTION (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
74 - 62	IRQ/($\overline{\text{IRQ}}$)	O	**INTERRUPT REQUEST:** This programmable processor interrupt request is enabled via Bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal is active, causing the interrupt. It stays active until cleared by CRTC11 Bit 4. An AT system uses IRQ as an active high signal. Although an AT system does not usually use IRQ it may be connected if desired. The Micro Channel mode uses $\overline{\text{IRQ}}$ as an active low to generate interrupts.
71 - 59	$\overline{\text{MEMCS16}}$/ ($\overline{\text{CDDS16}}$)	O	**MEMORY CHIP SELECT 16 BITS:** In AT mode, $\overline{\text{MEMCS16}}$ is used to inform the host that the WD90C31 is capable of performing the requested 16-bit video memory data transfer. In Micro Channel mode, $\overline{\text{CDDS16}}$ is used to indicate 16-bit video memory or I/O access.
85 - 75	$\overline{\text{EIO}}$/ (3C3B0)	I	**ENABLE I/O:** In AT mode, $\overline{\text{EIO}}$ is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, $\overline{\text{EIO}}$ is enabled by I/O port 3C3 bit 0 = 1, and is used to enable video subsystem memory and I/O address decoding.
87 - 77	$\overline{\text{EBROM}}$	O	**ENABLE BIOS ROM:** This is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A write to WD90C31 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
113 - 104	$\overline{\text{HTL}}$	O	**ENABLE HIGH-TO-LOW:** (for 16-bit BIOS) If only an eight-bit CPU interface is used, this output enables a data buffer to allow reading of the upper byte of ROM data on the lower data bus when two ROMs (16-bit) are supported.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
75 - 63	EMEM	I	**ENABLE MEMORY:** When asserted, EMEM enables memory decoding. It is normally connected to the Refresh signal.
72 - 60	$\overline{BHE}$	I	**BYTE HIGH ENABLE:** $\overline{BHE}$ should be connected to $\overline{BHE}$ of the AT or Micro Channel bus. $\overline{BHE}$, SA0 = 00 - Word transfer = 01 - High byte transfer = 10 - Low byte transfer = 11 - Illegal
81 - 69	$\overline{0WS}$	O	**ZERO WAIT STATE:** $\overline{0WS}$ is asserted to generate a zero wait state to the AT bus. $\overline{0WS}$ can be programmed by the PR33 register, bits 7 and 6 to generate a zero wait state under four possible conditions. Refer to section 7.7.26 PR33 DRAM Timing And Zero Wait State Register.
78 - 66	$\overline{MRD}$/(M/$\overline{IO}$)	I	**MEMORY READ:** In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
79 - 67	$\overline{MWR}$/($\overline{S0}$)	I	**MEMORY WRITE:** In AT mode $\overline{MWR}$ is the memory write strobe. In Micro Channel mode $\overline{S0}$ is the channel status signal and indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$ and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
76 - 64	$\overline{IOR}$/($\overline{S1}$)	I	**I/O READ:** In AT mode $\overline{IOR}$ is the I/O read strobe. In Micro Channel mode, $\overline{S1}$ is the channel status signal that indicates the start and type of a channel cycle.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
77 - 65	$\overline{IOW}$/($\overline{CMD}$)	I	**I/O WRITE:** In AT mode, $\overline{IOW}$ strobe signals an I/O write. In Micro Channel mode $\overline{CMD}$ is the bus data strobe. Address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
70 - 58	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	**I/O CHIP SELECT 16 BITS:** In AT mode, $\overline{IOCS16}$ is an output, and is used to inform the host that the WD90C31 is capable of performing the requested 16-bit I/O accesses. In Micro Channel mode, this signal is an input driven by the host to individually select channel connector slots during system configuration.
100 - 91	DIR	O	**DIRECTION CONTROL:** DIR is the Direction Control for external bus buffers in both AT and Micro Channel implementation. The default state is low until a read cycle occurs. The WD90C31 then drives DIR high to change the direction of the data buffers.
88 - 78	$\overline{EDBUFH}$	O	**ENABLE DATA BUFFER HIGH:** $\overline{EDBUFH}$ may be used to enable an external data buffer for data bits D15 through D8.
109 - 100	$\overline{EDBUFL}$	O	**ENABLE DATA BUFFER LOW:** $\overline{EDBUFL}$ may be used to enable an external data buffer for data bits D7 through D0.
98 - 88	$\overline{EABUF}$	O	**ENABLE ADDRESS BUFFER:** $\overline{EABUF}$ may be used to enable an external address buffer.

TABLE 3. SIGNAL DESCRIPTION (Continued)

NOTE:
( ) Signals enclosed in parentheses are Micro Channel only.

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE (Cont.)
86 - 76	ROM16/ (CSFB)/ EXBLANK	I/O	**BIOS ROM SELECT 16 BITS:** In AT Mode, ROM16 is an output and decodes the ROM address LA(23-17) for space 0C0000 - 0DFFFF. It may be combined with SA16 and SA15 externally to control MCS16 for the address space C0000 - C7FFF. If CNF(17) is set to 0 at power up reset, the ROM16 address decoding is disabled. ROM16 then reflects the status of PR1 bit 1. **CARD SELECT FEEDBACK:** In Micro Channel mode, CSFB is an output and is used as Card Selected Feedback to provide positive acknowledgement of its presence at the specified host's addresses. **EXTERNAL BLANK:** In AT or Micro Channel Mode, EXBLANK becomes an input if CNF(18) is set to zero (MD18 = 0 at power-up reset). EXBLANK = 1: Enables BLANK, VSYNC and HSYNC outputs. EXBLANK = 0: Tristate BLANK, VSYNC and HSYNC outputs.
			DISPLAY MEMORY INTERFACE
41 - 26	CAS	O	**COLUMN ADDRESS STROBE:** CAS is the Column Address Strobe for two, four and eight DRAM configurations.
39 - 24	RAS	O	**ROW ADDRESS STROBE:** RAS is the Row Address Strobe for the 256K by 4, or 256K by 16 DRAM interface. If 64K by 16 DRAMS are used, RAS is the strobe for the first 256 Kbyte memory bank. *For RAS2 see pin 61 in Video Memory Address section.*
28 - 12	RAS3	O	**ROW ADDRESS STROBE 3:** RAS3 is used only if eight 64K by 16 DRAMs are used. It controls the third 256 Kbyte memory bank.
27 - 11	RAS4	O	**ROW ADDRESS STROBE 4:** RAS4 is used only if eight 64K by 16 DRAMs are used. It controls the fourth 256 Kbyte memory bank.
6 - 132	OE	O	**OUTPUT ENABLE:** OE is the Output Enable signal for two, four and eight DRAM configurations.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
DISPLAY MEMORY INTERFACE (Cont.)			
52 - 39	$\overline{WE0}$	O	**WRITE ENABLE:** $\overline{WE0}$ is the write enable signal for MD7 through MD0.
30 - 14	$\overline{WE1}$	O	**WRITE ENABLE:** $\overline{WE1}$ is the write enable signal for MD15 through MD8.
16 - 142	$\overline{WE2}$	O	**WRITE ENABLE:** $\overline{WE2}$ is the write enable signal for MD23 through MD16.
7 - 133	$\overline{WE3}$	O	**WRITE ENABLE:** $\overline{WE3}$ is the write enable signal for MD31 through MD24.
PROGRAMMABLE OUTPUTS			
3 - 129	USR0	O	May be used to control special card or system features (see PR32 register).
2 - 128	USR1	O	May be used to control special card or system features (see PR32 register).

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
VIDEO MEMORY DATA			
8 - 134	MD31	I/O	**DISPLAY MEMORY DATA (MD31 through MD0):** These lines are the data bus to the video display DRAMS. The MD18-MD0 data lines are pulled up by internal 50 Kohm resistors, but may be pulled down by external 4.7 Kohm resistors to provide setup information on power-up reset as follows:
9 - 135	MD30	I/O	
10 - 136	MD29	I/O	
11 - 137	MD28	I/O	
12 - 138	MD27	I/O	
13 - 139	MD26	I/O	
14 - 140	MD25	I/O	
15 - 141	MD24	I/O	
19 - 3	MD23	I/O	
20 - 4	MD22	I/O	
21 - 5	MD21	I/O	
22 - 6	MD20	I/O	
23 - 7	MD19	I/O	
24 - 8	MD18	I/O	
25 - 9	MD17	I/O	
26 - 10	MD16	I/O	
31 - 15	MD15	I/O	
32 - 16	MD14	I/O	
33 - 17	MD13	I/O	
34 - 19	MD12	I/O	
35 - 20	MD11	I/O	
36 - 21	MD10	I/O	
37 - 22	MD9	I/O	
38 - 23	MD8	I/O	
42 - 27	MD7	I/O	
43 - 28	MD6	I/O	
44 - 29	MD5	I/O	
45 - 30	MD4	I/O	
46 - 31	MD3	I/O	
47 - 32	MD2	I/O	
48 - 33	MD1	I/O	
49 - 34	MD0	I/O	

MD	POWER-UP FUNCTION	REGISTER (BIT)
18	Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$	CNF(18) +
16	64K by 16 or 256K by 4 DRAM Select	CNF(16) +
15	EGA SW4/General Purpose	PR11(7) +
14	EGA SW3/General Purpose	PR11(6) +
13	EGA SW2/General Purpose	PR11(5) +
12	EGA SW1/General Purpose	PR11(4) +
11	ANALOG/TTL Display	CNF(8) *
10	Set 16-bit ROM	CNF(10) *
9	3C3H or 46E8H I/O port for wake up	CNF(9) +
8	A23-A20 connection	CNF(11) +
7	General Purpose	CNF(7) *
6	General Purpose	CNF(6) *
5	General Purpose	CNF(5) *
4	General Purpose	CNF(4) *
3	VCLK1,2 I/O	CNF(3) +
2	AT/Micro Channel Mode	CNF(2) +
1	1 or 2 ROMs	CNF(1) *
0	BIOS ROM Mapping	PR1(0) *

NOTES:
"*" Pulldown resistor sets these bits to logic 1.
"+" Pulldown resistor sets these bits to logic 0.
For more details refer to PR and Configuration Registers.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
			VIDEO MEMORY ADDRESS
61 - 48 60 - 47 59 - 46 58 - 45 57 - 44 56 - 43 55 - 42 54 - 41 53 - 40	MA8/$\overline{RAS2}$ MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	**MEMORY ADDRESS (MA8 through MA0):** Display memory DRAM address. For testing purposes, these pins can be tristated by setting Register PR4(4)=1. MA8/$\overline{RAS2}$ is an active low RAS strobe for the second 256 Kbyte memory bank if four 64K by 16 DRAMs are used.
			RAMDAC INTERFACE
126 - 119 125 - 118 124 - 117 123 - 116 122 - 115 121 - 114 120 - 113 119 - 112	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	O O O O O O O O	**VIDEO (VD7-VD0):** Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
115 - 106	$\overline{RPLT}$	O	**READ PALETTE:** Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H and 3C9H.
114 - 105	$\overline{WPLT}$	O	**WRITE PALETTE:** Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H through 3C9H.
118 - 111	PCLK	O	**PIXEL CLOCK:** Video pixel clock output used by the DAC to latch video signals VID7 through VID0. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output Register.
			CRT CONTROL
112 - 103	$\overline{BLANK}$	O	**BLANK**: Active low display monitor blank pulse to external RAMDAC.
111 - 102	HSYNC/ $\overline{HSYNC}$	O	**HORIZONTAL SYNC:** Display monitor horizontal synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.

TABLE 4-3. SIGNAL DESCRIPTIONS (Continued)

PIN NUMBER JEDEC - EIAJ	MNEMONIC	I/O	DESCRIPTION
CRT CONTROL (Cont.)			
110 - 101	VSYNC/ $\overline{\text{VSYNC}}$	O	**VERTICAL SYNC:** Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
1 - 127	MDET	I	**MONITOR DETECT:** When the RAMDAC is external, MDET is used to determine the monitor type and can be read at port 3C2H Bit 4.
FEATURE CONNECTOR SUPPORT			
132 - 125	$\overline{\text{EXVID}}$	I	**ENABLE EXTERNAL VIDEO DATA:** A Feature Connector input. A low tristates the video data lines VID7:0. An internal pullup resistor is provided.
131 - 124	$\overline{\text{EXPCLK}}$	I	**ENABLE EXTERNAL PIXEL CLOCK:** A Feature Connector input. A low tristates the PCLK output. An internal pullup resistor is provided.
POWER AND GROUND			
18 - 2	VCC	-----	+5VDC
50 - 35	VCC	-----	+5VDC
84 - 74	VCC	-----	+5VDC
116 - 107	VCC	-----	+5VDC
5 - 13	VSS	-----	Ground
17 - 25	VSS	-----	Ground
29 - 38	VSS	-----	Ground
40 - 55	VSS	-----	Ground
51 - 71	VSS	-----	Ground
67 - 89	VSS	-----	Ground
83 - 110	VSS	-----	Ground
99 - 120	VSS	-----	Ground
117 - 131	VSS	-----	Ground
127 - 143	VSS	-----	Ground
- 1 - 18 - 36 - 37 - 54 - 72 - 73 - 90 - 108 - 109 - 126 - 144			These pins are not connected in the 144-pin EIAJ package

TABLE 4-3. SIGNAL DESCRIPTION (Continude)

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C 32°F to 158°F
Storage Temperature	-40°C to 125°C -40°F to 257°F
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0°C to 70°C 32°F to 158°F
Power Supply Voltage	4.75 to 5.25 Volts
Power Dissipation	140 mA

5.2 DC CHARACTERISTICS

The WD90C31 outputs have 4.0 mA maximum source and sink capability (see Table 5-1), except as follows:

IRQ, IOCHRDY, $\overline{0WS}$,
$\overline{MEMCS16}$, $\overline{IOCS16}$ = 24 mA sink.

PCLK, VID7:0, $\overline{BLANK}$ = 10 mA source/sink.

DRAM Interface = 4.0 mA source/sink
(RAS, CAS, $\overline{WE}$, $\overline{OE}$, MA, MD)

HSYNC, VSYNC, DA15:0 = 6 mA sink.

$\overline{ROM16}$ = 16 mA sink.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz
C(I/O)	I/O Pin Capacitance	--	12	pF	FC=1 MHz

TABLE 5-1. DC CHARACTERISTICS

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

- All units are in nanoseconds.
- CL = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the spec number in column 1 of the same table.

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK (For configuration at power up.)
2	MD Setup to RESET low	50		
3	MD Hold from RESET low	30		
4	RESET low to first $\overline{IOW}$	10t		
	CLOCK TIMING			
1 *	VCLK period	12.5	72.0	
2	VCLK high	5		At 1/2 VDD
3	VCLK low	5		At 1/2 VDD
4 *	Clock rise time		2	1V - (VDD - 1V)
5 *	Clock fall time		2	1V - (VDD - 1V)
6	VCLK to PCLK delay	8	20	45 ns at 120 pF load
7a	VCLK to HSYNC delay	8	25	
7b	VCLK to VSYNC delay	8	25	
7c	VCLK to $\overline{BLANK}$ delay	8	20	
7d	VCLK to VID(7:0) delay	8	20	45 ns at 120 pF load up to 30 MHz
8 **	MCLK period	20	30	Max 50 MHz, Min 33.3 MHz
9	MCLK high	8		At 1/2 VDD
10	MCLK low	8		At 1/2 VDD
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

* Apply to both VCLK and MCLK.

** VCLK0 and MCLK use CMOS level input buffers. $V(IL)_{max}$ = 1.5 V, $V(IH)_{min}$ = VDD - 1.5 V

TABLE 6-1. AC TIMING CHARACTERISTICS

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$, $\overline{MWR}$ high	10		
3a	A(23:17) setup to ALE low	20		
3b	$\overline{BHE}$, DA(15:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	18		
4a	A(23:17) hold from ALE low	10		
4b	DA(15:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	10		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	10		
7a	$\overline{EABUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	9	25	
7b	$\overline{EDBUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ low	13.5	35	
7c	$\overline{HTL}$ low from $\overline{MRD}$ low		25	
8a	$\overline{EABUF}$ low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	14.5	35	
8b	$\overline{EDBUF}$ high from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ high	8.5	25	
8c	$\overline{HTL}$ high from $\overline{MRD}$ high		25	
9	DIR high from $\overline{IOR}$, $\overline{MRD}$ low		20	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		20	
11	DA(15:0) write data setup to $\overline{IOW}$, $\overline{MWR}$ high	20		
12a	DA(15:0) read data hold from $\overline{IOR}$ high or $\overline{MRD}$ high	10		
12b	DA(15:0) write data hold from $\overline{IOW}$, $\overline{MWR}$ high	10		
13	DA(15:0) read data valid after $\overline{IOR}$ low		70	
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15	Memory read data valid from RDY high		40	Note 1
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	20	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		37	
20b	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high	9	15	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high	9	20	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		1t + 20	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		25	
24	VCLK1 low from $\overline{IOW}$ low (3C2H port)		1t + 24	

TABLE 6-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
25	VCLK1 high from $\overline{IOW}$ high (3C2H port)		15	
26	A(15:0) valid to $\overline{IOCS16}$ low		35	C_L = 100pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		20	C_L = 100pF
28	A(23:17) valid to $\overline{MEMCS16}$ or $\overline{ROM16}$ low		39	C_L = 100pF
29	$\overline{MEMCS16}$ tristate from the next active ALE		39	C_L = 100pF
30a	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ high	2t + 15		t = ^{1}/MCLOCK Note 2
30b	$\overline{IOR}$, $\overline{IOW}$, $\overline{MWR}$, $\overline{MRD}$ low	2t		t=^{1}/MCLOCK (Note 3)
30c	ALE pulse width	30		
31	$\overline{OWS}$, low from $\overline{IOW}$, $\overline{MWR}$ low		15	C_L = 100pF

Note 1: Depends on setting of PR31 (3C5H, index 11H) bits 4, 3. t = ^{1}/MCLOCK
00 - Max 40
01 - Max 40 + 1t
10 - Max 40 + 2t
11 - Max 40 - 1t

Note 2: Minimum of #30a should be the greater of 2t + 15 or (#8a + #3b + delay on the external address buffer)

Note 3: Minimum of #30b should be the greater of 2t or (#7b + #11 + delay on the external data buffer)

TABLE 6-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTICS	MIN	MAX	TEST CONDITION
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	10		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low	13.5	35	
7b	$\overline{EABUF}$ high from $\overline{CMD}$ low	9	25	
8a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high	8.5	25	
8b	$\overline{EABUF}$ low from $\overline{CMD}$ high	14.5	35	
9	DIR active from $\overline{CMD}$ low		20	
10	DIR inactive from $\overline{CMD}$ high		20	
11	$\overline{CSFB}$ delay from valid address/status		30	C_L = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	DA(15:0) write data setup to $\overline{CMD}$ high	20		
17	DA(15:0) Write data hold after $\overline{CMD}$ high	10		
18	DA(15:0) I/O Read data valid from $\overline{CMD}$ low		70	
19	RDY high delay from $\overline{CMD}$ low	0	2.45 µs	
20	DA(15:0) Memory Read Data valid from RDY high		40	Note 1
21a	$\overline{CMD}$ high (inactive)	2t + 15		Note 2
21b	$\overline{CMD}$ low	2t		Note 3
22	RDY low delay from valid address/status		30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low	9	20	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high	9	20	
27	VCLK1 low from $\overline{CMD}$ low (3C2 port)		1t + 30	
28	VCLK1 high from $\overline{CMD}$ high (3C2 port)		25	

Note 1: Depends on setting of PR31 (3C5H, Index 11H) bits 4, 3. t = ^{1}/MCLK
00 max 40 ns
01 max 40 ns + 1t
10 max 40 ns + 2t
11 max 40 ns - 1t

Note 2: Minimum of #21a is the greater of 2t + 5 or (#8b + #1 + delay on external address buffer)

Note 3: Minimum of #21b is the greater of 2t or (#7a + #16 + delay on external data buffer)

TABLE 6-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	DRAM TIMING (256K By 256K By 16)			
1	$\overline{RAS}$ cycle time	*6t		
2	$\overline{RAS}$ pulse width low	*3.5t-d		
3	$\overline{RAS}$ high time (precharge)	*2.5t+d		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*2.5t-9	2.5t - d	
5	$\overline{CAS}$ cycle time	2t		
6	$\overline{CAS}$ pulse width low	*1t + d		
7	$\overline{CAS}$ high time (precharge)	*1t - d		
8	Row address setup to $\overline{RAS}$ low	1t - 10		
9	Row address hold time from $\overline{RAS}$ low	1t		
10	Column address setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	3		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup $\overline{CAS}$ low	1t- 5	1t + 5	
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as CAS low		
18	$\overline{OE}$ high before $\overline{WE}$ low	2t - 10		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	1t - 10		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t+10		

Notes:
The timing is the result of setting PR33 (3C5, Index = 13) = XXX00000
* Timings are adjustable by PR33.
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 1.
t = ^{1}/MCLK
(MCLK = 37.5 MHz for 80 ns DRAM)
(MCLK = 40 MHz for some faster 80ns DRAM)
(MCLK = 44.4 MHz for 70 ns DRAM)
(MCLK = 49.5 MHz for 60 ns DRAM)
} Maximum MCLK frequency
d = Delay with a min. of 4 ns and a max. of 7 ns.

TABLE 6-1. AC TIMING CHARACTERISTICS (Continued)

NUMBER	CHARACTERISTIC	MIN	MAX	TEST CONDITION
	DRAM TIMING (64 Kbytes by 16)			
1	$\overline{RAS}$ cycle time	*5t		
2	$\overline{RAS}$ pulse width low	*3t		
3	$\overline{RAS}$ high time (precharge)	*2t		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	*1.5t	1.5t	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	*1t+2d		
7	$\overline{CAS}$ high time (precharge)	*1t-2d		
8	Row address setup to $\overline{RAS}$ low	1t		
9	Row address hold time from $\overline{RAS}$ low	1/2t		
10	Column adress setup to $\overline{CAS}$ low	1t - 10		
11	Column address hold from $\overline{CAS}$ low	1t		
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read Data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t - 15		
15	Write Data hold after $\overline{CAS}$ low	1t - 5		
16	$\overline{WE}$ low setup before $\overline{CAS}$ low	1t - 10		
17	$\overline{WE}$ low hold after $\overline{CAS}$ high	Same as CAS low		
18	$\overline{OE}$ high before $\overline{WE}$ low	1t + 2		
19	$\overline{OE}$ low after $\overline{WE}$ high	1t - 10		
20	$\overline{CAS}$ high for $\overline{CAS}$ before $\overline{RAS}$ refresh	0.5t		
21	$\overline{RAS}$ low from $\overline{CAS}$ low for $\overline{CAS}$ before $\overline{RAS}$ refresh	1.5t		

MCLK edge to $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns.

NOTES:
The timing is the result of setting PR33 (3C5H, Index = 13H) = xxx01110
* Timings are adjustable by PR33
Memory write uses fast page early write, while keeping $\overline{OE}$ = 1.
Memory read uses fast page read, while keeping $\overline{OE}$ = 0.
t = ^{1}/MCLK (MCLK = 36 MHz for 80 ns, 64K by 16 DRAM)
d = Delay with a min. of 4 ns and a max. of 7 ns.

TABLE 6-1. AC TIMING CHARACTERISTICS (Continude)

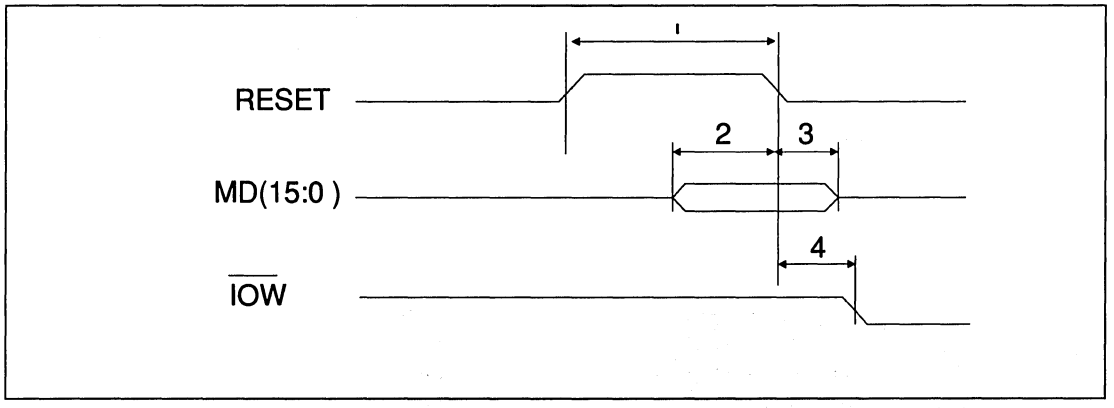

FIGURE 6-1. RESET TIMING

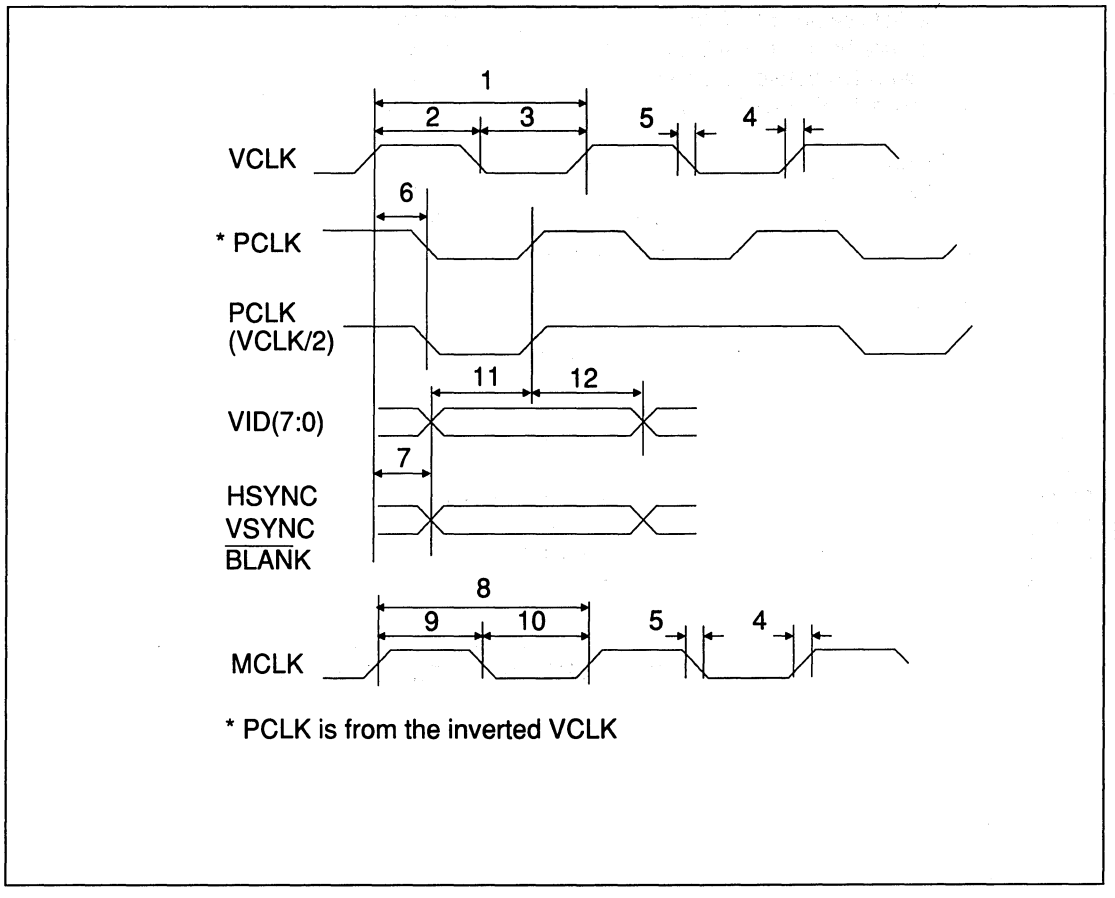

FIGURE 6-2. CLOCK AND VIDEO TIMING

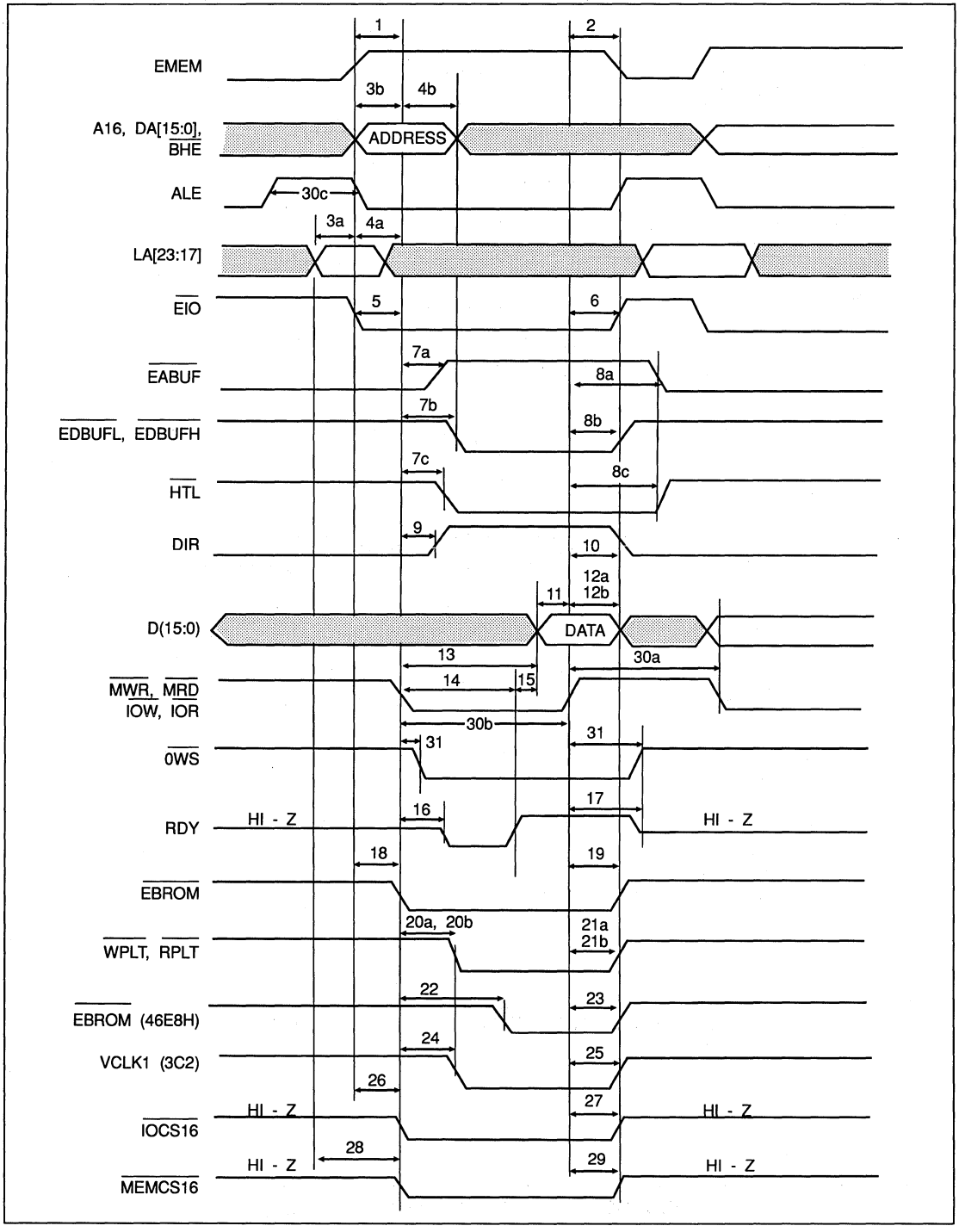

FIGURE 6-3. AT MODE BUS TIMING

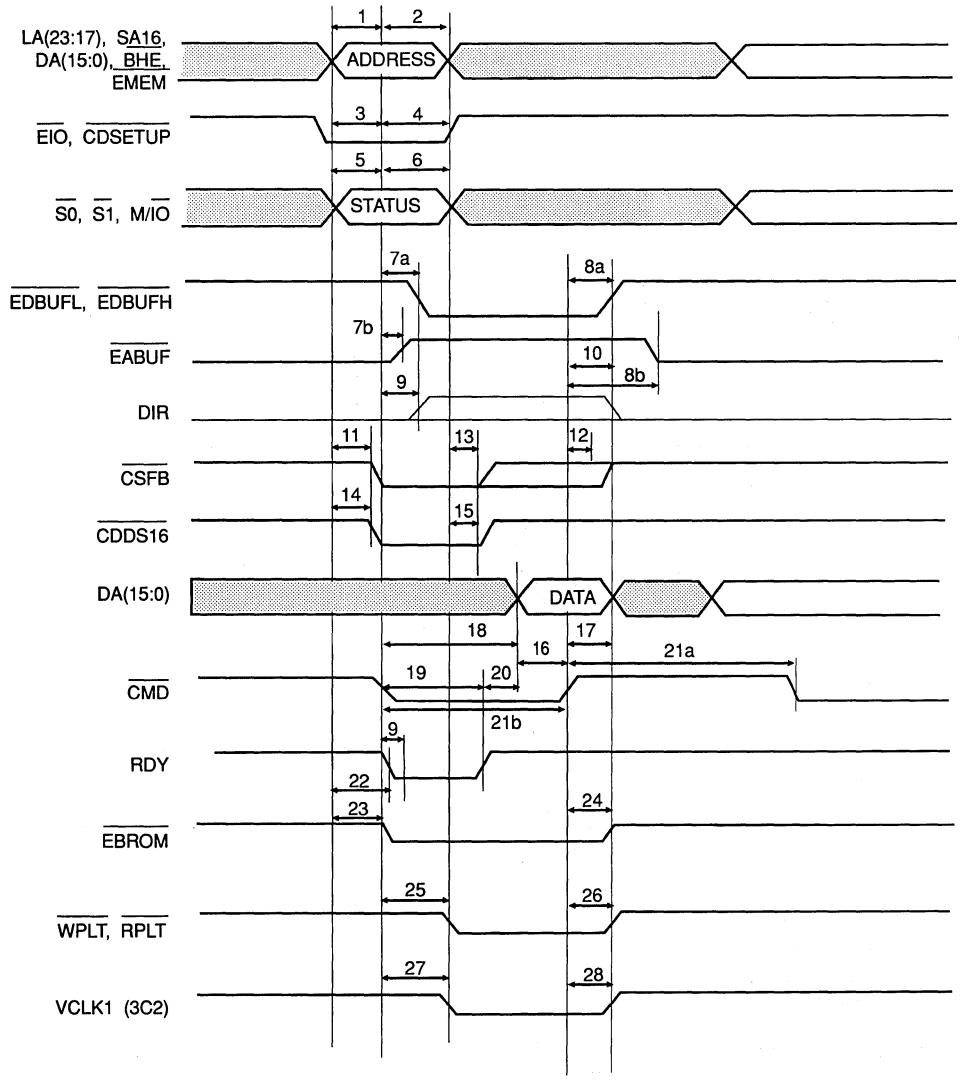

FIGURE 6-4. MICRO CHANNEL MODE BUS TIMING

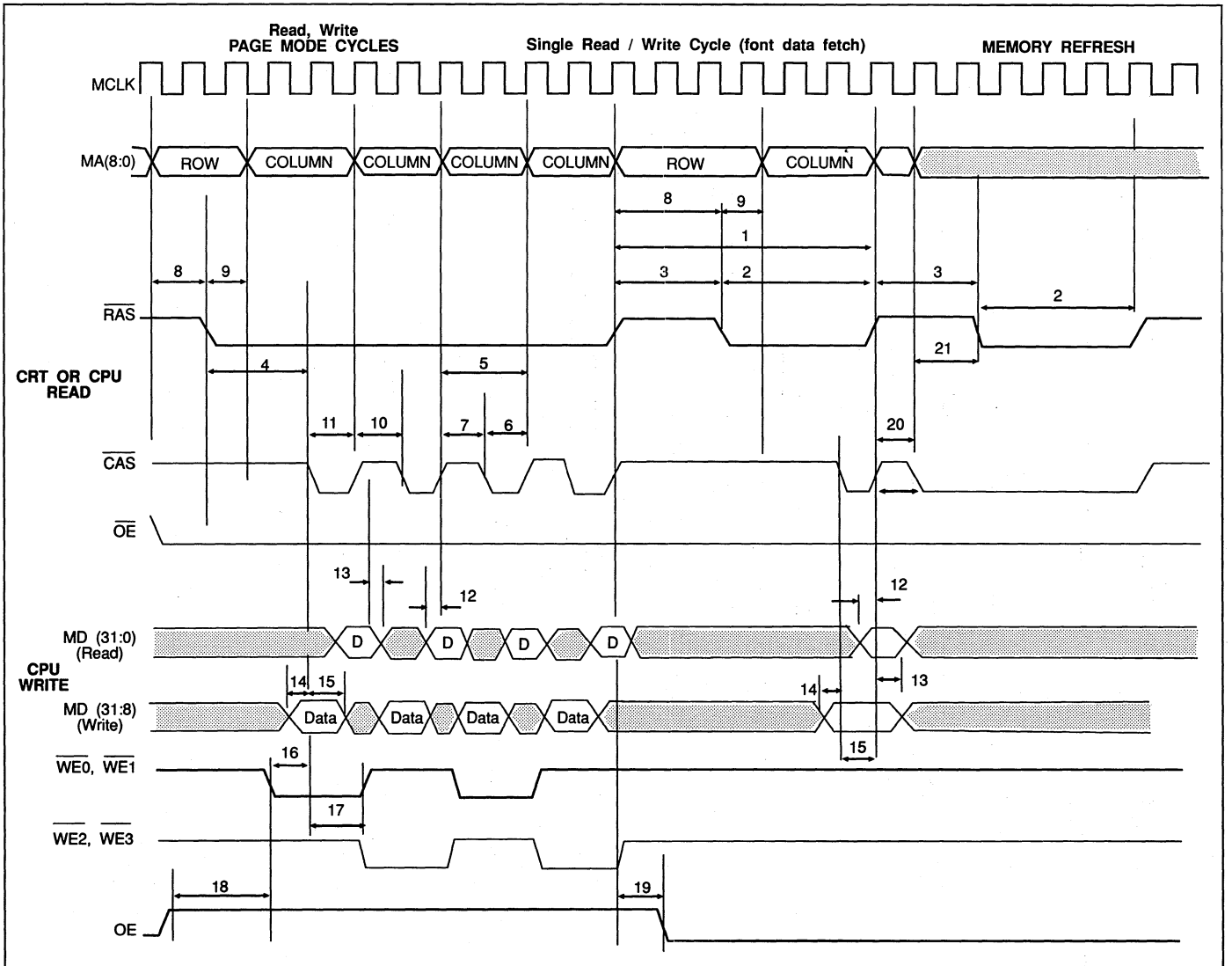

FIGURE 6-5. DRAM TIMING

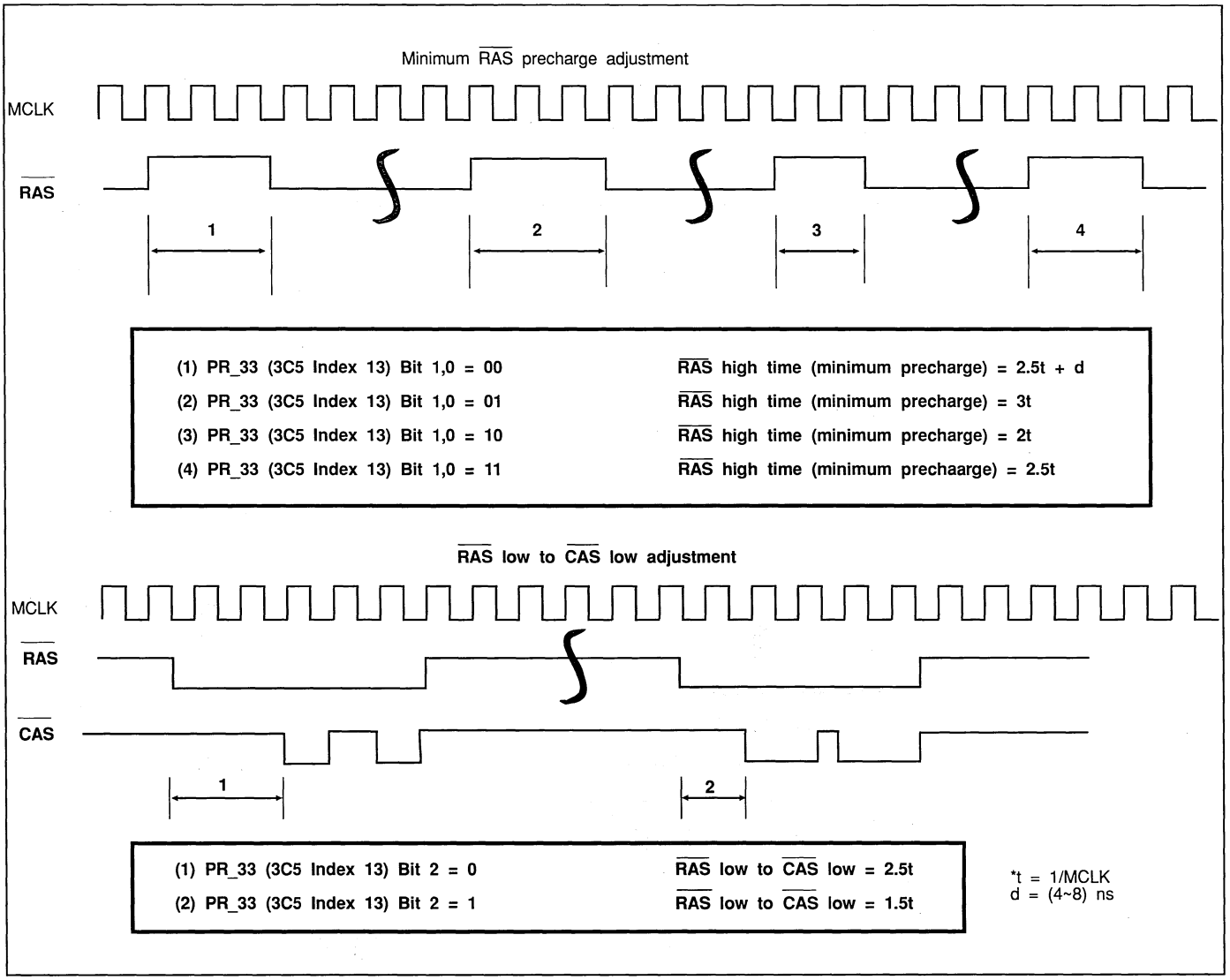

FIGURE 6-6. DRAM TIMING ADJUSTMENT

DRAM Timing Adjustment: The RAS, CAS timing can be adjusted by register PR33 (3C5H, Index 3H) bits 4 through 0. Only the following timing may be affected: (See Figures 6-5 and 6-6).

3 $\overline{RAS}$ high time (precharge)
4 $\overline{RAS}$ low to CAS low
6 $\overline{CAS}$ pulse width

$\overline{CAS}$ pulse width adjustment: $\overline{CAS}$ cycle time is always equal to 2t {t = 1/MCLK}, {d = (4~ 8) ns}.

PR33 (Bits 4 through 3) =
00, $\overline{CAS}$ low = 1t + d; $\overline{CAS}$ high = 1t - d
01, $\overline{CAS}$ low = 1t + 2d; $\overline{CAS}$ high = 1t - 2d
1X, $\overline{CAS}$ low = 1.5t; $\overline{CAS}$ high = $^1/2$t

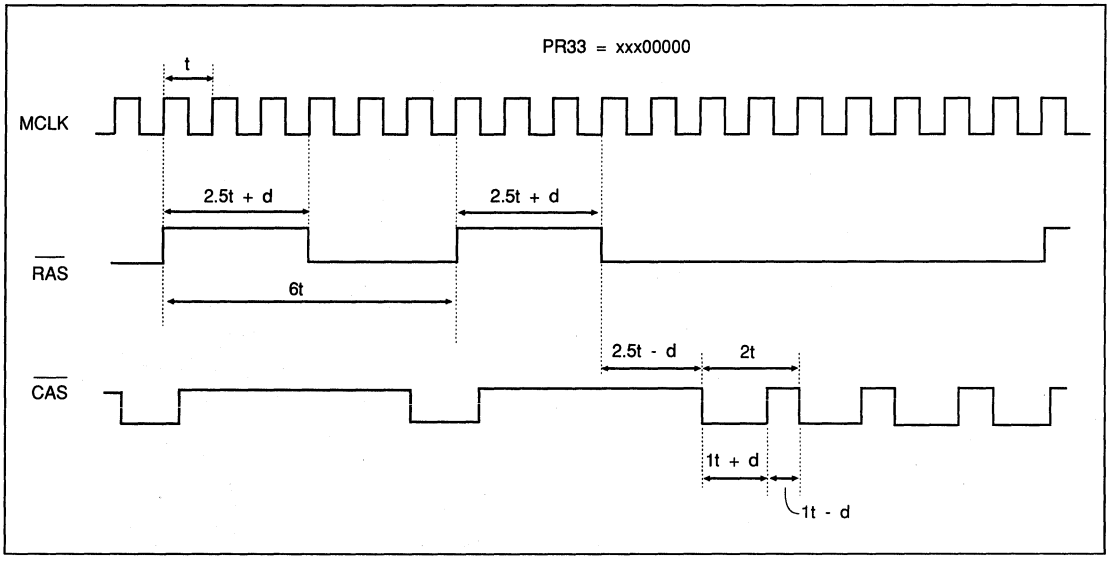

FIGURE 6-7. 256K BY 4 DRAM TIMING

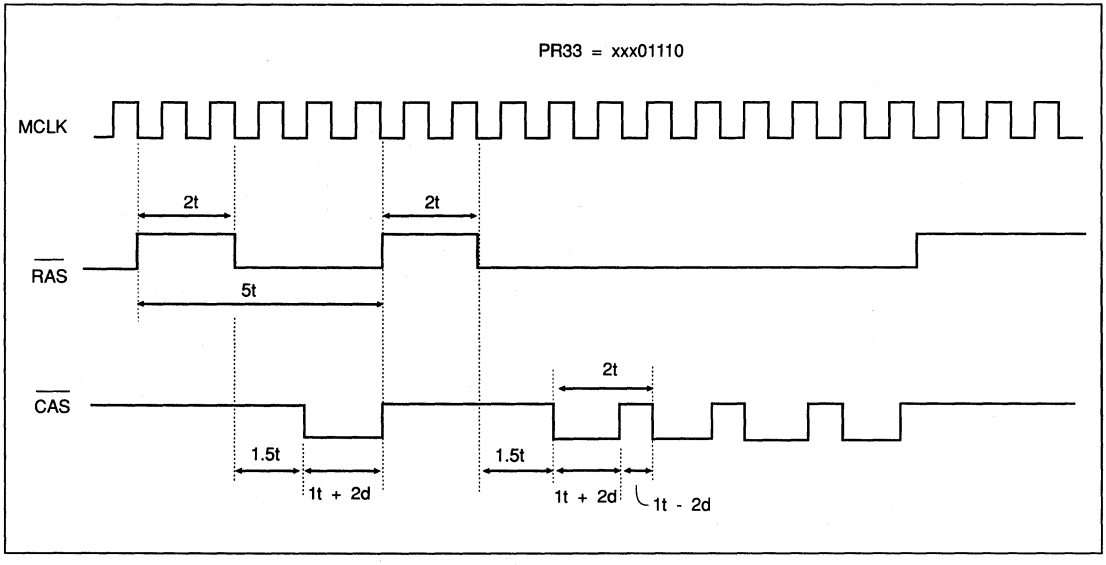

FIGURE 6-8. 64K BY 16 DRAM TIMING

7.0 WD90C31 REGISTERS

All the standard IBM registers incorporated inside the WD90C31 are functionally equivalent to the VGA implementation, while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

Throughout this section, all bit graphics and definitions apply to VGA mode, followed by their brief description.

② REGISTERS	① RW	MONO	COLOR
GENERAL REGISTERS			
Miscellaneous Output Register	W	3C2	3C2
	R	3CC	3CC
Input Status Register 0	RO	3C2	3C2
Input Status Register 1	RO	3BA	3DA
Feature Control Register	W	3BA	3DA
	R	3CA	3CA
* Video Subsystem Enable Register.	RW	3C3	3C3
* I/O Port 3C3H can be used to replace 46E8H [if CNF(9) = 0] for setup in AT mode. In Micro Channel mode, writes to 3C3H, Bit 0 = 1 enables memory and I/O address decoding.			
SEQUENCER REGISTERS			
Sequencer Index Register	RW	3C4	3C4
Sequencer Data Register	RW	3C5	3C5
CRT CONTROLLER REGISTERS			
Index Register	RW	3B4	3D4
CRT Controller Data Register	RW	3B5	3D5
GRAPHICS CONTROLLER REGISTERS			
Index Register	RW	3CE	3CE
Other Graphics Registers	RW	3CF	3CF
ATTRIBUTE CONTROLLER REGISTERS			
Index Register	RW	3C0	3C0
Attribute Controller Data Register	W	3C0	3C0
	R	3C1	3C1
VIDEO DAC PALETTE REGISTERS			
Write Address	RW	3C8	3C8
Read Address	W	3C7	3C7
DAC State	R	3C7	3C7
Data	RW	3C9	3C9
Pel Mask	RW	3C6	3C6
① RO = Read-Only, RW = Read/Write, W = Write, and R = Read. ② All Register addresses are in hexidecimal.			

TABLE 7-1. VGA REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
PR18 CRTC Vertical Timing Overflow	RW	3B5.3E	3B5.3E
PR19 Signature Analyzer Control	RW	3B5.3F	3D5.3F
Reserved 3X5.31- 3X5.3C	RW	3B5.31 - 3B5.3C	3D5.31 - 3D5.3C
PR1A CRTC Shadow Register Control	RW	3B5.3D	3D5.3D
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21 Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR22 Scratch Pad	RW	3C5.8	3C5.8
PR23 Scratch Pad	RW	3C5.9	3C5.9
PR30 Memory Interface write buffer and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12
PR33 DRAM Timing and Zero Wait State Control Registers	RW	3C5.13	3C5.13
PR34 Video Memory Mapping Register	RW	3C5.14	3C5.14
PR35 USR0, USR1 Output Select Register	RW	3C5.15	3C5.15

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers description for more details.

Register descriptions from locations such as 3CF.09 is the value read from or written to location 3CFH after a value of 09 has been written to the corresponding Index register 3CEH.

TABLE 7-2. PR REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

TABLE 7-3. COMPATIBILITY REGISTERS SUMMARY

7.1 GENERAL REGISTERS

REGISTER NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES
1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

7.1.1 Miscellaneous Output Register, Read Port = 3CCH, Write Port = 3C2H

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 - Vertical Sync Polarity Selection.

0 = Positive vertical sync polarity.

1 = Negative vertical sync polarity.

Bit 6 - Horizontal Sync Polarity Selection.

0 = Positive horizontal sync polarity.

1 = Negative horizontal sync polarity.

The vertical and horizontal sync polarity bits (bits 7:6) should be set to conform with the vertical size of the frame used by the monitor.

VERTICAL FRAME

00 = Reserved

01 = 400 lines/scan

10 = 350 lines/scan

11 = 480 lines/scan

Bit 5 - Odd or Even Memory Page Select.

When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.

0 = Lower page is selected.

1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bits (3:2) - Clock Select 1, 0.

00 = Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).

01 = Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register Bit 3 = 0.

10 = Selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

11 = Reserved. Also selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

Bit 1 - System Processor Video RAM Access Enable.

0 = CPU access disabled.

1 = CPU access enabled.

Bit 0 - CRT Controller I/O Address Range Selection.

Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).

1 = CRTC and status addresses for CGA mode (3DX).

7.1.2 Input Status Register 0, Read Only Port = 3C2H

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7 - CRT Vertical Retrace Interrupt Pending or Cleared.

0 = Vertical retrace interrupt cleared.

1 = Vertical retrace interrupt pending.

Bits (6:5)

Reserved in VGA.

Bit 4 - Monitor Detection in VGA Mode.

DA15 monitor status (Pin 20) is sampled and can be read from this bit.

0 = Monochrom.

1 = Color.

Bits (3:0)

Reserved.

7.1.3 Input Status Register 1, Read Only Port = 3?AH

BIT	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2:1	Reserved
0	Display Enable

Bits (7:6)
Reserved.

Bits (5:4) - Color Plane Diagnostics.

These bits return two of the eight video outputs VID7 through VID0, as selected by Color Plane Enable Register Bits 5 and 4. See section 7.5.5.

Bit 3 - Vertical Retrace Status.

0 = Vertical frame is displayed.

1 = Vertical retrace is active.

Bits (2:1)
Reserved.

Bit 0 - Display Enable Status.

0 = CRT screen display in process.

1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.1.4 Feature Control Register, Read Port = 3CAH, Write Port = 3?AH

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits (7:4)
Reserved

Bit 3 - Vertical Sync Control.

0 = VSYNC output enabled.

1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

Bits (2:0)
Reserved

7.2 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4H	-----	Sequencer Index
3C5H	00	Reset
3C5H	01	Clocking Mode
3C5H	02	Map Mask
3C5H	03	Character Map Select
3C5H	04	Memory Mode

NOTE
Reserved bits should be set to zero.

7.2.1 Sequencer Index Register, Read/Write Port = 3C4H

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/ Index Bits

Bits (7:5)
Reserved.

Bits (4:0) - Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer Register to be accessed. Sequencer extension registers are also indexed by this register.

7.2.2 Reset Register, Read/Write Port = 3C5H, Index = 00H

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits (7:2)
Reserved.

Bit 1 - Synchronous Reset. ☆

0 = Sequencer is cleared and halted synchronously.

1 = Operational mode (Bit 0 = 1).

Bit 0 - Asynchronous Reset. ☆

0 = Sequencer is cleared and halted asynchronously.

1 = Operational mode (Bit 1 = 1).

☆ Both bits 1 and 0 must be set to 1 for Operational mode.

7.2.3 Clocking Mode Register, Read/Write Port = 3C5H, Index = 01H

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits (7:6)
Reserved.

Bit 5 - Screen Off.

0 = Normal screen operation.

1 = Screen is turned off but SYNC signals remain active. This bit may be used to provide maximum display memory bandwidth for quick full screen updates.

Bit 4 - Video Serial Shift Register Loading.

0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.

1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3 - Dot Clock Selection.

0 = Normal dot clock selected by VCLK input frequency.

1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2 - Shift Load. Effective Only If Bit 4=0.

0 = Video serializers are loaded every character clock.

1 = Video serializers are loaded every other character clock.

Bit 1
Reserved.

Bit 0 - 8/9 Dot Clock.

Commands Sequencer to generate an eight or nine dot wide character clock.

0 = Nine dot wide character clock.

1 = Eight dot wide character clock.

7.2.4 Map Mask Register, Read/Write Port = 3C5H, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits (7:4)

Reserved.

Bits (3:0) - Enables Writing to Memory Maps 3 Through 0, Respectively.

0 = Writing to Maps (3-0) disallowed.

1 = Maps (3-0) accessible.

7.2.5 Character Map Select Register, Read/Write Port = 3C5H, Index = 03H

BIT	FUNCTION
7:6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4, Bit 1 = 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. A 0 selects Character Map B. A "1" selects Character Map A. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and Bit 4 of the attribute code.

Bits (7:6)

Reserved.

Bit 5 - Character Map A MSB Select.

The Most Significant Bit (MSB) of Character Map A along with Bits 3 and 2, select the location of Character Map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4 - Character Map B MSB Select.

The MSB of Character Map B along with Bits 1 and 0, select the location of Character Map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bits (3:2) - Character Map Select A.

Refer to Bit 5 table.

Bits (1:0) - Character Map Select B.

Refer to Bit 4 table.

7.2.6 Memory Mode Register, Read/Write Port = 3C5H, Index = 04H

BIT	FUNCTION
7:4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits (7:4)

Reserved.

Bit 3 - Chains Four Maps.

0 = Processor sequentially accesses data using Map Mask Register.

1 = Directs the two lower order video Memory Address pins (MA1,MA0) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 - Odd/Even Map Selection.

0 = Even processor addresses to access Maps 0 and 2. Odd processor addresses to access Maps 1 and 3.

1 = Sequential processor access as defined by Map Mask Register.

Bit 1 - Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/EGA modes.

Bit 0

Reserved.

PORT	INDEX	VGA REGISTER NAME	*6845 REGISTER NAME
3?4	---	CRT Controller Address Register	CRTC Address Register
3?5	00	Horizontal Total	HorizontalTotal
3?5	01	Horizontal Display Enable End	Horizontal Display
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Display
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line	Maximum Scan Line Address
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Address High
3?5	0D	Start Address Low	Start Address Low
3?5	0E	Cursor Location High	Cursor Location High
3?5	0F	Cursor Location Low	Cursor Location Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

TABLE 7-4. CRT CONTROLLER REGISTERS

7.3 CRT CONTROLLER REGISTERS

7.3.1 CRT Address Register, Read/Write Port = 3?4H

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bits (7:5)

Reserved.

Bits (4:0) - Index Register Bits.

CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed in hexidecimal.

7.3.2 Horizontal Total Register, Read/Write Port = 3?5H, Index = 00H

BIT	FUNCTION
7:0	Horizontal Total Period

Bits (7:0) - Count Plus Retrace Less Five.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.3.3 Horizontal Display Enable End Register, Read/Write Port = 3?5H, Index 01H

BIT	FUNCTION
7:0	Displayed Characters per Scan Line

Bits (7:0) - Number Of Dislay Characters Less One.

This register contains the total number of displayed characters less one. This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.4 Start Horizontal Blanking Register, Read/Write Port = 3?5H, Index = 02H

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the value written in this register. This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.5 End Horizontal Blanking, Read/Write Port = 3?5H, Index = 03H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

Bit 7

Reserved

Bits (6:5) - Display Enable Signal Skew Control.

These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

00 = 0, Character Clock Skews

01 = 1, Character Clock Skews

10 = 2, Character Clock Skews

11 = 3, Character Clock Skews

Bits (4:0) - End Horizontal Blanking.

These five bits, along with bit 7 of the End Horizontal Retrace Register (Index 05H), determine when horizontal blanking is to end. Bits 4:0 are the least significant bits, bit 7 is the most significant bit.

When the least significant six bits of the Horizontal Character Counter matches these six bits, the horizontal blanking ends.

7.3.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5H, Index = 04H

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits (7:0) - Start Horizontal Retrace Character Count.

The character count at which the horizontal retrace output is to become active is programmed in this register as a hexidecimal value. This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

7.3.7 End Horizontal Retrace Register, Read/Write Port = 3?5H, Index = 05H

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	End Horizontal Blank Bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

Bit 7 - End Horizontal Blank Bit 6.

This is the sixth bit (Bit 5) of the End Horizontal Blanking Value programmed in bits 4:0 of the End Horizontal Blanking Register at Port 3?5H, Index 03H.

Bits (6:5) - Horizontal Retrace Delay.

These bits define the horizontal retrace signal delay.

00 = 0, Character Clock Delay

01 = 1, Character Clock Delay

10 = 2, Character Clock Delays

11 = 3, Character Clock Delays

Bits (4:0) - End Horizontal Retrace.

The least significant five bits are programmed in this register. When the least significant bits of the Horizontal Character Counter match these five bits, the Horizontal Retrace signal is turned off.

7.3.8 Vertical Total Register, Read/Write Port = 3?5H, Index = 06H

This register is locked if register PR3(0) = 1, or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Raster Scan Line Total Less 2

Bits (7:0) - Raster Scan Line Total Less 2.

This register contains the least significant eight bits of an eleven bit count of raster scan lines for a display frame. The programmed value includes the total number of vertical scan lines, minus two. Time for vertical retrace and vertical sync are also included. Bit 10 of this count is in register PR18 at Port 3?5H, Index 3EH, Bit 0. Bits 9 and 8 of this count are loaded into the Vertical Overflow Register at Port 3?5H, Index 07H, Bit 5 and Bit 0, respectively.

In 6845 mode, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09H Bits 4 through 0).

7.3.9 Overflow Vertical Register, Read/Write Port = 3?5H, Index = 07H

BIT	FUNCTION
7	Start Vertical Retrace Bit 9
6	End Vertical Display Enable Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Start Vertical Retrace Bit 8
1	End Vertical Display Enable Bit 8
0	Vertical Total Bit 8

③ Bit 7

Start Vertical Retrace - Bit 9.
Bit 8 is in bit 2 of this register, bits 7:0 are at Index 10H.

② Bit 6

End Vertical Display Enable - Bit 9.
Bit 8 is in bit 1 of this register, bits 7:0 are at Index 12H.

③ Bit 5

Vertical Total - Bit 9.
Bit 8 is in bit 0 of this register, bits 7:0 are at Index 06H.

Bit 4

Line Compare - Bit 8 (Index = 18H).

③ Bit 3

Start Vertical Blank - Bit 8 (Index =15H).

③ Bit 2

Start Vertical Retrace - Bit 8 (Index = 10H).

② Bit 1

End Vertical Display Enable - Bit 8 (Index 12H).

② Bit 0

Vertical Total - Bit 8 (Index = 06H).

NOTES

① This register is locked if Register PR3(5) = 1 OR the End Vertical Retrace Register Bit 7 = 1.

② This register is locked if Register PR3(1) = 0 AND the End Vertical Retrace Register Bit 7 = 1.

③ This register is locked if Register PR3(0) = 1 OR the End Vertical Retrace Register Bit 7 = 1.

7.3.10 Preset Row Scan Register, Read/Write Port = 3?5H, Index = 08H

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits (6:5) - Byte Panning Control.

These bits allow up to three bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bits (4:0) - Preset Row Scan Count.

These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When the maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.3.11 Maximum Scan Line Register, Read/Write Port = 3?5H, Index = 09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

In 6845 mode, Bits 7 through 5 are reserved,

Bit 7 - 200 to 400 Line Conversion.

0 = Normal operation.

1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines. Each line is double scanned.

Bit 6 - Line Compare.

This is Bit 9 of the Line Compare Register at Port 3?5H, Index 18H.

Bit 5 - Start Vertical Blank.

This is Bit 9 of the Start Vertical Blank Register at Port 3?5H, Index 15H. The Vertical Blank Register is locked if register PR3(0) = 1.

Bits (4:0) - Maximum Scan Line.

These bits are the maximum number of scanned lines for each row of characters. The value programmed is one less than the maximum number of scanned rows per character.

In 6845 mode, the value programmed is one less than the maximum scan line count for non-interlace mode. Interlaced mode is not supported.

7.3.12 Cursor Start Register, Read/Write Port = 3?5H, Index = 0AH

BIT	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bits (7:6)

Reserved.

Bit 5 - Cursor Control.

0 = Cursor on.

1 = Cursor off.

Bits (4:0) - Cursor Start Scan Line.

These bits specify the value of the row scan counter within the cursor's starting character box. These bits are programmed with one less than the value of the character row. If these bits are programmed with a value greater than the Cursor End Register at Port 3?5H, Index 0BH, no cursor is generated.

For 6845 modes, Bits 7 and 6 are reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value.

7.3.13 Cursor End Register, Read/Write Port = 3?5H, Index = 0BH

BIT	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

In 6845 mode, Bits 7 through 5 are reserved.

Bit 7

Reserved.

Bits (6:5) - Cursor Skew Bits.

Moves the displayed cursor to the right by the skew value in character clocks, e.g., one character clock skew moves the cursor right by one position on the screen.

BIT 6	BIT 5	SKEW
0	0	0 Character Clocks
0	1	1 Character Clocks
1	0	2 Character Clocks
1	1	3 Character Clocks

Bits (4:0) - Cursor End Scanline.

These bits specify the value of the last row scan counter within the character box in which the cursor is active. If this value is less than the cursor start value, no cursor is displayed.

In 6845 mode Bits 4 through 0 contain the row value of the cursor end.

NOTE

There are three types of cursors generated, depending upon the mode, i.e, EGA, VGA or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.3.14 Start Address High Register, Read/Write Port = 3?5H, Index = 0CH

BIT	FUNCTION
7:0	Start Address High Byte

Bits (7:0) - Display Screen Start Address Upper Byte Bits.

These are the high order eight bits of the 16-bit video memory address, used for screen refresh. The low order 8-bit register is at Port 3?5H Index 0DH. Register PR3 Bits 4 and 3 extend this video memory start register to 18 bits.

In 6845 mode, Bits 7 and 6 are forced to 0 regardless of this register's contents. The lower order eight bits are at Port 3?5H Index 0DH.

7.3.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7:0	Start Address Low Byte

Bits (7:0) - Start Address Low Byte.

These are the low order eight bits of the 16-bit video memory address in VGA or 6845 modes.

7.3.16 Cursor Location High Register, Read/Write Port = 3?5H, Index = 0EH

BIT	FUNCTION
7:0	Cursor Location High Byte

Bits (7:0) - Cursor Address Upper Byte Bits.

In VGA mode, these are the eight high order bits of the 16-bit cursor location. For the low order eight bits, see the Cursor Location Low Register at Port 3?5H, Index 0FH. Register PR3 Bits 4 and 3 extend the cursor location High Register to 18 bits.

In 6845 mode, Bits 7 and 6 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

7.3.17 Cursor Location Low Register, Read/Write Port = 3?5H, Index = 0FH

BIT	FUNCTION
7:0	Cursor Location Low Byte

Bits (7:0) - Cursor Address Low Byte Bits.

These are the low order eight bits of the 16-bit video memory address in VGA or 6845 mode.

7.3.18 Vertical Retrace Start Register, Read/Write Port = 3?5H, Index = 10H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Vertical Retrace Start (Lower eight bits)

Bits (7:0) - Vertical Retrace Start Pulse Lower Eight Bits.

In VGA mode, these are the lower eight bits of the 11-bit Vertical Retrace Start Register. Bit 10 is located in 3?5H, Index 3EH, Bit 2. Bits 9 and 8 are located in the Overflow Register at Port 3?5H, Index 07H.

In 6845 compatible mode, Bits 7 and 6 are reserved and bits 5 through 0 are the high order six bits. Bits 5 through 0 are shown as the light pen read back value. The lower order eight bits of the Light Pen Read Back Register are at the Index 11H.

In EGA compatible mode this register shows the high order eight bits as the light pen value.

7.3.19 Vertical Retrace End Register, Read/Write Port = 3?5H, Index = 11H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

Bit 7 - CRTC Registers Write Protect.

0 = Enables writing to CRT index registers 00H-07H.

1 = Write protects CRT Controller index registers in the range of index 00H-07H. Line Compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6 - DRAM Refresh/Horizontal Scan Line.

This bit selects DRAM refresh cycles per horizontal scan line.

0 = Generates three refresh cycles for each horizontal scan line for normal VGA operation.

1 = Generates five DRAM refresh cycles per horizontal scan line.

Bit 5 - Enable Vertical Retrace Interrupt.

0 = Enable vertical retrace interrupt.

1 = Disable vertical retrace interrupt.

Bit 4 - Clear Vertical Retrace Interrupt.

0 = Clears vertical retrace interrupt by resetting (writing a 0 to) an internal flip flop.

1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bits (3:0) - Vertical Retrace End.

These bits specify the scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The four-bit result is written in the Vertical Retrace End Register.

In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.3.20 Vertical Display Enable End Register, Read/Write Port = 3?5H, Index = 12H

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bits (7:0) - Vertical Display Enable End Lower Eight Bits.

These bits define where the active display frame ends and are the lower eight bits of an 11-bit register. The programmed count is in scan lines minus one. Bit 10 is in Port 3?5H, Index 3EH, Bit 10. Bits 9 and 8 are in the Overflow Register at Port 3?5H, Index 07H, Bits 6 and 1, respectively.

7.3.21 Offset Register, Read/Write Port = 3?5H, Index = 13H

BIT	FUNCTION
7:0	Logical Line Screen Width

Bits (7:0) - Logical Line Screen Width.

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

7.3.22 Underline Location Register, Read/Write Port = 3?5H, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved.

Bit 6 - Doubleword Mode.

0 = Display memory addressed for byte or word access.

1 = Display memory addressed for double word access.

Bit 5 - Count by Four for Double Word Access.

0 = Memory address counter clocked for byte or word access.

1 = Memory address counter is clocked at the character clock rate divided by four.

Bits (4:0) - Underline Location.

These bits specify the row scan counter value within a character matrix where underline is to be displayed. Load a value one less than the desired scan line number.

7.3.23 Start Vertical Blank Register, Read/Write Port = 3?5H, Index =15H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Start Vertical Blank (Lower eight bits)

Bits (7:0) - Start Vertical Blank Lower Eight Bits.

These are the lower eight bits of the 11-bit Start Vertical Blank Register. Bit 10 is in register PR18 at Port 3?5H, Index 3EH, Bit 3. Bit 9 is in the Maximum Scan Line Register at Port 3?5H, Index 09H. Bit 8 is in the Overflow Register at Port 3?5H, Index 07H.

The eleventh bit value is reduced by one from the desired scan line count where the vertical blanking signal starts.

7.3.24 End Vertical Blank Register, Read/Write Port = 3?5H, Index = 16H

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	End Vertical Blank

Bits (7:0) - Vertical Blank Inactive Count.

End Vertical Blank is an eight-bit value calculated as follows:

Eight-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

7.3.25 CRT Mode Control Register, Read/Write Port = 3?5H, Index = 17H

This register is locked if register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7 - Hardware Reset.

0 = Horizontal and vertical retrace outputs inactive.

1 = Horizontal and vertical retrace outputs enabled.

Bit 6 - Word or Byte Mode.

0 = Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB. See the following Table.

1 = Byte address mode.

CRT14H Bit 6	CRT17H Bit 6	ADDRESS Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 - Address Wrap.

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.

1 = Select MA15 for odd/even mode when 256 Kbytes of video memory is used on the system board.

Bit 4

Reserved.

Bit 3 - Count by 2.

0 = Character clock increments memory address counter.

1 = Character clock divided by two increments the address counter.

Bit 2 - Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate

1 = Selects horizontal retrace clock rate divided by two.

Bit 1 - Select Row Scan Counter.

0 = Selects row scan counter Bit 1 as output at MA14 address pin.

1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0 - 6845 CRT Controller Compatibility Mode Support for CGA Operation.

0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.

1 = Enable memory address pin 13 to be output at MA13 address pin.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLE WORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See Bit 5, defining address wrap. This table is only applicable when register PR1 Bits 7 and 6 equal zero, or PR16 Bit 1 equals one.

The CRT Underline Location Register (Index = 14H) Bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) Bit 6 controls addressing.

TABLE 7-5. WORD OR BYTE MODE

7.3.26 Line Compare Register, Read/Write Port = 3?5H, Index = 18H

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bits (7:0) - Line Compare Lower Eight Bits.

These are the lower eight bits of the ten-bit Scan Line Compare Register. Bit 9 is in the Maximum Scan Line Register at Port 3?5H, Index 09H. Bit 8 is in the Overflow Register at Port 3?5H, Index 07H. When the vertical counter reaches the value programmed in the Scan Line Compare Register, the internal start of the line counter is cleared.

7.4 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE
Reserved bits should be set to zero.

7.4.1 Graphics Index Register, Read/Write Port = 3CEH

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits (7:4)
Reserved.

Bits (3:0) - Graphics Controller Register Index Pointer Bits.

NOTE
Some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.4.2 Set/Reset Register, Read/Write Port = 3CFH, index = 00H

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits (7:4)
Reserved.

Bits (3:0) - Set/Reset Map.

When the CPU executes display memory write, with Write Mode 0* selected and the Enable Set/Reset Register at Port 3CFH, Index 01H activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight-bit fill operation.

0 = Reset.

1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE*

The selection of Write Mode 0 is determined by the Graphics Mode Register (Index = 05H) Bit 1 and Bit 0.

7.4.3 Enable Set/Reset Register, Read/Write Port = 3CFH, Index = 01H

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, the corresponding bit (3:0) set to 0, disables the Set/Reset Register (Index = 00H) Memory Map access and the map is written with the rotated 8-bit data from the system microprocessor, as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, the corresponding bit (3:0) enables Memory Map access defined by the Set/Reset Register (Index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.4.4 Color Compare Register, Read/Write Port = 3CFH, Index = 02H

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Color Compare.

The Color Compare bits contain the value to which all eight bits of the corresponding memory map are compared. This comparison also occurs across all four maps and a 1 is returned for the map positions when the bits of all four maps equal the Color Compare Register. If a system read is done with Bit 3 = 0 for the Graphics Mode Register at Port 3CFH, Index 05H, data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.4.5 Data Rotate Register, Read/Write Port = 3CFH, Index = 03H

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits (7:5)

Reserved.

Bits (4:3) - Function Select.

This is the Function Select for any of the write mode operations defined in the Graphics Mode Register at Port 3CFH, Index 05H as defined below.

00 = Video memory data unmodified.

01 = Video memory data ANDed with system data in the latches.

10 = Video memory data ORed with system data in the latches.

11 = Video memory data XORed with system data in the latches.

NOTE

"Data" refers to CPU data that has gone through data rotation. The latches contain the data from the last memory read operation.

Bits (2:0) - Rotate Count.

These bits specify the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register at Port 3CFH, Index 05H.

7.4.6 Read Map Select Register, Read/Write Port = 3CFH, Index = 04H

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits (7:2)

Reserved.

Bits (1:0) - Map Select.

These bits select the memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value is defined below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.4.7 Graphics Mode Register, Read/Write Port = 3CFH, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6 - 256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four-bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID7, VID6) are determined by Bits 3 and 2 of the Color Select Register located at Port 3C1H/3C0H, Index 14H within the Attribute Controller.

1 = Load Video Shift Registers to support 256-color mode.

Bit 5 - Shift Register.

Shift Register Load controls the way in which memory data is formatted in the four Video Shift Registers. MSB is shifted out in all cases.

0 = Map 3 through Map 0 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 - Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the Sequencer Memory Mode Register at Port 3CFH, Index 04H. Even system addresses access Maps 2 or 0 and odd system addresses access Maps 3 or 1.

Bit 3 - Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register at Port 3CFH, Index 04H. This setting has no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

BIT 1	BIT 0	WRITE MODE
0	0	**Write Mode 0.** If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is rotated right by the number of bits defined in the Data Rotate Register (with the old LSB now the new MSB).
0	1	**Write Mode 1.** This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2.** Memory maps (3:0) are filled with the eight-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3.** Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an eight-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

TABLE 7-6. WRITE MODES

Bit 2

Reserved.

Bits (1:0) - Write Mode.

Table 7-6 defines the four write modes.

7.4.8 Miscellaneous Register, Read/Write Port = 3CFH, Index = 06H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits (7:4)

Reserved.

Bits (3:2) - Memory Map 1, 0.

Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1 - Odd/Even Mode.

0 = CPU address Bit A0 is the memory address Bit MA0.

1 = CPU address Bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects Map 2 or 0, while A0 = 1 selects Map 3 or 1.

Bit 0 - Graphics/Alphanumeric Mode.

This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register at Port 3C1H/3C0H, Index 10H.

0 = Alphanumeric mode selects.

1 = Graphics mode selected.

7.4.9 Color Don't Care Register, Read/Write Port = 3CFH, Index = 07H

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Memory Map Color Compare Operation.

0 = Disable color compare operation.

1 = Enable color compare operation.

7.4.10 Bit Mask Register, Read/Write Port = 3CFH, Index = 08H

BIT	FUNCTION
7:0	Bit Mask

Bits (7:0) - Bit Mask.

Bit Mask operation applies simultaneously to all four maps. In Write Modes 2 and 0, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.

1 = Bit position value is unmasked and can be changed in the corresponding map.

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7.5 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES

1. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the Address and Data Registers. Reading the Input Status Register 1 (Port 3?AH) clears the flip-flop and selects the Address Register, which is read at address 3C1H and written at address 3C0H. Once the Address Register has been loaded with an index, the next write operation to 3C0H loads the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0H but does not toggle for reads from address 3C1H.
2. Attribute Register data is written at 3C0H and register data is read from address 3C1H.
3. Reserved bits should be set to zero.

7.5.1 Attribute Index Register, Read/Write Port = 3C0H

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits (7:6)
Reserved.

Bit 5 - Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to Color Palette Registers Port 3C0H, Index 00 - 0FH.

1 = Enable internal color palette and normal video translation.

Bits (4:0) - Attribute Controller Index Register Address Bits.

7.5.2 Palette Registers, Read Port = 3C1H, Write Port = 3C0H, Index 00-0FH

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:6)
Reserved.

Bits (5:0) - Palette Pixel Colors.

Bits 5 through 0 control VID5 through VID0 respectfully.

They are defined as follows:

0 = Current pixel color deselected.

1 = Enables the corresponding pixel color.

7.5.3 Attribute Mode Control Register, Read Port = 3C1H, Write Port = 3C0H, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7 - VID5, VID4 Select.

0 = VID5 and VID4 palette register outputs are selected.

1 = Color Select Register Port 3C1H/3C0H, Index 14H, Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 - Pixel Width.

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.

1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5 - PEL Panning Compatibility.

Line Compare in the CRT Controller.

0 = A Line compare will have no effect on the PEL Panning Register.

1 = Allows a successful line compare to disable the PEL Panning Register and Bits 6 and 5 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3 - Background Intensity/Blink Selection.

0 = Selects background intensity from the MSB of the attribute byte.

1 = Selects blink attribute.

Bit 2 - Enable Line Graphics Character Code.

This bit should be set to zero for character fonts that do not utilize line graphics character codes.

0 = Forces the ninth dot to be the same color as the background in line graphics character codes.

1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 - Mono/Color Emulation.

0 = Color display attributes.

1 = MDA attributes.

Bit 0 - Graphics/Alphanumeric Mode Enable.

0 = Alphanumeric mode.

1 = Graphics mode.

7.5.4 Overscan Color Register, Read Port = 3C1H, Write Port = 3C0H, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:0) - Overscan/Border Color.

These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

7.5.5 Color Plane Enable Register, Read Port = 3C1H, Write Port = 3C0H, Index = 12H

BIT	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bits (7:6)

Reserved.

Bits (5:4) - Video Status Control.

These bits select two out of eight color outputs which can be read by the Input Status Register 1 at Port 3?AH, Bits 5 and 4.

COLOR PLANE		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bits (3:0) - Color Plane Enable.

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.

1 = Enables the respective display memory color plane.

7.5.6 Horizontal Pel Panning Register, Read Port = 3C1H, Write Port = 3C0H, Index = 13H

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits (7:4)

Reserved.

Bits (3:0) - Horizontal Pixel Panning.

Horizontal Pixel Panning is available in text or graphics modes. These bits select pixel shift to the left. For nine dots/character modes, up to eight pixels can be shifted. Likewise, for eight dots/character up to seven pixels can be shifted. For 256 color, up to three position pixel shifts can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.5.7 Color Select Register, Read Port = 3C1H, Write Port = 3COH, Index = 14H

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bits (7:4)

Reserved.

Bits (3:2) - Color Value MSB.

These are the two most significant bits of the eight-digit color value for the video DAC. They are normally used in all modes except 256 color graphics.

Bit 3 = Set color bit VID7.

Bit 2 = Set color bit VID6.

Bits (1:0) - Substituted Color Value Bits.

These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight-bit color value. They are selected by the Attribute Controller Mode Control Register at Port 3C0H, Index 10H.

7.6 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting register PR2(7) = 1.
3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register at Port 3CCH/3C2H and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes.

7.6.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7 - Select Display Memory Page Address In Hercules Mode.

Reserved in MDA mode.

In Hercules Graphics mode, this bit selects the Display Memory Page if Bit 1 of this register is 1 and Bit 0 in Port 3BFH is 0.

0 = Display memory page address starts at B000:0H.

1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5 - Enable Blink.

0 = Disable Blinking.

1 = Enable Blinking.

Bit 4

Reserved.

Bit 3 - Video Enable.

0 = Video Disabled.

1 = Video Activated.

Bit 2

Reserved.

Bit 1 - Port 3BFH Enabled.

0 = Prevents setting of Port 3BFH Bits 1:0, thereby forcing the alpha mode operation.

1 = Allows the Port 3BFH Bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0 - High Resolution Mode.

Should be set to "1".

0 = High resolution disabled.

1 = High resolution is enabled.

7.6.2 Hercules Registers

The Hercules Mode Register is a two-bit write only register located at I/O port address 3BFH. It affects the device operation only in the 6845 mode. The Enable Mode Register located at address 3B8H overrides the write port 3BFH functions defined by its Bits 1 and 0.

7.6.3 Enable Mode Register Port 3B8H

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7 - Select Display Memory Page Address In Graphics Mode.

0 = Display memory page address starts at B000:0H.

1 = Display memory page address starts at B800:0H.

Bits (6:2, 0)

Not applicable in Hercules Mode.

Bit 1 - Port 3BFH, Bit 0 Override.

0 = Prevents setting of Port 3BFH, Bit 0, thereby forcing the Alpha Mode operation.

1 = Allows the Port 3BFH, Bit 0 to switch for the Alpha or Graphics Mode selection.

7.6.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1 - Upper Memory Page Address.

In the graphics mode, Bit 7 of the Enable Mode Control Register at Port 3B8H selects the displayed memory page address. When that bit is reset, Bit 1 of this register prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.

0 = Upper memory page is mapped out.

1 = Upper memory page is accessible.

Bit 0 - Enable Graphics.

Bit 1 of Enable Mode Register at Port 3B8H may prevent setting this bit, thereby selecting Alpha Mode display.

0 = Alpha mode display.

1 = Graphics modes may be displayed.

7.6.5 Color CGA Operation Register, Write Only Port = 3D8H

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bits (7:6)
Reserved.

Bit 5 - Enable Blink Function.

0 = Disables blinking function.

1 = For normal operation, set this bit to allow blinking.

Bit 4 - B/W Graphics Mode Enable.

0 = Deselect 640 by 200 B/W graphics mode.

1 = Enable 640 by 200 B/W graphics mode.

Bit 3 - Activate Video Signal.

0 = Deactivates video signal. This is done during mode changes.

1 = B/W mode enabled.

Bit 2 - B/W or Color Display Mode.

0 = Color Mode Selected.

1 = B/W Mode Selected.

Bit 1 - Text or Graphics Mode Selection.

0 = Alpha mode enabled.

1 = Graphics mode (320 by 200) activated.

Bit 0 - (40 by 25) or (80 by 25) Text Mode Selection.

0 = 40 by 25 alpha mode enabled.

1 = 80 by 25 alpha mode activated.

7.6.6 CGA Color Select Register, Write Only Port = 3D9H

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bits (7:6)
Reserved.

Bit 5 - 320 by 200 Color Set Select for the CGA (two bits per pixel).

0 = Background, green, red, brown colors.

1 = Background, cyan, magenta, white colors.

Bit 4 - Alternate Color Set Enable.

0 = Background color in alpha mode.

1 = Enable alternate color set in graphics mode.

Bit 3 - Border Intensity.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.

1 = Selects intensified border color.

320 by 200 Graphics Mode.

1 = Selects intensified background and border color (C0 - C1).

640 by 200 Graphics Mode.

1 = Selects red foreground color.

Bit 2 - Red Border/Background.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

1 = Selects red border color.

320 by 200 Graphics Mode.

1 = Selects red background and border color (C0 - C1).

640 by 200 Graphics Mode.

1 = Selects red foreground color.

Bit 1 - Green Border/Background.

Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

1 = Selects green border color.

320 by 200 Graphics Mode.

1 = Selects green background and border color (C0 - C1).

640 by 200 Graphics Mode.

1 = Selects green foreground color.

Bit 0 - Blue Border/Background.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

1 = Selects blue border color.

320 by 200 Graphics Mode.

1 = Select blue background and border color (C0 - C1).

640 by 200 Graphics Mode.

1 = Selects blue foreground color.

7.6.7 CRT Status Register, MDA Operation, Read Only Port = 3BAH

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7 - Vertical Retrace.

0 = Indicates that the raster is in vertical retrace mode.

1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bits (6:4)

Reserved.

Bit 3 - B/W Video Status.

0 = B/W Video disabled.

1 = B/W Video enabled.

Bits (2:1)

Reserved.

Bit 0 - Display Enable.

0 = Display Enable is active.

1 = Indicates that the screen border or blanking is active; Display Enable is inactive.

7.6.8 CRT Status Register, CGA Operation, Read Only Port = 3DAH

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits (7:4)

Reserved.

Bit 3 - Vertical Retrace.

0 = Indicates that vertical retrace is inactive.

1 = Indicates that the raster is in vertical retrace mode.

Bit 2 - Light Pen Switch Status.

0 = Light pen switch closed.

1 = Light pen switch open

Bit 1 - Light Pen Latch.

0 = Light pen latch cleared.

1 = Light pen latch set.

Bit 0 - Display Enable.

0 = Display Enable is active.

1 = Indicates that the screen border or blanking is active; Display Enable is inactive.

7.6.9 AT&T/M24 Register, Write Only Port = 3DEH

This is a write only, eight-bit register located at address 3DEH. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting Bit 7 in register PR2.

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5:4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bits (7, 5, 4, 1)

Reserved.

Bit 6 - White/Blue Underline.

Defines underline attribute according to the MDA display requirements.

0 = Underline attribute selects blue foreground incolor text modes.

1 = Underline attribute selects white underlined foreground.

Bit 3 - Page Select.

Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.

0 = Display memory address starts at B800:0H (16 Kbyte length).

1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2 - Character Set Select.

Selects between two character font planes.

0 = Standard character font from plane 2.

1 = Alternate character font from plane 3.

Bit 0 - M24 or Non-IBM Graphics Mode, 400-line mode.

A 400-line monitor is required for this mode.

0 = 200-line graphics mode active, using paired lines.

1 = AT&T mode enabled for 400-line graphics.

7.7 WD90C31 PR REGISTERS

The WD90C31 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C31 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES

1. The designation 3?5H means that the register is mapped into either 3B5H in monochrome mode or 3D5H in color modes.
2. PR Register notation - XXX.YY where XXX is the data port address and YY is the register index, e.g., 3CF.0F implies 0F → 3CEH (Select Index register) followed by (Data byte) → 3CFH (Data Port). Registers PR0 through PR4 and PR11 through PR1A are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101. A register remains unlocked until another value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17, load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 Bit 1 to "1" does not read protect registers PR10 through PR17. PR21-PR23 and PR30-PR35 are R/W protected by PR20. PR20 must be loaded with 48H to make it possible to read or write to PR21-PR23 and PR30-PR35. All PR registers are set to "0" at power on reset except where noted.

7.7.1 Address Offset Registers PROA And PROB

PROA - Address Offset Register A, Read/Write Port = 3CFH, Index = 09H

BIT	FUNCTION
7:0	Primary Address Offset Bits

PROB - Address Offset Register B, Read/Write Port = 3CFH, Index = 0AH

BIT	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C31 can control up to 1 Mbyte of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA reach the memory beyond this range, the WD90C31 has two CPU address offset registers, PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PROA (Bits 6:0) or PROB (Bits 6:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture. PROA and PROB will then provide four Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a four Kbyte segment to another four Kbyte segment of the display memory.)

PROA and PROB are all set to zero at power-on-reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 0.**

  When PR1-3 = 0, PR0A is always selected as the CPU address offset register.

  When PR1-3 = 1 and the display memory is mapped into A000 - BFFFF (128 Kbytes), PR0A offset CPU address range is B0000 -

BFFFF, the PR0B offset CPU address range is A0000 - AFFFF. (If CPU address bit A16 = 1, select PR0A. Otherwise PR0B is selected.)

When PR1-3 = 1 and the display memory is mapped into A0000 - AFFFF (64 Kbytes) or B0000 - B7FFF or B800 - BFFFF (32 Kbytes), then PR0B offset CPU address range is A0000 - A7FFF or B0000 - B7FFF. PR0A offset CPU address range is A8000 - AFFFF or B8000 - BFFFF. (If CPU address bit A15 = 1, select PR0A. Otherwise PR0B is selected.)

- **Sequencer Extension Register 3C5H, Index = 11H, Bit 7 = 1.**

  Both PR0A and PR0B are enabled. A CPU memory write selects PR0B as the offset register. Otherwise, PR0A is selected as the offset register.

7.7.2 PR1 - Memory Size, Read/Write Port = 3CFH, Index = 0BH

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate Address Offset Register PR0B
2	16-Bit System Interface
1	16-bit BIOS ROM
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1(1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits (7:6) - Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits, in conjunction with PR0A, PR0B, PR16(1), select the way memory is mapped into the CPU address space. IF PR16(1) is set to 1, the memory mapping will be set identical to the IBM VGA, regardless of PR1(7), PR1(6).

Tables 7-7 through 7-10 list the different settings on these two bits for different memory organizations.

PR1(7) = 0 PR1(6) = 0 256K TOTAL, IBM VGA MEMORY ORGANIZATION						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)	MA(1)
A(0)	CA(0)	A(14) or ③ XRN(5)	CA(15) or ④ CA(14)	A(14)	CA(12)	MA(0)

TABLE 7-7. IBM COMPATIBLE MEMORY ORGANIZATION

PR1(7) = 0 PR1(6) = 1 256K TOTAL, 64K/PLANE, WD90C31 MEMORY ORGANIZATION						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(16)	CA(14)	MA(0)

TABLE 7-8. WD90C31 MEMORY ORGANIZATION - 256 KBYTES

PR1(7) = 1 PR1(6) = 0 512K TOTAL, 128K/PLANE, WD90C31 MEMORY ORGANIZATION						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
PA ⑤	PA	PA	PA	PA	PA	MA(17)
A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(16)	CA(14)	MA(0)

TABLE 7-9. WD90C31 MEMORY ORGANIZATION - 512 KBYTES

PR1(7) = 1 PR1(6) = 1		1M TOTAL, 256K/PLANE, WD90C31 MEMORY ORGANIZATION				
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLE WORD WIDE		
CPU	CRT/BITBLT	CPU	CRT/BITBLT	CPU	CRT/BITBLT	
A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)	MA(17)
A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)	MA(13)
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)	MA(1)
A(0)	CA(0)	A(16) or ③ XRN(5)	CA(15)	A(18)	CA(16)	MA(0)

TABLE 7-10. WD90C31 MEMORY ORGANIZATION - 1 MBYTES

NOTES:

1. A(19:0) are WD90C31 internally modified system Addresses (CPU address + offset address).
2. CA(17:0) are either CRT Character Address Counter Bits or bitblit generated counter bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted Bit 5. XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. In IBM compatible memory mapping, 3C5.4, Bit 1 = 1 will select XRN(5) to replace CPU address bits. In other memory mapping schemes (PR1(7,6) ≠ 00, 3C5.4, Bit 1 = 1 and PR16_2 = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as MA(0) if CRTC Mode Register 17, Bit 5 = 1 in word addressing modes.
5. PA is the memory plane select bit when DRAM interface is set for 16 bits.
   PA = 0 selects Plane 1,0
   PA = 1 selects Plane 3, 2
6. MA(17-0) are divided into $\overline{RAS}$, $\overline{CAS}$ addresses as follows:

For 256K by 4 DRAM or 256K by 16 DRAM		MA(16) - MA (8) ⇒ MA(17), M(7) - MA(0) ⇒	$\overline{RAS}$(8) - $\overline{RAS}$(0) $\overline{CAS}$(8) - $\overline{CAS}$(0)
For 64K by 16 DRAM		MA(15) - MA(8) ⇒ MA(7) - MA(0) ⇒	$\overline{RAS}$(7) - $\overline{RAS}$(0) $\overline{CAS}$(7) - $\overline{CAS}$(0)
MA(17, 16)	= 00	Select 1st 64K bank	
	= 01	Select 2nd 64K bank	
	= 10	Select 3rd 64K bank	
	= 11	Select 4th 64K bank	

Bits (5:4) - PRI(5,4) Memory Map Select.

0	0	IBM VGA mapping. CPU addresses are decoded from 0A0000H - 0BFFFFH from the lowest 1 Mbyte CPU address space (depending on 3CF.06 bits 2 and 3).
0	1	First 256 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X3FFFFH)
1	0	First 512 Kbyte in any 1 Mbyte CPU addressing space (X00000H - X7FFFFH)
1	1	In any 1Mbyte CPU address space (X00000H - XFFFFFH)

NOTE

PR34(3C5.14) Bits 3-0 control which 1 Mbyte of CPU address space the WD90C31 maps. See section 7.7.27.

Bit 3 - Enable Alternate Address Offset Register PROB.

Bit 2 - Enable 16 bit system interface bus.

0 = System interface is 8 bits.

1 = System interface is 16 bits.

Bit 1 - 16-bit BIOS ROM.

0 = BIOS ROM access is 8 bits.

1 = BIOS ROM access is 16 bits.

A pull-down resistor on MD(10) sets this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write cycle only if the CNF(1) = 1.

Bit 0 - BIOS ROM Map Out.

0 = The BIOS ROM is available.

1 = The BIOS ROM is mapped out.

A pull-down resistor on MD(0) sets this bit to 1 at power-on-reset.

7.7.3 PR2-Video Select Register, Read/Write Port = 3CFH, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7 - Enable AT&T/M24 Register and Mode.

0 = Disable.

1 = Enable.

Bit 6 - 6845 Compatibility.

0 = VGA or EGA mode.

1 = Non-VGA (6845) mode.

Bit 5 - Character Map Select.

The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from Planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE

Setting PR15(2) = 1, i.e., selecting page mode addressing overrides plane selected table shown above.

Bits (4:3) - Character clock period control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132-character text mode only)
1	0	9 dots
1	1	6 dots if PR17(5) = 0 10 dots if PR17(5) = 1.

NOTE

The character clock period control functions have no effect in graphics modes (Graphics Mode always uses eight dots).

Bit 2 - Underline and character map select.

Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., programming 1 gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1 - Third Clock Select Line.

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) = 1. When CNF(3) = 0, it locks the internal video clock select multiplexer.

Bit 0 - Force VCLK.

This bit forces horizontal sync timing clock of the CRTC to VCLK.

Uses VCLK when Sequencer Register 1, Bit 3, is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.7.4 PR3 - CRT Lock Control Register, Read/Write Port = 3CFH, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7 - Lock VSYNC Polarity.

This bit locks VSYNC polarity as programmed at Port 3C2H, Bit 7.

Bit 6 - Lock HSYNC Polarity.

This bit lock HSYNC polarity as programmed at Port 3C2H, Bit 6.

Bit 5 - Lock Horizontal Timing.

This bit locks CRTC registers of Groups 4 and 0. It prevents applications software from unlocking Group 0 registers by setting 3?5.11 Bit 7 = 0.

Bit 4 - Bit 9 Control.

Bit 9 of CRT Controller Start Memory Adress High Register 3?5.0C and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(17).

Bit 3 - Bit 8 Control.

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(16).

Bit 2 - Cursor Control.

Cursor Start, Stop, Preset Row Scan and Maximum Scan Line Address registers value multiplied by two.

Bit 1 - Lock Prevention.

1 = Prevents attempts by applications software to lock registers of Group 1 by setting 3?5.11, Bit 7 = 1.

Bit 0 - Lock vertical timing.

1 = Locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by setting 3?5.11, Bit 7 = 0.

7.7.5 WD90C31 CRT Controller Register Locking

Register locking is controlled by four bits. They are PR3(5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register Bit 7 controlled by Index register 11). When 3?5.11 Bit 7 = 1, CRT controller registers (R0-7) are write-protected per VGA definition. For more information on the five groups and their locking schemes, refer to the following sections.

- **Group 0**

  These registers are locked if PR3(5) = 1 OR 3?5.11(7) = 1.

  3?5 index 00 - Horizontal Total Characters per scan

  3?5 index 01 - Horizontal Display Enable End

  3?5 index 02 - Start Horizontal Blanking

  3?5 index 03 - End Horizontal Blanking

  3?5 index 04 - Start Horizontal Retrace

  3?5 index 05 - End Horizontal Retrace

- **Group 1**

  These registers are locked if PR3(1) = 0 AND 3?5.11(7) = 1.

  3?5 index 07 (Bit 6) - Vertical Display Enable End Bit 9

  3?5 index 07 (Bit 1) - Vertical Display Enable End Bit 8

  3?5 index 0E (Bit 1) - Vertical Display Enable End Bit 10

- **Group 2**

  These registers are locked if PR3(0) = 1 OR 3?5.11(7) = 1.

  3?5 index 06 - Vertical Total

  3?5 index 07 (Bit 7) - Vertical Retrace Start Bit 9

  3?5 index 07 (Bit 5) - Vertical Total Bit 9

  3?5 index 07 (Bit 3) - Start Vertical Blank Bit 8

  3?5 index 07 (Bit 2) - Vertical Retrace Start Bit 8

  3?5 index 07 (Bit 0) - Vertical Total Bit 8

  3?5 index 09 (Bit 5) - Start Vertical Blank Bit 9

  3?5 index 3E (Bit 0) - Vertical Total Bit 10

  3?5 index 3E (Bit 2) - Vertical Retrace Start Bit 10

  3?5 index 3E (Bit 3) - Start Vertical Blank Bit 10

- **Group 3**

  These registers are locked if PR3(0) = 1.

  3?5 index 10 - Vertical Retrace Start

  3?5 index 11 [Bits(3:0)] - Vertical Retrace End

  3?5 index 15 - Start Vertical Blanking

  3?5 index 16 - End Vertical Blanking

- **Group 4**

  This register is locked if PR3(5) = 1.

  CRTC Mode Control Register 17 (Bit 2) - Selects divide-by-two vertical timing.

7.7.6 PR4 - Video Control Register, Read/Write Port = 3CFH, Index = 0EH

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs, as well as video data for the RAMDAC and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$/Display Enable
6	PCLK = VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256-color Shift Register Control

Bit 7 - $\overline{\text{BLANK}}$/Display Enable.

This bit controls the output signal $\overline{\text{BLANK}}$. Normally in the VGA mode, $\overline{\text{BLANK}}$ is used by the external video DAC to generate blanking.

1 = The $\overline{\text{BLANK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected and is determined by PR15(1).

Bit 6 - Select PCLK equal to VCLK.

0 = PCLK is either the inverted internal video dot clock or half the dot clock frequency, depending upon the video mode.

1 = PCLK is always the non-inverted VCLK input clock.

Bit 5 - Tristate Video Outputs.

1 = Video Outputs $\overline{\text{VID}}$(7:0), HSYNC, VSYNC, and $\overline{\text{BLANK}}$ are tristated.

Bit 4 - Tristate Memory Control Outputs.

1 = The memory address bus, MA(8:0), and all ten DRAM control signals are tristated.

Bit 3 - Override CGA Enable Video Bit.

Overrides the CGA Enable Video Bit 3 of mode register 3D8H, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2 - Lock Internal Palette and Overscan Registers.

1 = Internal palette and overscan registers are locked.

Bit 1 - EGA compatibility.

1 = EGA Compatible Mode. Reads are disabled to all registers which are write-only registers in the IBM EGA mode.

Also, registers at 3COH/3C1H change to write-only mode.

Reading PR5 through PR0 is disabled. In VGA mode [PR(4) Bit 1 = 0] 3C0H register is read/write while 3C1H register is read only, per the Attribute Controller Register's definitions.

Bit 0 - Extended Shift Register Control.

1 = Extended 256-color modes selected (IBM Mode 13 is not included).

7.7.7 PR5 - General Purpose Status Bits, Read/Write Port = 3CFH, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR4-PR0 Unlock
1	PR4-PR0 Unlock
0	PR4-PR0 Unlock

Bits 7-3 provides readable status for the Configuration Register Bits 8 through 4.

Bit 7 - CNF(7) Status.

This is a read only bit.

Bit 6 - CNF(6) Status.

This is a read only bit.

Bit 5 - CNF(5) Status.

This is a read only bit.

Bit 4 - CNF(4) Status.

This is a read only bit.

Bit 3 - CNF(8) Status.

This is a read only bit.

Bits (2:0) - PR4-PR0.

These are read/write bits and are cleared by reset. They provide lock and unlock capability for PR registers PR4 through PR0. The PR4 through PR0 registers are unlocked when "X5H" is written to PR5. They remain unlocked until any other value is written to PR5.

Setting PR(4) Bit 1 to 1, read protects registers PR5 through PR0.

PR5 2 1 0	PR4-PR0
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected
1 0 1	Write enabled

7.7.8 PR10 Unlock, PR1A-PR11 Read/Write Port = 3?5H, Index = 29H

PR10 is a read/write register and is cleared by reset. PR10 can be written to if it contains XXXXX101, and can only be read if it contains 1XXX0XXX. PR10 controls access to PR registers PR1A-PR10.

Bits 7 and 3 enable register read operation for PR1A - PR10. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR1A through PR11.

BIT	FUNCTION
7	PR1A-PR10 - Read Enable Bit 1
6:4	PR10(6:4) - Scratch Pad
3	PR1A-PR10 - Read Enable Bit 0
2:0	PR1A-PR11 - Write Enable

Bits 7, 3 - PR17-PR10 Read Enable.

BIT7	BIT3	PR17-PR10
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

Bits 6:4 - PR10 Scratch Pad.

PR10 6 5 4	PR10(6:4)
0 X X	Scratch pad
X 1 X	Scratch pad
X X 0	Scratch pad
1 0 1	Reserved for manufacturing test.

Bits 2:0 - PR11-PR1A Write Enable.

PR10 2 1 0	PR17-PR11
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected
1 0 1	Write enabled

7.7.9 PR11 EGA Switches, Read/Write Port = 3?5H, Index = 2AH

The EGA switch configuration details are stored in register PR11.

BIT	FUNCTION
7	EGASW4/General Purpose
6	EGASW3/General Purpose
5	EGASW2/General Purpose
4	EGASW1/General Purpose
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4) - EGA Configuration Switches SW4-SW1.

These read/write bits from corresponding memory data bus pins MD(15:12) are latched internally at power-on-reset with either pull-up or pull-down external resistors. Pulling-up MD(15:12) causes PR11(7:4) to be latched high. These bits can be read from Bit 4 of Port 3C2H if the EGA compatibility bit PR4(1) = 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows.

WRITE 3C2H Bit 3	Bit 2	READ 3C2H Bit 4
0	0	PR11(7) = EGA SW4
0	1	PR11(6) = EGA SW3
1	0	PR11(5) = EGA SW2
1	1	PR11(4) = EGA SW1

These bits may be used as general purpose scratch bits.

Bit 3 - Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

This is a read/write bit and is set to zero at power-on-reset.

Bit 2 - Lock Clock Select.

This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

This is a read/write bit and is set to zero at power-on-reset.

Bit 1 - Lock Graphics Controller/Sequencer Screen Control.

Setting this bit to 1 prevents modification of the following bits in the Graphics Controller as well as the Sequencer:

Graphics Controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by the graphics controller and sequencer bits are locked by setting PR11 Bit 1 to 1, they appear unlocked to the system processor during read operation.

This is a read/write bit and is set to zero at power-on-reset.

Bit 0 - Lock 8/9 Dots.

Setting this bit to 1 prevents modification of the Clocking Mode Sequencer Register 3C5.01, Bit 0.

1 = Eight and nine dot wide character timing is locked. Register 3C5H.01 Bit 0 still appears unlocked to the system processor during read opreations.

This is a read/write bit and is set to zero at power-on-reset.

7.7.10 PR12 Scratch Pad, Read/Write Port = 3?5H, Index = 2BH

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

7.7.11 PR13 Interlace H/2 Start, Read/Write Port = 3?5H, Index = 2CH

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up.

In interlaced operations, this register defines the starting horizontal character count at which vertical timing is clocked on alternate fields. Interlaced operation is enabled by setting PR14(5) to 1.

All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE

In the above expression, HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

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7.7.12 PR14 Interlace H/2 End, Read/Write Port = 3?5H, Index = 2DH

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bits 7 through 5 are set to 0 by reset.

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up.

Bit 7 - Enable IRQ.

This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

0 = IRQ disabled. Used in VGA operations with an AT bus and Micro Channel operations.

1 = IRQ enabled.

Bit 6 - Vertical Double Scan.

This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed Line Counter and Row Scan Counter to be clocked by divide-by-two horizontal timing, if vertical sync polarity (3C2H Bit 7 = 0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: N=2(n+1).

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5 - Interlaced Mode.

The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000. Line compare and double scan are not supported.

0 = Interlaced Mode not enabled.

1 = Interlaced Mode is enabled.

Bits (4:0) - Interlaced H/2 End Bits (4:0).

Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program the five LSBs of the sum into these bit locations.

7.7.13 PR15 Miscellaneous Control 1, Read/Write Port = 3?5H, Index = 2EH

BIT	FUNCTION
7	Read 46E8H Enable
6	High VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7- Enable Reading Port 46E8H.

This bit is functional only if AT BUS architecture [CNF(2)=1] is selected.

1 = I/O Port 46E8H may be read, regardless of the state of its own Bits 4 and 3 and of Port 102H, Bit 0 (sleep bit). Only Bits(4:0) of Port 46E8H are readable, Bits (7:5) are 0.

Bit 6 - High VCLK.

This bit should be set to 1 when (MCLK in MHz / VCLK in MHz) equals 1.5, or in an extended 256-color mode.

1 = Memory timing is adjusted to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency.

Bit 5 - Latched VCLK1 and VCLK2.

This bit is used only if CNF(3) = 1, which configures the VCLK1 and VCLK2 pins as outputs.

1 = Outputs VCLK2 and VCLK1 are equal to Bits 3 and 2 of I/O write register (Miscellaneous Output Register) at Port 3C2H, respectively.

Bit 4 - Select MCLK as Video Clock.

1 = MCLK input is selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3 - Interlaced Compatibility.

This bit should be set to 1 only if interlaced mode is selected (see PR14) and exact timing emulation of the IBM 8514/A's interlaced video timing is required.

1 = Vertical sync is generated from the trailing edge of non-skewed horizontal sync instead of the leading edge, as generated for VGA timing. Also, two VCLK delays are removed from the default VGA video dot path delay chain.

Bit 2 - Select Page Mode Addressing.

Graphics Modes automatically use Page Mode addressing.

Alpha modes require this bit to be set to 1 for screen refresh memory read cycles to use Page Mode addressing. Setting this bit to 1 in any Alpha Mode overrides the character map select functions of PR2(2) and PR2(5).

Page Mode addressing requires less time than RAS-CAS addressing, therefore, selecting Page Mode addressing increases the bandwidth for the CPU to access video memory by 30-40%.

Bit 2 should be set to 1 if 132 Character Mode timing is selected (see description of PR2).

When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight 8K memory segments containing a pair of maps in Plane 3 or Plane 2 is addressed by Bits (2:0) of this register while the map selection is determined by Bits(4:3). A pair of adjacent 8K character maps in Planes 3 and 2, (adjacent in the sense that they have the same addressing) may be selected by Bit 3 of the attribute code.

The character attribute, Bit 3, in conjunction with Bits 4 and 3 of the Character Map Select Register (3C5.03), determine a character map from either Plane 3 or Plane 2 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE

The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1, internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1 - Display Enable Timing Select.

This bit is used to select between two types of display enable timings available at output pin $\overline{\text{BLANK}}$ if PR4(7) = 1. If PR4(7) = 0, this bit has no effect.

0 = $\overline{\text{BLANK}}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{\text{BLANK}}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0 - Disable Border.

Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.7.14 PR16 Miscellaneous Control 2, Read/Write Port = 3?5H, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7 - Lock External 46E8H Register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to Port 46E8H.

Bits (6:5) - CRTC Address Counter Width.

Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory, in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. See the following table.

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bits (4:3) - CRTC Address Counter Offset.

Bits 4 and 3 are summed with the CRT Controller's Address Counter Bits CA(17) and CA(16), respectively, and the two-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2 - Enable Page Bit for Odd/Even.

This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the Page Bit for Odd/Even [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size Bits PR1(7:6).

Bit 1 - VGA Memory Mapping.

Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size Bits PR1(7:6).

Bit 0 - Lock RAMDAC Write Strobe (3C6H - 3C9H).

0 = Normal operation.

1 = Output $\overline{\text{WPLT}}$ to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C31, is also protected from the modification but may still be read at the Port 3C7H.

7.7.15 PR17 Miscellaneous Control 3, Read/Write Port = 3?5H, Index = 30H

BIT	FUNCTION
7:6	Reserved
5	Character Clock Period Select
4	PCLK = $^{VCLK}/_{2}$
3	Map Out 4K Of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map Out 2K Of BIOS ROM

Bits (7:6)
Reserved.

Bit 5: - Character Clock Period Select.

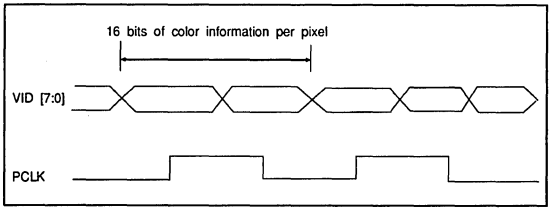
To enable PR17 Bit 5, PR2 (3CF.0C) Bits 4:3 must equal 11. When Bit 5 is not enabled, it has no effect.

0 = Six-dot font is selected.

1 = Ten-dot font is selected.

Bit 4 - PCLK = $^{VCLK}/_{2}$.

1 = Forces PCLK = $^{VCLK}/_{2}$. This control is useful for interface with high color RAM-DAC as follows:



Bit (3) - Map Out 4K of BIOS ROM.

1 = Disables access of the BIOS ROM in the system address range C600:0H through C6FF:FH.

Power-on-reset sets this bit to 0.

Bit 2 - Enable 64K BIOS ROM.

1 = Enables access of the BIOS ROM in the system address range C000:0H through CFFF:FH.

Power-on-reset sets this bit to 0.

Bit 1 - Hercules Compatibility.

1 = Locks Hercules compatibility register (I/O Port 3BFH).

Power-on-reset sets this bit to 0.

Bit 0 - Map Out 2K of BIOS ROM.

1 = Disables access of the BIOS ROM in the system address range C600:0H through C67F:FH.

Power-on-reset sets this bit to 0.

7.7.16 PR18 CRTC Vertical Timing Overflow, Read/Write Port = 3?5H, Index = 3EH

These bits, combined with other vertical timing overflow bits in CRTC, constitutes an 11-bit vertical timing control. These bits are set to zero at power-on-reset.

BIT	FUNCTION
7:5	Reserved
4	Line Compare Bit 10
① 3	Start Vertical Blank Bit 10
① 2	Start Vertical Retrace Bit 10
② 1	Vertical Display Enable End Bit 10
① 0	Vertical Total Bit 10

① The bit is locked if PR3(0) = 1 OR the 3?5 Index 11 Bit 7 = 1

② The bit is locked if PR3(1) = 0 AND the 3?5 Index 11 Bit 7 = 1

7.7.17 PR19 Video Signature Analyzer Control Read/Write Port = 3?5H, Index = 3FH

BIT	FUNCTION
7:4	Reserved
3	SIgnature Read Enable
2	Enable Video Input
1	PreLoad Control
0	Enable/Status Bits

Bits (7:4)

Reserved

Bit 3 - Signature Read Enable.

1 = Read signature analyzer results from 3?5H, Index 20 and 21.

Bit 2 - Enable Video Input.

This bit is used for self-test.

0 = Enable video input for signature analyzer.

1 = Self-testing. The video input to the signature analyzer is disabled.

Bit 1 - Preload Control.

0 = The Signature Analyzer Result Register (3?5, Index 20 and 21) is preloaded with 0001H.

1 = Normal operation.

Bit 0 - Enable/Status Bits.

Writing to this bit:

1 = Enables the signature analyzer to collect signature on video input.

Reading this bit:

Indicates the status of the signature analyzer collecting the signature on video input.

0 = Finished (or not enabled).

1 = Busy.

7.7.18 PR1A Shadow Register Control, Read/Write Port = 3?5H, Index = 3DH

Bits (7:4)

Reserved.

Bits 3 - I/O Read Select.

0 = Select actual CRTC registers for read.

1 = Select shadow CRTC registers for read.

Bits (2:0) - Shadow Lock.

101 = Locks all the shadowed register bits. This lock overrides any locks. Refer to the shadow register description for details.

7.7.19 PR20 Unlock Sequencer Extended Registers, Read/Write Port 3C5H, Index = 6H, (Reset State = Locked)

A value of X1X01XXXX (48H) must be written to this register to allow Read or Write operations of the Sequencer Extended Registers. When the extended registers are locked, the Sequencer Index is read as three bits. When unlocked, the Sequencer Index reads as six bits.

7.7.20 PR21 Display Configuration Status and Scratch Pad Bits Register, Bits 7:4 Read/Write Bits 3:0, Read Only Port 3C5H, Index = 7H

This register provides a convenient location for determining the current state of the VGA configuration. This information is required for many BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2 Bit 0
2	Status of PR2 Bit 6
1	Status of PR4 Bit 1
0	Status of PR5 Bit 3

Bits (7:4) - Scratch Pad Bits.

These read/write bits serve as a scratch pad for any BIOS status data that may need to be saved. These bits are preset to 1111 at reset.

Bit 3 - Status of 3C2H Bit 0.

This read only bit represents the setting of the I/O address select bit in the Miscellaneous Output Register.

0 = MDA (3Bx) addresses have been selected.

1 = CGA (3Dx) addresses have been selected by this read-only bit.

Bit 2 - Status of PR2 Bit 6.

This read only bit represents the setting of the VGA/6845 select bit in PR2 (3CFH Index CH).

0 = VGA or EGA compatibility has been selected.

1 = 6845 compatibility has been selected by this read-only bit.

Bit 1 - Status of PR4 Bit 1.

This read only bit represents the setting of the VGA/EGA select bit in PR4 (3CFH Index EH).

1 = EGA compatibility has been selected by this read-only bit.

0 = VGA was selected.

Bit 0 - Status of PR5 Bit 3.

This read only bit represents the setting of the Analog/TTL status bit in PR5 (3CFH Index FH).

0 = An analog monitor was selected.

1 = A TTL-type monitor was selected.

7.7.21 PR22 Scratch Pad Register, Read/Write Port = 3C5H, Index = 8H

Bits (7:0)

Scratch pad bits.

7.7.22 PR23 Scratch Pad Register, Read/Write Port = 3C5H, Index = 9H

Bits (7:0)

Scratch pad bits.

7.7.23 PR30 Memory Interface, Write Buffer and FIFO Control Register, Read/Write Port = 3C5H, Index 10H

This register controls display memory data width and its bandwidth. All bits are reset to zero at power-on-reset.

BIT	FUNCTION
7:6	Write Buffer Control
5	32-bit or 16-bit Memory Data Path
4	Disable 16-bit CPU Interface for Unchain Mode
3	Two-level FIFO
2	Four or Eight-level FIFO
1:0	Display FIFO control

Bits (7:6) - Write Buffer Control.

Bits 7 and 6 determine the depth of the write buffer.

PR31 Bit 2 must be set to 1 for these two bits to have any effect.

BITS 7 6	WRITE BUFFER LEVEL
00	One level deep.
01	Two levels deep.
10	Three levels deep.
11	Four levels deep.

Bit 5 - Memory Data Path.

0 = The display memory data path is 32-bits wide.

1 = The display memory data path is 16-bits wide.

Bit 4 - Disable Unchained Mode.

0 = Normal conditions.

1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3 - Two-level FIFO.

0 = The FIFO is four or eight levels deep, depending on Bit 2 of this register.

1 = The FIFO is two levels deep, regardless of Bit 2.

Bit 2 - Four or Eight-Level FIFO.

0 = FIFO set to eight levels deep.

1 = FIFO set to four levels deep.

Bits (1:0) - Display FIFO Control.

These two bits can be used to adjust the display memory bandwidth. In general, to accommodate most applications, it is recommended that these two bits be set to 01. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

BIT	FUNCTION	
00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

7.7.24 PR31 System Interface Control, Read/Write Port = 3C5H, Index = 11H, Reset State = 00

This register provides the control bits for the system interface. This register should be set during the post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 is used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7 - Read/Write Offset Enable.

0 = Normal (Refer to PR0A and PR0B definitions).

1 = During read cycles, the offset register PR0-A, is added to the CPU address. During write cycles PR0-B is added to the CPU address.

Bit 6 - Turbo Mode for Blanked Lines.

0 = Normal.

1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.

Bit 5 - Turbo Mode for Text.

0 = Normal.

1 = Improved text mode performance.

Bits (4:3) - CPU Read RDY Release Controls 1,0.

These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier, since it takes longer to complete the read cycle.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle.

01 = RDY is inserted 1MCLK before the end of a CPU memory cycle.

10 = RDY is inserted 2MCLK before the end of a CPU memory cycle.

11 = RDY is inserted 1MCLK after the end of a CPU memory cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2 - Enable Write Buffer.

0 = Write buffer disabled.

1 = Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.

Bit 1 - Enable 16-bit I/O Attribute Controller.

If Bit 1 and Bit 0 are both set to 1, the Attribute Controller (3C0H/3C1H) is configured for 16-bit access. The index is at 3C0H while the data is at 3C1H and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for eight-bit cycles. $\overline{\text{IOCS16}}$ is asserted for all cycles to 3C0H or 3C1H.

Bit 0 - Enable 16-bit I/O Operations.

0 = The VGA I/O is eight-bits.

1 = Enables 16-bit access to the CRTC (3?4H/3?5H), Sequencer (3C4H/3C5H) and Graphics Controller (3CEH/3CFH). The output $\overline{\text{IOCS16}}$ will be active for any I/O read or write to these addresses.

7.7.25 PR32 Miscellaneous Control 4, Read/Write Port = 3C5H, Index = 12H, Reset State = 00

This register provides control for several different features. Some of these features help to support Genlock of the WD90C31 to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow Read Back in Backward compatible Modes
0	Force Standard CPU Addressing in 132-column Mode

Bit 7 - Enable External Sync Mode.

0 = Normal operation mode.

1 = $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external $\overline{\text{HSYNC}}$ signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID 7:0 and PCLK output buffers, but they are used to genlock the WD90C31 to another display controller.

Bit 6 - Disable Cursor Blink.

0 = Blink enabled.

1 = The text cursor blink is disabled and the cursor remains on. This option can be used when cursor blink is not desired.

Bit 5 - USR1 Function Select.

0 = The USR1 output reflects the state of Bit 4. This can be used to control new features added by the system board designer.

1 = The USR1 output is slected by PR35 Bits 5, 4 and 3. See PR35 description.

Bit 4 - USR1 Control.

Controls the USR1 output when selected by Bit 5.

Bit 3 - USR0 Function Select.

0 = The USR0 output represents the state of Bit 2. This can be used to control new features added by the system board designer.

1 = The USR0 output is selected by PR35 Bits 2, 1 and 0. See PR35 description.

Bit 2 - USR0 Control.

Controls the USR0 output when selected by Bit 3.

Bit 1 - Read Backward in Compatible Modes.

0 = Registers that are not normally readable in backward compatibility modes may not be read.

1 = Registers that are not normally readable in backward compatibility modes may be read.

This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0 - 132-Column Mode.

1 = The special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This is used only for special virtual VGA applications.

7.7.26 PR33 DRAM Timing and Zero Wait State Control Register, Read/Write Port = 3C5H, Index = 13H

Bits (7:6) - $\overline{\text{0WS}}$ Control.

These two bits control the operation of the $\overline{\text{0WS}}$ output pin. $\overline{\text{OWS}}$ is disabled if PR31 bit 2 = 0 (Write Buffer is off).

00 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready.

01 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready and the memory address is decoded.

10 = $\overline{\text{0WS}}$ = 0 if the internal write buffer is ready and the memory address is decoded and MWR = 0.

11 = $\overline{\text{0WS}}$ = 0 if the condition in 10 is true or I/O write to the WD90C31 is occuring.

Bit 5

Reserved

Bits (4:3) - $\overline{CAS}$ Timing.

These two bits control the $\overline{CAS}$ timing.

00 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1 MCLK + (4~7) ns.
$\overline{CAS}$ high is 1 MCLK - (4~7) ns.

01 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1 MCLK + (8~14) ns.
$\overline{CAS}$ high is 1 MCLK - (8~14) ns.

10 = $\overline{CAS}$ cycle is 2 MCLKs.
$\overline{CAS}$ low is 1.5 MCLKs.
$\overline{CAS}$ high is 0.5 MCLKs.

11 = Reserved.

Bit 2 - $\overline{CAS}$ After $\overline{RAS}$ Timing.

0 = $\overline{CAS}$ cycle starts 2.5 MCLKs after $\overline{RAS}$ low.

1 = $\overline{CAS}$ cycle starts 1.5 MCLKs after $\overline{RAS}$ low.

Bits (1:0) - $\overline{RAS}$ Precharge.

These two bits control $\overline{RAS}$ precharge. Refer to DRAM timing adjustments in Section 6.0.

00 = $\overline{RAS}$ high is 2-1/2 MCLKs plus a 4-7 ns. delay.

01 = $\overline{RAS}$ high is 3 MCLKs wide.

10 = $\overline{RAS}$ high is 2 MCLKs wide.

11 = $\overline{RAS}$ high is 2-1/2 MCLKs.

7.7.27 PR34 Video Memory Mapping Register, Read/Write Port = 3C5H, Index = 14H

Bits (7:4)

Reserved

Bits (3:0) - Video Memory Mapping.

These four bits are compared with the CPU address A(23:20) as part of the video memory address decoding. This allows the VGA to be mapped into any 1 Mbyte CPU memory space. This register does not affect the $\overline{EBROM}$ and $\overline{ROM16}$ decoding. $\overline{EBROM}$ and $\overline{ROM16}$ are still decoded at A(23:20) = 0H. Used with the correct setting of PR1, Bits 5 and 4, this register supports virtual VGA applications.

These four bits are set to 0 at power-on-reset.

7.7.28 PR35 USR0, USR1 Output Select Register, Read/Write Port = 3C5H, Index = 15H

This register determines which internal signals can be observed through USR0 and USR1 output pins. This is for debug purposes and may be useful for using internal signals to control external functions. PR35, Bits 5 and 3, must be set to 1 for this register to have any effect.

Bits (7:6)

Reserved.

Bits (5:3) - USR1.

000 = USR1 = 1 if WD90C31 is fetching fonts from DRAM.

001 = USR1 = 1 if WD90C31 is fetching graphics data from DRAM.

010 = USR1 = 1 if the internal write buffer is ready.

011 = USR1 = 1 if a CPU write cycle is occurring.

100 = USR1 = 0 if a CPU write cycle is not caused by write buffer.

101 = Reserved.

110 = Reserved.

111 = Reserved.

Bits (2:0) - USR0.

000 = USR0 = 1 if I/O address is decoded.

001 = USR0 = 1 if WD90C31 is fetching character attributes from DRAM.

010 = USR0 = 0 if the internal write buffer is not empty.

011 = USR0 = 1 if CPU read cycle is occurring.

100 = USR0 = 0 if a write buffer cycle is occurring.

101 = Reserved.

110 = Reserved.

111 = Reserved.

7.8 INTERNAL I/O PORTS

7.8.1 AT Mode Setup, Enable, Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7:5	Reserved
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bits (7:5)

Unused.

Bit 4 - Setup.

This bit puts the WD90C31 into Setup mode where only I/O Port 102H is accessible.

Bit 3 - Enable I/O and Memory Accesses.

This bit enables I/O and memory accesses.

Bits (2:0) - BIOS ROM Page Select.

On I/O accesses to Port 46E8H, $\overline{\text{EBROM}}$ becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits and define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM therefore, appears to consist of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using these bits (D2:D0). The WD90C31 also provides Port 3C3H as an alternative to Port 46E8H. If a pull-down resistor is connected to MD(9) during power-on-reset (CNF9 = 0), Port 3C3H is decoded instead of Port 46E8H to support the same functions as described above. Otherwise, Port 46E8H is selected and decoded.

7.8.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7:1	Reserved
0	Wakeup VGA

Bits (7:1)

Unused.

Bit 0 - Wakeup VGA.

Wakeup VGA for I/O and Memory Accesses. Only the lower three address bits are decoded for this port and the WD90C31 must be in Setup mode. VGA Enable Sleep bit or Programmable Option Select (POS) Register 102H Bit 0 is used to awaken the WD90C31 after power on in the MCA and AT mode. To enter the Setup mode in AT bus applications, Bit 4 of the partially decoded internal I/O Port 46E8H is set to 1 before accessing the I/O Port 102H. In MCA mode, the WD90C31 is in Setup mode and Port 102H can be accessed when the VGASETUP ($\overline{\text{EIO}}$) signal pin is active low.

7.9 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C31. However, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals required by the RAMDAC are provided by the WD90C31. Setting PR(16) Bit 0 to 1 de-asserts $\overline{\text{WPLT}}$ disabling I/O writes to the RAMDAC. Normally, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL Address Port (Write)	Read/Write Port
3C7H	PEL Address Port (Read)	Read Only Port
*3C7H	*DAC State (Read Only)	* If Bits 1:0 = 1, DAC is in read operation. When Bits 1:0 = 0, DAC is in write operation. Bits 7-2 are reserved.
3C6H	PEL Mask (Read/Write)	Not to be written to by application code. To do so changes the color look-up table.
3C9H	PEL Data Register (Read/Write)	Three successive read/write bytes.
* This port is internal to the WD90C31.		

TABLE 7-11. VIDEO RAMDAC PORTS

7.10 WD90C31 CONFIGURATION REGISTER BITS CNF(18:0)

Memory Data Lines (18:0) [MD(18:0)] are used to input configuration data [CNF(18:0)] at power-on-reset (RST) by pull-up or pull-down resistors. This configuration data sets the bits in internal registers. CNF15:12, CNF10 and CNF0 can also be changed by software, while all others are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on. All MD(18:0) are internally pulled up by 50 ohm resistors.

CNF	FUNCTION
18	Enable $\overline{\text{ROM16}}$ as $\overline{\text{EXBLANK}}$ input
17	
16	64K by 16 or 256K by 4 DRAM select
15:12	EGA Switches
11	A23 - A20 Connection Select
10	Disable $\overline{\text{ROM16}}$ address decode
9	46E8H/3C3H Select
8	Display Status
7:4	General Purpose Status
3	Video Clock Source Control
2	AT/MCA Bus Select
1	ROM Configuration
0	BIOS ROM Mapping

CNF(18) - $\overline{\text{ROM16}}$ As $\overline{\text{EXBLANK}}$ input.

0 = A 4.7K pull-down resistor on Pin MD(18). $\overline{\text{ROM16}}$ is configured as $\overline{\text{EXBLANK}}$ input.

1 = No pull-down resistor, the internal pull-up sets CNF(18) to 1. Normal $\overline{\text{ROM16}}$ operation. $\overline{\text{ROM16}}$ is an output.

CNF(16) - 64K By 16 Or 256K By 4 DRAM Select.

0 = A 4.7K pull-down resistor on pin MD(16) sets the WD90C31 to interface with a 64K by 16 DRAM.

1 = No pull-down resistor. The internal pull-up sets WD90C31 to interface with a 256K by 4 or 256K by 16 DRAM.

CNF(15:12) - EGA Configuration Switches SW4-SW1.

No external pull-down resistors on MD(15:12) causes PR11(7:4) to be latched high. Pulling down MD(15:12) causes these bits to be latched low.

PR11(7:4) are writable bits. These bits can be read as Bit 4 of Port 3C2H (as on a standard EGA) if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of which bit to read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2H, as follows.

WRITE		READ
3C2 Bit 3	3C2 Bit 2	3C2 Bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF(11) - A23 - A20 Connection Selection.

0 = A 4.7K pull-down resistor on the Pin MD8.

The A23 pin should be connected to the NOR of AT bus signals LA(23:20).

The A(22:20) pins should be connected to the AT bus signals LA(19:17), unlatched CPU address.

The A(19:17) pins should be connected to AT bus SA(19:17), latched CPU address. This allows the WD90C31 to directly drive $\overline{\text{MEMCS16}}$ in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).

1 = No pull-down resistor. The internal pull-up sets CNF(11) to 1. Pins A(23:17) should be connected to AT bus signals LA(23:17). LA(23:17) are internally latched by ALE signal.

CNF(10) - Disable $\overline{\text{ROM16}}$ Address Decode.

0 = The internal pull-up sets CNF(10) = PR1(1) = 0. To enable the 16-bit BIOS, PR1(1) must be set to 1 by writing to Port 3CFH, Index 0BH Bit 1 and at the same time CNF(1) must be 1.

1 = A 4.7K pull-down on Pin MD10 sets CNF(10) = PR1(1) = 1. Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding.

This bit is read/write at PR1(1).

CNF(9) - 46E8H/3C3H Select.

This bit has no effect in Micro Channel applications.

0 = A 4.7K pull-down on Pin MD9. Port 03C3H is selected as the VGA setup and enable register instead of Port 46E8H in the AT interface.

1 = No pull-down resistor. The internal pull-up sets CNF(9) = 1. Port 46E8H is selected as VGA setup and enable register.

CNF(8) - Analog/TTL Display Status Bit.

CNF(8) is latched internally at power-on-reset from memory data bus Pin MD(11), provided with either a pull-up or pull-down external resistor.

Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached.

1 = TTL (EGA-compatible) display is attached.

CNF(7:4) - General Purpose Status Bits.

Bits CNF(7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pull-up or pull-down external resistors.

Pulling down MD(7:4) causes CNF(7:4) to be latched high.

These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F).

CNF(3) - Video Clock Source Control.

This bit cannot be written or read as I/O port.

Pulling up MD(3) causes CNF(3) to be latched high. It configures WD90C31 pins VCLK1 and VCLK2 as inputs or outputs.

0 = Inputs.

1 = Outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer.

When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to Port 3C2H. This load pulse may be inhibited by setting PR11(2) = 1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK2 and VCLK1 outputs are equal to Bits 3 and 2 of the Miscellaneous Output Register at 3C2H when PR15 Bit 5 = 1.

CNF (2) - AT/MCA Bus Architecture Select.

This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0 = Micro Channel architecture.

1 = AT BUS architecture.

Selecting CNF(2) changes the pinout definition between AT BUS and Micro Channel bus. (See Signal Description.)

PC-AT BUS	I/O	MICRO CHANNEL	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF(1) - ROM Configuration.

With an 8-bit system interface [CNF(1) = 0]:

Address bit A(0) = 0, selects the even ROM.
A(0) = 1, selects the odd ROM.

With a 16-bit system interface, [CNF(1) and PR(1) = 1] enables $\overline{\text{ROM16}}$.

This bit can not be written or read.

0 = No pull-down resistor on MD(1). The internal pull-up sets CNF(1) = 0 at power-on-reset. The WD90C31's data bus buffer controls are configured for one ROM (eight bits). PR1(1) can not be set high.

1 = The WD90C31's data bus buffer controls are configured for 16-bits (as with two ROMs). Setting CNF(1) to 1 enables the $\overline{\text{HTL}}$ output pin.

CNF (0) - BIOS ROM Mapping.

This bit may read or written at PR1(0).

0 = No pull-down resistor on MD(0). The internal pullup resistor sets this bit to 0 at power-on-reset.

1 = The BIOS ROM is mapped out. An external 4.7 Kohm pull-down resistor sets CNF(0) = 1 on power-on-reset.

8.0 HARDWARE CURSOR

The Hardware Cursor supports a user-defined pattern of up to 64 x 64 pixels, defined at 2 bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all packed and planar VGA graphics modes, as well as VGA text modes.

The registers are located at Port 23C2H/23C3H with Port 23C0H=2 and identified by the Index number in bits 15:12.

INDEX	FUNCTION
Index 0	Cursor Control
Index 1	Cursor Pattern Address Low
Index 2	Cursor Pattern Address High
Index 3	Cursor Primary Color
Index 4	Cursor Secondary Color
Index 5	Cursor Origin
Index 6	Cursor Display Position X
Index 7	Cursor Display Position Y
Index 8	Cursor Auxiliary Color

TABLE 8-1. CURSOR REGISTERS

8.1 CURSOR CONTROL REGISTER, INDEX 0

The Cursor Control register controls operation of the hardware cursor.

BIT	FUNCTION
15:12	0000 (Index)
11	Cursor Enable
10:9	Cursor Pattern Type
8	Cursor Plane Protection
7:5	Cursor Color Mode
4:0	Reserved

Bits (15:12) - Index 0.

Bit 11 - Cursor enable.

0 = Cursor is not displayed.

1 = Cursor is displayed.

Bits (10:9) - Cursor pattern type.

00 = Cursor is 2 bits per pixel, 32x32 pixels.

01 = Cursor is 2 bits per pixel, 64x64 pixels.

10 = Reserved.

11 = Reserved.

Bit 8 - Cursor plane protection.

0 = Cursor plane protection disabled.

1 = Cursor plane protection enabled.

Bits (7:5) - Cursor color mode.

000 = Straight monochrome (compatibility).

001 = Two-color cursor with inversion.

010 = Two-color cursor with special inversion.

011 = Three-color cursor.

100 = Reserved.

101 = Reserved.

110 = Reserved.

111 = Reserved.

Bits (4:0)

Reserved.

8.2 CURSOR PATTERN ADDRESS

The two Cursor Pattern Address registers form a 20-bit address, specifying the location in the display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin. The cursor pattern may be stored anywhere in the display memory, but is generally stored in a non-visible location.

Generally, this address represents the CPU address at which the pattern begins, minus the CPU address of the top-left corner of the screen, in whichever current VGA mode is in use. Not all addresses are valid in all modes. See the section on "Cursor Address Mapping."

NOTE

A write to either of the Cursor Pattern Address Registers or the Cursor Origin Register does not take effect until the beginning of a video frame following the next write to the Cursor Control Register. (In interlace mode, it's the next video field.)

8.2.1 Cursor Pattern Address Low, Index 1

BIT	FUNCTION
15:12	0001 (Index)
11:0	Cursor Pattern Address Bits 11:0

8.2.2 Cursor Pattern Address High, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:9	Reserved
8:0	Cursor Pattern Address Bits 20:12

8.3 CURSOR ORIGIN, INDEX 5

The Cursor Origin register specifies the offset in pixels from the top-left corner of the pattern which will be displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

For 32 x 32 cursor patterns each field is restricted to the values 31-0.

BIT	FUNCTION
15:12	0101 (Index)
11:6	Cursor Origin Y (63-0)
5:0	Cursor Origin X (63-0)

8.4 CURSOR DISPLAY POSITION

The Cursor Display Position X and Y registers specify the location on the screen at which the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels not characters. The cursor can be displayed at any position on the screen, including between characters.

NOTE

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. (In interlace mode, it's the next video field.)

8.4.1 Cursor Display Position X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11	Reserved
10:0	Cursor Display Position X

8.4.2 Cursor Display Position Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:10	Reserved
9:0	Cursor Display Position Y

8.5 CURSOR COLOR REGISTERS

The cursor color registers control the display of 2-bit per pixel cursor patterns.

The Cursor Primary Color, Cursor Secondary Color and Cursor Auxiliary Color registers specify eight-bit colors to be displayed for different parts of the cursor pattern.

NOTE

Even in planar mode, with four-bit pixels, these colors are 8 bits per pixel.

8.5.1 Cursor Primary Color, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:8	Reserved
7:0	Cursor Primary Color

8.5.2 Cursor Secondary Color, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:8	Reserved
7:0	Cursor Secondary Color

8.5.3 Cursor Auxiliary Color, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color

8.6 CURSOR REGISTER UPDATES

When a new cursor pattern is selected, up to four different registers must be updated. If a new video frame were to begin before all registers were updated, a single frame could be displayed with incorrect cursor data. While the display would recover within one video frame, the results would be visually annoying. Therefore, the WD90C31 holds off use of updated register data until all of the associated registers have been updated.

Writing to either the Cursor Pattern Address register or the Cursor Origin register does not take effect until the beginning of a video frame followng the next write to the Cursor Control register. Therefore, the Cursor Control register must be written to after up-dating either of these registers, even if the data in the Cursor Control register is to remain unchanged. However, reading any of these registers always returns the data last written to the register, whether or not such data has already taken effect.

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. In interlaced mode, updates occur at the beginning of a video field rather than frame.

8.6.1 Cursor Address Mapping

Cursor patterns are always stored in contiguous locations in display memory, usually in a non-visible portion, and always across all four maps. The definition of contiguous locations differs slightly by mode, as defined in the following tables.

Each mode has restrictions on where a cursor pattern may begin and how such a pattern must be stored. The location where the currently required cursor pattern is stored in display memory is loaded by the host into the Cursor Pattern Address registers, according to the following tables.

The Cursor Pattern Address registers point to the doubleword starting region of the cursor pattern. They are not byte addesses and consecutive register values generally do not point to consecutive memory bytes. However, the cursor pattern must use all of the consecutive memory bytes (1K or 256 bytes) assigned to it starting from the byte pointed to.

PLANAR MODES	
CPU Address	**Cursor Pattern Address**
Bank 0	
A0000 ①	
Map 0	0 If pattern starts here . . .
Map 1	② then next byte is here . . .
Map 2	② then here . . .
Map 3	② then here . . .
A0001	
Map 0	1 and fifth byte is here
⇓	
AFFFF	
Map 0	FFFF
Bank 1	
A0000	
Map 0	10000
⇓	
AFFFF ③	
⇓	
Map 3	1FFFF (Theoretical maximum for 1K X 1K display memory.)

256-COLOR MODES	
CPU Address	**Cursor Pattern Address**
Bank 0	
A0000 ①	0 If pattern starts here . . .
A0001	② then next byte is here . . .
A0002	② then here . . .
A0003	② then here . . .
A0004	1 and fifth byte is here
⇓	
AFFFC	3FFF
Bank 1	
A0000	4000
⇓	
Bank 0F	
⇓	
AFFFC ③	3FFFF (Theoretical maximum for 1K X 1K display memory.)

TEXT MODES	
CPU Address ④	**Cursor Pattern Or Pattern MaskAddress**
Maps 0:1	
B8000 ①	0 If pattern starts here . . .
B8001	② then next byte is here . . .
Maps 2:3	
B8000	② then here . . .
B8001	② then here . . .
Maps 0:1	
B8002	1 and fifth byte is here
B8003	
⇓	
BFFFE	3FFF
BFFFF	See the following notes.

NOTES

①. These locations are usually visible. In practice, cursor pattern is usually stored in non-visible memory.

②. Cursor pattern must start in map 0 but pattern is stored on all maps.

③. Some modes and/or boards may not support CPU addresses up to this level. Since up to 1K consecutive locations are required for the pattern, the pattern cannot actually start at the highest locations.

④. In mode 7, CPU addresses are B0000-B7FFE.

8.6.2 Two-Bit Cursor Pattern Format

The cursor pattern pointed to by the Cursor Pattern Address registers for two-bit cursor patterns is stored in either 1K or 256 consecutive memory byte locations. The cursor pattern data is stored for 64x64 and 32x32 cursors as follows:

8.6.2.1 Cursor Pattern - 2-bit, 64 x 64 cursors

Offset	Cursor Pattern
0 ①	Cursor pattern, AND plane, row 0, col. 0-7 ②.
1	Cursor pattern, XOR plane, row 0, col. 0-7.
2	Cursor pattern, AND plane, row 0, col. 8-15.
⇓	
15	Cursor pattern, XOR plane, row 0, col. 56-63.
16	Cursor pattern, AND plane, row 1, col. 0-7.
⇓	
1023	Cursor pattern, XOR plane, row 63, col. 56-63.

NOTES

① Offset is in bytes from cursor pattern starting location.

② Within each byte, the high-order bit represents the leftmost column.

8.6.2.2 Cursor Pattern - 2-bit, 32 x 32 cursors

Offset	Cursor Pattern
0	Cursor pattern, AND plane, row 0, col. 0-7.
1	Cursor pattern, XOR plane, row 0, col. 0-7.
2	Cursor pattern, AND plane, row 0, col. 8-15.
⇓	
7	Cursor pattern, XOR plane, row 0, col. 24-31.
8	Cursor pattern, AND plane, row 1, col. 0-7.
⇓	
255	Cursor pattern, XOR plane, row 31, col. 24-31.

8.6.3 Loading the Cursor Pattern

Loading a cursor pattern requires writing the pattern to a non-visible portion of display memory, then pointing to the pattern with the Cursor Pattern Address registers (Index 1, 2). A cursor pattern already in display memory can be selected simply by loading these registers.

In some VGA modes, certain maps are not defined but the physical RAM connected to those maps appears at higher memory locations in the maps that are defined. For instance, the first byte of map 2 may appear as the 64th Kbyte in map 0. Therefore a cursor pattern that occupies contiguous locations in one mode may appear fragmented in other modes. It is the responsibility of the software to track these fragments and assure that no part of the pattern will be accidentally overwritten.

8.6.4 Cursor Color Modes

A cursor may be displayed using any of four color modes selected by the Cursor Color Mode field of the Cursor Control Register (Index 1). Depending on the color mode selected, each 2-bit pixel of the cursor pattern will be displayed against the background as described in Table 8-2.

The "special" color generates the exclusive-NOR (XNOR) of the background and the Auxiliary Color Register (Index 8). This retains the "different from background" color property of inversion while adding the ability to specify one preferred "special inversion" from a background color to any desired color.

To use this feature, the Cursor Color Mode field must be set to "special", and the Cursor Auxiliary Color should be loaded with the exclusive NOR (XNOR) of the background color to be translated and the desired color to be displayed. When set in this manner, any screen pixel of the former color covered by an inverting cursor pattern pixel will be "inverted" into the auxiliary color.

8.6.5 Compatibility Differences Between Hardware and Software Cursor

Some cursor colors may display differently using the hardware cursor than when using a software cursor. This can happen in Planar Modes, because a software cursor modifies memory data that is then passed through the VGA Palette registers, while the hardware cursor operates on data at the output of the VGA Palette registers. The section on "Cursor Plane Protection" explains how to minimize these incompatibilities.

CURSOR PATTERN ①	COLOR MODE 0	COLOR MODE 1	COLOR MODE 2	COLOR MODE 3
00	All 0s ②	Secondary	Secondary	Secondary
01	All 1s ②	Primary	Primary	Primary
10	Transparent	Transparent	Transparent	Transparent
11	Inverted ②	Inverted ②	Special ③	Auxiliary

TABLE 8-2. CURSOR COLOR MODES

NOTES

① The high-order bit of each 2-bit pattern is the AND mask, the low-order bit is the OR mask.

② Cursor plane protection may apply in this case.

③ Background is XNOR'd with the auxiliary color.

8.6.6 Cursor Plane Protection

In 256-color modes, a background pixel covered by the cursor is either replaced by a specified 8-bit color or is inverted. For other modes, cursor plane protection is available.

When the Cursor Plane Protection bit of the Cursor Control register is set, some bits of the background are handled differently in certain cases. Cursor plane protection applies to all but transparency in cursor Mode 0 and to inversion in cursor Mode 1. In these cases the two or four high-order bits of the background are replaced with the corresponding bits of the Cursor Auxiliary Color register (Index 8).

When bit 7 of the VGA Attribute Mode Control register (Port 3C0H/3C1H, Index 10H) is reset, cursor plane protection applies to the two high-order bits of the background. When this bit is set, protection applies to the four high-order bits.

This feature is designed to provide as much flexibility and compatibility with a software cursor as possible, due to the processing done by the VGA attribute controller.

Typically when using cursor plane protection, the host driver sets the Cursor Auxiliary Color register's high-order bits to match the VGA Color Select register, which often maps most cursor pixels into the same palette locations as their software counterparts. Alternatively, those auxillary color bits may be set to point to an unused section of the palette and load the palette with all of the desired cursor colors for primary, secondary and all possible inversion colors. This latter method can be used for full color compatibility when necessary, as long as the driver has control over the loading of the external palette and the internal color registers.

9.0 HARDWARE BITBLT

The BITBLT hardware supports accelerated data transfers between regions of display memory. Display memory regions may be rectangular or linear.

A full complement of raster operations are available. Color expansion and transparency, useful for accelerating text modes as well as Plane Masking is also supported.

This same hardware can be used to rapidly copy 8X8 patterns and fill rectangles.

The BITBLT hardware supports text modes and monochrome, 4-bit, and 8-bit color modes.

Index 0	BITBLT Control - part 1*
Index 1	BITBLT Control - part 2
Index 2	BITBLT Source Low
Index 3	BITBLT Source High
Index 4	BITBLT Destination Low*
Index 5	BITBLT Destination High*
Index 6	BITBLT Dimension X
Index 7	BITBLT Dimension Y
Index 8	BITBLT Row Pitch
Index 9	BITBLT Raster Operation
Index A	BITBLT Foreground Color
Index B	BITBLT Background Color
Index C	BITBLT Transparency Color
Index D	BITBLT Transparency Mask
Index E	BITBLT Map And Plane Mask

* All or part of these registers can change automatically.

TABLE 9-1. BITBLT REGISTERS

9.1 SOURCE AND DESTINATION

The BITBLT Source Low and BITBLT Source High registers specify the source address for BITBLT operations. The BITBLT Destination Low and BITBLT Destination High registers specify the destination address. The high and low fields of each register pair are concatenated to form a 21-bit address pointing to the starting corner of the source or destination area.

The starting corner for source and destination will be either the top-left or bottom-right corner. The corner specified must be coordinated with the BITBLT Direction bit of the BITBLT Control register.

When the source and destination areas do not overlap, BITBLT can be started in either corner. When these areas overlap, the corner and direction must be selected to prevent parts of the source area from being overwritten by the destination array before they are copied.

When the BITBLT Update Destination bit in the BITBLT Control register is set, the host should not read the BITBLT Destination registers while a BITBLT is in progress, since these registers change just before the end of the operation.

When the BITBLT Quick Start bit in the BITBLT Control Register is set, writing these registers may start BITBLT operations.

9.1.1 BITBLT Source Low, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:0	BITBLT Source Position - Bits 11:0

9.1.2 BITBLT Source High, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:9	Reserved (Must Be 0)
8:0	BITBLT Source Position - Bits 20:12

9.1.3 BITBLT Destination Low, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:0	BITBLT Destination Position - Bits 11:0

9.1.4 BITBLT Destination High, Index 5

BIT	FUNCTION
15:12	0101 (Index)
11:9	Reserved (Must Be 0)
8:0	BITBLT Destination Position - Bits 20:12

9.2 ADDRESS MAPPING

The source and destination addresses are partially mode dependent. Addresses represent the character or pixel at the starting corner of the move, which may be the top left or bottom right corner.

9.2.1 Monochrome And Planar Modes

REGISTER ADDRESS	DISPLAY MEMORY LOCATION
0	All maps, location 0, bit 7 (left most pixel).
1	All maps, location 0, bit 6.
⇓	
7	All maps, location 1, bit 0 (right most pixel).
8	All maps, location 1, bit 7.
⇓	
512K - 1	All maps, location 64K-1, bit 0 ①.
512K	All maps, location 64K, bit 7.
⇓	
1M - 1	All maps, location 128K-1, bit 0 ②.
⇓	
2M - 1	All maps, location 256K-1, bit 0 ③.

① Last location in a 256 KB system.

② Last location in a 512 KB system.

③ Last location in a 1 MB system.

9.2.2 Packed Modes

REGISTER ADDRESS	DISPLAY MEMORY LOCATION
0	Map 0, location 0, entire byte (left most pixel).
1	Map 1, location 0, entire byte.
2	Map 2, location 0, entire byte.
3	Map 3, location 0, entire byte (right most pixel).
4	Map 0, location 1, entire byte.
⇓	
256K - 1	Map 3, location 64K-1, entire byte á.
256K	Map 0, location 64K, entire byte.
⇓	
512K - 1	Map 3, location 128K-1, entire byte ②.
⇓	
1M - 1	Map 3, location 256K-1, entire byte ③.
① Last location in a 256 KB system.	
② Last location in a 512 KB system.	
③ Last location in a 1 MB system.	

The location referred to in sections 9.2.1 and 9.2.2 is the CPU address offset in bytes from the top of the display memory for any given mode. For example, where display memory starts at CPU address A0000H, location 123H would correspond to CPU address A0123H. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64 Kbytes, location 10123H would correspond to CPU address A0123H in the second page of the display memory.

When the source or destination of a BITBLT operation is not a memory location, the corresponding pair of position registers are unused and may contain any value, except that the two or three low-order bits of the BITBLT Source Low register are still used to specify a source alignment of the data.

9.3 DIMENSIONS AND ROW PITCH

When neither source nor destination regions are rectangular, the product of the X and Y dimension values represents the number of pixels to be moved.

Linear areas larger than 2K pixels or bytes cannot be moved in a single operation unless the dimension can be expressed as a product of the two registers. In this case, best performance is obtained by selecting values that specify the X dimension as large as possible.

9.3.1 BITBLT Dimension X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension X *
* legal range is 1 to 2K pixels	

The BITBLT Dimension X register specifies the width of the rectangular region to be copied.

In Graphic Modes, this value is expressed in pixels.

In Text Modes, this value is expressed in the number of characters multiplied by eight (even though each character is stored using only two bytes).

9.3.2 BITBLT Dimension Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:0	BITBLT Dimension Y *
* legal range is 1 to 2K pixels	

The BITBLT Dimension Y register specifies the height of the rectangular region to be copied.

In Graphic Modes, this value is the height of the region in pixels.

In Text Modes, this value is the height of the region in character rows.

9.3.3 BITBLT Row Pitch, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:0	BITBLT Row Pitch *
* In Packed Mode, the two low order bits of this field must be zero. In Panar Mode, the three low order bits must be zero.	

The BITBLT Row Pitch register specifies the linear offset from any location in a given row to the same location in the next row. This offset is in the same units as the source and destination fields to which it applies.

When both source and destination are rectangular areas, the BITBLT Row Pitch applies to both areas. When either or both are non-rectangular, the offset does not apply to that range.

9.4 FOREGROUND AND BACKGROUND COLORS

The BITBLT Foreground and Background Color registers specify 8-bit or 4-bit digital colors to be used when expanding monochrome source areas. The foreground color can also be specified as the source of a BITBLT to produce a filled rectangle.

BITBLT Foreground Color, Index A

BIT	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	BITBLT Foreground Color *
* In Planar modes, only bits 3:0 are used to specify a color.	

BITBLT Background Color, Index B

BIT	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	BITBLT Background Color *
* In Planar modes, only bits 3:0 are used to specify a color.	

9.5 MAP AND PLANE MASK

The BITBLT Mask register controls both Plane and Map Masks used in BITBLT.

The BITBLT Map Mask field specifies a four-bit mask that prevents data in the specified maps from being updated. This map is needed for BITBLT in all text modes to prevent font data from being overwritten in a character-attribute move and vice versa, and VGA mode F. It can also be used in VGA modes 4, 5 and 6 for partial hardware support. Additionally, it can be used in VGA modes D, E, 10, 11 and 12 and extended Planar modes as a Plane Mask if desired.

The BITBLT Plane Mask field specifies an eight-bit mask that prevents data in the specified planes from being updated. It is useful in VGA Mode 13 and extended Packed modes when Plane Masking is desired.

BITBLT Mask - VGA, Index E

BIT	FUNCTION
15:12	1110 (Index)
11:8	Reserved
7:0	BITBLT Plane Map Mask Mode *
* In Planar Modes, only bits 3:0 are used.	

BITS 7:0	BITBLT PLANE MASK
XXXX XXX0	Plane 0 Disabled
XXXX XXX1	Plane 0 Enabled
⇓	
0XXX XXXX	Plane 7 Disabled
1XXX XXXX	Plane 7 Enabled

BITS 3:0	BITBLT MAP MASK
XXX0	Map 0 Disabled
XXX1	Map 0 Enabled
⇓	
0XXX	Map 3 Disabled
1XXX	Map 3 Enabled

9.6 RASTER OPERATIONS

The BITBLT Raster Operation register specifies a bitwise logical operation to be performed on the source and destination fields. This field is always active and must be loaded with the appropriate value even when a simple source copy is to be performed.

BITBLT Raster Operation, Index 9

BIT	FUNCTION
15:12	1001 (Index)
11:8	BITBLT Raster Operation
7:0	Reserved

The Raster Operation code is defined as follows.

For the two operands source and destination, define the results of the 2-input truth table below for the desired function. The source (S) and destination (D) form a 2-bit value in the table.

The four 1-bit results of the truth table for the desired operation in the form "abcd" form the raster operation code. The "a" is defined as the high-order bit of the code.

While the Raster Operation code represents a 2-input operation, both inputs are not always relevant in the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination field.

Arithmetic operations are not supported.

Table 9-2 presents the Raster Operation Codes.

BITBLT Truth Table

S D	Result
0 0	A
0 1	B
1 0	C
1 1	D

abcd	Function	abcd	Fucntion
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	S•$\overline{D}$	1010	Inv Dest
0011	Src	1011	S+$\overline{D}$
0100	$\overline{S}$•D	1100	Inv Src
0101	Dest	1101	$\overline{S}$+D
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 9-2.
RASTER OPERATION CODE

9.7 PATTERNS

The WD90C31 has a special mode to accelerate the copying of 8X8 source patterns. In this mode, an 8X8 full-color or monochrome pattern can be repetitively applied to a large destination area in an efficient manner.

To perform a pattern copy, the host first writes the 8X8 pattern to display memory in a linear fashion,usually to a non-visible location, depending on the current addressing mode, as described in sections 9.7.1 and 9.7.2. The host then loads the BITBLT Source registers, with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The BITBLT Pattern Select field of the BITBLT Control register must be set to 8X8 patterns.

To specify a monochrome pattern, the host must write a color pattern in the current mode, planar or packed, and then use the control registers to specify a single plane of the source to be used.

9.7.1 BITBLT Pattern Storage - Monochrome And Planar Modes

In planar mode, the 8X8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

PIXEL ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 8	Any data.
n*	All maps, top row of 8X8 pattern.
n + 8	All maps, second row of 8X8 pattern.
⇓	
n + 56	All maps, bottom row of 8X8 pattern.
n + 64	Any data.
* 'n' must be a multiple of 64	

9.7.2 BITBLT Pattern Storage - Packed Modes

In packed mode, the 8X8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region and the pattern wraps to the right and down from that point.

PIXEL ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data.
n*	Top row of 8X8 pattern, left most pixel.
n + 1	Top row of 8X8 pattern, second pixel.
⇓	
n + 7	Top row of 8X8 pattern, right most pixel.
n + 8	Second row of 8X8 pattern, left most pixel.
⇓	
n + 63	Bottom row 8X8 pattern, right most pixel.
n + 64	Any data.
* 'n' must be a multiple of 64	

9.8 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each 0 in the source region is replaced with the specified background color, while each 1 is replaced with the foreground color. All other processing options, including masks and raster operations, remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination will be filled with the foreground color, subject to masks, raster operations and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available, since the transparency color registers are in use.

9.9 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data extracted in this manner is replicated to each plane or map as if it had been read from the memory.

When extracted, monochrome data is usually extracted from color data in display memory. However, when the BITBLT source is the system I/O location, monochrome data can be extracted in the same manner.

To extract a single plane from a color source field, the BITBLT Transparency Color register should be loaded with FFH (all ones), while the BITBLT Transparency Mask register should be loaded with a 0 in the map or plane position to be extracted, and a 1 in all other positions.

Monochrome data is usually extracted as a specific bit of each 4-bit or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color 1, with all other colors returning a monochrome 0.

When the Monochrome Transparency bit is set in the BITBLT Control register, all monochrome source pixels of 0 do not affect the background, regardless of any selected raster operation.

The Transparency Enable and Polarity bits in this register have no effect on monochrome data extraction.

9.10 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually transparent, with the rest being opaque. Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color, since when OR'ed with the destination, it does not change.

Color destination transparency is supported by the WD90C31, in addition to the more limited monochrome transparency described elsewhere.

9.10.1 BITBLT Transparency Color, Index C

BIT	FUNCTION
15:12	1100 (Index)
11:8	Reserved
7:0	BITBLT Transparency Color *
* In Planar Modes, only the four low-order bits are used.	

The BITBLT Transparency Color register specifies an 8-bit or 4-bit digital color to be used as the transparency color.

9.10.2 BITBLT Transparency Mask, Index D

BIT	FUNCTION
15:12	1101 (Index)
11:8	Reserved
7:0	BITBLT Transparency Mask *
* In Planar Modes, only the four low-order bits are used.	

The BITBLT Transparency Mask register specifies an 8-bit or 4-bit mask for use in comparison against the transparency color.

The pixels of the destination are compared against the Transparency Color under control of the Transparency Mask. Each bit of the Transparency Mask that is a 1 makes the corresponding bit of the Transparency Color a "don't care".

The BITBLT Transparency Enable bit of the BITBLT Control register (Index 1) specifies whether Color Transparency is enabled or disabled. The BITBLT Transparency Polarity bit specifies whether pixels matching the Transparency Color are considered opaque, or considered transparent, in which case the destination at that location is not overwritten, and pixels not matching the Transparency Color cause the background not to be overwritten.

9.11 FILLED RECTANGLES

Filled rectangles can be drawn very efficiently by the BITBLT hardware. A filled rectangle is simply a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the Source Format field in the BITBLT Control register (Index 0) to "fixed color", and the Foreground Color register (Index A) to the desired fill color. A source address is not required. All other BITBLT options are available normally.

9.12 SYSTEM MEMORY TO DISPLAY MEMORY OPERATIONS

To copy data from system memory to display memory, the host may specify the source of a BITBLT as a system I/O location rather than display memory. In this case, display memory reads come from the 32-bit readback latch written by the host.

After starting the BITBLT operation, the host writes a series of doublewords to the readback latch. This 32-bit register is accessed by two consecutive writes to the 16-bit BITBLT I/O port, with the low-order word of this register written first. This port may also be accessed by two 8-bit writes as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a source read is required and data from the host is unavailable, the WD90C31 suspends the BITBLT operation until data becomes available. Similarly, when the host attempts to write the register before previous data in it has been processed, the WD90C31 holds off the host.

Conceptually, the 32 bits written by the host exactly replace the 32 bits that would have been read from the display memory. Just like the destination, the source may have any alignment. The two or three low-order bits (Packed or Planar Mode) of the BITBLT Source Low register (Index 2) specify the alignment of the source region. The other bits of the BITBLT Source Low register may have any value. That is, the pixel of the source word pointed to by those low-order bits corresponds to the first pixel of the destination.

NOTE

Source writes from the host are always performed in 32-bit groups, however the data is written to a 16-bit port. Therefore the host must always perform two 16-bit I/O writes at a time to the port, even when the remaining destination width is less than four or eight pixels.

Just like display memory, no source doubleword from the host may straddle two lines of the destination.

9.13 DISPLAY MEMORY TO SYSTEM MEMORY OPERATIONS

To copy data from display memory to system memory, the host may specify the source of a BITBLT as a system I/O location, rather than display memory. In this case, display memory writes are replaced by writes to a 32-bit register read by the host.

This 32-bit register is accessed by two consecutive reads of the 16-bit BITBLT I/O port. The low-order word of this register is read first. This port may also be accessed by two 8-bit reads, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a destination write is required and the host has not read data from the previous write, the WD90C31 suspends the BITBLT operation until the host catches up. Similarly, when the host attempts to read the register before data is available, the WD90C31 holds off the host.

Conceptually, the 32 bits read by the host exactly match the 32 bits that would have been written to the display memory. Unlike outputting to display memory, the destination is always doubleword aligned, that is, the first pixel of the source corresponds to the first pixel of the destination.

NOTE

Source reads by the host are always performed in 32-bit groups, however the data is read from a 16-bit port. Therefore the host must always perform two 16-bit I/O reads at a time from the port, even when less than 32 bits remain in the current line.

Just like display memory, no destination doubleword to the host may straddle two lines of the source.

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9.14 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION

The host may transfer monochrome data from system memory to display memory, and in the process, expand it to any two colors or one color plus transparent.

To accomplish this, the host sets the BITBLT Source Select field in the BITBLT Control register (Index 0) to "System I/O Location" and the BITBLT Source Format field to "Monochrome From Host". If transparency is desired, the Monochrome Transparency bit is also set. The BITBLT Foreground and Background Color registers (Index A and B) may also be set.

The host then issues a series of 16-bit I/O writes to the BITBLT I/O port which are expanded to eight 4-bit pixels. The remaining eight high-order bits are ignored. In Packed Mode, the four low-order bits are expanded to four 8-bit pixels and the remaining 12 bits are ignored.

The low-order bits of the BITBLT Source register (Index 2) work as in other system-to-video memory transfers.

No source word may straddle two lines of the destination. All other BITBLT options work normally in this mode.

9.15 CONTROL AND STATUS

BITBLT Control - Part 1, Index 0

BIT	FUNCTION
15:12	0000 (Index)
11	BITBLT Activation/Status*
10	BITBLT Direction
9:8	BITBLT Addressing Mode
7	BITBLT Destination Linearity
6	BITBLT Source Linearity
5:4	BITBLT Destination Select
3:2	BITBLT Source Format
1:0	BITBLT Source Select
* This bit is automatically reset when BITBLT is completed.	

Bits (15:12) - Index 0.

Bit 11 - BITBLT Activation/Status.

Writing a 1 to this bit starts a BITBLT operation using the currently loaded register values. This bit is reset automatically when the BITBLT operation is completed. Therefore, reading a 1 from this bit indicates a BITBLT opration is in progress.

Writing a 0 to this bit will not start a BITBLT operation, but may be useful in "quick start" mode to set the other bits in the register for the coming series of quick-start operations.

CAUTION

Writing a 0 to this bit while a BITBLT operation is in progress may cause unexpected and unrecoverable results.

0 = Do not start BITBLT (write), BITBLT completed (read).

1 = Start BITBLT (write), BITBLT in progress (read).

Bit 10 - BITBLT Direction.

0 = BITBLT direction is top to bottom, left to right.

1 = BITBLT direction is bottom to top, right to left.

Bits (9:8) - BITBLT Address Mode.

00 = Planar Mode (includes monochrome modes).

01 = Packed Mode, includes text and 256-color modes.

1X = Reserved for future expansion.

Bit 7 - BITBLT Destination Linearity.

0 = Destination area is rectangular.

1 = Destination area is linear.

Bit 6 - BITBLT Source Linearity.

0 = Source area is rectangular.

1 = Source area is linear.

Bits (5:4) - BITBLT Destination Select.

00 = Destination is screen memory.

10 = Destination is system I/O location.

X1 = Reserved for future expansion.

Bits (3:2) - BITBLT Source Format.

00 = Source format is color.

01 = Source format is monochrome from color comparators.

10 = Source format is fixed color (filled rectangle).

11 = Source format is monochrome from host.

Bits (1:0) - BITBLT Source Select.

00 = Source is screen memory.

10 = Source is system I/O location, 32 bits.

X1 = Reserved for future expansion.

BITBLT Control - Part 2, Index 1

BIT	FUNCTION
15:12	0001 (Index)
11	Reserved
10	BITBLT Interrupt Enable
9:8	Reserved
7	BITBLT Quick Start
6	BITBLT Update Destination
5:4	BITBLT Pattern Select
3	BITBLT Monochrome Transparency
2	BITBLT Transparency Polarity
1	Reserved, must be 0
0	BITBLT Transparency Enable

Bits (15:12) - Index 1.

Bit 11

Reserved.

Bit 10 - BITBLT Interrupt Enable.

0 = Do not interrupt on completion of BITBLT.

1 = Interrupt on completion of BITBLT.

Bits (9:8)

Reserved.

Bit 7 - BITBLT Quick Start.

Quick Start Mode

When BIT 7 is set, BITBLT starts automatically as soon as the BITBLT Destination Low register (Index 4) is written, unless automatic destination update is enabled for BITBLT, in which case the BITBLT starts automatically when the BITBLT Source Low register (Index 2) is written.

This mode permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control register operate as they were last written, and the BITBLT Activation bit is physically set and can be read back normally.

0 = BITBLT starts only when explicitly enabled.

1 = BITBLT starts automatically when destination register is written, or source register if destination update is enabled.

BIT 6 - BITBLT Update Destination.

Automatic Destination Update

A host doing multiple BITBLTs need only update those registers that change from one BITBLT to the next. Most BITBLT registers never change unless written by the host. The exceptions to this are the two BITBLT Destination registers (Index 4, 5) and the status bit in the BITBLT Control register (Index 0).

When bit 6 of this register is set, the BITBLT Destination registers are automatically updated at the end of each BITBLT operation to point to the rectangular region immediately to the right of the previous destination region. This is specifically aimed at improving text output operations. When the destination area is specified as linear rather than rectangular, the destination registers point to the location immediately past the previous destination area.

0 = Do not update destination on completion of BITBLT.

1 = Update destination on completion of BITBLT.

Bits (5:4) - BITBLT Pattern Select.

00 = Patterns are not used.

01 = 8X8 patterns are used for source.

1X = reserved for future expansion.

Bit 3 - BITBLT Monochrome Transparency.

0 = Monochrome transparency is not enabled.

1 = Monochrome transparency is enabled.

Bit 2 - BITBLT Transparency Polarity.

0 = Matching pixels are transparent.

1 = Matching pixels are opaque.

Bit 1

Reserved, must be set to 0.

Bit 0 - BITBLT Transparency Enable.

0 = Transparency is not enabled.

1 = Transparency is enabled.

10.0 REGISTER ACCESS

All of the WD90C31 enhanced functions are controlled by one or more registers, most of which are above and beyond standard VGA registers.

Some enhanced functions are controlled by VGA-type index/data register pairs, where one register acts as an index pointer for a group of registers while the other is a read/write port for the data.

Other enhanced functions are controlled by indexed register blocks. Each indexed register block can contain up to sixteen 12-bit indexed registers. The 4-bit register index is written, along with the 12-bit data field, to form a 16-bit word.

Access to the VGA-type registers is described elsewhere. This section only describes the access to indexed register blocks.

10.1 ACCESSING INDEXED REGISTERS

To write to one or more indexed registers within any register block, that register block must first be selected by loading its address into the Register Block Pointer field of the Index Control register. This causes the selected register block to appear at the Register Access port.

A 16-bit word is then written to the Register Access port. The four high-order bits specify the Index of the individual register being written, while the 12 low-order bits are the data to be written. Additional registers within the same register block may then be written without re-selecting that register block.

To read one or more indexed registers within a register block, the address of that register block is first written to the Register Block Pointer Field of the Index Control Register. The desired starting register to be read within the block is then written to the Register Index Field of this register. This causes the selected register to appear at the Register Access port. The Register Index Field and Register Block Pointer Field can be set with a single 16-bit write.

A 16-bit word is then read from the Register Access port. When reading an indexed register, the value returned contains the index of the register in the four high-order bits.

If the Auto-Increment Disable bit in the Index Control register is reset, consecutive reads to the Register Access port will return consecutively indexed registers within the same register block. Registers are read in ascending order through register F (the 16th register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Addressing a non-existant register results in zeros being returned in the 12-bit data field.

If the Auto-Increment Disable bit is set, consecutive reads return the same indexed register.

10.2 INDEX CONTROL REGISTER

The Index Control register is a read/write register which controls reads and writes to indexed registers blocks.

BIT	FUNCTION
15:14	Reserved
13	Invalid register block. This bit is read only
12	Auto-increment disable
11:8	Register Index. When read, this field returns the index of the next register to be read.
7:0	Register Block Pointer

Bit 13 - Invalid Register Block.

0 = Currently addressed register block exists on this device.

1 = Currently addressed register block does not exist on this device.

Bit 12 - Auto-increment Disable.

0 = Consecutive reads return consecutive indexed registers.

1 = Consecutive reads return the same indexed register.

10.3 SYSTEM CONTROL REGISTER BLOCK

The System Control register block contains registers controlling overall system functions.

Index 0	Interrupt Status

10.3.1 Interrupt Status Register, Index 0

Interrupt status information is provided by the Interrupt Status register in the System Control Register block. This register returns information as to which part of the WD90C31 caused an interrupt.

Reading this register does not reset any interrupts. Resetting of each interrupt is handled independently.

Unassigned interrupts are returned as zeroes.

BIT	FUNCTION
15:12	0000 (Index)
11	Interrupt 10 active
⇓	
8	Interrupt 7 active
7	High when at least one of the interrupts 10 through 7 is active
6	Interrupt 6 active
⇓	
1	Interrupt 1 active
0	Any interrupt is active

10.3.2 Global Port Map

Port 23C0H	Index Control register (low byte)
Port 23C1H	Index Control register (high byte)
Port 23C2H	Register Access Port (low byte)
Port 23C3H	Register Access Port (high byte)
Port 23C4H	BITBLT I/O Port
Port 23C5H	BITBLT I/O Port
Port 23C6H	Reserved
Port 23C7H	Reserved

10.3.3 Register Block Map

Pointer	Register Access Port Accesses
0	System Control registers
1	BITBLT registers
2	Cursor registers

10.3.4 Global Interrupt Map

Interrupt	Meaning
1	VGA interrupt
2	BITBLT interrupt

10.4 APPLICATION AND PROGRAMMING NOTES

10.5 USE OF THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE

The hardware cursor, while not specifically designed for hi-color mode operation, can still be used with certain limitations in that mode.

The hardware cursor is unaware of the existence of hi-color mode but can still be used by specifying two adjacent 2-bit pixel codes for each high-color cursor pixel. A transparent hi-color pixel would be specified using two adjacent transparency codes (1010), while a "color" hi-color pixel would usually be specified using adjacent primary and secondary color codes, such as 0100. The desired 16-bit cursor color would then be split between the 8-bit primary and 8-bit secondary color registers. Inversion is also available as 1111 but the results might not be visually desirable.

This limits the effective maximum cursor width in hi-color mode to 32 pixels. Further, the cursor origin and position are defined in terms of 8-bit, not the displayed 16-bit, pixels. Therefore, these values should be horizontal multiples of two.

Secondary and auxiliary color registers may be used to create additional cursor colors by mixing cursor codes within a 16-bit pixel region. It is important to keep in mind the effects of inversion in systems that use one bit to switch between false color and hi-color modes on a pixel-by-pixel basis.

10.6 BITBLT IN VGA MODES 4, 5, AND 6

VGA modes 4, 5 and 6 are partially supported by the WD90C31. Since these modes are not commonly used in Windows, the additional hardware required to support the even/odd scan line offset technique employed in these modes is not supported.

However, a BITBLT operation in these VGA modes can often be broken up into two or three BLT operations, each of which operates on a contiguous area of memory.

When the vertical offset between source and destination is an even number of rows, the desired operation can be broken into two BITBLTs, one for the even rows and one for the odd rows. This requires careful consideration of the register parameters, especially the BITBLT Dimension Y register.

Where the offset is an odd number of rows, it may still be possible to break up the operation into only two BITBLTs, provided there is no overlap between the source and destination regions. This is because information is being swapped between the even and odd scan line regions.

Where source and destination do overlap, it may be possible to use a scratch space in off-screen memory and break up the operation into three BITBLTs.

Another possibility is to break up a BITBLT into a series of one-line high operations that can be referred to as Line-BLTs. In this manner, a BITBLT may be simulated by the driver as a series of Line-BLTs.

10.7 BITBLT OPERATIONS IN TEXT MODE

BITBLT acceleration is available in VGA Text Modes. Text Mode BITBLTs generally consist of moving only character and attribute data (in maps 0 and 1), while leaving the font data (in maps 2 and 3) alone. The BITBLT mask is set to prevent update to those maps. For this reason, Planar (not Packed) Mode must be used. Similarly, the BITBLT mask can be set to move only character data, or only font data.

Each display memory location consists of four bytes: one character, one attribute and two font plane bytes that are not part of the character but happen to fall in the same location as the character, but on maps 2 and 3. In planar mode, this is a space of eight pixels. Therefore, the source and destination of a character BLIT must be multiples of eight. The X dimension is the number of character columns to be copied times eight but the Y dimension is simply the unmultiplied number of character rows. The row pitch is set to the CPU address offset between character rows times eight.

10.8 USE OF BITBLT IN 16-BIT PER COLOR MODE

The BITBLT hardware can be used in 16-bit per color hi-color mode with a few changes and a few limitations.

Hi-color BITBLTs should be performed in packed mode, remembering that each hi-color pixel takes up two adjacent normal packed pixels. The BITBLT Source and Destination registers should point to the first byte of the respective regions. Generally, the values in these register pairs are double the corresponding values for normal packed mode.

In a right-to-left BITBLT in hi-color mode, the source and destination values must point to the second byte of each region.

The BITBLT dimensions are twice the number of pixel columns, but the correct number of pixel rows. The Row Pitch register contains eight times the number of bytes between rows on the screen. Linear source and destination operate normally.

Monochrome to color expansion or plane masking is not generally useable. Raster operations are available, but often produce undesired results. Similarly, color transparency is seldom useable.

Pattern fills are available, however, the effective pattern is only 4X8 pixels. This may be useable where an 8X8 pattern is identical in the left and right halves.

Filled rectangles are available in two ways. First, where the desired fill color is the same in the high and low bytes (generally meaning all black or all white), rectangle fill can be used normally.

In the more general case of filling a rectangle with an arbitrary 16-bit color, the host should create a 4X8 pattern of the fill color and use pattern fills to create the rectangle.

Host I/O BITBLTs can operate normally be treating each 16-bit hi-color pixel as two adjacent, aligned 8-bit packed mode pixels.

Care should be used when implementing the use of one of the 16 bits in a hi-color pixel as a switch between false color and hi-color, since no mask exists to protect this flag bit during operations.

10.9 USE OF BITBLT FOR ARBITRARY SIZED PATTERNS

While the BITBLT hardware specifically accelerates 8X8 patterns, patterns of arbitrary size can be accelerated by use of the BITBLT, although to a lesser degree.

To copy an arbitrary size pattern to a destination region, the pattern should be stored in non-visible memory as a rectangular region, not a linear strip. With destination update enabled, one copy of the pattern should be BITBLT'ed to the top-left corner of the destination. The BITBLT source is then set to point to the pattern now in the destination region.

A series of BITBLTs are then performed, each doubling the width of the patterned area, simply by adjusting the X Dimensions register. (The last of this series of BITBLTs just fill out the destination region.)

A new series of BITBLTs is then performed, taking the horizontally complete pattern and doubling it in height each time. The destination update should be turned off, and the destination must be set for each new BITBLT. The final BITBLT will probably not be a double of the previous one since it just fills out the region.

10.10 PATTERNS BUILT ON-SCREEN

Normally, a pattern to be used in BITBLT is stored in a non-visible portion of display memory. This requires an aligned strip of 32 or 64 bytes to be available.

When this is not available, it may still be possible to perform a pattern BITBLT by placing the pattern in the last line of the destination region. This can be done if the raster operation is a source copy or source inversion, and if the destination region can accommodate the specified aligned strip on a single line. This technique is possible because each row of the pattern is read at the beginning of the row in which it is used, and the pattern is not overwritten until it after it has been read for the last time.

Where a full strip is unavailable, the destination can be broken up into a series of line-BLTs, with a one line pattern, requiring only 4 or 8 aligned bytes, placed on each destination line before the

BITBLT is started for that line. This method is substantially slower than other pattern BITBLTs.

A possible alternative is to write the pattern in a visible portion of memory, first saving the underlying area and restoring it after the BITBLT. This temporary usage of a visible region might be visible to the user. This might be reduced by using the last line of the destination and saving and restoring only those regions that overhang the destination.

10.11 USE OF PATTERNS IN TEXT MODE

Patterns may be in text mode to quickly set character and/or attribute bytes in a rectangular area to a common value. A pattern space must be created containing eight consecutive copies of the four-byte area consisting of the character, the attribute and two Font Map bytes, all aligned to a 64-pixel boundary. The BITBLT map mask is then used to protect the font maps. This pattern should be created in off-screen memory.

If an off-screen pattern space is not available, one may be created on screen by loading an aligned group of eight character/attribute pairs within the destination area, then pointing to that as the pattern source.

If the first character of the destination space happens to be on an 8-byte boundary (such as the conventional top of screen) then, as long as the destination is at least eight characters wide, only the first character/attribute pair must be loaded, and the BITBLT operation creates its own pattern as it goes along. This also works if the destination is less than eight characters wide, but is still wider than it is high.

If this is not possible, then the operation can be performed one character row at a time, loading the first character of each row to be used as an on-screen pattern.

Filled rectangles have a very limited application in text mode, but could be used to clear out a section of a font map or to set a section of a character or attribute map to all zeroes or all ones. Different values are not easily set in this manner because, in order to protect the font maps, planar mode, rather than packed mode, must be used.

10.12 SUPPORT FOR KANJI CHARACTERS

The BITBLT hardware can efficiently support generation of Kanji characters. The common implementation of Kanji characters calls for a character box of 28X28 pixels, with five possible scoring lines for each character box.

Kanji characters are best drawn in two passes. The first pass draws the characters while erasing any old ones. The second pass adds the score lines.

The Kanji font should be stored in non-visible display memory. Since the font is monochrome, multiple characters can be stored one per plane, one under the other. The color compare registers are used to switch between banks of characters stored on different planes.

A group of 32 special characters is generated along with the font, consisting of all possible combinations of scoring lines.

The dimension registers are loaded with the size of the character box. Foreground and background colors are set as desired. Destination update and quick BITBLTs are enabled.

For each character row, the source and destination registers are set to the beginning of the row, and monochrome expansion is enabled. A series of quick BITBLTs is performed, one per character, by loading the source address of each desired character. If a font-plane change is required, it is done before loading the source registers, which start the BITBLT automatically.

After the character row is complete, the destination registers are reset to the beginning of the row. Monochrome transparency is enabled, and a second pass is done over the character drawn to add score lines as needed, one special score-line character per Kanji character.

Where a Kanji character requires no score lines, either a BITBLT of a special "blank" score-line character is performed, or the destination registers may be updated to skip the position. The driver may add additional intelligence to skip entire character rows or parts where score lines are not required.

11.0 EGA MODE

11.1 EGA MODE ENTRY

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to section 7 for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register Bit 8. Select logic 0 for a VGA-compatible PS/2 display or logic 1 for an EGA-compatible TTL monitor by using the appropriate pull-up or pull-down resistor on MD(11). (A pull-up resistor on MD11 causes CNF(8) to be latched with logic 0 for analog PS/2 compatible displays.) This status information signifies the type of monitor attached to the system and is available to the BIOS or application.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 Bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on Pins MD(15:12). (A pull-up resistor causes logic 1 to be latched after power-on-reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O Port 3C2H Bit 4.
- If EGA mode is to be emulated on an IBM PS/2 analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force clock control rate of the CRT controller.
  - o Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional).
  - o Lock the PR registers PRO through PR5 and PR10 through PR17.
  - o Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - o Initialize all the registers.
  - o Set EGA TTL mode by programming:
    PR11(3)=0; EGA TTL
    PR14(7)=1; Enable IRQ
    PR15(6)=1; Set Low Clock
    PR14(7)=1; Enable IRQ
  - o Lock PR registers PRO through PR5 and PR10 through PR17.
  - o Read protect PR registers.

For more details on the PR registers, refer to the PR registers section 7.7. The EGA register summary shown on the next page highlight all the EGA mode registers.

REGISTERS	EGA	I/O PORT HEX
General Registers:		
Miscellaneous Output Register	WO	3C2
Input Status Register 0	RO	3C2
Input Status Register 1	RO	3?A
Feature Control Register	WO	3?A
Sequencer Registers:		
Sequencer Index Register	WO	3C4
Sequencer Data Register	WO	3C5
CRT Controller Registers:		
Index Register	WO	3?4
CRT Controller Data Register, except the following:	WO	3?5
Start Address High (Index=0CH)	RW	3?5
Start Address Low (Index=0DH)	RW	3?5
Cursor Location High (Index=0EH)	RW	3?5
Cursor Location Low (Index=0FH)	RW	3?5
Light Pen High, (Index=10H)	R	3?5
Light Pen Low, (Index=11H)	R	3?5
Graphics Controller Registers:		
Index Register	WO	3CE
Other Graphics Register	WO	3CF
Attribute Controller Registers:		
Index Register	WO	3CO*
Attribute Controller Data Register	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. ? = "B" in Monochrome modes or "D" in Color modes.
4. * = Identical responses from I/O Ports 3C0H and 3C1H.

TABLE 11-1. EGA REGISTERS SUMMARY

11.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are described. Their EGA mode bit definitions are provided.

11.2.1 Miscellaneous Output Register, Write Port = 3C2H

Bits (7:5) - EGA.

Same as Miscellaneous Output Register Bits (7:5) defined in the VGA section 7.1.1.

Bit 4

Reserved

Bits (3:2) - EGA, Clock Select 2:0.

00 = 14.318 Mhz clock (VCLK0) is selected.

01 = 16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.

10 = External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.

11 = Reserved. VCLK2 selected if Configuration Register Bit 3 is 0.

Bit 1

Reserved

Bit 0 - EGA, CRT Controller I/0 Address Range Selection

Same as Miscellaneous Output Register Bit 0 defined in the VGA section 7.1.1.

11.2.2 Input Status Register 0, Read Port = 3C2H

Bit 7 - EGA, CRT Vertical Retrace Interrupt Pending Or Cleared.

Same as input Status Register 0, Bit 7 defined in the VGA section 7.1.2.

Bits (6:5)

Reserved

Bit 4 - EGA.

The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0) - EGA.

Reserved, must be set to 1.

11.2.3 Input Status Register 1, Read Port = 3?AH

Bit 7 - EGA.

Reserved

Bit 6 - EGA.

Reserved, must be set to 1.

Bits (5:3) - EGA.

Same as Input Status Register 1 Bits (5:3) defined in the VGA section 7.1.3.

Bit 2 - EGA.

Reserved, must be set to 1.

Bit 1 - EGA.

Reserved

Bit 0 - EGA, Display Enable Status.

Same as Input Status Register 1 Bit 0 defined in the VGA section 7.1.3.

11.2.4 Feature Control Register, Write Port = 3?AH

Bits (7:0) - EGA.

Reserved

11.3 SEQUENCER REGISTERS, PORT = 3C5H

11.3.1 Clocking Mode Register, Read/Write Index = 01H

Bits (7:4) - EGA.

Reserved

Bits (3:2) - EGA.

Same as Clocking Mode Register Bits (3:2) defined in the VGA section 7.2.3.

Bit 1 - EGA.

Reserved, must be set to 0.

Bit 0 - EGA, 8/9 Dot Clock.

Same as Clocking Mode Register Bit 0 defined in the VGA section 7.2.3.

11.3.2 Character Map Select Register, Read/Write Index = 03H

Bits (7:4) - EGA.

Reserved

Bits (3:2) - EGA, Character Map Select A.

		Map Selected	Font Table/Plane 2 Location
00	=	0	1st 8 KByte
01	=	1	2nd 8 KByte
10	=	2	3rd 8 KByte
11	=	3	4th 8 KByte

Bits (1:0) - EGA, Character Map Select B.

		Map Selected	Font Table/Plane 2 Location
00	=	0	1st 8 KByte
01	=	1	2nd 8 KByte
10	=	2	3rd 8 KByte
11	=	3	4th 8 KByte

NOTE

Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

11.3.3 Memory Mode Register, Read/Wrte Index = 04H

Bits (7:3) EGA.

Reserved

Bits (2:1) - EGA.

Same as Memory Mode Register Bits (2:1) defined in the VGA section 7.2.6.

Bit 0 - EGA, Alpha Mode.

0 = Disables Alpha modes and enables non-Alpha modes.

1 = Alpha mode is active and character map selection is enabled.

11.4 CRT CONTROLLER REGISTERS, READ/WRITE PORT = 3?5H

Only the CRT Controller registers and the bit definitions that differ between the VGA and EGA are described. For similar registers and identical bits within registers refer to the VGA section 7.3. Also, "?" implies that a register is mapped into either 3B5H for Monochrome or 3D5H for Color display modes.

11.4.1 Index Register, Port = 3?4H

Bits (7:5) - EGA.

Reserved

Bits (4:0) - EGA.

These five bits point to the CRT Registers Address Index where the data is to be written.

11.4.2 Horizontal Total Register, Index = 00H

Bits (7:0) - EGA, Number Of Characters To Be Displayed Per Horizontal Line.

Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

11.4.3 End Horizontal Blanking Register, Index = 03H

Bit 7 - EGA.

Reserved

Bits (6:5) - EGA, Display Enable Skew.

These bits define display enable skew in character clocks.

00 = 0 Skew

01 = 1 Skew

10 = 2 Skew

11 = 3 Skew

Bits (4:0) - EGA, End Horizontal Blanking.

These five bits of the character count determine when the horizontal blanking ends.

11.4.4 End Horizontal Retrace Register, Index = 05H

Bit 7 - EGA.

This bit defines the start of the odd or even CRT counter memory address following the horizontal retrace time.

0 = Even Address.

1 = Odd Address.

Bits (6:0) - EGA.

Same as End Horizontal Retrace Registers Bits (6:0) defined in VGA section 7.3.7.

11.4.5 Vertical Total Register, Index = 06H

Bits (7:0) - EGA.

This register contains the least significant eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

11.4.6 CRT Controller Overflow Register, Index = 08H

Bits (7:5) - EGA.

Reserved

Bits (4:0) - EGA.

Same as CRT Controller Overflow Register Bits (4:0) definitions in the VGA section 7.3.9.

11.4.7 Maximum Scan Line Register, Index = 09H

Bits (7:5) - EGA.

Reserved

Bits (4:0) - EGA, Maximum Scan Line.

Same as Maximum Scan Line Register Bits (4:0) defined in the VGA section 7.3.11.

11.4.8 Cursor Start Register, Index = 0AH

Bits (7:5) - EGA

Reserved

Bits (4:0) - EGA, Cursor Start Scan Line.

Same as Cursor Start Register Bits (4:0) defined in the VGA section 7.3.12.

11.4.9 Cursor End Register, Index = 0BH

Bit 7 - EGA.

Reserved

Bits (6:5) - EGA, Cursor Skew Bits.

These bits define cursor signal skew in character clocks.

00 = 0 Skew

01 = 1 Skew

10 = 2 Skew

11 = 3 Skew

Bits (4:0) - EGA, Cursor End Scan Line.

These bits specify the Cursor End value of the last row scan address counter. The programmed value is equal to N+1 where N is the last row of the Cursor to be displayed.

11.4.10 Vertical Retrace Start Register, Write Index = 10H

(Light Pen High register, Index = 10H - Read)

Bits (7:0) - EGA.

Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

11.4.11 Vertical Retrace End Register, Write Index = 11H

(Light Pen Low register, Index = 11H - Read)

Bits (7:6) - EGA.

Reserved

Bit 5 - EGA, IRQ Output Buffer.

0 = The IRQ output buffer control is enabled. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal.

1 = The IRQ output buffer is switched to a high impedance state.

Bit 4 - EGA, IRQ Latch.

0 = The IRQ latch is reset and cleared to 0 if Bit 5 = 0.

1 = The IRQ latch gets set at the end of the vertical display.

Bits (3:0) - EGA, Vertical Retrace End.

Same as Vertical Retrace End Register Bits (3:0) defined in the VGA section 7.3.19.

11.4.12 Underline Location Register, Index = 14H

Bits (7:5) - EGA.

Reserved

Bits (4:0) - EGA, Underline Location.

These bit determine the Horizontal Scan Row where the underline will be displayed. The value programmed is one less than the scan line desired.

11.4.13 End Vertical Blanking Register, Index = 16H

Bits (7:5) - EGA.

Reserved

Bits (4:0) - EGA, End Vertical Blanking.

Same as End Vertical Blanking Register Bits (4:0) defined in the VGA section 7.3.24.

11.4.14 Mode Control Register, Index = 17H

Bits (7:5) - EGA.

Same as CRT Mode Control Register Bits (7:5) defined in the VGA section 7.3.25.

Bit 4 - EGA.

Reserved

Bits (3:0) - EGA.

Same as Mode Control Register Bits (3:0) defined in the VGA section 7.3.25.

11.5 GRAPHICS CONTROLLER REGISTERS, PORT = 3CFH

11.5.1 Read Map Select Register, Read/Write Index = 04H

Bits (7:3) - EGA.

Reserved

Bits (2:0) - EGA, Map Select.

These bits represent the encoded value of the memory plane selected.

000 = Map 0 selected.

001 = Map 1 selected.

010 = Map 2 selected.

011 = Map 3 selected.

11.5.2 Mode Register, Index = 05H

Bit (7:6) - EGA.

Reserved

Bits (5:2) - EGA.

Same as Graphics Mode Register Bits (5:2) defined in the VGA section 7.4.7.

Bits (1:0) - EGA, Write Mode.

These bits select the Write Mode.

00 = Write mode 0 - Refer to VGA Table 7.6.

01 = Write mode 1 - Refer to VGA Table 7.6.

10 = Write mode 2 - Refer to VGA Table 7.6.

11 = Write mode 3 - Not Legal. Selects write mode 1.

11.6 ATTRIBUTE CONTROLLER REGISTERS, PORTS = 3C0H/3C1H

11.6.1 Palette Registers, Read Port = 3C1H, Write Port = 3C0H, Index = 00H - 0FH

Bits (7:6) - EGA.

Reserved

Bits (5:0) - EGA, Dynamic color selection.

Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection.

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

11.6.2 Attribute Mode Control Register, Read Port = 3C1H, Write Port = 3C0H, Index = 10H

Bits (7:4) - EGA.

Reserved

Bits (3:0) - EGA.

Same as Mode Control Register Bits (3:0) defined in the VGA section 7.5.3.

11.6.3 Overscan Color Register, Read Port = 3C1H, Write Port = 3C0H, Index = 11H

Bits (7:6) - EGA.

Reserved

Bits (5:0) - EGA, Overscan Color For Border

For a monochrome display, Bits 5:0 = 0.
The border color is defined by the color table for the Palette registers shown in section 12.6.1.

11.6.4 Color Plane Enable Register, Read Port = 3C1H, Write Port = 3C0H, Index = 12H

BIT	FUNCTION
7:6	Same as Color Plane Enable - VGA (Reserved)
5:4	Video Status Multiplexer
3:0	Same as Color Plane Enable - VGA

Bits (7:6) - EGA

Same as Color Plane Enable Register Bits (7:6) in the VGA section 7.5.5 (Reserved).

Bits (5:4) - EGA, Video Status Multiplexer.

These bits select two out of six colors which can be read by the Input Status Register 1 (Video Status Multiplexer) at Port 3?AH, Bits 5 and 4.

COLOR PLANE		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID 2 (Red)	VID 0 (Blue)
0	1	VID 5 (SRed)	VID 4 (SGreen)
1	0	VID 3 (SBlue)	VID 1 (Green)
1	1	VID 5 (SRed)	VID 4 (SGreen)

Bits (3:0) - EGA

Same as Color Plane Enable Register Bits (3:0) defined in the VGA section 7.5.5.

11.6.5 Horizontal PEL Panning Register, Read Port = 3C1H, Write Port = 3C0H, Index = 13H

BIT	FUNCTION
7:4	Reserved.
3:0	Horizontal left shift of the video data in number of pixels.

Bits (7:4) - EGA

Reserved

Bits (3:0) - EGA, Horizontal Pixel Panning.

These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alphanumeric modes, (nine dots/character) image can be shifted by nine pixels. For all other graphics or alphanumeric modes, a maximum left shift of eight pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section 7.5.6..

12.0 WD90C31 INTERFACES

The WD90C31 applications section is divided into various interfaces: processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes and technical briefs at the end of this document will supplement the information provided in this section.

Figure 12-1 highlights the WD90C31 interfaces.

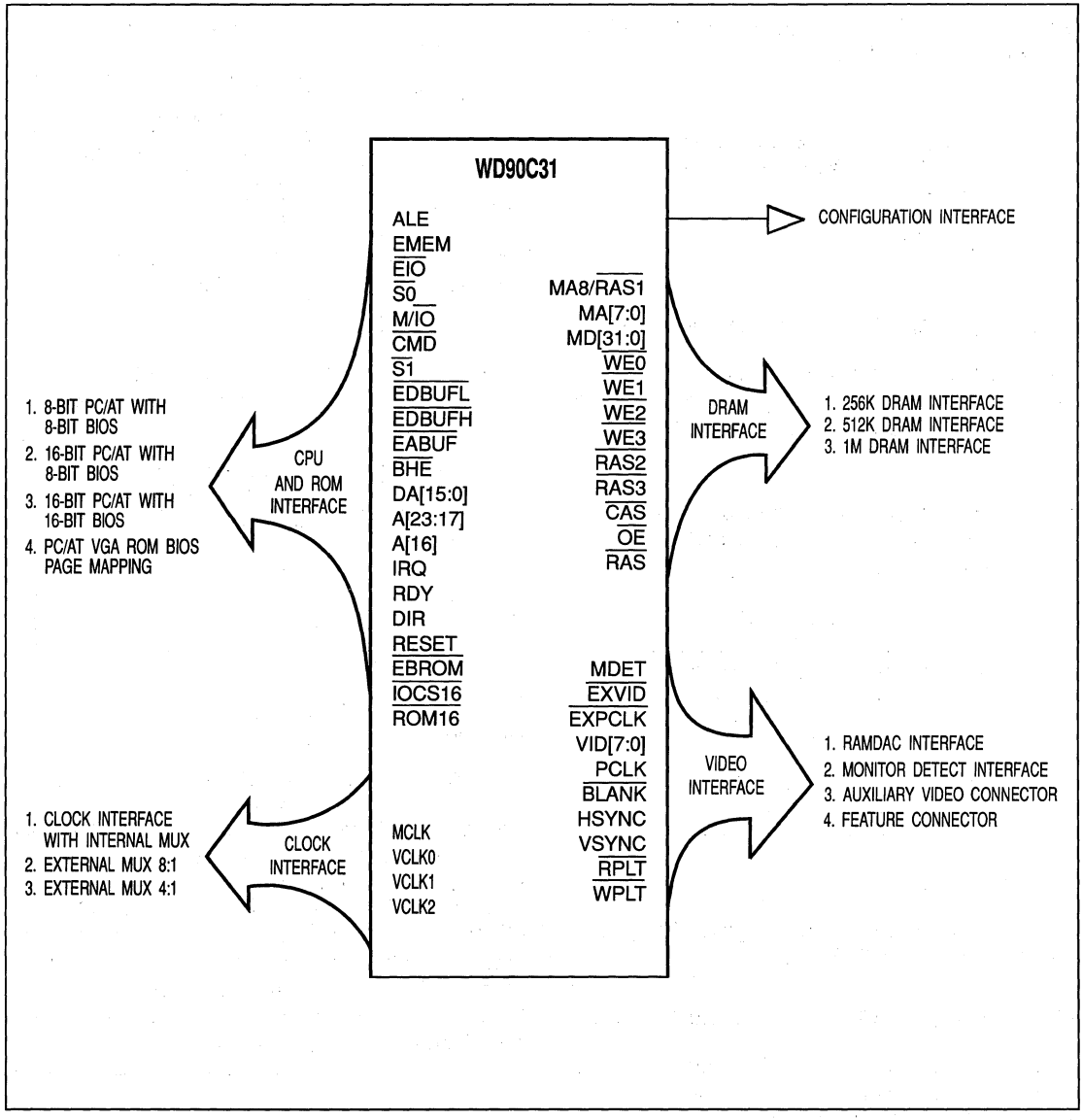

FIGURE 12-1. WD90C31 INTERFACES

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12.1 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 12-2 shows a block diagram of the WD90C31 with eight-bit PC/AT interface using eight-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

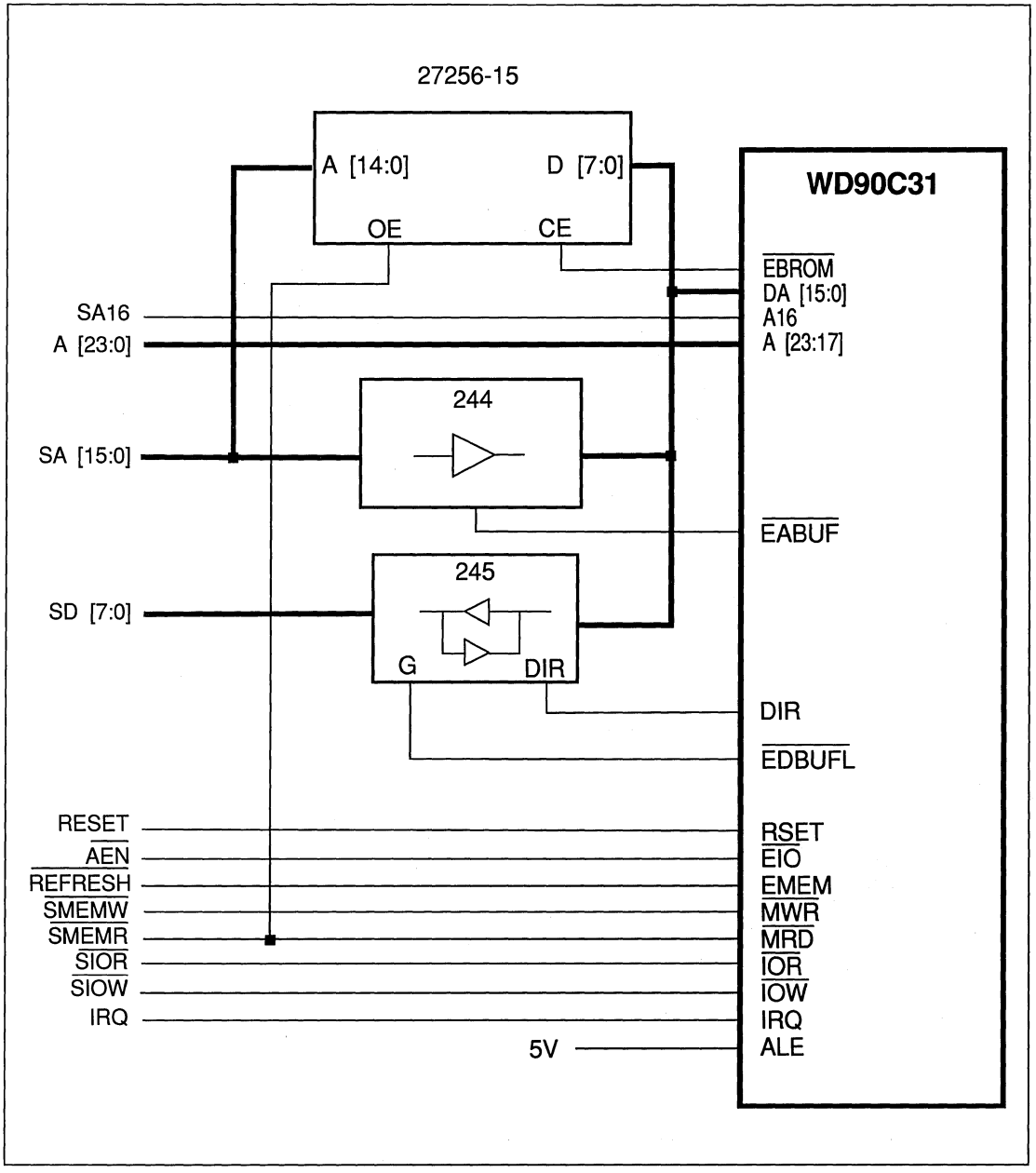


FIGURE 12-2. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

12.2 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 12-3 illustrates 16-bit PC/AT interface with an eight-bit BIOS using WD90C31. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown.

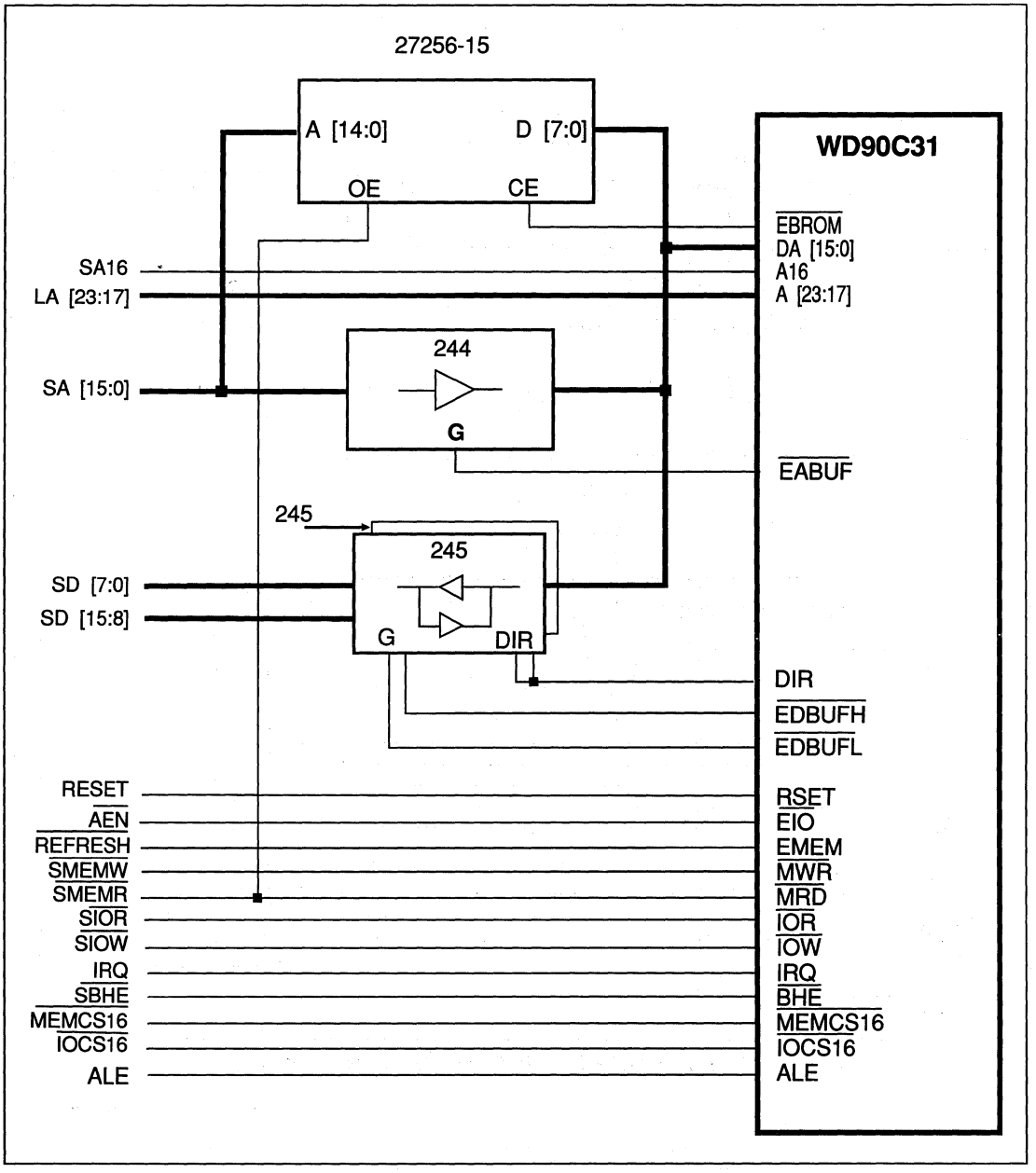


FIGURE 12-3. 16-BIT PC AT INTERFACE WITH 8-BIT BIOS

12.3 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

Figure 12-4 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C31. The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds since SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 12-6 for 286-based systems.

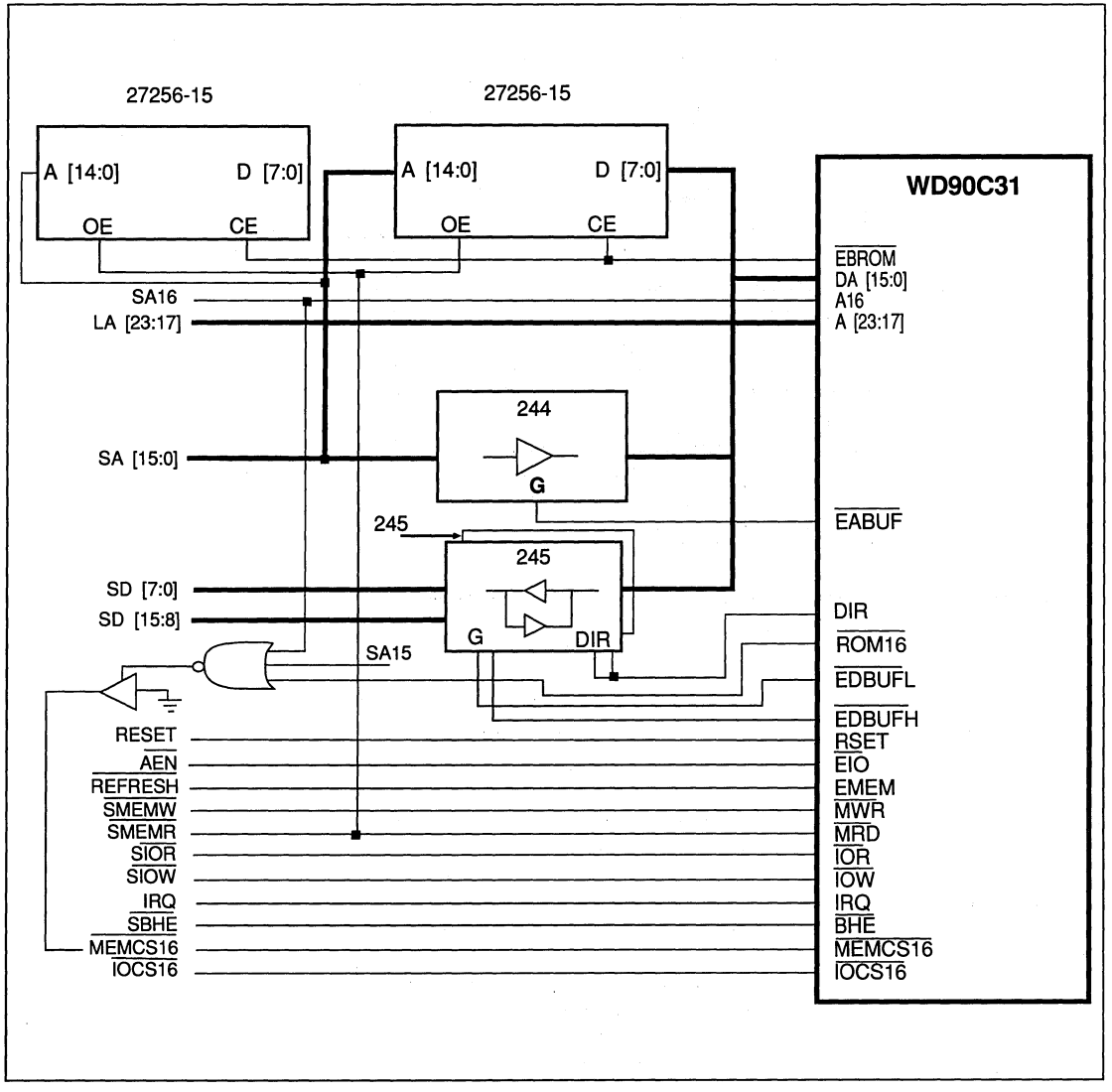


FIGURE 12-4. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS

12.4 16-BIT MICRO CHANNEL

Figure 12-5 illustrates the WD90C31 and 16-bit Micro Channel interface. 3C3.D0 is output of Port 3C3H Bit 0 VGA Subsystem Enable Register.

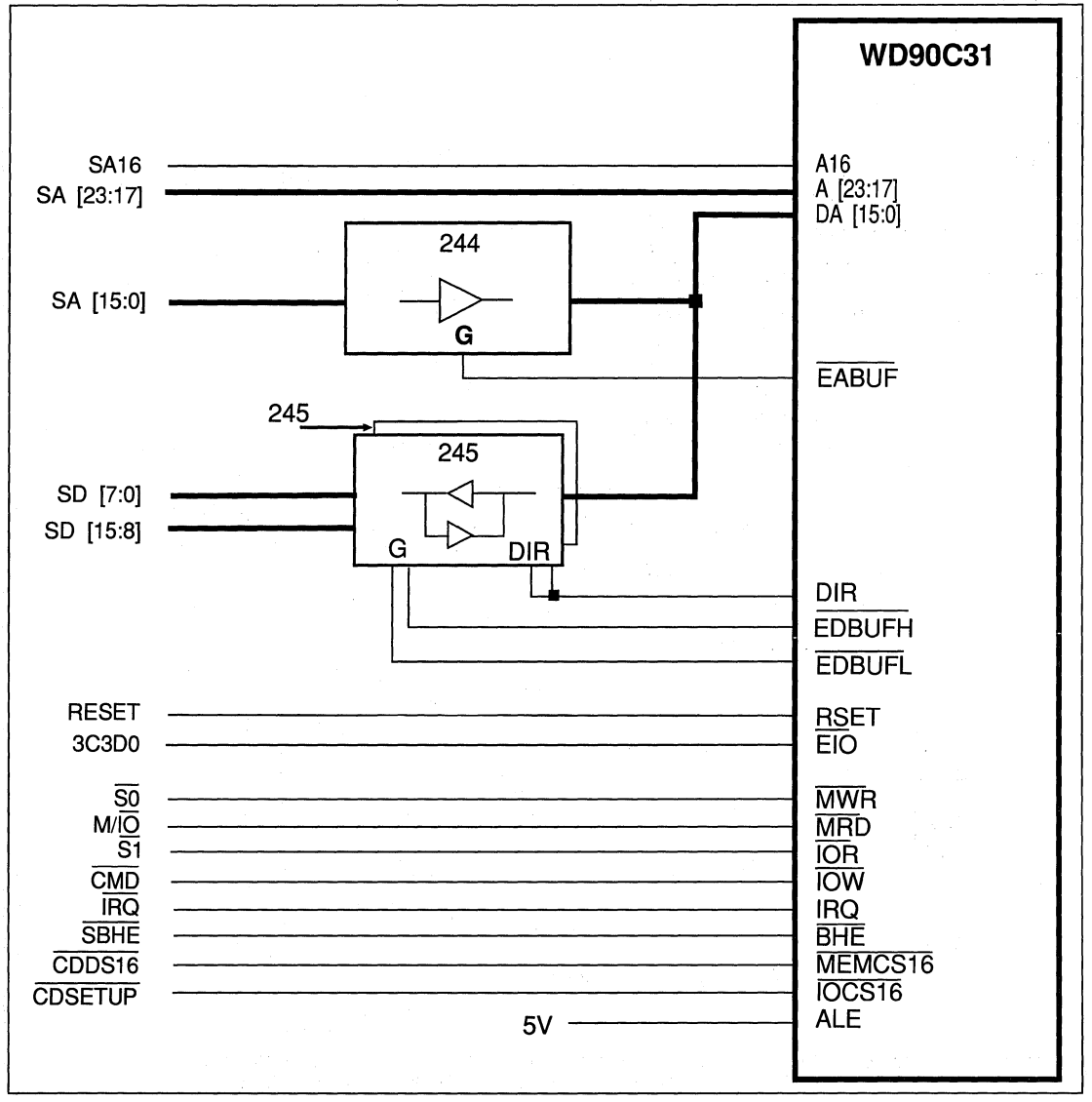
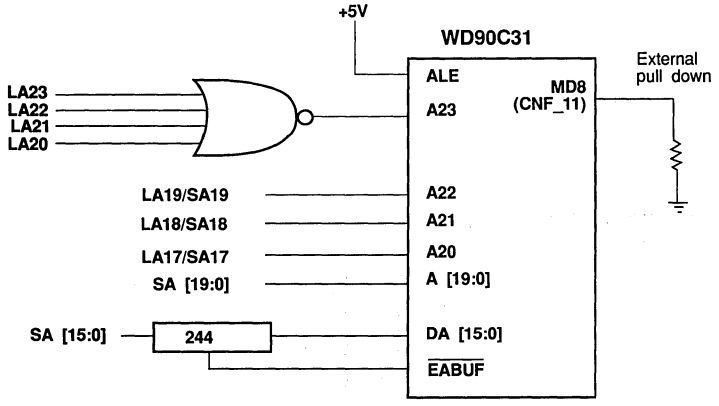


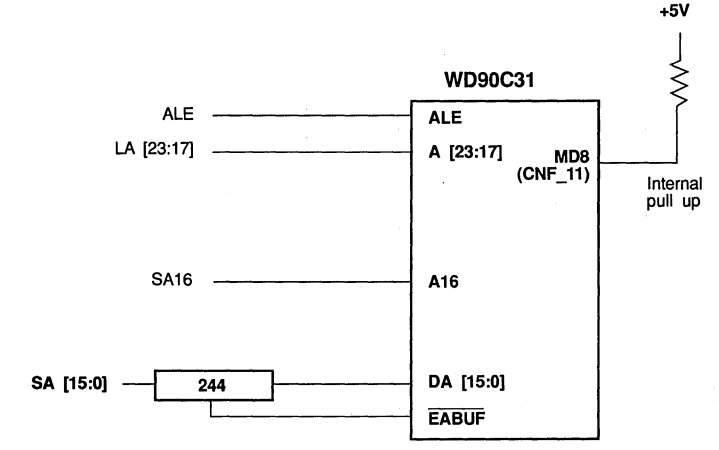
FIGURE 12-5. 16-BIT MICRO CHANNEL INTERFACE

12.5 WD90C31 INTERFACE FOR 286 OR 386 BASED SYSTEMS

For systems that do not meet the hold time of LA address valid from the falling edge of MEMR or MEMW, pull MD8 down and connect LA addresses and SA addresses as shown in the upper half of Figure 12-6. This applies to most 286 systems. Otherwise, connect LA addresses and SA addresses as shown in the lower half of Figure 12-6. This applies to most 386 systems.



Note: MD8 (CNF_11 is pulled down at power-on-reset. This configuration is recommended for interfacing with 8-bit and 16-bit AT buses. For an 8-bit interface, A23 should be connected to SA [19:17] on the AT bus. For a 16-bit interface, LA [23:17] must be connected to generate MEMCS16.



Note: MD8 (CNF_11) is pulled up internally at power-on-reset. This configuration is recommended for interface with a 16-bit AT bus only. LA {23:17] is internally latched by ALE.

FIGURE 12-6. WD90C31 INTERFACE FOR 286 OR 386-BASED SYSTEMS

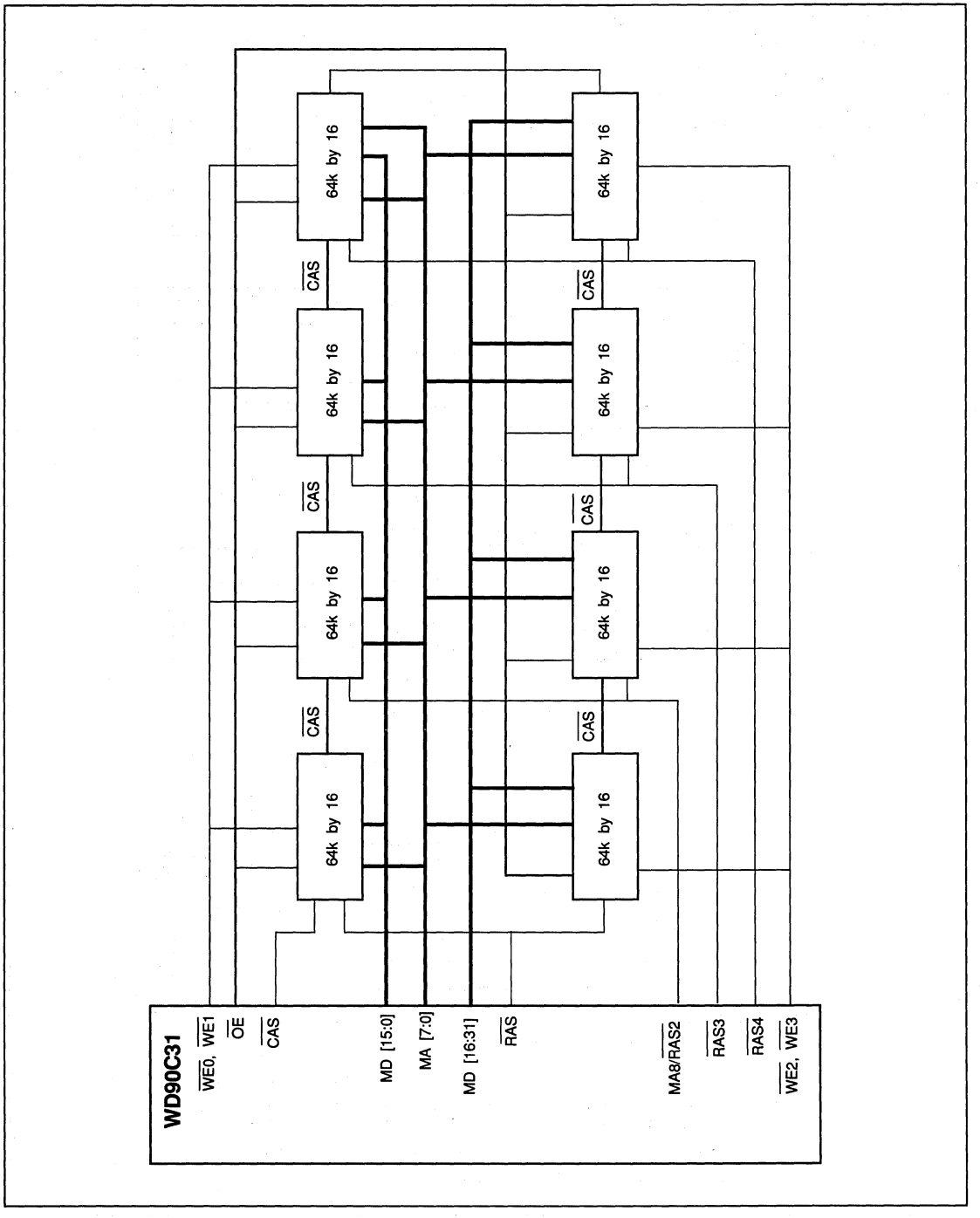
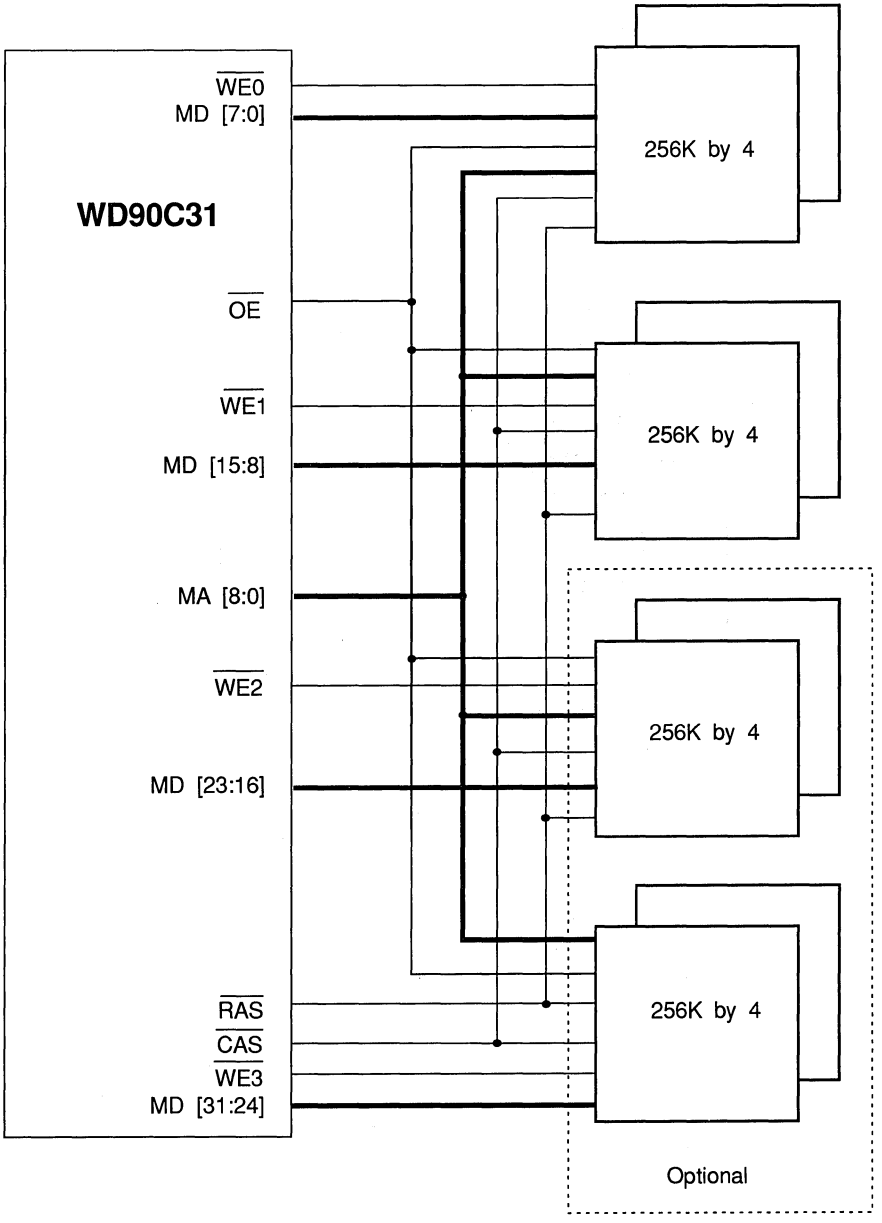


FIGURE 12-7. TWO, FOUR OR EIGHT 64K BY 16 DRAM INTERFACE



Note: Only MD [15:0] will be used if four 25K by 4 DRAMs are installed.

FIGURE 12-8. FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

12.6 WD90C31 WITH RAMDAC INTERFACE

Figure 12-9 illustrates the WD90C31 and RAMDAC (WD90C50) interface block diagram for analog monitors.

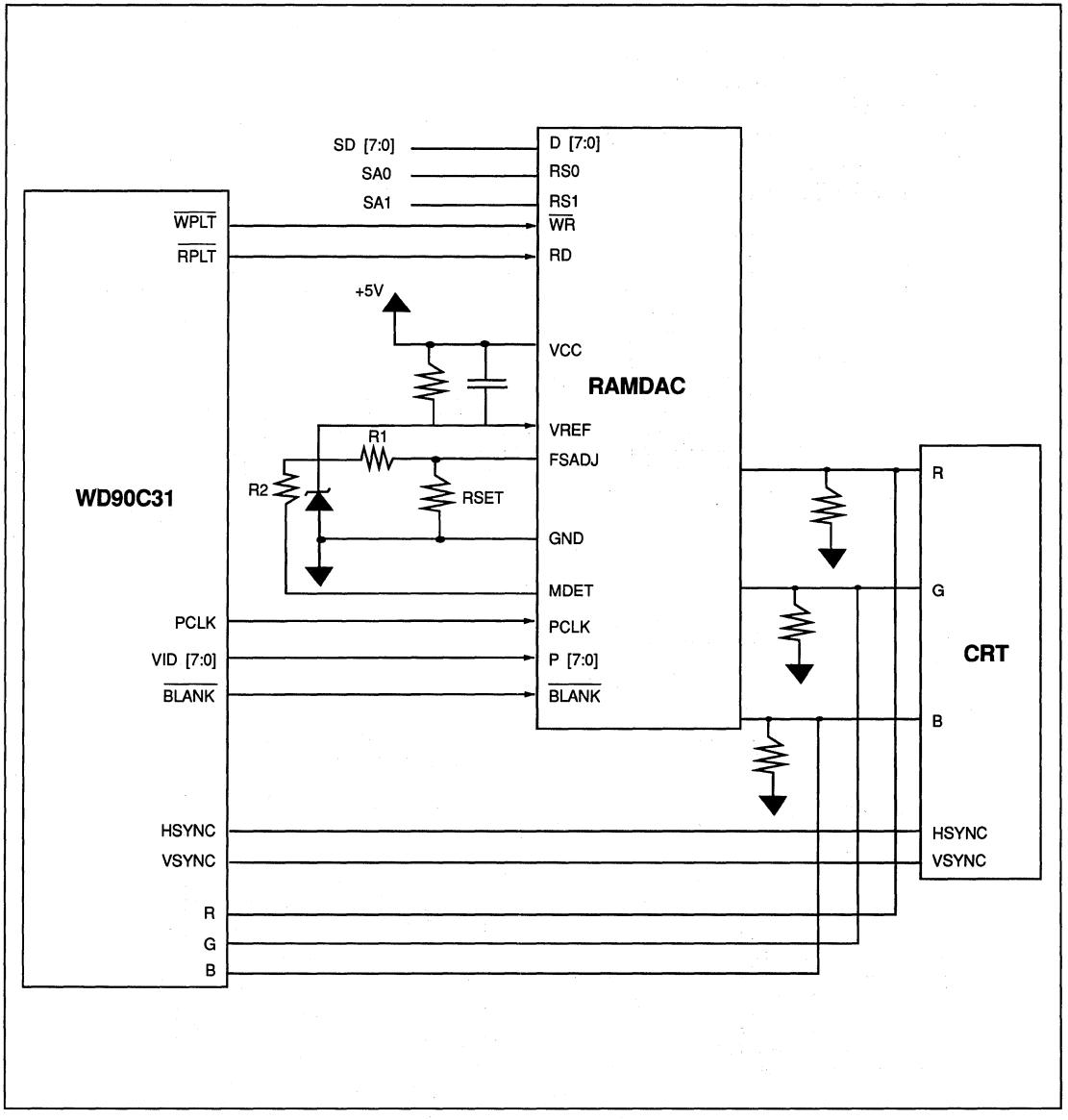


FIGURE 12-9. WD90C31 WITH RAMDAC INTERFACE

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12.7 WD90C31 AND TTL MONITOR CONNECTIONS

Figure 12-10 illustrates the WD90C31 and TTL monitor connections

NOTE:

- VGA/TTL switch may be used to disable HSYNC and VSYNC for analog or TTL Video connector.
- MD(15:12) may also be connected as the EGA switches if desired. See PR Register and Pinout sections for more detail.
- For AT applications using the WD90C31, install the IRQ9 resistor.
- Transistor 2N2222A is used to emulate a monochrome and color display connection.

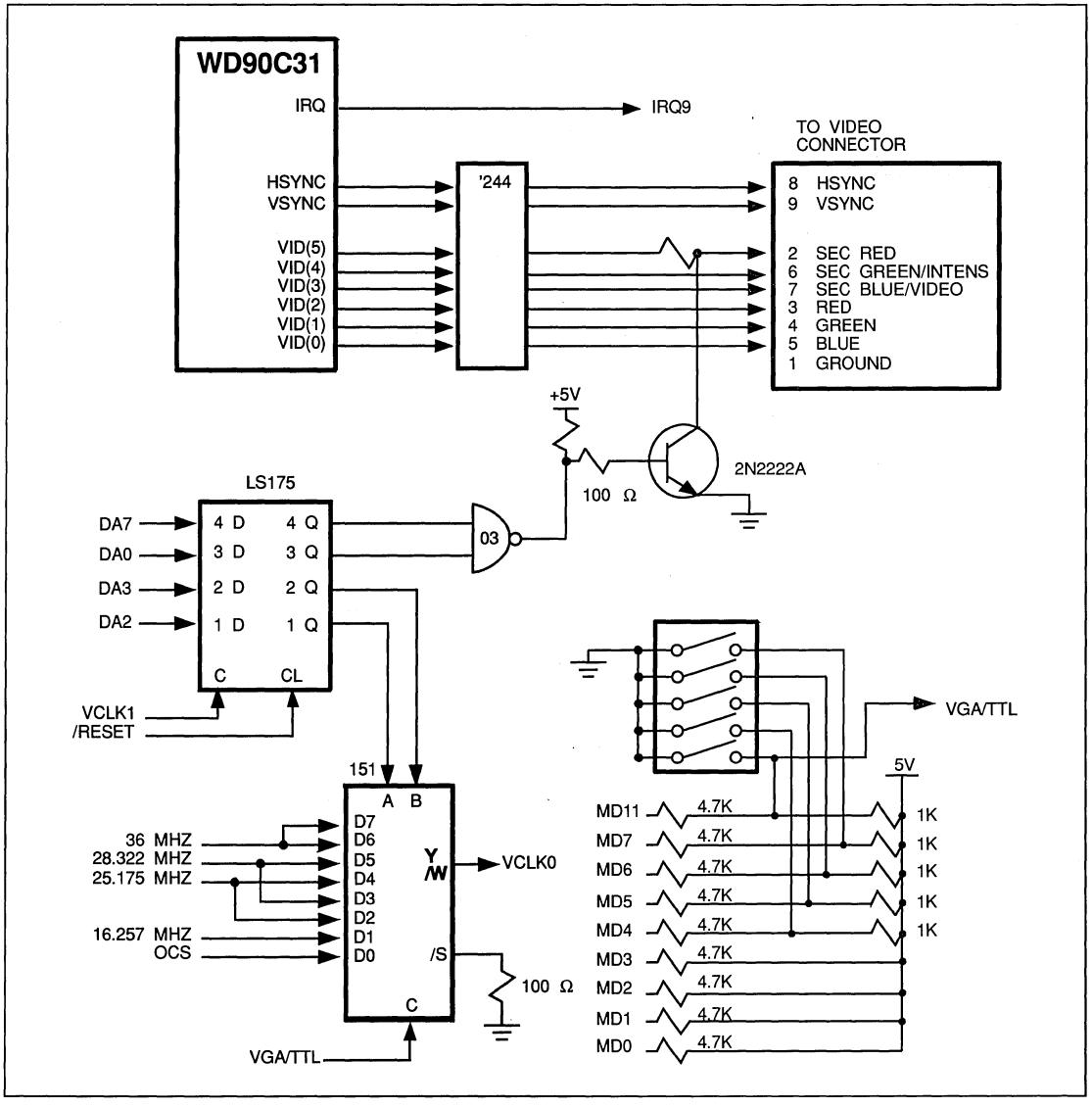

FIGURE 12-10. WD90C31 AND TTL MONITOR CONNECTIONS

12.8 CLOCK INTERFACE

Figure 12-11 illustrates the WD90C31 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H Bit 3 and Bit 2 and is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C31 signal pins (VCLK1, VCLK2) inputs.

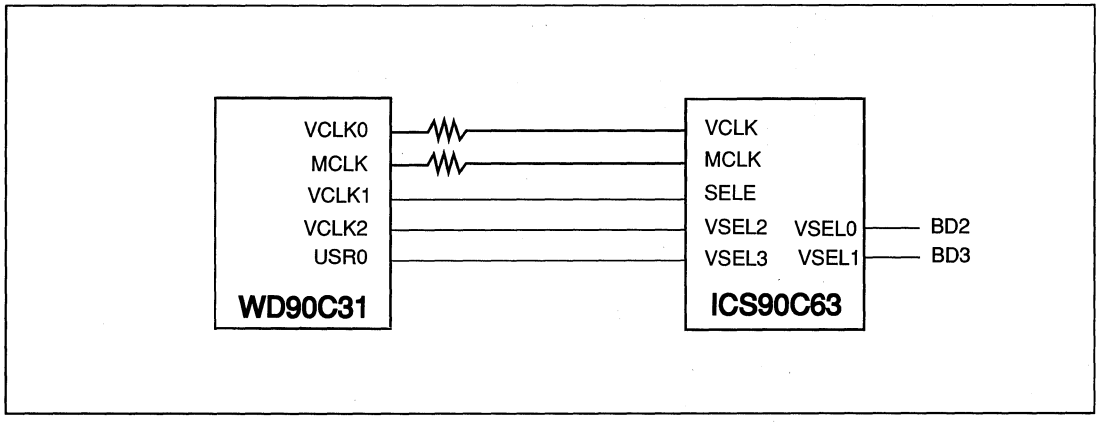

FIGURE 12-11. CLOCK INTERFACE

13.0 SHADOW REGISTER IMPLEMENTATION

The Shadow Register has been implemented on some of the CRTC registers. The purpose of using the shadow register is to have one CRTC register that is writable and readable all the time by application programs without actually changing CRTC timing. The actual CRTC timing registers are initialized and locked while using the shadow register for compatibility.

Registers are added to the following CRTC registers. The shadowed registers can be locked by writing "XXXXX101" to PR1A(3?5.3D). This lock overrides any other locks. Then by setting PR1A Bit 3 = 1, this will select the shadow register for read.

HORIZONTAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.00	7:0	Group 0	Horizontal Total
3?5.02	7:0	Group 0	Start Horizontal Blanking
3?5.03	4:0	Group 0	End Horizontal Blanking
3?5.05	7	Group 0	Bit 6 of EHB
3?5.04	7:0	Group 0	Start Horizontal Retrace
3?5.05	4:0	Group 0	End Horizontal Retrace
3?5.03	6:5	Group 0	Display Enable Skew
3?5.05	6:5	Group 0	Horizontal Retrace Skew
VERTICAL TIMING			
ADDRESS	**BITS**	**LOCK**	**DESCRIPTION**
3?5.06	7:0	Group 2	Vertical Total
3?5.07	5,0	Group 2	Bits 9, 8 of VT
3?5.10	7:0	Group 3	Vertical Retrace Start
3?5.07	7,2	Group 2	Bits 9, 8 of VRS
3?5.11	3:0	Group 3	Vertical Retrace Start
3?5.15	7:0	Group 3	Start Vertical Blank
3?5.07	3	Group 2	Bit 8 of SVB
3?5.09	5	Group 2	Bit 9 of SVB
3?5.16	7:0	Group 3	End Vertical Blank

Note:
Group 0: Registers will be locked if PR3(5) = 1 or 3?5.11 bit 7 = 1
Group 2: Registers will be locked if PR3(0) = 1 or 3?5.11 bit 7 = 1
Group 3: Registers will be locked if PR3(0) = 1
Group 0, 2, 3 registers listed above will be locked if PR1A = "xxxxx101", regardless of the contents of PR3.
The Horizontal Display End and the Vertical Display End registers are not shadowed.

TABLE 13-1. SHADOW REGISTER IMPLEMENTATION

14.0 SIGNATURE ANALYZER

A signature analyzer was designed for use in the WD90C31. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

14.1 DESCRIPTION

The basis of the signature analyzer is a Linear Feedback Shift Register (LFSR). The inputs to the LFSR tap onto the VID[0:7] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately $1/2^n$, where n is the length of the shift register. A 16-bit signature register is used on the WD90C31. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$) has been implemented on the WD90C31. It was modified for multiple inputs as shown in the block diagram.

14.2 OPERATION

The signature analyzer was designed to collect signature of the VID[0:7] outputs over one vertical frame. The signal path of the VID[0:7] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3F). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 Bits 2 through 0. PR10 also serves as the lock for other registers.

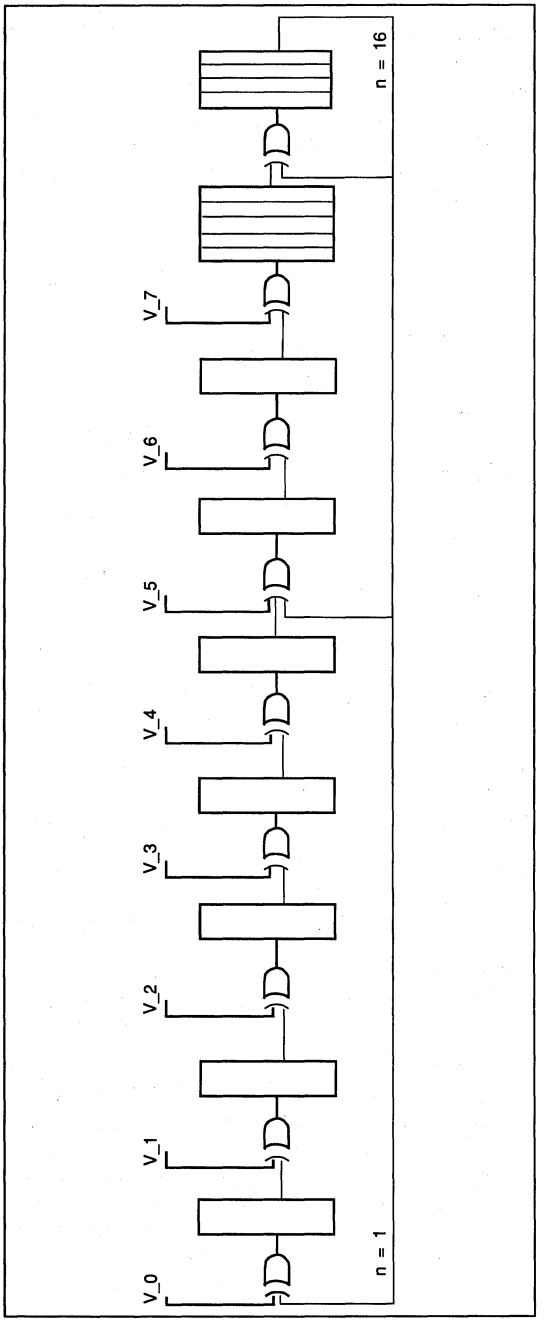

FIGURE 14-1. LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/WRITE	DESCRIPTION
0	Start/status	R/W	Writing "1" to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. 1: Busy 0: Finished or not enabled
1	Clear	R/W	Writing "0" to this bit position preloads the LFSR with 0001H. This bit must be set to operate the signaure analyzer. 1: Normal operation 0: Preload LFSR
2	Disable Video input	R/W	This bit is used in a self-test mode. A fixed signature will be generated for any given mode (independent of video memory data). 1: Disable video inputs 0: Enable video inputs
3	Lock Read Port	R/W	This bit must be set in order to read the signature and status. 1: Enable read of LFSR (addresses 3?5.20 and 3?5.21). 0: Disable reads of LFSR

TABLE 14-1. CONTROL REGISTER PR19

The following programming steps highlight the sequence that will setup, check, and read the signature.

Step 1) 85H-> 3?5.29; release control register (PR10) read and write lock

Step 2) 00H-> 3?5.3F; clear signaure analyzer

Step 3) 03H-> 3?5.3F; enable signature analyzer to collect signature

Step 4) read 3?5.3F; check status for busy
if LSB = 1 repeat step 4
if LSB = 0 signature is collected, proceed to step 5

Step 5) OAH-> 3?5.3F; enable signature analyzer read port

Step 6) read 3?5.20; read low byte of signature

Step 7) read 3?5.21; read high byte of signature

Step 8) 00H-> 3?5.3F; clear signaure analyzer and lock read port.

15.0 I/O MAPPING

15.1 INTRODUCTION

The I/O Mapping was designed for use in the WD90C31 to isolate board level solder defects. The I/O Mapping allows the IC to enter a test mode where all of pins in the IC are divided into various groups as inputs and output. The path from PCB trace through inputs, IC, output and PCB trace can be treated as a simple path. With test points on board, test for opens and shorts can be performed quickly.

15.2 TEST MODE

There are four requirements to meet for the WD90C31 to enter the I/O mapping test mode .

- $\overline{\text{MWR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CONFIGURATION SWITCH 2 is HIGH (MD2 is pulled high)
- RESET is HIGH

If both $\overline{\text{MWR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in AT machines and a reserved condition in the PS/2 machines. Configuration switch 2 high will ensure that WD90C31 is in AT mode. Reset controls a transparent latch as shown in Figure 15-1. Reset can be dopped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

15.3 PIN GROUPINGS

The following pin groupings are done to minimize routing overhead of I/O pin mapping. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the pin name that corresponds to the input pin(s).

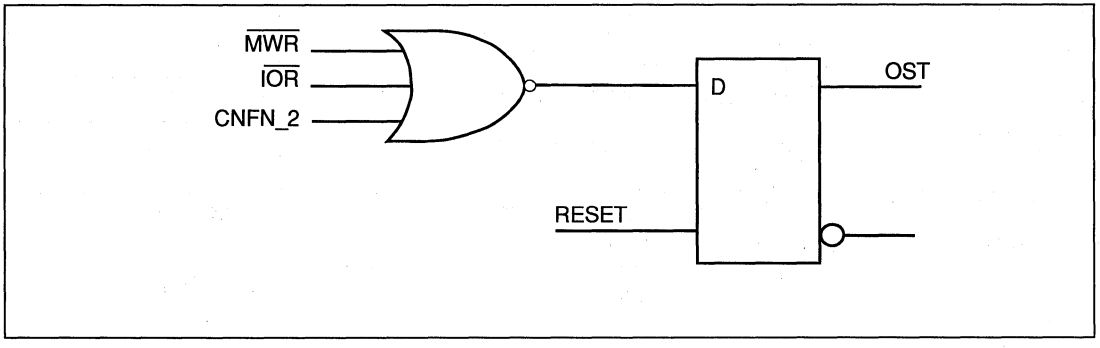

FIGURE 15-1. TEST MODE CIRCUIT

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P1	MDET	P123	VID4
P4	MCLK	P124	VID5
P8	MD31	P125	VID6
P9	MD30	P126	VID7
P10 + P13	MD29 + MD26	P2	USR1
P11 + P14	MD28 + MD25	P3	USR0
P12	MD27	P7	$\overline{WE3}$
P15	MD24	P6	$\overline{OE}$
P19 + P24 + P31	MD23 + MD18 + MD15	P27	$\overline{RAS4}$
P20	MD22	P16	$\overline{WE2}$
P21 + P25 + P32	MD21 + MD17 + MD14	P28	$\overline{RAS3}$
P22 + P26 + P33	MD20 + MD16 + MD13	P30	$\overline{WE1}$
P23 + P34 + P43	MD19 + MD12 + MD6	P39	$\overline{RAS}$
P35 + P38	MD11 + MD8	P52	$\overline{WE0}$
P36 + P41	MD10 + $\overline{CAS}$	P53	MA0
P37 + P42 +P46	MD9 + MD7 + MD3	P54	MA1
P44 + P47	MD5 + MD2	P55	MA2
P45 + P49	MD4 + MD0	P56	MA3
P48 + P62	MD1 + A17	P57	MA4
P63 + P68	A18 + A22	P59	MA6
P64 + P69 + P72	A19 + A23 + $\overline{BHE}$	P58	MA5
P65	A20	P60	MA7
P66 + P73 + P86	A21 + ALE + $\overline{ROM16}$	P61	MA8
P70 + P77 + P80	$\overline{IOCS16}$ + $\overline{IOW}$ + RESET	P74	IRQ
P90 + P93 + P95 P79 + P89	DA15 + DA12 + DA10 + $\overline{MWR}$ + A16	P71	$\overline{MEMCS16}$
P75 + P78 + P88	EMEM + $\overline{MRD}$ + $\overline{EDBUFH}$	P82	IOCHRDY

TABLE 15-1. WD90C31 PIN SCAN MAP FOR 132-PIN PACKAGE

INPUT PINS		OUTPUT PINS	
PIN	NAME	PIN	NAME
P85 + P92	$\overline{EIO}$ + DA13	P81	$\overline{0WS}$
P91 + P94	DA14 + DA11	P87	$\overline{EBROM}$
P76 + P77	$\overline{IOR}$ + $\overline{IOW}$	P100	DIR**
P96 + P101	DA9 + DA7	P115	$\overline{RPLT}$
P97 + P102	DA8 + DA6	P114	$\overline{WPLT}$
P98 + P103	$\overline{EABUF}$ + DA5	P113	$\overline{HTL}$
P104 + P109	DA4 + $\overline{EDBUFL}$	P112	$\overline{BLANK}$
P105 + P107	DA3 + DA1	P110	VSYNC
P106 + P108	DA2 + DA0	P111	HSYNC
P128	VCLK0	P118	PLCK
P129	VCLK1	P119	VID0
P130	VCLK2	P120	VID1
P131	$\overline{EXPCLK}$	P121	VID2
P132	$\overline{EXVID}$	P122	VID3
Note: A "+" in the input column indicates an OR function for the test input pins only. ** This mapping for DIR output is valid only during RESET HIGH.			

TABLE 15-1. WD90C31 PIN SCAN MAP FOR 132-PIN PACKAGE (Cont.)

Refer to Table 4-3 for the comparable pin number for a 144-pin package.

18

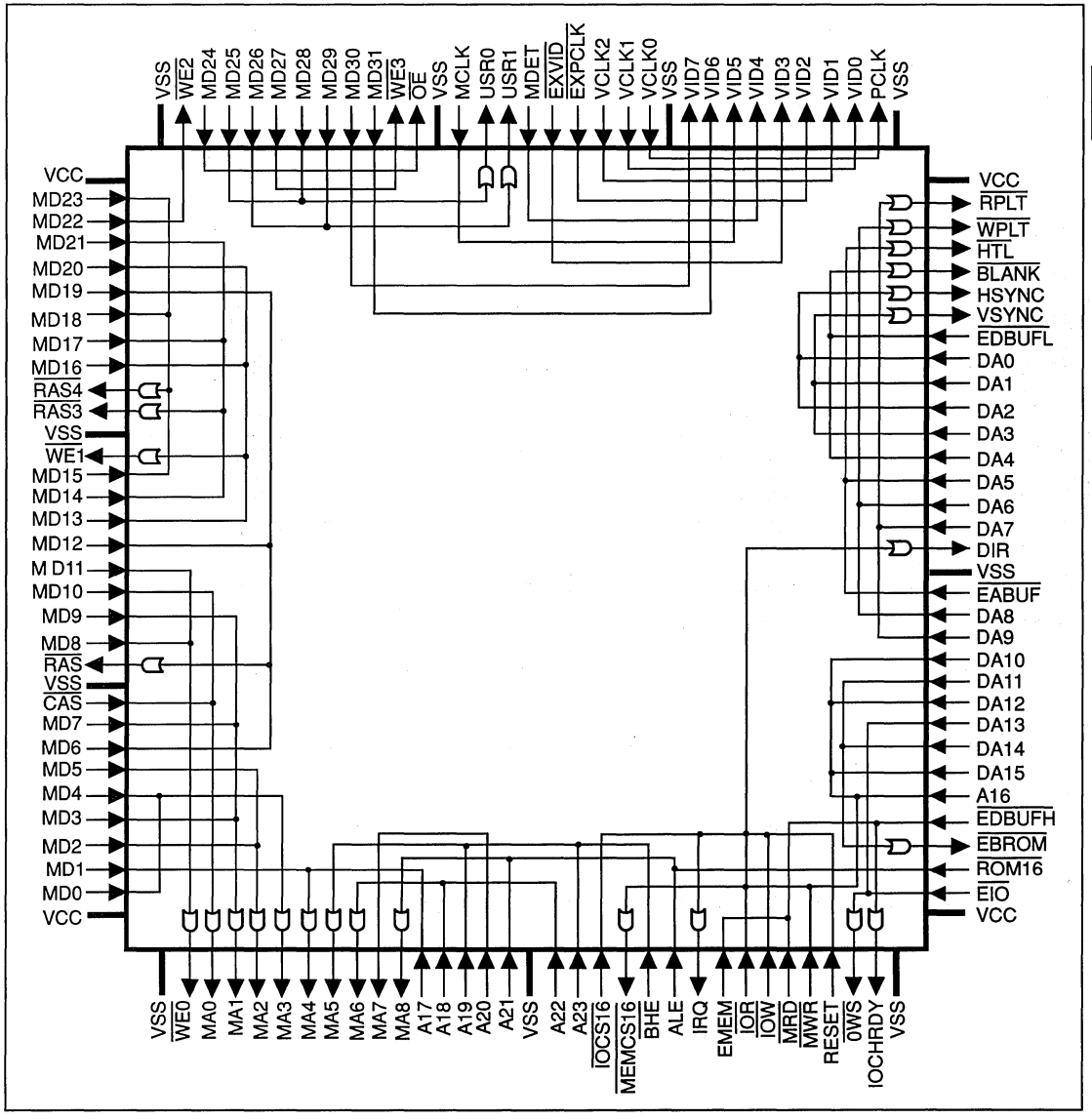

FIGURE 15-2. WD90C31 PIN SCAN MAP FOR A 132-PIN PACKAGE

16 .0 PACKAGE DIMENSIONS

Figure 16-1 illustrates the 132-pin JEDEC package showing the dimensions in inches. Figure 16-2 illustraes the 144-pin EIAJ package showing the dimensions in millimeteres and inches.

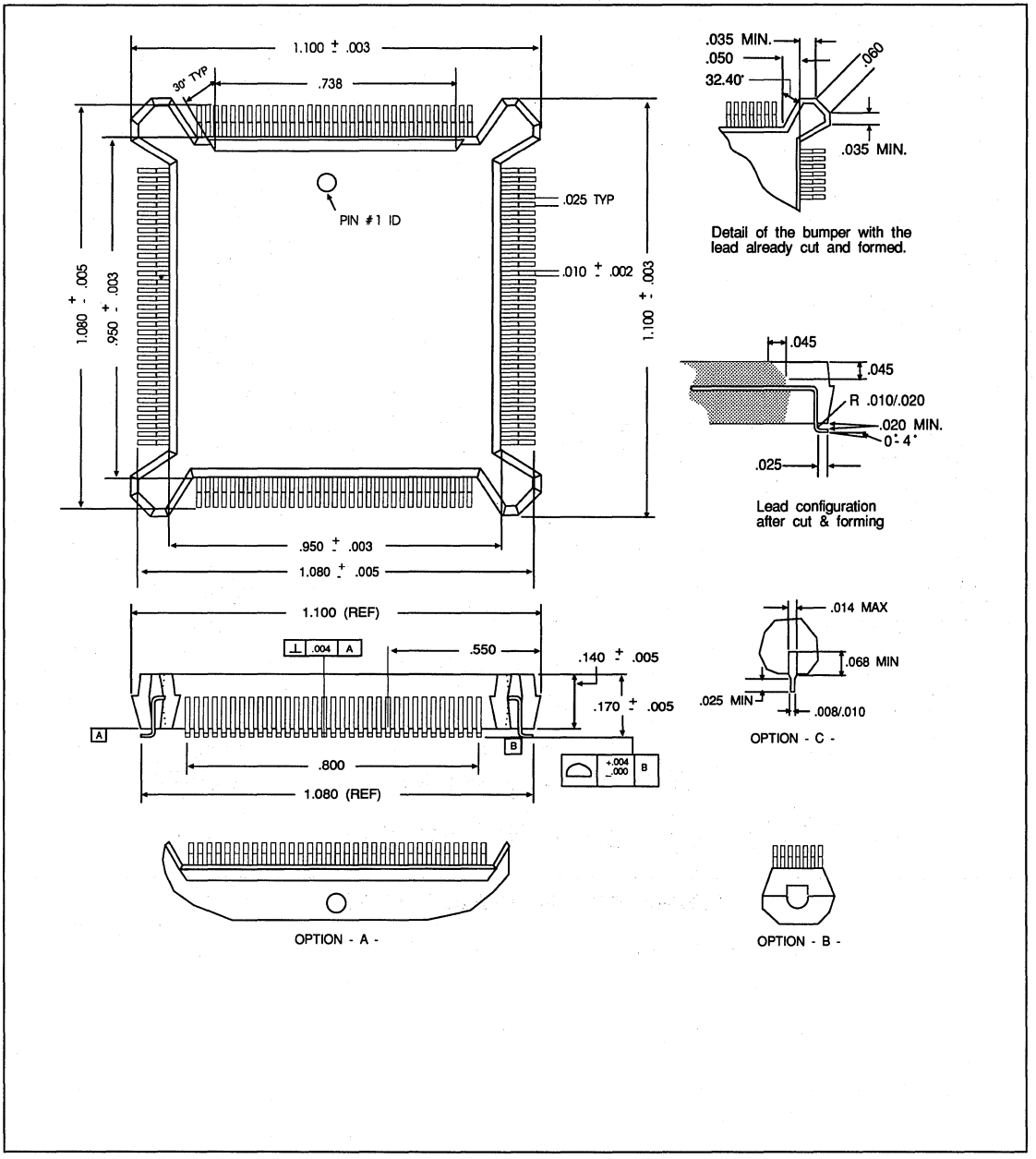

FIGURE 16-1. 132-PIN JEDEC PACKAGE

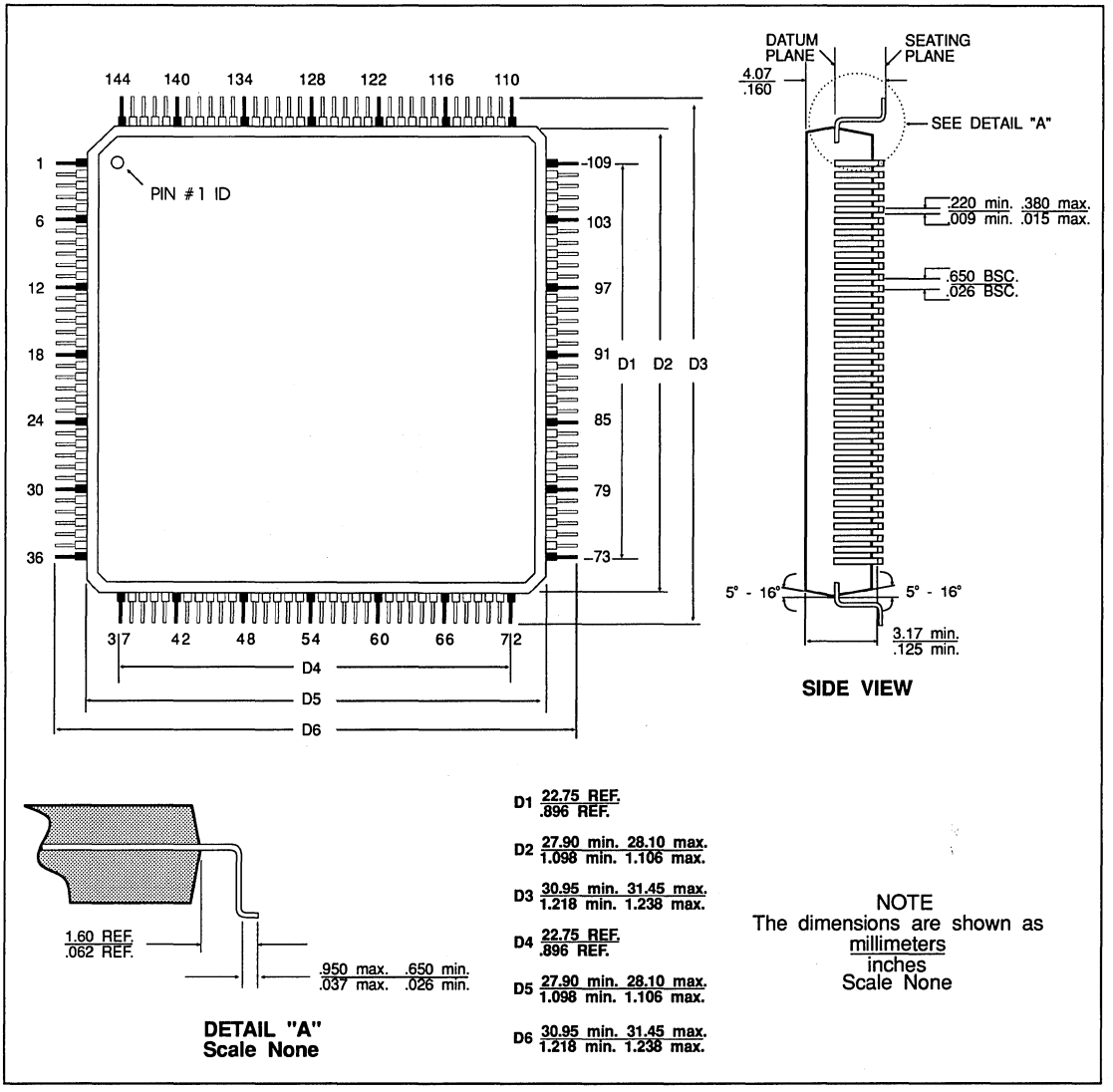

FIGURE 16-2. 144-PIN EIAJ PACKAGE

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WD90C55

VGA LCD

Interface

WESTERN DIGITAL

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1.0 INTRODUCTION

The WD90C55 color interface chip provides the RGB data exchange interface between the WD90C2X family of VGA/LCD controller chips and a number of color panels. The WD90C55 also acts as a pass-through buffer for LCD monochrome data.

This section provides an introduction to the WD90C55 as well as a list of features.

1.1 GENERAL DESCRIPTION

The WD90C55 has been designed to fit the needs of the fast-growing laptop computer market and color-LCD panel technologies. This device interfaces with the following VGA laptop controllers to provide a complete solution in designing laptop computers with both mono- and color-LCD interfaces listed below:

- 90C20
- 90C22
- 90C20A
- 90C26

The WD90C55 drives color LCD panels directly, without requiring additional buffers. It can also be used to drive mono-LCD panels as output buffers.

Using a combination of the WD90C55 and WD90C2X product lines, both mono- and color-LCD panel applications are possible for laptop computers. OEM customers can upgrade their flat-panels as easily as upgrading their CRT displays.

Tables 1-1 and 1-2 show color LCD implementations and number of colors available for each type.

1.2 FEATURES

The major features of the WD90C55 are listed below.

- Direct interface with WD90C20, WD90C22, WD90C20A and WD90C26
- Power down mode control to reduce power consumption
- I/O pin mapping to improve board level testability
- 8-bit (2 and 2/3 pixels) STN color LCD interface
- 16-bit (5 and 1/3 pixels) STN color LCD interface
- Timing adjustment for TFT color LCD panel
- 44-pin PQFP or 48-pin VQFP package

PRODUCT NAME PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26
STN Color LCD	with WD90C55	with WD90C55	with WD90C55	with WD90C55
Hitachi TFT	with WD90C55	with WD90C55	direct	direct
Sharp TFT	N/A	direct	direct	direct

TABLE 1-1 COLOR LCD IMPLEMENTATION

PRODUCT NAME PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26
STN Color LCD	512	4K or 256K	4K	4K or 256K
TFT Color LCD	512	512	512	512 or 27K

TABLE 1-2 COLOR CAPABILITY

2.0 ARCHITECTURE

The WD90C55 color interface chip provides the RGB data exchange interface between the WD90C2X family of VGA/LCD controller chips and a number of color LCD panels, TFT color panels and STN 8-bit/16-bit LCD color panels. It acts as a pass-through buffer for LCD monochrome data, buffering LCD monochrome data from the WD90C2X family, and passing it, along with control signals, to LCD monochrome panels. These interface functions are provided for by the following five modes:

- STN 8-bit Color LCD mode
- STN 16-bit Color LCD mode
- TFT Color LCD for WD90C20
- TFT Color LCD mode for WD90C22
- LCD Monochrome mode

The following additional modes are also provided:

- Pin scan mode
- Output tri-state mode

The WD90C55 turns off any unnecessary logic not selected by SEL[2:0] inputs.

Described in the following subsections are the eight major functional modules of the WD90C55:

- Sequencer (SEQ)
- Data Conversion Control (DCC)
- Bi-Phase Clock Generator (BCG)
- Power Down Control (PDC)
- I/O Pin Mapping Control (IOMP)
- TFT Timing Control (TTC) Interface
- Color Panel Interface (CPI)
- Monochrome LCD Interface

These modules are illustrated in the functional block diagram provided in this section.

2.1 SEQUENCER - STN INTERFACE

The sequencer provides the key timing control from the WD90C2X product to the color LCD panel. In STN color-LCD mode, the WD90C2X sends out 6-bits (2-pixels) every shift clock. The shift clock (XSCLK) is not free-running but toggling. It toggles only when the video data is valid. "WGT-CLK" is used to qualify the valid data and to start the state machine in the sequencer.

2.2 DATA CONVERSION CONTROL - STN INTERFACE

The DCC block provides both 6-bit to 8-bit and 6-bit to 16-bit data conversion.

Only one type of color LCD panel is enabled during the operation.

Unused logic is automatically turned off.

2.3 BI-PHASE CLOCK GENERATOR - STN INTERFACE

The BCG block is used to generate the bi-phase clock outputs XUCLK and XLCLK. These outputs are used in the 8-bit STN color LCD interface.

Eight-bit data is latched on the falling edges of XUCLK and XLCLK. Sixteen-bit data is latched on the falling edge of XLCLK.

2.4 POWER DOWN CONTROL

The PDC block generates the control signals to turn off the WD90C55 when the system goes to power down mode.

The output data bus is driven "Low".

The output clocks are turned off and stay "Low" when the "$\overline{\text{PDOWN}}$" is active low.

2.5 I/O PINS MAPPING/PIN SCAN TEST MODE

This is a unique test mode provided by the WD90C55. When the SEL[2:0] = 000, test mode is enabled.

Test mode allows input pins to be logically connected to the outputs. During In-Circuit Test, test pads can be connected to the pins on a PCB, and a simple "opens and shorts" test verifies that there are no defects.

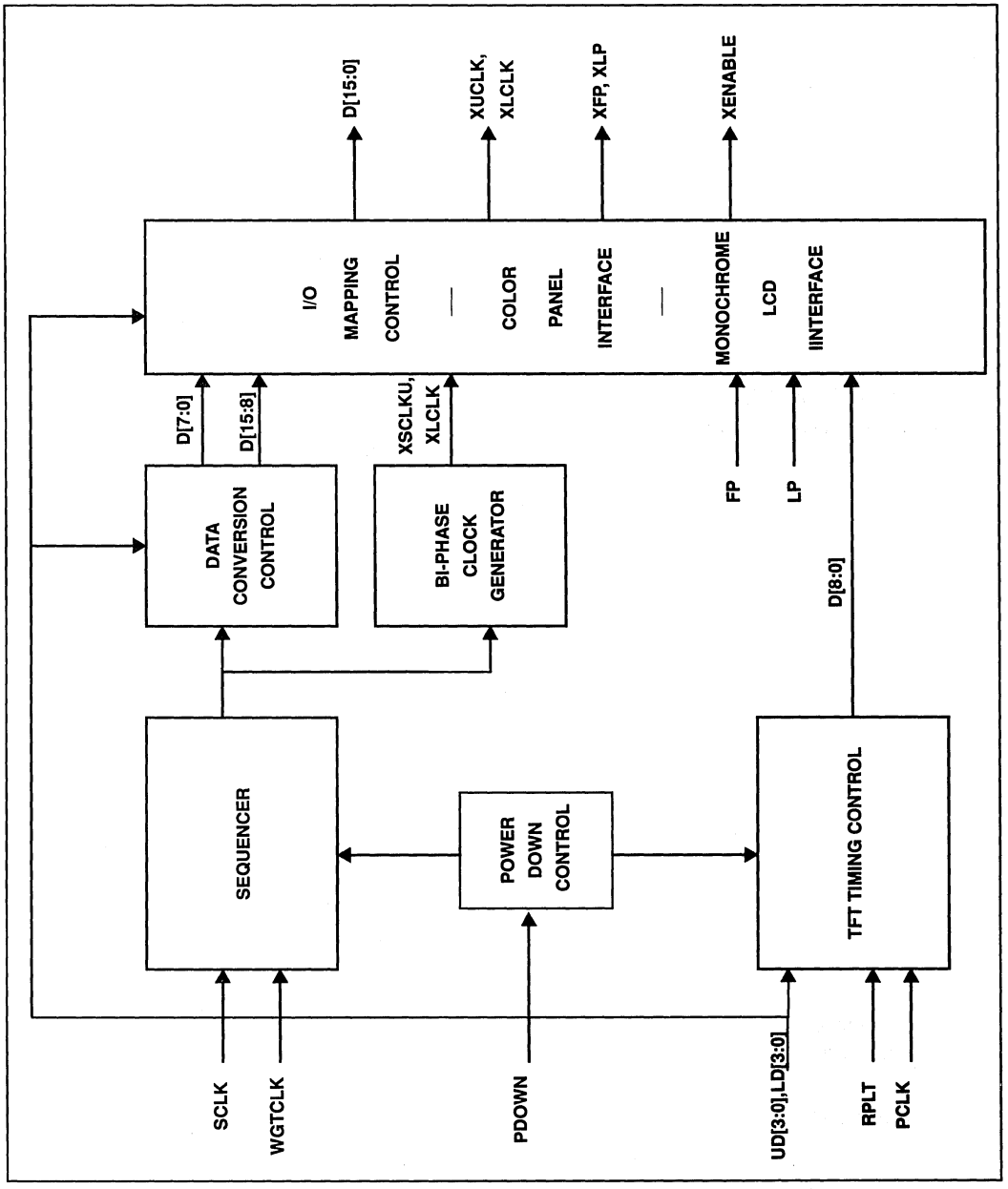

FIGURE 2-1 COLOR LCD FUNCTIONAL BLOCK DIAGRAM

2.6 TFT TIMING CONTROL - TFT INTERFACE

The WD90C20 and WD90C22 require different timing. It is the function of the TTC Block to adjust the timing specification for the Hitachi TFT Color LCD Panel. This adjustment consists of a 7 PCLK delay and 2 PCLK delay for the WD90C20 and WD90C22, respectively.

The WD90C22, WD90C20A and WD90C26 can drive the Sharp TFT color LCD panel directly.

The WD90C20A and WD90C26 can also drive the Hitachi TFT color LCD directly, without a WD90C55 interface.

2.7 COLOR PANEL INTERFACE

The color panel interface block contains the logic to multiplex 8-bit STN data onto the external data bus (D0-D7), or 16-bit STN data onto D0-D15. Nine-bit TFT data (R0-2, G0-2, B0-2) are multiplexed onto D0-DX8, and 8-bit monochrome LCD data is muxed onto D0-D7 via this block.

2.8 MONOCHROME LCD INTERFACE

In Monochrome LCD mode, input data UD[3:0] LD[3:0] and control signals for FP, LP, and SCLK, are multiplexed onto the color interface bus. These input data and control signals are simply buffered and passed through the WD90C55. See the following figure for input data to pixel mapping information.

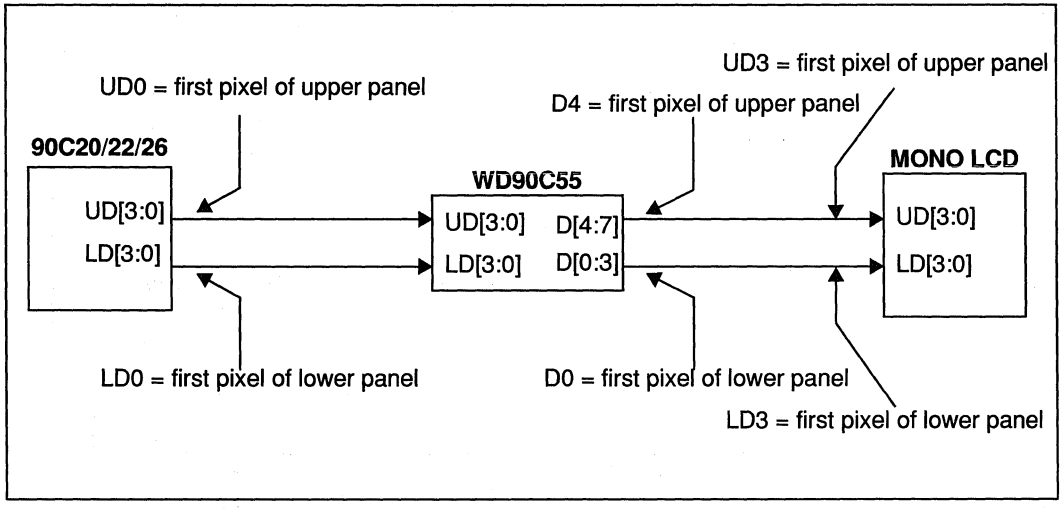

FIGURE 2-2 WD90C55 MONO LCD INTERFACE BLOCK DIAGRAM

3.0 SIGNAL DESCRIPTION

This section contains pin information for both the 44- and 48-pin WD90C55 products. Pin assignment tables and pin diagrams of both are provided.

Section 4.1 describes the 44-pin product and section 4.2 describes the 48-pin device.

3.1 44-PIN WD90C55 PINOUT

This section contains the following information:

- Pinout diagram
- Pin list
- Pin package definitions
- Pin description
- Bus definition
- LCD panel pinout spec

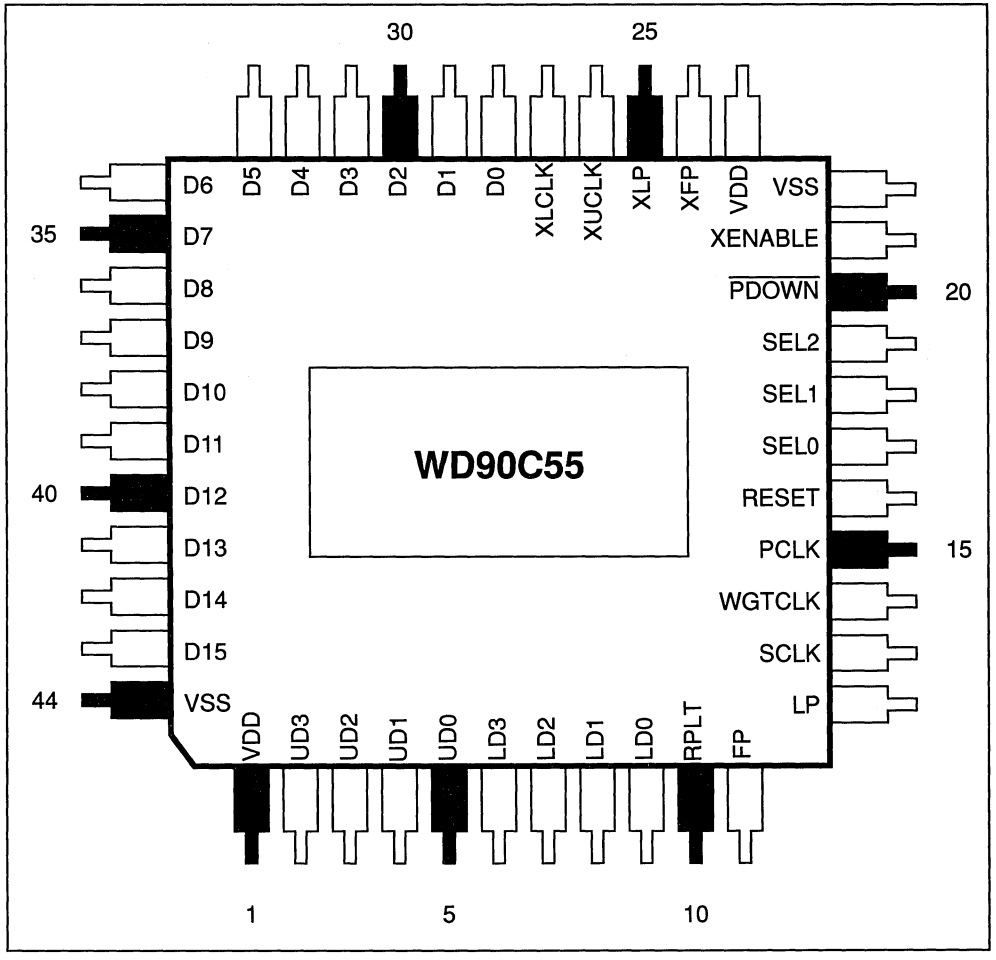

FIGURE 3-1 44-PIN WD90C55 PINOUT DIAGRAM

NAME	PIN#	NAME	PIN#	NAME	PIN#
VDD	1	RESET	16	D3	31
UD3	2	SEL0	17	D4	32
UD2	3	SEL1	18	D5	33
UD1	4	SEL2	19	D6	34
UD0	5	$\overline{\text{PDOWN}}$	20	D7	35
LD3	6	XENABLE	21	D8	36
LD2	7	VSS	22	D9	37
LD1	8	VDD	23	D10	38
LD0	9	XFP	24	D11	39
RPLT	10	XLP	25	D12	40
FP	11	XUCLK	26	D13	41
LP	12	XLCLK	27	D14	42
SCLK	13	D0	28	D15	43
WGTCLK	14	D1	29	VSS	44
PCLK	15	D2	30		

TABLE 3-1 44-PIN PACKAGE PIN LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1,22,23,44	VSS, VDD	I	Power
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[0:2]	I	WD90C55 Selection Bus, bit 0 to bit 2
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output

TABLE 3-2 44-PIN PACKAGE PIN DESCRIPTIONS

SEL[2:0]	DESCRIPTION
0 0 0	Test Mode 1 I/O pin mapping, ICT test
0 0 1	8-Bit STN Panels (Sharp, Seiko)
0 1 0	16-Bit STN Panels (Sanyo)
1 0 0	Monochrome LCD Panels
1 0 1	Hitachi TFT Color Panel (WD90C20)
1 1 0	Hitachi TFT Color Panel (WD90C22)
1 1 1	Test Mode 2, Output buffer tristate test

TABLE 3-3 44-PIN PACKAGE SEL[2:0] BUS DEFINITION

NOTE

The WD90C22 can drive the Sharp TFT color LCD directly without WD90C55.

WD90C55	MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN	9-BIT TFT
XFP	FP	DIN	YD	FLM	VSYNC
XLP	LP	LP	LP	CL1	HSYNC
XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
FR	FR	UNUSED	UNUSED	M	UNUSED
XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
D8	UNUSED	UNUSED	UNUSED	UD0	B0
D7	UD3	D7	D0	LD7	R2
D6	UD2	D6	D1	LD6	R1
D5	UD1	D5	D2	LD5	R0
D4	UD0	D4	D3	LD4	G2
D3	LD3	D3	D4	LD3	G1
D2	LD2	D2	D5	LD2	G0
D1	LD1	D1	D6	LD1	B2
D0	LD0	D0	D7	LD0	B1

TABLE 3-4 44-PIN PACKAGE LCD PANEL PINOUT SPEC

3.2 48-PIN WD90C55 PINOUT

This subsection contains the following information:

- Pinout diagram of the 48-pin WD90C55
- 48-Pin Package List

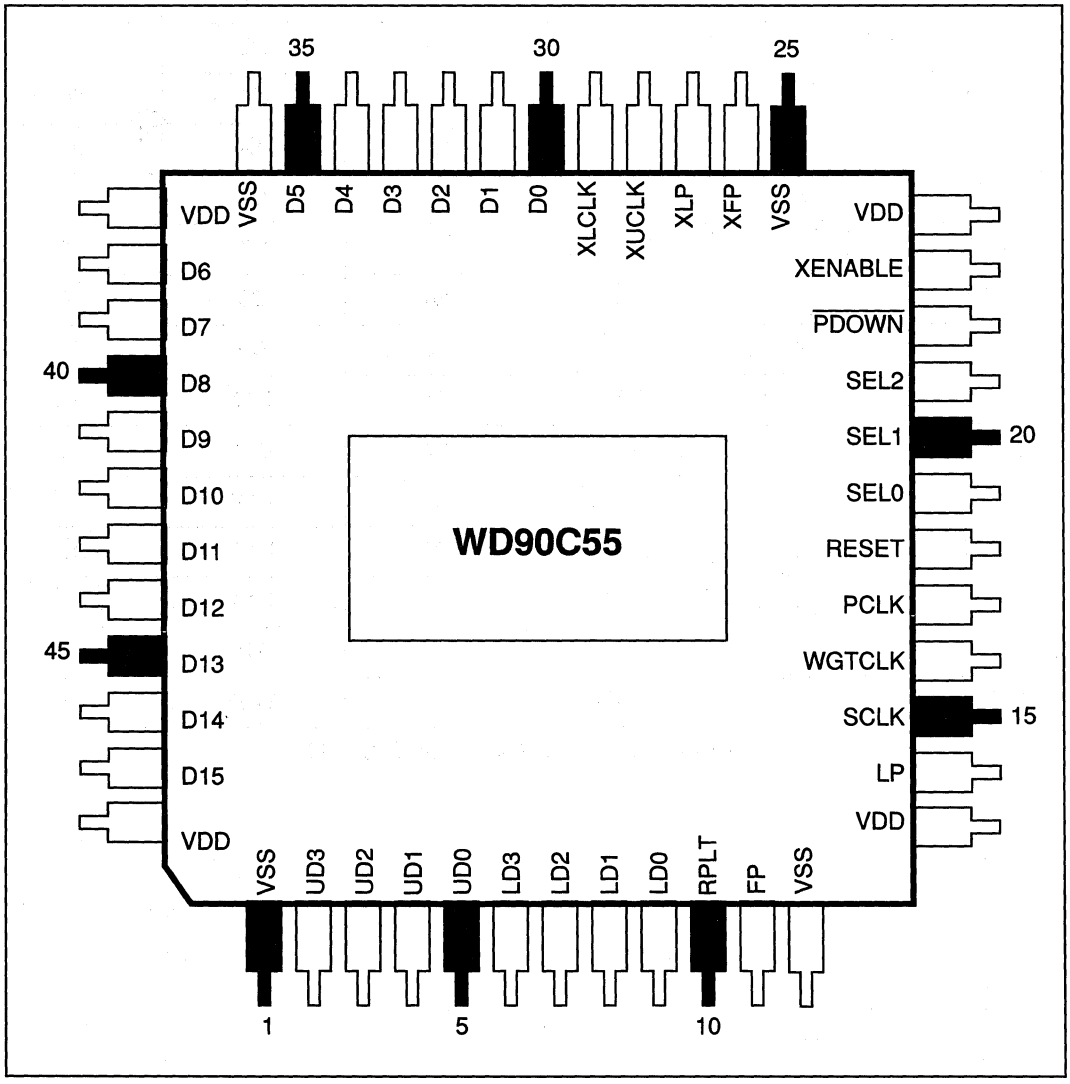

FIGURE 3-2 48-PIN PACKAGE PINOUT DIAGRAM

NAME	PIN #	NAME	PIN #	NAME	PIN #
VSS	1	PCLK	17	D3	33
UD3	2	RESET	18	D4	34
UD2	3	SEL0	19	D5	35
UD1	4	SEL1	20	VSS	36
UD0	5	SEL2	21	VDD	37
LD3	6	$\overline{\text{PDOWN}}$	22	D6	38
LD2	7	XENABLE	23	D7	39
LD1	8	VDD	24	D8	40
LD0	9	VSS	25	D9	41
RPLT	10	XFP	26	D10	42
FP	11	XLP	27	D11	43
VSS	12	XUCLK	28	D12	44
VDD	13	XLCLK	29	D13	45
LP	14	D0	30	D14	46
SCLK	15	D1	31	D15	47
WGTCLK	16	D2	32	VDD	48

TABLE 3-5 48-PIN PACKAGE PIN LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1,22,23,44	VSS, VDD	I	Power
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[0:2]	I	WD90C55 Selection Bus, bit 0 to bit 2
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output

TABLE 3-6 48-PIN PACKAGE PIN DESCRIPTIONS

SEL[2:0]	DESCRIPTION
0 0 0	Test Mode 1 I/O pin mapping, ICT test
0 0 1	8 Bit STN Panels (Sharp, Seiko)
0 1 0	16 Bit STN Panels (Sanyo)
1 0 0	Monochrome LCD Panels
1 0 1	Hitachi TFT Color Panel (WD90C20)
1 1 0	Hitachi TFT Color Panel (WD90C22)
1 1 1	Test Mode 2, Output buffer tristate test

TABLE 3-7 48-PIN PACKAGE SEL[2:0] BUS DEFINITION

NOTE

The WD90C22 can drive the Sharp TFT color LCD directly without WD90C55.

WD90C55	MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN	9-BIT TFT
XFP	FP	DIN	YD	FLM	VSYNC
XLP	LP	LP	LP	CL1	HSYNC
XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
FR	FR	UNUSED	UNUSED	M	UNUSED
XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
D8	UNUSED	UNUSED	UNUSED	UD0	B0
D7	UD3	D7	D0	LD7	R2
D6	UD2	D6	D1	LD6	R1
D5	UD1	D5	D2	LD5	R0
D4	UD0	D4	D3	LD4	G2
D3	LD3	D3	D4	LD3	G1
D2	LD2	D2	D5	LD2	G0
D1	LD1	D1	D6	LD1	B2
D0	LD0	D0	D7	LD0	B1

TABLE 3-8 48-PIN PACKAGE LCD PANEL PINOUT SPEC

4.0 DC ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0° C to 70° C
Storage temperature	-40° C to 125° C
Voltage on all inputs and outputs with respect to Vss	-0.3 to 7 Volts
Power dissipation	0.85 watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70° C
Power Supply Voltage	4.75 to 5.25 Volts

4.3 SUPPLY PINS

PARAMETER	MIN	MAX	CONDITIONS
VDD	4.75V	5.25V	Pins 1, 23 (44 pin package), Pin 8, 48 (48 pin package)

4.4 INPUT PINS

PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC +0.5V	
IIL	-10µA	-10 µA	VIH = VCC, VIL = 0V
IDDS		100 µA	VIN = VCC or VSS, IOH = IOL = 0mA

FP, LP, SCLK, WGTCLK,PCLK,UD[3:0], LD[3:0], RESET, RPLT, $\overline{\text{PDOWN}}$, SEL[2:0]

4.5 OUTPUT PINS

PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6mA
VOH	2.4V		IOH = -2mA
IOZ	-50 µA	50 µA	VOUT = VCC or VSS
C_{out}		100pf	

XFP, XLP, XENABLE, XUCLK, XLCLK, D[15:0]

5.0 AC OPERATING CHARACTERISTICS

Timing is provided for the following:

- STN Color LCD Mode - Input Timing
- STN Color LCD Mode - 8-bit interface
- STN Color LCD Mode - 16-bit interface
- TFT Color LCD Mode - 9-bit interface
- Mono LCD Mode

ITEM	DESCRIPTION	MIN	MAX
1	Rise/Fall Time (Inputs: PCLK SCLK FP LP WGTCLK		5 ns 10 ns 10 ns 10 ns 10 ns
2	UD[3:1], LD[3,1] setup to ↓ SCLK	18 ns	
3	UD[3:1], LD[3,1] hold from ↓ SCLK	18 ns	
4	UD[3:1], LD[3,1] valid from ↑ WGTCLK	10 ns	
5	UD[3:1], LD[3,1] invalid from ↓ WGTCLK	-10 ns	
6	SCLK period	62.5 ns (PCLK = 32 MHz)	80 ns (PCLK = 25 MHz)
7	FP ⇑ to LP ⇓ SETUP time	1LP	
8	FP ⇓ to LP ⇓ HOLD time		0

TABLE 5-1 STN COLOR LCD MODE - INPUT TIMING

Refer to the following figure for timing diagram.

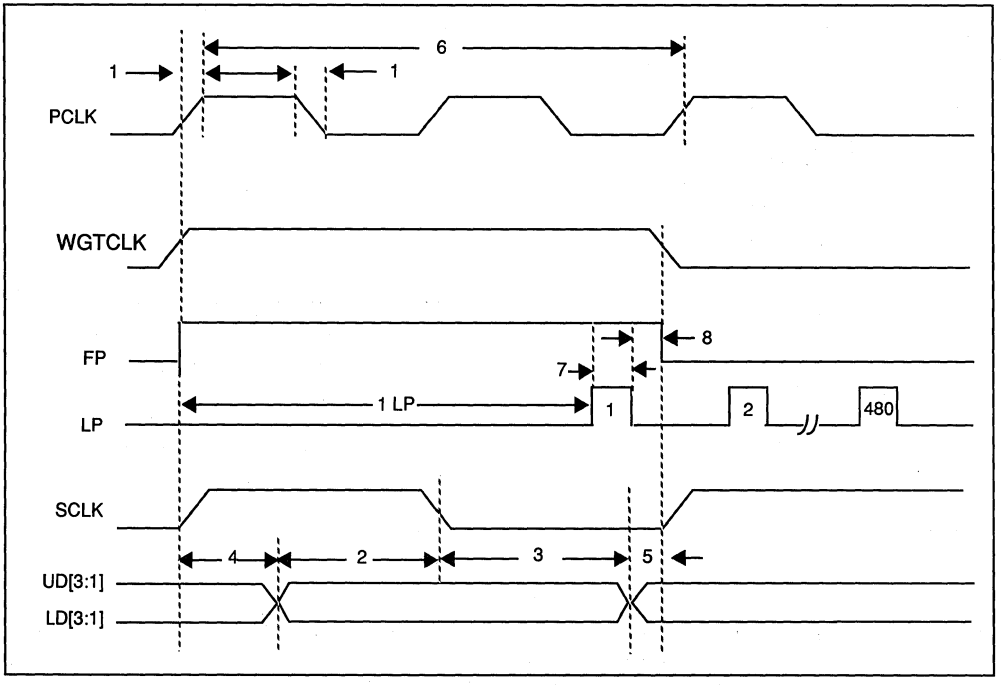

FIGURE 5-1 STN COLOR LCD MODE - INPUT TIMING DIAGRAM

NOTE

$LP = 1/_{PCLK} * 800$

ITEM	DESCRIPTION	MIN	MAX
1	XFP to XLP- Hold time	24PCLK	32 PCLK
2	XFP to XLP- Setup time		1LP
3	↑ SCLK to ↑ XUCLK		240 ns
4	↑ SCLK to ↑ XLCLK		345 ns
5	D[7:0] (even byte) setup to ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
6	D[7:0] (odd byte) hold from ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
7	XUCLK cycle time	163 ns	218 ns
8	XLCLK cycle time	165 ns	205 ns

TABLE 5-2 STN COLOR LCD MODE - 8-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

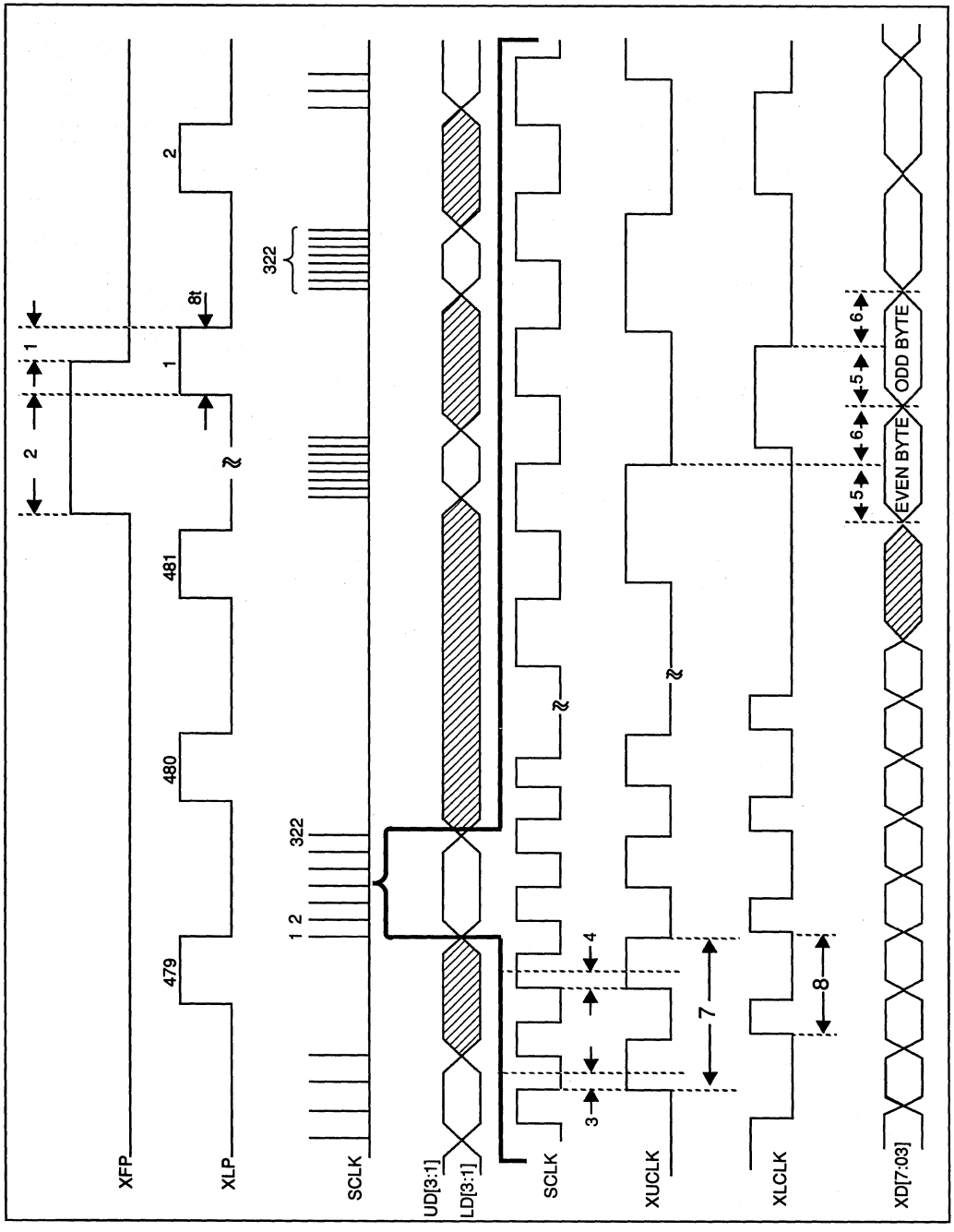

FIGURE 5-2 STN COLOR LCD 8-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	XFP to XLP- Hold time	24PCLK	32 PCLK
2	XFP to XLP- Setup time		1LP
3	↑ SCLK to ↑ XUCLK		240 ns
4	↑ SCLK to ↑ XLCLK		345 ns
5	D[7:0] (even byte) setup to ↓ XUCLK, ↓ XLCLK	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	

TABLE 5-3 STN COLOR LCD MODE - 8-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

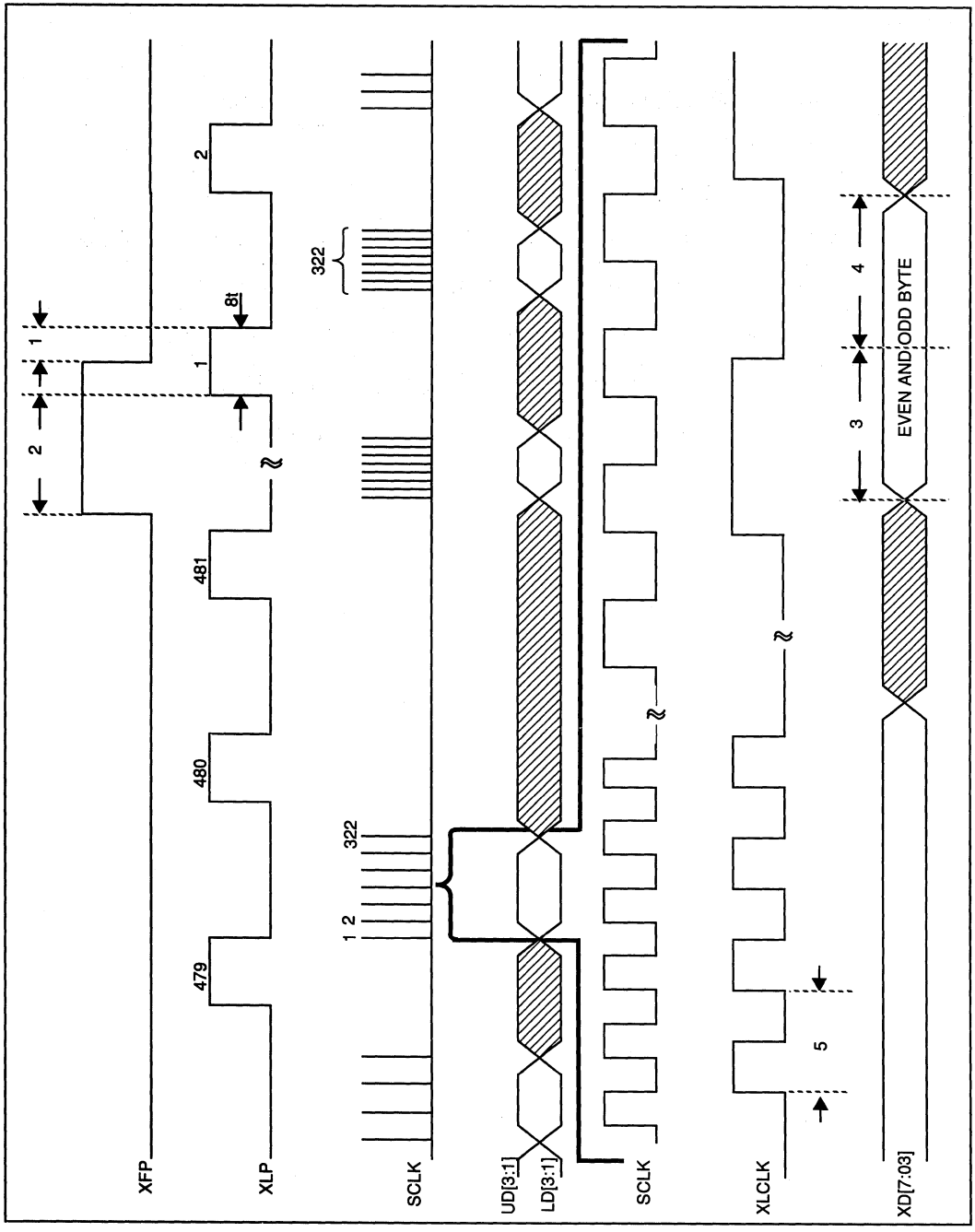

FIGURE 5-3 STN COLOR LCD 16-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	Data IN [8:0] setup to PCLK ↓	10 ns	
2	Data IN [8:0] hold from PCLK ↓	10 ns	
3	D[8:0] setup to XUCLK ↓ (WD90C22) PCLK=25MHz	10 ns	
4	D[8:0] hold from XUCLK ↓ (WD90C22) PCLK=25MHz	10 ns	
5	D[8:0] setup to XUCLK ↓ (WD90C20) PCLK=25MHz	10 ns	
6	D[8:0] hold from XUCLK ↓ (WD90C20) PCLK=25MHz	10 ns	

TABLE 5-4 TFT COLOR LCD MODE - 9-BIT INTERFACE

Refer to the following figure for timing diagram.

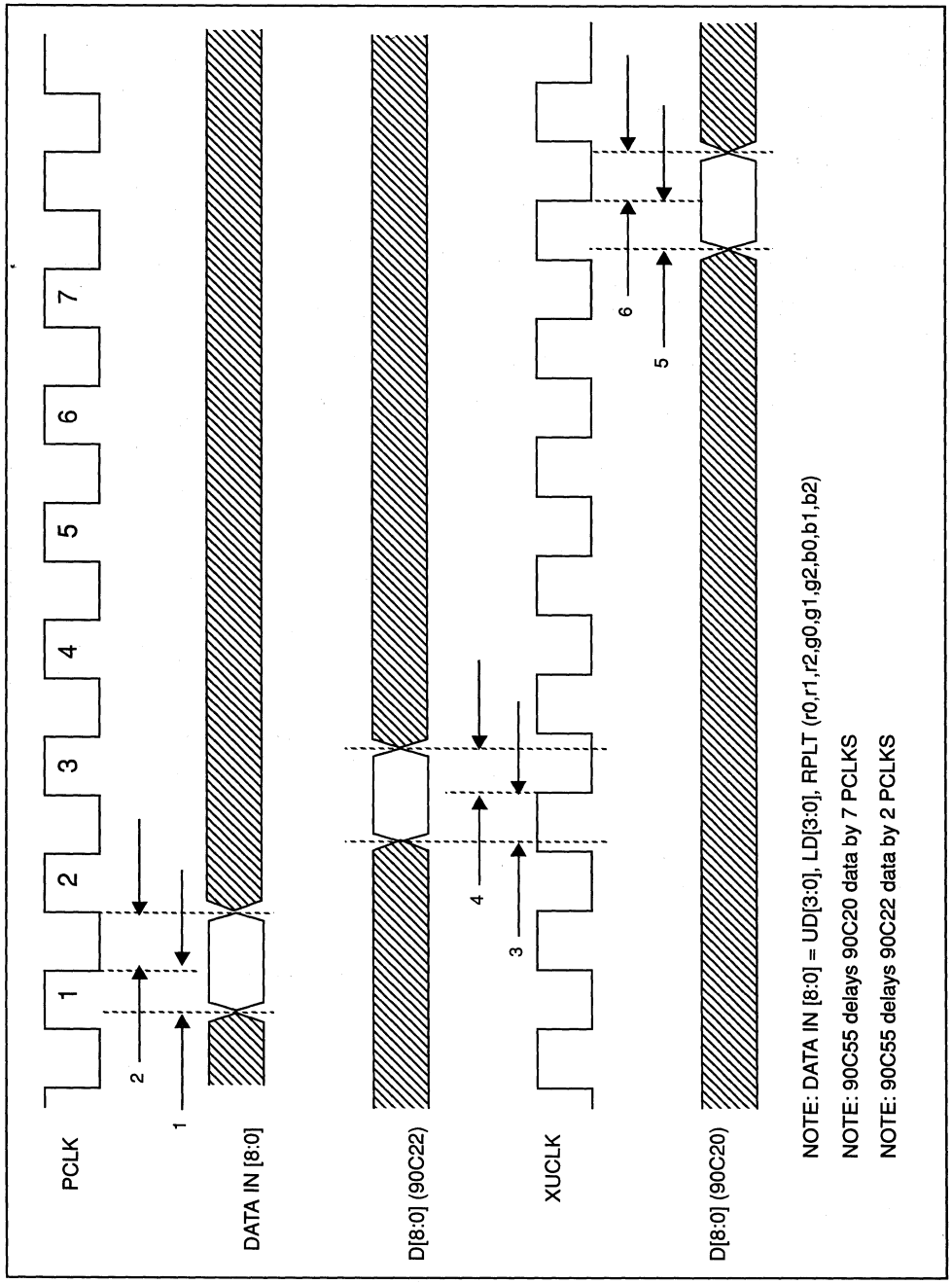

FIGURE 5-4 TFT COLOR LCD 9-BIT INTERFACE MODE TIMING DIAGRAM

6.0 IMPLEMENTATION

This section provides block diagrams of the WD90C55 in each implementation:

- 90C20 Implementation
- 90C20A Implementation
- 90C22 Implementation
- 90C26 Implementation

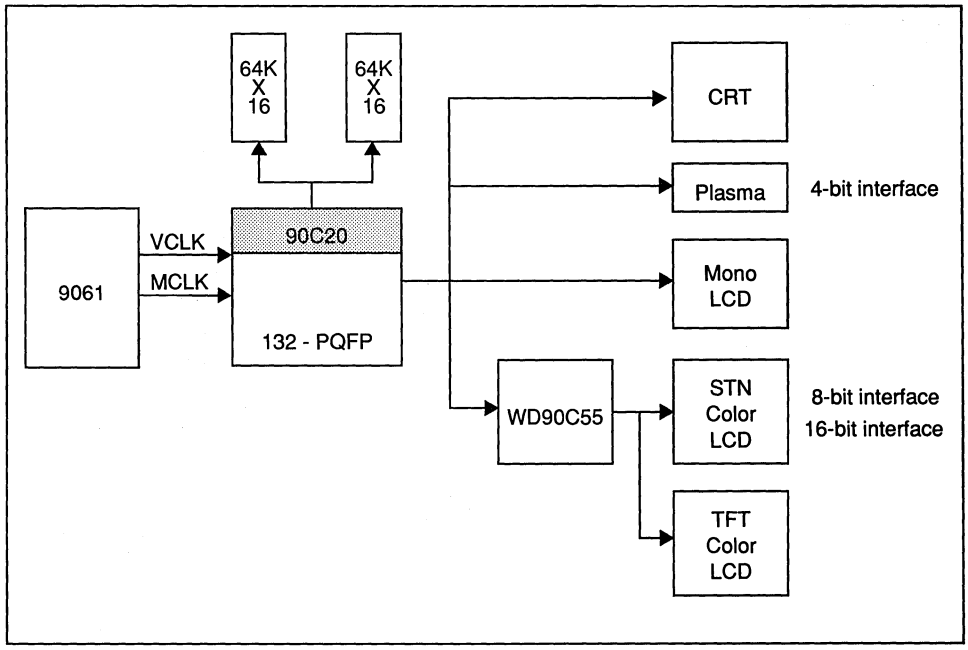

FIGURE 6-1 WD90C55 WITH WD90C20 IMPLEMENTATION

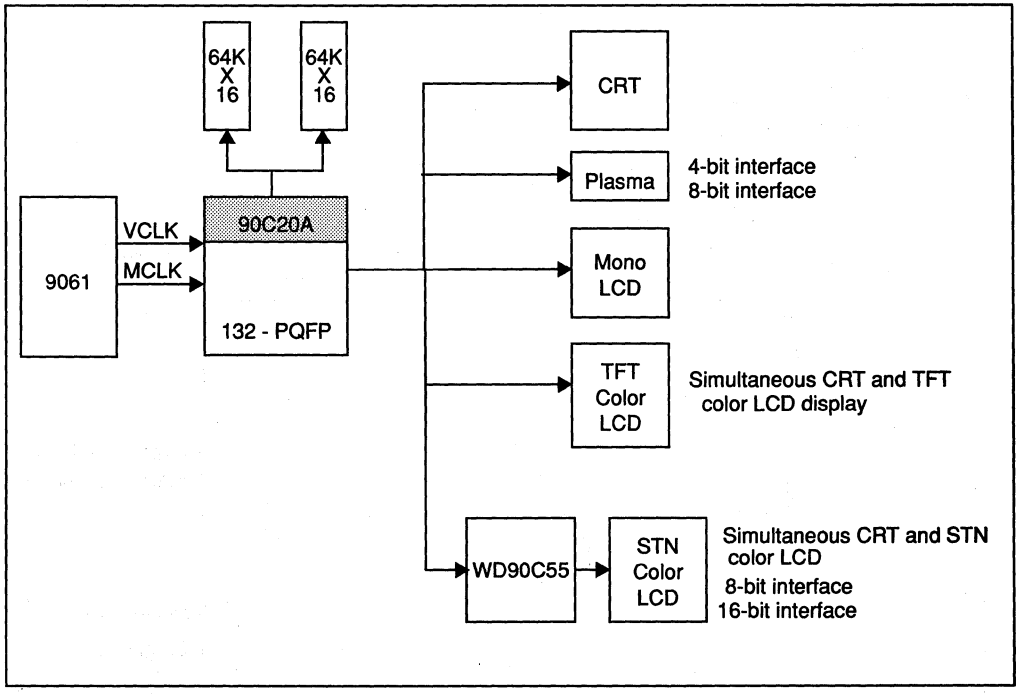

FIGURE 6-2 WD90C55 WITH WD90C20A IMPLEMENTATION

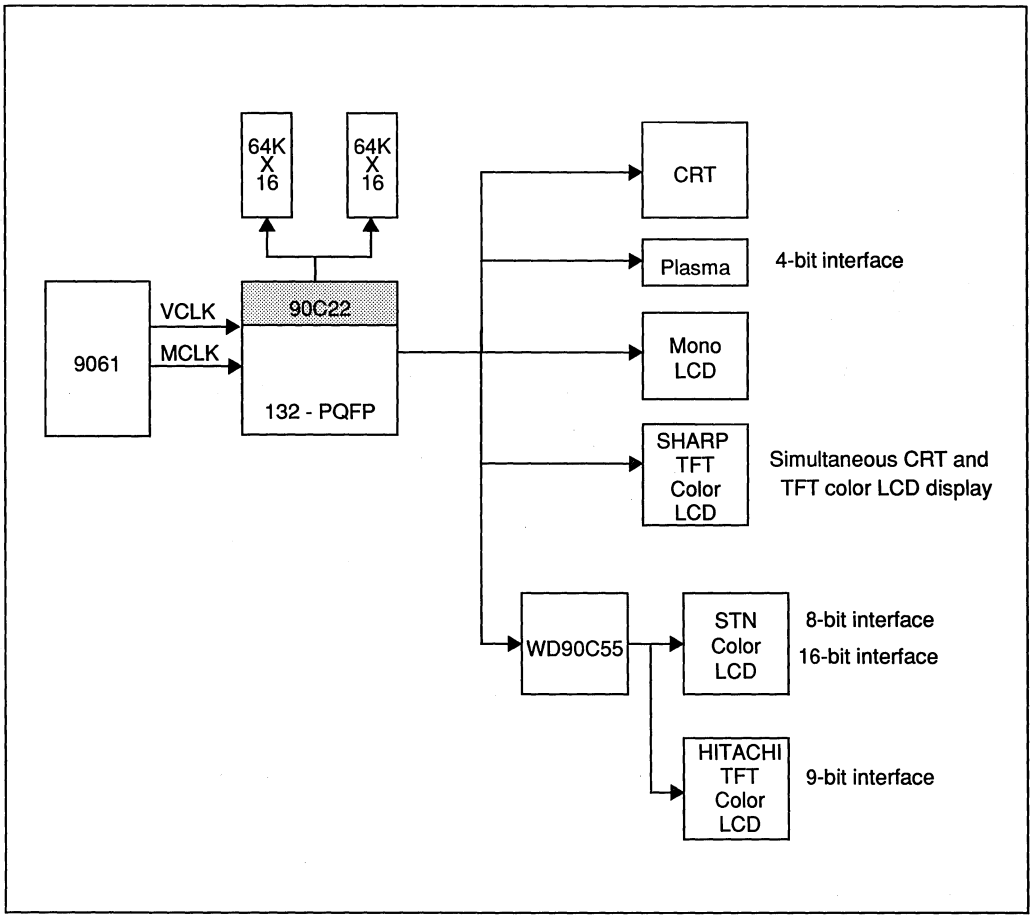

FIGURE 6-3 WD90C55 WITH WD90C22 IMPLEMENTATION

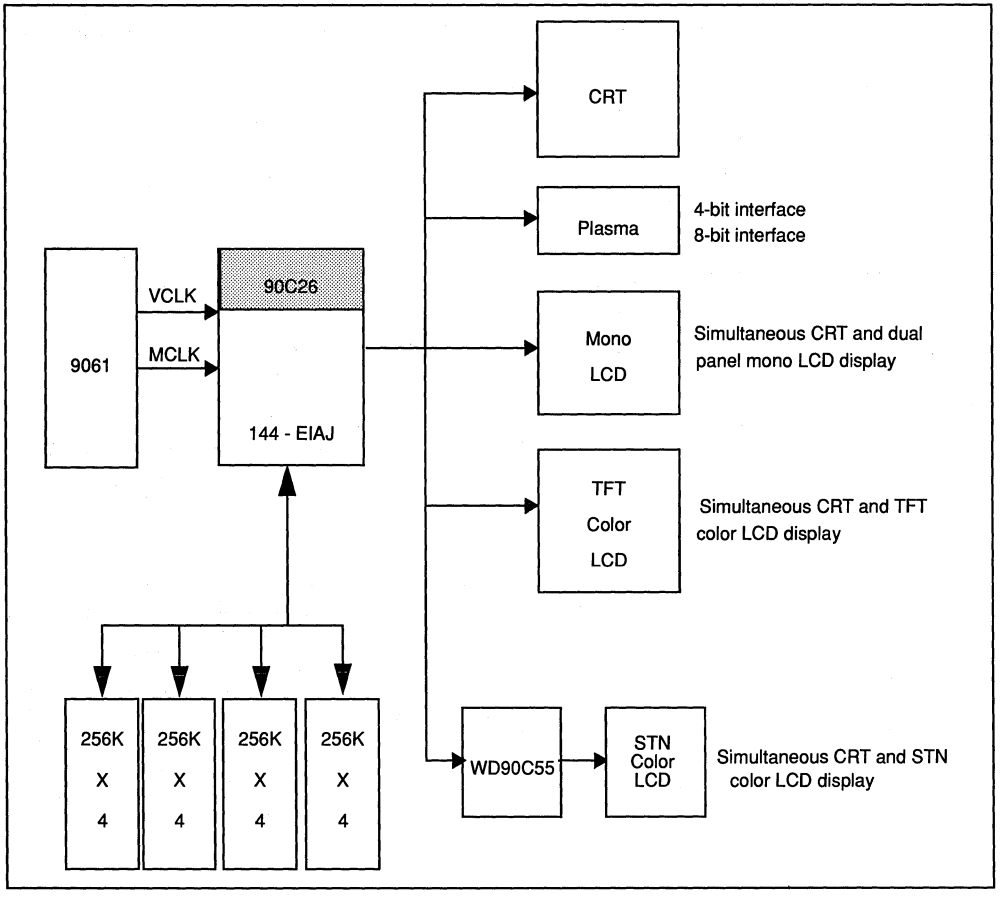

FIGURE 6-4 WD90C55 WITH WD90C26 IMPLEMENTATION

7.0 MECHANICAL SPECIFICATIONS

Figures 7-1 and 7-2 contain the mechanical specifications for WD90C55 44- and 48-pin packages.

7.1 44-PIN PACKAGE

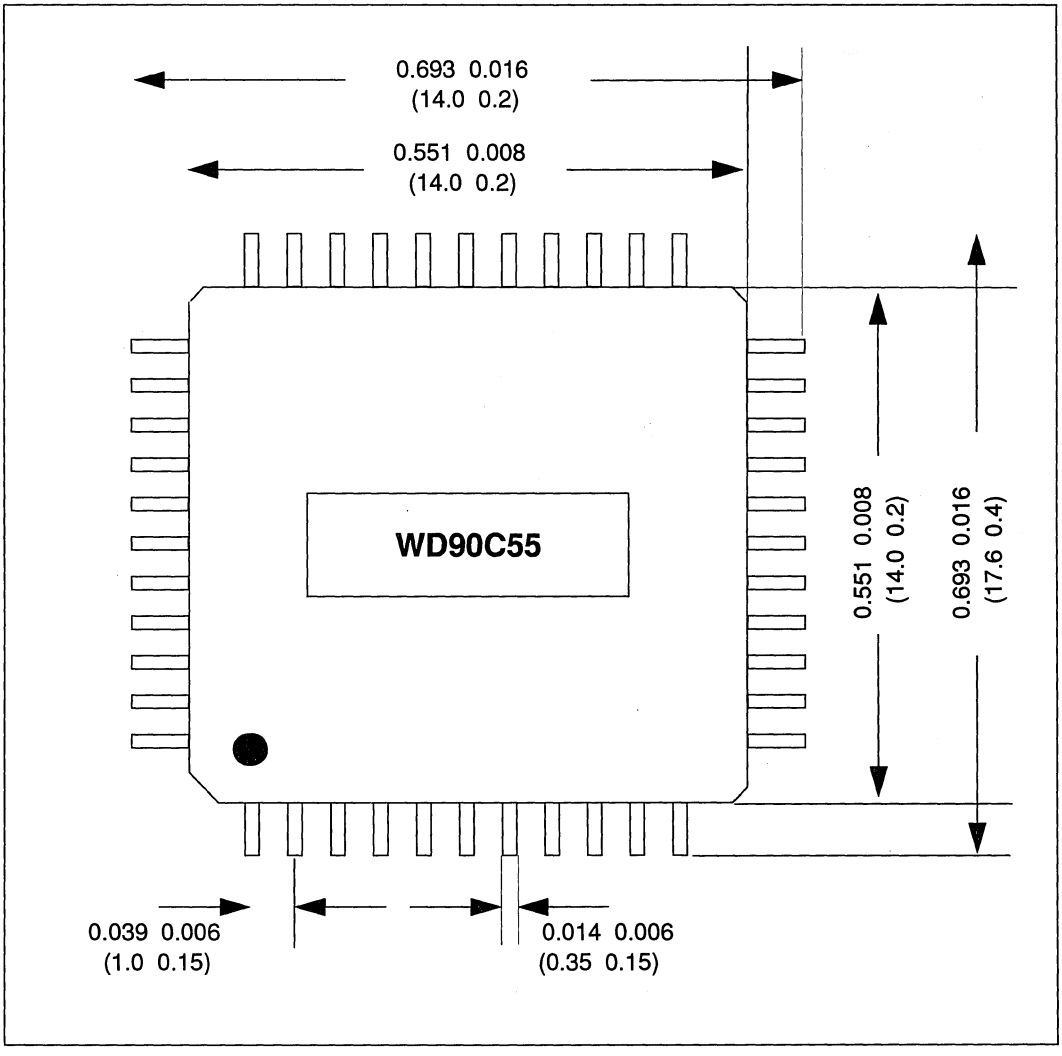

FIGURE 7-1 44-PIN LAYOUT MECHANICAL SPECIFICATION

7.2 48-PIN PACKAGE

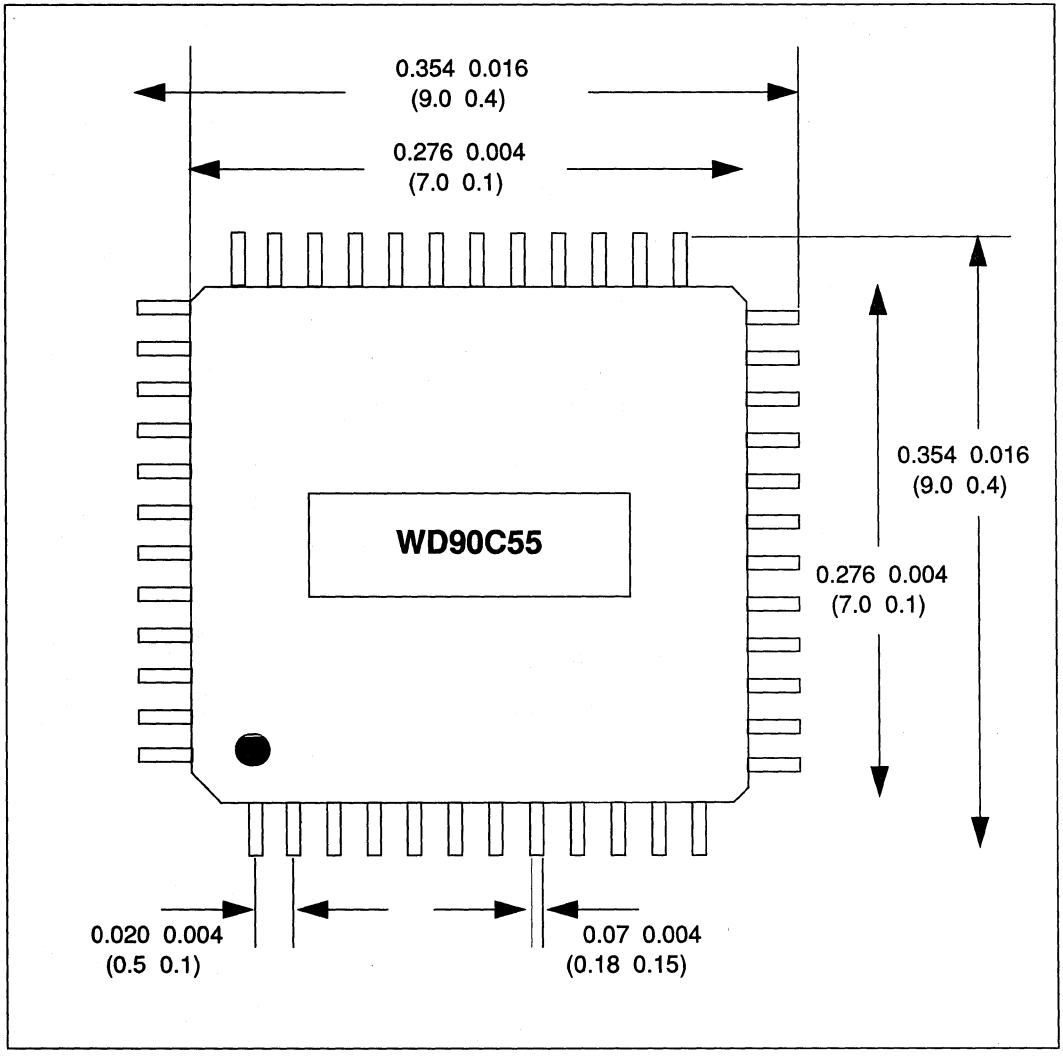

FIGURE 7-2 48-PIN LAYOUT MECHANICAL SPECIFICATION

WD10C01A

Winchester

Disk Controller

WESTERN DIGITAL

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LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The WD10C01A is a VLSI Winchester/Optical Disk Controller chip that provides the data handling and control for intelligent disk applications. The WD10C01A interfaces to nearly any serial disk interface, including ST412, ST412HP, ESDI, SMD, and many optical disk interfaces. The WD10C01A provides great flexibility in format design, allowing for multiple ID fields, special synchronization requirements, special information fields, or almost any other special requirement. The WD10C01A can provide all of the data, status, and control signals required by these interfaces.

1.1 FEATURES

- Disk interfaces and formats supported include ST412, ST412HP, ESDI, SMD and optical disks
- Full multi-sector operation with four byte ID auto-increment
- Up to 24 mbit/second maximum transfer rate
- Supports 16-bit CRC-CCITT polynomial on ID field
- Degree 5 and 6 Reed-Solomon ECC with 3- or 5-way interleave to protect data field against long error burst
- Provides composite syndromes for error correction
- Up to 1:1 interleave operation
- Writeable control store allows flexible error Recovery, including redundant ID and sync fields

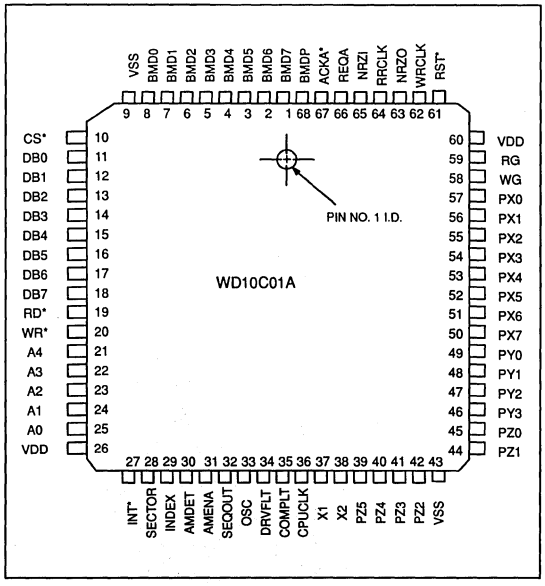

FIGURE 1-1. WD10C01A PIN DIAGRAM

- Support hard or soft sector formats, sector size to 1250 bytes when 5-way interleave is used for degree 5 Reed-Solomon code
- Built in crystal driver for data rate and/or CPU use
- Generic non-multiplexed CPU interface with maskable interrupts
- Separate CPU and disk data busses
- On-the-fly compare against buffer data
- 20 general I/O Lines for disk drive control
- 68-Pin PLCC package

2.0 GENERAL DESCRIPTION

The WD10C01A has separate ports for data DMA transfer and for the microprocessor to achieve a maximum performance.

The WD10C01A performs the disk data serialization and de-serialization. It can interface with various magnetic and optical Data Encoder/Decoders (ENDEC). The data format on the disk is controlled by a Writeable Control Store. It is very flexible with the capability to support various formats including optical disk. The device also has the capability to compare data and verify the ECC. The WD10C01A can perform full track operations without CPU intervention using the Writeable Control Store, auto-incrementing ID registers and the sector counter.

The WD10C01A includes logic implementing CCITT-CRC and Reed-Solomon ECC for data protection. The ID field is protected by sixteen bit CRC and the data field is protected by degree five or six RS-ECC. The user can also select the interleave factor of three or five for the data field. The term "interleave" here should not be confused with the term "sector interleave," which defines the relation between the physical and the logical location of sectors within a track. Interleaving the data field means spreading the data across several ECC code words to improve the capability for correcting longer error bursts.

For the error correction, the WD10C01A generates the composite syndromes. From this error information, the correction software can generate individual syndromes to correct up to two error bytes per interleave (for degree 5) or up to three error bytes per interleave (for degree 6). Optionally, the user can use external, more powerful ECC device, such as WD60C80.

The highly programmable nature of the WD10C01A allows the use of redundant ID and data sync fields within a single sector. This feature, along with the programmable degree 5 or 6 RS-ECC, gives the WD10C01A a greater capability for recovering user data in a sector with 'grown' defects.

The WD10C01A interfaces to the buffer manager, such as WD60C40 through an eight bit DMA port. It uses asynchronous protocol through DREQ/$\overline{\text{DACK}}$ signals.

The WD10C01A has a generic microprocessor interface that allows the WD10C01A to be used with all popular 8-bit microprocessors. The WD10C01A has interrupt capability, which frees up the microprocessor from constantly polling the device status. The WD10C01A also has a built-in crystal oscillator driver that can be used to generate data reference, buffer management, or microprocessor clocks. Two separate outputs are provided with internal programmable dividers. Both outputs have the extra drive voltage and current necessary for driving MOS microprocessor clock inputs.

The WD10C01A has 20 lines dedicated to external I/O ports that the microprocessor can use to control the drive and head select lines, seek command and drive status. Eight lines are output only, six lines are input only, and four other lines can be individually programmed for input or output. Two other latch and hold input lines are tied to the interrupt logic and can be used to detect fault and ready conditions without constantly polling the device.

3.0 SYSTEM BLOCK DIAGRAM

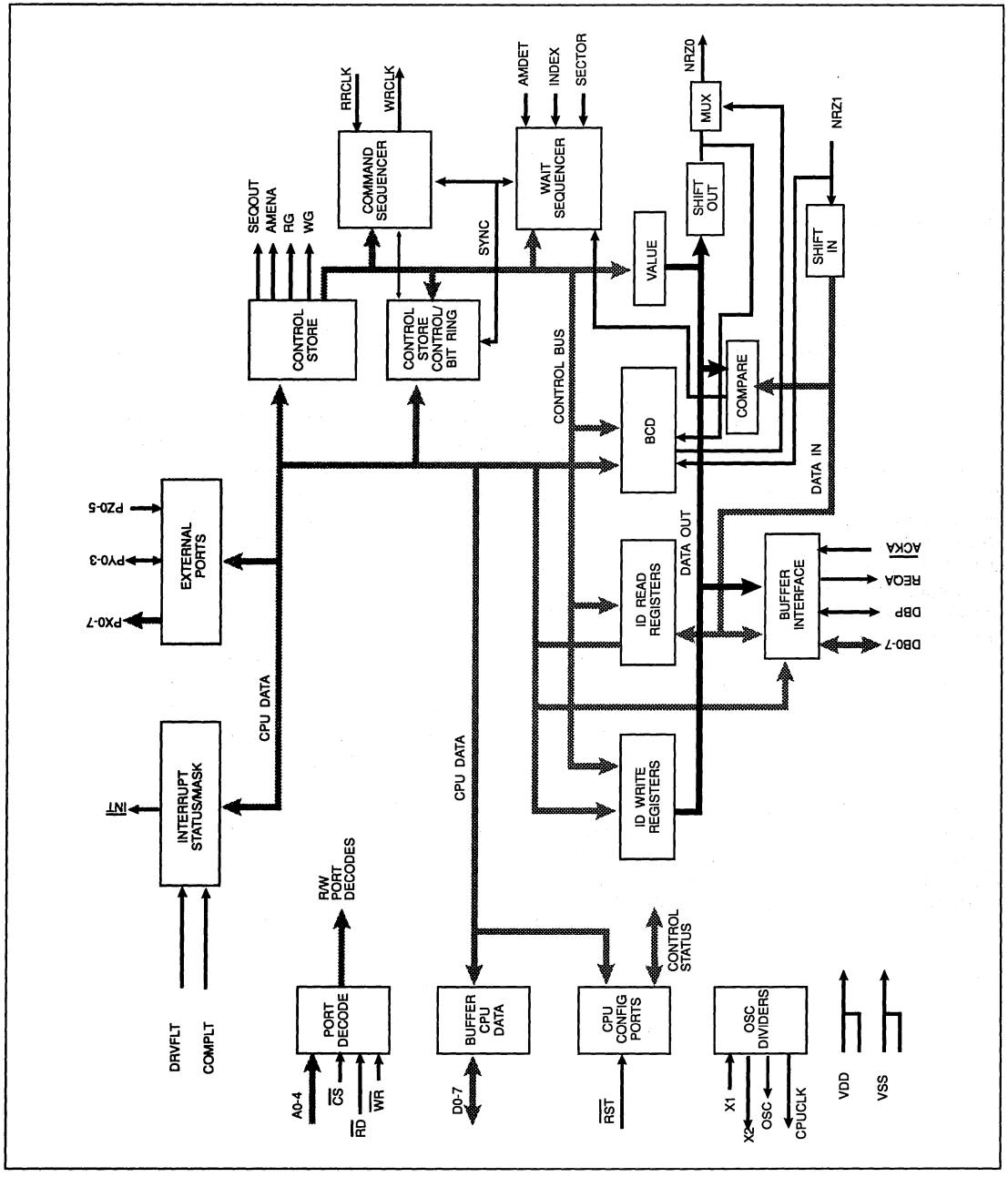

FIGURE 3-1. SYSTEM BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTION

The WD10C01A is a 68-pin PLCC device.

The following section describes the external signals available on the WD10C01A. Conventions are as follows:

I indicates that a signal is an input to the WD10C01A.

O indicates that a signal is an output from the WD10C01A.

I/O indicates that a signal is bidirectional.

I,O indicates that a signal can be input output.

* as a suffix indicates an active low signal; however, most drawings and text use an overscore to indicate an active low signal.

PIN	MNEMONIC	I/O	DESCRIPTION
25-21	A0-A4	I	CPU ADDRESS BUS. These signals are used to address internal WD10C01A registers.
36	CPUCLK	O	CPU CLOCK OUTPUT. This is the OSC output (see below) divided by two or three, selected by an internal register. This output has extra drive for use with certain microprocessors.
10	$\overline{CS}$	I	CHIP SELECT. This active low signal enables the WD10C01A bus interface logic.
11-18	DB0-DB7	I/O	CPU DATA I/O BUS. This data bus is used to transfer data between the CPU and the WD10C01A.
27	$\overline{INT}$	O	CPU INTERRUPT. This active low, open drain output is asserted whenever an enabled interrupt condition occurs on the WD10C01A.
33	OSC	O	OSCILLATOR OUTPUT. The 1x crystal oscillator output, optionally divided by two. This signal has the same drive capability as CPUCLK.
19	$\overline{RD}$	I	CPU READ STROBE. This active low signal enables data from the WD10C01A on to the CPU data bus.
61	$\overline{RST}$	I	RESET. This active low signal resets all internal circuits that must be reset at power on. A complete list is given later in this document. The reset is latched and the condition must be cleared by the CPU.
20	$\overline{WR}$	I	CPU WRITE STROBE. This active low signal strobes data into the selected WD10C01A register from the CPU data bus.
37	X1	I	CRYSTAL DRIVER INPUT. X1 can also be driven by an external clock.
38	X2	O	CRYSTAL DRIVER OUTPUT.

TABLE 4-1. CPU INTERFACE

PIN	MNEMONIC	I/O	DESCRIPTION
67	$\overline{\text{ACKA}}$	I	BUFFER DATA ACKNOWLEDGE. This active low signal indicates to the WD10C01A that data can now be transferred to or from the data buffer.
8-1	BMD0-7	I/O	BUFFER MEMORY DATA BUS. This is an eight bit data bus that interfaces the WD10C01A with the disk data buffer memory.
68	BMDP	I/O	DATA BUS PARITY. This signal is used to generate and check parity with the disk data buffer memory.
66	REQA	O	BUFFER DATA REQUEST. This signal is asserted when the WD10C01A has data to write to the data buffer, or needs data from the data buffer.

TABLE 4-2. BUFFER INTERFACE

PIN	MNEMONIC	I/O	DESCRIPTION
30	AMDET	I	ADDRESS MARK DETECTED. Used only in ST412 type interfaces that use missing clocks or other qualifiers to the sync bytes that mark the start of a field.
31	AMENA	O	ADDRESS MARK ENABLE. Used to write a missing clock sync byte (ST412) or soft sector mark (ESDI, SMD) on the media.
65	NRZI	I	NRZ READ DATA IN. Serial data input from the disk phase-locked loop. This signal is clocked in by the rising edge of RRCLK.
63	NRZO	O	NRZ WRITE DATA OUT. Serial data output. NRZO is valid on the rising edge of WRCLK.
59	RG	O	READ GATE. Active when reading from the disk drive. This signal is turned off for one byte time on an ID search error to reset external data decoders.
64	RRCLK	I	READ/REFERENCE CLOCK. This is the reference clock used to set the data rate for write, and is the recovered clock for read. The switching must be glitch free. NRZI is clocked into the WD10C01A by the rising edge of this clock.
32	SEQOUT	O	SEQUENCER OUTPUT. This signal is a user definable output bit that is set up in the control byte of the sequencer control store (see below). This signal can be used to control an external ECC generator and checker, and is byte aligned with both read and write data.
58	WG	O	WRITE GATE. Active when writing to the disk drive.
62	WRCLK	O	WRITE CLOCK. This is output during write for drives that require it. NRZO data is valid on the rising edge of this clock.

TABLE 4-3. DISK DATA INTERFACE

PIN	MNEMONIC	I/O	DESCRIPTION
35	COMPLT	I	COMPLETE. This signal is used to detect function complete conditions, such as seeks or status requests. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
34	DRVFLT	I	DRIVE FAULT. This signal is used to detect faults from the drive. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
29	INDEX	I	INDEX. This signal is used to indicate the start of a track. This signal is latched for CPU status and interrupt.
57-50	PX0-7	O	PORT X. This general purpose output port is intended for use as drive select and head select signals.
49-46	PY0-3	I,O	PORT Y. This general purpose port is intended for use as other control outputs or inputs. Each bit is selectable as input or output, but all bits are initialized to input when the WD10C01A is reset.
45,44, 42-39	PZ0-5	I	PORT Z. This general purpose input port is used to receive drive status signals.
28	SECTOR	I	SECTOR MARK. This signal is used for marking sector start locations on the media. This can either be a hard sector mark, or a soft mark written on the media using AMENA (ESDI or SMD).

TABLE 4-4. DISK CONTROL INTERFACE

PIN	MNEMONIC	I/O	DESCRIPTION
26,60	VDD	I	+5 VOLTS DC.
9,43	VSS	I	GROUND.

TABLE 4-5. DEVICE POWER

5.0 ARCHITECTURE

The WD10C01A consists of the functional blocks shown in the block diagram in Figure 3-1. VDD and VSS are applied to the device through two separate pins each to improve noise immunity. The top and left hand sides of the diagram show CPU interface features, the right hand side shows disk interface features, and the bottom shows buffer interface features. These blocks are discussed in the following paragraphs.

The PORT DECODE block generates the 28 write strobes and 25 read strobes used by the microprocessor to access the various internal control and status ports. These include the interrupt registers, external disk control ports, control store, control store control, configuration, ECC control, and ID registers.

The BUFFER CPU DATA block controls the transfer of data between the microprocessor and the internal registers. The direction control is qualified by chip select ($\overline{CS}$) and read strobe ($\overline{RD}$).

The CPU CONFIGURATION PORTS are used to reset the WD10C01A, set the address mark enable timing, set the buffer interface timing, and select the frequency of the clock outputs, OSC and CPUCLK.

The OSCILLATORS AND DIVIDERS block generates the clock outputs, OSC and CPUCLK, using an external crystal (or clock input) and dividers to select the frequency. Frequency selection is glitch free.

The INTERRUPT STATUS AND MASK registers are used to check and mask interrupts. The mask register does not affect the status register inputs. The interrupt sources include index and sector mark, drive fault and operation complete, ECC errors, and internal event status.

The EXTERNAL PORTS are used to generate control signals and read status with the disk drive. Eight bits are output, six are input, and four are individually programmable for either input or output.

The CONTROL STORE consists of 32 words of 28 bits that are used to program the format of the disk sector. The data source, field length, error handling and checksum selection, and control signals, like Read Gate and Write Gate, are controlled by the data stored here.

The CONTROL STORE CONTROL determines the next address in the control store to use, whether the next sequential address or a jump to another address. This block includes the sector counter used for multi-sector commands. This block also includes the BIT RING COUNTER, which determines the timing of data transfers in the WD10C01A.

The WAIT SEQUENCER handles searches for index, sector mark, address mark, and byte synchronization.

The ID WRITE REGISTERS are 8 eight bit registers that are used to set the ID write field for format, or the search field for read/update write. Four of the registers are counters that auto-increment during multi-sector commands. The other four registers do not increment, and are used for defect and flag information. The first byte of the four counters can be disabled for three byte ID fields.

The ID READ REGISTERS are used to read the last ID read from the media to aid in defect handling.

The ECD block performs the CRC on ID, selects the degree of RS-ECC with 3- or 5-way interleave on data fields, generates the checksum bytes, creates the composite syndromes and ECC error status necessary for the calculation of error location and mask.

The VALUE register holds immediate data from the control store when generating gaps, sync fields, and address mark bytes.

The SHIFT OUT register serializes internal or external (buffer) data for writing on the disk. The output is multiplexed with the output of the checksum register.

The SHIFT IN register de-serializes the read data from the disk, clocked in by RRCLK. The data is also transferred to the checksum register for checking.

The COMPARE block is used to compare incoming read data with an internal or external data

source. These include byte synchronization detection, ID field search, and buffer data compare.

The BUFFER INTERFACE handles the fetching and writing of data with the external data buffer. This includes parity generation and checking, and data handshake with the buffer controller.

5.1 ERROR CORRECTION AND DETECTION CODES

5.1.1 CCITT-CRC

The WD10C01A protects the ID fields using the CCITT-CRC code. The polynomial is defined as follow:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

The user can select the initial state of the shift registers to be either all zero's or all one's.

5.1.2 Reed-Solomon ECC

The data fields are protected using the interleaved Reed-Solomon code operating on 8 bits symbols. The redundancy bytes are inverted. WD10C01A supports two polynomials of degree five and six. The generator polynomials operate in the finite field GF(256), which are defined as follow:

Let β^i represent elements of a finite field defined by a polynomial over GF(2):

$$g(x) = x^8 + x^5 + x^3 + x^2 + 1.$$

The elements of the finite field employed by the codes are:

$$a^i = (\beta^i)^{88}.$$

The generator polynomials are self reciprocal and defined as follows:

1. Degree 5, distance 6:

$$G(x) = (x+a^{253})*(x+a^{254})*(x+a^0)*(x+a^1)*(x+a^2).$$

The coefficients of the polynomial in decimals are:

1, 60, 183, 183, 60, 1.

2. Degree 6, distance 7:

$$G(x) = (x+a^{125})*(x+a^{126})*(x+a^{127})*(x+a^{128})*$$
$$(x+a^{129})*(x+a^{130}).$$

The coefficients of the polynomial in decimals are:

1, 176, 126, 163, 126, 176, 1.

The calculated checkbytes are **inverted** before they are written into the disk. During read operation, the WD10C01A computes the composite syndromes by recalculating the checkbytes for the data field being read and compare them against the checkbytes written on the disk. The individual syndromes can be computed by dividing the composite syndromes with the factors of the generator polynomial:

$$S_i(x) = R(x) \text{ MODULO } G_i(x)$$

where:

i = 0..ecc degree -1.

$S_i(x)$ = i'th individual syndrome.

R(x) = composite syndrome.

$G_i(x)$ = factor of the generator polynomial, $(x+a^i)$.

The WD10C01A supports two data interleaving factors. The user can optimize the performance by choosing the right degree and interleave combination.

The following table shows the redundancy overhead and maximum field size.

Interleave Factor	Degree 5		Degree 6	
	Overhead*	Max. Data* Field Size*	Overhead*	Max. Data* Field Size*
3	15	750	18	747
5	25	1250	30	1245

* all units bytes

6.0 PROGRAMMING REFERENCE

6.1 REGISTER ASSIGNMENTS

The WD10C01A contains 32 output and 23 input ports distributed in a 32 port address space, selected by A0-A4, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$.

The ports are split into three functional groups:

- configuration group
- device control group
- ID registers.

Address lines A4 and A3 select the group, and A2 through A0 select the register in the group.

CONFIGURATION			DEVICE CONTROL 1		
Address	**Assignment**	**R/W**	**Address**	**Assignment**	**R/W**
00000	SRESET	W	01000	PORTX	R/W
00001	SISR	R/W	01001	PORTY	R/W
00010	SIMR	R/W	01010	PORTZ/AMC	R/W
00011	SEQSTS/PYC	R/W	01011	SEQCTL	R/W
00100	CSERR	R/W	01100	START	R/W
00101	CSCTL	R/W	01101	LOOP	R/W
00110	CSVAL	R/W	01110	ECCCTL	R/W
00111	CSCNT	R/W	01111	SECCNT	R/W
DEVICE CONTROL 2			**ID REGISTERS**		
Address	**Assignment**	**R/W**	**Address**	**Assignment**	**R/W**
10000	ECCP	W	11000	ID0	R/W
10001	ECCS	R	11001	ID1	R/W
10010	SPORT	R	11010	ID2	R/W
10011			11011	ID3	R/W
10100			11100	ID4	R/W
10101			11101	ID5	R/W
10110	TEST - do not use		11110	ID6	R/W
10111	SKIP	W	11111	ID7	R/W

TABLE 6-1. REGISTER GROUPS

6.2 REGISTER DEFINITIONS

The following sections describe each register in detail. The use of the register is described in general and/or each bit is described. The table below defines how bit directions are defined in these sections. Sometimes, a bit encoding is used to select a function that is not obvious from the definition of the bits involved. Refer to the section on Programming Notes for descriptions of these special modes.

The following table contains bit direction definitions.

Direction	Meaning
R	indicates that the bit is read only
W	indicates that the bit is write only
R/W	indicates that the bit may be written and read
R/C	indicates that the bit may be read and cleared by writing a one to that bit
C	indicates that the bit may be cleared by writing a one to that bit

6.3 CONFIGURATION GROUP

The configuration group is used to do initial set up of ports and clocks, handle interrupts, and set up the control store memory.

OSCDIV	CLKDIV	OSC	CPUCLK
0	0	XTAL/2	XTAL/6
0	1	XTAL/2	XTAL/4
1	0	XTAL	XTAL/3
1	1	XTAL	XTAL/2

6.3.1 SRESET - Set Hardware Reset Register (00)

Bits 7-1 are cleared to zero by reset. Bit 0 is set to one by an external reset. When writing one to SRST, any data on bits 7-1 are lost.

REGISTER	BIT	DIR	DEFINITION
00	7	W	CLKDIV: CPUCLK divisor (see Note 1 below)
00	6	W	OSCDIV: OSC divisor (see Note 1 below)
00	5	W	Unused.
00	4	W	Unused.
00	3	W	Unused.
00	2	W	REQTIM: buffer request timing. When this bit is one, REQA is set at the same time that the internal buffer data holding register is ready. When this bit is zero, REQA occurs one RRCLK period early. This aids in interfacing to certain buffer circuits that have a lag in their response times.
00	1	W	ID3$4: select ID address size (see Note 2)
00	0	W	SRST: hardware reset. This bit is set by an external reset on the $\overline{RST}$ input, or can be set by writing one to this bit. This bit must be set to zero before operating the WD10C01A, or before setting any of the other bits in this register or any other register.

TABLE 6-2. SRESET - SET HARDWARE REGISTER (00)

NOTE 1: The CPUCLK dividers are prescaled by the OSC dividers, as shown in the table below (XTAL is the clock generated by a crystal at X1 and X2):

NOTE 2: The eight ID register bytes are split into two fields: the first four are address, and auto-increment for each sector; and the second four are flag bytes which do not increment. The ID3$4 bit selects whether 3 or 4 bytes of ID address bytes will be used in the ID field. In 3 byte address fields, register ID0 is ignored. See Table 6-2A.

Two other considerations:

- CPUCLK = XTAL/3 will not be a 50% duty cycle unless XTAL is also a 50% duty cycle clock.
- When resetting the WD10C01A under CPU control, and the CPU is clocked by CPUCLK or OSC, set CPUDIV and OSCDIV back to zero before setting SRST. If this is not done, the clocks could glitch and cause the CPU to fail.

ID3$4	Address Counter Size	First Register In Field
0	4 bytes	ID0
1	3 bytes	ID1 (ID0 not used)

TABLE 6-2A. ID REGISTER SELECTION

6.3.2 SISR - Interrupt Status Register (01)

The interrupt status register is designed to be used in interrupt or polled mode. The status is not affected by the interrupt mask register (see below). The interrupting condition has precedence over the CPU clear, which is performed by writing a one to the selected interrupt bit. If the condition still exists, the clear will not be successful. The COMPLT and FAULT interrupts will stay set until the cause of the interrupt goes away. The IDFULL, DXFER, SECEND, and SM$IX interrupts are generated by single bit time pulses that are triggered by the leading edge of the interrupt cause, and can therefore be cleared immediately. SEQSTP is a direct status signal and is cleared when the sequencer is executing a command.

Before checking any bit (except SEQSTP), it should be cleared by writing a one to it. This register is not affected by reset.

REGISTER	BIT	DIR	DEFINITION
01	7	R	GINT - group interrupt. This is the state of the $\overline{INT}$ output, which is the logical OR of all of the enabled (by SIMR, see below) interrupt sources in this register.
01	6	R/C	IDFULL - ID registers full. This interrupt is set at the end of any ID field access by the transition of the control store ID bit from true to false. This interrupt should be serviced before the next ID field is accessed. This interrupt can be cleared immediately.
01	5	R/C	DXFER - data transfer started. This interrupt is set at the start of the data field by the transition of the control store BUFF or NOXFER bit from false to true. This interrupt can be used to determine when it is safe to write to the LOOP, SKIP, SECCNT, or ID registers, if necessary. This interrupt can be cleared immediately.
01	4	R/C	COMPLT - complete. This interrupt is set in response to the COMPLT input pin going true. This interrupt cannot be cleared until the COMPLT input pin goes false.
01	3	R	SEQSTP - sequencer stopped. This interrupt is set when the sequencer has stopped executing a command. This interrupt is cleared when the sequencer starts a new command.
01	2	R/C	SECEND - sector end interrupt. This interrupt is set by the leading edge of the LAST bit in the control store (see below). This is used to signal the end of a sector for buffer management and other overhead processing. The size of the field in which the LAST bit is set can be adjusted to match the processing overhead to the end of the sector for maximum CPU performance; the minimum size for this field is two bytes. This interrupt can be cleared immediately.
01	1	R/C	SM$IX - sector mark or index passed. This interrupt is set by the leading edge of the SECTOR or INDEX input going true, as selected by the mask in the sequencer control register (SEQCTL). RRCLK must be present for this interrupt to function. This interrupt can be cleared immediately.

TABLE 6-3. SISR - INTERRUPT STATUS REGISTER

REGISTER	BIT	DIR	DEFINITION
01	0	R/C	FAULT - drive fault. This interrupt is set in response to the DRVFLT input pin going true. This interrupt cannot be cleared until the DRVFLT input pin goes false.

TABLE 6-3. SISR - INTERRUPT STATUS REGISTER (CONTINUED)

6.3.3 SIMR - Interrupt Mask Register (02)

The interrupts listed are described in the SISR description. Writing a one to the mask bit enables the interrupt. The state of the mask bits does not affect the reading of status in SISR in any way. This register is cleared to zero by reset (interrupts disabled). Disabling GINT overrides any other enables set in this register.

REGISTER	BIT	DIR	DEFINITION
02	7	R/W	GINT - enable all interrupts
02	6	R/W	IDFULL - enable IDFULL interrupt
02	5	R/W	DXFER - enable DXFER interrupt
02	4	R/W	COMPLT - enable COMPLT interrupt
02	3	R/W	SEQSTP - enable SEQSTP interrupt
02	2	R/W	SECEND - enable SECEND interrupt
02	1	R/W	SM$IX - enable SM$IX interrupt
02	0	R/W	FAULT - enable FAULT interrupt

TABLE 6-4. SIMR - INTERRUPT MASK REGISTER

6.3.4 SEQSTS - Sequencer Status (03)

The following status bits are further clarified in later registers and sections. These bits can be used to check what sequencer operation is taking place.

REGISTER	BIT	DIR	DEFINITION
03	7	R	DATFLD - data field active. This bit means that the either the BUFF or the NOXFER bit is now active from the control store.
03	6	R	ECCEN - checksum calculation active. The WD10C01A is now calculating the checksum. This status line usually encompasses the ID or data field and checksum bytes, and is active during both read and write.
03	5	R	LAST - The LAST bit is now active from the control store.
03	4	R	ID - The ID bit is now active from the control store.
03	3	R	CHK - The CHK bit is now active from the control store. The WD10C01 is now processing the checkbytes or syndromes for the CRC or ECC.
03	2	R	WAIT - The wait sequencer is waiting for an event such as index, sector mark, address mark, or byte sync.
03	1	R	AMDET - Address mark detect. This is the raw AMDET pin input. This pin can be used as an extra input bit in designs (such as ST506) that do not require this function.
03	0	R	SEQOUT - The SEQOUT bit is now active from the control store.

TABLE 6-5. SEQSTS - SEQUENCER STATUS REGISTER

6.3.5 PYC - PORT Y Configuration (03)

This port is used to configure each port Y bit for input or output. This register is cleared to zero by reset, which causes all port Y pins to become inputs.

REGISTER	BIT	DIR	DEFINITION
03	3	W	PY3DIR - bit 3 direction: 0 = in; 1 = out
03	2	W	PY2DIR - bit 2 direction: 0 = in; 1 = out
03	1	W	PY1DIR - bit 1 direction: 0 = in; 1 = out
03	0	W	PY0DIR - bit 0 direction: 0 = in; 1 = out

TABLE 6-6. PYC - PORT Y CONFIGURATION (03)

6.3.6 Control Store Windows

The heart of the WD10C01A is its control store memory, which is organized as 32 instruction words of 28 bits each. Each 28 bit instruction is divided into three 8 bit parts: the control byte, the value byte, and the count byte; and one 4 bit part: the error control byte. The window registers are used to access these bytes. The control store address is specified by writing to the START register. Any write to a control store window register causes the START register to automatically increment to the next address to facilitate loading.

The contents of the control store are not affected by reset.

6.3.6.1 CSERR - Control Store Error Control Byte Window (04)

The transition of DAC from false to true, together with WG (in the control byte of the control store) or RCMP (read compare enable in the SEQCTL register), causes a one byte prefetch from the buffer. If an immediate fill character is used to specify the format data field or read compare byte (see below), and DAC is used to select the ECC for the data field, prefetch REQA signals are generated anyway.

REGISTER	BIT	DIR	DEFINITION
04	3	R/W	FAIL - Enable error failure. Setting this bit to one causes a command stop if an error is detected while executing the current control store instruction. The error can be CRC/ECC error, data miscompare error or a parity error during write operation.
04	2	R/W	RTY - Enable read error retry. This bit is valid only during read. Setting this bit to one causes a sector retry (see below) if a read error is detected while executing the current control store instruction. An example of the use of this bit is to cause a retry on an ID field miscompare.
04	1	R/W	DAC - Data field active. Set this bit to one when the current control store instruction involves a data field operation. This signal is used to select the data field checksum (RS-ECC) and to control data prefetch. When this bit is zero an ID field operation is assumed, and the ID field checksum (CRC) is selected.
04	0	R/W	SEQOUT - user defined output. This is tied to the SEQOUT output pin through some delays which align the signal to the byte boundary of the read or write serial data. This output can be used to control an external ECC circuit, such as a Reed-Solomon code circuit.

TABLE 6-7. CSERR-CONTROL STORE ERROR CONTROL BYTE WINDOW

6.3.6.2 CSCTL - Control Store Control Byte Window (05)

REGISTER	BIT	DIR	DEFINITION
05	7	R/W	SVSEL - value byte select. This bit selects the use of the value byte, which can be either immediate data (SVSEL = 0) or a select for data source or destination (SVSEL = 1).
05	6	R/W	CWSEL - count byte select. The bit selects the use of the count byte, which can be either an immediate byte count (CWSEL = 0) or to specify an external condition to wait for (CWSEL = 1).
05	5	R/W	WG - write gate output. This is tied directly to the WG output pin.
05	4	R/W	RG - read gate output. This is tied to the retry logic, which is then tied to the RG output pin.
05	3	R/W	AM - address mark enable output. This is tied to the AMC register (see below) which generates the AMENA signal.
05	2	R/W	CMPEN - compare enable. This signal is used to indicate that the bytes of the currently selected data source are to be compared with incoming serial data (ID, marker bytes, buffer data).
05	1	R/W	SKPEN - jump to SKIP address at end of the current instruction. This causes an absolute jump to the SKIP register address when the current control store instruction is finished. Typically, this is used to set up a read and write program in the control store with a common ID search routine. (See later examples and SKIP register definition.)
05	0	R/W	JMPEN - jump to LOOP address at end of the current instruction. This causes a conditional jump to the LOOP register if the sector count (SECCNT) is not zero. If SECCNT is zero, the next sequential instruction is executed. Typically, this is used to specify the end of a sector, and tells the sequencer to go to the LOOP register address to operate on the next sector.

TABLE 6-8. CSCTL - CONTROL STORE BYTE WINDOW (05)

6.3.6.3 CSVAL - Control Store Value Byte Window (06)

The use of the value byte depends on the state of the SVSEL bit of the control byte. When SVSEL is zero, the value byte specifies actual immediate data, like address mark, gap, and PLL sync bytes. When SVSEL is one, the value byte becomes an encoded bit field that enables the correct data source or destination. Both uses are shown below.

To get large sector sizes, multiple control store instructions are used. For example, for a 1024 byte sector size, use four instructions with 256 byte count fields. With this scheme, the last instruction must be flagged for error correction and write prefetch purposes. The LAST bit must be set with the BUFF or NOXFER bit to ensure proper operation.

REGISTER	BIT	DIR	DEFINITION
06	7-0	R/W	VALUE7-0 (actual value for field)

TABLE 6-9. SVSEL of CONTROL BYTE ZERO

REGISTER	BIT	DIR	DEFINITION
06	7	R/W	BUFF - data buffer. This bit causes data to be transferred to (disk read) or from (disk write or read compare) the disk data buffer. The leading edge of BUFF causes a decrement of the SECCNT register, and increments the ID write register counters (see below).
06	6	R/W	NOXFER - no data transfer. This bit is used when an ECC/CRC verify on the data field with no buffer data transfer is being performed. This bit is set INSTEAD of the BUFF bit, and affects the SECCNT and ID registers in the same way as the BUFF bit.
06	5	R/W	LAST - last data buffer xfer control store instruction. Long data fields (greater than 256 bytes) are specified by using multiple control store instructions (2 for 512 bytes, 4 for 1024 bytes, etc.). When the control store instruction is the last instruction of the data field specifiers, the LAST bit must be set to flag this. This only applies to data buffer transfers. LAST is set in ADDITION to BUFF or NOXFER. The CSCNT byte must be set to at least 01 when this bit is used.
06	4	R/W	R/W ID - ID registers. On ID read, the incoming ID field from the disk is compared against the ID write registers and written at the same time to the ID read registers. On write (format), the data source is the ID write registers.
06	3	R/W	CHK - checksum field. On read, this starts the check for a correct checksum. On write, this causes the checksum shift register to be gated into the NRZ0 data. In either case, the calculation is halted at the end of this instruction. The DAC bit in CSERR window selects the appropriate checksum automatically.

TABLE 6-10. SVEL of CONTROL BYTE ONE

6.3.6.4 CSCNT - Control Store Count Byte Window (07)

The use of the count byte depends on the state of the CWSEL bit of the control byte. When CWSEL is zero, the count byte specifies the actual length of that field in bytes. When CWSEL is one, the count byte becomes an encoded bit field that specifies a condition to wait for before proceding. Both uses are shown below.

The count value is set to the actual number of bytes to do minus one. Therefore, 00 denotes a one byte field, and FF a 256 byte field.

REGISTER	BIT	DIR	DEFINITION
07	7-0	R/W	COUNT7-0 (actual size of field - 1)

TABLE 6-11. CWSEL of CONTROL BYTE ZERO

REGISTER	BIT	DIR	DEFINITION
07	7	R/W	WDAM - Wait for data address mark (ST412 ONLY). This bit causes the WD10C01A to pause until a data address mark is detected at the AMDET input. Bits 6-0 specify a timeout count that is the maximum number of byte times from the end of the ID field to the data address mark. The value field is used to specify the data pattern to compare against for byte sync.
07	6	R/W	WIAM - Wait for ID address mark (ST412 ONLY). This bit causes the WD10C01A to pause until an ID address mark is detected at the AMDET input. The value field is used to specify the data pattern to compare against for byte sync.
07	5	R/W	WIX - Wait for index. Pauses until index is detected at the INDEX input.
07	4	R/W	WSM - Wait for sector mark. Pauses until sector mark is detected at the SECTOR input.
07	0	R/W	STOP - Stop immediate. This bit causes the command sequencer to immediately turn off all control outputs and return to the stopped state.

TABLE 6-12. CWSEL of CONTROL BYTE ONE

6.3.6.5 Wait Condition Sequences

The following sequences are performed on the above wait conditions to ensure proper error handling:

WDAM:

Wait for AMDET. If the byte count is exceeded, a sync error is recorded, and (if the control store FAIL bit is set) the command halts. When AMDET is detected correctly, the sequencer waits sixteen bit times for the sync byte in the value byte to be matched. The bit counter is decremented on each bit while the AMDET signal is active. If this bit count is exceeded, this is also a sync error. When a sync error occurs, the sequencer will stop or retry as defined by the control store FAIL and RTY bits. Checksum calculation starts when the sync byte is detected, and the sync byte is included in the calculation.

WIAM:

Wait for AMDET. Since ID address marks could be found anywhere, there is no byte count, and the CPU must perform its own timeout. However, after AMDET is detected, the sequencer waits sixteen bit times for the sync byte in the value byte to be matched. The bit counter is decremented on each bit while the AMDET signal is active. If this bit count is exceeded, this is considered a sync error, and (if the control store RTY bit is set) a retry is performed (ID retry is discussed in a later section). Checksum calculation starts when the sync byte is detected, and the sync byte is included in the calculation.

WIX and WSM:

The signal (index or sector mark) is waited on forever. The CPU must perform its own timeout and issue the KILL bit to the SEQCTL register to stop the command (see below). To do a wait for either index or sector mark (typical on hard sector drives), set both WIX and WSM.

6.4 DEVICE CONTROL GROUP

The device control group is used to set and read port X, Y, and Z bits for drive control. It is also used to execute data transfer commands with the sequencer, and correct ECC errors.

6.4.1 PORTX - PORTX Output Bits (08)

This register is cleared to zero by reset. The state of the output bits may be read back, allowing for read/modify/write operation.

REGISTER	BIT	DIR	DEFINITION
08	7-0	R/W	PX7-0 (direct to output pins)

TABLE 6-13. PORTX OUTPUT BITS (08)

6.4.2 PORTY - PORT Y I/O Bits (09)

The direction of each bit is controlled by the Port Y Control Register (03). If a particular bit is set for input, then the state of the external pin is read by a read of this port. If the bit is set for output, then the last state written to that bit is read (same as Port X). Writing to this register does not affect bits configured for input. Reset sets all bits to input, but does not affect the output latched data.

REGISTER	BIT	DIR	DEFINITION
09	3-0	R/W	PY3-0 (direct to I/O pins)

TABLE 6-14. PORTY I/O BITS (09)

6.4.3 PORTZ - PORT Z INPUT BITS (0A)

REGISTER	BIT	DIR	DEFINITION
0A	5-0	R	PZ5-0 (direct from input pins)

TABLE 6-15. PORTZ INPUT BITS (0A)

6.4.4 AMC - Address Mark Control (0A)

The AMC register defines during which bit times the AMENA signal is active. When AM is set in the control store control byte of the current instruction, the AMENA signal will be active during the bit times specified in this register. This register is not affected by reset. Note that the bits in this register are ordered backwards from the data bus numbering; i.e., writing 01 to this register will turn on AMENA when bit 7 of the serial data stream is active on NRZO.

REGISTER	BIT	DIR	DEFINITION
0A	7-0	W	Address mark bit control bit 0-7

TABLE 6-16. AMC - ADDRESS MARK CONTROL (0A)

6.4.5 SEQCTL - Sequencer Control Register (0B)

REGISTER	BIT	DIR	DEFINITION
0B	7	W	RGERLY - read gate early bit. This bit controls the timing of RG signal. If the bit is set to zero, the RG signal is extended automatically until the ECC/CRC calculation is finished. Setting this bit to one will disable this feature.
0B	3	W	IXMASK - index interrupt mask. This bit is used with the SMMASK bit to select the conditions for the SM$IX interrupt (see table below).
0B	2	W	SMMASK - sector mark interrupt mask (see table below).
0B	1	W	RCMP - enable read compare. This bit MUST be set when performing a read data compare command with the data buffer. It is used to change the buffer access from write buffer to read buffer.
0B	0	W	KILL - immediately kill the currently executing command. The sequencer will stop within three byte times. This bit must be asserted for at least 2 bytes time.
0B	5	R	ECCERR - checksum error. An ECC or CRC error has been detected. This bit is valid when the sequencer is stopped. If the control bit IGNERR in ECCCTL is turned on, this status bit will always be zero and the sequencer will continue its operation ignoring the error condition.
0B	4	R	IDERR - ID checksum error. A CRC ID field error occurred during the previous ID field read. This condition is latched when a checksum error causes an ID retry, and is cleared at the start of the next ID field read (ID false to true transition).
0B	3	R	PTYERR - parity error. A parity error during a transfer from the data buffer to the WD10C01A occurred during the previous command. If FAIL bit is set in the current CS instruction, the sequencer will stop its operation at the end of current instruction and WG output will be deasserted. This bit is valid only after the sequencer is stopped.
0B	2	R	SYNCER - sync search error. The search for a data field marker byte or sync byte failed. This bit is valid when the sequencer is stopped.
0B	1	R	CMPERR - compare data error. A field that was compared against some specified data source compared incorrectly. This bit is valid when the sequencer is stopped.

TABLE 6-17. SEQCTL - SEQUENCER CONTROL REGISTER (0B)

This register is not affected by reset. The IXMASK and SMMASK select the conditions for the SM$IX interrupt. Note that these mask bits are used to select only the source, and do not affect or enable the external interrupt signal. The table below defines the use of the SM$IX source mask bits:

SMMASK	IXMASK	SM$IX set true on leading edge of:
0	0	nothing
0	1	INDEX
1	0	SECTOR
1	1	INDEX OR SECTOR

6.4.6 START - Sequencer Start Address (0C)

The START register is not affected by reset. This register is actually two devices: the START holding register, and the control store address counter. When the CPU writes to this port, the data bus value is latched into both the holding register and the address counter. The holding register is affected only by CPU writes, but the counter is incremented or reloaded by several different events. The START register is used for the following functions:

1. The START register specifies the starting address in the control store for the program loaded there. When the CPU writes to the SECCNT register (see below), and the sequencer is stopped, the sequencer loads the contents of the holding register into the address counter and starts with the instruction at that location.

2. Reading this port gives the current contents of the control store address counter. Reading the counter while the sequencer is running indicates which control store instruction is currently being executed. It is recommended that the CPU 'debounce' this port by reading the START register until the same value is read twice. This prevents erroneous values being read at transition times. Reading the counter when the sequencer is stopped indicates where in the control store the condition causing the last halt occurred. This can be used to determine in which instruction an ECC or other fatal error occurred.

3. The START register is used to specify the current address for control store window access. See control store windows above. The control store address counter is automatically incremented after any write to a control store window register (CSERR, CSCTL, CSVAL, or CSCNT).

4. Writing to the START register clears error conditions. When a read error occurs, causing the command to halt (see FAIL bit in CSERR above), the error status is latched in the SEQCTL register. A write to the START register clears ECCERR, I0E-I4E, CERR, EERR, SYNCER, CMPERR, and also PTYERR (which does not cause a halt). This must be performed prior to issuing any new commands. If SECCNT is non-zero, the sequencer will start as soon as the error is cleared.

While the sequencer is running, the control store address counter is the program counter, and points at the current instruction being executed. The address in the counter can be changed by the following events during program execution:

1. At the end of an instruction that has the SKPEN bit set, the address counter is loaded with the contents of the SKIP register.

2. At the end of an instruction that has the JMPEN bit set, if the SECCNT register is not zero (i.e., more sectors to do), the address counter is loaded with the contents of the LOOP register. If SECCNT is zero, the address counter is incremented and the next sequential instruction is executed.

REGISTER	BIT	DIR	DEFINITION
0C	4-0	R/W	START4-0

TABLE 6-18. START - SEQUENCER START ADDRESS (0C)

3. If an instruction has the RTY bit set, and an error flag is currently set (ECCERR, CMPERR, or SYNCER), a retry occurs and the address counter is loaded with the contents of the LOOP register.

4. If a program halts due the STOP bit being set (i.e., the normal end of the program with SECCNT zero), and the CPU writes to the SECCNT register with more blocks to do before it detects the stopped condition, the sequencer will restart using the current value of the START holding register. This prevents erroneous restarts from occurring.

5. In all other cases, the control store address counter is incremented and the next sequential instruction is executed.

6.4.7 LOOP - Sequencer Loop Address (0D)

The LOOP register specifies the address to set the START value to at the end of a control store instruction that has the JMPEN bit set in the control byte. This also happens when an ID retry occurs (see below). The use of the LOOP register is based on the idea that all sector operations are sequential in nature, and that when the operation is complete, a single jump back to the start of the sequential sector operation is all that is needed. This register is not affected by reset.

REGISTER	BIT	DIR	DEFINITION
0D	4-0	W	LOOP4-0 (address to loop to in loop)

TABLE 6-19. LOOP - SEQUENCER LOOP ADDRESS (0D)

6.4.8 ECCCTL - Error Correction Control Register (0E)

CRCSET and ECCCLR must be set high and then low to complete the preset or clear operation. All bits in this register are cleared to zero upon reset time.

REGISTER	BIT	DIR	DEFINITION
0E	5	W	ECCCLR - clear CRC and ECC shift register. Writing one to this register causes the CRC and ECC shift register to be held in the clear (all bits zero) state. The CPU must then write zero to this bit to complete the clear pulse.
0E	4	W	CRCSET - preset CRC shift register. Writing one to this register causes the CRC shift register to be held in the preset (all bits one) state. The CPU must then write zero to this bit to complete the preset pulse.
0E	3	W	CRCNIT - CRC shift register initial state. This bit selects whether to start the CRC shift register with all zeros (CRCNIT = 0) or all ones (CRCNIT = 1) when starting checksum calculation.
0E	2	W	IGNERR - ignore CRC/ECC error. Forces ECCERR bit in the SEQCTL register to zero, and causes the read error logic to ignore this error by continuing with its operation. The status bit EERR/CERR in the ECCS register is not affected by this control bit and will be set on error.
0E	1	W	DISPTY: disable parity checking. Setting this bit to one forces the PTYERR bit in the SEQCTL register to zero. Even if the FAIL bit in the current CS instruction is set, the sequencer will continue its operation normally on parity error.

TABLE 6-20. ECCCTL - ERROR CORRECTION REGISTER (0E)

6.4.9 SECCNT - Sector Count Register (0F)

The sector count register is used to specify the number of iterations to perform the operation programmed into the control store. Writing any non-zero value to the SECCNT register causes the sequencer to start, so therefore the range of possible sector counts is from 1 to 255. Writing a zero to SECCNT during the data field will cause the sequencer to halt at the end of the current sector. The sector count is automatically decremented at the start of the data field, after the byte sync or address mark character(s) have been detected (leading edge of BUFF or NOXFER). The SECCNT register can be written to at any time except the start of the data field.

This register is cleared to zero by reset, or when the KILL bit in the SEQCTL register is set. It is NOT cleared by a halt on error, so that the sector in error can be determined.

REGISTER	BIT	DIR	DEFINITION
0F	7-0	R/W	Sector count value

TABLE 6-21. SECCNT - SECTOR COUNT REGISTER (0F)

6.4.10 ECCP- ECC Parameter Register (10)

REGISTER	BIT	DIR	DEFINITION
10	3	W	SYNCECC - include sync byte in the ECC calculation. This bit is initialized to one upon reset. If this control bit is set to one, the ECC calculation begins with the first data sync byte. Otherwise, the first data sync byte is excluded from the ECC calculation.
10	2	W	WSYNCCRC - include sync byte in the CRC calculation. This bit is initialized to one upon reset. If this control bit is set to one, the CRC calculation begins with the first ID sync byte. Otherwise, the first data sync byte is excluded from the CRC calculation.
10	1	W	DEG6/5 - RS ECC degree control bit. This bit is initialized to zero upon reset. If this bit is set to zero, degree 5 polynomial is selected, otherwise degree 6 will be used.
10	0	W	WIFS5/3 - Interleave select. This bit is initialized to zero upon reset. Setting this bit to one will select five way interleave format, otherwise three way format will be used.

TABLE 6-22. ECCP - ECC PARAMETER REGISTER (10)

6.4.11 ECCS - RS-ECC Status Register (11)

REGISTER	BIT	DIR	DEFINITION
11	6	R	EERR - ECC error detected. This bit is set whenever an ECC error is detected in any one of the interleaves. At least one of the status bits I4E - I0E will also be set. This bit is cleared to zero after reset and before another operation is started. This bit is not affected by the control bit IGNERR, which prevent the status ECCERR from being set.
11	5	R	CERR - CRC error detected. This status bit is set whenever a CRC error is detected in the ID field. This bit is cleared upon reset. The control bit IGNERR does not affect this status bit.
11	4	R/W	I4E - ECC error in interleave 4. This bit is set only when an ECC error is detected in the interleave 4. The microprocessor can read the syndrome bytes from this interleave only when this status bit is set. This status bit is cleared upon reset. It also be cleared by writing a zero into this bit.
11	3	R/W	I3E - ECC error in interleave 3. This bit is set only when an ECC error is detected in the interleave 3. The microprocessor can read the syndrome bytes from this interleave only when this status bit is set. This status bit is cleared upon reset. It also be cleared by writing a zero into this bit.
11	2	R/W	I2E - ECC error in interleave 2. This bit is set only when an ECC error is detected in the interleave 2. The microprocessor can read the syndrome bytes from this interleave only when this status bit is set. This status bit is cleared upon reset. It also be cleared by writing a zero into this bit.
11	1	R/W	I1E - ECC error in interleave 1. This bit is set only when an ECC error is detected in the interleave 1. The microprocessor can read the syndrome bytes from this interleave only when this status bit is set. This status bit is cleared upon reset. It also be cleared by writing a zero into this bit.
11	0	R/W	I0E - ECC error in interleave 0. This bit is set only when an ECC error is detected in the interleave 0. The microprocessor can read the syndrome bytes from this interleave only when this status bit is set. This status bit is cleared upon reset. It also be cleared by writing a zero into this bit.

TABLE 6-23. ECCS - RS-ECC STATUS REGISTER (11)

6.4.12 SPORT - Syndrome Port (12)

The microprocessor reads the syndrome bytes for each interleave through this port. The WD10C01A automatically transfers the syndromes of the next interleave in error after all the syndromes in the current interleave are read. The microprocessor must read (interleave number * ECC degree) times from this port to complete a syndrome transfer from an interleave. The syndrome bytes are transferred starting with the **highest** byte from the **lowest** interleave number. Only the syndromes from an interleave in error are transferred. If the microprocessor clears the error flag from an interleave, the syndromes from that interleave cannot be read, but the content of the syndrome registers are not destroyed. Those can be read by reseting the error flag to one.

The syndrome bytes are valid only when sequencer is stopped. The syndrome registers are cleared upon reset.

6.4.13 TEST - Test Register (16)

This register is intended for test purpose in the manufacturing and must not be used in normal operations. It is described here only for reference.

There are three test functions implemented in this register. First, writing into this register with any data, will set the OSC and CPUCLK outputs in a predetermined state. During the write cycle, the OSC output is set to 0 level and the CPUCLK output is set to a 1 level.

Second, the microprocessor can write 080H into this register to disable the output signal WG. This signal will remain inactive until the microprocessor writes a 00H into the register.

Third, the microprocessor can write 0C0H into the register to increment the ID registers. Subsequently, the microprocessor must write 00H, before it can continue to increment the registers again. The output WG is also disabled during the test operation.

REGISTER	BIT	DIR	DEFINITION
12	7-0	R	SYNDR7-0 - Syndrome bit7-bit0.

TABLE 6-24. SPORT - SYNDROME PORT (12)

6.4.14 SKIP - Skip Address Register (17)

This register is not affected by reset. The SKIP register is used to perform an absolute jump to the location specified at the completion of a control store instruction that has the SKPEN bit set to one. This can typically be used to define whether the current operation is to be a sector read or a sector update write. Consider the following generalized control store program that has three parts: ID search, read data field, and write data field.

When the SKIP register is set to address 05, the WD10C01A will perform a sector read operation. When the SKIP register is set to address 0C, the WD10C01A will perform a sector write operation. A more detailed example can be found in a subsequent section of this document.

REGISTER	BIT	DIR	DEFINITION
17	4-0	W	SKIP4-0

TABLE 6-25. SKIP - SKIP ADDRESS REGISTER (17)

ADDRESS	CONTROL STORE OPERATION
00	ID SEARCH
01	ID SEARCH
02	ID SEARCH
03	ID SEARCH
04	ID SEARCH (SKPEN bit set)
05	READ DATA FIELD
06	READ DATA FIELD
07	READ DATA FIELD
08	READ DATA FIELD
09	READ DATA FIELD
0A	READ DATA FIELD
0B	STOP
0C	WRITE DATA FIELD
0D	WRITE DATA FIELD
0E	WRITE DATA FIELD
0F	WRITE DATA FIELD
10	WRITE DATA FIELD
11	WRITE DATA FIELD
12	STOP

TABLE 6-26. SKIP CONTROL STORE EXAMPLE

6.5 ID REGISTER GROUP

The eight ID registers (ID0 - ID7) are used to set the ID field during format and read/write operations. Writing to the ID registers sets the field to search for, or to write during format. These registers are refered to as the ID write registers. The first four ID write registers are set up as a 32-bit counter, and they automatically increment at the start of the data field. The second four are simple registers and are intended for use as flag and defect indicators.

The ID read registers contain the last ID field read from the media (valid when IDFULL in SISR is true). These registers must be read when the sequencer is NOT reading an ID field, or else the CPU will not read the correct value.

REGISTER	BIT	DIR	DEFINITION
18	7-0	R/W	ID0 bits 7-0 (counter MSbyte)

TABLE 6-27. ID0 - ID REGISTER 0 (18)

REGISTER	BIT	DIR	DEFINITION
19	7-0	R/W	ID1 bits 7-0 (counter)

TABLE 6-28. ID1 - ID REGISTER 1 (19)

REGISTER	BIT	DIR	DEFINITION
1A	7-0	R/W	ID2 bits 7-0 (counter)

TABLE 6-29. ID2 - ID REGISTER 2 (1A)

REGISTER	BIT	DIR	DEFINITION
1B	7-0	R/W	ID3 bits 7-0 (counter LSbyte)

TABLE 6-30. ID3 - ID REGISTER 3 (1B)

REGISTER	BIT	DIR	DEFINITION
1C	7-0	R/W	ID4 bits 7-0 (flag)

TABLE 6-31. ID4 - ID REGISTER 4 (1C)

REGISTER	BIT	DIR	DEFINITION
1D	7-0	R/W	ID5 bits 7-0 (flag)

TABLE 6-32. ID5 - ID REGISTER 5 (1D)

REGISTER	BIT	DIR	DEFINITION
1E	7-0	R/W	ID6 bits 7-0 (flag)

TABLE 6-33. ID6 - ID REGISTER 6 (1E)

REGISTER	BIT	DIR	DEFINITION
1E	7-0	R/W	ID7 bits 7-0 (flag)

TABLE 6-34. ID7 - ID REGISTER 7 (1F)

6.6 DEVICE PROGRAMMING

6.6.1 Initialization

1. Write one and then zero to the SRST bit of the SRESET register to complete the device reset sequence.

2. Write the remainder of the bits of the SRESET register to the CPU and OSC clock speeds, and ID counter size and data request timing.

3. Clear all interrupts that can be cleared by writing 0FFH to the SISR (some may still be set because they are level true). Write the initial mask to the SIMR.

4. Configure port Y.

5. Configure the address mark control bits using the AMC register.

6. Set up the ECC by programming the ECCCTL and ECCP registers. Set CRCNIT in the ECCCTL register to the appropriate value for a zero seed or a one's seed.

7. Load the control store program into the control store.

6.6.2 Command Programming

1. Load the control store with the particular instructions appropriate for the command desired (format, read, write, etc.), if necessary.

2. Set the START, LOOP, and SKIP registers to the appropriate values for the control store program.

3. Write the number of sectors to do to SECCNT. This also starts the command sequencer.

4. Clear the interrupt status bits, and set the mask.

5. Wait for SEQSTP. Check the SEQCTL and ECCS status bits for an error.

6.6.3 Control Store Programming

There are a few 'tricks' in programming the WD10C01A control store that are not indicated by the discussions of the individual control bits:

READ BYTE SYNC

On formats that use a simple byte sync byte (like ESDI) for ID and data field markers, the search is performed by setting the control byte bits RG and CMPEN, and the count field is set with a maximum byte timeout count. The condition of no byte sync yet found, and RG * CMPEN set, defines this mode. AMDET is not used and has no effect on this operation. Checksum calculation starts when the sync byte is detected, and the sync byte is included in the calculation.

WRITE BYTE SYNC

Write byte sync is used to mark the start of the byte string for which the ECC/CRC checksum is calculated. To do this, set WG and CMPEN in the control byte. The start of the control store instruction with WG and CMPEN set clears the checksum register to the state defined by CRCNIT. The transition to the next instruction begins the checksum calculation. For example, in a ST412 drive the ID field might be defined by the byte string: A1 FE ID ID ID FLAG ECC ECC ECC ECC; with PLL sync before, and gap after. The control store instructions would be coded as follows.

ADDRESS	DATA	COUNT	CONTROL	ERROR
00	00	0B	WG,CMPEN	PLL sync field
01	A1	00	WG,AM	address mark
02	FE	00	WG	address marker
03	ID	02	WG,SVSEL	ID field
04	ID	00	WG,SVSEL	flag byte
05	CHK	03	WG,SVSEL	checksum
06	00	03	WG	pad and splice

TABLE 6-35. WRITE BYTE SYNC EXAMPLE

In the example, control store instruction 00 contains the WG-CMPEN combination that says to begin checksum calculation on instruction 01; therefore, the bytes defined in instructions 01 through 05 are included in the checksum calculation. The calculation is terminated by the CHK value code in instruction 05.

DATA FIELD SIZES

The data field size is set by using multiple control store instructions to build up the size in 256 (or less) increments. Two issues come up with this method:

1) The last data field instruction must be marked to ensure correct buffer data transfer timing and checksum calculation. The LAST bit is used with the BUFF or NOXFER bit to perform this marking.

2) For programming purposes, it is desirable to not have to change the control store significantly when changing sector size. To do this, allocate enough control store instructions to be able to set the largest sector size to be supported. Then, adjust the count fields in all of the instructions to get the desired sector size. For example, if a controller supports 256, 512, and 1024 byte sectors, use the programming shown in the example below:

Rel Addr	Counts for		
	256	512	1024
00	3F	7F	FF
01	3F	7F	FF
02	3F	7F	FF
03	3F	7F	FF

TABLE 6-36. DATA FIELD SIZE EXAMPLE

If the LAST bit is being used as an interrupt, the last instruction can be split into two parts. The second part contains the LAST bit, and can be adjusted to the required time before the end of the sector, since the leading edge of LAST generates the interrupt.

ID SEARCH AND FLAG BYTES

When specifying an ID field, it is desirable to have address bytes that are compared on a search, and flag bytes that are not. To do this, split the ID field in the control store into two separate instructions for address and flag. When performing an ID search, set the CMPEN bit only in the ID address instruction, and not in the ID flag instruction.

DATA CHECKSUM VERIFY

To do a data field ECC or CRC verify only command, set the data field source as NOXFER. No data will be transferred to the buffer.

DATA COMPARE VERIFY

To do a data field compare verify, set the RCMP bit in the SEQCTL register, and set the CMPEN bit in the data field control store instruction. Data will be transferred from the data buffer and compared with the incoming disk data.

FILL GAP TO END OF TRACK

To generate fill data through to the end of the track during format, set the WIX bit in the last control store instruction, and set WG and the fill character. The WD10C01A will fill in gap bytes until index occurs. This also works for gaps to sector marks.

6.6.4 Programming Examples

This section gives programming examples for ST412 format, read, and write commands. The following design parameters are assumed:

1. The ID field is three bytes of address, one byte of flag, and two bytes of CRC.
2. Intersector gaps are 20 bytes of 04EH data, PLL sync fields are 12 bytes of 000H.
3. ID address mark and marker byte are 0A1FEH, data address mark and marker byte are 0A1F8H.
4. Data field is protected through degree six ECC with interleave factor of five. There are 30 bytes of checksum.

The WD10C01A registers are programmed as follows:

SRESET: ID3$4 = 1 (3 bytes of address counter)

6.6.4.1 Format Track Example

ADDRESS	VALUE	COUNT	CONTROL	NOTES
00	00	WIX	CWSEL	start on index
01	4E	13	WG	post index gap
02	00	0B	WG, CMPEN	PLL sync
03	A1	00	WG,AM	address mark
04	FE	00	WG	address mark
05	ID	03	WG,SVSEL	ID address & flag
06	CHK	01	WG,SVSEL	CRC
07	00	02	WG	write splice
08	00	0B	WG, CMPEN	data PLL sync
09	A1	00	WG, AM, DAC	address mark
0A	F8	00	WG, DAC	address mark
0B	BUFF	7F	WG, SVSEL,DAC	data field
0C	BUFF	7F	WG, SVSEL,DAC	data field
0D	BUFF	7F	WG, SVSEL,DAC	data field
0E	BUFF, LAST	7F	WG, SVSEL,DAC	data field
0F	CHK	1D	WG, SVSEL,DAC	ECC
10	00	02	WG,JMPEN,DAC	write splice
11	4E	WIX	WG, CWSEL	pre-index gap
12	00	STOP	CWSEL	stop at end of track
START = 00, LOOP = 01, SKIP = NOT USED				

TABLE 6-37. FORMAT TRACK EXAMPLE CONTROL STORE

Line by line discussion of Format Track Example:

00: This instruction just waits until the leading edge of index. No writing is occurring. If there is no index signal working on the drive, the CPU will have to timeout and issue an abort. The DAC bit is zero to select the checksum for the ID, as specified by the SRESET register.

01: This instruction is the standard 4E gap from index to the start of the first sector. This instruction is also the intersector gap, because after the data field write splice on instruction 11 is written, the WD10C01A will jump to this address specified by the LOOP register.

02: This instruction is the PLL sync field for the ID field. The WG - CMPEN combination also marks the start of the CRC calculation starting with instruction 03.

03: This is the first address mark byte for the ID field. The AM bit generates AMENA with the AMC register, suppressing the clock bit in the A1 byte.

04: This is the second address mark byte, and is treated as simple immediate data for format purposes.

05: This is the ID address and flag field.

06: ID CRC field. The count field is set to (2-1) bytes for the ID CRC. The end of this instruction also stops the checksum calculation.

07: ID write splice and data PLL sync field. This gap protects the end of the ID field from the start of the data field on later update write commands.

08: Data PLL sync field. The WG - CMPEN combination also marks the start of the ECC calculation starting with instruction 0A. The DAC bit is set here to select the data field checksum, and in this case it also causes a one byte prefetch from the buffer.

09: This is the first address mark byte for the data field. The AM bit generates AMENA with the AMC register, suppressing the clock bit in the A1 byte.

0A: This is the second address mark byte, and is treated as simple immediate data for format purposes.

0B-0D: These are the first three instructions that define the sector data field. The data field is split into four control instructions so that switching between sector sizes will not require reordering the control store data (see above). The example shows a 512 byte sector.

0E: The last instruction of the data field marks the end of the data field using the LAST bit set with BUFF.

0F: Data ECC field. ECC degree six with interleave factor of five is used, the count field is set to (30-1) bytes. The end of this instruction also stops the checksum calculation.

10: Data field write splice. This instruction pads the end of the data field, making sure that the checksum is not lost by the drive. The JMPEN bit is also set in this instruction, meaning that the next instruction to be accessed will be the one addressed by the LOOP register, in this case 01. This happens only if SECCNT is not zero. If SECCNT is zero, the next control instruction is 11.

11: After the last sector, SECCNT is zero. After instruction 10 is done, the next instruction will be this one instead of instruction 01 (LOOP register). This instruction writes the 4E gap until index.

12: The STOP bit causes the sequencer to shut down immediately and turn off all external signals (like WG, etc.).

The CPU performs the FORMAT TRACK command as follows:

1. After setting up the control store and address registers as defined above, write the total sectors per track to the SECCNT register.

2. Write DXFER, FAULT, and SEQSTP true to the SISR register to clear those status bits, and to the SIMR register to enable them.

3. Wait until GINT is true with a timeout in case INDEX is not present on the interface. Check FAULT for error, and abort if true. If DXFER goes true, update the ID write registers with the next ID field (when using non-consecutive, i.e., not 1:1 interleave).

4. Repeat step 3 for all sectors on the track.

5. After the last sector, wait for SEQSTP to be true, indicating the end of the command.

6.6.4.2 Read Sector Example

ADDRESS	VALUE	COUNT	CONTROL	NOTES
00	A1	WIAM	RG,CWSEL, RTY	address mark search
01	FE	00	RG,CWSEL, RTY	ID marker byte
02	ID	02	RG, SVSEL, CMPEN	ID address
03	ID	00	RG, SVSEL	ID flag
04	CHK	01	RG, SVSEL	CRC
05	00	03	RTY	allow ID retry
06	A1	WDAM (1F)	RG, CWSEL, DAC, FAIL	address mark search
07	F8	00	RG, CWSEL, DAC, FAIL	data marker byte
08	BUFF	3F	RG, SVSEL, DAC	data field
09	BUFF	3F	RG, SVSEL, DAC	data field
0A	BUFF	3F	RG, SVSEL, DAC	data field
0B	BUFF, LAST	3F	RG, SVSEL,DAC	data field
0C	CHK	ID	RG, SVSEL,DAC	ECC
0D	00	02	JMPEN,DAC, FAIL	end of sector
0E	00	STOP	WG, SVSEL,DAC	stop at end of read
START = 00, LOOP = 00, SKIP = NOT USED				

TABLE 6-38. READ SECTOR EXAMPLE CONTROL STORE

Line by line discussion of Read Sector example:

00: This is the first instruction of the read sector command. The WIAM bit tells the WD10C01A to search for an ID address mark byte. The WD10C01A will not timeout, so the CPU will have to abort after some period of time, if necessary. The DAC bit is zero during the ID field to select the ID checksum. The RTY bit is set so that if a read error (in this case, no sync match after AMDET true) occurs, a retry will be performed.

01: This tells the WD10C01A to verify the ID marker byte. If it does not compare exactly, an ID retry occurs (see below) because the RTY bit is set.

02: This is the ID address field. The CMPEN bit causes a compare of the ID write registers with the incoming ID field. The incoming ID is also written to the ID read registers.

03: This is the ID flag field. This control store instruction is separate from the ID address field because the flag byte is not compared with the ID write register. It is still written to the ID read register.

04: ID CRC field. The count field is set to (2-1) bytes for the ID CRC. This instruction switches the checksum shift register into check mode.

05: This instruction is both a pad over the write splice and a check for an ID retry. The ID compare status and checksum error status are latched

and held, and the RTY bit is now set, allowing the checking of this status. An ID retry occurs if the ID did not match, or if there was a checksum error. The checksum error is latched into the IDERR bit for future reference. We waited until this instruction to check for an error so that the ID read registers could be loaded with this ID field.

06: The WDAM bit tells the WD10C01A to look for the data address mark. The (1F) indicates the byte count that is loaded into the byte count. This value is the maximum number of byte times that the WD10C01A will look for the address mark. This prevents locking up on a subsequent data field address mark. An error here causes an immediate halt, with SYNCER set in the SEQCTL register, because the FAIL bit is set.

07: This is the data marker byte. The CMPEN bit indicates that the byte must compare exactly with the immediate data byte. An error here causes an immediate halt, with SYNCER set in the SEQCTL register, because the FAIL bit is set.

08-0A: These are the first three instructions that define the sector data field. The data field is split into four control instructions so that switching between sector sizes will not require rearranging the control store data (see above). The example shows a 256 byte sector. On ECC verify commands, change BUFF to NOXFER. On compare verify commands, set BUFF, the CMPEN bit in the control byte, and RCMP in the SEQCTL register.

0B: The last instruction of the data field marks the end of the data field using the LAST bit set with BUFF. LAST must be used for BUFF or NOXFER.

0C: Data ECC field. ECC degree six with interleave factor of five is used, the count field is set to (30-1) bytes. This instruction switches the checksum shift register into check mode.

0D: The purpose of this instruction is to turn off RG, resetting any external data decoder circuits. The JMPEN bit is also set in this instruction, meaning that the next instruction to be accessed will be the one addressed by the LOOP register, in this case 00. This happens only if the SECCNT register is not zero. If SECCNT is zero, the next instruction is 12. The FAIL bit is also set, causing the checksum status to be checked, and if there was an error, the command stops, with ECCERR set in the SEQCTL register.

0E: After the last sector, the SECCNT register is zero. After instruction 0D is done, the next instruction will be this one instead of instruction 00 (LOOP register). This instruction stops the command immediately.

The CPU performs the READ SECTOR command as follows:

1. After setting up the control store and address registers as defined above, write the sector count to the SECCNT register to start the transfer.

2. Write FAULT, IDFULL, and SEQSTP true to the SISR register to clear those status bits, and to the SIMR register to enable them.

3. Wait until GINT is true with a timeout in case INDEX is not present on the interface. Check FAULT for error, and abort if true. If IDFULL is true, perform any checks on the value in the ID FIFO. If SEQSTP is true, make sure that no error occurred that must be serviced. Clear the status serviced.

6.6.4.3 Write Sector Example

ADDRESS	VALUE	COUNT	CONTROL	NOTES
00	A1	WIAM	RG,CWSEL, RTY	address mark search
01	FE	00	RG,CMPEN, RTY	ID marker byte
02	ID	02	RG, SVSEL, CMPEN	ID address
03	ID	00	RG, SVSEL	ID flag
04	CHK	01	RG, SVSEL	CRC
05	00	02	RTY	wait past splice
06	00	0B	WG, CMPEN, DAC	PLL sync
07	A1	00	WG, AM, DAC	address mark
08	F8	00	WG, DAC	data marker byte
09	BUFF	FF	WG, SVSEL,DAC	data field
0A	BUFF	FF	WG, SVSEL,DAC	data field
0B	BUFF	FF	WG, SVSEL,DAC	data field
0C	BUFF, LAST	FF	WG, SVSEL,DAC	data field
0D	CHK	1D	WG, SVSEL,DAC	ECC
0E	00	02	WG,JMPEN,DAC	write splice
0F	00	STOP	CW SEL	stop at end of cmd
START = 00, LOOP = 00, SKIP = NOT USED				

TABLE 6-39. WRITE SECTOR EXAMPLE CONTROL STORE

Line by line discussion:

00: This is the first instruction of the write sector command. The WIAM bit tells the WD10C01A to search for an ID address mark byte. The WD10C01A will not timeout, so the CPU will have to abort after it times out, if necessary. The DAC bit is zero during the ID field to select the ID checksum. The RTY bit is set so that if a read error (in this case, no sync match after AMDET true) occurs, a retry will be performed.

01: This tells the WD10C01A to verify the ID marker byte. If it does not compare exactly, an ID retry occurs (see below) because the RTY bit is set.

02: This is the ID address field. The CMPEN bit causes a compare of the ID write registers with the incoming ID field. The incoming ID is also written to the ID read registers.

03: This is the ID flag field. This instruction is separate from the ID address field because the flag byte is not compared with the ID write register. It is still written to the ID read register.

04: ID CRC field. The count field is set to (2-1) bytes for the ID CRC. This instruction switches the checksum shift register into check mode.

05: This instruction spaces over the ID field write splice to the start of the data field, protecting the ID checksum in the process. This instruction also performs a check for an ID retry. The ID compare status and checksum error status are latched and held, and the RTY bit is now set, allowing the checking of this status. An ID retry occurs if the ID

did not match, or if there was a checksum error. The checksum error is latched into the IDERR bit for future reference.

06: Data PLL sync field. This instruction is the start of the update write sector data. The WG - CMPEN combination also marks the start of the ECC calculation starting with instruction 07.

07: This is the first address mark byte for the data field. The AM bit generates AMENA with the AMC register, suppressing the clock bit in the A1 byte.

08: This is the data marker byte, and is treated as simple immediate data for write sector purposes.

09-0A: These are the first three instructions that define the sector data field. The data field is split into four control instructions so that switching between sector sizes will not require reordering the control store data (see above). The example shows a 1024 byte sector.

0B: The last instruction of the data field marks the end of the data field using the LAST bit set with BUFF.

0C: Data ECC field. ECC degree six with interleave factor of five is used, the count field is set to (30-1) bytes. The end of this instruction also stops the checksum calculation.

0D: Data field write splice. This instruction pads the end of the data field, making sure that the checksum is not lost by the drive. The JMPEN bit is also set in this instruction, meaning that the next instruction to be accessed will be the one addressed by the LOOP register, in this case 00. This happens only if the SECCNT register is not zero. If SECCNT is zero, the next control instruction is 0E.

0E: After the last sector, SECCNT is zero. After instruction 11 is done, the next instruction will be this one instead of instruction 00 (LOOP register). This instruction stops the command immediately.

The CPU performs the WRITE SECTOR command as follows:

1. After setting up the control store and address registers as defined above, write the sector count to the SECCNT register to start the transfer.

2. Write IDFULL, FAULT, and SEQSTP true to the SISR register to clear those status bits, and to the SIMR register to enable them.

3. Wait until GINT is true with a timeout in case INDEX is not present on the interface. Check FAULT for error, and abort if true. If IDFULL is true, perform any checks on the data in the ID FIFO. If SEQSTP is true, check to see if an error occurred that must be serviced. Clear the status serviced.

6.6.4.4 Read and Write Sector Example

This example makes use of the SKIP register to merge the read and write sector operations into one control store program. Selection between read and write is performed solely by changing the contents of the SKIP register. The control store example shown in the table below is divided into the ID search, read data field, and write data field sections.

ADDRESS	VALUE	COUNT	CONTROL	NOTES
00	A1	WIAM	RG,CWSEL, RTY	address mark search
01	FE	00	RG,CMPEN, RTY	ID marker byte
02	ID	02	RG, SVSEL, CMPEN	ID address
03	ID	00	RG, SVSEL	ID flag
04	CHK	01	RG, SVSEL	CRC
05	00	02	SKPEN, RTY	retry ID
08	00	00	00	wait past splice
09	A1	WDAM(1F)	RG,CWSEL,DAC,FAIL	address marker search
0A	F8	00	RG, SVSEL,DAC	data marker byte
0B	BUFF	3F	RG, SVSEL,DAC	data field
0C	BUFF	3F	RG, SVSEL,DAC	data field
0D	BUFF	3F	RG, SVSEL,DAC	data field
0E	BUFF, LAST	3F	RG,SVSEL,DAC	data field
0F	CHK	1D	RG,SVSEL,DAC	ECC
10	00	02	JMPEN,DAC, FAIL	end of sector
11	00	STOP	CW SEL	stop at end of read
14	00	0B	WG, CMPEN,DAC	PLL sync
15	A1	00	WG, AM,DAC	address mark
16	F8	00	WG, DAC	data marker byte
17	BUFF	FF	WG, SVSEL,DAC	data field
18	BUFF	FF	WG, SVSEL,DAC	data field
19	BUFF	FF	WG, SVSEL,DAC	data field
1A	BUFF, LAST	FF	WG, SVSEL,DAC	data field
1B	CHK	1D	WG, SVSEL,DAC	ECC
1C	00	02	WG,JMPEN,DAC	write splice
1D	00	STOP	CW SEL	stop at end of cmd
START = 00, LOOP = 00, SKIP = 08 for read, 14 for write				

TABLE 6-40. READ AND WRITE SECTOR EXAMPLE CONTROL STORE

Line by line discussion of Read and Write example:

00: This is the first instruction of the ID search. The WIAM bit tells the WD10C01A to search for an ID address mark byte. The WD10C01A will not timeout, so the CPU will have to abort after it times out, if necessary. The DAC bit is zero during the ID field to select the ID checksum. The RTY bit is set so that if a read error (in this case, no sync match after AMDET true) occurs, a retry will be performed.

01: This tells the WD10C01A to verify the ID marker byte. If it does not compare exactly, an ID retry occurs (see below) because the RTY bit is set.

02: This is the ID address field. The CMPEN bit causes a compare of the ID write registers with the incoming ID field. The incoming ID is also written to the ID read registers.

03: This is the ID flag field. This instruction is separate from the ID address field because the flag byte is not compared with the ID write register. It is still written to the ID read register.

04: ID CRC field. The count field is set to (2-1) bytes for the ID CRC. This instruction switches the checksum shift register into check mode.

05: This instruction performs a check for an ID retry. The ID compare status and checksum error status are latched and held, and the RTY bit is now set, allowing the checking of this status. An ID retry occurs if the ID did not match, or if there was a checksum error. The checksum error is latched into the IDERR bit for future reference. Also, the SKPEN bit is set, meaning the next address (assuming no errors occurred) will be the value in the SKIP register, which is 08 for read sector, and 14 for write sector.

READ DATA FIELD

08: This instruction spaces over the ID field write splice to the start of the data field, protecting the ID checksum in the process.

09: The WDAM bit tells the WD10C01A to look for the data address mark. The (1F) indicates the byte count that is loaded into the byte count. This value is the maximum number of byte times that the WD10C01A will look for the address mark. This prevents locking up on a subsequent data field address mark. An error here causes an immediate halt, with SYNCER set in the SEQCTL register, because the FAIL bit is set.

0A: This is the data marker byte. The CMPEN bit indicates that the byte must compare exactly with the immediate data byte. An error here causes an immediate halt, with SYNCER set in the SEQCTL register, because the FAIL bit is set.

0B-0D: These are the first three instructions that define the sector data field. The data field is split into four instructions so that switching between sector sizes will not require reordering the control store data (see above). The example shows a 256 byte sector. On ECC verify commands, change BUFF to NOXFER. On compare verify commands, set BUFF, the CMPEN bit in the control byte, and RCMP in the SEQCTL register.

0E: The last instruction of the data field marks the end of the data field using the LAST bit set with BUFF. LAST must be used for BUFF or NOXFER.

0F: Data ECC field. ECC degree six with interleave factor of five is used, the count field is set to (30-1) bytes. This instruction switches the checksum shift register into check mode.

10: The purpose of this instruction is to turn off RG, resetting any external data decoder circuits. The JMPEN bit is also set in this instruction, meaning that the next instruction to be accessed will be the one addressed by the LOOP register, in this case 00. This happens only if the SECCNT register is not zero. If SECCNT is zero, the next control instruction is 11. The FAIL bit is also set, causing the checksum status to be checked, and if there was an error, the command stops, with ECCERR set in the SEQCTL register.

11: After the last sector, the SECCNT register is zero. After instruction 10 is done, the next instruction will be this one instead of instruction 00 (LOOP register). This instruction stops the command immediately.

WRITE DATA FIELD

14: Data PLL sync field. This instruction is the start of the update write sector data. The WG - CMPEN combination also marks the start of the ECC calculation starting with instruction 15.

15: This is the first address mark byte for the data field. The AM bit generates AMENA with the AMC register, suppressing the clock bit in the A1 byte.

16: This is the data marker byte, and is treated as simple immediate data for write sector purposes.

17-19: These are the first three instructions that define the sector data field. The data field is split into four instructions so that switching between sector sizes will not require reordering the control store data (see above). The example shows a 1024 byte sector.

1A: The last instruction of the data field marks the end of the data field using the LAST bit set with BUFF.

1B: Data ECC field. ECC degree six with interleave factor of five is used, the count field is set to (30-1) bytes. The end of this instruction also stops the checksum calculation.

1C: Data field write splice. This instruction pads the end of the data field, making sure that the checksum is not lost by the drive. The JMPEN bit is also set in this instruction, meaning that the next instruction to be accessed will be the one addressed by the LOOP register, in this case 00. This happens only if the SECCNT register is not zero. If SECCNT is zero, the next control instruction is 1D.

1D: After the last sector, SECCNT is zero. After instruction 1C is done, the next instruction will be this one instead of instruction 00 (LOOP register). This instruction stops the command immediately.

The CPU performs the READ SECTOR command as follows:

1. After setting up the control store and address registers as defined above, write 06 to the SKIP register, and then write the sector count to the SECCNT register to start the transfer.

2. Write IDFULL, FAULT, and SEQSTP true to the SISR register to clear those status bits, and to the SIMR register to enable them.

3. Wait until GINT is true with a timeout in case INDEX is not present on the interface. Check FAULT for error, and abort if true. If IDFULL is true, perform any checks on the data in the ID FIFO. If SEQSTP is true, check to see if an error occurred that must be serviced. Clear the status serviced.

The CPU performs the WRITE SECTOR command as follows:

1. After setting up the control store and address registers as defined above, write 0F to the SKIP register, and then write the sector count to the SECCNT register to start the transfer.

2. Write IDFULL, FAULT, and SEQSTP true to the SISR register to clear those status bits, and to the SIMR register to enable them.

3. Wait until GINT is true with a timeout in case INDEX is not present on the interface. Check FAULT for error, and abort if true. If IDFULL is true, perform any checks on the data in the ID FIFO. If SEQSTP is true, check to see if an error occurred that must be serviced. Clear the status serviced.

6.6.5 ID Retry and Error Conditions

The WD10C01A manages errors by using the RTY and FAIL bits in the control store error control byte. These bits tell the WD10C01A when to check its internal error status bits, and what to do about the error. All internal status bits in the WD10C01A are held in their error state until reset by a retry, or by writing to the START register.

If an error occurs when or before the RTY bit is set, an ID retry is performed. The LOOP register address will be loaded into the control store address register, restarting the sector. Also, the RG signal is switched false for one whole byte time to reset external decoders/PLLs. If the control store instruction at the LOOP address does not specify that RG is true, then it will stay false.

If an error occurs when or before the FAIL bit is set, an immediate abort of the command occurs when FAIL goes true. The appropriate error status bit(s) are set, and the sequencer stops.

The following list summarizes the read error conditions of the WD10C01A:

1. When executing a WIAM or WDAM operation, and the AMDET signal goes true, but the sync byte does not match within the sixteen bit timeout period. SYNCER will be set true if a halt is commanded (FAIL set).

2. When searching for a simple byte sync byte, and the count in the control store count field is exhausted. SYNCER will be set true if a halt is commanded (FAIL set).

3. Once byte sync is established, any read compare operations (CMPEN bit set) that fail. In the case of immediate data, this handles the ST412 second address mark byte (FE or F8) and the SYNCER bit will be true if a halt is commanded (FAIL set). In all other cases (i.e., buffer or ID data), the CMPERR bit is be true if a halt is commanded (FAIL set).

4. Any checksum error. This error status is retained by the IDERR bit in the SEQCTL register if a retry is commanded (RTY set) until the next ID field starts. The ECCERR bit is set if an abort was commanded (FAIL set). In this case, the checksum shift register contains the correction syndrome. The register ECCS shows the additional ECC status.

5. When executing a WDAM operation, if the AMDET signal does not go true, and the count in the control store count field is exhausted. SYNCER will be set true if a halt is commanded (FAIL set).

6.6.6 Error Recovery

When a read error occurs that causes a halt of the command before it is completed, certain steps must be performed to recover from that error. When the sequencer stops, the following conditions are in effect:

1. The SECCNT register contains a remainder. If the error is an ID error or a sync error (SYNCER set), this is the number of sectors to read including the one in error. Any other error gives the number of sectors to read after the one in error.

2. The ID set registers are set to an ID field. If the error is a sync error, this is the sector address of the one in error. Any other error gives the sector address following the one in error. In general, any error that is detected after the data field transfer starts (DXF went true, see the SEQSTS register) will cause SECCNT and the ID write registers to be set for the sector following the one in error.

3. The SEQCTL read bits define the error. If ECCERR is set, then the error is a checksum error. If CMPERR is set, the error is a verify or second address mark byte error. If SYNCER is set, the error is a byte sync error.

4. The internal checksum register may contain a correction syndrome, depending on the type of error.

The SECCNT contains a non-zero remainder. SECCNT is inhibited from restarting the sequencer by the latched error status. In order to restart for retry or continuing, the START register must be written with the starting control store address. This immediately clears any error status (SEQCTL read bits), and if the SECCNT register is still non-zero, will cause the sequencer to start.

6.6.7 Error Correction

The Reed-Solomon ECC implemented in the WD10C01A can correct up to 2 error bytes (degree 5) and up to 3 error bytes (degree 6) per interleave. Depending on the interleave factor being used, it can correct up to 30 bytes of error within a sector.

During read operations, the device produces composite syndromes. These syndromes are used by the error correction routine (microprocessor) to calculate the error location and error value. The microprocessor responses to the SEQSTP interrupt by first reading the SISR and the ECCS registers to determine the type of failure. If the EERR bit in the ECCS is set, the microprocessor determines which interleaves are in error by reading the status bits I0E-I4E in the ECCS. The microprocessor then start reading the SPORT register to transfer the syndromes. The WD10C01A automatically transfer the syndromes from the lowest interleave number. The highest byte is transferred first. The microprocessor has to read the SPORT register five times for degree 5 and six times for degree 6 to complete the syndrome transfer of an interleave. After all syndromes of the interleave are transferred, the microprocessor must reset the corresponding error status bit in the ECCS by writing a 0 into that bit. The microprocessor can then continue reading the syndromes of the next interleave.

7.0 DC ELECTRICAL SPECIFICATIONS

7.1 MAXIMUM RATINGS

Ambient temperature	0°C to 70°C
Storage temperature	-65° C to 150° C
Voltage on any pin with respect to V_{SS}	-0.3 to V_{DD}+0.3 Volts
Voltage on V_{DD} with respect to V_{SS}	7 Volts
Leakage current	±10 µA
Power dissipation	1000 mW at X1=32 MHz, RRCLK=27 MHz, 0°C, all outputs open
Input Static Discharge Protection	2000 V pin to pin

NOTE

Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

7.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70° C
V_{DD} supply voltage with respect to V_{SS}	+5 Volts ± 0.5 V
V_{SS}	0 Volts
Latch-up current (min)	±40 mA
Operating humidity range	20 to 95%
X1 input operating frequency with crystal	32 MHz(max) 8 MHz (min)
X1 input operating frequency with TTL source	25 MHz(max) --- MHz (min)

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7.3 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	2.0	---	V	V_{DD} = 5V ±5%
V_{IL}	Input Low Voltage	---	0.8	V	V_{DD} = 5V ±5%
I_{IH}	Input High Current	---	600	µA	V_{IL} = 0.8V
I_{IL}	Input Low Current	---	-600	µA	V_{IH} = 2.0V
V_{OH}	Output High Voltage	2.4	---	V	*, I_{OH} = -400 µA
V_{OL}	Output Low Voltage	---	0.40	V	*, I_{OL} = 2 mA
V_{OH}	Output High Voltage	V_{DD}-0.5	---	V	**,I_{OH} = -800 µA
V_{OL}	Output Low Voltage	---	0.40	V	**, I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4	---	V	***,I_{OH} = -2.5 mA
V_{OL}	Output Low Voltage	---	0.40	V	****, I_{OL} =6 mA
C_I	Input Capacitance	---	10	pF	all inputs
C_O	Output Capacitance	---	50	pF	All outputs except: D0-D7, BMD0-BMD7,BMP, OSC, and CPUCLK
C_O	Output Capacitance	---	100	pF	Outputs D0-D7,BMD0-BMD7, and BMP
C_O	Output Capacitance	---	100	pF	Outputs OSC and CPUCLK
I_{CC}	Supply Current	---	200	mA	60 mA (typical); X1=32MHz, RRCLK=27MHz, 0°C, all outputs open, V_{DD}=5V

TABLE 7-1. DC CHARACTERISTICS

NOTES:

Ta = 0°C (32°F) to 70°C (158°F),
V_{DD} = +5V ±5%

* Output Voltages (all outputs except X2, CPUCLK, OSC, D0-D7), see †

** Output Voltages (CPUCLK and OSC only), see†

***Output Voltages (D0-D7), see †

****Output Voltages (D0-D7, $\overline{INT}$ Logic 0)

† Even under worst case AC transient switching conditions V_{OL} = 0.8V shall not be exceeded on any output pin at any time.

8.0 AC OPERATING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

1. All unit are in nanoseconds

2. These timing relationships assume the maximum capacitive loading for both inputs and outputs, V_{DD} = 4.50 volts to 5.50 volts.

3. Temperature = 0°C to 70°C.

4. All timing is measured between 0.8 volts logic low and 2.0 volts logic high, unless otherwise noted.

8.1 OSC AND CPUCLK TIMING

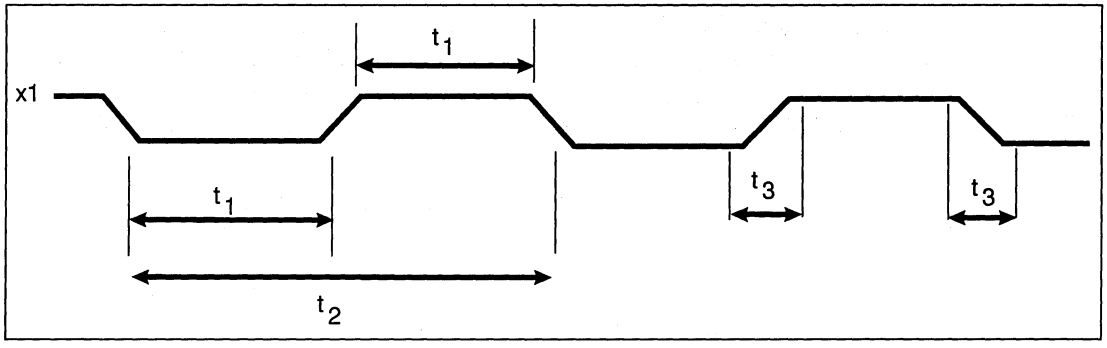

FIGURE 8-1. TTL SOURCE X1 CLOCK INPUT

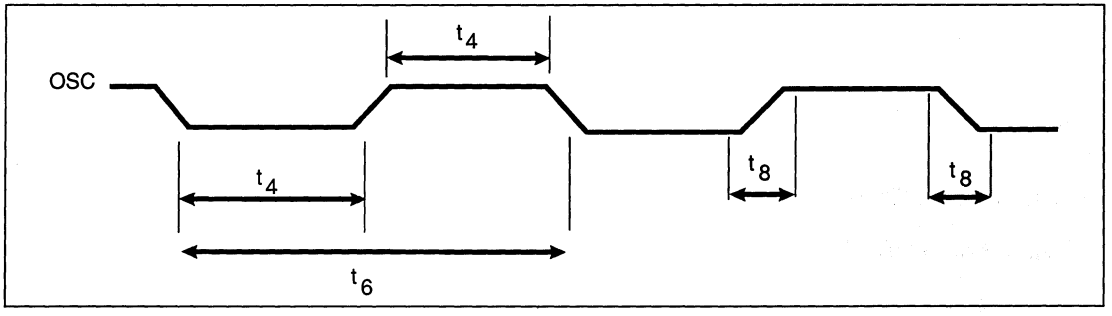

FIGURE 8-2. OSC OUTPUT

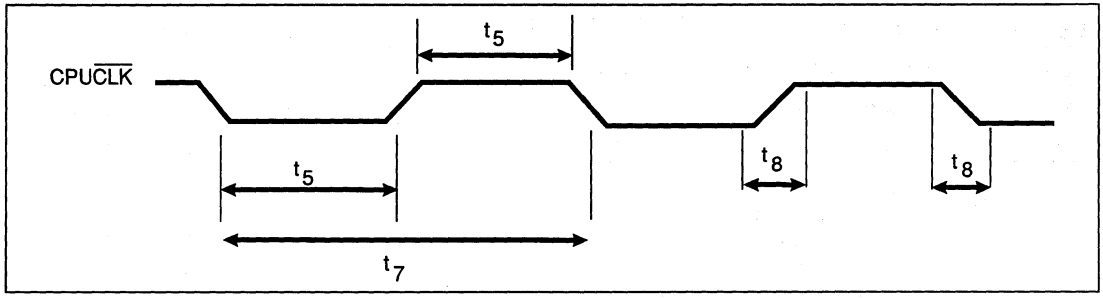

FIGURE 8-3. CPUCLK OUTPUT

The following table summarizes the relationship between the clock at X1 and the resultant outputs at OSC and CPUCLK. OSCDIV and CPUDIV are control bits in the RESET register that determine how the X1 clock is divided to produce OSC and CPUCLK. See the programming section for more information.

OSCDIV	CLKDIV	OSC	CPUCLK
0	0	X1/2	X1/6
0	1	X1/2	X1/4
1	0	X1/1	X1/3
1	1	X1/1	X1/2

No.	DESCRIPTION	MIN	MAX	UNITS
t_1	TTL source X1 high or low(*1)	13		ns
t_2	TTL source X1 cycle time	40		ns
t_3	TTL source X1 rise or fall time (*1)		5	ns
t_4	OSC high or low when: (*2)		---	---
	X1/1 crystal (*3)	10	---	ns
	X1/2 crystal (*3)	27	33	ns
	X1/1 TTL source (*5)	16	24	ns
	X1/2 TTL source (*4)	36	44	ns
t_5	CPUCLK high or low when: (*2)	---	---	---
	X1/2 crystal (*3)	27	33	ns
	X1/3 crystal (*3)	36	54	ns
	X1/4 crystal (*3)	54	66	ns
	X1/6 crystal (*3)	81	99	ns
	X1/2 TTL source (*4)	36	44	ns
	X1/3 TTL source (*5)	48	72	ns
	X1/4 TTL source (*4)	72	88	ns
	X1/6 TTL source (*4)	108	132	ns
t_6	OSC cycle time when:	---	---	---
	X1/1 crystal (*3)	30	125	ns
	X1/2 crystal (*3)	60	250	ns
	X1/1 TTL source (*4)	40	---	ns
	X1/2 TTL source (*4)	80	---	ns
t_7	CPUCLK cycle time when:	---	---	---
	X1/2 crystal (*3)	60	250	ns
	X1/3 crystal (*3)	90	375	ns
	X1/4 crystal (*3)	120	500	ns
	X1/6 crystal (*3)	180	750	ns
	X1/2 TTL source (*4)	80	---	ns
	X1/3 TTL source (*4)	120	---	ns
	X1/4 TTL source (*4)	160	---	ns
	X1/6 TTL source (*4)	240	---	ns
t_8	CPUCLK and OSC rise or fall time (*2)	---	5	ns

TABLE 8-1. OSC AND CPUCLK TIMING PARAMETERS

NOTES:

*1)Times are measured relative to V_{IH} and V_{IL}.

*2)High and low times are measured relative to the midpoints between V_{OL} and V_{OH}. Rise and fall times are measured between V_{OH} and V_{OL}.

*3)Assumes 33.3 MHz crystal across X1 and X2 for min times, 8.0 MHz crystal for max times.

*4)Assumes 25.0 MHz TTL source to X1.

*5)Assumes 25.0 MHz TTL source to X1, 50/50 duty cycle.

8.2 CPU INTERFACE TIMING

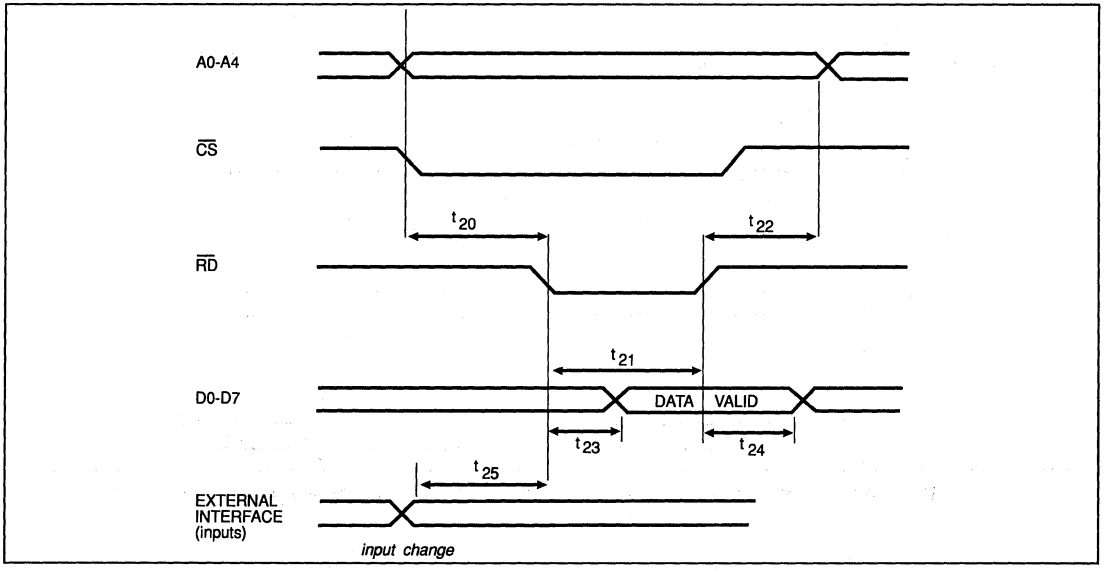

FIGURE 8-4. MICROPROCESSOR RD* TIMING (RD* CONTROLLED)

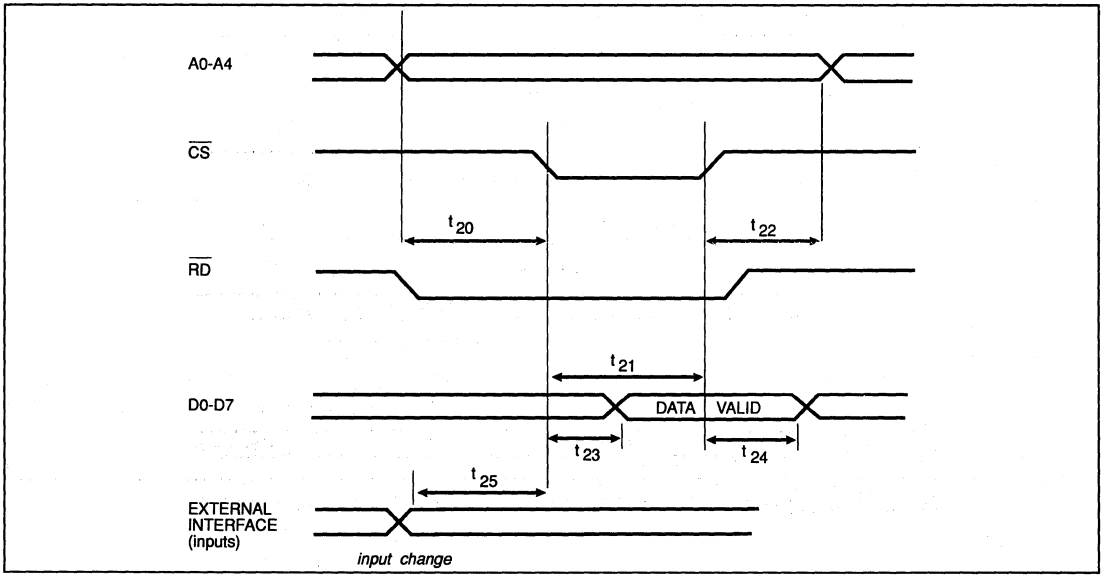

FIGURE 8-5. MICROPROCESSOR RD* TIMING (CS* CONTROLLED)

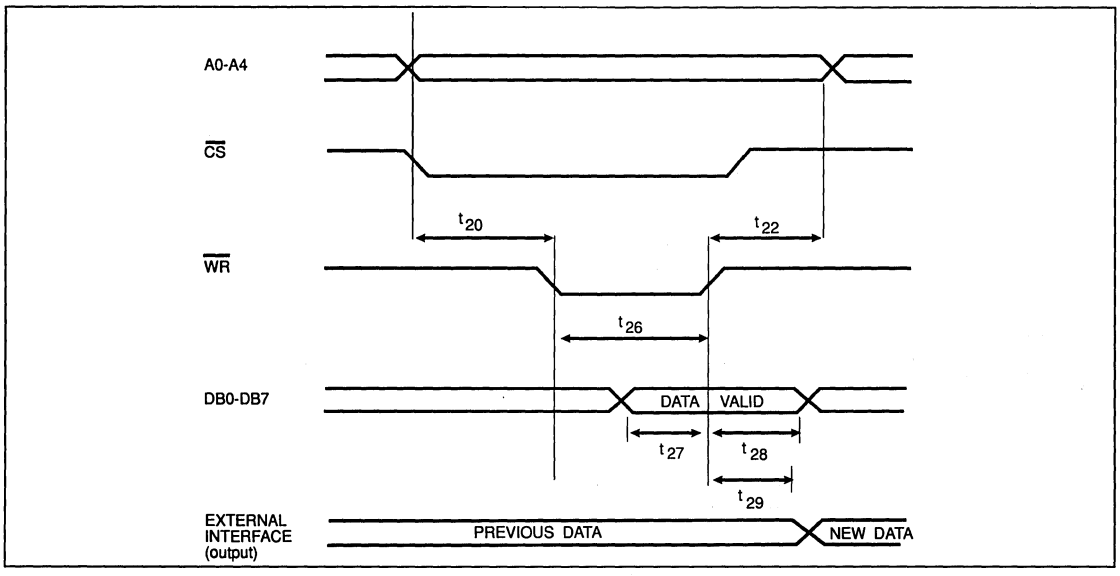

FIGURE 8-6. MICROPROCESSOR WR* TIMING (WR* CONTROLLED)

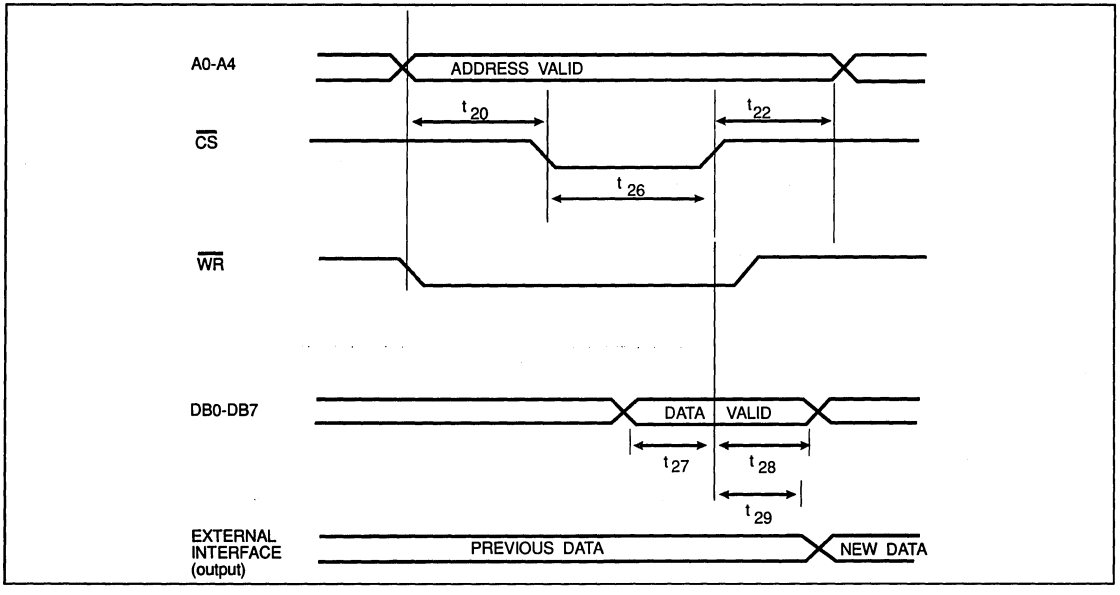

FIGURE 8-7. MICROPROCESSOR WR* TIMING (CS* CONTROLLED)

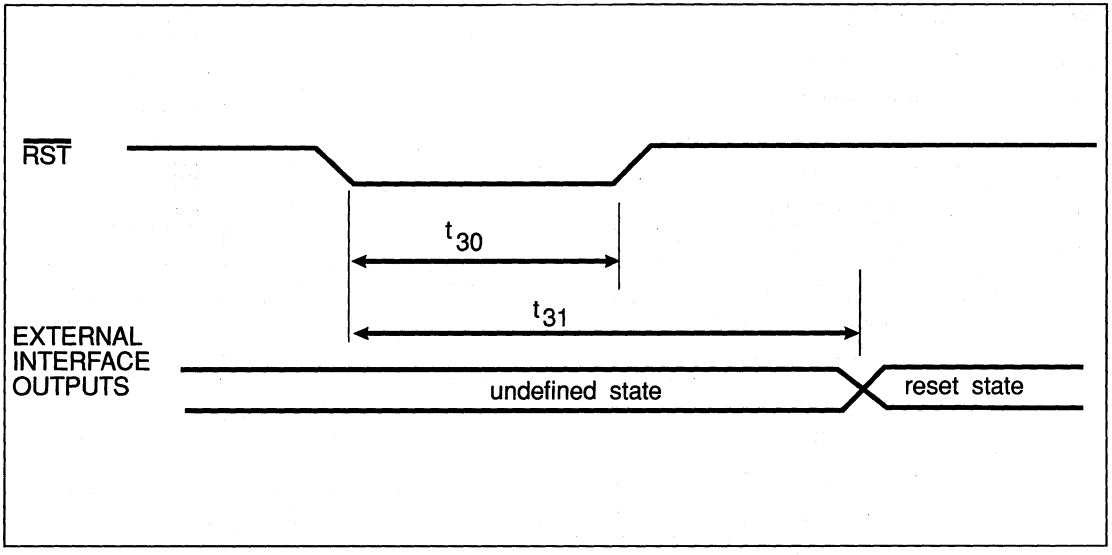

FIGURE 8-8. RESET TIMING

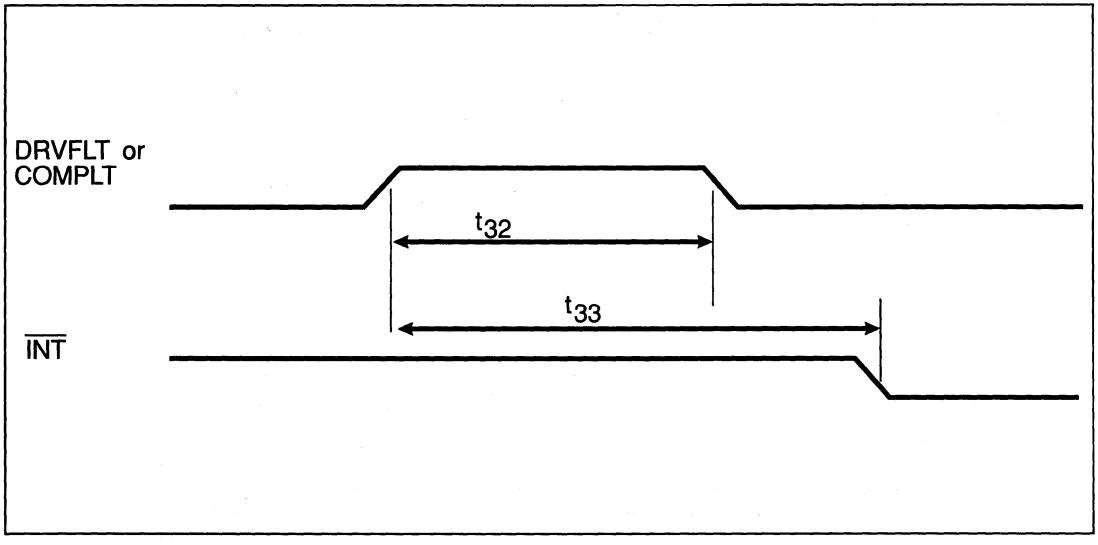

FIGURE 8-9. EXTERNALLY GENERATED INTERRUPT TIMING

No.	DESCRIPTION	MIN	MAX	UNITS
t_{20}	address valid to $\overline{RE}$ or $\overline{WE}$ (*3)	20		ns
t_{21}	$\overline{RE}$ pulse width (*3)	100		ns
t_{22}	$\overline{RE}$ or $\overline{WE}$ to address change (*3)	0		ns
t_{23}	$\overline{RE}$ true to data valid (*3)	---	95	ns
t_{24}	$\overline{RE}$ false to data hold (*3)	20	60	ns
t_{25}	input port setup to $\overline{RE}$ true (*1)(*3)	80	---	ns
t_{26}	$\overline{WE}$ pulse width (*3)	100	---	ns
t_{27}	data setup to $\overline{WE}$ false (*3)	80		ns
t_{28}	$\overline{WE}$ false to data hold (*3)	0		ns
t_{29}	$\overline{WE}$ false to output change (*2)(*3)	---	80	ns
t_{30}	$\overline{RST}$ pulse width	100	---	ns
t_{31}	$\overline{RST}$ true to stable outputs	---	150	ns
t_{32}	DRVFLT or COMPLT pulse width	100	---	ns
t_{33}	DRVFLT or COMPLT high to $\overline{INT}$ low	---	150	ns

TABLE 8-2. CPU INTERFACE TIMING PARAMETERS

NOTES:

*1) Inputs are: PZ0-5, PY0-3 when defined as inputs, and AMDET when being used as a simple input pin.

*2) Outputs are: PX0-7, and PY0-3 when defined as outputs.

*3) $\overline{RE}$ = $\overline{RD}$ or $\overline{CS}$;
$\overline{WE}$ = $\overline{WR}$ or $\overline{CS}$

8.3 BUFFER INTERFACE TIMING

(Data is coming out of the WD10C01A)
REQTIM=1 in RESET register. (REQA true when internal data register is full.)

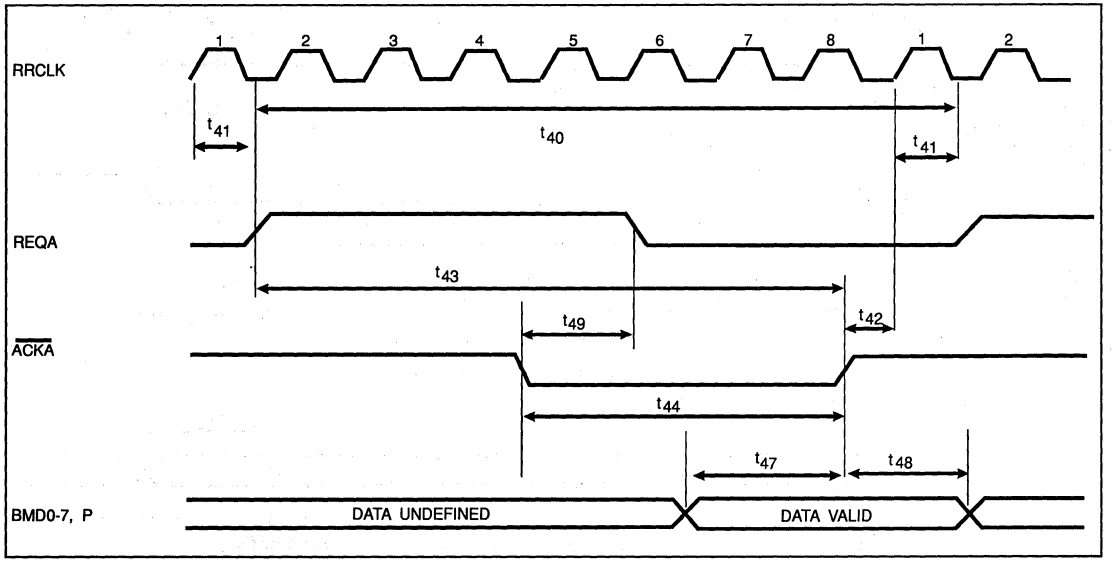

FIGURE 8-10. ASYNCHRONOUS MODE DATA BUS WRITE TIMING (1)

REQTIM=0 in RESET register. (REQA true one bit time before internal data register is full. Note that the cycles overlap by one bit time.)

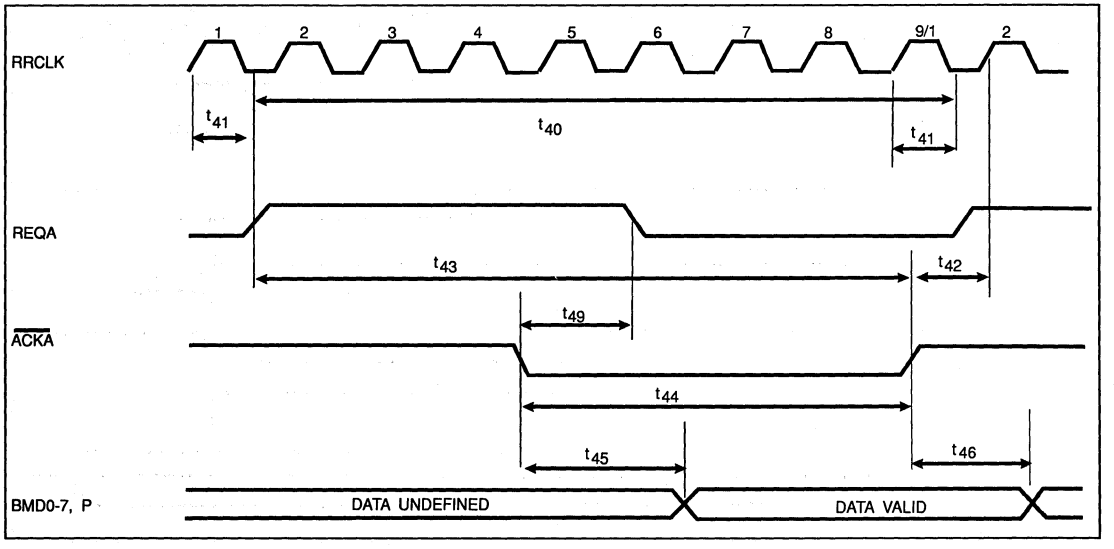

FIGURE 8-11. ASYNCHRONOUS MODE DATA BUS READ TIMING (0)

(Data is going into the WD10C01A)
REQTIM=1 in RESET register. (REQA true when internal data register is empty.)

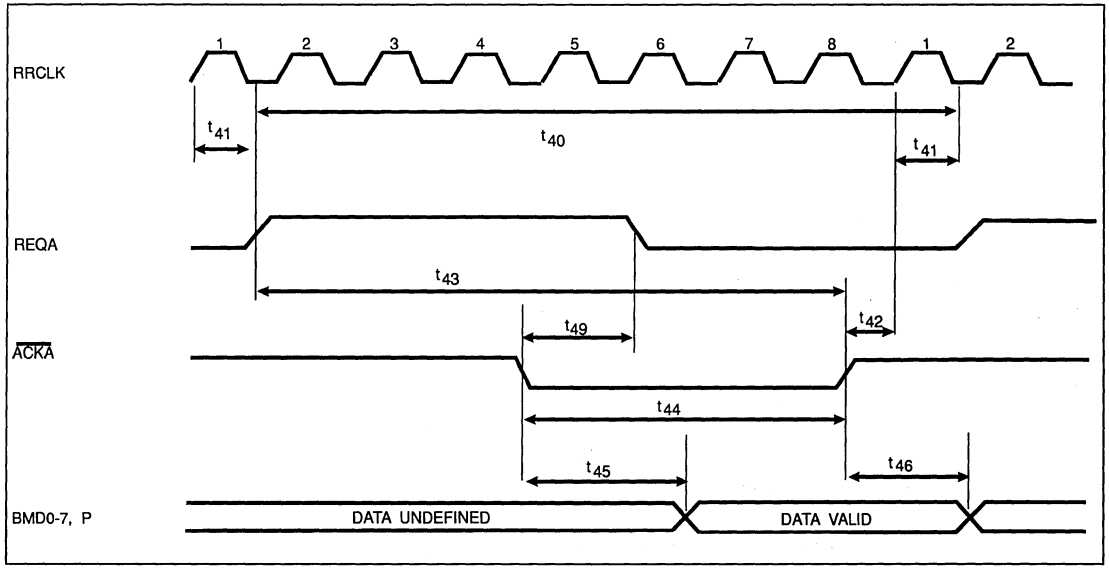

FIGURE 8-12. ASYNCHRONOUS MODE DATA BUS READ TIMING (1)

REQTIM=0 in RESET register. (REQA true one bit time before internal data register is empty. Note that the cycles overlap by one bit time.)

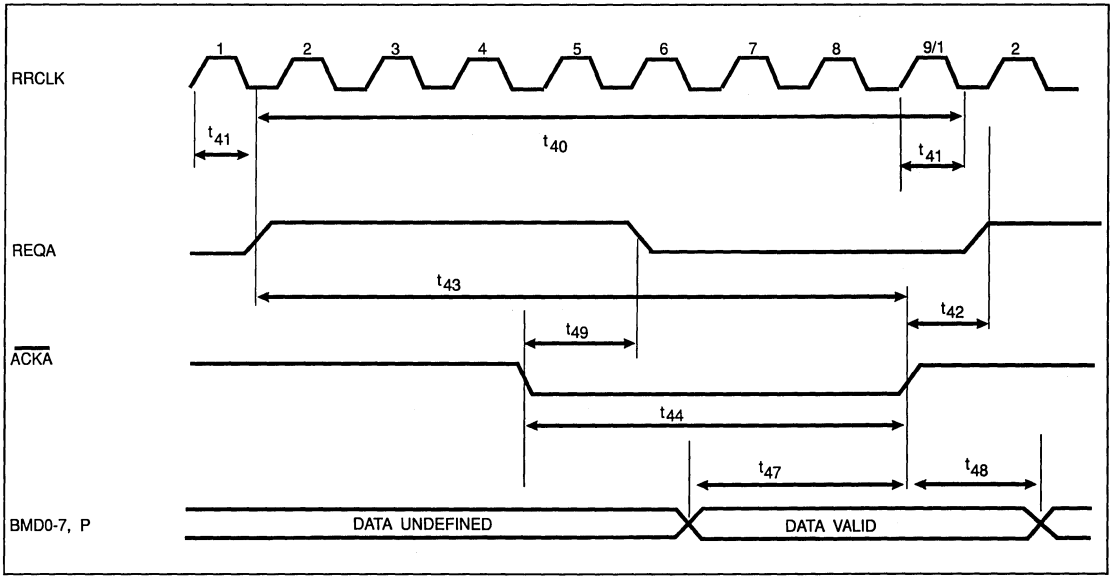

FIGURE 8-13. ASYNCHRONOUS MODE DATA BUS WRITE TIMING (0)

No.	DESCRIPTION	MIN	MAX	UNITS
t_{40}	DMA (REQA) cycle time (*1)		$8*T_{cyc}$	ns
t_{41}	RRCLK true to REQA true		40	ns
t_{42}	$\overline{ACKA}$ false to RRCLK true	20		ns
t_{43}	REQA true to $\overline{ACKA}$ false: (*1) REQTIM=0 REQTIM=1		--- $9*T_{cyc}-t_{41}-t_{42}$ $8*T_{cyc}-t_{41}-t_{42}$	ns
t_{44}	$\overline{ACKA}$ active low	100	---	ns
t_{45}	$\overline{ACKA}$ true to data valid		60	ns
t_{46}	$\overline{ACKA}$ false to data hold	10	60	ns
t_{47}	data setup to ACKA* false	35		ns
t_{48}	$\overline{ACKA}$ false to data hold	5		ns
t_{49}	$\overline{ACKA}$ true to REQA false		35	ns

TABLE 8-3. BUFFER INTERFACE TIMING PARAMETERS

NOTES:

*1)T_{cyc} is the RRCLK cycle time used.

8.4 SERIAL DATA TIMING

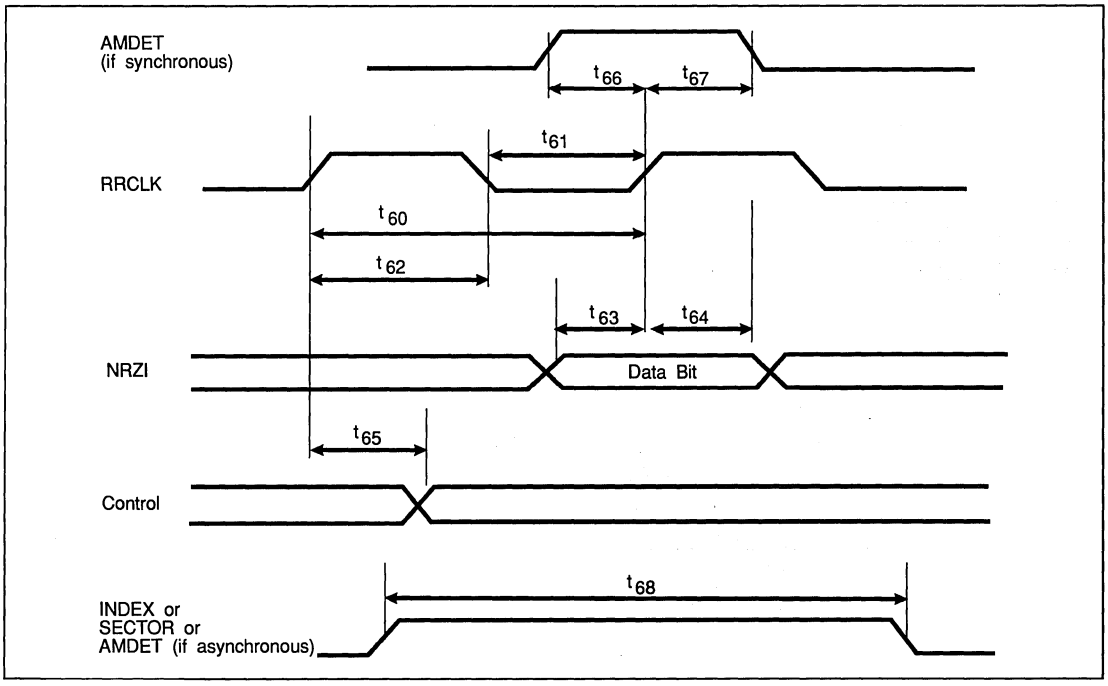

FIGURE 8-14. NRZ DATA INPUT TIMING

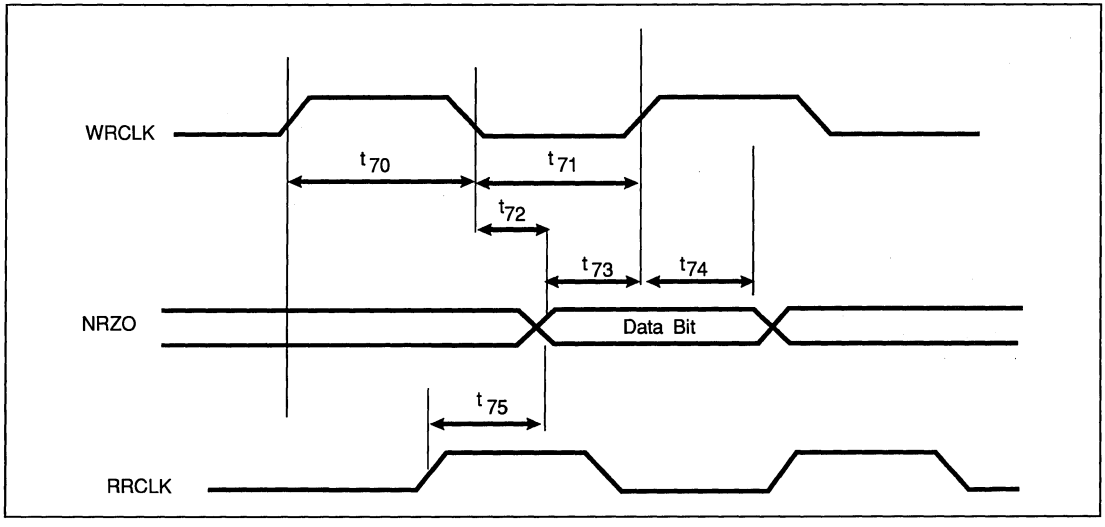

FIGURE 8-15. NRZ DATA OUTPUT TIMING

No.	DESCRIPTION	MIN	MAX	UNITS
t_{60}	RRCLK cycle time	37		ns
t_{61}	RRCLK low (*1)	14		ns
t_{62}	RRCLK high (*1)	14		ns
t_{63}	NRZI setup to RRCLK high	10		ns
t_{64}	RRCLK high to NRZI hold	10		ns
t_{65}	RRCLK high to new control out (*3)		30	ns
t_{66}	AMDET setup to RRCLK high (*4)	10		ns
t_{67}	RRCLK high to AMDET hold (*4)	10		ns
t_{68}	asynchronous input width	$2*T_{cyc}$		ns
t_{70}	WRCLK high (*2) (*6) (*2) (*6) (*7)	T_{rlo}-6.0 T_{rlo}-5.0		ns
t_{71}	WRCLK low (*2) (*6) (*2) (*6) (*7)	T_{rhi}-6.0 T_{rhi}-5.0		ns
t_{72}	WRCLK low to NRZO change(*6) (*6) (*7)	-3.5 -2.75	3.5 2.75	ns
t_{73}	NRZO setup to WRCLK high(*6) (*6) (*7)	T_{rhi}-9.5 T_{rhi}-8.75		ns
t_{74}	WRCLK high to NRZO hold (*6) (*6) (*7)	T_{rlo}-9.5 T_{rlo}-8.75		ns
t_{75}	RRCLK high to NRZO change		30	ns

TABLE 8-4. SERIAL DATA TIMING PARAMETERS

NOTES:

*1)High and low times measured relative to V_{IH} and V_{IL}.

*2)T_{rlo} and T_{rhi} are the clock low and clock high (respectively) for the RRCLK input used. T_{cyc} is RRCLK cycle time used.

*3)Control outputs are: SEQOUT, WG, RG, and AMENA.

*4)When AMDET is supplied from a synchronous source.

*5)Asynchronous inputs are: INDEX, SECTOR, and AMDET when it is supplied from an asynchronous source.

*6)Where the RRCLK input is driven from 0.4V (V_{IL}) to 2.4V (V_{IH}).

*7)The specification with reduced load capacitance of 25 pF.

A.0 WD10C01A PROGRAMMER'S BENCH REFERENCE (PBR)

ADDR	NAME	DIR	SIZE
00	SRESET	W	6-0
01	SISR	R/W	7-0
02	SIMR	R/W	7-0
03	SEQSTS/PYC	R/W	7-0/ 3-0
04	CSERR	R/W	3-0
05	CSCTL	R/W	7-0
06	CSVAL	R/W	7-2; 7-0
07	CSCNT	R/W	7-4, 0;7-0
08	PORTX	R/W	7-0
09	PORTY	R/W	3-0
0A	PORTZ/AMC	R/W	5-0/ 7-0
0B	SEQCTL	R/W	5-0
0C	START	R/W	4-0
0D	LOOP	W	4-0
0E	ECCCTL	W	5-1
0F	SECCNT	R/W	7-0
10	ECCP	R/W	3-0
11	ECCS	R/W	4-0
12	SPORT	R	7-0
13	Reserved		7-0
14	Reserved		7-0
15	Reserved		7-0
16	do not use - test only		
17	SKIP	W	4-0
18	ID0	R/W	7-0
19	ID1	R/W	7-0
1A	ID2	R/W	7-0
1B	ID3	R/W	7-0
1C	ID4	R/W	7-0
1D	ID5	R/W	7-0
1E	ID6	R/W	7-0
1F	ID7	R/W	7-0

TRUE = 1 FOR ALL BITS

A.1 ADDRESS BIT TABLES

The following is a set of bit tables.

SRESET(00)	
Bit	**Write**
7	CLKDIV
6	OSCDIV
5	
4	
3	
2	REQTIM
1	ID3$4
0	SRST

SISR(01) AND SIMR(02)	
Bit	**Read/Write**
7	GINT
6	IDFULL
5	DXFER
4	COMPLT
3	SEQSTP
2	SECEND
1	SM$IX
0	FAULT

SEQSTS(03)	
Bit	**Read**
7	DATFLD
6	ECCEN
5	LAST
4	ID
3	CHK
2	WAIT
1	AMDET
0	SEQOUT

PYC(03)	
Bit	**Write**
7	
6	
5	
4	
3	PY3OUT
2	PY2OUT
1	PY1OUT
0	PY0OUT

CSVAL(06)	
Bit	**Read/Write**
7	BUFF
6	NOXFER
5	LAST
4	ID
3	CHK
2	
1	
0	

CSERR(04)	
Bit	**Read/Write**
7	
6	
5	
4	
3	FAIL
2	RTY
1	DAC
0	SEQOUT

CSCNT(07)	
Bit	**Read/Write**
7	WDAM (COUNT)
6	WIAM
5	WIX
4	WSM
3	
2	
1	
0	STOP

CSCTL(05)	
Bit	**Write**
7	SVSEL
6	CWSEL
5	WG
4	RG
3	AM
2	CMPEN
1	SKPEN
0	JMPEN

SEQCTL(0B)		
Bit	**Read**	**Write**
7		RGERLY
6		
5	ECCERR	
4	IDERR	
3	PTYERR	IXMASK
2	SYNCER	SMMASK
1	CMPERR	RCMP
0		KILL

ECCCTL(0E)	
Bit	**Write**
7	
6	
5	ECCCLR
4	CRCSET
3	CRCNIT
2	IGNERR
1	DISPTY
0	

ECCS(11)		
Bit	**Read**	**Write**
7		
6	EERR	
5	CERR	
4	I4E	I4E
3	I3E	I3E
2	I2E	I2E
1	I1E	I1E
0	I0E	I0E

ECCP(10)	
Bit	**Read/Write**
7	
6	
5	
4	
3	SYNCCRC
2	SYNCECC
1	DEG6/5
0	IFS5/3

B.0 RESET CONDITIONS

The following list defines what is reset when $\overline{RST}$ is asserted on the WD10C01A, or the CPU sets the internal reset bit (SRST in SRESET register):

- SRST bit in SRESET is left set, and must be cleared by the CPU to take the WD10C01A out of the reset state
- interrupts are disabled
- PY0-3 are set to input
- BMD0-7,P are disabled
- OSC is set to X1/2
- CPUCLK is set to X1/6
- command sequencer stops

The following CPU registers are reset to zero:

- PORT X
- PORT Y CONFIGURATION
- SECTOR COUNTER
- INTERRUPT MASK REGISTER
- SRESET REGISTER (except SRST)
- ECCP except SYNCCRC and SYNCECC, which are initialized to one's
- ECCS
- SPORT
- KILL and RGERLY bits in SEQCTL register

The following outputs are reset to zero:

- PX0-7
- SEQOUT
- AMENA
- RG
- WG
- NRZO
- REQA

The following error status bits are reset to zero:

- IDERR
- PTYERR

C.0 CRYSTAL OSCILLATOR APPLICATIONS

For applications that use the internal oscillator capability of the WD10C01A, a series resonant crystal must be used. This crystal must meet the following internal specifications:

CS = 7 pf MAX

RS = 30 ohms MAX

The oscillator also requires bypass capacitors, as shown in the following diagram:The following table lists values for C1 and C2 for several typical crystal frequencies. The capacitor tolerances are ±10%. Values for intermediate frequencies (not listed in the table) may be extrapolated.

FREQ (MHz)	C1 (pf)	C2 (pf)
8	180	100
10	180	68
12	150	47
14	120	56
16	82	56
20	82	33
24	56	27
25	56	22
30	39	12
32	33	12

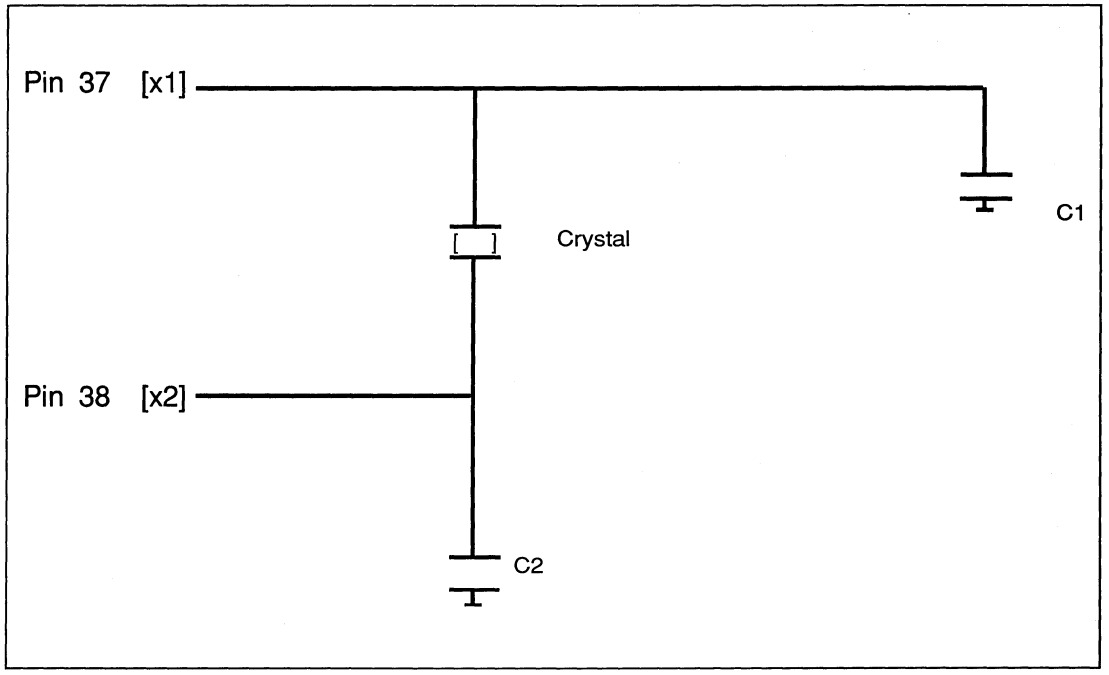

FIGURE C-1. OSCILLATOR WITH CAPACITORS

D.0 PIN/SIGNAL SUMMARY

PIN	SIGNAL	I/O	FUNCTION
1	BMD7	I/O	Buffer
2	BMD6	I/O	Buffer
3	BMD5	I/O	Buffer
4	BMD4	I/O	Buffer
5	BMD3	I/O	Buffer
6	BMD2	I/O	Buffer
7	BMD1	I/O	Buffer
8	BMD0	I/O	Buffer
9	VSS	I	Ground
10	$\overline{CS}$	I	CPU Interface
11	DB0	I/O	CPU Interface
12	DB0	I/O	CPU Interface
13	DB0	I/O	CPU Interface
14	DB0	I/O	CPU Interface
15	DB0	I/O	CPU Interface
16	DB0	I/O	CPU Interface
17	DB0	I/O	CPU Interface
18	DB0	I/O	CPU Interface
19	$\overline{RD}$	I	CPU Interface
20	$\overline{WR}$	I	CPU Interface
21	A4	I	CPU Interface
22	A3	I	CPU Interface
23	A2	I	CPU Interface
24	A1	I	CPU Interface
25	A0	I	CPU Interface
26	VDD	I	+5 Volts
27	$\overline{INT}$	O	CPU Interface
28	SECTOR	I	Disk Control
29	INDEX	I	Disk Control
30	AMDET	I	Disk Data
31	AMENA	O	Disk Data
32	SEQOUT	O	Disk Data
33	OSC	O	CPU Interface
34	DRVFLT	I	Disk Control
35	COMPLT	I	Disk Control

PIN	SIGNAL	I/O	FUNCTION
36	CPUCLK	O	CPU Interface
37	X1	I	CPU Interface
38	X2	O	CPU Interface
39	PZ5	I	Disk Control
40	PZ4	I	Disk Control
41	PZ3	I	Disk Control
42	PZ2	I	Disk Control
43	VSS	I	Ground
44	PZ1	I	Disk Control
45	PZ0	I	Disk Control
46	PY3	I,O	Disk Control
47	PY2	I,O	Disk Control
48	PY1	I,O	Disk Control
49	PY0	I,O	Disk Control
50	PX7	O	Disk Control
51	PX6	O	Disk Control
52	PX5	O	Disk Control
53	PX4	O	Disk Control
54	PX3	O	Disk Control
55	PX2	O	Disk Control
56	PX1	O	Disk Control
57	PX0	O	Disk Control
58	WG	O	Disk Data
59	RG	O	Disk Data
60	VDD	I	+5 Volts
61	RST*	I	CPU Interface
62	WRCLK	O	Disk Data
63	NRZO	O	Disk Data
64	RRCLK	I	Disk Data
65	NRZI	I	Disk Data
66	REQA	O	Buffer
67	$\overline{ACKA}$	I	Buffer
68	DBP	I/O	Buffer

E.0 DIFFERENCES BETWEEN WD10C00 AND WD10C01A

E.1 ERROR CORRECTION AND DETECTION

The computer-generated-code ECC in WD10C00 was replaced with the Reed-Solomon ECC in WD10C01A. Six registers (ECC[0:5]) which define the masks for ECC polynomials in WD10C00 were taken out. The new ECCP, ECCS, SPORT registers facilitate the configuration parameters, operation status and the syndrome access for the new RS encoder/decoder.

E.2 SRESET REGISTER

The control bits IDCHK, DCHK, ECCSIZ bits of the WD10C00 are removed. By default, data field is covered by RS-ECC, and ID Field is covered by CCITT-CRC with $g(x)= X^{16} + X^{12} + X^5 + 1$.

E.3 ECCCTL REGISTER

The ECCINL, ECCSHT, ECCINM bits of the WD10C00 are removed. The control bit ECCSET is renamed to CRCSET, bit ECCNIT is renamed to CRCNIT. These bits affect only the CRC shift registers, the RS-ECC shift registers are be default reset to zero. The control bit DISCHK of WD10C00 is changed into IGNERR. Its function is still the same.

E.4 TIMING

The timing t_{47} (data setup time on the BMD bus before ACKA goes inactive) is changed from 30 ns to 35 ns; t_{70}, t_{71}, t_{72}, t_{73} and t_{74} have additional specifications with reduced loading capacitance of 25 pF.

E.5 PIN NAME

The name of the microprocessor data bus and the DMA data bus are changed to reflect the name on the circuit diagrams. The pin order and the functions are exactly the same as before.

WD10C00	WD10C01A
DB0-DB7	BMD0-BMD7
DBP	BMDP
D0-D7	DB0-DB7

E.6 PARITY ERROR HANDLING

WD10C00 will latch the parity error condition into the SEQCTL register and the operation will continue normally. WD10C01A will stop at the end of the current CS instruction if the FAIL bit is set to one. The WG output is also deasserted.

E.7 SEQCTL REGISTER

Bit 6 and bit 0 in the SEQCTL register are unused in the WD10C00 and in the WD10C01A. These bits are read-only type and are set to one in the WD10C00; in the WD10C01A, these bits are set to zero.

WD10C27

Data

Separator

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The WD10C27 Read/Write Channel is a fully integrated LSI device intended for variable frequency applications in conjunction with the WD61C22 Hard Disk Controller/Buffer Manager.

In a typical application, the WD10C27 performs all of the handling of the sensitive read/write signals between a disk controller and data drivers and receivers. Raw read data corresponds to previous write data, with added phase, frequency, and write splice noise added during read-back. The fundamental purpose of the WD10C27 is to remove these noise components and present a clean digital recovered data and reference clock to the controller. See Figure 1-1 - Signal/Pin Assignments.

1.2 FEATURES

- General
  - Specifically designed for the WD61C22 Hard Disk Controller/Buffer Manager
  - Supports Constant Density Recording with no component changes
  - 1.25 micron +5 volt only CMOS technology
  - Available in 64-pin SQFP and MQFP packages
- Frequency Synthesizer
  - Range of 7.5 - 33 MBps with resolution ≤140 KHz
  - Programmable input reference frequency to 40 MHz
- Microprocessor Interface
  - Eight bit Intel compatible multiplexed address/data port
  - Programmable test and low power modes
- Write Data Conditioner
  - Crystal controlled processing of the write data to eliminate pulse pairing
  - Programmable pattern dependent Skew Symmetric Precompensation matrix for precomp. of up to ±25% with 1.5% resolution
- Encoder/Decoder
  - IBM Compatible 1,7 RLL
  - Hard/soft sector support and Address Mark Detection/Generation
- Data Synchronizer
  - Precision internal self adjusting VCO compensates for component, temperature, voltage, and aging variations
  - Internal gain/bandwidth modulation linearizes loop gain and increases phase margin across zones
  - Dual gain charge pump for faster acquisition and better jitter rejection while tracking
  - Dual mode phase/phase-frequency detector eliminating quadrature and harmonic lock
  - µP controlled Window Shift Synthesis for window shifting from 0% to ±50% of the window
  - Window monitoring capability
- Channel Control
  - 5-bit DACs specifically designed for use with the SSI3040 Electronic Filter/Pulse Detector
  - Independent Servo/Data Filter Optimization
  - Bandwidth, Boost and Hysteresis Control for ZBR
  - Five Programmable Microprocessor Ports

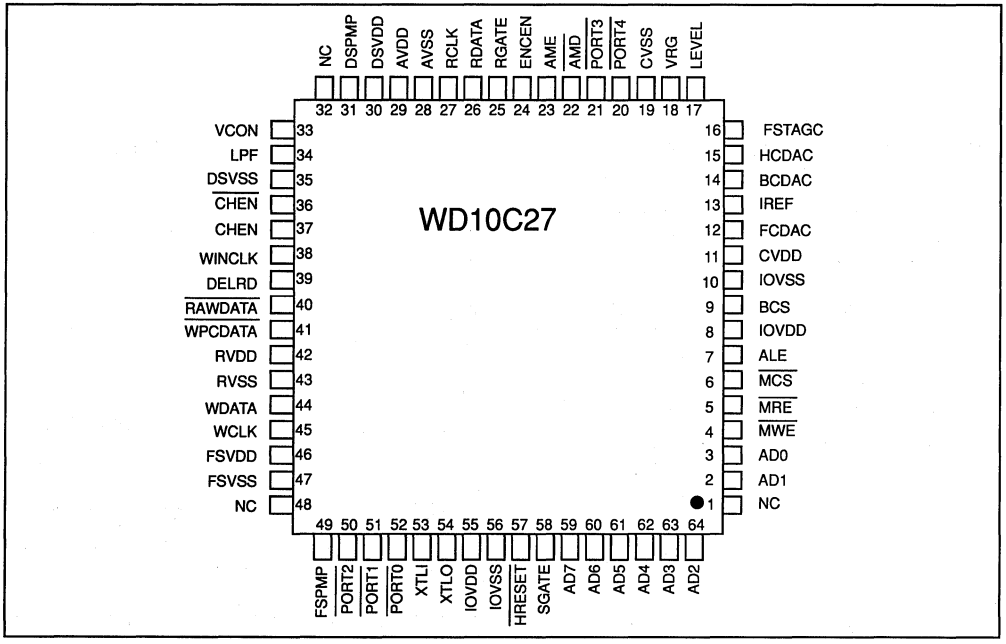

FIGURE 1-1. SIGNAL/PIN ASSIGNMENTS

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
59-64, 2-3	AD7-0	I/O	**Address/Data Bus** ADDRESS inputs used in conjunction with ALE to select the internal register to be transmitted or received on the DATA input/outputs.
4	$\overline{\text{MWE}}$	I	**$\overline{\text{Microprocessor Write Enable}}$** When asserted will transmit data from the AD bus into internal registers.
5	$\overline{\text{MRE}}$	I	**$\overline{\text{Microprocessor Read Enable}}$** When asserted will transmit data from internal registers onto the AD bus.
6(9†)	$\overline{\text{MCS}}$	I	**$\overline{\text{Microprocessor Chip Select}}$** When asserted allows information to be read from or written to the AD bus.
7	ALE	I	**Address Latch Enable** Address information is latched on the falling edge.
8,55	IOVDD	S	**I/O Supply** +5 volt supply to all I/O except $\overline{\text{WPCDATA}}$, $\overline{\text{RAWDATA}}$, and analog pins.
9(6†)	BCS	O	**Buffered Chip Select** This pin is the inverted, buffered version of the $\overline{\text{MCS}}$ input.
10,56	IOVSS	S	**I/O Ground** Dedicated ground to all I/O except $\overline{\text{WPCDATA}}$, $\overline{\text{RAWDATA}}$, and analog pins (designated "A").
11	CVDD	S	**Analog Supply** Dedicated +5v for the Channel Control DAC circuitry.
12(17)	FCDAC	A	**Freq. Ctl. DAC** Frequency Control current DAC output.
13(15)	IREF	A	**Current Reference** External current reference used to set the compliance of IDAC. When not used, IREF should be connected to CVSS.
14(18)	BCDAC	A	**Boost Ctl. DAC** Boost Control voltage DAC output.
15(13)	HCDAC	A	**Hyst. Ctl. DAC** Hysteresis Control voltage DAC output.
16(57)	FSTAGC	A	**Fast AGC** Discharge path to force fast AGC response.
17(12)	LEVEL	A	**Level** External voltage used to adjust the Hysteresis DAC offset. Should be tied to CVSS when not used.
18(14)	VRG	A	**Voltage Reference** External voltage reference used by the DAC circuits. Should be tied to CVSS when the Boost Control, Frequency Control, and Hysteresis Control DACs are not used.

TABLE 1-1. SIGNAL DESCRIPTIONS

21

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
19	CVSS	S	**Analog Ground** Dedicated ground for the Channel Control DAC circuitry.
20(58)	$\overline{\text{PORT4}}$	O	**$\overline{\text{Port Four}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
21(36)	$\overline{\text{PORT3}}$	O	**$\overline{\text{Port Three}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
22(24)	$\overline{\text{AMD}}$	O	**$\overline{\text{Address Mark Detect}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
23(26)	AME	I	**Address Mark Enable** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
24(22)	ENCEN	I	**Encode Enable** Asserted during write commands to enable the Encoder and associated write circuits.
25(27)	RGATE	I	**Read Gate** In soft sector, RGATE responds to $\overline{\text{AMD}}$ to validate the acquisition sequence during reads. In hard sector, RGATE initiates the acquisition sequence w/o $\overline{\text{AMD}}$ qualification.
26(23)	RDATA	O	**Recovered Data** Recovered NRZ read data represents the decoded RLL raw read data with all phase and frequency noise removed.
27(25)	RCLK	O	**Reference Clock** Nominally at the NRZ data frequency, RCLK tracks the low frequency variations on $\overline{\text{RAWDATA}}$ during reads, otherwise tracks the crystal reference.
28	AVSS	S	**Main Analog Ground** Main ground dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase Detectors, etc.). This supply also supports the sensitive $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$ I/O to prevent intermodulation with IOVDD /IOVSS.
29	AVDD	S	**Main Analog Supply** Main +5v supply dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase Detectors, etc.) This supply also supports the sensitive $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$ I/O to prevent intermodulation with IOVDD/IOVSS.
30	DSVDD	S	**Analog Supply** Dedicated +5v for the Data Synchronizer circuitry.
31(34)	DSPMP	A	**Data Synchronizer Pump** Charge pump to the data synchronizer PLL filter.
33(38)	VCON	A	**N-Channel Voltage Control** N-channel control voltage for the internal VCO and charge pump. This voltage is the filtered output of the charge pump.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
34(31)	LPF	A	**Low Pass Filter** Controls low pass filter characteristics under zone control via the AD bus.
35	DSVSS	S	**Analog Ground** Ground dedicated to the Data Synchronizer PLL.
36(21)	$\overline{\text{CHEN}}$	O	**$\overline{\text{Channel Enable}}$** This pin is an inverted, buffered version of the channel enable input, CHEN.
37(50)	CHEN	I	**Channel Enable** This input, active high when the Read/Write Channel Electronics are enabled, controls the state of the on-board DACs.
38(33)	WINCLK	O	**Window Clock** This output, when enabled, represents the window clock at the Data Detector and may be used for window monitoring. Phase detector pump down output in test mode.
39(41)	DELRD	O	**Delayed Read Data** This output, when enabled, represents the latched RAWDATA at the Data Detector and may be used for window monitoring. Phase detector pump up output in test mode.
40(45)	$\overline{\text{RAWDATA}}$	I	**$\overline{\text{Raw Data}}$** Disk drive raw read data from the read channel circuits. Leading edge timing, programmable polarity.
41(39)	$\overline{\text{WPCDATA}}$	O	**$\overline{\text{Write Precomp Data}}$** Precompensated/Conditioned encoded write data sent to the write channel drivers. Leading edge timing, programmable polarity.
42	RVDD	S	**Analog Supply** Dedicated +5v supply to Ramp Locked Loop circuits.
43	RVSS	S	**Analog Ground** Dedicated ground to Ramp Locked Loop circuits.
44(51)	WDATA	I	**Write Data** NRZ write data from the controller. This data is conditioned and precompensated and sent out on $\overline{\text{WPCDATA}}$.
45(40)	WCLK	I	**Write Clock** Running at the NRZ data frequency. WCLK is provided from the the hard disk controller and serves as a reference clock for sampling the incoming WDATA.
46	FSVDD	S	**Analog Supply** Dedicated +5v for the Frequency Synthesizer circuitry.

* XTLO and BCS are inversions of XTLI and MCS respectively and this IOMAP is not bidirectional.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
47	FSVSS	S	**Analog Ground** Dedicated ground for the Frequency Synthesizer circuitry.
49(52)	FSPMP	A	**Frequency Synthesizer Pump** Charge pump for the frequency synthesizer PLL.
50-52 (37,44,49)	$\overline{\text{PORT2-0}}$	O	**Port Two through Zero** Open drain TTL output. These outputs are directly programmable via the microprocessor interface.
53(54†)	XTLI	I	**Crystal Input** Input to active stage of integrated oscillator circuit, this frequency establishes the frequency synthesizer reference. The reference frequency is programmable via the AD bus.
54(53†)	XTLO	O	**Crystal Output** Output from active state of integrated oscillator circuit. This output is left open if an external source is desired.
57(16)	$\overline{\text{HRESET}}$	I	**Hard Reset** When low, this input latches the reset/power-down mode.
58(20)	SGATE	I	**Servo Gate** When high, this input indicates servo operations.

* XTLO and BCS are inversions of XTLI and MCS respectively and this IOMAP is not bidirectional.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

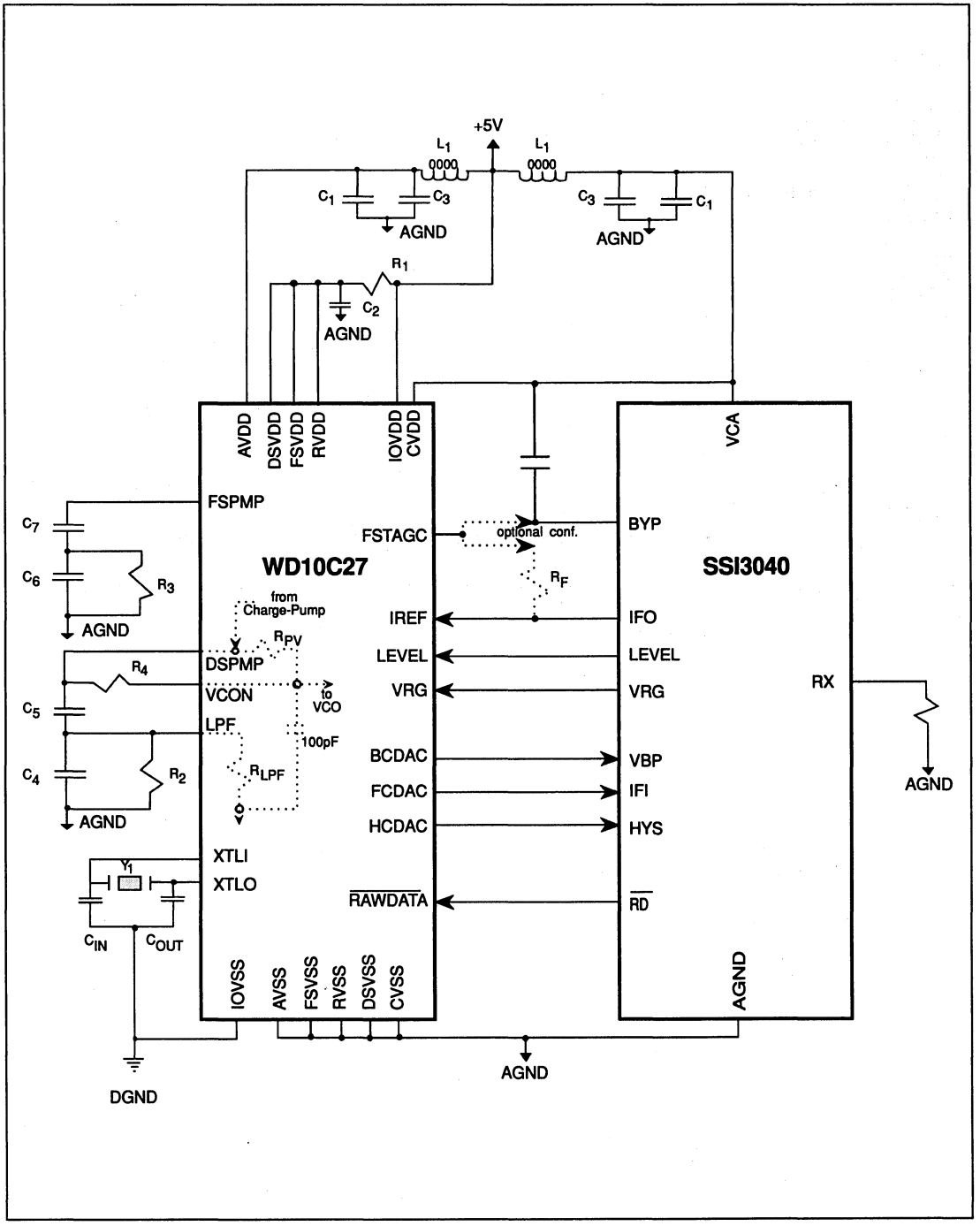

FIGURE 1-2. VARIABLE FREQUENCY CHANNEL SCHEMATIC

WD PART NUMBER	COMPONENT CHARACTERISTICS	REFERENCE DESIGNATOR
39-600000-001	Inductor, 4.7µH, 20% 4532 (3Ω max. DC Resistance)	L_1
19-600000-180	Capacitor, TANT, 22µF, 10V, 20% (C)	C_1
19-600000-171	Capacitor, TANT, 47µF, 10V, 20% (D)	C_2
17-602000-006	Capacitor, CER, 0.1µF, +80%/-20%, 50V, Z5R (1206)	C_3
17-600002-151	Capacitor, CER, 150pF, 5%, 50V, NPO (0805)	C_4
17-601000-046	Capacitor, CER, 4700pF, 5%, 50V, X7R (1206)	C_5
17-601000-098	Capacitor, CER,0.033µF, 5%, 50V, X7R (1206)	C_6
972666-022	Capacitor, CER,0.22µF, 10%, 50V, X7R (1210)	C_7
15-600003-338	Resistor, CM, 5.1Ω, 5%, 1/10 Watt, 200PPM (0805)	R_1
15-601003-346	Resistor, CM, 590Ω, 1%, 1/10 Watt, 200PPM (0805)	R_2
15-601003-347	Resistor, CM, 604Ω, 1%, 1/10 Watt, 200PPM (0805)	R_3
15-601003-414	Resistor, CM, 3.01kΩ, 1%, 1/10 Watt, 200PPM (0805)	R_4
17-600002-220†	Capacitor, CER, 22pF (/47pF/68pF), 5%, NPO, (0805)	C_{OUT}
17-600002-330†	Capacitor, CER, 33pF (/68pF/100pF), 5%, NPO, (0805)	C_{IN}
	Crystal Oscillator (≤40 MHz)‡	Y_1

† Loading capacitor values are dependent on the selection of crystal frequency. These part numbers are given as examples only. See Table 9-11 - Crystal Oscillator Timing Specifications for appropriate load capacitor values. Not required when an external source is supplied.

‡ When an external source is provided, XTLO is left floating.

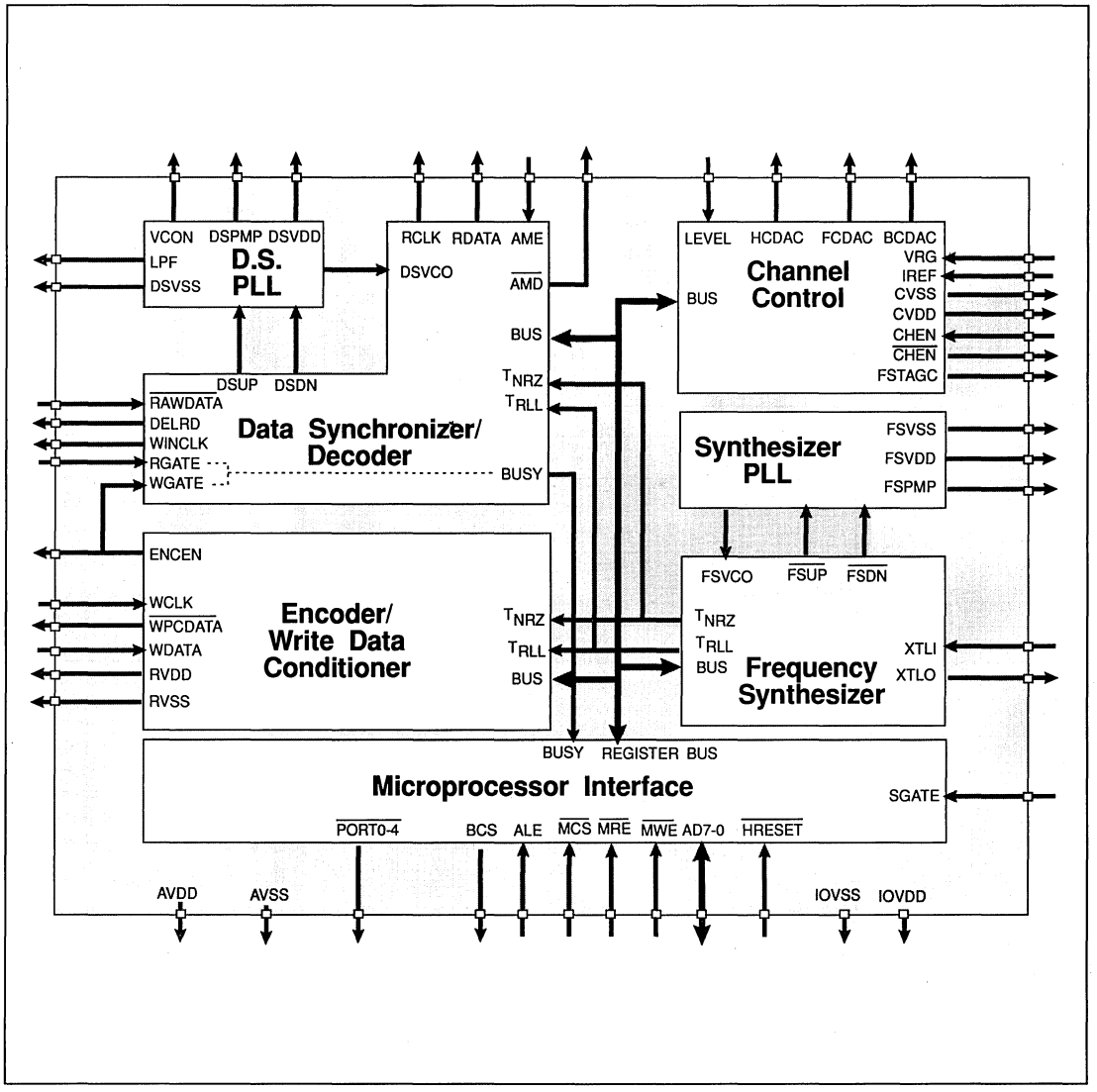

FIGURE 1-3. WD10C27 BLOCK DIAGRAM

2.0 MICROPROCESSOR INTERFACE

The WD10C27 provides an 8- bit interface to the microprocessor for programmability. The interface is compatible with the Intel multiplexed address/data bus architecture. Virtually all of the sub-systems within the WD10C27 are accessible via this interface. The processor interface is decoupled from the input pads during disk reads/writes (i.e., RGATE or ENCEN true) to reduce the possibility of unwanted disturbances to sensitive signal processing. Ensuring that de-coupling is performed is accomplished by deactivating the BZOVR (busy override) bit in the Configuration register. In either configuration, registers should never be modified unless the Hard Disk Controller is not indicating a busy status.

2.1 REGISTER ACCESS

Registers are accessed by placing the correct address word on the AD bus and latching this address on the falling edge of ALE. Subsequent reads/writes will access the addressed registers. Read/writes are performed when MCS is low and the MRE/MWE lines are strobed.

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
1 1 0 0 0 0 0 0	TEST0	Test Modes Zero
1 1 0 0 0 0 0 1	TEST1	Test Modes One
1 1 0 0 0 0 1 0	TEST2	Test Modes Two
1 1 0 0 0 0 1 1	TSTADD1	Test Address One
1 1 0 0 0 1 0 0	TSTADD2	Test Address Two
1 1 0 0 0 1 0 1	WSCOD	Window Synthesizer Clock Oscillator Divider
1 1 0 0 0 1 1 0	WSVCOD	Window Synthesizer VCO Divider
1 1 0 0 0 1 1 1	SAM	Window Synthesizer Amplifier
1 1 0 0 1 0 0 0	FCDAC	Frequency Control DAC
1 1 0 0 1 0 0 1	BCDAC	Boost Control DAC
1 1 0 0 1 0 1 0	HCDAC	Hysteresis Control DAC
1 1 0 0 1 0 1 1	SFCDAC	Servo Frequency Control DAC
1 1 0 0 1 1 0 0	SBCDAC	Servo Boost Control DAC
1 1 0 0 1 1 0 1	SHCDAC	Servo Hysteresis Control DAC
1 1 0 0 1 1 1 0	FSCOD	Frequency Synthesizer Clock Oscillator Divider
1 1 0 0 1 1 1 1	FSVCOD	Frequency Synthesizer VCO Divider
1 1 0 1 0 0 0 0	WPC10	Write Precompensation One/Zero
1 1 0 1 0 0 0 1	WPC32	Write Precompensation Three/Two
1 1 0 1 0 0 1 0	WPC54	Write Precompensation Five/Four
1 1 0 1 0 0 1 1	WPC76	Write Precompensation Seven/Six
1 1 0 1 0 1 0 0	WPC98	Write Precompensation Nine/Eight
1 1 0 1 0 1 0 1	WPC1110	Write Precompensation Eleven/Ten
1 1 0 1 0 1 1 0	WPC1312	Write Precompensation Thirteen/Twelve
1 1 0 1 0 1 1 1	WPC1514	Write Precompensation Fifteen/Fourteen
1 1 0 1 1 0 0 0	WPC1716	Write Precompensation Seventeen/Sixteen
1 1 0 1 1 0 0 1	WPC1918	Write Precompensation Nineteen/Eighteen

TABLE 2-1. REGISTER ADDRESS MAP

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
1 1 0 1 1 0 1 0	WFC2021	Write Precompensation Twenty/Twenty-One
1 1 0 1 1 0 1 1	-	Unused
1 1 0 1 1 1 0 0	CFG0	Configuration Zero
1 1 0 1 1 1 0 1	CFG1	Configuration One
1 1 0 1 1 1 1 0	CFG2	Configuration Two
1 1 0 1 1 1 1 1	CFG3	Configuration Three

TABLE 2-1. REGISTER ADDRESS MAP (Continued)

All registers in the WD10C27 are read/write registers, with the exception of the Version ID Register. As previously stated, register access is limited to times when disk read/write operations are inactive. In addition, registers are not readable during low power modes (i.e., RSTPDN and ARSTPDN active.) Register bits correspond to bits 7-0 of the AD bus such that the most significant maps to AD7, the least significant to AD0.

The internal read data bus utilizes a repeater which will latch this bus to the value of the register which was last read and for which the address is not "unused." All registers load asynchronously, thereby requiring no clocks to the device. Exceptions are the Frequency Synthesizer and the Window Shift Synthesizer Registers.

For the Frequency Synthesizer, reads/writes are performed to a master stage. The slave is not updated until synchronization circuitry has deemed it appropriate. This requires XTLI and Frequency Synthesizer VCO clocks.

The WSS will not allow loads to its registers when WSSEN is active.

Following a hard reset on $\overline{\text{HRESET}}$ input, the ARSTPDN bit in the Configuration register will be latched and all other register bits placed in their specified initial state.

Following a soft reset/power down mode, the reset must first be deactivated and then all registers re-configured (excluding CFG3). While re-configuration may be performed immediately following deactivation of the low power modes, reads may not be performed until after the specified setting time, ensuring the output drver's bias generators have become fully operational.

2.2 REGISTER DESCRIPTION

There are six main registers banks in the WD10C27:

- Configuration
- Frequency Synthesizer Dividers
- Window Synthesizer Control
- Skew Symmetric Precompensation
- Channel Control
- Test

2.2.1 Configuration Registers

The configuration (CFG) registers control the basic functions of the sub-circuits. These registers are eight bits wide.

CFG0 Register:

7:RLLEN	6:WPCEN	5:WSSEN	4:PWSEN	3:PWSI	2:PWS0	1:FBS1	0:FBS0

Bit 0: Frequency Band Select Zero.
In conjunction with FBS1, FBS0 controls the Data Synchronizer, Frequency Synthesizer, and Ramp Lock Loop characteristics. See "Table 4-2 - Frequency Band Selection" for band selection.

Bit 1: Frequency Band Select One.
See Bit 0 above.

Bit 2: Percentage Window Shift Zero.
Used in conjunction with PWS1, PWS0 controls the direction of window shift when PWSEN is active.

Bit 3: Percentage Window Shift One.
See Bit 2 above.

Bit 4: Percentage Window Shift Enable.
When active, this bit enables the PWS system.

Bit 5: Window Shift Synthesis Enable.
When active, this bit enables the WSS system. Must be inactive during loads to the WSS registers. (See section 4.2.4, "Window Shifting").

Bit 6: Write Precompensation Enable.
When active, this bit enables the Pattern Dependent Precompensation system (RLLEN must be set to utilize fine resolution capabilities). (See section 5.1, "Pattern Dependent Precompensation").

Bit 7: Ramp Locked Loop Enable.
This bit, when set in conjunction with WPCEN, activates the fine resolution capabilities of the write precompensation sub-circuit. (See section 5.1, "Pattern Dependent Precompensation").

CFG1 Register:

7:TSTEN	6:ENODD	5:AMODD	4:ARSTPDN	3:RSTPDN	2:$\overline{\text{BZOVR}}$	1:IOMAP	0:BYPMODE

Bit 0: Bypass Mode.
When active, this bit enables the bypass mode of the FSTATT pin. when inactive, the FSTATT pin is used to force fast attack in CHEN applications. See section 8.0, "Channel Control DACs".

Bit 1: Input/Output Mapping.
When set, this bit configures the WD10C27 input/output in accordance with the I/O map. IOMAP is logically or'd with HIZEN to ensure all outputs and analog pins are tri-stated during I/O mapping. (See "Table 1-1- Signal Description").

Bit 2: $\overline{\text{Busy Override}}$.
When active, this bit defeats the decoupling of the AD7-0 pads from the Microprocessor Interface during disk read/write operations. Override mode is not recommended. Busy should be defeated during certain test modes. (See section 2.2.6, "Test Registers".)

Bit 3: Reset/Power Down.
When active, this bit will reset/power down all functions and set all register bits to a logic zero for initialization and/or reduced power. All outputs are held inactive, and the crystal oscillator stopped. Exceptions include: FCDAC, HCDAC, and BCDAC registers and related functions, all of which are not effected by this bit; the COD and VCOD registers in both the Frequency and Window Shift Synthesizers, which are set to logic ones; and PORT0-4 bits and $\overline{\text{PORT0-4}}$ pins, which are not effected; and the $\overline{\text{CHEN}}$ and BCS outputs will remain operational. The microprocessor interface is operable during rest/power down, and reset/power down remains active until the RSTPDN bit is written off.

Bit 4: All Reset/Power Down.
This bit, when active, performs the same functions as the RSTPDN bit, with the addition that it will reset/power down the FCDAC, HCDAC and BCDAC registers and circuitry, as well as the RSTPDN bit itself. This bit will be latched upon $\overline{\text{HRESET}}$.

Bit 5: $\overline{\text{AME Odd}}$. This bit controls relationship between the AME input and the NRZ code word boundary. With $\overline{\text{AMODD}}$ active, the data word is assumed to start on an odd bit in the NRZ synchronization byte (i.e. the first non-zero bit is bit 1,3,5,7); when inactive, the data word starts on an even bit (i.e., 0,2,4,6).

Bit 6: $\overline{\text{ENCEN}}$ Odd.
This bit controls relationship between the ENCEN input and the NRZ data word boundary. With $\overline{\text{ENODD}}$ active, the data word is assumed to start on an odd bit in the NRZ synchronization byte (i.e., the first non-zero bit is bit 1,3,5,7); when inactive, the data word starts on an even bit (i.e., 0,2,4,6). This bit reflects the data word boundary for GAP prior to address mark in ID fields, as well as the sync. byte following the synchronization field in DATA fields. This implies that the GAP data and synchronization byte must have the same data word odd/even boundary.

Bit 7: Test Enable.
When active, this bit enables the activation of test modes based on the contents of TEST0-3 registers. When not active, this bit serves to lockout all test modes. (See section 2.2.6, "Test Registers").

CFG2 Register:

7:$\overline{\text{HFCEN}}$	6:VLOCK1	5:VLOCK0	4:WPCPOL	3:RAWPOL	2:WMEN	1:ERRPAT	0:DECERR

Bit 0: Decoder Error.
When set, this bit represents an error detected in the $\overline{\text{RAWDATA}}$ bit stream into the Decoder. This bit should be cleared via a soft reset or an explicit write to this bit. (See section 7.2, "Decoding").

Bit 1: Error Pattern.
When high, forces the Decoder to output NRZ ones when illegal 1,7 codes sequences are encountered on the $\overline{\text{RAWDATA}}$ input. When low, NRZ zeros will be output for illegal sequences.

Bit 2: Window Monitor Enable.
When set, this bit enables the DELRD and WINCLK outputs for window monitoring capabilities. (See section 4.2.3, "Window Monitoring").

Bit 3: Raw Data Polarity.
When set, this bit selects active high leading edge polarity on the $\overline{\text{RAWDATA}}$ input. When not set, active low leading edge polarity is selected.

Bit 4: Write Precomp. Data Polarity.
When set, this bit selects active high leading edge polarity on the $\overline{\text{WPCDATA}}$ output. When not set, active low leading edge polarity is selected.

Bit 5: Velocity Lock Zero.
In conjunction with VCLOCK1, this bit set the velocity lock time for the acquisition sequence. (See section 4.1, "Acquisition Sequencer").

Bit 6: Velocity Lock One.
See Velocity Lock Zero above.

Bit 7: $\overline{\text{High Frequency Clock Enable}}$.
When active, this bit will divide the XTLI frequency by two at the HFCOD prior to the division which occurs at the FSCOD. (See section 3.0, "Frequency Synthesizer").

CFG3 Register:

7:VID2	6:VID1	5:VID0	4:PORT4	3:PORT3	2:PORT2	1:PORT1	0:PORT0

The upper four bits of this register are read only.

Bit 0: Port Zero.
This bit is used to set or reset the $\overline{\text{PORT0}}$ open drain output. Note that setting this bit forces $\overline{\text{PORT0}}$ low. Although these ports are unaffected by the soft reset states invoked via RSTPDN and ARSTPDN, a hard reset issued to the $\overline{\text{HRESET}}$ pin will reset the port pins effectively floating $\overline{\text{PORT0-3}}$.

Bit 1: Port One.
See PORT0 above.

Bit 2: Port One.
See PORT0 above.

Bit 3: Port One.
See PORT0 above.

Bit 4: Port One.
See PORT0 above.

Bit 5: Version Identification Zero.
VID2-0 are used to store a binary number which represents the version number of the device. The version number may be used to verify the correct iteration by the system. This bit is read only.

Bit 6: Version Identification Two.
See VID0 above.

Bit 7: Version Identification Three.
See VID0 above.

2.2.2 Frequency Synthesizer Registers

The Frequency Synthesizer is controlled by the Clock Oscillator Divider (FSCOD) and the VCO Divider (FSVCOD) which are programmed via the contents of the FSCOD and FSVCOD registers. These registers hold eight bit unsigned integers. Programming is performed using the information given in section 3.3, "Programming the FS Dividers". Pre-scaling of the input to the FSCOD is performed based on the state of the $\overline{\text{HFCEN}}$ bit in the Configuration registers.

FSCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

FSVCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

2.2.3 Window Synthesizer Registers

The Window Synthesizer Clock Oscillator Divider (WS-COD), VCO Divider (WSVCOD), and Shift Amplifier are controlled by the WSCOD, WSVCOD, and SAM registers respectively. The WSCOD, WSVCOD, and SAM registers hold four and five bit unsigned integers. These registers should be programmed using the information given in section 4.2.4, "Window Shift Synthesis."

WSCOD Register:

3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

WSVCOD Register:

4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

SAM Register:

3:SAM 8	2:SAM 4	1:SAM 2	0:SAM 1

2.2.4 Skew-Symmetric Precomp. Registers

There are twenty-two 4 bit wide nibbles which control the magnitude of precompensation for the Skew-Symmetric Precompensation system. Each nibble corresponds to a phase shift value in percent of the code bit window, T, for a given three bit sequence. The upper two bits are programmed to generate a coarse setting, while the lower two bits generate a fine setting. Eleven registers are used to hold the complete precompensation matrix, each register holding two consecutive nibbles. *Note that WPC2021 has the nibbles reversed.* See section 5.1, "Pattern Dependent Precompensation."

WPCxxxx Registers:

7:HiCoarse 1	6:HiCoarse 0	5:HiFine 1	4:HiFine 0	3:LoCoarse 1	2:LoCoarse 0	1:LoFine 1	0:LoFine 0

2.2.5 Channel Control Registers

The Channel Control registers consist of registers for controlling the three on board DACs. These registers and their associated functions remain unaffected by the RSTPDN bit. Resetting and power reduction are accomplished by the ARSTPDN bit. SGATE multiplexes the input code to the DACs between the Data bank and the Servo bank.

The DAC registers hold five bit unsigned integers representing the DAC conversion values for each of the three DACs. In addition, each register has a bit which can be used to disable the DAC for reduced power. The HCDAC has one additional bit for function control.

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FCDAC & BCDAC Registers:

5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

HCDAC Registers:

6:$\overline{\text{HCTL}}$	5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

SFCDAC, SBCDAC, and SHCDAC Registers:

4:DAC16	3:DAC8	2:DAC4	1:DAC2	0:DAC1

2.2.6 Test Registers

There are three registers which control test functions on the WD10C27 called TEST0-2. TSTEN must be active in the Configuration register before the test modes will be invoked.

Each bit in the TEST registers represents a unique mode which has been created to ensure the quality of the product through design for testability. Some of the test modes provide synchronization of otherwise asynchronous circuits, while others provide visibility of internal logic structures to ensure high fault coverage.

In addition, mutually exclusive test modes (i.e., RLBTST/NLBTST, WSUSDTST/WSLSDTST, DSFUPTST/DSFDNTST, WSFUPTST/WSFDNTST, DSPLKTST/DSVLKTST) are leveraged to enable additional test modes when both are selected.

TEST0 Register:

7:PATREC	6:WPCDC	5:ILBTST	4:CNTRS	3:FSSYNC	2:FSFDN	1:FSFUP	0:PDIO

Bit 0: Frequency and Window Shift Synthesizer Phase Detector I/O Test.
This test takes the Frequency Synthesizer's phase detector pump up and pump down outputs to AD0-1 respectively, the Frequency Synthesizer's phase detector inputs (the FSVCOD and FSCOD outputs) to AD2-3 respectively, the Window Synthesizer's phase detector pump up and pump down outputs to AD4-5 respectively, and the Window Synthesizer's phase detector inputs (the WSVCOD and WSCOD outputs) to AD6-7 respectively during reads of the special address, TSTADD1. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 1: Frequency Synthesizer Frequency Up Test.
This test forces a DC pump up error in the Frequency Synthesizer by gating off the FSCOD input to the phase detector. If both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 2: Frequency Synthesizer Frequency Down Test.
This test forces a DC pump down error in the Frequency Synthesizer by gating off the FSVCOD input to the phase detector. If both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 3: Frequency Synthesizer Synchronization Test.
This test takes the output of the HFCOD to the input of the FSVCOD as well as to the Frequency Synthesizer output for synchronous open loop testing. The ring oscillator is halted.

Bit 4: Frequency Synthesizer and Window Shift Synthesizer COD/VCOD Counts.
This test takes each of the eight counts out of the Frequency Synthesizer's FSCOD to the AD bus during reads of the FSCOD, each of the eight counts out of the Frequency Synthesizer's FSVCOD to the AD bus during reads of the FSVCOD, each of the four counts of the Window Shift Synthesizer's WSCOD to AD0-3 during reads of the WSCOD, and each of the five counts of the Window Shift Synthesizer's WSVCOD to AD0-4 during reads of the WSVCOD. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 5: Internal Loopback Test.
This bit, when set, internally activates RGATE and ENCEN, and is intended to be used in conjunction with either RLBTST or NLBTST. When used, for example with NLBTST, 3T $\overline{\text{WPCDATA}}$ will be steered internally to $\overline{\text{RAWDATA}}$ and PLL lockup achieved without a disk drive present.

Bit 6: $\overline{\text{WPCDATA}}$ DC Test.
When active, this bit causes the output on $\overline{\text{WPCDATA}}$ to remain inactive during disk write operations, resulting in DC erasure of the media. This bit will not affect the in-

ternal WPCDATA signal used during loop-back testing.

Bit 7: Pattern Recognizer Test.
When active, this bit allows special control of the precompensation circuits. Used in conjunction with a read from any of the WPC registers, the Pattern Recognizer's register selection will be dynamically directed to the AD4-0, with AD4 reflecting precompensation direction (high is late, low is early). In addition, unprecompensated data out of the Pattern Recognizer is available on AD7, AD6 and AD5 are grounded. Used in conjunction with writes to any of the WPC registers, the value written on AD4-0 will subsequently be used as a constant precompensation value, thus bypassing the Pattern Recognizer. Writes must be at least two T long, and must not be followed by a read unless XTLI is temporarily stopped.

TEST1 Register:

7:NLBTST	6:RLBTST	5:DLLTST	4:WSUSDTST	3:WSLSDTST	2:WSSYNCTST	1:WSFDNTST	0:WSFUPTST

Bit 0: Window Shift Synthesizer Frequency Up Test.
This test forces a DC pump up error in the Window Shift Synthesizer by gating off the WSCOD input to the phase detector. If both WSFUPTST and WSFDNTST are set, neither test is activated and ENCBYP test mode is enabled. During this test mode, WDATA (or RDATA is RLBTST is set) is presented to the precompensation circuits directly, bypassing the FIFO, Encoder and Pattern Recognizer.

Bit 1: Window Shift Synthesizer Frequency Down Test.
This test forces a DC pump down error in the Window Shift Synthesizer by gating off the WSVCOD input to the phase detector. If both WSFUPTST and WSFDNTST are set, neither test is activated and ENCBYP test mode is enabled. See WSFUPTST for details.

Bit 2: Window Shift Synthesizer Synchronization Test.
This test takes the input of the WSCOD to the input of the WSVCOD for synchronous open loop testing.

Bit 3: Window Shift Synthesizer Lower SAM Decode Test.
This test takes the Window Shift Synthesizer's lower eight of sixteen SAM decode values to the AD bus during reads of the SAM register. The decode is active low. Note that BZOVR must not be active. Note that if both Upper and Lower SAM Decode tests are selected, neither will be activated and the CLKRST test mode is invoked. During the CLKRST test mode, the Data Synchronizer and Frequency Synthesizer are reset. This is useful following selection of FSSYNC and/or XVCOTST modes to reset clock paths (i.e., dividers and counters, including the FSCOD and FSVCOD registers) to known states.

Bit 4: Window Shift Synthesizer Upper SAM Decode Test.
This test takes the Window Shift Synthesizer's upper eight of sixteen SAM decode values to AD bus during reads of the SAM register. The decode is active low. Note that BZOVR must not be active. Note that if both Upper and Lower SAM Decode tests are selected, neither will be activated and the CLKRST test mode is invoked. See WSLSDTST for details.

Bit 5: Delay Locked Loop Test.
When set, this bit forces the DLL control voltages to the rails and bypasses the RLL, allowing low frequency functional testing without concern for DLL/RLL frequency limitations. RAWDATA and WPCDATA pulse forming are disabled.

Bit 6: RLL Loop Back Test.
When set, this bit will internally connect

the RDATA/RCLK outputs to the WDATA/WCLK inputs for simultaneous testing of the Data Synchronizer, Decoder, Encoder, and Write Data Conditioner functions by driving RLL $\overline{\text{RAWDATA}}$ and inspecting RLL $\overline{\text{WPCDATA}}$. If both NLBTST and RLBTST are set, neither loopback test is activated and FSFUP/FSFDN and DSFUPTST /DSFDNTST test modes are modified so as to drive the Charge Pump circuits directly, requiring no digital stimulation to test pump currents. See ILBTST in TEST0.

Bit 7: NRZ Loop Back Test.
When set, this bit internally connects the $\overline{\text{WPCDATA}}$ output to the $\overline{\text{RAWDATA}}$ input for simultaneous testing of the Encoder, Write Data Conditioner, Data Synchronizer, and Decoder functions by driving NRZ WDATA/WCLK and inspecting NRZ RDATA/RCLK. If both NLBTST and RLBTST are set, neither loopback test is activated and FSFUP /FSFDN and DSFUPTST /DSFDNTST test modes are modified so as to drive the Charge Pump circuits directly, requiring no digital stimulation to test pump currents. Note that loopback tests force internal polarity consistency between $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$. See ILBTST in TEST0.

TEST2 Register:

7:PDMXTST	6:DSPLKTST	5:DSVLKTST	4:XVCOTST	3:OLPTST	2:DSFDNTST	1:DSFUPTST	0:ACQTST

Bit 0: Acquisition Sequencer Test.
This test takes the Acquisition Sequencer outputs DET6, DET9, HFDET, TIMEOUT, PLOCK, FRAMED, FIFORST, and DECERR to AD0-7 respectively during reads of the special address, TSTADD2. If the PWSD test has also been selected, neither test mode will be activated. Note that $\overline{\text{BZOVR}}$ must not be active.

Bit 1: Data Synchronizer Frequency Down Test. This test force a DC pump up error in the Data Synchronizer by gating off the data input to the phase detector. If both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 2: Data Synchronizer Frequency Up Test. This test force a DC pump down error in the Data Synchronizer by gating off the VCO input to the phase detector. If both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 3: Open Loop Test.
This test disconnects the Data Synchronizer's charge pump output, DSPMP, from the VCON pin to allow for testing of the charge pump and VCO characteristics. It also disables the voltage clamps on both the Data Synchronizer's and Frequency Synthesizer's VCOs while leaving these ring oscillators fully operational.

Bit 4: External VCO Enable Test.
When active, this bit allows for an external VCO signal to be applied on the LPF pin. The VCO signal should be at TTL levels and at a frequency which equals three times the NRZ data rate. The ring oscillator is halted.

Bit 5: Data Synchronizer Velocity Lock Test. This test will force the Data Synchronizer to remain in Velocity Lock mode by stalling the Acquisition Sequencer prior to entering Phase Lock. If both DSVLKTST and DSPLKTST are set, neither are activated, HIZEN mode is activated. When active, this mode will cause all output drivers and analog pins to be placed in a high impedance state. Exceptions include the microprocessor pins and XTL0. The microprocessor outputs may be tri-stated by asserting either RGATE or ENCEN

with $\overline{BZOVR}$ inactive, and all outputs are placed in a high impedance state.

Bit 6: Data Synchronizer Phase Lock Test. This test forces the Acquisition Sequencer and Data Synchronizer charge pump and filter into phase lock configuration to allow for testing of the PLL tracking characteristics without the need to stimulate the Acquisition Sequencer or Address Mark Detector. VCO clocks are required to synchronize phase lock to the digital circuits. $\overline{BZOVR}$ should be activated prior to setting this bit, as this test mode forces internal RGATE true and places the device in the BUSY state. Without $\overline{BZOVR}$ active, permanent lockout of the Microprocessor interface will result, requiring power down to escape the test mode. See $\overline{BZOVR}$ in the Configuration register for details. If both DSVLKTST and DSPLKTST are set, neither are activated, HIZEN mode is activated. When active, this mode will cause all output drivers and analog pins to be placed in a high impedance state. Exceptions include the microprocessor pins and XTL0. The microprocessor outputs may be tri-stated by asserting either RGATE or ENCEN with $\overline{BZOVR}$ inactive, and all outputs are placed in a high impedance state.

Bit 7: Phase Detection Multiplex Enable Test. When active, this bit directs the phase detector frequency up/down error signals to the DELRD/WINCLK outputs respectively. The WMEN bit must be set in the configuration register. (See section 2.2.1, "Configuration Registers").

3.0 FREQUENCY SYNTHESIZER

The frequency synthesizer output serves as the "crystal" reference for several sub-circuits: the Delay Locked Loop and Ramp Locked Loop circuits for scaling with data rate; the Data Synchronizer for reference when the PLL is not locked to RAWDATA; the Address Mark Detector and Acquisition Sequencer; and the Write Data Conditioner/Encoder for processing of sensitive write signals.

The WD10C27 utilizes a dual divider frequency synthesizer architecture to generate frequencies which never exceeds 140 KHz. Given this, and the flexibility of the programmable crystal input frequency, highly efficient use of zones may be accomplished.

3.1 PROGRAMMABLE FS CRYSTAL REFERENCE (XTLI)

The crystal input is designed to accept input frequencies up to 16 MHz when using the active stage, or up to 40 MHz when an external source is provided. If an external source is used, XTLO is left open. The crystal input frequency should never exceed 20 MHz unless $\overline{\text{HFCEN}}$ is active in the Configuration register. To avoid harmonic lock-up of the various PLLs, the crystal input frequency should never be removed unless a soft reset is issued after the crystal input is re-applied.

3.2 FS DIVIDER OPERATION

The digital portion of the synthesizer consists of a High Frequency Clock Oscillator Divider, a Clock Oscillator Divider to divide the input reference (XTLI), and a VCO Divider to divide the VCO output. The crystal input frequency is divided down based on the contents of the $\overline{\text{HFCEN}}$ bit in the Configuration registers, and the contents of the FSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the FSVCOD register, to match the frequency output of the FSCOD output.

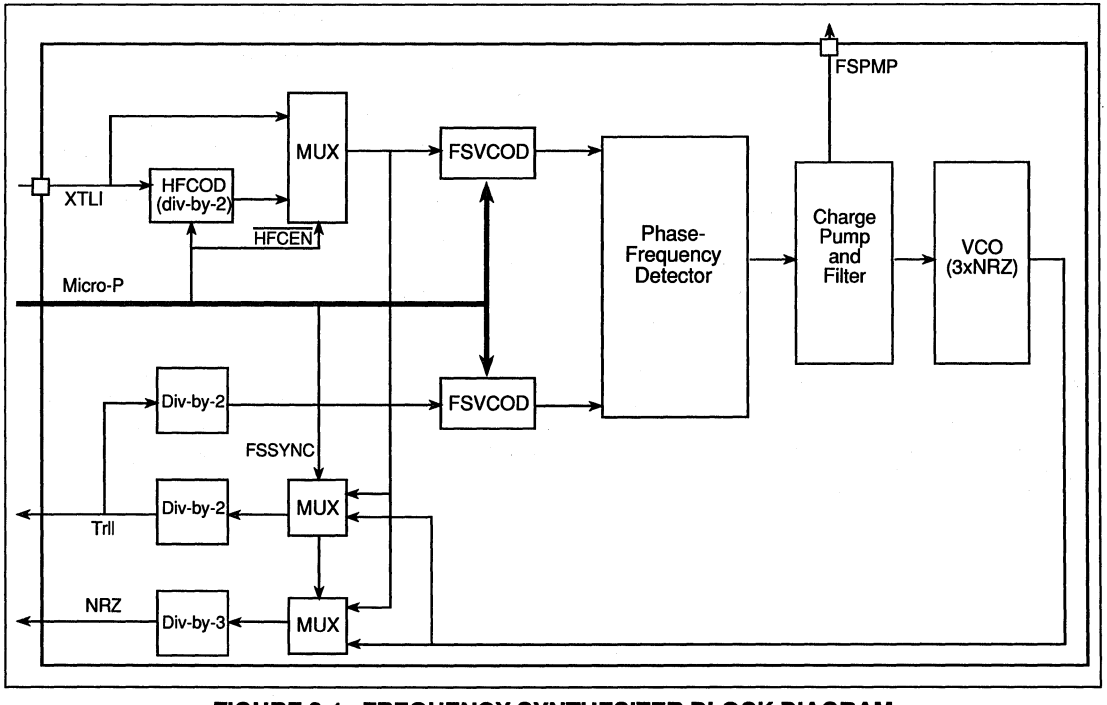


FIGURE 3-1. FREQUENCY SYNTHESIZER BLOCK DIAGRAM

The PLL architecture is almost identical to that of the Data Synchronizer. Phase-frequency locked loop synchronization is performed on the output of the FSCOD. The Charge Pump drives a VCO which utilizes a ring oscillator architecture at three times the NRZ data rate. The output of the charge pump is filtered at a very low bandwidth for high jitter rejection, while the VCO gain is modified based on the current zonal frequency to establish loop gain constancy. At the output of the Frequency Synthesizer, the VCO is operating at three times the NRZ data frequency. The NRZ and channel rate frequencies are ultimately steered to the other sub-circuits as their "crystal references". The coded rate, channel rate, or window clock, is herein referred to as T_{RLL}. The period, T, of the window clock defines the width of the phase and data detection windows. The frequency of T_{RLL} defined with respect to the NRZ data rate (f_{NRZ}), is therefore given by

EQ. 1.0

$$f_{RLL} = \frac{3 \times f_{NRZ}}{2}$$

where

EQ. 2.0

$$T_{RLL} = \frac{1}{f_{RLL}}$$

and

EQ. 3.0

$$7.5 \text{ MHz} \leq f_{NRZ} \leq 33 \text{ MHz}$$

Finally, the 3X NRZ VCO output is divided by four and used as the input to the FSVCOD.

3.3 PROGRAMMING THE FS DIVIDERS

Frequency Synthesis is accomplished by programming the FSCOD and FSVCOD registers such that the equality

EQ 4.0

$$\frac{3/4 \times f_{NRZ}}{FSVCOD + 1} = \frac{f_{HFCOD}}{FSCOD + 1} = f_{FSPLL}$$

is satisfied, where f_{HFCOD} is the pre-scaled crystal input frequency, and f_{FSPLL} is the Frequency Synthesizer PLL operating frequency range and is given by

EQ. 5.0

$$95 \text{ KHz} \leq f_{FSPLL} \leq 105 \text{ KHz}$$

Rearranging EQ. 4.0,

EQ. 6.0

$$f_{NRZ} = \frac{(4)}{(3)} \times \frac{(FSVCOD + 1)}{(FSCOD + 1)} \times f_{HFCOD}$$

it can easily be seen that the NRZ frequency is simply a ratio of the crystal reference frequency which may be pre-scaled in the HFCOD.

Because each side of EQ. 4.0 must not only satisfy the equality, but satisfy EQ. 5.0, selection of VCOD value can now be determined based on the NRZ data rate and the preferred crystal frequency. Note that to program a value of N, the registers must be loaded with a value of N-1.

The FSCOD and FSVCOD registers are eight bits, allowing for division up to 256 in both dividers. In addition, if the $\overline{\text{HFCEN}}$ (high frequency clock enable) bit in the Configuration registers is active, the XTLI frequency is divided by two in the HFCOD prior to entering the FSCOD. This results in the FSCOD values effectively being doubled, allowing for division of the input from 2 up to 512 in multiples of 2. $\overline{\text{HFCEN}}$ will be active on power up.

Minimum and maximum divider values are determined from EQ. 3.0 through EQ. 5.0 as follows. For the legal range of FSVCOD values, given the NRZ frequency range and the FS PLL range, we have

EQ. 7.0

$$\frac{3/4 \times f_{NRZ}\ (min)}{f_{FSPLL}\ (max)} \leq FSVCOD + 1 \leq \frac{3/4 \times f_{NRZ}\ (max)}{f_{FSPLL}\ (min)}$$

EQ. 7.1

$$\frac{5.625\ MHz}{105\ KHz} \leq FSVCOD + 1 \leq \frac{24.75\ MHz}{95\ KHz}$$

EQ. 7.2

$$53 \leq FSVCOD \leq 255$$

For the FSCOD values, the legal maximum is constrained by the maximum frequency of the crystal reference. This reference may never exceed 40 MHz. Since the $\overline{HFCEN}$ bit must be set for crystal reference frequencies greater than 20 MHz, the output of the HFCOD will never exceed 20 MHz.

Therefore, we have

EQ. 8.0

$$\frac{f_{HFCOD}\ (min)}{f_{FSPLL}\ (max)} \leq FSCOD + 1 \leq \frac{f_{HFCOD}\ (max)}{f_{FSPLL}\ (min)}$$

EQ. 8.1

$$\frac{0\ MHz}{105\ KHz} \leq FSCOD + 1 \leq \frac{20\ MHz}{95\ KHz}$$

EQ. 9.0

$$0 \leq FSCOD \leq 209$$

See section A.1, "Frequency Synthesizer" for software automation of these calculations.

4.0 READ CHANNEL

4.1 ACQUISITION SEQUENCER

The WD10C27 supports both hard and soft sector formats. The acquisition sequence is initiated when either RGATE or $\overline{AMD}$ are asserted. Other than the Address Mark search and timing of data acquisition off of $\overline{AMD}$, there are no further distinctions between hard and soft sector operations.

4.1.1 Soft Sector Sequencing

In soft sector formats, the Acquisition Sequence is initiated upon receipt of $\overline{AMD}$. When AME is asserted, and neither SGATE or ENCEN are active, pulse formed raw read data is synchronized to T_{RLL} and sent to the Address Mark Detection circuitry. The previously written address mark (AM) is matched, $\overline{AMD}$ is asserted and the AM search is complete.

Redundancy in the address mark creates an inherent uncertainty in the timing of $\overline{AMD}$ with respect to the synchronization field. It is therefore necessary to delay the start of the acquisition sequence to avoid acquisition to the end of the address mark. Unlike other designs which simply count three raw read data transitions from the assertion of RGATE, the WD10C27's Address Mark Detector actually uses pulse period discrimination to further qualify address mark detection. Thus, $\overline{AMD}$ is asserted only after three high frequency periods have been sensed on the raw read data following the occurrence of an address mark. This additional qualification serves to reduce the chances of false detection due to servo fields, write splices, unformated surface, defects, etc. Additionally, the acquisition sequence begins immediately upon assertion of $\overline{AMD}$, saving several bits of synchronization field lost in other schemes due to the $\overline{AMD}$-to-RGATE round trip delay.

Upon receipt of AMD, the hard disk controller should respond by asserting RGATE and de-asserting AME. The acquisition sequence is initiated upon receipt of AMD. At the end of the velocity lock time, if the hard disk controller has not yet responded with RGATE, the acquisition sequence is terminated.

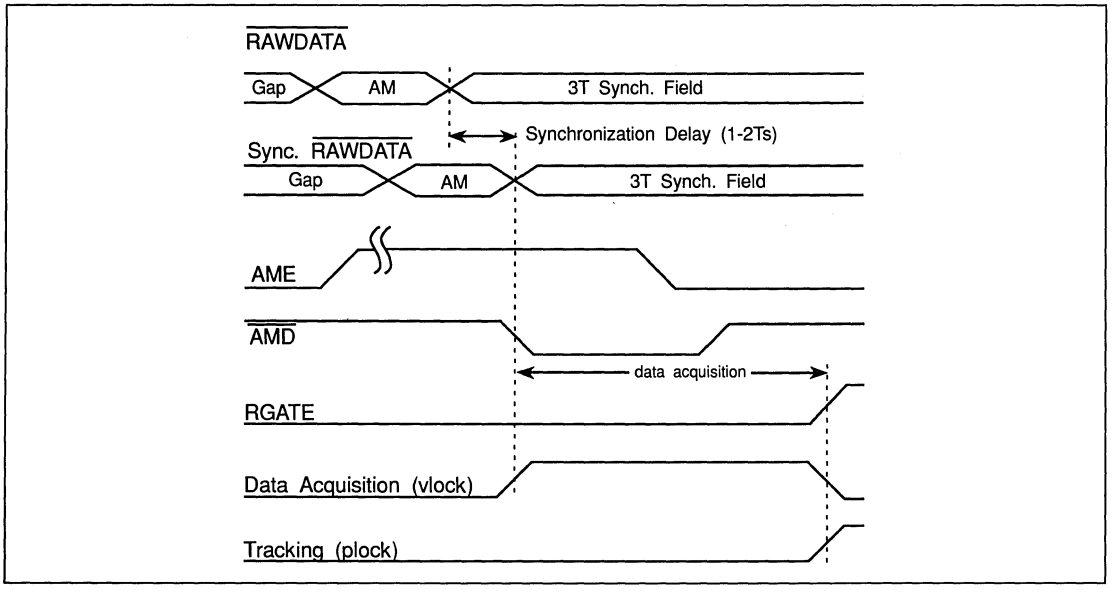


FIGURE 4-1. SOFT SECTOR TIMING

4.1.2 Data Acquisition and Tracking

For both hard and soft sector formats, upon receipt of either RGATE or $\overline{AMD}$ respectively, phase-frequency detection (velocity lock) is used to quickly and reliably acquire lock to the incoming raw read data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The velocity lock time is programmable from 5 to 8 NRZ byte times via the VLOCK0/1 bits in the Configuration register, although eight byte times is recommended.

VLOCK1	VLOCK0	Vlock Time Tvlk
0	0	60 T (5 NRZ Bytes)
0	1	72 T (6 NRZ Bytes)
1	0	84 T (7 NRZ Bytes)
1	1	96 T (8 NRZ Bytes)

TABLE 4-1. VELOCITY LOCK TIME SELECTION

At the end of the programmed velocity lock time, the Acquisition Sequencer switches the PLL to phase-only detection (phase lock). Phase lock is used to complete phase acquisition before the end of the synchronization field and enable tracking of the average channel rate as seen on the random raw read data. The phase jump at the acquisition-to-tracking switch-over due to multiplexing seen in other circuits is avoided through the use of a patented frequency switch-over circuit which guarantees zero-phase jump. However, due to the possibility of defects in the synchronization field, a minimum of four NRZ byte times (16 "001"s) are recommended to eliminate any residual phase/frequency errors.

At the switch-over from velocity lock to phase lock, several critical events occur:

- as mentioned, phase-only detection begins in the PLL
- the charge pumps/filter are switched for low gain and reduced bandwidth following synchronization to two pump pulses
- the RCLK source is redirected from the Frequency Synthesizer's reference to the Data Synchronizer's VCO, divided to the NRZ data frequency
- the Decoder begins a pattern match for 3 consecutive "001"s - when complete, framing is assured and decoded raw read data is presented on the RDATA output

When reading is complete, RGATE is de-asserted and the RCLK source will return to the Frequency Synthesizer reference, the PLL returns to high gain acquisition of the reference frequency, and the Acquisition Sequencer is re-armed to repeat sequencing when appropriate.

4.1.3 RCLK Source

In the WD10C27 architecture, it is assumed that the hard disk controller will be using RCLK during write commands as its NRZ reference clock, WCLK. To accommodate the fast ID read-to-data write times (i.e., RGATE de-assertion to WGATE assertion), RCLK must switch back to the crystal reference without the transients that are associated with acquisition back to the Data Synchronizer's reference. Therefore, at both the onset and termination of phase lock, the Frequency Synthesizer or Data Synchronizer's VCO, divided down to the NRZ data rate, is steered to the RCLK output accordingly. During this transition, RCLK will be stopped for up to two NRZ clock cycles to perform synchronization and provide a glitch-free RCLK transition.

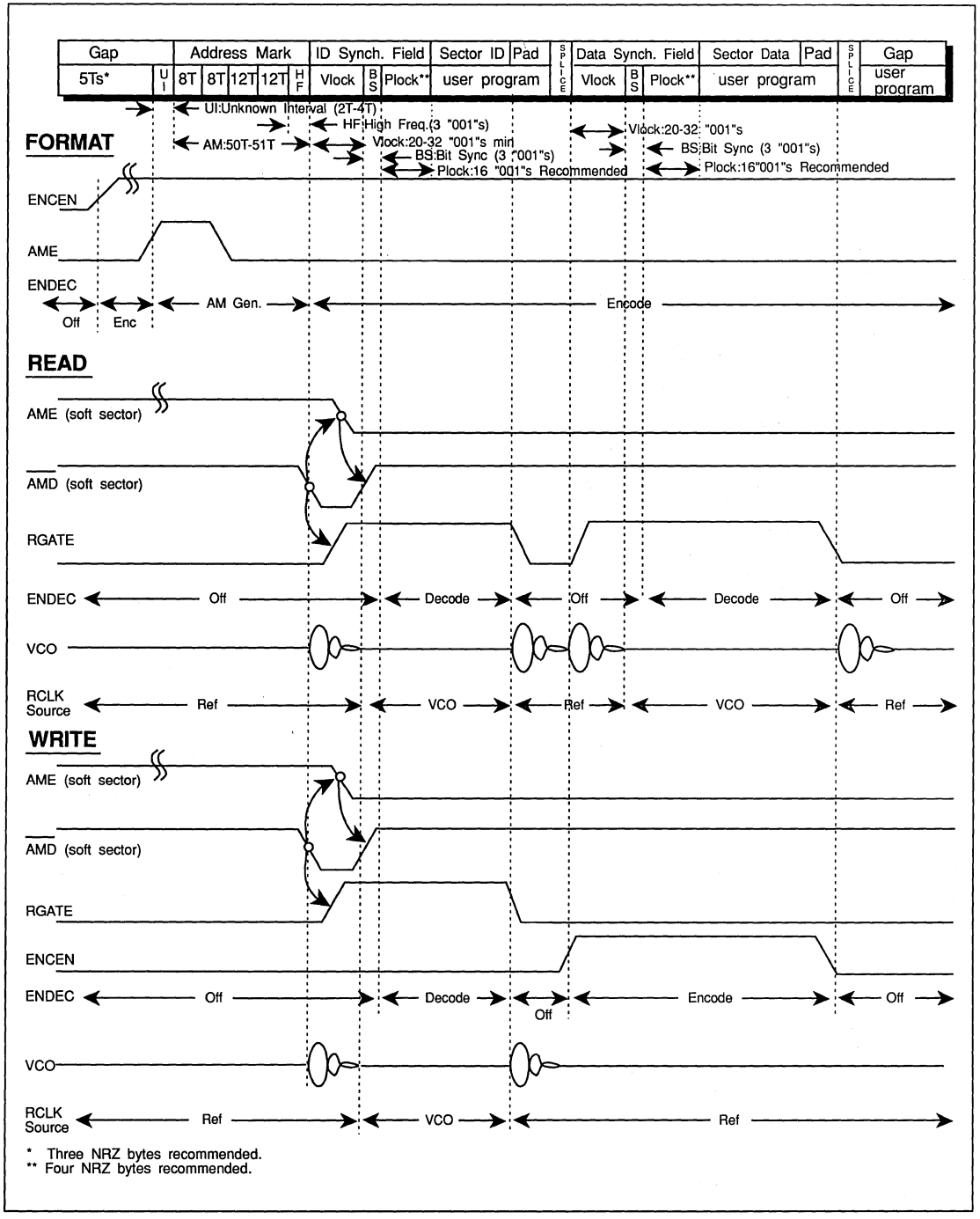


FIGURE 4-2. THE ACQUISITION SEQUENCE

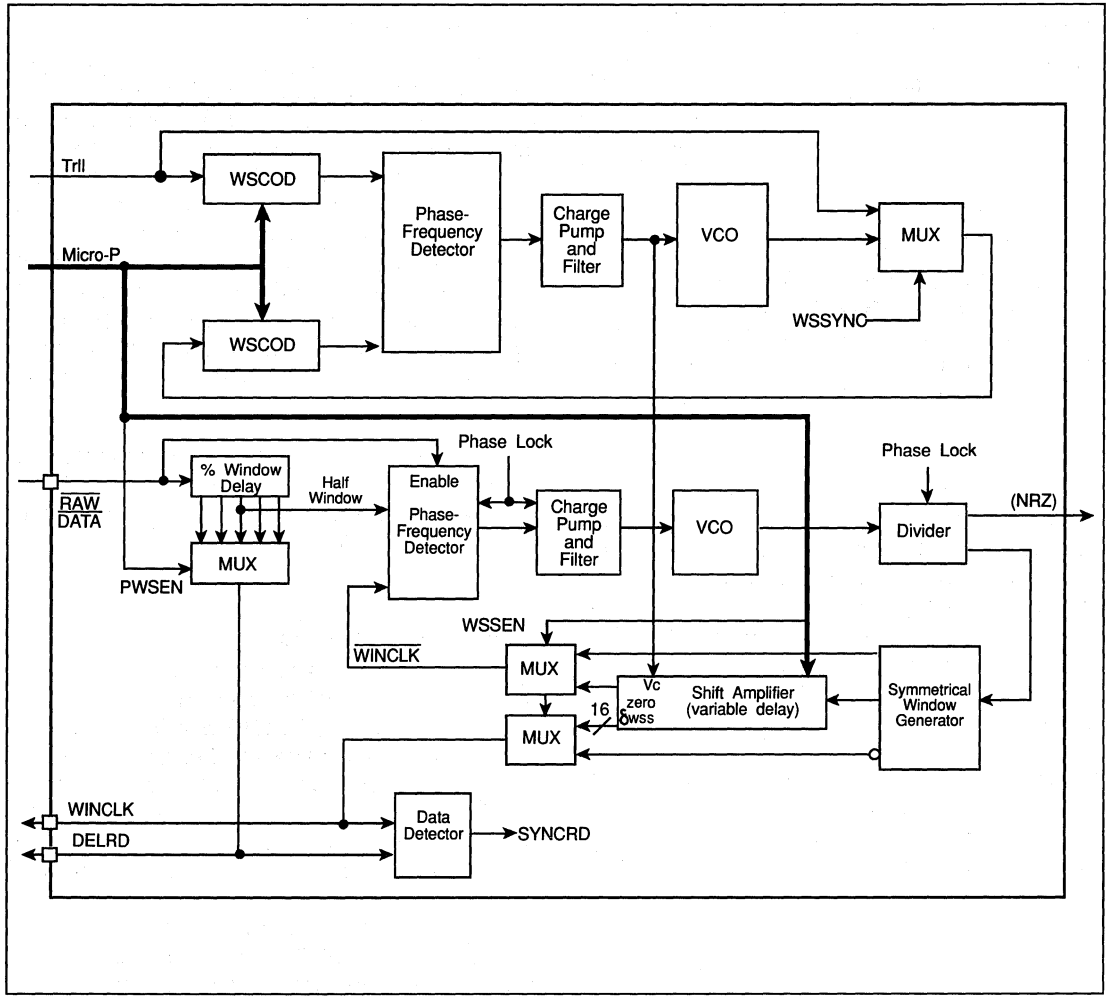


FIGURE 4-3. DATA SYNCHRONIZER BLOCK DIAGRAM

4.2 DATA SYNCHRONIZER

4.2.1 Phase-Locked Loop

The PLL is uniquely designed to eliminate the typically non-linear loop characteristics inherent in other architectures. Using a proprietary technique, the charge pump and VCO gains are inter-dependent. As VCO gain changes, the charge pumps are compensated, thus maintaining charge pump symmetry and loop gain linearity.

In most PLL designs, increased or decreased sample rates into the PLL for zoned media results in an undesirable change in loop gain. Some designs compensate by allowing for gain changes based on zonal information. This can result in phase margin loss and necessitates a compromised loop design. In contrast, the WD10C27 makes use of the zonal information not only to modify gain, but to optimize the filter characteristics. This is accomplished with no external component changes.

The VCO ring oscillator architecture is fully integrated, allowing for precise compensation of temperature, voltage, processing, and aging effects. The VCO operates at three times the NRZ data rate (two times the channel rate) and is divided down to the NRZ data rate at the RCLK output.

The WD10C27 optimizes loop gain and bandwidth using frequency information obtained via the processor interface. PLL characteristics are modified at pre-determined frequency bands, selectable via the frequency band selection bits FBS0 and FBS1 in the CFG register.

4.2.2 Window Generation

The Data Synchronizer utilizes Western Digitals proven DLL technology to generate precision phase detection window centering. The data detection window generation is accomplished via a proprietary symmetrical window generation scheme employing the 3xNRZ VCO and symmetrical CMOS circuit/layout structures. Window centering automatically tracks frequency changes, either due to components such as motor speed variations, or as a result of zonal frequency changes. This system suffers no digital losses due to setup/hold times, rise/fall variations, current imbalance, inaccurate 180 degree phase shifts, parasitics, etc.

4.2.3 Window Monitoring

Window monitoring may be performed through inspection of the DELRD and WINCLK outputs. Window centering is achieved when DELRD rising edges are centered within the rising edges of WINCLK. With the PDMXTST (phase detector multiplex test) bit active in the test registers, these outputs will reflect the digital phase error signals out of the phase detector. DELRD will represent frequency up errors, while WINCLK will represent frequency down errors. Used differentially, these signals may be used to reconstruct the error amplifier envelope during acquisition and/or tracking.

Window monitoring is enabled by activating the WMEN bit in the configuration registers. When WMEN is not set, the DELRD and WINCLK outputs will be held low.

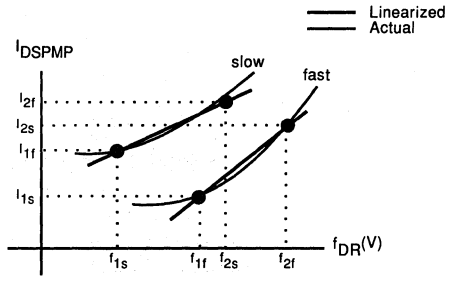
4.2.4 Window Shifting

Window shifting takes place at the Data Detector by two methods which result in a shift in the relationship between DELRD and WINCLK. The first method, Percentage Window Shift, uses the half-window delay line to advance or delay DELRD by an amount determined via the microprocessor, and which automatically scales with changes in the data rate. The second method, Window Shift Synthesis, synthesizes a delay value selected via the microprocessor and advances or delays WINCLK by the programmed amount. Both methods may be used simultaneously.

Band	FBS1	FBS0	NRZ Data Rate (MBps)	Phase Detector Gain † K_D	VCO Gain K_O	Open Loop Gain K_V	Filter Resistors			
							R_{PV} ‡		R_{LPF}	
							Int.	Ext.	Int.	Ext.
0	0	0	$7.5 \le f_{dr} \le 9.6$	K_{D0}	K_{O0}	K_{V0}	∞	3.01kΩ	∞	0Ω
1	0	1	$9.6 < f_{dr} \le 13.5$	K_{D1}	K_{O1}	K_{V1}			2.2kΩ	
2	1	0	$13.5 < f_{dr} \le 19.1$	K_{D2}	K_{O2}	K_{V2}	3kΩ		1.4Ω	
3	1	1	$19.1 < f_{dr} \le 33.0$	K_{D3}	K_{O3}	K_{V3}	1.5kΩ			

† Halved during data acquisition ‡ Shorted during data acquisition

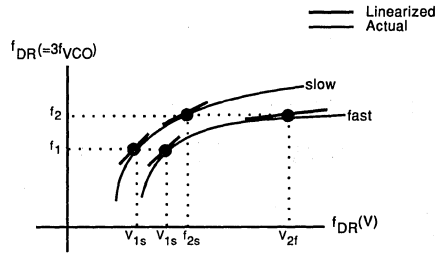
TABLE 4-2. FREQUENCY BAND SELECTION



$$K_{Dx} = \left(\frac{1}{2\pi}\right)\left(\left(\frac{I_{2x}-I_{1x}}{f_2-f_1}\right)(f_{DR}-f_1) + I_{1x}\right)\left(\frac{\mu A}{rad}\right)$$

KD_x is the linearized Phase Detector gain. I_1 and I_2 are the charge pump currents obtained at the frequency limits of the frequency bands, f_1 and f_2.

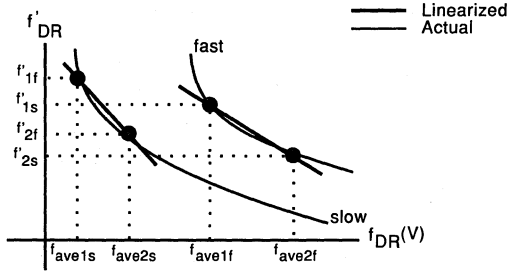
FIGURE 4-4. CHARGE PUMP GAIN CHARACTERISTIC



$$f'_{DR} = 100x\left(\frac{f(V) - f(V+\Delta V)}{f_{ave\Delta V}}\right)\left(\frac{percent}{volt}\right)$$

f'_{DR} is the VCO gain in %Δf/V at data rates f_1 and f_2, where f_1 and f_2 are the limits of the ZBR bands. ΔV is a 5-mV Change in VCON in a direction away from the band edge. f_{ave} is the average of f(V) and f(V+ΔV).

FIGURE 4-5. VCO IV CHARACTERISTIC



$$K_{Ox} = \left(\frac{f'_{2x}-f'_{1x}}{f_{ave2x}-f_{ave1x}}\right)(f_{DR}-f_{ave1x}) + f_{1x}\left(\frac{percent}{volt}\right)$$

K_{Ox} is the linearized VCO gain in %Δf/Vas a function of data rate. The gain is linearized between f'_{1x} and f'_{2x}, where f'_{1x} and f'_{2x} are defined in "Fig. 4-5, VCO IV Characteristic", and subscript "x" reflects the variation in gain associated with the fast and slow operating corners.

FIGURE 4-6. VCO GAIN CHARACTERISTIC

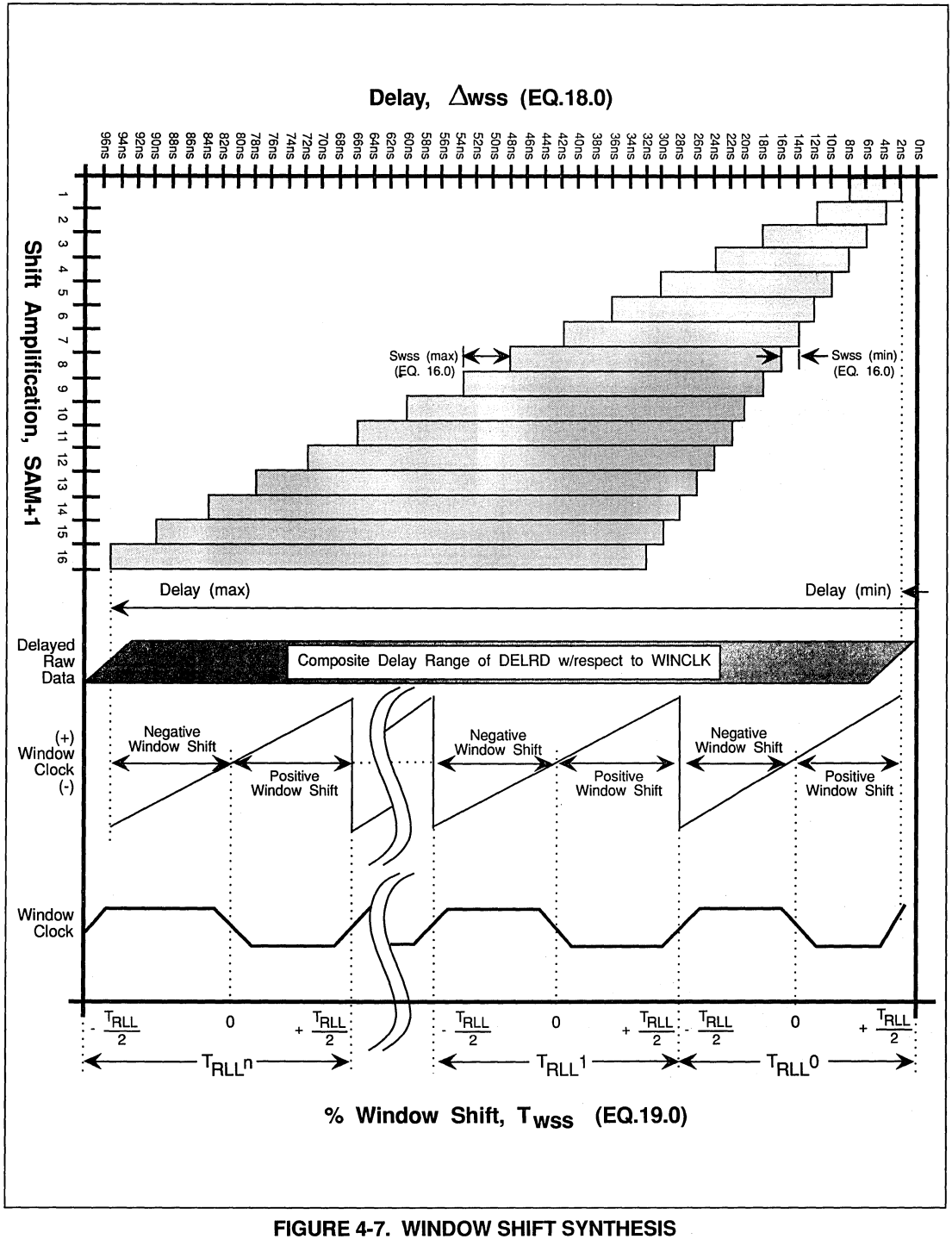


FIGURE 4-7. WINDOW SHIFT SYNTHESIS

Percentage Window Shifting

The Percentage Window Shift (PWS) approach allows for window shifting as a percentage of the window, T. This system is convenient as it is simple to use and scales with data frequencies. Window shifting can be programmed to 6.25% or 12.5% of T using this system.

PWS is enabled by activating the PWSEN bit in the CFG register, while direction and magnitude are selected by programming the PWS0 and PWS1 bits in the CFG register.

PWS1	PWS0	WINDOW SHIFT (%T_{RLL})
0	0	6.25% Early
0	1	6.25% Late
1	0	12.50% Early
1	1	12.50% Late

TABLE 4-3. PERCENTAGE WINDOW SHIFT SELECTION

Window Shift Synthesizer

The Window Shift Synthesis (WSS) system (patent pending) employed on the WD10C27 uses information programmed through the microprocessor interface to synthesize virtually any value of window shift which may be desired. Synthesis is achieved in a manner similar to the Frequency Synthesizer.

WSS is a 4-bit time DAC with a programmable synthesized LSB. Using T_{RLL} as its reference, the system synthesizes the user selected LSB value in a servo controlled delay element. Delay elements may be programmed essentially continuously across the range of 2ns to 6ns. Sixteen of these delay stages are chained back-to-back to create a tapped delay line which serves to create a user programmable amplification of the shift value developed in the servo delay element. Thus, a resultant delay of 2ns to 96ns is generated in the position of delayed raw data (DELRD) with respect to the leading edge of the detection window (WINCLK).

WSS is enabled by activating the WSSEN bit in the CFG register.

WSS Divider/Shift Amp. Operation

The digital portion of the synthesizer consists of a Clock Oscillator Divider to divide the input reference (T_{RLL}), and a VCO Divider to divide the VCO output. The T_{RLL} input frequency is divided down based on the contents of the WSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the WSVCOD register, to match the frequency output of the WSCOD.

Care should be taken never to modify the registers while WSSEN is active. Correct load sequencing is as follows: de-assert WSSEN; load the WSCOD and WSVCOD values; and assert WSSEN.

The VCO design utilizes 4.5 double inverting stages in a ring oscillator architecture. When phase-frequency lock is achieved on the output of the WSCOD, the delay through each VCO stage will be precisely controlled. These stages are duplicated in the Shift Amplifier to generate a precision delay line. The delay may be amplified by selecting anywhere from one to sixteen delay stages. Selection of the amplification is accomplished via the contents of the SAM register.

Programming the WSS Dividers/Amp.

Window synthesis calculations are similar to those in section 3.0, "Frequency Synthesizer". Programming the Window Shift Synthesizer is accomplished by programming the WSCOD and WSVCOD registers such that the equality

EQ. 10.0

$$\frac{f_{WSVCO}}{WSVCOD + 1} = \frac{f_{RLL}}{WSCOD + 1} = Fwspll$$

is satisfied. F_{RLL} is given by EQ. 1.0, and Fwspll is the Window Synthesizer PLL operating frequency range, limited such that

EQ. 11.0

$$3\ MHz \leq f_{WSPLL} \leq 15\ MHz$$

Fwsvco is the Window Synthesizer VCO frequency and is limited such that

EQ. 12.0

$$18.52\ MHz \leq f_{WSVCO} \leq 55.56\ MHz$$

Note that to program the register to a value of N, a value of N-1 must be loaded.

The WSCOD and WSVCOD registers are 4 and 5 bits respectively. Minimum and maximum divider values are determined from EQ. 4.0 through EQ. 12.0 as follows.

For the legal range of WSVCOD values, given the WSS VCO range and the WSS PLL range, we have

EQ 13.0

$$\frac{f_{WSVCO}\ (min)}{f_{WSPLL}\ (max)} \leq WSVCOD + 1 \leq \frac{f_{WSVCO}\ (max)}{f_{WSPLL}\ (min)}$$

EQ. 13.1

$$\frac{18.52\ MHz}{15\ MHz} \leq WSVCOD + 1 \leq \frac{55.56\ MHz}{3\ MHz}$$

EQ. 13.2

$$1 \leq WSVCOD \leq 17$$

For the WSCOD values, we have

EQ. 14.0

$$\frac{f_{RLL}\ (min)}{f_{WSPLL}\ (max)} \leq WSCOD + 1 \leq \frac{f_{RLL}\ (max)}{f_{WSPLL}\ (min)}$$

EQ. 14.1

$$\frac{11.25\ MHz}{15\ MHz} \leq WSCOD + 1 \leq \frac{40.5\ MHz}{3\ MHz}$$

EQ. 14.2

$$0 \leq WSCOD \leq 12$$

The Window Shift value, Twss, may now be determined as follows. As stated previously, the VCO has 4.5 double inverting stages. The frequency of the WSS VCO can therefore be given in terms of the delay of each stage, δwss, by

EQ. 15.0

$$f_{WSVCO} = \frac{1000}{9 \times \delta wss}$$

Combining EQ. 2.0, EQ. 4.0, and EQ. 15.0, we derive the relationship for the synthesized theoretical LSB, LSB_T

EQ. 16.0

$$\delta wss = LSB_T = \left(\frac{T_{RLL}}{9}\right) = \left(\frac{WSCOD + 1}{WSVCOD + 1}\right)$$

where, substituting EQ.12.0 into EQ. 16.0, we have

EQ. 16.1

$$2ns \leq LSB_T \leq 6ns$$

Since the SAM selects from one to sixteen LSB_Ts, the legal SAM values are bounded by

EQ. 17.0

$$1 \leq SAM + 1 \leq 16$$

EQ. 17.1

$$0 \leq SAM \leq 15$$

Therefore, Δwss, the total delay, from the rising edge of DELRD to the late edge of the detection window (as defined by WINCLK), may be generated by amplifying δwss by the SAM value, and is given by

EQ. 18.0

$$\Delta wss = \left(\frac{T_{RLL}}{9}\right)\left(\frac{WSCOD + 1}{WSVCOD + 1}\right)(SAM + 1)$$

Finally, the normalized window shift T*wss*, in percent T_{RLL} is given by

EQ. 19.0

$$T_{WSS} = 100 \times \left(\frac{1}{2} - MOD\left[\frac{\Delta wss}{T_{RLL}}\right]\right)$$

Where the "MOD" function in EQ 19.0 returns the fractional part of the operand.

5.0 WRITE CHANNEL

The Write Data Conditioner processes the NRZ write data (WDATA) from the hard disk controller. Encoded data is resynchronized from the encoder off of the crystal reference from the Frequency Synthesizer (T_{RLL}) to remove any sources of timing jitter. The re-conditioned write data is sent out to the write channel electronics on the $\overline{\text{WPCDATA}}$ pin, where high-to-low transitions represent the accurate crystal controlled timing edges. When $\overline{\text{WGATE}}$ is inactive, the Write Data Conditioner sleeps to conserve power. $\overline{\text{WPCDATA}}$ is held high during this time.

5.1 PATTERN DEPENDENT PRECOMPENSATION

Write precompensation is accomplished by implementation of a pattern dependent skew-symmetric precompensation matrix. A skew-symmetric matrix is defined as having zeroes along the diagonal while being symmetrical about the diagonal (except for signs). Thus, for the 7-by-7 matrix of all possible consecutive pulse period pairs (three bit combinations) in a 1,7 RLL code, if we assume no precompensation for symmetrically spaced bits (the diagonal), and precompensation of the same magnitude for non-symmetrical pulse period pairs and their mirror images.

One exception to the skew-symmetric rule is the inclusion of the 2T/2T pulse period pair. This pair has a matrix entry to account for write induced peak shift on 2T runs. Also note that although entries exist for 7T8T and 8T7T pulse period pairs, these are pairs which cannot be realized by virtue of the encode rules (8T8T is another such pair, although it has no entry due to its position along the diagonal). These entries may however be utilized at the gap-to-Address Mark transition.

The Pattern Recognizer has been designed to recognize two special cases of run length violations which can occur in soft sector applications during formats: pulse periods greater than 8T (i.e. 12T) generated in the Address Mark; pulse periods less than 2T or greater than 8T (i.e. 1T or 9T) generated at the gap-to-Address Mark transition. To handle the "greater than 8T" run length violations, the Pattern Recognizer will always force a pulse period of greater than 8T to be precompensated as an 8T. This does not effect what actually gets sent out on $\overline{\text{WPCDATA}}$. Therefore, the 8T/12T, 12T/12T, and 12T/3T intervals in the Address Mark will be precompensated as 8T/8T, 8T/8T, and 8T/3T respectively. For the case "less than 2T" run length violations, consecutive "1"s will be modified such that the second "1" in the sequence is converted to a "0" prior to entering the Pattern Recognition circuitry. Therefore, if a "11" is generated at the gap-to-Address Mark transition, the Pattern Recognizer, as well as $\overline{\text{WPCDATA}}$, will actually be a "10".

COARSE 1	COARSE 0	FINE 1	FINE 0	PHASE SHIFT
0	0	0	0	0.0000%
0	0	0	1	1.5625%
0	0	1	0	3.1250%
0	0	1	1	4.6875%
0	1	0	0	6.2500%
0	1	0	1	7.8125%
0	1	1	0	9.3750%
0	1	1	1	10.9375%
1	0	0	0	12.5000%
1	0	0	1	14.0625%
1	0	1	0	15.6250%
1	0	1	1	17.1875%
1	1	0	0	18.750%
1	1	0	1	20.3125%
1	1	1	0	21.8750%
1	1	1	1	23.4375%

TABLE 5-1. PRECOMPENSATION SELECTION

Write precompensation is enabled through the microprocessor interface by activating the WPCEN bit in the CFG register. Precompensation takes place by means of a pattern detector which determines the distance of the previous and next bits to the current bit.

The pulse period pair which has been detected addresses the WPC registers, keeping track of the order of the pulse periods, or sign. This information is passed to the Write Precompensation circuits for appropriate phase shifting of the WPCDATA output.

The WPC registers have two bits for coarse precompensation selection and two bits for fine resolution, both based on a percentage of the code bit window, T. The value of the coarse setting will be summed with the value of the fine setting to produce a resultant precompensation value, as depicted in "Table 5-1, Precompensation Selection".

RLLEN must be set in the configuration registers to utilize the fine resolution capabilities. If RLLEN is disabled, the Ramp Locked Loop (RLL), which performs fine resolution precompensation, will be powered down and the fine resolution settings in the WPC registers disregarded. Because the RLL needs time to acquire and lock to its internal reference, this bit should be enabled well in advance of a write operation, as indicated by the timing specifications of the RLL.

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Next Pulse Period (Trailing)	Previous Pulse Period (Leading) 2T	3T	4T	5T	6T	7T	8T
8T	+WPC16	+WPC17	+WPC18	+WPC19	+WPC20	+WPC21	
7T	+WPC12	+WPC13	+WPC14	+WPC15	+WPC7		-WPC21
6T	+WPC8	+WPC9	+WPC10	+WPC11		-WPC7	-WPC20
5T	+WPC4	+WPC5	+WPC6		-WPC11	-WPC15	-WPC19
4T	+WPC2	+WPC3		-WPC6	-WPC10	-WPC14	-WPC18
3T	+WPC0		-WPC3	-WPC5	-WPC9	-WPC13	-WPC17
2T	+WPC1	-WPC0	-WPC2	-WPC4	-WPC8	-WPC12	-WPC16

TABLE 5-2. SKEW SYMMETRIC MATRIX MAP

6.0 ADDRESS MARK GENERATION/DETECTION

For soft sector formats, the WD10C27 supports address mark generation and detection. The following describes the AM detection rules and considerations of format during AM generation to reduce false AM detection.

6.1 ADDRESS MARK DETECTION RULES

Address mark detection is assumed to be successful only when specific pattern sequences have been detected on the synchronized raw read data. The patterns must be found in sequence according to the following rules, and only following assertion of AME. (See Table 6-1, "Address Mark Detect Sequences"):

1. Detect a "1" followed by at least six consecutive "0"s (i.e., 1...00000...)
2. Detect a "1" followed by at least nine consecutive "0"s (i.e., 1...000000000...) no more than 3 NRZ byte times following detection of sequence 1.
3. Detect a "1" followed by at least three consecutive high frequency (HF) intervals (i.e., ...1001001001) no more than 3NRZ byte times following detection of sequence 2.

Address marks are formatted with several unique qualities which are important in ensuring high probability of correct detection. The AM used by the WD10C27 is formatted as 8T8T12T12T3T3T3T. The leading "1" in the AM is always formatted preceding the first 8T interval in order to guarantee the interval width.

6.2 ADDRESS MARK GENERATION

When AME is asserted during disk write operations, the AM is "jammed" into the serial encoded bit stream. This is necessary to ensure that the AM placement is exact and does not depend upon synchronization to a previous interval. Jamming of the AM therefore will create an arbitrary run length between the user programmed gap and the AM. This may result in a violation of the *d* constraints of the 1,7 code, such that a 1T interval is created.

In the event that a 1T interval is created at the leading edge of the AM, the second of the two "1"s will be suppressed, and the AM sent to the write electronics will be

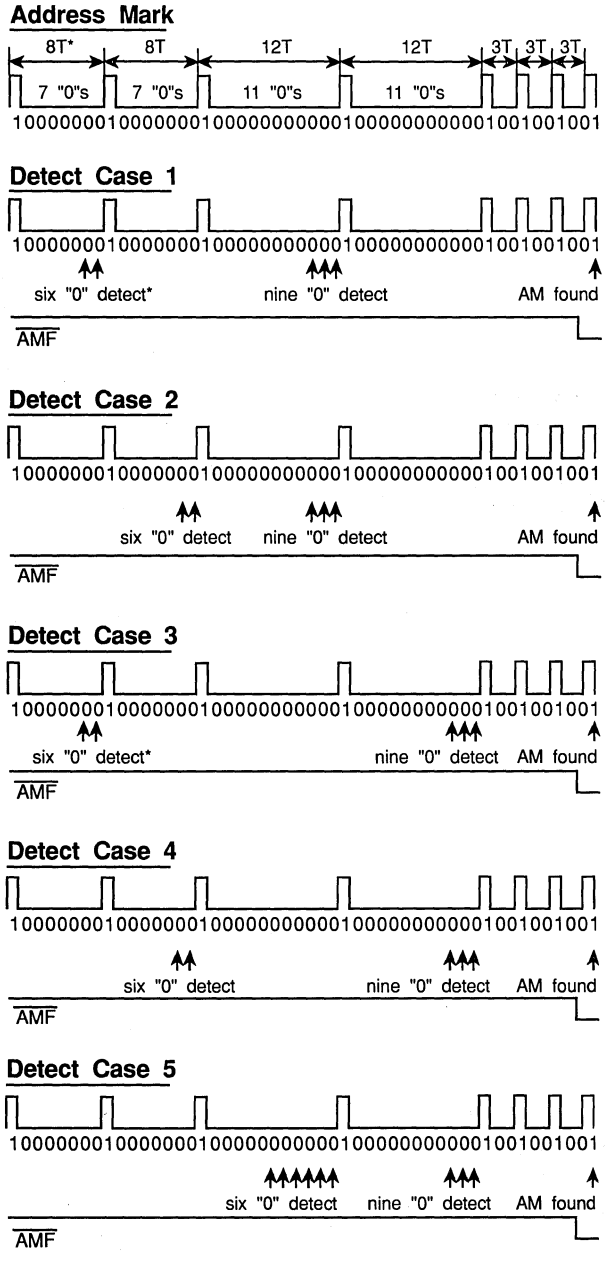
9T8T12T12T3T3T3T.

HF intervals will be formatted as three 3T (001) intervals during AM generation. The threshold of the HF detection circuitry will actually allow any interval in the range of 2T to 4T to account for asynchronisms. The frequency detection portion of the AM recognition process provides additional protection against false detection during write splices and unformated surface. Programming the user gap prior to the AM with a constant 5T pattern will guarantee that any false detection of six and/or nine "0" intervals, will not result in an address mark detection, as the 5T gap falls outside the threshold of the HF detection circuitry. False detections of this kind are not unlikely, as a 6T interval in a data field CRC, followed by a 9T interval in the write splice is entirely possible.

To prevent lockup of the detection circuitry, time-outs are provided for nine "0" detection and for HF detection. As can be seen from "Table 6-1, Address Mark Detect Sequences", several AM detection sequences are possible. In the most extreme case (Case 3), nine "0"s should be detected no more that 34T after the six "0" detect, remembering that the six "0" detect may actually occur 1T earlier in the event that the AM begins with a 9T. Similarly, HF must be detected no later than 24T following detection of nine "0"s.

In the event that either a six "0" detect or a six "0"/nine "0" detect is tripped in the write splice preceding the gap, the gap length needs to be long enough that the respective time-outs do not occur within the real AM following the gap. This is accomplished by formatting a gap length of no less than 3 NRZ bytes.

In summary, formatting a minimum of 3 NRZ bytes of 5T gap prior to any AM will greatly reduce the susceptibility to false AM detection. This can be done with a repeating $735CD_H$ NRZ gap pattern assuming even framing, or a $35CD7_H$ repeating for odd framing.



* The leading 8T interval may increase to 9T, thus the six "0"s will be detected 1T earlier.

TABLE 6-1. ADDRESS MARK DETECT SEQUENCES

7.0 ENCODER/DECODER

Encoding and Decoding in the WD10C27 is based on the IBM 2/3, 1, 7 RLL code. The following sections describe the Encoder, Decoder, and related framing issues.

7.1 ENCODING

NRZ data is encoded based on five bits: the current NRZ data word, C_1C_0, the next NRZ data word, N_1N_0, and the last bit of the previous RLL code word, R_0. These five bits are used to produce the current three bit RLL code word, $R_2R_1R_0$.

Although intended to reflect the Decode process, Figure 7-1 - Code Word to Data Word Relationship exemplifies the 2/3 rate relationship between the NRZ data word and RLL code word.

7.2 DECODING

Synchronized RLL data is decoded based on seven bits: the current three bit RLL code word, $C_2C_1C_0$; the last two bits of the previous code word, P_1P_0; and the first two bits of the next code word, N_2N_1. The seven bit sequence is analyzed and the appropriate two bit NRZ data word, Z_1Z_0, is output.

At the velocity lock-to-phase lock transition, the Data Detector is enabled and the Decoder begins to see synchronized RLL data and clock. Although the synchronization field of repeating "001" is self framing for a 2/3 rate code, pattern matching is performed on the synchronized data to further ensure correct framing. When the pattern "001001001" has been detected, the Decoder is enabled and the synchronized RLL data is decoded to NRZ and presented at the RDATA output.

The NRZ data words are clocked into a FIFO at the channel rate established by the Data Synchronizer. The FIFO output is clocked off of the Data Synchronizer's NRZ clock and presented at the RDATA output centered about the rising edges on RCLK.

CASE NO.	NRZ DATA WORD IN		RLL CODE WORD OUT	
	Current C_1C_0	Next N_1N_0	Previous R_0	Current $R_2R_1R_0$
1	00	00	0	001
2	00	00	1	001
3	00	01	0	001
4	00	01	1	001
5	00	10	0	000
6	00	10	1	010
7	00	11	0	000
8	01	11	1	010
9	01	00	0	001
10	01	00	1	010
11	01	01	0	001
12	01	01	1	000
13	01	10	0	000
14	01	10	1	000
15	01	11	0	000
16	01	11	1	000
17	10	00	0	101
18	10	01	0	101
19	10	10	0	010
20	10	11	0	010
21	11	00	0	010
22	11	01	0	100
23	11	10	0	100
24	11	11	0	100
Exhaustive encode pattern: $0132149AD7E3770_{HEX}$				

TABLE 7-1. EXPANDED 1,7 ENCODE RULES

Of the 128 possible combinations of the seven bit decode word given by $P_1P_0C_2C_1C_0N_2N_1$, all but 34 have adjacent ones and are therefore illegal due to the *d* constraints of the 1,7 RLL code. Although the decode table may be reduced to less than 34 entries, the expanded table has been presented here for your convenience.

If the Decoder sees a "11" anywhere in the decode word, the NRZ data word will be forced to either a "00" or "11" based on the stated of the ERRPAT bit in the Configuration register, and the DECERR bit will be set to indicate that a decode error has occurred.

There are other RLL sequences which may not be realized by virtue of the encode rules, however these do not result in decode errors, In other words, since the encode rules are a subset of the decode rules, there are many RLL sequences which may be decoded legally, but which could never have been encoded to start with. This is evident when the Encode-Decode process is run in reverse. For certain RLL sequences, including those containing 7T7T7T...7T, 7T87, 8787...87, and 8T7T, the RLL output of the Encoder will not match the original RLL input to the Decoder. Another obvious example is a sequence of more than seven zeroes. While this is an illegal Encode due to the *k* constraints in the 1,7 RLL code, the Decoder will simply output 0101... (case 1) in response to this constant zero input.

Therefore, determination of a NRZ sequence which results in a specific RLL sequence may not necessarily be accomplished by use of the Decoder. The Encode-Decode process is not guaranteed to run in reverse.

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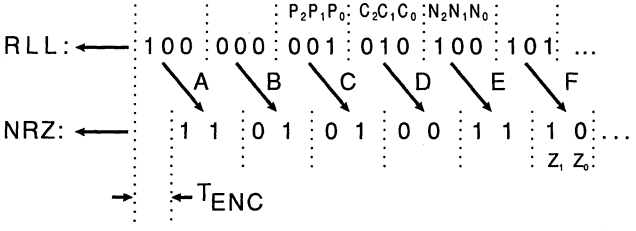
Code Word Relationship



Decode Table Entry

	$P_1P_0C_2C_1C_0N_2N_1 \rightarrow Z_1Z_0$
A) Case 9	XX10000 → 11
B) Case 1	0000000 → 01
C) Case 5	0000101 → 01
D) Case 21	0101010 → 00
E) Case 12	1010010 → 11
F) Case 10	00101XX → 10

FIGURE 7-1. CODE WORD TO DATA WORD RELATIONSHIP

Case No.	1,7 RLL Code Word			NRZ Data Word
	Previous $P_1 P_0$	Current $C_2C_1C_0$	Next $N_2 N_1$	NRZ $Z_1 Z_0$
1	00	000	00	01
2	00	000	01	01
3	00	000	10	01
4	00	001	00	01
5	00	001	01	01
6	00	010	00	11
7	00	010	01	10
8	00	010	10	10
9	00	100	00	11
10	00	100	01	11
11	00	100	10	11
12	00	101	00	10
13	00	101	01	10
14	00	000	00	01
15	01	000	01	01
16	01	000	10	01
17	01	001	00	00
18	01	001	01	00
19	01	010	00	01
20	01	010	01	00
21	01	010	10	00
22	10	000	00	00
23	10	000	01	00
24	10	000	10	00
25	10	001	00	00
26	10	001	01	00
27	10	010	00	11
28	10	010	01	10
29	10	100	00	11
30	10	100	01	11
31	10	100	10	11
32	10	101	00	10
33	10	101	01	10
34	10	101	01	10
Exhaustive decode pattern: 010200402202412122512445104205210124 25 OCT				

TABLE 7-2. EXPANDED 1,7 DECODE RULES

7.3 FRAMING

Framing is the determination of a specific data word to code word boundary. Framing during the decode process is assured by the 001 pattern in the synchronization field. This pattern is self-framing in the sense that the code work boundary is unambiguous. However, as the encode process has no synchronization byte, the Encoder must make some assumptions about the data word boundary. For example, if the NRZ sequence on WDATA is ...000000101001000..., it is important to know if this should be encoded as ...00/10/10/01/00... or as ...00/01/01/00/10/00..., as these will produce different encoded sequences.

7.3.1 Framing in Hard Sector Formats

Upon assertion of ENCEN and after some synchronization delay, WDATA is shifted into a FIFO on the rising edges of WCLK. The output of the FIFO is clocked using the channel rate clock, T_{RLL}. In this way, two bits of WDATA are presented to the Decoder for every 3 T_{RLL}'s satisfying the 2/3 code rate requirement of 1,7 RLL.

Framing during the encode process is accomplished via the $\overline{\text{AMODD}}$ and $\overline{\text{ENODD}}$ bits in the configuraiton register. Framing following address marks is based on the sense of $\overline{\text{AMODD}}$, and is discussed in 7.3.2 Framing In Soft Sector Formats.

$\overline{\text{ENODD}}$ established framing for encoding following assertion of ENCEN. In soft sector formats, this applies to gap data which precedes the AM, and to user data following the synchronization field. When $\overline{\text{ENODD}}$ is active (low), framing will be established assuming that the two bit NRZ data word begins on an odd numbered bit in the NRZ data byte. Thus, the first transition on WDATA must occur in bits 7, 5, 3 or 1 of the NRZ byte $N_7N_6N_5N_4N_3N_2N_1N_0$, and the NRZ data words N_7N_6, N_5N_4, N_3N_2, N_1N_0, etc., will be encoded. If $\overline{\text{ENODD}}$ is inactive (high), framing will be even such that the NRZ data words N_6N_5, N_4N_3, N_2N_1, N_0N_7, etc., are encoded. In this case, the first transition on WDATA must occur in bits 6, 4, 2 or 0.

As an example, the sequence ...00AA$_H$..., if intended to be encoded as ...00/00/10/10..., would require $\overline{ENODD}$ = 0 to establish odd framing. $\overline{ENODD}$ = 1 would result in encoding this same sequence as ...00/00/01/01... It can be seen from Table 7-1 - Expanded 1,7 Encode Rules that these two Encoder inputs will result in different RLL outputs.

Since ENCEN is asserted prior to gap during formats, and prior to data fields during writes, the odd/even framing requirement must be consistent. This implies that the data field synchronization byte, usually written just after the synchronization field, and the 5T gap data must both have either odd or even framing.

7.3.2 Framing in Soft Sector Formats

Framing must be re-established following the insertion of address. While $\overline{ENODD}$ is used to establish framing following assertion of ENCEN for gaps and data field synchronization bytes, $\overline{AMODD}$ is similarly used following assertion of AME to establish framing for ID synchronization bytes.

Following the address mark generation, WDATA is once again encoded and shifted out to $\overline{WPCDATA}$. Because WDATA must be 00H following the AM to generate the 3T synchronization field, framing does not take place until the first non-zero transition is seen on WDATA. At this time, framing is forced to be either odd or even as described above.

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8.0 CHANNEL CONTROL DACS

The WD10C27 provided three DACs which have been specifically designed to optimize the variable frequency read channel's frequency, boost, and hysteresis characteristics. The DACs have been specifically designed to be compatible with the SSI3040 Electronic Filter/Pulse Detector. In addition, a unique method of maintaining servo field optimization is also incorporated.

In a typical application, each DAC is programmed based on the optimization cut-off frequency, hysteresis, and boost settings for a given zone. These values are loaded into the DAC control registers as a 5-bit unsigned integer. Independent values, optimized for the servo fields, are loaded into the equivalent servo control registers. The DAC outputs are then dynamically switched between the logical and servo settings via the SGATE input.

DACs should be enabled by setting the DACEN bit in the respective DAC control register. When a DAC is disabled, the output is placed in a high impedance state and power shut off to the relevant circuits. The reset/low power states invoked via the ARSTPDN bit in the Configuration regists clear the DAC registers and thereby leave the DACs disabled. Reset/low power mode, issued via the RSTPDN bit, will not have any effect on the DAC functions.

8.1 FAST AGC

When DAC settings are being modified "on-the-fly", special considerations must be made to keep the AGC recovery times at a minimum. This includes not only the "data-to-servo" and servo-to-data" recovery at the SGATE transitions, but the recovery times encountered at the leading edge of CHEN when duty cycling CHEN for power management. See 8-2, "Duty Cycling with CHEN".

In much the same way as a "write-to-read" recovery scenario, it is desirable to assure that AGC is in a fast attach whenever the DACs are switched. Whenever a modification to the cutoff frequency is made such that the cutoff frequeency is reduced, the effect is to place the AGC circuits in a slow dacay mode. This is highly undesirable as the AGC recovery time may be extremely long. Unfortunately, this situation arises whenever the cutoff frequency in the servo fields is lower than in the data zones.

The FSTABC (fast AGAC) pin has been provided to force fast AGC recovery. By setting the BYPMODE bit in the configuration register, this pin may be connected to the BYP capacitor of the AFC circuits and used to force fast attack. On either edge of SGATE, when the DAC values switch from servo to data or vice versa, the FSTAGC pin will discharge the BYP capacitor by pulling up towards +4V. In this way, fast attack can be guaranteed.

8.2 DUTY CYCLING WITH CHEN

To provide for minimal power consumption by the channel electronics, a CHEN (channel enable) signal may be used for power management. Since servo fields represent a small percentage of the total surface format, a significant power savings may be accomplished by de-asserting CHEN during the logical fields, and asserting CHEN over the servo fields. This technique is known as "CHENing".

When CHEN is low, the DACs are forced into a configuration which will optimize read channel recovery time and minimize power consumption: the FCDAC will be forced to 8 LSB's; the BCDAC will be forced to ground; and the HCDAC will be forced to +5V.

To minimize transient response upon re-assertion of CHEN, it is desirable to keep current flowing at the IREF (IFO) and FCDAC (IFI) pins. As the current reference from the SSI3040 will be disabled when CHEN is low, a current into the IREF input may be established in one of two ways:

1. With the BYPMODE bit in the configuration register disabled, FSTAGC will be pulled towards +5V during CHEN low. By placing an external resistor between FSTAGC and IREF, a programmable current may be established. This current should be programmed such that upon re-assertion of CHEN, fast attack is guaranteed in the AGC.

2. With the BYPMODE in the configuration register enabled, an internal current source is steered to the IREF input. This current source is of sufficient tolerance to keep FCDAC and SSI3040 related circuits out of saturation. AGC fast attack is ensured via the connection of FSTAGC to the BYP capacitor.

8.3 FREQUENCY CONTROL

The Frequency Control DAC, FCDAC, has been specifically designed to allow for bandwidth optimization of the read channel. In a typical variable frequency application, selection of the channel bandwidth is made based on signal-to-noise ratio and recording frequency considerations.

FCDAC is a current DAC whose compliance is set by an external current reference applied at the IREF input. FCDAC is enabled and programmed via the FCDAC register described in section 2.2.5, "Channel Control Registers."

The FCDAC will be forced to 8 LSBs when CHEN is low.

8.4 BOOST CONTROL

The Boost Control DAC, BCDAC, has been specifically designed to allow for programmable pulse slimming. BCDAC is a voltage DAC whose compliance is set by an external voltage reference applied at the VRG input. BCDAC is enabled and programmed via the BCDAC register described in section 2.2.5, "Channel Control Registers."

Although BCDAC is a five bit DAC, the lower two counts (00000 and 00001) are used to indicate a no boost control state. When the lower two counts are programmed, the BCDAC output is clamped to ground rather than following the normal DAC progression. When used in conjunction with the SSI3040, this stated will be sensed and the 3040 will assume a nominal boost value.

Note that after ARSTPDN, BCDAC will be set to a zero count but will be disabled. Enabling the DAC without modifying the count will result in the no boost configuration.

The HCDAC will be forced to ground when CHEN is low.

8.5 HYSTERESIS CONTROL

Hysteresis Control DAC, HCDAC, has been specifically designed to allow for threshold optimization under microprocessor control. HCDAC is a voltage DAC whose compliance is set as a programmable ratio of the voltage difference seen between the LEVEL and VRG inputs. When HCDAC is connected to the hysteresis input of the pulse detector, the threshold will automatically maintain the programmed ratio as the amplitude of the voltage on the LEVEL input changes.

HCDAC is enabled and programmed via the HCDAC and SHCDAC registers described in section 2.2.5, "Channel Control Registers."

If desired, HCDAC may be converted into a voltage DAC configuration identical to that the BCDAC by disabling the HCTL bit in the HCDAC resister. When HCTL is inactive, the DAC characteristics will be as described in section 8.4, "Boost Control". In this configuration, the LEVEL input is used as a voltage reference, and the VRG input is unused.

The HCDAC will be forced to +5V when CHEN is low, regardless of the state of the HCTL bit in the HCDAC register.

9.0 PERFORMANCE SPECIFICATIONS

9.1 MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

PARAMETER	RATING	UNIT
V_{DD} with respect to V_{SS}	+7	V
Voltage on any pin with respect to V_{SS} (ground)	-0.5 to +7	V
Ambient Operating Temperature (T_A)	0 to 70	°C
Storage Temperature	-55 to +125	°C
ESD Protection	5000	V
Latchup Immunity	40	mA

TABLE 9-1. ABSOLUTE MAXIMUM RATINGS

9.2 DC ELECTRICAL CHARACTERISTICS

The following specifications are over T_A = 0°C to 70°C, T_J = 0°C to 90°C and V_{DD} = +5V ± 250mV. When indicated (*), limits represent characterized values and are not tested.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DDA} †	Active Power Supply Current		25 50 60	30 75 85	mA mA mA	@ 7.5 MBps @ 27 MBps @ 33 MBps
I_{DDLP} ‡	Power Down Supply Current		2.0 0.6	4.0 1.5	mA mA	RSTPDN=1, CHEN=1 RSTPDN=1, CHEN=0
I_{DDLPA} ‡	All Power Down Supply Current		0.3	1	mA	ARSTPDN = 1
t_{RDY}*	Time from valid configuration to full operating capability (e.g., lockup of PLLs)			3	ms	

† Measured during write operations with V_{DD} = 5.25V at 0°C.
Typical values are at ambient temperature and V_{DD} = 5.0V.

‡ Measured with all inputs at ground (or V_{DD}), V_{DD} = 5.25V, and 0°C.
Typical values are at ambient temperature and V_{DD} = 5.0V.

TABLE 9-2. POWER SUPPLY SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): XTLI, XTLO						
V_{IH}	Input High Voltage	2.0	1.4		V	$f_{XTL} \leq 16$ MHz
V_{IL}	Input Low Voltage		1.4	0.8	V	$f_{XTL} \leq 16$ MHz
V_{IBIAS}	Input Bias Voltage	1.0		1.8	V	XTLO floating, V_{DD} = 5V
I_{ILKX}	Crystal Input Leakage Current			±100	nA	XTLI = XTLO = V_{IBIAS}
I_{OLS}	Short Circuit Sink Current	1.8		10	mA	XTLO=V_{DD}=5V.XTLI=2.5V
I_{OHS}	Short Circuit Source Current	0.6		4.0	mA	V_{DD}=5V.XTLO=XTLI=0V
R_{BO}	Operating Bias Resistance	2.0		2.7	MΩ	V_{DD}=5V.XTLI=V_{IBIAS}, XTLO=0V

TABLE 9-3. CRYSTAL OSCILLATOR DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AD7-0, $\overline{\text{MWE}}$, $\overline{\text{MRE}}$, $\overline{\text{MCS}}$, *ALE, AME, ENCEN, RGATE, LPF (test),* $\overline{\text{RAWDATA}}$, *WDATA, WCLK, CHEN,* $\overline{\textit{HRESET}}$						
V_{IH}	Input High Voltage	2.0	1.4		V	
V_{IL}	Input Low Voltage		1.4	0.8	V	
I_{ILK}	Input Leakage Current			±10	µA	

TABLE 9-4. INPUT RECEIVERS DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{AMD}}$, RDATA, RCLK						
V_{OH}	Output High Voltage	2.4			V	IOH = -20 µA
V_{OL}	Output Low Voltage			0.4	V	IOL = +20 µA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT} = V_{SS} TO V_{DD}, HIZEN=1
T_{RS}*	Output Rise Time			2.5	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20 pF
T_{FL}*	Output Fall Time			2.1	ns	V_{OUT} = 2.0V TO 0.8V C_L = 20 pF
PIN(S): WINCLK, DELRD, $\overline{\text{WPCDATA}}$, $\overline{\text{CHEN}}$, BCS						
V_{OH}	Output High Voltage	2.4			V	IOH = -1mA
V_{OL}	Output Low Voltage			0.4	V	IOL = +1mA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} TO V_{DD}, HIZEN=1
T_{RS}*	Output Rise Time			2.3	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20pF. R_L = 20kΩ to V_{SS}
T_{FL}*	Output Fall Time			1.4	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20pF. R_L = 2kΩ to V_{DD}
PIN(S): $\overline{\text{PORT0-4}}$						
V_{OL}	Output Low Voltage			0.4	V	IOH = +8mA. Open Drain
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
PIN(S): AD7-0						
V_{OH}	Output High Voltage	2.4			V	IOH = -1mA
V_{OL}	Output Low Voltage			0.4	V	IOL = +1mA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
t_{RS}*	Output Rise Time			13	ns	V_{OUT} = 0.8V to 2.0V CL = 100 pF R_L = 20kΩ to V_{SS}

TABLE 9-5. OUTPUT DRIVE DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): DSPMP, VCON, LPF						
I_{ILKP}	DSPMP Input Leakage Current			±100	nA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
I_{ILKV}	VCON Input Leakage Current			±100	nA	V_{CON} = V_{DD}, HIZEN=1
I_{ILKL}	LPF Input Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
R_{PV0}	DSPMP to VCON Resistance. BAND0		∞		Ω	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PV1}	DSPMP to VCON Resistance. BAND1		∞		Ω	DSPMP=1.5V. VCON=2V, V_{CC}=5V
R_{PV2}	DSPMP to VCON Resistance. BAND2	2.0	3.01	4.9	kΩ	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PV3}	DSPMP to VCON Resistance. BAND3	1.0	1.5	2.45	kΩ	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PVV}	DSPMP to VCON Vlock Resistance	50		1700	Ω	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{LPF0}	LPF Resistance to ground. BAND0		∞		Ω	LPF = 200mV, V_{DD}=5V
R_{LPF1}	LPF Resistance to ground. BAND1	1.3	2.2	4.3	kΩ	LPF = 200mV, V_{DD}=5V
R_{LPF2}	LPF Resistance to ground. BAND2	0.8	1.4	2.7	kΩ	LPF = 200mV, V_{DD}=5V
R_{LPF3}	LPF Resistance to ground. BAND3	0.48	0.7	1.65	kΩ	LPF = 200mV, V_{DD}=5V

TABLE 9-6. DATA SYNC. INTERNAL FILTER DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): DSPMP, VCON						
V_{HFCA}	VCO High Freq. Clamp Act. Voltage †	2.7		3.9	V	$I_{DSPMP} \geq 2.5mA$, $V_{DD}=5V$
V_{HFCD}	VCO High Freq. Clamp De-act. Voltage †	0.45		1.15	V	$I_{DSPMP} \leq 2.5mA$, $V_{DD}=5V$
V_{LFC}	VCO Low Frequency Clamp Voltage ‡	0.5		0.95	V	$I_{VCON} = -1\mu A$, $V_{DD}=5V$
I_{HFC}	VCO High Frequency Clamp Current †	4		15	mA	VCON=DSPMP=V_{DD}=5V
I_{LFC}	VCO Low Frequency Clamp Current ‡	1.3		4.5	mA	VCON = 0V, V_{DD}=5V

† The VCO high frequency clamp will activate when the voltage sensed on VCON rises above the high frequency clamp activation voltage, V_{HFCA}. The clamp is latched, pulling DSPMP low and discharging the filter. When all of the VCO energy is discharged and internal VCO control voltages fall below the VCO High Frequency Clamp De-activation Voltage, V_{HFCD}, the clamp is released. V_{HFCD} is BAND dependent. Clamp voltages and currents should be measured after stopping all clocks and tri-stating the phase detector by pulsing HIZEN.

‡ The VCO low frequency clamp on when the voltage sensed on VCON falls below the VCO Low Frequency Clamp Voltage, V_{LFC}. Voltage and currents should be measured after stopping all clocks and tri-stating the phase detector by pulsing HIZEN

TABLE 9-7. DATA SYNCHRONIZER INTERNAL VCO DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): IREF, VRG, FCDAC (with CHEN=1)						
I_{REF}	External Current Reference	100		400	µA	$0.7V \leq V_{IREF} \leq 1.6V$
I_{OZ}	FCDAC Tri-state Output Leakage			±100	nA	$V_{OUT}=V_{SS}$ to V_{DD}, DACEN=0
LSB_T‡	Theoretical Resolution (5-bit)		I_{REF}/12		mA	for codes 0 through 31
GAIN‡	Gain (LSB) Accuracy			±8.0	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
$I_{INITIAL}$‡	Code Zero Current		8		LSB_R	
I_{OFFSET}‡	Offset Current			±7.0	%I_{REF}	
INL†	Integral Non-Linearity			±0.5	LSB_R	
DNL‡	Differential Non-Linearity			±0.5	LSB_R	
R_L*	External Series Resistive Load			2k	kΩ	
PSRR*	Power Supply Rejection Ratio	30	40		dB	w/o external filtering
t_S*	Setting Time from SGATE Transitions			150	ns	w/ 10pF and R_L external load to 90% of final value
PIN(S): IREF, FCDAC (with CHEN = 0)						
V_{IREF}	IREF Voltage Accuracy	0.65		1.5	mV	error from (0.48) VRG
I_{CFC}	CHEN Mode Forced FCDAC Current	40 50		235 75	µA µA	BYPMODE=1, Internal I_{REF} BYPMODE=0, R_F = 40KΩ
PIN(S): FSTAGC						
I_{FSTAGC}	Source Current	3			mA	$V_{FSTAGC} \leq V_{RST}$
V_{RST}	Fast AGC Threshold Voltage			.8V_{DD}	V	BYPMODE=1
I_{OZ}	Tri-state Output Leakage			±100	nA	$V_{OUT}=V_{SS}$ to V_{DD}, DACEN=0

† LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$I_R \text{ (code)} = LSB_R^* \text{ (code+8)} + I_{OFFSET} = LSB_R^* \text{ code} + I_{INITIAL} + I_{OFFSET}$$

The theoretical equation is given by:

$$I_T \text{ (code)} = LSB_T^* \text{ (code+8)} + 0 = (I_{REF}/12)^* \text{(code+8)} + 0.$$

The offset, I_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, I_R (code = -8).

TABLE 9-8. FREQUENCY CONTROL DAC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): VRG, LEVEL, HCDAC w/$\overline{HCTL}$ = 0 and CHEN = 1 (See "Boost Control DAC Specifications" when $\overline{HCTL}$ = 1)						
V_{RG}	External Voltage Reference	2.2		2.45	V	$I_{IN} \leq$ 2 mA maximum sink
$V_{INITIAL}$†	Measured Code Zero Voltage	[V_{DD}-(30/31)*V_{RG}] ±0.04			V	
LSB_T†	Theoretical Resolution (5-bit)		V_{DIF}/31		V	$V_{DIF}=V_{LEVEL} - V_{INITIAL}$ $0.5V \leq V_{DIF} \leq 1.0V$
GAIN†	Gain (LSB) Accuracy			±0.4	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
INL†	Integral Non-Linearity			±0.5	LSB_R	
DNL†	Differential Non-Linearity			±0.5	LSB_R	
PSRR*	Power Supply Rejection Ratio	35	40		dB	
t_S*	Setting Time from SGATE Transitions			2	µs	to 90% of final value with 10pF external load
PIN(S): HCDAC (w/$\overline{HCTL}$=0 or 1 and CHEN=0)						
V_{CHC}	CHEN Mode Forced HCDAC Voltage		CV_{DD}		V	

† LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$V_R(code) = LSB_R * code + V0.$$

The theoretical equation is given by:

$$V_T(code) = LSB_T * code + V_{INITIAL} = (V_{LEVEL} - V_{INITIAL}) * (code/31) + V_{INITIAL}.$$

TABLE 9-9. HYSTERESIS CONTROL DAC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): VRG, BCDAC (with CHEN = 1)						
V_{RG}	External Voltage Reference	2.2		2.45	V	$I_{IN} \leq 2$ mA maximum sink
V_{OFFSET}†	Offset Voltage		±15	±30	mV	Extrapolated Regression Code 0
$V_{INITIAL}$†	Code Zero/One Voltage		0	+20	mV	for codes 0 through 1
LSB_T†	Theoretical Resolution (5-bit)		V_{RG}/31		V	for codes 2 through 31
GAIN†	Gain (LSB) Accuracy		±0.1	±0.4	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
INL†	Integral Non-Linearity			±0.5	LSB_R	for codes 2 through 31
DNL†	Differential Non-Linearity			±0.5	LSB_R	for codes 2 through 31
PSRR*	Power Supply Rejection Ratio	40	45		dB	w/o external filtering
t_S*	Setting Time from SGATE Transitions			2	µs	to 90% of final value with 10pF external load
PIN(S): BCDAC (w/CHEN=0)						
V_{cbc}	CHEN Mode Forced BCDAC Voltage		CV_{SS}		V	

† LSBT is the theoretical resolution. It should not be confused with LSBR which is derived from the regression analysis. The regression equation is given by:

$V_R(code) = LSB_R*code + V_{OFFSET}$ (for codes 2 through 31).

The theoretical equation is given by:

$V_T(code)=LSB_T*code + 0 = (V_{RG}/31)*code + 0$ (for codes 2 through 31).

The offset, V_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, $V_R(code=0)$.

TABLE 9-10. BOOST CONTROL DAC SPECIFICATIONS

9.3 AC ELECTRICAL AND TIMING CHARACTERISTICS

The following specifications are over T_A = 0°C to 70°C, T_J = 0°C to 90°C, V_{SS} = 0V, V_{DD} = +5V ± 250mv (max of 50mV p-p ripple), V_{OH} = 2.0V, V_{OL} = 0.8V, V_{IL} = 0.4V, V_{IH} = 2.4V, and $f_{XTL} \leq 40$ MHz unless otherwise specified. When indicated (*), limits represent characterized values and are not tested.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
			PIN(S): XTLI, XTLO			
f_{XTL}	Crystal Input Frequency			16 20 40	MHz MHz MHz	Active Stage, $\overline{HFCEN}$-1 Ext., $\overline{HFCEN}$=1, 40/60% D_{CYC} Ext., $\overline{HFCEN}$=0, 40/60% D_{CYC}
t_{XS}*	Crystal Start-up Time Following Reset		1	3	ms	
C_{IN}	Crystal External Input Capacitance		100 68 33		pF pF pF	$f_{XTL} \leq 5$ MHz 5 MHz $\leq f_{XTL} \leq$ 10 MHz 10 MHz $\leq f_{XTL} \leq$ 16 MHz
C_{OUT}	Crystal External Output Capacitance		68 47 22		pF pF pF	$f_{XTL} \leq 5$ MHz 5 MHz $\leq f_{XTL} \leq$ 10 MHz 10 MHz $\leq f_{XTL} \leq$ 16 MHz

TABLE 9-11. CRYSTAL OSCILLATOR TIMING SPECIFICATIONS

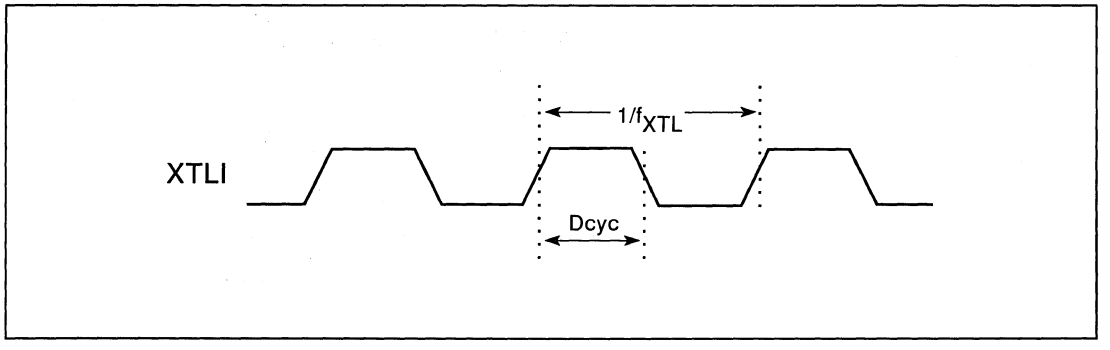

FIGURE 9-1. CRYSTAL INPUT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$						
t_{SWC}	Setup of ENCEN and WDATA to WCLK Rising	5			ns	
t_{HWC}	Hold of ENCEN and WDATA from WCLK Rising	5			ns	
f_{NRZ}	WCLK Frequency ($1/T_{NRZ}$)	7.5		33	MHz	40/60% Duty Cycle
t_{ENCON1}	ENCEN Rising to Encode On	t_{SWC}		t_{SWC} +1	T_{NRZ}	
t_{ENCOFF}	ENCEN Falling to $\overline{\text{WPCDATA}}$ Off	t_{SWC}		tSWC +2	T_{NRZ}	
t_{ENC}	WDATA to $\overline{\text{WPCDATA}}$ Encode Delay	10		16	T_{NRZ}	w/o RLL and w/max. precomp.

TABLE 9-12. ENCODER TIMING SPECIFICATIONS

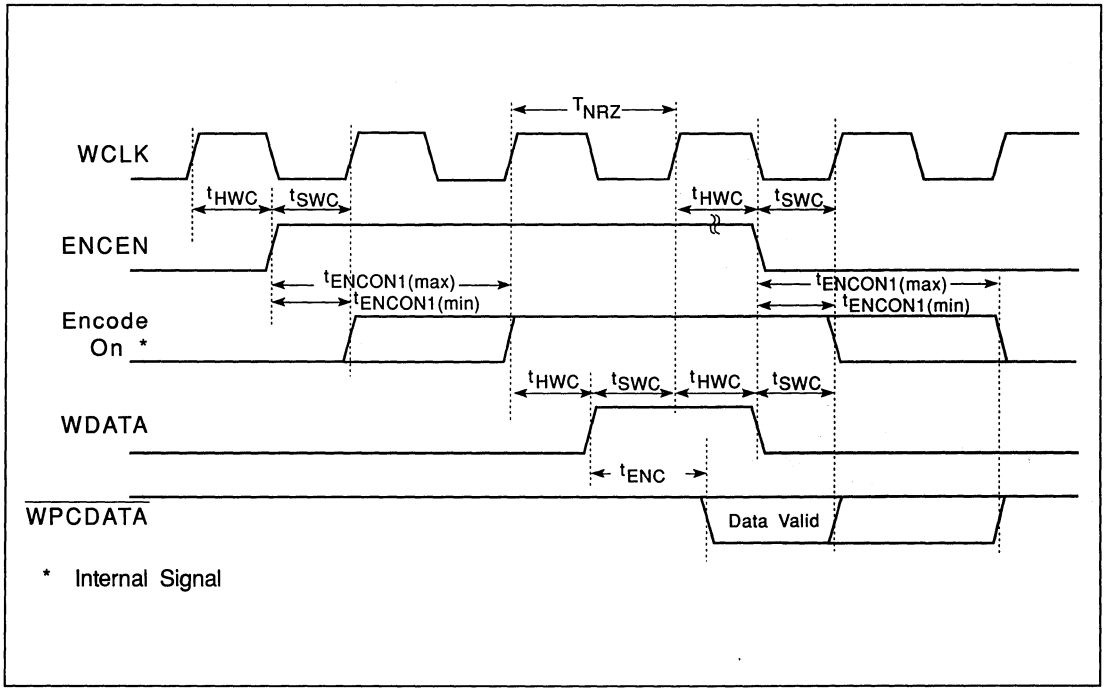

FIGURE 9-2. ENCODER TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$						
t_{SWC}	Setup of AME to WCLK Rising	5			ns	
t_{HWC}	Hold of AME from WCLK Rising	5			ns	
t_{AME}	AME Pulse Width	1			T_{NRZ}	
t_{ENCON2}	AME Rising to Encode On			36	T_{NRZ}	
t_{DAM}	AME to AM on $\overline{\text{WPCDATA}}$ Delay	10		13	T_{NRZ}	w/o RLL and w/max. precomp.
t_{AM}	Address Mark Length			34	T_{NRZ}	(e.g., 51 TRLL)
t_{SAMG}	Setup of AME to End of Gap on WDATA	0			ns	
t_{GAPL}	GAP Loss (due to superposition of AM)	t_{SAMG}-(t_{ENCON2}-t_{AM})			T_{NRZ}	positive or zero means no loss
t_{PLOL}	PLO Loss (due to superposition of AM)	t_{ENCON2}-t_{SAMG}			T_{NRZ}	positive or zero means no loss

TABLE 9-13. ADDRESS MARK GENERATION TIMING SPECIFICATIONS

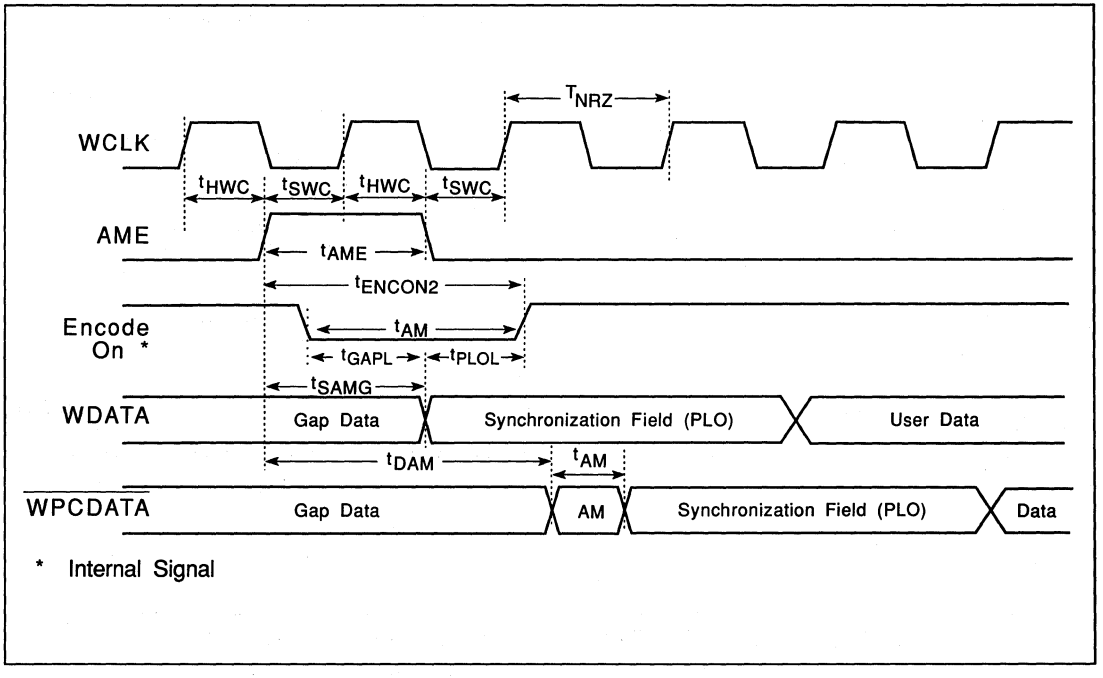

FIGURE 9-3. ADDRESS MARK GENERATION TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
			PIN(S): $\overline{\text{WPCDATA}}$			
LSB_T†	Resolution		T_{RLL} /64			for codes 0 to 15
INL	Integral Non-Linearity			±0.5	LSB_R	
DNL	Differential Non-Linearity			±0.5	LSB_R	
GAIN	Gain Accuracy			±3	$\%LSB_T$	$100*(LSB_R-LSB_T)/LSB_T$
t_{WPC}	$\overline{\text{WPCDATA}}$ Pulse Width	11/16		17/16+x	T_{RLL}	x is 10ns max. and ind. of T_{RLL}
t_{WTJ}*	$\overline{\text{WPCDATA}}$ Timing Jitter		±200 ±200		ps ps	one σ, lab supply one σ , w/filtered‡ 50mv p-p power supply ripple
t_{RL}*	Ramp Lock Loop Lock-Up Time		1.5	3	ms	from assertion of RLLEN

† LSB_T is the theoretical resolution. It should not be confused with the LSB_R which is derived from the regression analysis.

‡ See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-14. WRITE PRECOMPENSATION TIMING SPECIFICATIONS

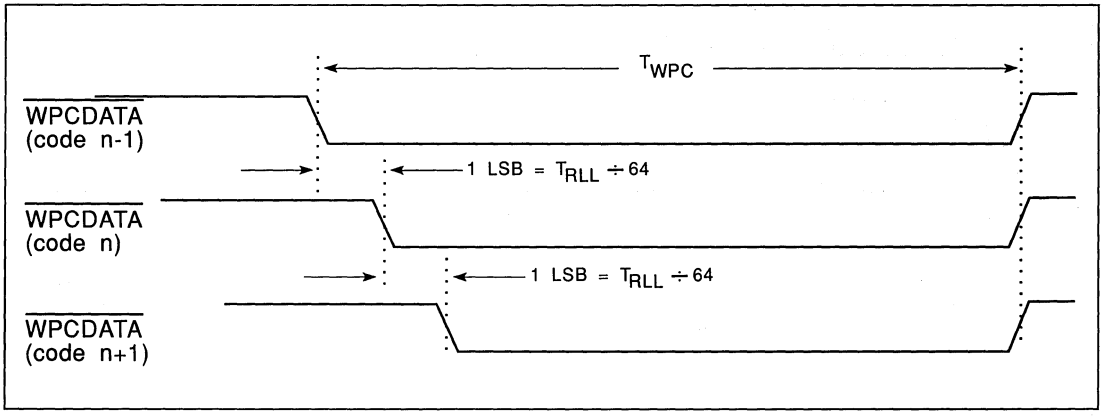

FIGURE 9-4. WRITE PRECOMPENSATION TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, $\overline{\text{AMD}}$, $\overline{\text{RAWDATA}}$, RDATA, RCLK						
t_{AMD}	End of AM to $\overline{\text{AMD}}$ Valid	1		3	T_{RLL}	
t_{RG}	$\overline{\text{AMD}}$ Valid to RGATE Valid			1	Byte	
t_{LG}	End of AM† to End of Velocity Lock	60		96	T_{RLL}	user programmable 5-8 Bytes
t_{DET}	End of AM† to Start of Data Detection	t_{LG}-3		t_{LG}	T_{RLL}	
t_{DECON}	End of AM† to Decode On			t_{DET}+10	T_{RLL}	
t_{DEC}	$\overline{\text{RAWDATA}}$ to RDATA Decode Delay	1		1.25	Bytes	
t_{RAW}	$\overline{\text{RAWDATA}}$ pulse width high/low	10			ns	
t_{RDT}	Minimum $\overline{\text{RAWDATA}}$ period	1.5			T_{RLL}	w/o internal drop out
t_{RDC}	Centering of RDATA rising to RCLK rising	-5		+5	ns	from center (T_{NRZ}/2) measured during closed loop
t_{RCD}	RCLK Duty Cycle (during Read & Write)	45		55	$\%T_{NRZ}$	measured during closed loop at 0.8V and 2.0V crossings

† Specified from RGATE rising for hard sector operations.

TABLE 9-15. READ TIMING SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{RAWDATA}}$, RDATA, RCLK, DELRD, WINCLK						
t_{DWL}	Data Detection Window Loss			250	ps	open loop fixed losses
t_{DWC}	Data Detection Window Centering Error			± 1	$\%T_{RLL}$	
t_{PWC}	Phase Detection Window Centering Error			± 2	$\%T_{RLL}$	
t_{WM}	Window Monitoring Error			± 250	ps	Matching of DELRD/WINCLK to internal Data Det. Window

TABLE 9-16. PHASE & DATA DETECTION WINDOW TIMING SPECS

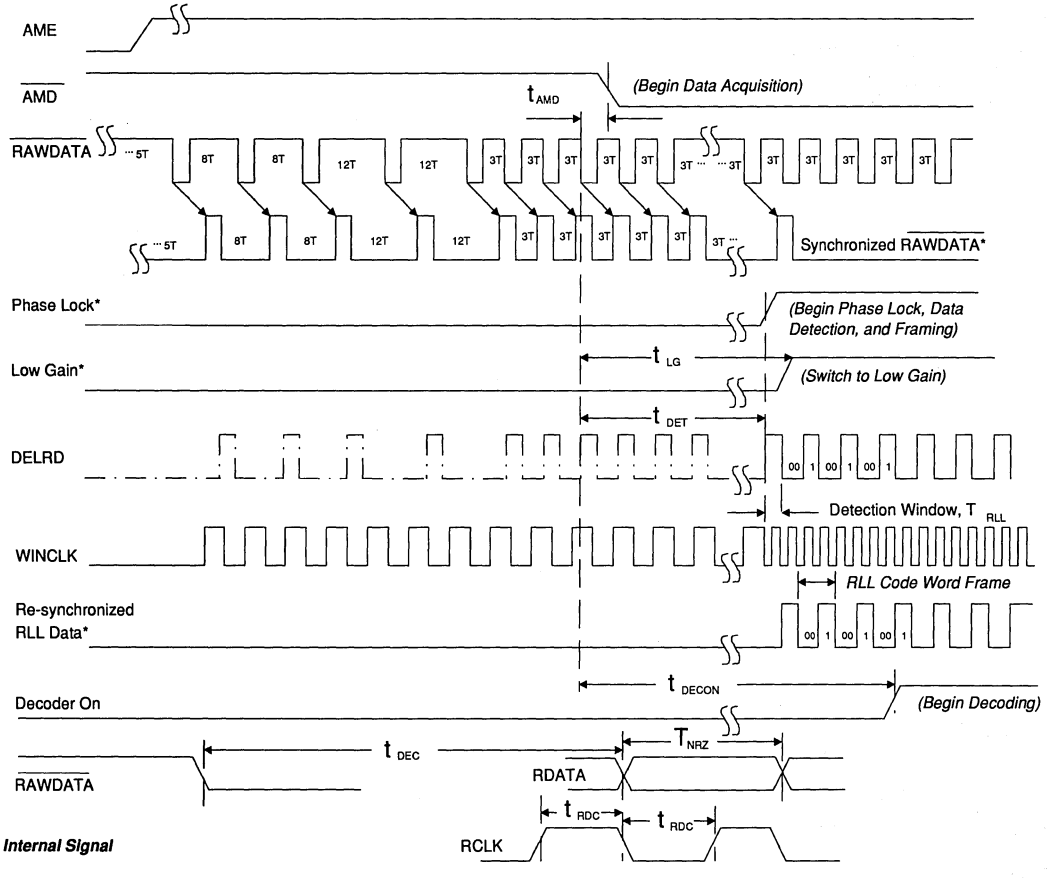

FIGURE 9-5. READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{RAWDATA}}$, RDATA, RCLK						
t_{PWS}	Percentage Window Shift Accuracy			±2	$\%T_{RLL}$	
LSB_T	Theoretical Resolution	2	δ_{wss}	6	ns	See EQ. 16.0
GAIN†	Gain (LSB) Accuracy			±TBD	$\%LSB_T$	$100*(LSB_R-LSB_T)/LSB_T$
INL†	SAM Integral Non-Linearity (Δ_{wss})		±250	±500	ps	See EQ. 18.0
DNL†	SAM Differential Non-Linearity (Δ_{wss})		±250	±500	ps	See EQ. 18.0
t_{OFFSET}†	SAM Code Zero Offset			±TBD	ns	Extrapolated Regression Code 0
t_{WL}*	WSS Lock-Up Time			3	ms	From assertion of WSSEN

† Specifications are for the full range of LSB_T, LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$\Delta_{WSSR}(code)=LSB_R*(code+1)+t_{OFFSET}.$$

The theoretical equation is given by:

$$\Delta_{WSST}(code)=LSB_T*(code+1)+0=\delta_{WSS}*(code+1)+0.$$

The offset, t_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, $\Delta_{WSSR}(code=-1)$.

TABLE 9-17. WINDOW SHIFT TIMING SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): FSPMP						
t_{FTJ}*	Frequency Synthesizer Timing Jitter		±50 ±100		ps ps	one σ, lab supply one σ , w/filtered‡ 50mv p-p power supply ripple at 1-2KHz
t_{FSL}*	Frequency Synthesizer Lock-up Time		1.5	3	ms	Following COD/VCOD load

† See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-18. FREQUENCY SYNCHRONIZER PLL AC SPECIFICATIONS

SYM.	CHARAC-TERISTIC	SLOW	NOMINAL	FAST	UNITS	CONDITIONS
PIN(S): DSPMP, LPF, VCON (Specified for Phase Lock. V_{DD}=5V)						
K_{D0}†	Phase Detector Gain, BAND0	$1/2\pi(52f_{dr}-129)$	$1/2\pi(29f_{dr}-17)$	$1/2\pi(26f_{dr}-28)$	µA/rad	
K_{D1}†	Phase Detector Gain, BAND1	$1/2\pi(28f_{dr}-54)$	$1/2\pi(23f_{dr}-18)$	$1/2\pi(21f_{dr}-33)$	µA/rad	
K_{D2}†	Phase Detector Gain, BAND2	$1/2\pi(38f_{dr}-182)$	$1/2\pi(27f_{dr}-109)$	$1/2\pi(18f_{dr}-24)$	µA/rad	
K_{D3}†	Phase Detector Gain, BAND3	$1/2\pi(31f_{dr}-131)$ $1/2\pi(208f_{dr}-4800)$	$1/2\pi(17f_{dr}-3)$ $1/2\pi(23.2f_{dr}-117)$	$1/2\pi(15f_{dr}-33)$ $1/2\pi(14.3f_{dr}-1)$	µA/rad µA/rad	$19.1\le f_{dr}\le 27$ MHz $27.0\le f_{dr}\le 33$ MHz
K_{O0}†	VCO Gain, BAND0	$-17f_{dr}+218$	$-12f_{dr}+308$	$-23f_{dr}+469$	%/V	
K_{O1}†	VCO Gain, BAND1	$-13f_{dr}+254$	$-13f_{dr}+363$	$-8f_{dr}+356$	%/V	
K_{O2}†	VCO Gain, BAND2	$-11f_{dr}+251$	$-8f_{dr}+331$	$-14f_{dr}+513$	%/V	
K_{O3}†	VCO Gain, BAND3	$-6f_{dr}+177$	$-7f_{dr}+362$	$-9f_{dr}+510$	%/V	$19.1\le f_{dr}\le 27$ MHz $27.0\le f_{dr}\le 33$ MHz
K_{V3}†	Open Loop Gain Limit, BAND3	$1/2\pi(60000)$	$1/2\pi(76000)$	$1/2\pi(92000)$	%µA/V	f_{dr}=33 MHz
R_{KDG}	Acquisition to Tracking Gain Ratio	1.9	2.0	2.1		$K_{D(ACQ)}$:$K_{D(TRACK)}$
R_{KDS}	Up to Down Symmetry Ratio	0.95	1.0	1.05		$K_{D(UP)}$:$K_{D(DOWN)}$
t_{DTJ}*	Data Synchronizer Timing Jitter		±0.25 ±0.25		%T_{DR} %T_{DR}	one σ, lab supply, 3T data (001) one σ, w/filtered‡ 50mv p-p power supply ripple at open loop unity gain, 3T data (001)

† K_D varies with frequency, inversely as K_O, to linearize loop gain product (K_V=K_D*K_O). K_D and K_O are specified as linearized gains, using the measured VCON voltages found at the frequency extremes of each of the frequency bands. Slow and fast values represent variations in the linear approximation due to process, temperature, and voltage variations. The open loop gain product K_V should be calculated within a given speed corner. Note that K_D doubles during high gain acquisition.
‡ See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-19. DATA SYNCHRONIZER PLL AC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): ALE, $\overline{MCS}$ (Chip Select), $\overline{MRE}$ (Read), $\overline{MWE}$ (Write), AD7-0 (Address/Data)						
t_{ALw}	ALE pulse width high	15			ns	
t_{AsALl}	Address setup to ALE low	10			ns	
$t_{AhldALl}$	Address hold after ALE low	5			ns	
t_{AzRDl}	Read low to Address tri-state			15	ns	
t_{RDw}	Read pulse width	110			ns	
t_{RDhALh}	Read high to next ALE high	15			ns	
t_{RDax}	Read (data) access time	18		90	ns	C_L = 30pF to 100pF
t_{DzRDh}	Data tri-state after Read high	5		30	ns	@ V_{OH}-0.5V & V_{OL}+ 0.5V
t_{AvWRl}	Address valid to Write low	25			ns	
t_{WRw}	Write pulse width	70			ns	
t_{WRhALh}	Write high to next ALE high	10			ns	
t_{DsWRh}	Data setup to Write high	50			ns	
$t_{DhldWRh}$	Data hold after Write high	5			ns	
T_{CSlRWl}	Chip Select low to Read/Write low	10			ns	
T_{RWhCSh}	Read/Write high to Chip Select high	5			ns	
t_{LPSRD}	Setup of Low Power Mode Deactivation to Register Reads (i.e. settling time of output driver bias from RSTPDN off)	100			µs	Does not effect register writes
t_{BCS}	$\overline{MCS}$ to $\overline{BCS}$ Propagation Delay			19	ns	
t_{RST}	$\overline{HRESET}$ Minimum Pulse Width Low			20	ns	

TABLE 9-20. MICROPROCESSOR INTERFACE TIMING SPECIFCATIONS

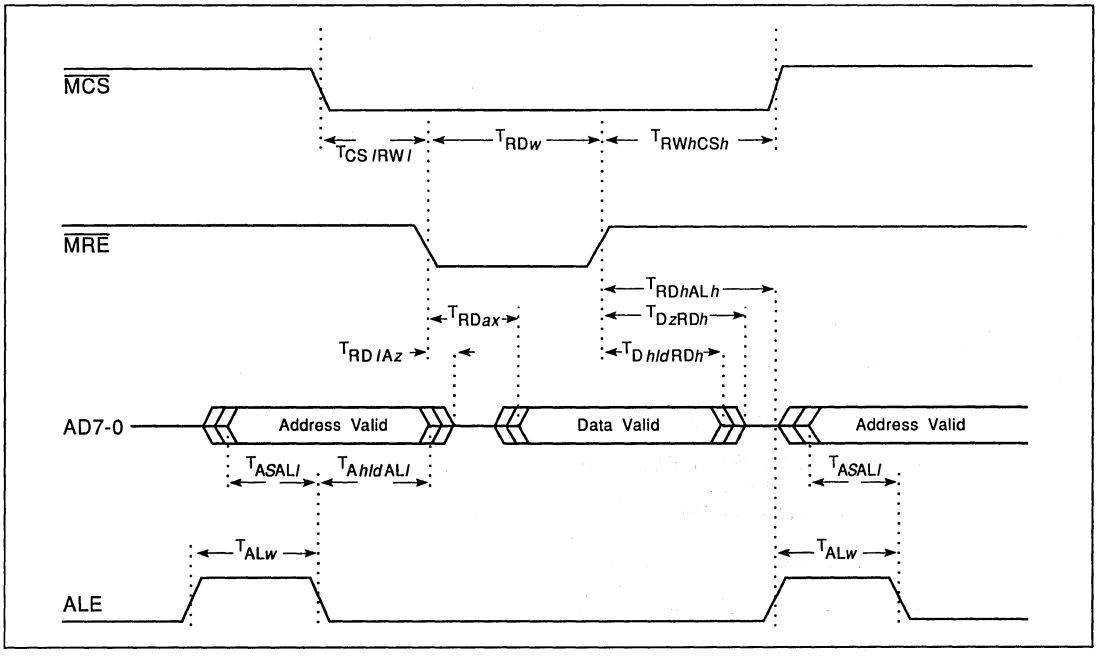

FIGURE 9-6. MICROPROCESSOR READ TIMING DIAGRAM

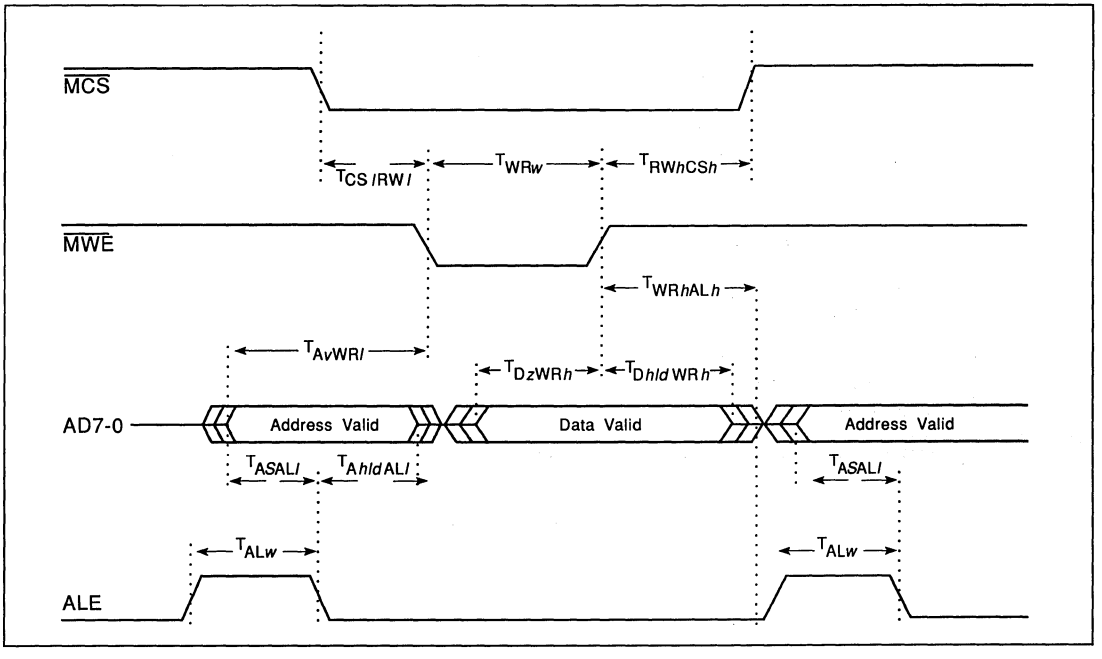

FIGURE 9-7. MICROPROCESSOR WRITE TIMING DIAGRAM

APPENDIX

A.0 APPLICATION NOTES

A.1 FREQUENCY SYNTHESIZER

As discussed in section 3.0, "Frequency Synthesizer", the Frequency Synthesizer utilizes one divider to divide the crystal reference (COD) and one for the VCO (VCOD). This leads to some confusion as to the resolution which can be expected in generating the NRZ data rate.

As can be seen from EQ. 6.0, the output of the Synthesizer is simply a ratio of the crystal input frequency pre-scaled by the HFCOD. That is, for any given crystal frequency, there is a set of ratios which may be generated by programming the value of the VCOD and COD registers. The resulting VCOD/COD ratios will be contained by the input frequency limits to the PLL, and the maximum and minimum data rates allowable (EQ. 3.0 and EQ. 5.0). Disregarding these constraints for the time being, the ratios have certain characteristics which are of interest and which greatly effect the resolution of the system.

Take, for example, the ratios generated by x/y where x and y range from 1 to 10. Let's further bound these ratios by zero and one. If we create an axis on which to plot the ratios, we can begin to see an interesting phenomenon. Starting with the ratio 1/2, place a mark at this point on the axis.We have reduced the distance between the marks at zero and one by a factor or two. If we take the next ratio, 1/3 and 2/3, we further reduce the distance from zero and one to the next nearest mark, down to 1/3. As this process continues, we see that the distance from zero and one to the next nearest mark will be equal to the smallest ratio we generate. In this case it will be 1/10. There is a mark at 9/10 and a mark at 1/10, both of which are 1/10 away from their respective neighboring integer ratios, one and zero. In the mean time, the intervals created between one and zero have been reduced to much less than 1/10. For example, the distance between 1/10 and 1/9 is 1/90. This phenomena repeats at all integer ratios. In fact, it can be show that the resolution similarly degrades around multiples of 1/2, but to a much lesser degree. This process continues, with the resolution around multiples of 1/3 being better an 1/2, but worse than 1/4, etc.

Following this same pattern, the Frequency Synthesizer will have resolutions which are coarser at and around integer ratios of the VCOD/COD, and it can be said that the worst possible resolution will be equal to 1/COD, in the same fashion as the worst resolution in the illustration given above was 1/10. However, in general, the resolution will be much better, as was also illustrated with the example of 1/90 above.

Another way of visualizing the resolution question is as follows. Since the COD serves to divide the crystal input frequency down to the range of 95 to 105 KHz, the VCO can only be generated as a multiple of this (i.e. EQ. 6.0). It is therefore easily seen that the best resolution will occur when the PLL is operated at 95 KHz. However, in order to reach the higher data rates, the PLL will ultimately have to be operated at up to 105 KHz. The actual NRZ output of the synthesizer will therefore have a resolution which is never worse than, and almost always much better than 105kHz times 4/3, or 140 KHz.

The C program on the following page is provided to assist in programming the Synthesizer. The program requires as its input, the desired crystal frequency. The output will be the exhaustive set of all possible data rates along with the necessary COD and VCOD values. Taking the output of this program and sorting based on the first column (NRZ data rate) produces a convenient look up table of data rates for the given crystal frequency.

```
#include <stdio.h, math.h. string.h>
main(argc, argv)
int argc;
char *argv[ ];
{
        float fxtli = 0.0;
        float fxtlicod      = 0.0;
        float fvco          = 0.0;
        float fnrz          = 0.0;
        float cod           = 1.0;
        float vcod          = 1.0;
        char *fxtliptr;
        fxtliptr = argv[1];
        fxtli = (float) atof(fxtliptr);
        printf("fxtli =%02f MHz \n", (fxtli/1e6));
        while (cod <= 256.0)
        {
                fxtlicod = fxtli/cod/1e3;
                if ((fxtlicod <= 105) && (fxtlicod >= 95))
                {
                        while (vcod  <= 256.0)
                        {
                                fnrz = 4.0*fxtlicod*vcod/3e3;
                                if ((fnrz  <= 33.0) && (fnrz >= 7.5))
                                printf("%02f MHz: cod =%02f vcod =
                                        %02f fpll =%02f kHz \n",
                                        fnrz, (cod-1), (vcod-1), fxtlicod);
                                 vcod = vcod + 1.0;
                        }
                        vcod = 1.0;
                }
                cod = cod + 1.0;
        }
}
```

A.2 WINDOW SHIFT SYNTHESIZER

For discussion of the resolution, refer to "A-1 Frequency Synthesizer". The following C program is provided to assist in programming the Synthesizer. The program requires as its input the expected data rate. The output will be the exhaustive set of all possible data rates along with the necessary COD and VCOD values. Taking the output of this program and sorting based on the first column (NRZ data rate) produces a convenient look up table of data rates for the given crystal frequency.

```
#include <stdio.h, math.h, string.h
main(argc, argv)
int argc;
char *argv[];
{
        float delay = 0;
        int wsi = 0;
        float fdr = 0.0;
        float fclk = 0.0;
        float tclk = 0.0;
        float ftclkcod = 0.0;
        float fvco = 0.0;
        float fvcovcod = 0.0;
        float SAM = 1.0;
        float range = 0.0;
        float cod = 1.0;
        float vcod = 1.0;
        float ws = 0.0;
        float wsf = 0.0;
        float delta = 0.0;
        char *fdrptr;
        fdrptr = argv[1];
        fdr = (float) atof(fdrptr);
        ftclk = 1.5*fdr;
        tclk = 1e9/ftclk;
        printf("Data Rate =%02f MHz\n", (fdr/1e6));
        while (cod ≤16.0)
        {
                ftclkcod = (ftclk/cod)/1e6;
                if ((ftclkcod <= 15) && (ftclkcod >= 3))
                {
                        while (vcod <= 32)
                        {
```

```
                                        fvco = ftclkcod*vcod;
                                        delta = (1000.0/fvco)/9.0;
                                        if ((delta <= 6) && (delta >= 2))
                                        {
                                                while (SAM ≤16)
                                                {
                                                        delay = (SAM*delta);
                                                        wsi = (int) (delay/tclk);
                                                        wsf = (float) wsi;
                                                        ws = 100*((((tclk/2) * ((2*wsf) + 1))-delay)/tclk)
                                                        printf("%02f percent (delay =%02f ns):
                                                           cod =%02f vcod =%02f
                                                           SAM =  %02f/n".ws, delay,(cod-1).
                                                           (vcod-1), ( SAM-1)):
                                                SAM=SAM+1.0;
                                                }
                                                SAM=1.0;
                                        }
                                        vcod=vcod+1.0;
                                }
                                vcod=1.0;
                        }
                        cod=cod+1.0;
                }
        }
```

WD33C92A

Enhanced SCSI Bus

Interface Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

The 33C92A is a MOS/VLSI device which is implemented in Western Digital's CMOS process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 48-pin dual-in-line package. All inputs and outputs are TTL-compatible.

1.1 FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers.
- Synchronous offset selectable from 1 to 12 bytes, with selectable transfer period up to 5 Mbytes/s. ANSI spec compatibility guaranteed to 4 Mbytes/s.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Can be used as host adapter (SCSI Initiator) or peripheral adapter (SCSI Target).
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Burst data transfers up to 4096 bytes.
- Programmable timeout for selection and reselection.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Special "Translate Address" command performs the Logical-to-Physical address translation.
- Single +5V supply.
- Available in 44-pin chip carrier or 48-pin DIP.
- Low-power CMOS design.
- Compatible with single-ended or differential external drivers.

2.0 DESCRIPTION

The 33C92A is intended for use in systems which interface to the SCSI (Small Computer System Interface) Bus. The 33C92A can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C92A interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor must issue a command to the 33C92A to select the desired Target. The 33C92A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying, notifying the host when it has succeeded by generating an interrupt. At this point, the 33C92A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C92A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C92A. The 33C92A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C92A also offers high-level Select-and-Transfer commands, eliminating the interrupt handling otherwise required between each SCSI bus phase.

When the 33C92A is used in a peripheral system, it interfaces with a local processor and the SCSI bus just as it does when used as a host adapter. In this environment, the 33C92A will operate primarily in a Target role. The Target-role command set enables the 33C92A to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C92A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

3.0 33C92A PINOUT

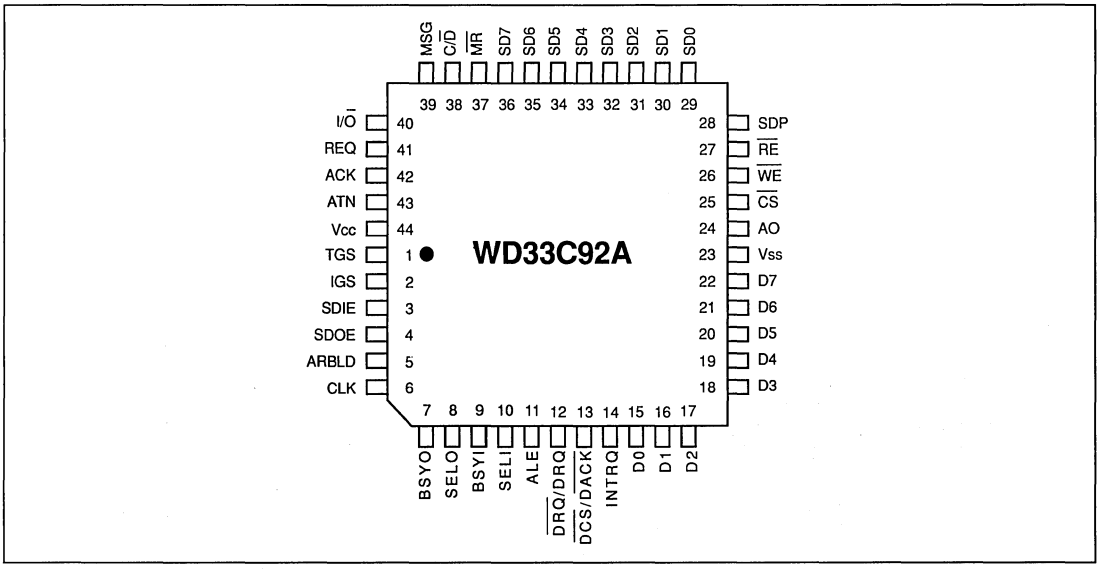

FIGURE 3-1. 44-PIN QUAD PIN DIAGRAM

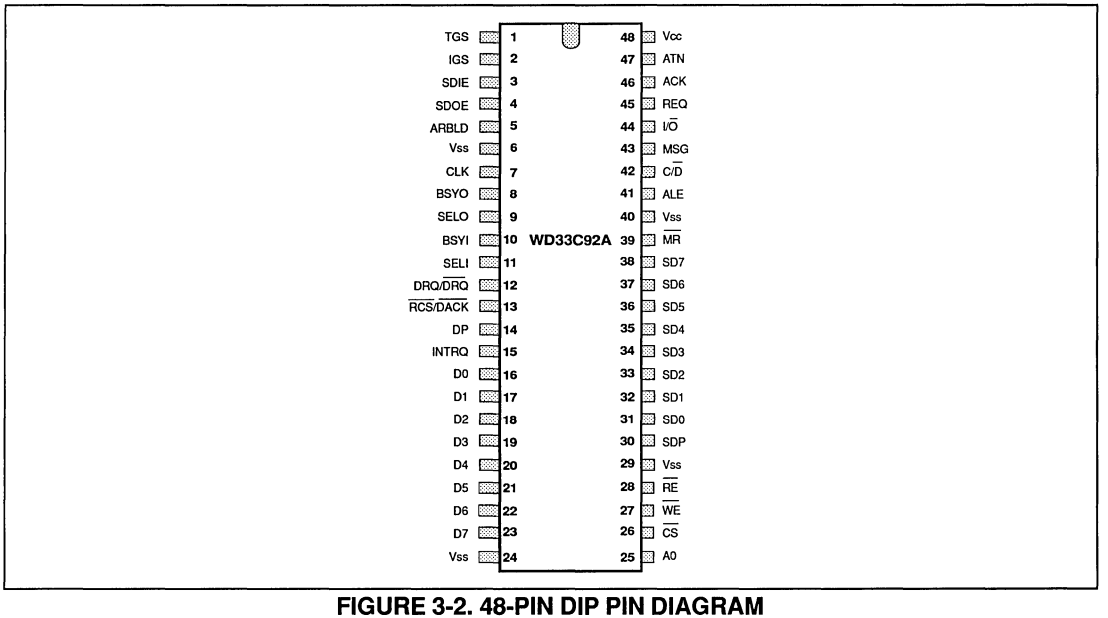

FIGURE 3-2. 48-PIN DIP PIN DIAGRAM

4.0 SIGNAL DESCRIPTIONS

PIN	MNEMONIC	I/O	DESCRIPTION
6	CLK	I	8-20 MHz square wave clock.
37	MR-	I	Reset is an active-low input which forces the 33C92A into an idle state. All SCSI outputs are tristated.
14	INTRQ	O	Interrupt Request to external microprocessor. Indicates command completion/termination or a need to service the SCSI interface. This bit is reset when the SCSI STATUS register is read.
27	RE-	I/O	Read enable is an active-low input which is used with CS- to read a register. In WD Bus mode, it is used as an output to read data from a sector buffer. Also used for DMA transfers. (TRI-STATE)
26	WE-	I/O	Write enable is an active-low input which is used with CS- to write a register. In WD Bus mode, it is used as an output to write data to a sector buffer. Also used for DMA transfers. (TRI-STATE)
25	CS-	I	Chip Select is an active-low input which qualifies RE- and WE- when accessing a register. This signal must be inactive during a DMA cycle (DACK- active in DMA/burst mode or DRQ active in WD Bus mode).
24	A0	I	Address pin used to access the internal registers for non-multiplexed address/data busses (i.e. the ALE pin is grounded). The address of the desired register is loaded into the ADDRESS register during a write cycle with A0=0. The selected register is then accessed when A0=1.
11	ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C92A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
13	DACK- (RCS-)	I/O	DMA acknowledge input used for interfacing to an external DMA controller (e.g. 8237). When DACK- is low, all bus transfers are to/from the DATA register regardless of the contents of the ADDRESS register. In WD Bus mode, this pin functions as a RAM chip select output to allow the 33C92A to access a sector buffer. RE- and WE- are outputs when RCS- is active. Since this pin can be an open drain output, a pullup resistor may be required when operating in WD Bus mode.

TABLE 4-1. PROCESSOR/DMA INTERFACE

NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

PIN	MNEMONIC	I/O	DESCRIPTION
12	DRQ-	I/O	Data request is an output when interfacing to (DRQ) an external DMA controller and an input when in WD Bus mode. When used with an external DMA controller, DRQ- and DACK- form the handshake for the data-byte transfers. In Burst mode, DRQ- remains low as long as there is data to transfer. In WD Bus mode, the 33C92A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, RCS- is false, and the RE- and WE- outputs are disabled. Since this pin can be an open drain output, a pullup resistor may be required when operating in DMA or Burst mode.
15-22	D7-D0	I/O	Processor data bus.
28	DP	I/O	Data Parity, used only for checking/generating parity during data transfers.

TABLE 4-1. PROCESSOR/DMA INTERFACE (CONTINUED)

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NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

PIN	MNEMONIC	I/O	DESCRIPTION
43	ATN	I/O	ATN is an output in the initiator role and an input in the target role. It is used to indicate the ATTENTION condition.
41	REQ	I/O	REQ is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ACK data transfer.
42	ACK	I//O	ACK is an output in the initiator role and an input in the target role. It indicates an acknowledgement for a REQ/ACK data transfer handshake.
39	MSG	I/O	MSG is an input in the initiator role and an output in the target role. It is asserted during a MESSAGE phase.
38	C/D-	I/O	C/D- is an input in the initiator role and an output in the target role. It is used to indicate whether CONTROL or DATA information is on the SCSI data bus.
40	I/O-	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
29-36	SD7 | SD0	I/O	SCSI data bus.
28	SDP	I/O	SCSI data bus parity signal.
9	BSYI	I	BSYI signals the 33C92A that SCSI BSY- is asserted.
7	BSYO	O	The 33C92A asserts BSYO to assert the SCSI BSY- signal.
10	SELI	I	SELI signals the 33C92A that SCSI SEL- is asserted.
8	SELO	O	The 33C92A asserts SELO to assert the SCSI SEL-signal.
3	SDIE	O	Enables SCSI data bus receivers.
4	SDOE	O	Enables SCSI data bus drivers.
5	ARBLD	O	Latches the decoded port number into an external register just prior to the SCSI bus arbitration process.
2	IGS	O	The 33C92A asserts IGS when operating as an Initiator. IGS enables the SCSI drivers for ATN and ACK.
1	TGS	O	The 33C92A asserts TGS when operating as a Target.TGS enables the SCSI drivers for REQ, MSG, C/D- and I/O-.

TABLE 4-2. SCSI INTERFACE

NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

5.0 33C92A BLOCK DIAGRAM

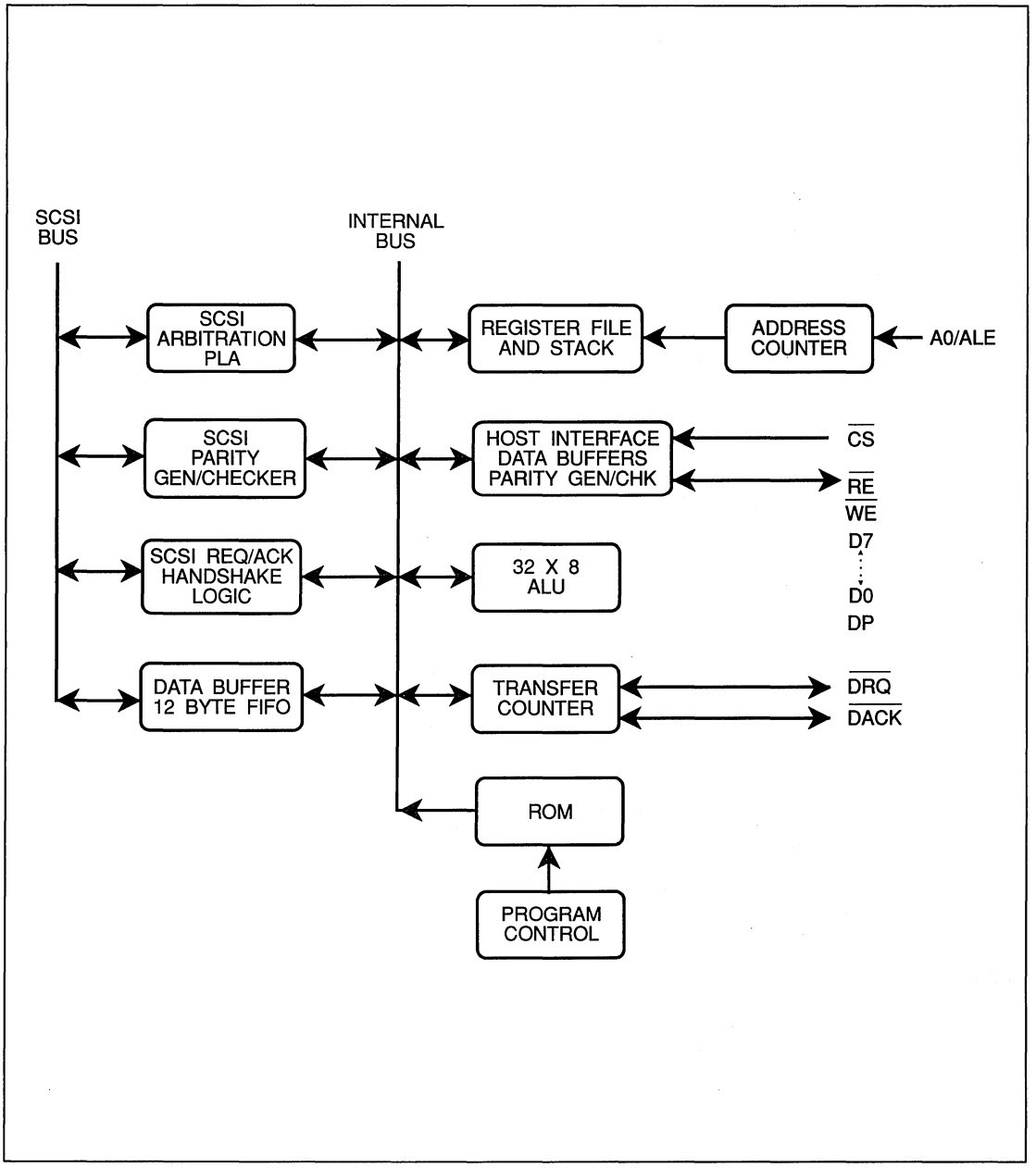

FIGURE 5-1. 33C92A BLOCK DIAGRAM

6.0 33C92A REGISTERS

6.1 REGISTER MAP

A0	R/W	REGISTER ACCESSED	ADDRESS (HEX)
0	R	AUXILIARY STATUS REGISTER	XX
0	W	ADDRESS REGISTER	XX
1	R/W	OWN ID REGISTER /CDB SIZE 00	00
1	R/W	CONTROL REGISTER	01
1	R/W	TIMEOUT PERIOD REGISTER	02
1	R/W	TOTAL SECTORS REGISTER /CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER /CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER(MSB)/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER(LSB)/CDB 4TH	06
1	R/W	LOGICAL ADDRESS(MSB) /CDB 5TH	07
1	R/W	LOGICAL ADDRESS(2ND) /CDB 6TH	08
1	R/W	LOGICAL ADDRESS(3RD) /CDB 7TH	09
1	R/W	LOGICAL ADDRESS(LSB) /CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER /CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER /CDB 10TH	0C
1	R/W	CYLINDER NUMBER(MSB) REGISTER/CDB 11TH	0D
1	R/W	CYLINDER NUMBER(LSB) REGISTER/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER	0F
1	R/W	COMMAND PHASE REGISTER	10
1	R/W	SYNCHRONOUS TRANSFER REGISTER	11
1	R/W	TRANSFER COUNT REGISTER (MSB)	12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)	13
1	R/W	TRANSFER COUNT REGISTER (LSB)	14
1	R/W	DESTINATION ID REGISTER	15
1	R/W	SOURCE ID REGISTER	16
1	R	SCSI STATUS REGISTER	17
1	R/W	COMMAND REGISTER	18
1	R/W	DATA REGISTER	19

NOTES:

1. All unused bits of a defined register are reserved and must be zero.

2. Reading an undefined or unavailable register results in an all-ones data bus output.

3. Register addresses are determined by the ADDRESS register bits AR7 through AR0.

4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at hex 1F.

5. See section 6.3 for a description of how reset affects the internal registers.

6.2 REGISTER DESCRIPTIONS

6.2.1 Auxiliary Status Register

The AUXILIARY STATUS register is a read-only register which contains general status information not directly associated with the interrupt condition. The AUXILIARY STATUS register may be accessed at any time, except during DMA accesses (DACK- asserted in DMA/Burst mode or DRQ asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 0 DBR-DATA BUFFER READY

DATA BUFFER READY is used during programmed I/O to indicate to the processor whether or not the DATA register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the 33C92A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.

Bit 1 PE-PARITY ERROR

PARITY ERROR status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus and is checked on data received from the SCSI bus during transfers out to the host bus.

Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTROL register. The PE bit is cleared when a new command is issued.

Bit 2,3 Not Used

Not used bits are zero.

Bit 4 CIP-COMMAND IN PROGRESS

COMMAND IN PROGRESS, when set, indicates that the 33C92A is interpreting the last command entered into the COMMAND register and therefore this register is unavailable. When this bit is reset, a command may be written to the COMMAND register.

Bit 5 BSY-BUSY

BUSY indicates that a Level II command is currently executing and therefore only the COMMAND register (when CIP = 0), the DATA register, and the AUXILIARY STATUS register are accessible by the host. A Level II command may not be written to the COMMAND register when this bit is one.

Bit 6 LCI-LAST COMMAND IGNORED

LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored.

Bit 7 INT-INTERRUPT PENDING

INTERRUPT PENDING indicates that the INTRQ pin is asserted. The host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

6.2.2 Address Register

The ADDRESS register is a write-only register which contains the address of the register to be accessed. Registers in the 33C92A may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The A0 pin should be connected to ground when using this method. The ALE is typically then followed by the CS- and WE- or RE- signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F hex.

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- Indirect addressing (separate address/data busses). In indirect addressing, the register access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the ADDRESS register is loaded by performing a write of the desired address to the 33C92A (WE- and CS- asserted) with A0=0. Then the register is accessed by asserting CS- and WE- or RE-, with A0=1. Also, following every access with A0=1, the ADDRESS register will automatically increment to point at the next register, with the exception of the following locations: AUXILIARY STATUS register, DATA register, and the COMMAND register. In indirect addressing, the AUXILIARY STATUS register is accessed by performing a read (CS- and RE- asserted) with A0=0.

6.2.3 Own ID/CDB Size Register

The OWN ID/CDB SIZE register, in its first mode, contains both the encoded ID of the 33C92A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the divisor for the input clock. In its second mode (when advanced features are enabled, see 7.3), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the 33C92A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and a "Reset" command must then be issued, following a hardware reset to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see 7.3).

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0-2 IDn-SCSI ID Bits 0-2

SCSI ID Bits 0-2 set the SCSI bus ID number that the 33C92A will use during arbitration and selection.

Bit 3 EAF-ENABLE ADVANCED FEATURES

ENABLE ADVANCED FEATURES, when set to one, causes the 33C92A to enable certain advanced features (see section 7.3). When this bit is zero, those features are disabled.

Bit 4 EHP-ENABLE HOST PARITY

ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the AUXILIARY STATUS register will indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 Not Used

Not used bits are zero.

Bit 6-7 FSn-FREQUENCY SELECT 0-1

FREQUENCY SELECT 0-1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
xx	1	1	undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

MAXIMUM SCSI TRANSFER RATE =
INPUT CLOCK FREQUENCY/CLOCK DIVISOR[MByte/sec]

6.2.4 Control Register

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR

The HALT on SCSI PARITY ERROR bit enables the 33C92A to immediately terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the ACK pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.

Bit 1 HA-HALT on ATTENTION

The HALT on ATTENTION bit (in Target mode only) enables the 33C92A to terminate a Send or Receive command if the ATN input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the 33C92A. The ATN input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to bothsynchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT

The INTERMEDIATE DISCONNECT INTERRUPT bit, when set, enables the 33C92A to generate an 85H interrupt and complete a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode Combination commands that serve to reduce host system overhead. Refer to Section 7 for more details.

Bit 3 EDI-ENDING DISCONNECT INTERRUPT

When the ENDING DISCONNECT INTERRUPT bit is set, the 16H interrupt which normally follows the COMMAND COMPLETE message during the execution of a Select-and-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode Combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to Section 7 for more details.

Bit 4 HHP-HALT on HOST PARITY ERROR

The HALT on HOST PARITY ERROR bit enables the 33C92A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the ACK signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.

Bit 5-7 DMx-DMA MODE SELECT

DMA MODE SELECT bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	POLLED MODE, or no DMA enabled. All data phase transfers are performed by polling for DBR in the AUXILIARY STATUS register, and then writing (reading) the data to (from) the DATA register.
0	0	1	BURST MODE selects a demand-mode DMA interface. In this mode, the DRQ- signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and RE-/WE- as long as DRQ- is active.
0	1	0	WD-BUS MODE is selected when the 33C92A is connected to a WD Bus. This mode also can be called Direct Buffer Access (DBA) mode. In this mode, the 33C92A acts as a bus master, and all data access signals reverse their direction: The DRQ- output signal becomes the DRQ input, which enables the 33C92A to drive the buffer bus control signals. The DACK- output signal becomes the RCS- input, which is asserted as a chip select for the buffer. The RE- and WE- inputs become outputs which drive the read and write functions of the RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or the decides to pause the transfer by negating the DRQ signal; one more transfer may occur after this transition, and then the DACK-, RE-, and WE- signals are negated.
1	0	0	DMA MODE is selected when the 33C92A is to be used with a DMA controller in single-byte transfer mode. In this mode, DRQ- is asserted and then negated, and the DMA controller responds by asserting DACK- and WE- or RE-, for each data byte transferred to/from the 33C92A.

TABLE 6-1. DMA MODE SELECTED

6.2.5 Timeout Period Register

The TIMEOUT PERIOD register is an 8-bit register containinga preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

register value = Tper * Ficlk/80

Where:

Tper = the desired timeout period in milliseconds

Ficlk = the input clock frequency at the MCK pin in Megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the 33C92A will wait for a response (indicated by assertion of the BSY- signal) after it has begun the selection phase (assert SEL- and negate BSY-) before terminating the command. The timeout function can be disabled by loading the TIMEOUT PERIOD register with zero.

The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

6.2.6 Total Sectors Register/CDB 1st Byte

Translate Address:
The TOTAL SECTORS register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer:
This register should be loaded with the first byte of the COMMAND DESCRIPTOR BLOCK before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the first byte of the received CDB in this register.

6.2.7 Total Heads Register/CDB 2nd Byte

Translate Address:
This register holds the total number of heads during a Translate Address command.

Select-and-Transfer:
This register should be loaded with the second byte of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the second byte of the received CDB in this register.

6.2.8 Total Cylinders Register/CDB 3rd and 4th Bytes

Translate Address:
This is a 16-bit register which holds the total number of cylinders.

Select-and-Transfer:
This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the third and fourth bytes of the received CDB in this register.

6.2.9 Logical Address Register/CDB 5th-8th Bytes

Translate Address:
The LOGICAL ADDRESS register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-and-Transfer:
For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-for-Select-and-Receive:
The 33C92A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

6.2.10 Sector Number Register/CDB 9th Byte

Translate Address:
This register will contain the resulting sector number following a Translate Address command.

Select-and-Transfer:
This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the ninth byte of a ten or twelve byte received CDB in this register.

6.2.11 Head Number Register/CDB 10th Byte

Translate Address:
The HEAD NUMBER register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed

by the WD33C92A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-and-Transfer:
This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select- and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the tenth byte of a ten or twelve byte received CDB in this register.

6.2.12 Cylinder Number Register/CDB 11th and 12th Bytes

Translate Address:
The CYLINDER NUMBER register is a 16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the HEAD NUMBER register initially contains a nonzero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track * total heads - total spare sectors/cyl) before issuing the command.

Select-and-Transfer:
This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing aSelect-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-and-Command-Complete:
The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-and-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the 33C92A. If bit 0 of the CDB12 register is set to one, then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 hex) is sent.

6.2.13 Target Lun Register

The TARGET LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various 33C92A commands and sequences. During a Select-and-Transfer or Reselect-and-Transfer command, the contents of this register (along with the SOURCE ID register) are used to generate and check the IDENTIFY messages which are transferred across the SCSI bus. In addition, the TARGET LUN register is used to hold the Target Status byte received during a Select-and-Transfer command.

During Wait-for-Select-and-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether of not the Initiator has enabled disconnects.

During Reselect-and-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.

In advanced mode, during Select-and-Transfer commands, this register is used to handle reselection by an unexpected Target. In this mode, this register will hold the logical unit number of the reselecting target. The TLV and DOK bits will be set to zero.

7	6	5	4	3	2	1	0
TLV	DOK	0	0	0	TL2	TL1	TL0

Bit 0-2 TLx-Target LUN

The Target Logical Unit Numbers bits 0-2.

Bit 3-5 Not Used

Not used bits are zero.

Bit 6 DOK-Disconnects OK

Disconnects permitted.

Bit 7 TLV-TARGET LUN Valid

TARGET LUN Valid.

6.2.14 Command Phase Register

The COMMAND PHASE register is used during combination commands to indicate which phases of these multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bit 0-6 CPx-COMMAND PHASE bits0-6

Bit 7 Not Used.
Not used bits are zero.

6.2.15 Synchronous Transfer Register

The SYNCHRONOUS TRANSFER register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3=OF2=OF1=OF0=0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if WD-Bus mode is used, the transfer period and the width of the RE-/WE- strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.

7	6	5	4	3	2	1	0
0	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx-OFFSET bit 0-3

OFFSET bits 0-3 are used to select the desired offset according to the following:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0(= Asynchronous data
0	0	0	1	1 phase transfers)
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	x	Undefined

Bit 4-6 TPx-TRANSFER PERIOD bits 0-3

The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

6	5	4	SCSI/Bus Transfer Period	(SCSI REQ/ACK* & Bus RE-/WE-
0	0	x	8 cycles	4 cycles
0	1	0	2 cycles	1 cycles
0	1	1	3 cycles	1 cycles
1	0	0	4 cycles	2 cycles
1	0	1	5 cycles	3 cycles
1	1	0	6 cycles	4 cycles
1	1	1	7 cycles	4 cycles

*synchronous pulse width & pulse width

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

cycle = divisor (from OWN ID)(nsec) / 2 * input clock frequency (MHz)

Bit 7 Not Used.

Not used bits are zero.

6.2.16 Transfer Count Register

The TRANSFER COUNT register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a "successful completion" interrupt when the counter reaches zero. In Combination commands, this register specifies the number of bytes to be transferred during a Data phase.

The counter function can be disabled by loading the TRANSFER COUNT register with zeros prior to issuing a command or by setting the SINGLE-BYTE TRANSFER bit in the COMMAND register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the TRANSFER COUNT register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including clearing the internal FIFO of any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the TRANSFER COUNT register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the TRANSFER COUNT should be used to determine the actual number of bytes transferred to/from the SCSI bus.

6.2.17 Destination ID Register

The DESTINATION ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	0	0	0	DI2	DI1	DI0

Bit 0-2 DIx-DESTINATION ID bits 0-2

DESTINATION ID bits 0-2.

Bit 3-5 Not Used.

Not used bits are zero.

Bit 6 DPD-DATA PHASE DIRECTION,

DATA PHASE DIRECTION, when advanced features are enabled (see 7.3), is used to specify the expected direction of the SCSI data phase, when it occurs. This allows the 33C92A to verify the direction during Select-and-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.

Bit 7 SCC-SELECT COMMAND CHAIN

SELECT COMMAND CHAIN is used only when the Reselect-and-Transfer command is issued with EDI=1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

6.2.18 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C92A. It also contains bits that

enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SIV	SIV	SIV

Bit 7 ER-ENABLE RESELECTION

ENABLE RESELECTION, when set to one, enables the 33C92A to respond to a reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.

Bit 6 ES-ENABLE SELECTION

ENABLE SELECTION, when set to one, enables the 33C92A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.

Bit 5 DSP-DISABLE SELECT PARITY

DISABLE SELECT PARITY, when set to one, causes the 33C92A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.

Bit 4 Not Used.

Not used bits are zero.

Bit 3 SIV-SOURCE ID VALID

SOURCE ID VALID is set to one after the 33C92A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the 33C92A) during the select/reselect phase. This bit is zero if only the bus ID bit of the 33C92A was asserted.

Bit 2-0 SIx-SOURCE ID Bits 2-0

SOURCE ID Bits 2-0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the 33C92A.

6.2.19 SCSI Status Register

The SCSI STATUS register is a read-only register which indicates the cause of the most recent INTRQ assertion. INTRQ is asserted whenever a condition occurs within the 33C92A that requires intervention by the host; for example:

- the 33C92A has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

Once INTRQ has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the 33C92A has been reset.

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7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx-SCSI STATUS bits 0-3

SCSI STATUS bits 0-3 are status qualifiers whose meaning depends upon which upper (4-7) status bit is set.

Bit 4-7 SSx-SCSI STATUS bits 4-7

SCSI STATUS bits 4-7 define the type of interrupt that occurred. The possible codes are defined in the following table:

STATUS CODE	GROUP MEANING
0000 xxxx	The 33C92A is in a reset state.
0001 xxxx	A 33C92A command has completed successfully.
0010 xxxx	A 33C92A command has paused or was aborted by an Abort command.
0100 xxxx	A 33C92A command has been terminated prematurely due to an error or other unexpected condition.
1000 xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the current state in which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase:

MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The following table summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

STATUS CODE	STATE	SPECIFIC MEANING
0000 0000	DTI	33C92 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C92A is disconnected.
0000 0001	DTI	33C92A Reset. The device has successfully completed a Reset command with advance features enabled. The new state of the 33C92A is disconnected.

TABLE 6-2. RESET STATE INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0001 0000	D	A Reselect command completed successfully. The new state of the 33C92A is connected as a Target.
0001 0001	D	A Select command completed successfully. The new state of the 33C92A is connected as an Initiator.
0001 0010	-	Reserved for future use.
0001 0011	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is not asserted).
0001 0100	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is asserted).
0001 0101	DT	A Translate Address command completed successfully.
0001 0110	D I	A Select-and-Transfer command completed successfully.
0001 0111	-	Reserved for future use.
0001 1MCI	I	A Transfer (non-MESSAGE IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

TABLE 6-3. SUCCESSFUL COMPLETION INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0010 0000	I	A Transfer Info (MESSAGE-IN phase) command has paused with ACK asserted. This allows the host to examine the message before accepting it.
0010 0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010 0010	D	A Select or Reselect command was aborted.
0010 0011	T	A Receive or Send command was halted by an error or was aborted (ATN is not asserted).
0010 0100	T	A Receive or Send command was halted by an error, assertion of ATN, or was aborted (ATN is asserted).
0010 0101	D	Reserved for future use.
0010 0110	-	Reserved for future use.
0010 0111	D	The 33C92A has been reselected during a Select-and-Transfer (with IDI=0) by a Target that does not match the SCSI bus ID loaded into the DESTINATION ID register, or the following Identify message did not match the LUN loaded into the TARGET LUN register. ACK has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the SOURCE ID and TARGET LUN registers. (Advanced Mode only)
0010 1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

TABLE 6-4. PAUSED OR ABORTED INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0100 0000	DTI	An invalid command was issued.
0100 0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the 33C92A is disconnected.
0100 0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C92A is disconnected.
0100 0011	TI	A parity error caused a command to terminate ATN is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0100	TI	A parity error caused a command to terminate (ATN is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0101	DT	The Logical Address exceeded the disk boundaries.
0100 0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the 33C92A during a Select-and-Transfer command (with IDI=0). This interrupt occurs when the 33C92A is not in Advanced Mode. The new state of the 33C92A is connected as an Initiator.
0100 0111	I	A status byte with bad parity was received during a Select-and-Transfer command. ACK is asserted.
0100 1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested.This is typically caused by a phase change before the Transfer Counthas reached zero, or an unexpected phase sequence occurred during a Select-and-Transfer command.

TABLE 6-5. TERMINATED INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
1000 0000	D	The 33C92A has been reselected. The new state of the 33C92A is connected as an Initiator. No Identify message transfer has yet occurred.
1000 0001	D	The 33C92A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the SOURCE ID register. The Identify message from the Target may be read from the DATA register. The ACK signal is left asserted. The new state of the 33C92A is connected as an Initiator.
1000 0010	D	The 33C92A has been selected (no ATN assertion). The new state of the 33C92A is connected as a Target.
1000 0011	D	The 33C92A has been selected (ATN was asserted). The new state of the 33C92A is connected as a Target.
1000 0100	T	The ATN signal has been asserted.
1000 0101	I	A disconnect has occurred. The new state of the 33C92A is disconnected.
1000 0110	-	Reserved for future use.
1000 0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not a known command group. The OWN ID register must be loaded with the CDB length,and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the 33C92A is connected as a Target. (Advanced Mode only)
1000 1MCI	I	The REQ signal has been asserted following connection or when the 33C92A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

TABLE 6-6. SERVICE REQUIRED INTERRUPTS

6.2.20 Command Register

The COMMAND register is used to issue the 33C92A commands. This register should never be loaded when the CIP or INT bits (in AUXILIARY STATUS) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the TRANSFER COUNT register. The previous contents of the TRANSFER COUNT register are not preserved.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit 0-6 CCx-COMMAND CODE bits 0-6

COMMAND CODE bits 0-6.

Bit 7 SBT-SINGLE-BYTE TRANSFER

SINGLE-BYTE TRANSFER bit.

6.2.21 Data Register

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/WD interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the internal twelve byte FIFO of the 33C92A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the 33C92A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the processor during a data phase when the CONTROL register DMA mode select bits are all reset (=0), and when the DBR bit in the AUXILIARY STATUS register is true. The processor writes (reads) the DATA register by loading the ADDRESS register with a hex value of 19 and asserting the WE- (RE-) and CS- pins. This access also occurs during non-data phases.

When the CONTROL register DMA mode select bits are set for DMA mode or BURST mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the DACK- and WE-(RE-) pins are asserted in response to the assertion by the 33C92A of the DRQ- pin.

When the WD BUS is selected by the DMA mode select bits, the RCS- pin functions as an external buffer chip select and the WE- and RE- pins become outputs, allowing the 33C92A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any other device by negating the DRQ pin.

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6.3 RESET CONDITIONS

6.3.1 Hardware Reset

The following results occur when the 33C92A is reset by the assertion of the MR- signal:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the MR- signal:
  - Registers 01 hex through 15 hex;
  - SOURCE ID (16 hex) register bits 0-3;
  - COMMAND register (18 hex);

The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the 33C92A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

6.3.2 Software Reset

The following results occur when the 33C92A executes the Reset command:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

7.0 COMMANDS

7.1 COMMAND LIST

COMMAND CODE (HEX)	COMMAND	VALID STATES	LEVEL
00	Reset	D,T,I	I
01	Abort	D,T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D,I	II
09	Select-without-ATN-and-Transfer	D,I	II
0A	Reselect-and-Receive-Data	D,T	II
0B	Reselect-and-Send-Data	D,T	II
0C	Wait-for-Select-and-Receive	D,T	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

33C92A States:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

7.2 33C92A COMMAND TYPES

There are two basic types of 33C92A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an AUXILIARY STATUS of BSY=1,CIP=0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single 33C92A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence. These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can be chained together to further minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The 33C92A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the COMMAND LIST. An attempt to issue a Level II command which is invalid for the present 33C92A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

7.3 ADVANCED MODE FEATURES

The 33C92A has several new features included which add new functions to the original 33C92 design. Some of these features cause the 33C92A to be incompatible with the 33C92. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the 33C92A is reset by the MR- signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAF) bit set in the OWN ID register. The host can determine if advanced features have been enabled (thereby implying that a 33C92A is installed) by examining the SCSI STATUS register after issuing the 'Reset' command.

The features enabled by this bit are described in the subsections below.

7.3.1 Unexpected Reselection

When in normal (33C92) mode, a reselection when idle (ER=1) or when disconnected during a Select-and-Transfer command (and the Target bus ID does not match the DESTINATION ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the 33C92A will continue to the Message In phase to fetch the Identify message. If the 33C92A was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the 33C92A was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the Identify message will be in the TARGET LUN register. In either case, the SOURCE ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rEjected.

7.3.2 Unknown SCSI Command Groups

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7-5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands are defined by the SCSI standard (X3.131-1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the 33C92A will assume that these undefined groups are six byte commands when executing Select-and-Transfer or Wait-for-Select-and-Receive commands. In Advanced Mode, the following events will occur:

Select-and-Transfer:

When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The 33C92A uses

this value to make sure the correct number of bytes are then transferred in the command phase.

Wait-for-Select-and-Receive

When receiving the CDB from the Initiator, the 33C92A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host can examine the first command byte in the CDB 1ST register, and then load the TOTAL command length into the OWN ID register. The SCSI STATUS register is set to 87 hex, and the COMMAND PHASE register is set to 31 hex, when this interrupt occurs. After the interrupt, the 33C92A will only accept a Resume Wait-for-Select-and-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the 33C92A will continue to transfer the first six bytes of the command into its internal FIFO.

7.3.3 Data Phase Direction

During a Select-and-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the 33C92A will not detect this error but expects that the transfer will continue. In Advanced Mode, the DPD bit in the DESTINATION ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI STATUS register.

7.4 LEVEL I COMMANDS

7.4.1 Reset (00 hex)

The Reset command performs a similar function to the hardware reset caused by asserting the MR- pin except that the OWN ID register is sampled for information concerning the operating configuration of the 33C92A. The 33C92A is also initialized as described in the RESET CONDITIONS section. The Reset command may be executed in any 33C92A state and will force the 33C92A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 hex or 01 hex, depending on the contents of the OWN ID register.

7.4.2 Abort (01 Hex)

The Abort command is valid in the Disconnected and Connected-as-Target states. The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State

In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the WD33C92A has won arbitration, the WD33C92A releases the SCSI bus by removing the Bus ID bits while SEL- is asserted and checking for a negated BSY- signal. If, after at least 200 us, there is no BSY- response, the WD33C92A goes to a Bus Free condition, and a "paused/aborted" interrupt is generated. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the WD33C92A has not yet won arbitration, it will immediately abort the Select or Reselect command. The abort command will also terminate a Wait-for-Select-and-Receive command, if selection has not already begun. Once selected, the WD33C92A will ignore any abort attempts, and the command will finish normally.

Target State

When the WD33C92A is in a Connected-as-a-Target state, the Abort command may be used to abort Receive, Send, or the data phase portion of a Target combination command.
When issuing an Abort in the Connected-as-a-Target state, the following rules apply:

1. When a Abort command is issued to abort a Send or Reselect-and-Send command, the local processor must not service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The WD33C92A removes the data request at

an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.

2. When a Abort command is issued to abort a Receive or Reselect-and-Receive command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processorhas received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C92A remains in the Connected-as-a-Target state. The WD33C92A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

7.4.3 Disconnect (04 hex)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the 33C92A transitions to the Disconnected state.

7.4.4 Assert ATN (02 hex)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (The Target is expected to respond by performing a Message Out Phase). ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the Target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C92A to automatically assert ATN prior to the release of SEL- providing the bus arbitration is won.

7.4.5 Negate ACK (03 hex)

The Negate ACK command causes ACK to be negated. It may be used:

- When Connected as an Initiator following Message-In Transfer Info commands.
- After the 33C92A has detected a parity error on any received information and the HALT on SCSI PARITY ERROR (HSP) bit is set.
- After unexpected reselection in advanced mode.
- After a Save-Data-Pointer message is received during a Select-and-Transfer command.
- Host parity errors do not affect the ACK signal. For all other Initiator transfers, ACK negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "MESSAGE REJECT" or a "MESSAGE PARITY ERROR" Message by issuing the Assert ATN command prior to issuing the Negate ACK command. If the incoming message is to be accepted, only the Negate ACK command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by a parity error, the Assert ATN command can again be issued prior to

Negate ACK, this time indicating the Initiator's intent to send an "INITIATOR DETECTED ERROR" Message.

7.4.6 Set IDI (0F hex)

The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the CONTROL register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of 33C92A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

7.5 SIMPLE LEVEL II COMMANDS

7.5.1 Select-with-ATN (06 hex)

Select-with-ATN is valid only in the Disconnected state and when issued will cause the 33C92A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the DESTINATION ID register. When the Select-with-ATN command is issued, the 33C92A begins bus arbitration. If the 33C92A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x hex) is generated.

Should the 33C92A win the arbitration, SEL- and ATN are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then BSY- is deasserted. At this time, a timeout sequence whose length is determined by the value in the TIMEOUT PERIOD register begins. If BSY- is not asserted by the Target before a timeout occurs, the 33C92A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select-with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the 33C92A negates the SEL-signal, putting the 33C92A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the 33C92A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the 33C92A is disconnected from the bus and a "paused/aborted" interrupt is generated.

7.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with-ATN command except that ATN is not set during the Selection Phase.

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7.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C92A being Connected as a Target.

7.5.4 Receive (10-13 hex)

There are four Receive commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of the Receive command selected determines the state of the I/O-, C/D-, and MSG outputs during the command according to the following chart (1=asserted):

Receive Command Type	OP Code	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

The Receive commands are information transferring commands and are therefore dependent on the SBT bit in the COMMAND register for deter-

mination of a successful completion. In addition to a termination caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Receive command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred.
3. A parity error has been detected on one of the received data bytes (and HSP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.
6. A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the TRANSFER COUNT register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the 33C92A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the CONTROL register for the DATA register accessing mode. These bits determine whether the DATA register accesses will be handled by the processor or through a DMA/WD interface. When the processor is required to read the DATA register (i.e. DMA mode select bits=0), it must monitor the DBR status bit (in AUXILIARY STATUS) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the DATA register and set when a byte is loaded into the DATA register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the SYNCHRONOUS TRANSFER register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

7.5.5 Send (14-17 hex)

As in the case of the Receive commands, there are four Send commands which are distinguished only by the state of the I/O-,C/D-, and MSG pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular command as follows (asserted=1):

Send Command Type	OP Code	MSG	C/D	I/O
Send Status	14	0	1	1
Send Data	15	0	0	1
Send Message In	16	1	1	1
Send Unspecified Info In	17	1	0	1

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the COMMAND register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Send command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred
3. A parity error has been detected on one of the data bytes from the host (and HHP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.

6. A Disconnect command is issued. The 33C92A remains Connected-as-a-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, DATA register accessing is controlled by the DMA mode select bits in the CONTROL register. When these bits are set to the appropriate mode, loading of the DATA register is accomplished by a DMA controller or through the WD-Bus interface. If the DMA mode select bits are zero, the processor must poll the AUXILIARY STATUS register and can write to the DATA register only when the DATA BUFFER READY bit is set (DBR=1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the DATA register and set when a byte is transferred from the DATA register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

7.5.6 Transfer Info (20 hex)

The Transfer Info command is valid only when Connected as an Initiator and is used to send and receive data, command, status, and message information.

The first REQ assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the 33C92A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when completion of the Transfer Info command depends upon the internal transfer counter, the processor should load the TRANSFER COUNT register prior to issuing this command. The DMA mode select bits in the CONTROL register, the offset and transfer period bits in the SYNCHRONOUS TRANSFER register, and the SBT bit in the COMMAND register are used during Transfer Info commands just as they are during the Send and Receive commands. However, for processor access of the DATA register during Transfer Info commands (when the DMA mode select bits are zero or the bus phase is other than Data phase), behavior of the DATA BUFFER READY (DBR) status bit is determined by the direction of information transfer as defined by the I/O- pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the DATA register and is set when the byte is transferred from the DATA register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the DATA register and is reset by reading the DATA register. DBR is also reset whenever a Transfer Info command is issued.

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There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect command, causing an immediate disconnect but no interrupt.

A Transfer Info command will either complete or pause when the specified number of bytes (either a single byte or multiple bytes as defined by the SINGLE-BYTE TRANSFER bit in the COMMAND register) has been sent or received. The 33C92A generates a "successful completion" interrupt only after receiving another REQ from the Target during non-Message-In information phases but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional REQ (Note that when the completed Transfer Info command was a Message-In transfer phase, the ACK pin will be left asserted by the 33C92A in the last REQ/ACK cycle of the command, and the processor is required to issue a Negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message).

If a parity error is detected on a data byte received from the SCSI bus (and HSP=1) or on a data byte byte received from the host (and HHP=1), then the 33C92A will terminate the command and, for SCSI parity errors, will leave ACK asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, a negation of the BSY- signal (i.e. the Target suddenly disconnects) or a transition in the I/O-, C/D-, and/or MSG pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP=0 or HHP=0, as appropriate), the 33C92A will still set the PARITY ERROR status bit in the AUXILIARY STATUS register but will not terminate the command as a result of this error.

7.5.7 Translate Address (18 hex)

The Translate Address command performs a logical-address to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can load the logical address into the 33C92A LOGICAL ADDRESS register and then issue the Translate Address command to have the 33C92A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUMBER registers to extract the logical address. The disk parameters contained in the TOTAL SECTORS, TOTAL HEADS, and TOTAL CYLINDERS registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the WD33C92A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded, respectively, into the HEAD NUMBER and CYLINDER NUMBER registers. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

7.6 COMBINATION LEVEL II COMMANDS

7.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C92A's internal microprocessor to manage the low-level SCSI protocol, resulting in as few as one interrupt per SCSI operation. Select-and-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases:

1. Selection of a Target device.
2. Sending of a command.
3. Reception of status information.
4. Reception of a COMMAND COMPLETE Message.

These commands optionally consist of a Data Transfer phase and additional Message Transfer phases.

The 33C92A will update the COMMAND PHASE register as the Select-and-Transfer command executes. Upon completion or termination of the command, the local processor can read this register to determine where the SCSI operation stopped.

The two Select-and-Transfer commands differ from each other only by whether or not the ATN pin is asserted during the Selection phase. The ability to assert ATN during Selection supports the SCSI Message Protocol which calls for an IDENTIFY Message Out phase following the Selection. When executing a Select W/ATN-and-Transfer commands, the 33C92A expects the Target to request a Message Out phase immediately following selection, whereas for a Select W/O ATN-and-Transfer command, it expects the Target to directly enter Command phase. The Select-and-Transfer commands, moreover, support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands.

When a Select-and-Transfer command is issued, the 33C92A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-and-Transfer command halts and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the Selection is successful, no interrupt is generated, but the COMMAND PHASE register will be set to a hex 10.

After completing the Selection phase, the 33C92A begins an information transfer phase. If ATN has been asserted (i.e. a Select W/ATN-and-Transfer command was issued), the 33C92A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the 33C92A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the 33C92A will respond by automatically sending an IDENTIFY Message. This single byte message is of the binary

form: 1r000ttt, where r=1 if the ENABLE RESELECTION bit in the SOURCE ID register is equal to 1, and ttt is the encoded Target LOGICAL UNIT NUMBER contained in the TARGET LUN register. Once the IDENTIFY Message has been sent, the 33C92A will set the COMMAND PHASE register to hex 20.

Following the Message Out phase (or Selection phase when ATN was not asserted during Selection), a Command phase is expected by the 33C92A. Again, and throughout the entire Select-and-Transfer command execution, if the Target requests an unexpected information phase type, the 33C92A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the 33C92A will extract the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and send the 6-, 10-, or 12-bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The COMMAND PHASE register is set to hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the COMMAND PHASE register will contain hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the 33C92A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The 33C92A therefore expects to receive either a Save-Data-Pointer message (hex 02) or a Disconnect message (hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the DATA register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save-Data-Pointer message is received, a "paused/aborted" interrupt is generated and the Select-and-Transfer command terminated to allow the processor to save the SCSI data pointer. However, if a Disconnect message is received, the COMMAND PHASE register will be updated to hex 42 and command execution continues.

When the actual Target-disconnection does occur, the COMMAND PHASE register is updated to hex 43 and if the IDI bit is set, the WD33C92A terminates the Select-and-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the WD33C92A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the 33C92A, a "terminated" interrupt is generated. However, if the original Target Reselects the 33C92A, no interrupt is generated and the COMMAND PHASE register is set to hex 44.

Following the original Target Reselection, the 33C92A expects a Message In phase which should consist of the Target sending an IDENTIFY Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target LUN. If the data received by the 33C92A is different or the Target LUN specified in this byte does not match the contents of the TARGET LUN register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct IDENTIFY Message In phase results in the COMMAND PHASE register being updated to hex 45.

After the IDENTIFY Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase, or Status phase should occur. If the TRANSFER COUNT register contains any non-zero value, then the 33C92A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the 33C92A will use the TRANSFER COUNT register to determine the number of bytes to be transferred, and all host-side DATA register accesses will be accomplished via the method selected by the DMA mode select bits in the CONTROL register. When the internal counter reaches zero, the Data Transfer phase is complete and the COMMAND PHASE register is set to hex 46.

Any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the 33C92A following the Data Transfer phase (or instead of the Data Transfer phase when the TRANSFER

COUNT register contains a value of zero). At the start of the Status phase, the COMMAND PHASE register is loaded with hex 47. Upon completion of the Status phase, the COMMAND PHASE register will be updated to hex 50, and the received status byte is stored in the TARGET LUN register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The 33C92A expects the Target to send a COMMAND COMPLETE Message (hex 00) to indicate that the SCSI command operation has been completed. After the 33C92A receives this COMMAND COMPLETE Message, the COMMAND PHASE register advances to hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the TARGET LUN register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when another REQ is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion" interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-and-Transfer commands, an abnormal or unexpected condition will cause the 33C92A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the 33C92A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the 33C92A being in a Disconnected state. Transfer commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Select-and-Transfer commands, and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C92A is in the disconnected state.
10	The Target has been selected. The 33C92A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The 33C92A is now in the disconnected state.
44	The 33C92A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The 33C92A is now in the connected as an Initiator state.
45	The 33C92A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The 33C92A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The 33C92A has successfully received a Command Complete message from the Target.

A "Resume Select-and-Transfer" command is assumed whenever a normal "Select-and-Transfer" command is issued while the 33C92A is in the Connected-As-An-Initiator state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Select-and-Transfer command execution. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun (REQ asserted).
41	Resume after Command phase or after Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data has has been completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

7.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands include the Reselect-and-Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C92A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the CONTROL register; and the SCC bit in the DESTINATION ID register. The SCSI bus phase sequences are summarized below.

Refer to the command descriptions of the Send-Status-and-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

1. Reselect-and-Receive command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Completion interrupt.

2. Reselect-and-Send command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Completion interrupt.

3. Reselect-and-Receive command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Status-and-Command Complete;

4. Reselect-and-Send command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Status-and-Command-Complete;

5. Reselect-and-Receive command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Disconnect-Message;

6. Reselect-and-Send command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Disconnect-Message;

If the reselection attempt times out during a Reselect-and-Transfer command, ATN is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the COMMAND

PHASE register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI=0, then a "successful completion" interrupt would be generated at this point. However, if EDI=1, no interrupt is generated and command chain occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Reselect-and-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C92A is in the disconnected state.
10	The 33C92A has successfully reselected the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

A "Resume Reselect-and-Transfer" command is assumed whenever a normal "Reselect-and-Transfer" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C92A to idle until it is selected by an Initiator, at which time the 33C92A will enter the Target mode and message and command information will automatically be requested. As an option, the 33C92A may be programmed to disconnect when a SCSI read command is received while executing a Wait-for-Select-and-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If ATN was asserted by the Initiator during the selection phase, the 33C92A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (hex addresses 03 to 0E), and if a valid IDENTIFY message is received, it will be saved in the TARGET LUN register (hex address 0F). The number of command bytes requested by the 33C92A is determined by the SCSI group code in the first byte of the CDB.

After the 33C92A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the 33C92A is enabled to perform an automatic disconnect when a SCSI read command is received. Therefore, when EDI=1 and the 1st CDB byte received contains a 6-, 10-, or 12-byte read command code, then the 33C92A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the COMMAND PHASE register should be read to determine which phase of the Wait-for-Select-and-Receive command was last completed before the error condition occurred. A COMMAND PHASE hex value of hex 10 indicates that the 33C92A was successfully selected. A hex value of 20 indicates that a message was received from the Initiator, and when the 33C92A begins receiving command bytes, the COMMAND PHASE is set to hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Wait-for-Select-and-Receive command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C92A has not been selected. The 33C92A is in the disconnected state.
10	The 33C92A has been successfully selected by the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The 33C92A has begun command phase by setting the SCSI bus phase signals and asserting REQ.
31	The 33C92A has transferred 1 command byte from the Initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The 33C92A has transferred x command bytes from the Initiator.

A "Resume Wait-for-Select-and-Receive" command is assumed whenever a normal "Wait-for-Select-and-Receive" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the Initiator is complete; start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the TARGET LUN register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the 33C92A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the OWN ID register.

7.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-and-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs.

The bits used by the 33C92A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the COMMAND PHASE register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

1. CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex). A "successful completion" interrupt now occurs.

2. CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

3. CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (0B hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

A Send-Status-and-Command-Complete command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-and-Command-Complete" command is assumed whenever a normal "Send-Status-and-Command-Complete" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Send-Status-and-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

7.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save-Data-Pointer message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The COMMAND PHASE register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save-Data-Pointer message is sent, the COMMAND PHASE will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the COMMAND PHASE register will contain a 43H.

A Send-Disconnect-Message command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C92A is now in the disconnected state.

8.0 DC ELECTRICAL SPECIFICATIONS

8.1 MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-55° C to 125° C
Voltage on any pin with respect to GND	-0.5 to 7 Volts
Power dissipation	190 mW
Input Static Discharge Protection	2000 V pin to pin

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

8.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70° C
V_{CC}	+5 Volts ± 0.25 V
V_{SS}	0 Volts

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8.3 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage	---	10	µA	V_{IN} = .4 to VCC
I_{OL}	Output Leakage (inactive)	---	50	µA	V_{OUT} = .4 to VCC
V_{IH}	Input High Voltage	2.0	---	V	
V_{IL}	Input Low Voltage	---	0.8	V	
V_{OH}	Output High Voltage	2.4	---	V	I_O = -400 µA
V_{OL1}	Output Low Voltage (TGS, IGS)	---	0.4	V	I_O = 7.0 mA
V_{OL2}	Output Low Voltage (all others)	---	0.4	V	I_O = 4.0 mA
I_{CC}	Supply Current	---	36	mA	T_A = +25°C

9.0 AC OPERATING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges. All pins are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, except for SCSI bus pins, which are referenced to 1.5 volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

Tcyc =Tcp * DIVISOR/ 2

where:

Tcyc is the internal clock cycle time;
Tcp is the period of the clock at the CLK input;
DIVISOR is the clock divisor selected in the OWN ID register.

For example, with a 16MHz clock input to the 33C92A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

Tcyc = 62.5 nsec * 4/ 2 = 125 nsec

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9.1 PROCESSOR/DMA INTERFACE

9.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	CLOCK PERIOD	50	125	ns
tch	CLOCK HIGH	20		ns
tcl	CLOCK LOW	20		ns

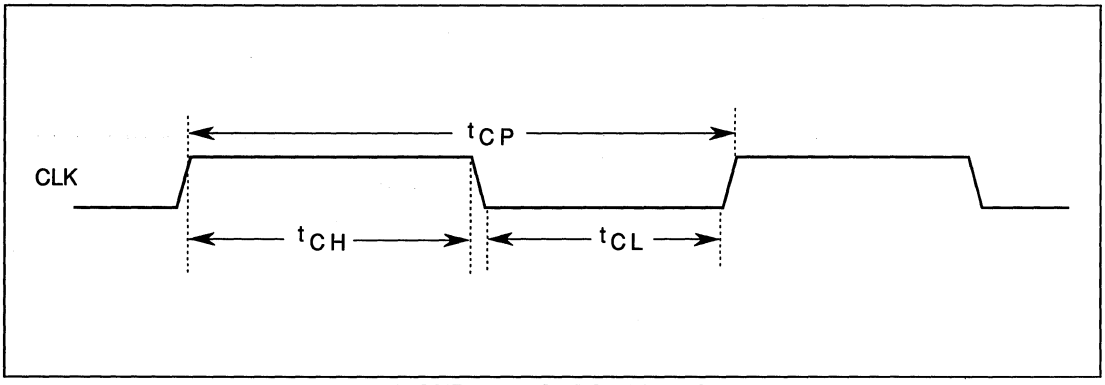

FIGURE 9-1. CLOCK TIMING

9.1.2 MR-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	MR- PULSE WIDTH	1		µs

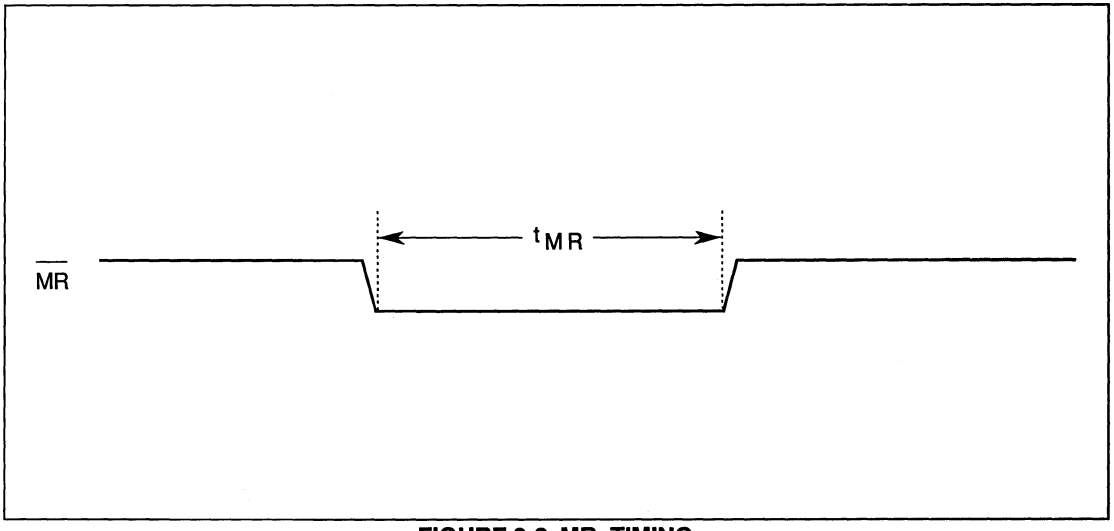

FIGURE 9-2. MR- TIMING

9.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 VALID TO WE- LOW	0		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhai	WE- HIGH TO A0 INVALID	0		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns

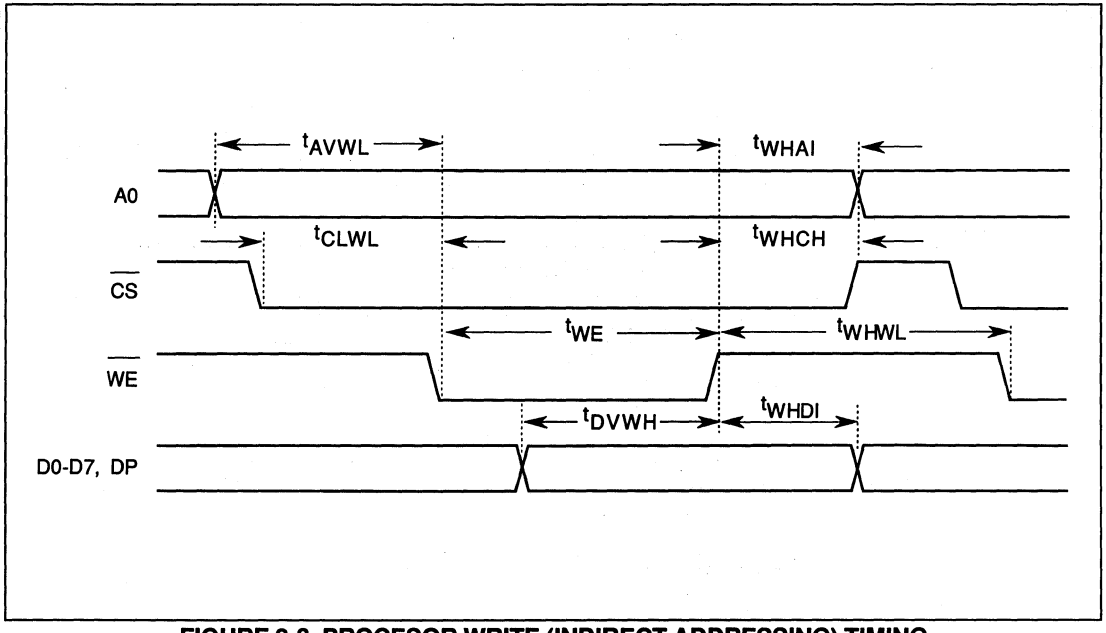

FIGURE 9-3. PROCESOR WRITE (INDIRECT ADDRESSING) TIMING

9.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 VALID TO RE- LOW	0		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID	---	180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
trhai	RE- HIGH TO A0 INVALID	0		ns

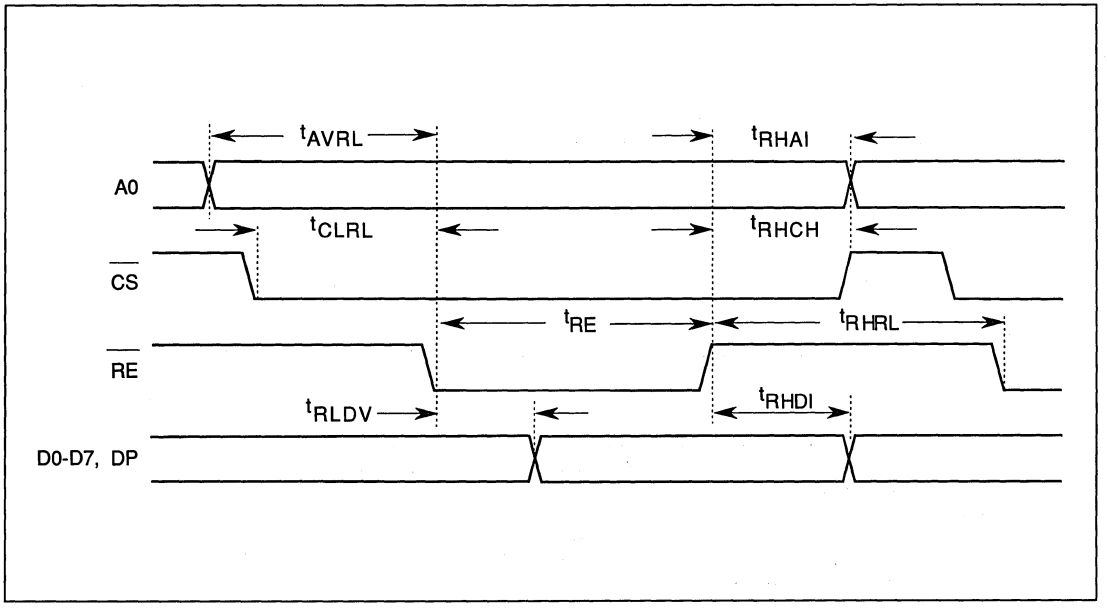

FIGURE 9-4. PROCESSOR READ (INDIRECT ADDRESSING) TIMING

9.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talwl	ALE LOW TO WE- LOW	90		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW	---	1	µs

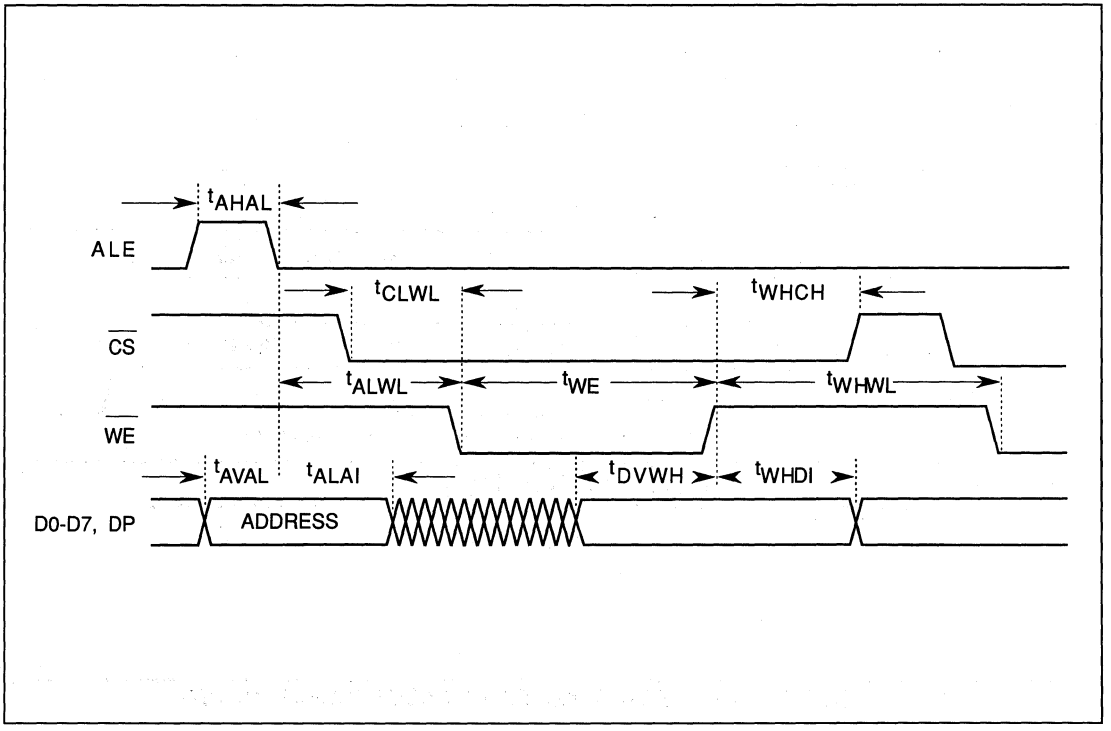

FIGURE 9-5. PROCESSOR WRITE (DIRECT ADDRESSING) TIMING

9.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talrl	ALE LOW TO RE- LOW	30		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID		180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW		1	µs

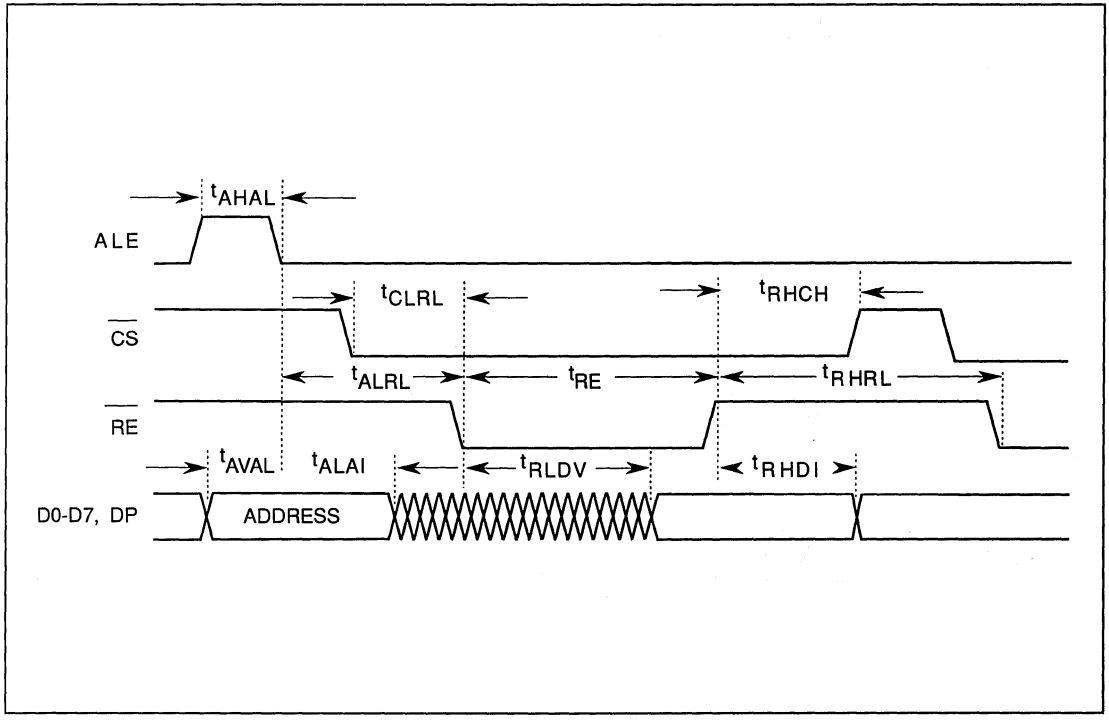

FIGURE 9-6. PROCESSOR READ (DIRECT ADDRESSING) TIMING

9.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	100		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

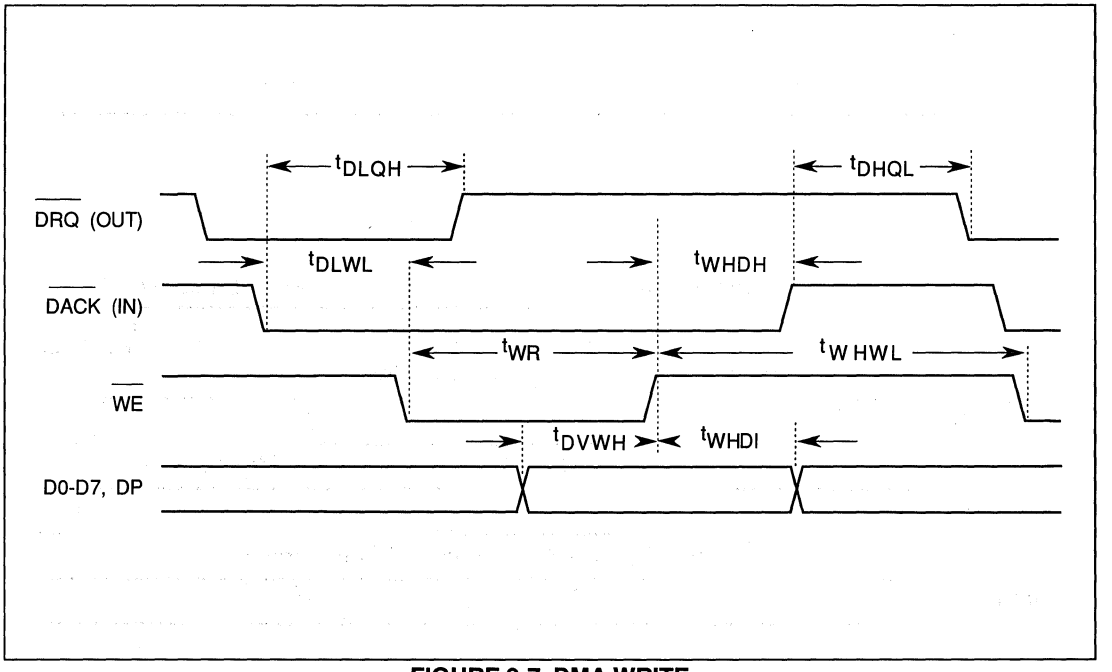

FIGURE 9-7. DMA WRITE

9.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	100		ns
trldv	RE- LOW TO DATA VALID		70	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

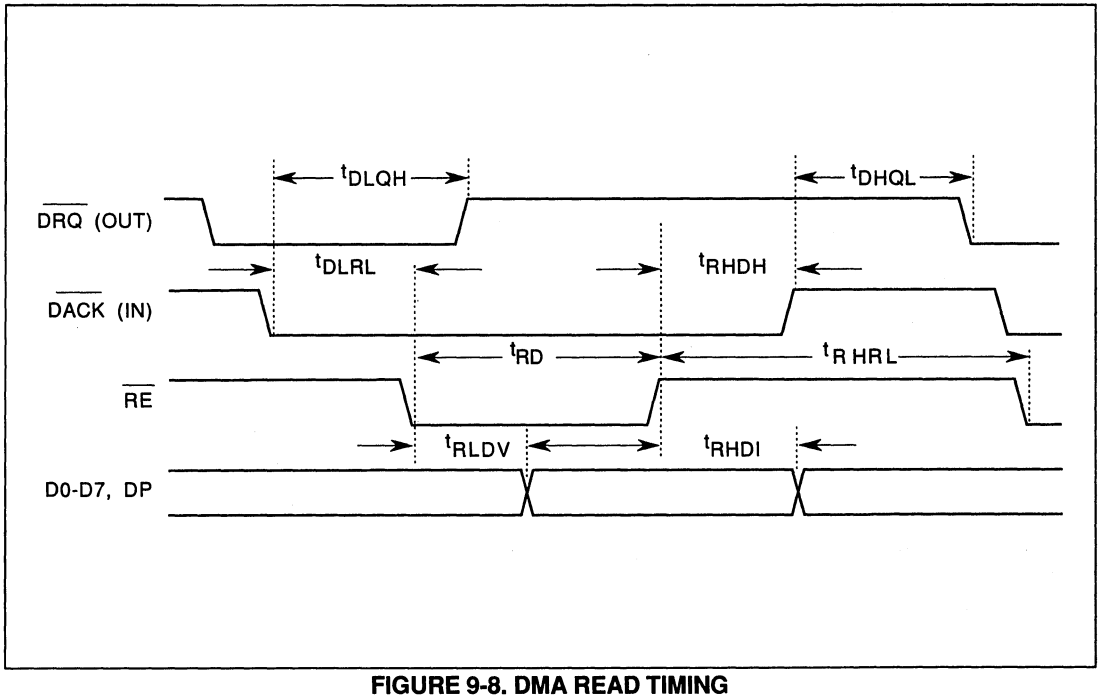

FIGURE 9-8. DMA READ TIMING

9.1.9 Bus Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslwv	RCS- LOW TO WE- VALID	-5	20	ns
two	WE- PULSE WIDTH	1-20ns		Tcyc
twldv	WE- LOW TO DATA VALID		50	ns
twhdi	WE- HIGH TO DATA INVALID	10		ns
twhwl	WE- HIGH TO WE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshwi	RCS- HIGH TO WE- INVALID		100	ns
twhsh	WE- HIGH TO RCS- HIGH	0		ns
tslwl	RCS- LOW TO WE- LOW	60		ns
tqlwl	DRQ LOW TO WE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

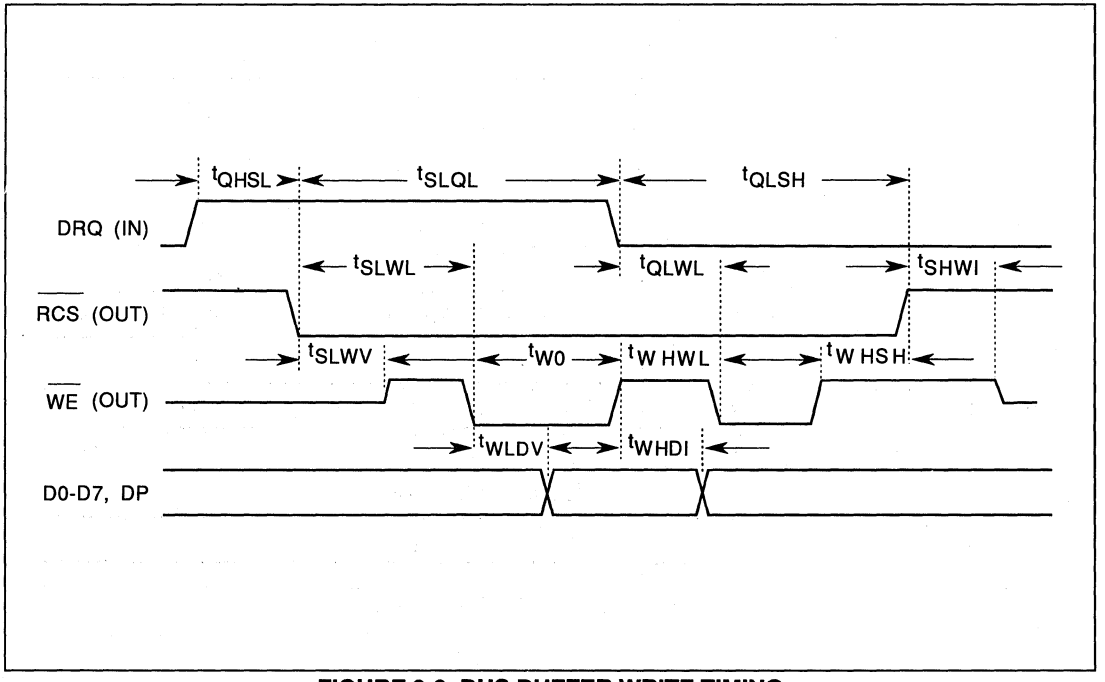

FIGURE 9-9. BUS BUFFER WRITE TIMING

9.1.10 Bus Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslrv	RCS- LOW TO RE- VALID	-5	20	ns
tro	RE- PULSE WIDTH	1-20ns		Tcyc
tdvrh	DATA VALID TO RE- HIGH	20		ns
trhdi	RE- HIGH TO DATA INVALID	0		ns
trhrl	RE- HIGH TO RE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshri	RCS- HIGH TO RE- INVALID		100	ns
trhsh	RE- HIGH TO RCS- HIGH	0		ns
tslrl	RCS- LOW TO RE- LOW	60		ns
tqlrl	DRQ LOW TO RE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

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(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

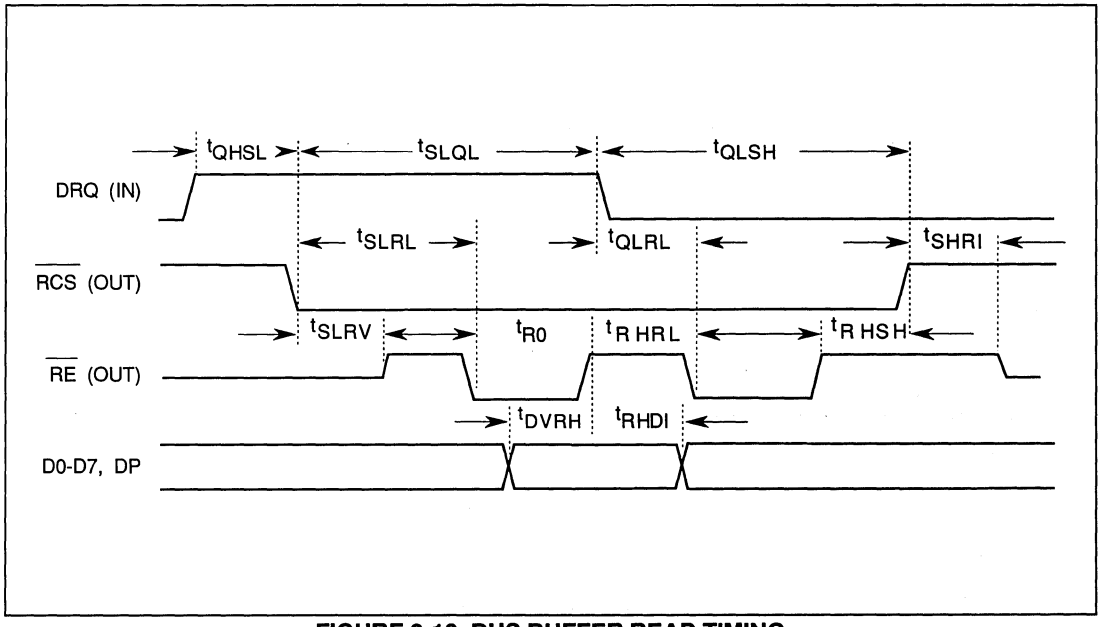

FIGURE 9-10. BUS BUFFER READ TIMING

9.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
twlqh	WE- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	80		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

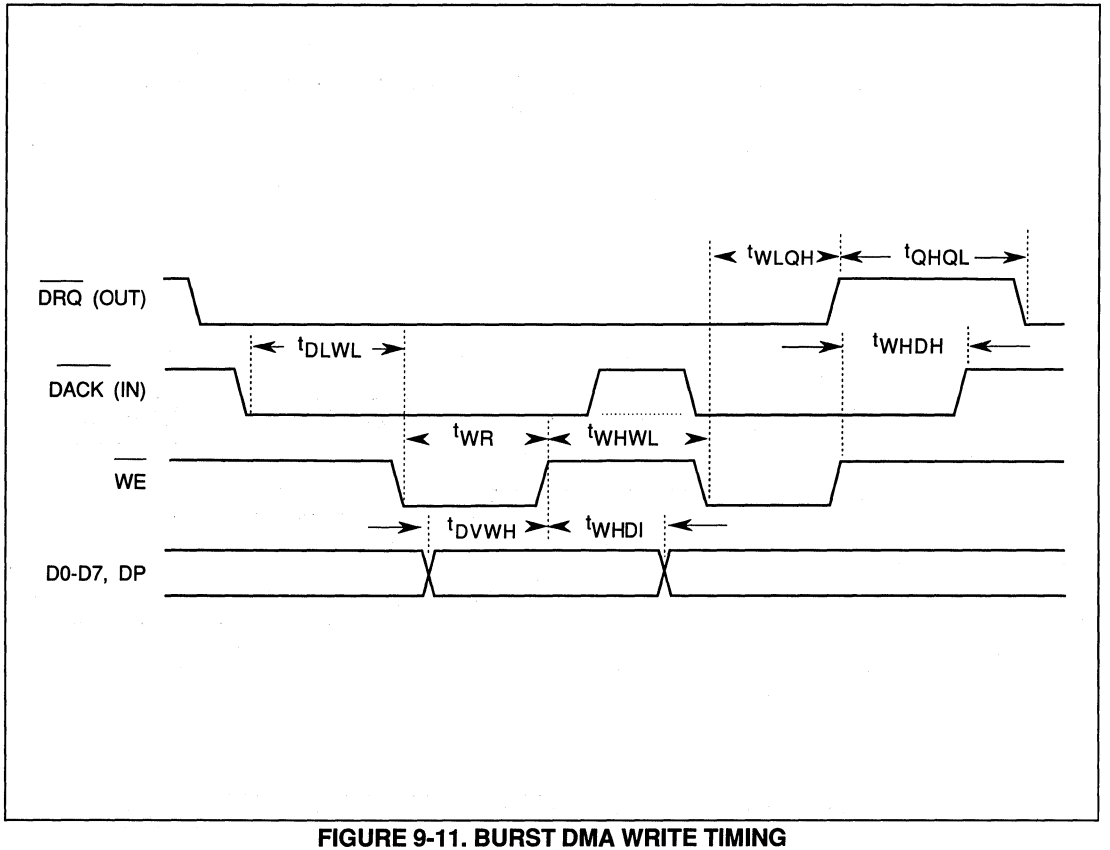

FIGURE 9-11. BURST DMA WRITE TIMING

9.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
trlqh	RE- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	80		ns
trldv	RE- LOW TO DATA VALID		50	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

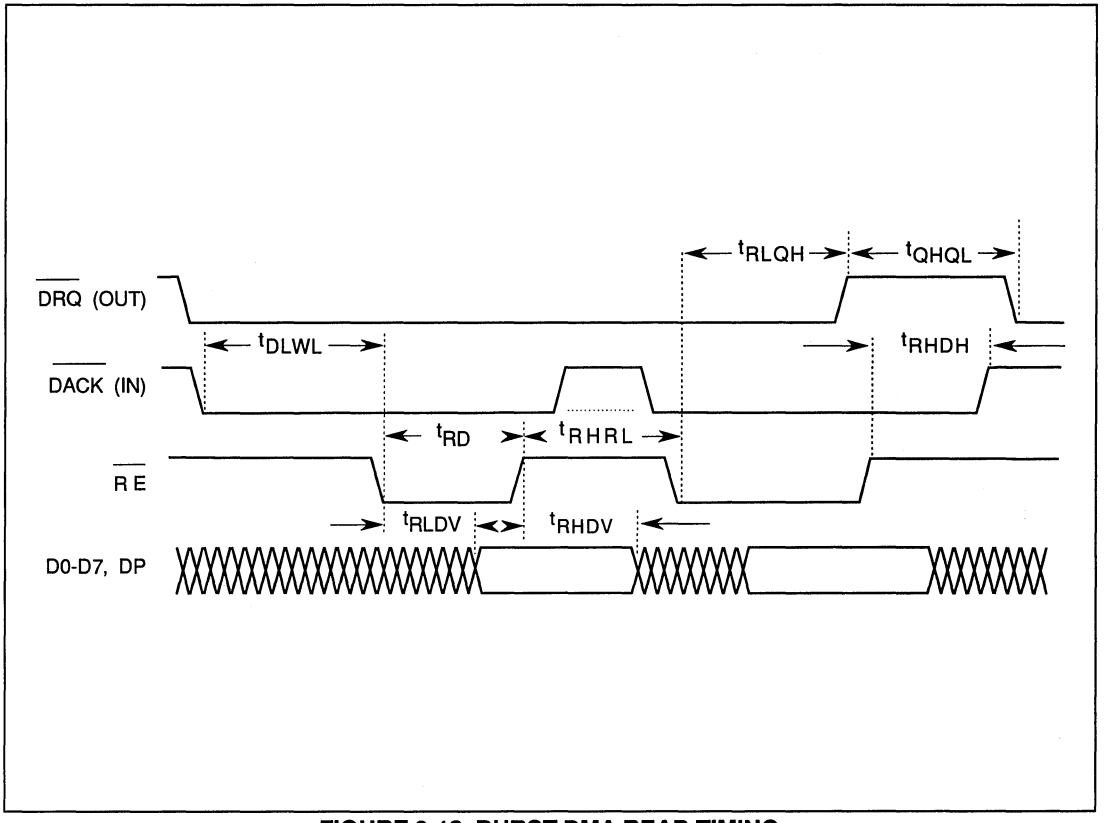

FIGURE 9-12. BURST DMA READ TIMING

9.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ HIGH TO RE- LOW	0		ns
tri	RE- PULSE WIDTH	180		ns
trhil	RE- HIGH TO INTRQ LOW	0	100	ns
tilih	INTRQ LOW TO INTRQ HIGH	100		ns

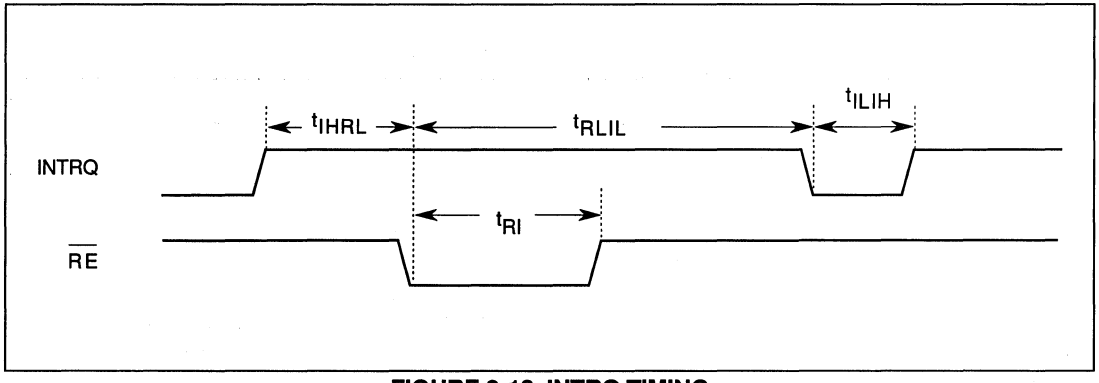

FIGURE 9-13. INTRQ TIMING

9.2 SCSI INTERFACE

9.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblel	BSYI, SELI LOW TO SDIE LOW	4		Tcyc
telio	SDIE LOW TO BUS ID OUT	1		Tcyc
tioah	BUS ID OUT TO ARBLD HIGH	1		Tcyc
tahdf	ARBLD HIGH TO DATA FLOAT	1		Tcyc
tdfeh	DATA FLOAT TO SDIE, SDOE HIGH	1		Tcyc
tblbh	BSYI, SELI LOW TO BSYO HIGH	12	17	Tcyc
tbheh	BSYO HIGH TO SDIE, SDOE HIGH	0	200	ns
tbhsh	BSYO HIGH TO SELO HIGH	2.2		µs

22

NOTE:
I/O* = I/O, C/D, MSG, REQ; ATN* = ATN, ACK

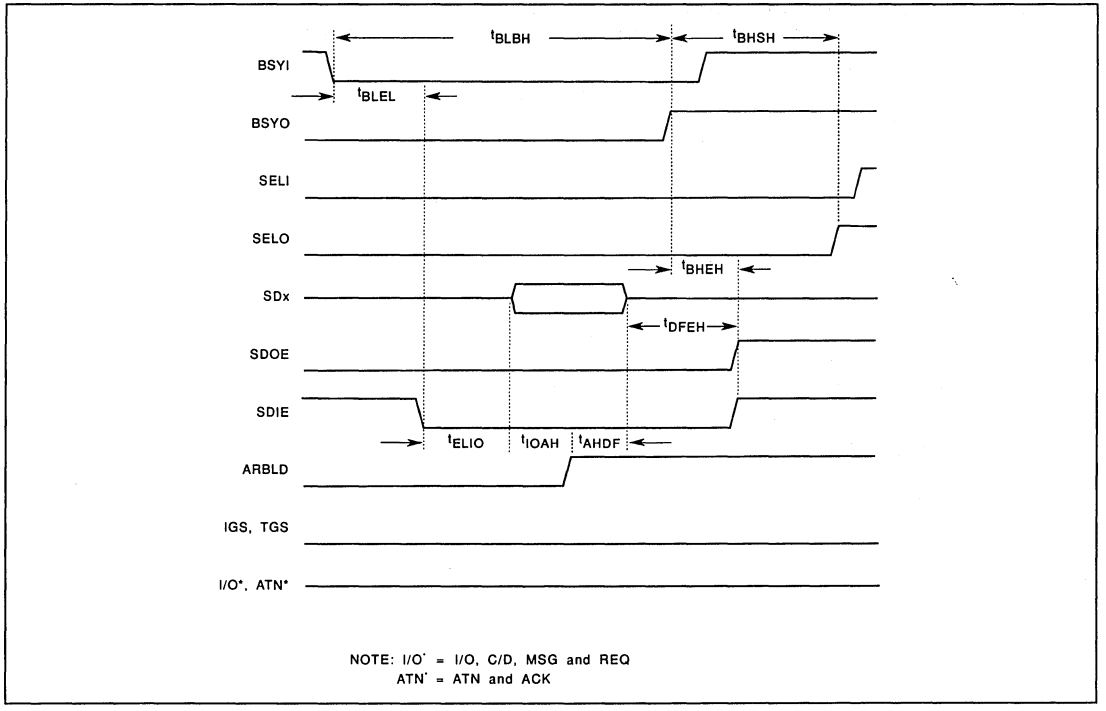

FIGURE 9-14. ARBITRATION TIMING

9.2.2 Selection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO IGS HIGH	100		ns
taogh	ATN, ACK OUT TO IGS HIGH	100		ns
tghav	IGS HIGH TO ATN VALID	400		ns
tavbl	ATN, ACK VALID OUT TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSY HIGH VALID	400		ns
tbhsl	BSYI HIGH TO SELO LOW	100		ns

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDIE* = SDIE, ARBLD

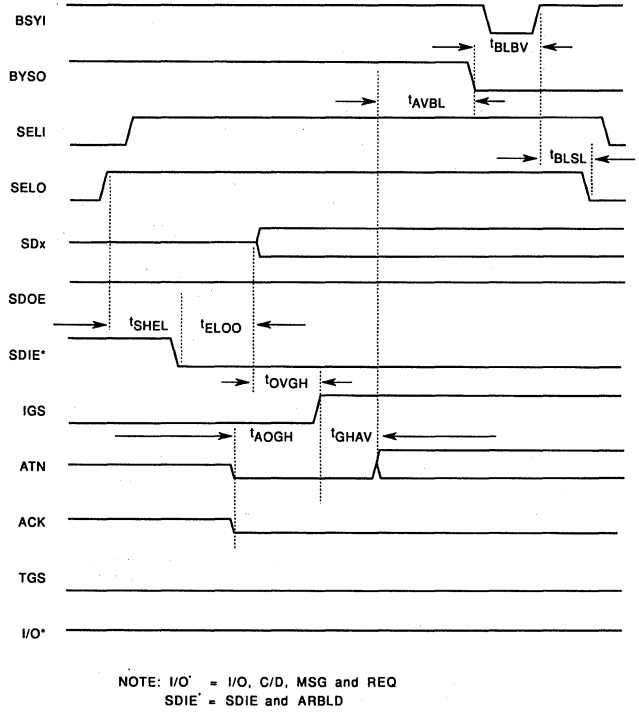

FIGURE 9-15. SELECTION (INITIATOR) TIMING

9.2.3 Selection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tblbh	SELI HIGH, ID VALID, BSYI LOW TO BSYO HIGH	0.4	200	µs
tbhoi	BSYO HIGH TO "OR-ED" ID INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tavsl	ATN VALID IN TO SELI LOW	0		ns
tslio	SELI LOW TO I/O OUT	100		ns
tivgh	I/O OUT VALID TO TGS HIGH	100		ns

22

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDOE* = SDOE, ARBLD

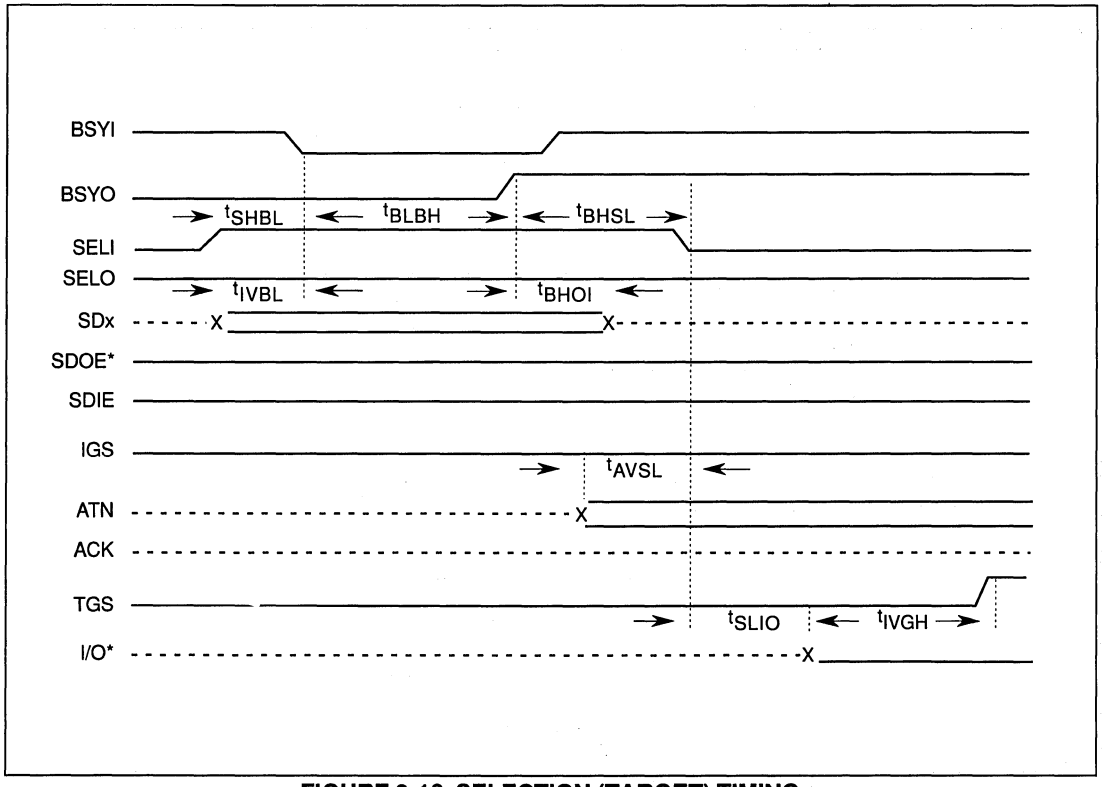

FIGURE 9-16. SELECTION (TARGET) TIMING

9.2.4 Reselection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO IGS HIGH	100		ns
taogh	ATN, ACK OUT TO IGS HIGH	100		ns
tghav	IGS HIGH TO ATN VALID	400		ns
tavbl	ATN, ACK VALID OUT TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSY HIGH VALID	400		ns
tbhsl	BSYI HIGH TO SELO LOW	100		ns

NOTE:
C/D* = C/D, MSG, REQ; ATN* = ATN, ACK; SDIE* = SDIE, ARBLD

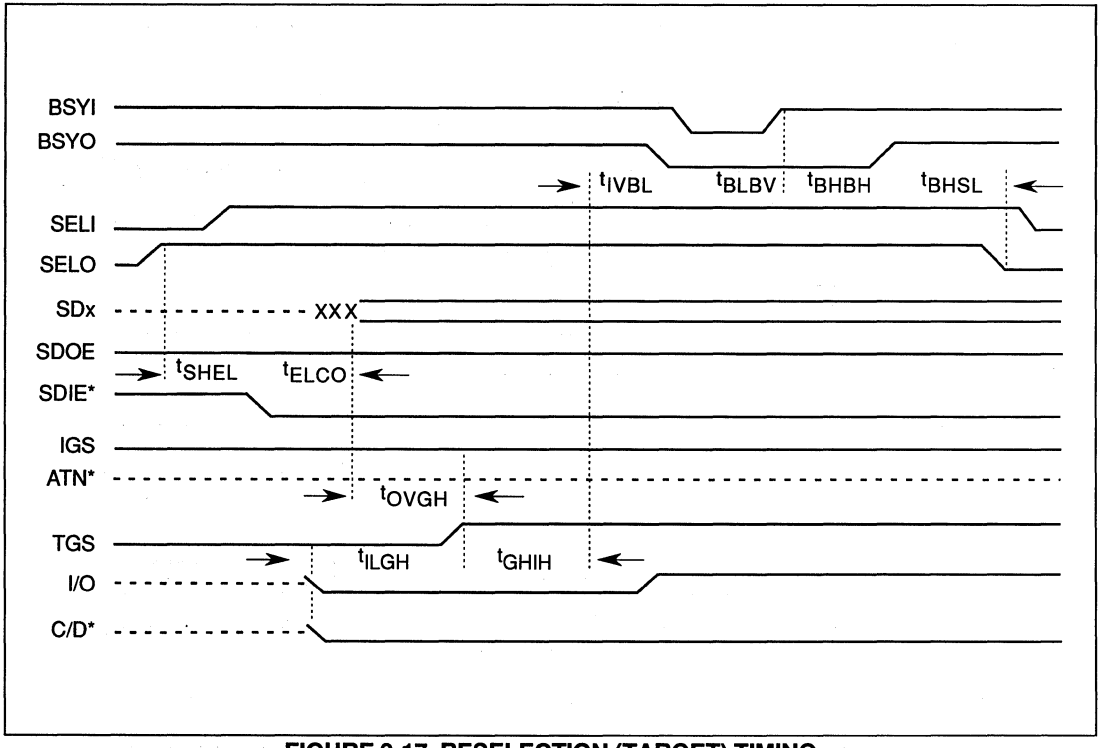

FIGURE 9-17. RESELECTION (TARGET) TIMING

9.2.5 Reselection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tihbl	I/O IN HIGH TO BSYI LOW	0		ns
tblal	SELI HIGH, ID VALID, BSYI LOW TO ATN LOW	0		ns
tghao	IGS HIGH TO ATN OUT	100		ns
talgh	ATN LOW TO IGS HIGH	400		ns
tihbh	IGS HIGH TO BSYO HIGH	100		ns
tblbh	BSYI LOW TO BSYO HIGH	0.4	200	ns
tbhoi	BSYO HIGH TO "OR-ED" INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tslbl	SELI LOW TO BSYO LOW	0		ns

22

NOTE:
ATN* = ATN, ACK; SDOE* = SDOE, ARBLD, SELO; C/D* = C/D, MSG, REQ

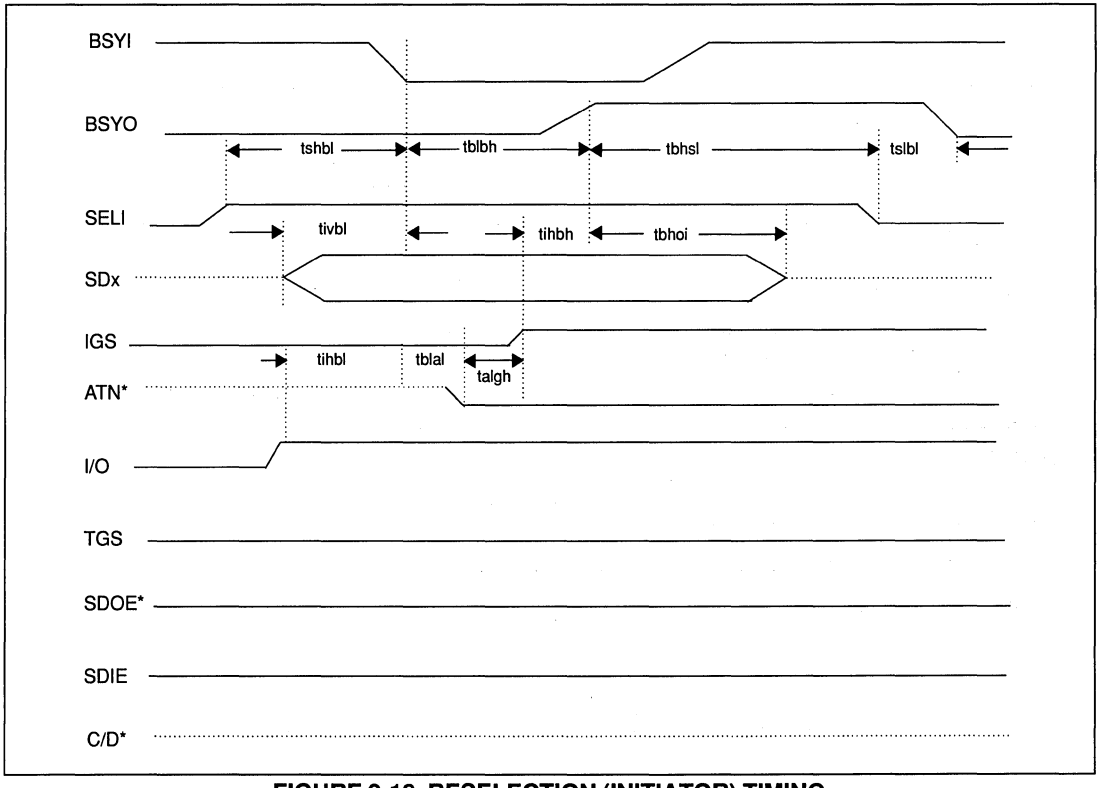

FIGURE 9-18. RESELECTION (INITIATOR) TIMING

9.2.6 Asynchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tihol	I/O IN HIGH TO SDOE LOW, DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
tahdi	ACK OUT HIGH TO DATA INVALID IN	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

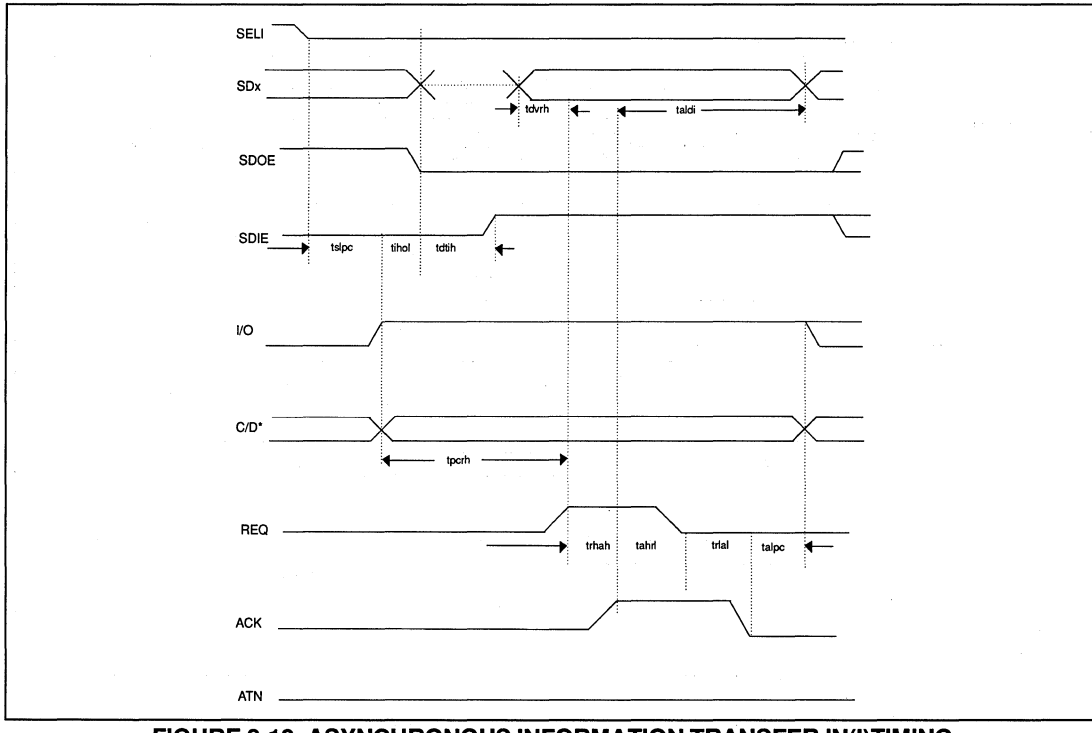

FIGURE 9-19. ASYNCHRONOUS INFORMATION TRANSFER IN(I)TIMING

9.2.7 Asynchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tihil	I/O OUT HIGH TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tdvrh	DATA OUT VALID TO REQ OUT HIGH	80		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
tahdi	ACK IN HIGH TO DATA OUT INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	100		ns

22

NOTE: C/D* = C/D, MSG

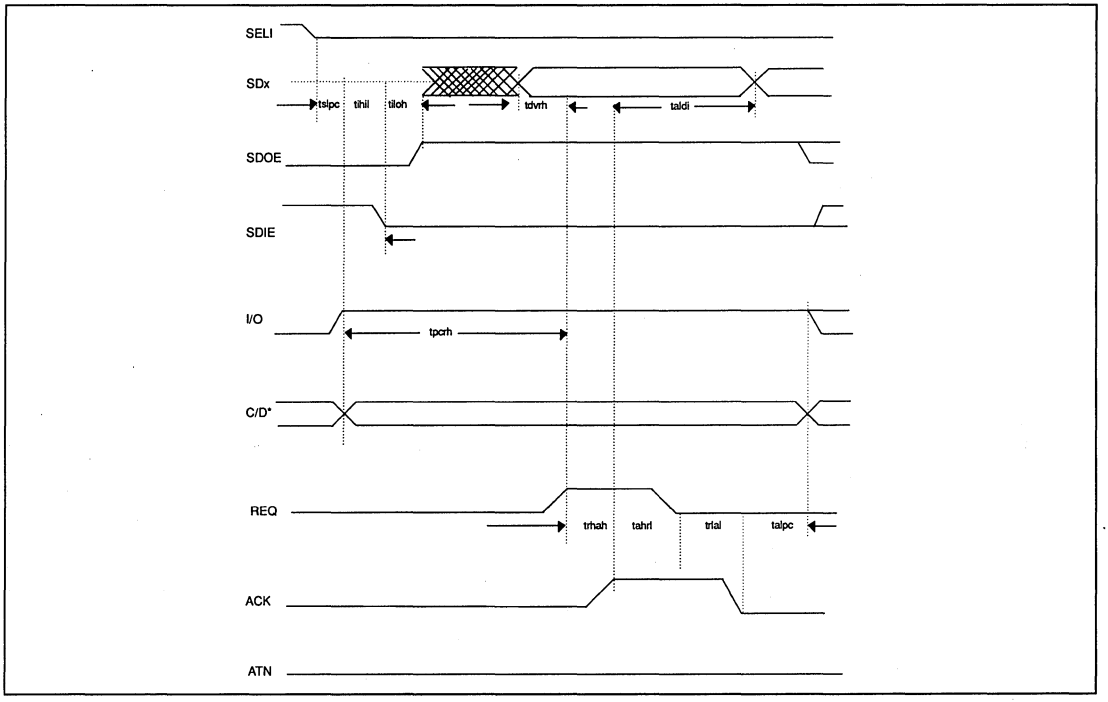

FIGURE 9-20. ASYNCHRONOUS INFORMATION TRANSFER IN(T)TIMING

9.2.8 Asynchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tilil	I/O IN LOW TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tdvah	DATA OUT VALID TO ACK OUT HIGH	80		ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
trldi	REQ IN LOW TO DATA OUT INVALID	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

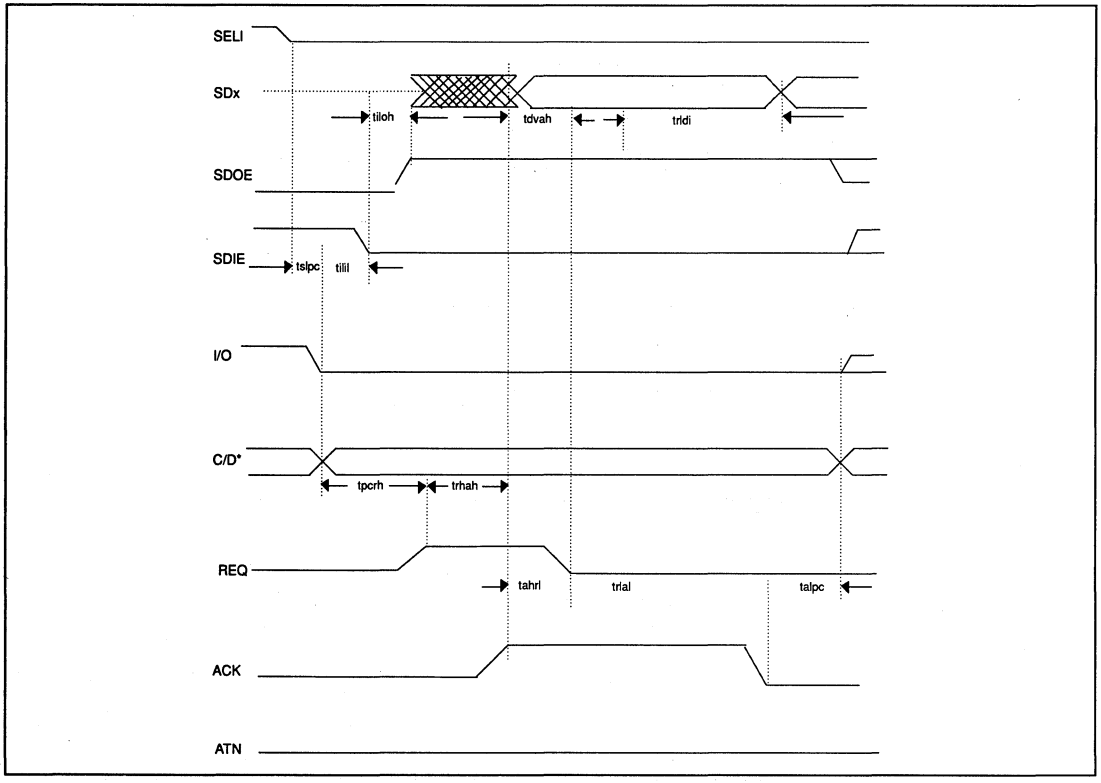

FIGURE 9-21.ASYNCHRONOUS INFORMATION TRANSFER OUT(I)TIMING

9.2.9 Asynchonous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tilol	I/O OUT LOW TO SDOE LOW DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tdvah	DATA IN VALID TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
trldi	REQ OUT LOW TO DATA IN INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

22

NOTE:
C/D* = C/D, MSG

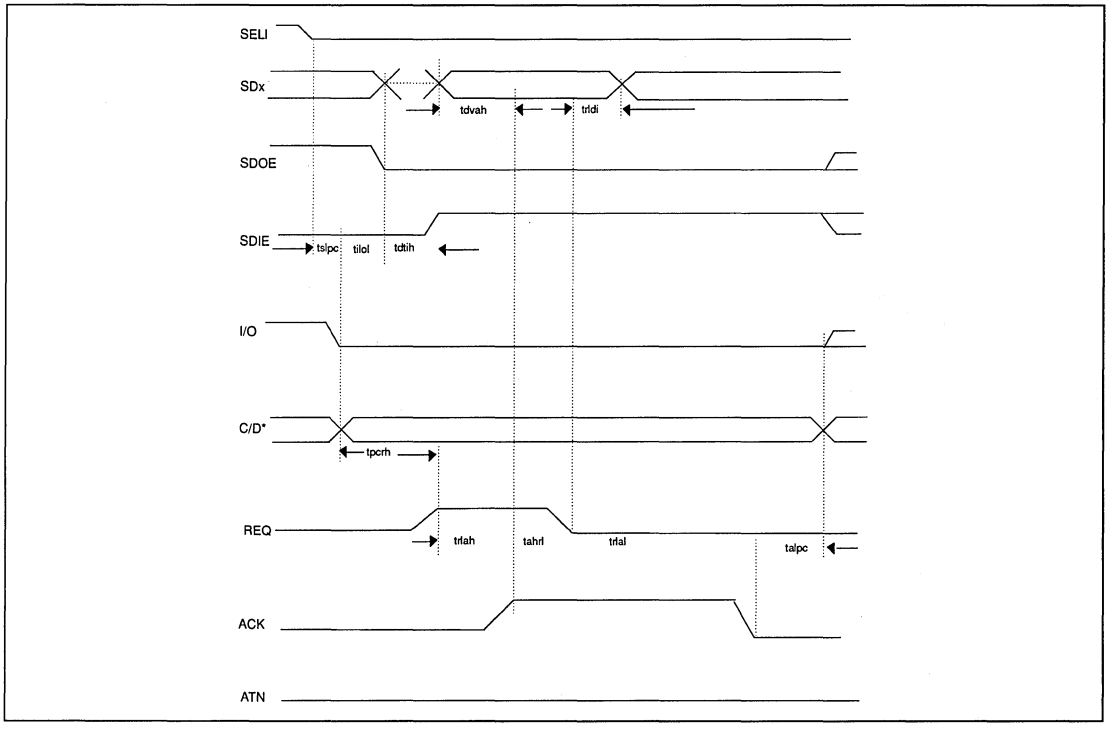

FIGURE 9-22. ASYNCHRONOUS INFORMATION TRANSFER OUT (T)

9.2.10 Synchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhdi	REQ IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tihol, tdtih, and tpcrh ALSO APPLY (see 9.2.6).

NOTE:
C/D* = C/D, MSG

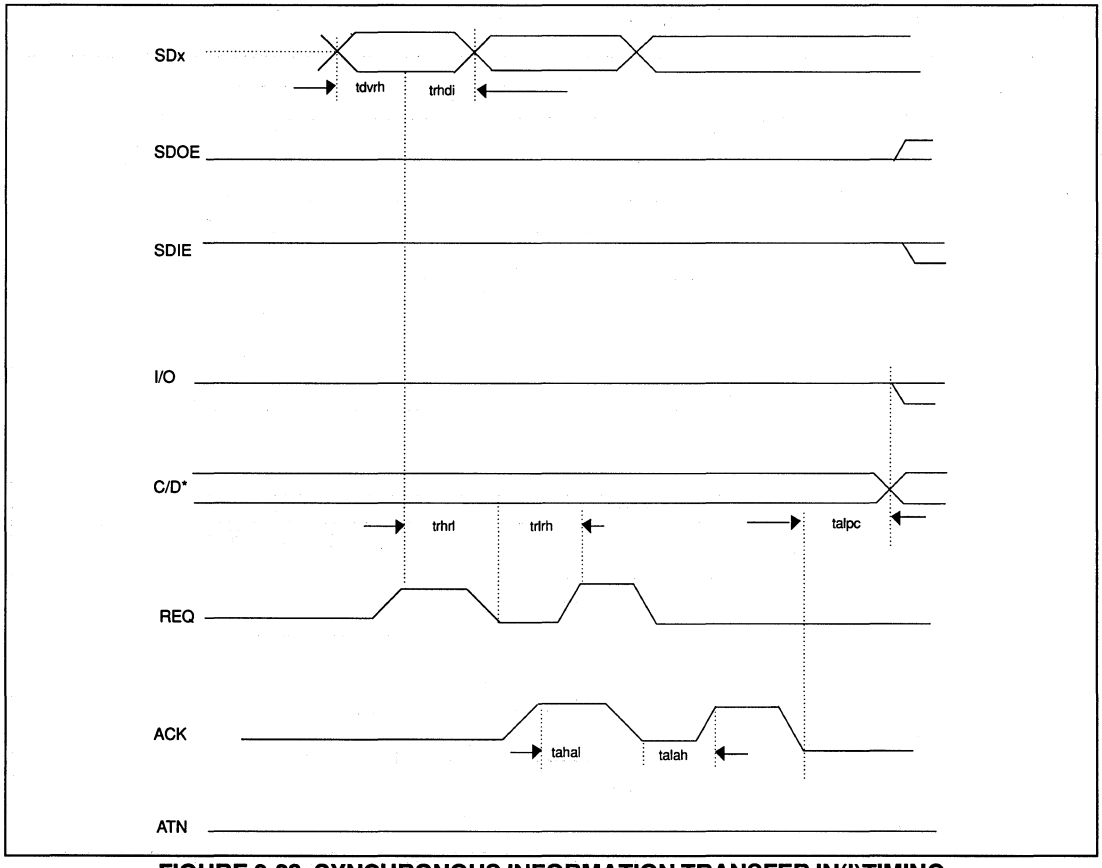

FIGURE 9-23. SYNCHRONOUS INFORMATION TRANSFER IN(I)TIMING

9.2.11 Synchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID OUT TO REQ OUT HIGH	75		ns
trhdi	REQ OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tihil, tiloh, and tpcrh ALSO APPLY (see 9.2.7).

NOTE:
C/D* = C/D, MSG

22

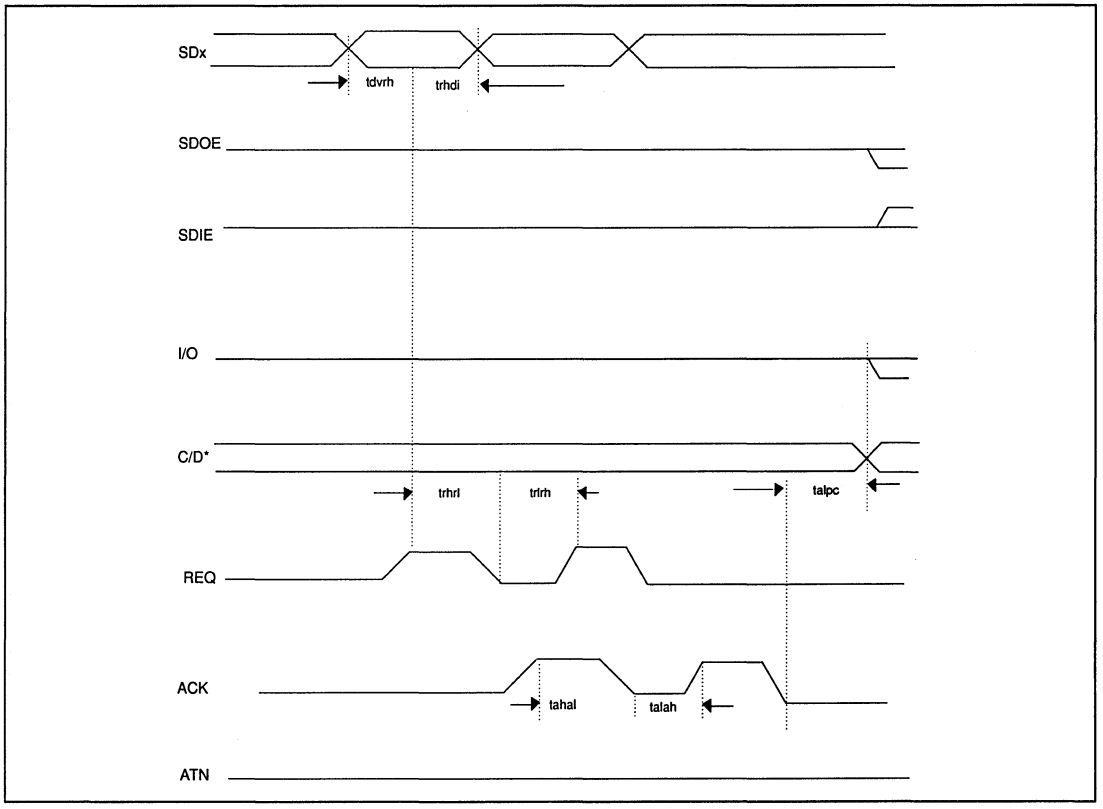

FIGURE 9-24. SYNCHRONOUS INFORMATION TRANSFER IN(T)TIMING

9.2.12 Synchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID OUT TO ACK OUT HIGH	75		ns
tahdi	ACK OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tiloh, tilil, and tpcrh ALSO APPLY (see 9.2.8).

NOTE:
C/D* = C/D, MSG

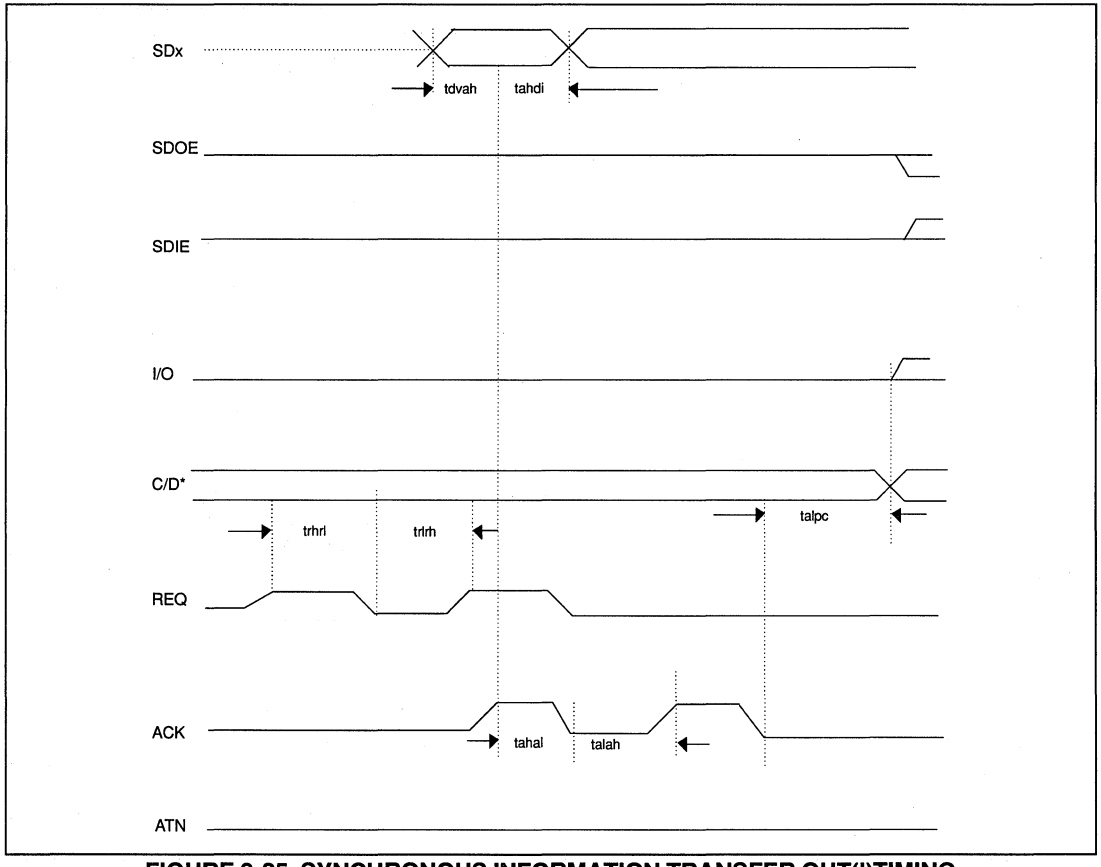

FIGURE 9-25. SYNCHRONOUS INFORMATION TRANSFER OUT(I)TIMING

9.2.13 Synchronous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID IN TO ACK IN HIGH	0		ns
tahdi	ACK IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tilol, tdtih, and tpcrh ALSO APPLY (see 9.2.9).

NOTE:
C/D* = C/D, MSG

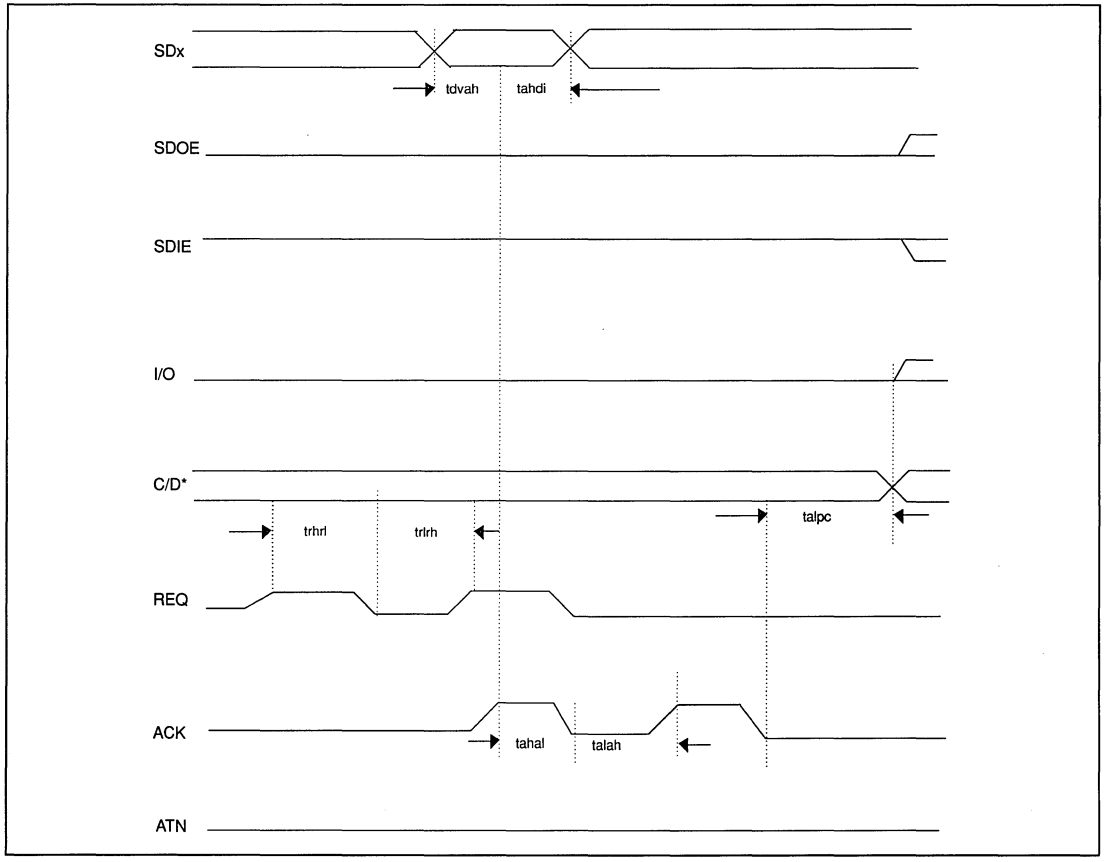

FIGURE 9-26. SYNCHRONOUS INFORMATION TRANSFER OUT(T)TIMING

9.2.14 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYO, SDOE, ARBLD LOW		8+120ns|	Tcyc

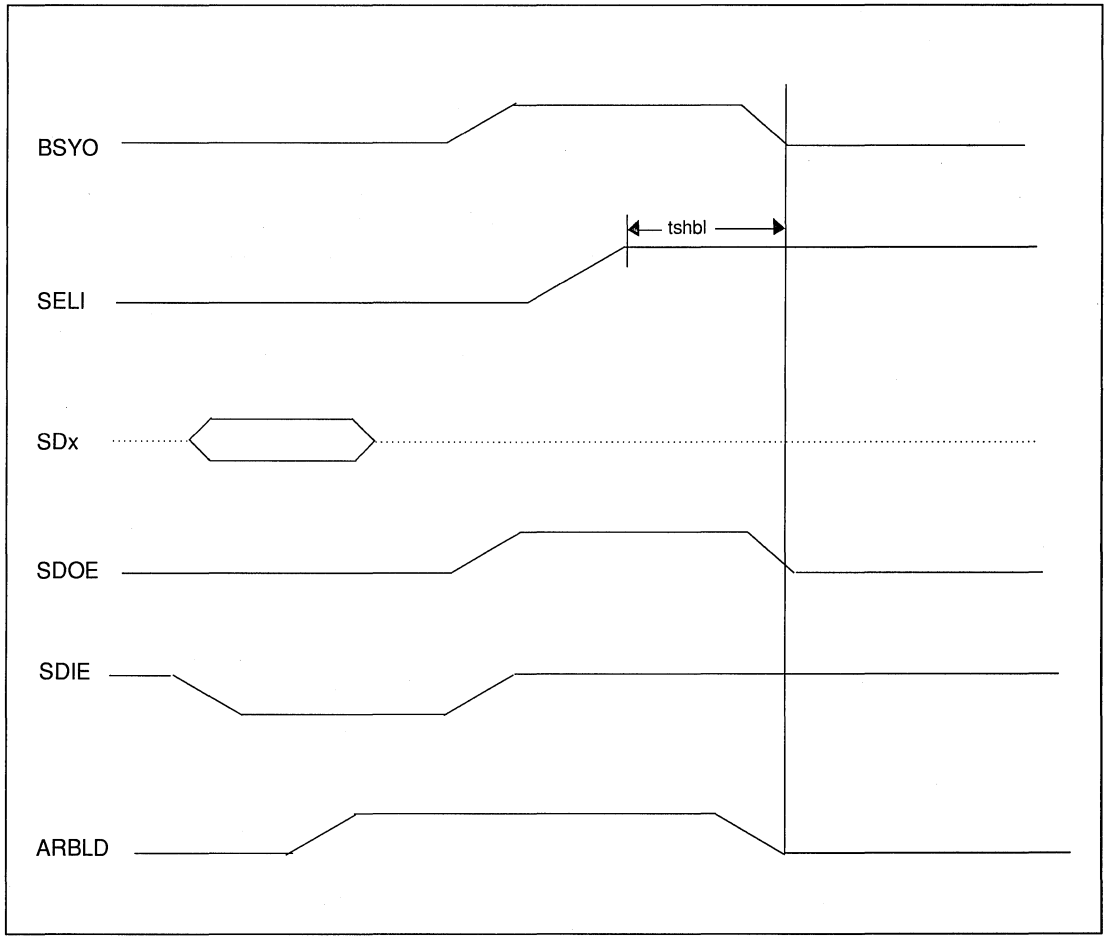

FIGURE 9-27. ARBITRATION TO BUS FREE TIMING

9.2.15 Selection (Initiator) Or Reselection (Target) To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	TIMEOUT OR ABORT TO DATA BUS CLEARED*	0		ns
tdcsl	DATA BUS CLEARED* TO SELO LOW	200		µs
tslih	SELO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tsldt	SELO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tslgl	SELO LOW TO gs LOW, cntl TRISTATE		8+120ns	Tcyc

* SDx logic low, causing logic low on SCSI data bus.

NOTE:
gs = IGS (INITIATOR) or TGS (TARGET)
cntl = ATN, ACK (INIT) or I/O, C/D, MSG, and REQ (TARGET)

22

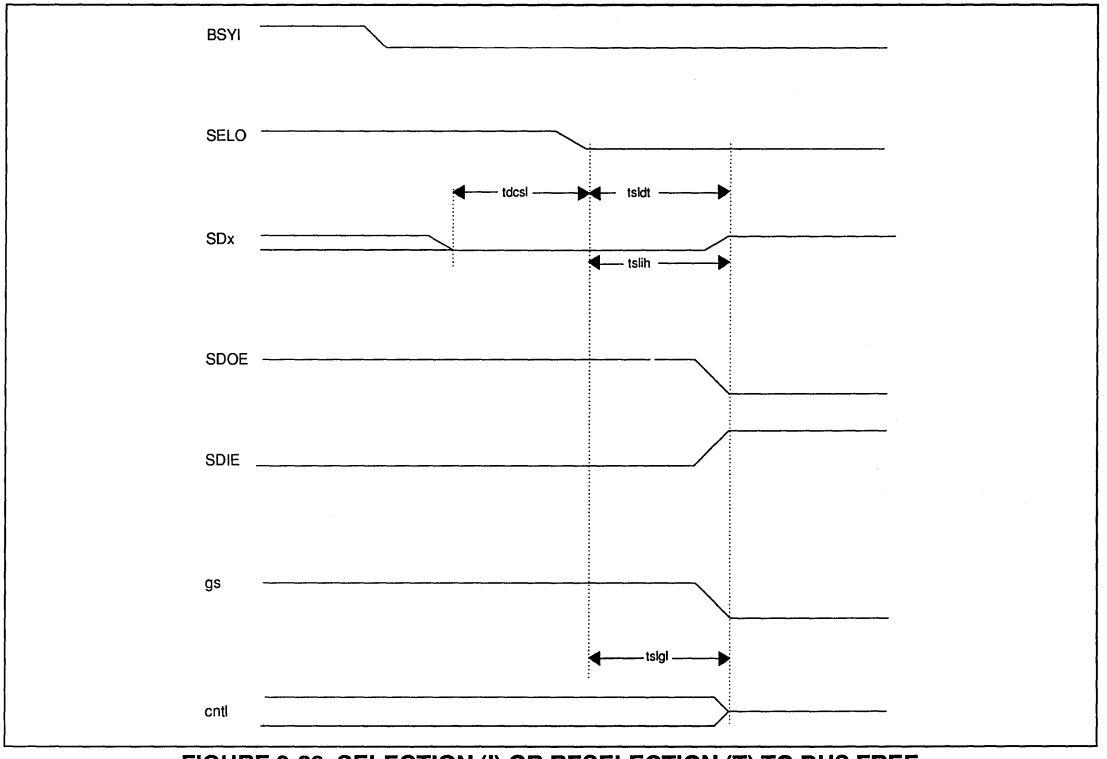

FIGURE 9-28. SELECTION (I) OR RESELECTION (T) TO BUS FREE

9.2.16 Connected-as-an-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYI LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYI LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYI LOW TO IGS LOW, ATN TRISTATE		8+120ns	Tcyc

NOTE:
ATN* = ATN, ACK

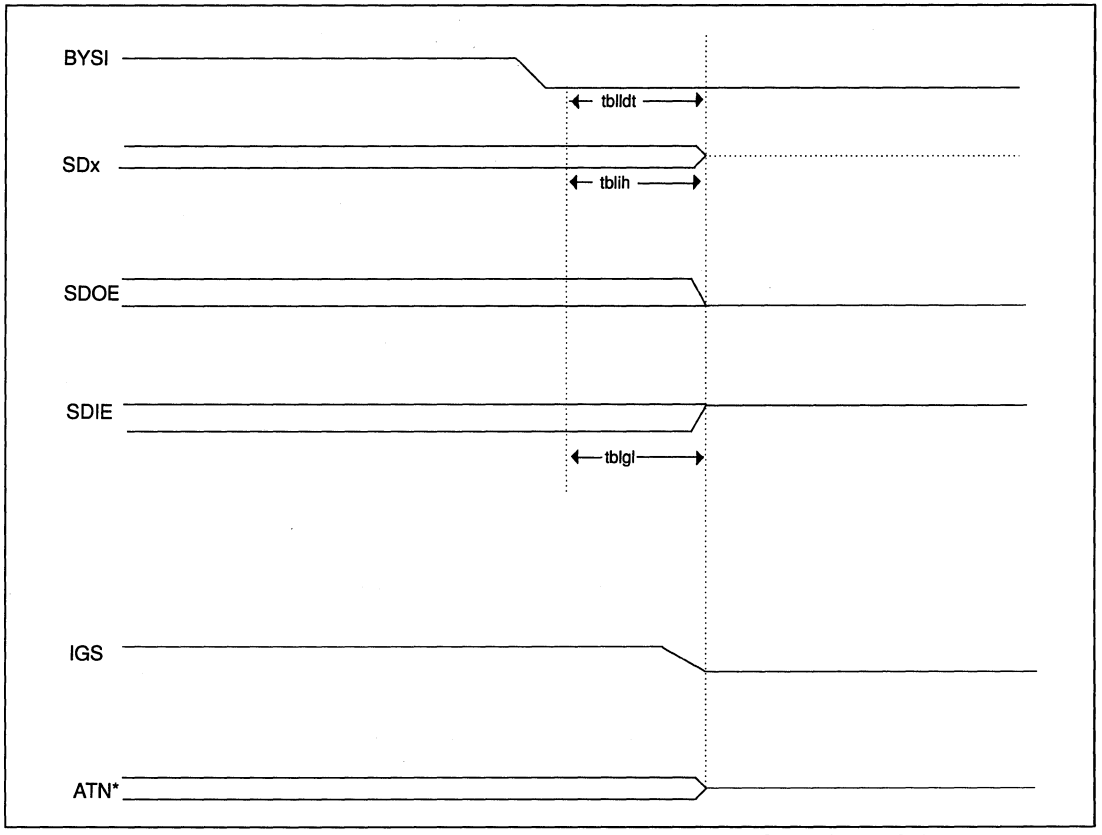

FIGURE 9-29. CONNECTED-AS AN-INITIATOR TO BUS FREE TIMING

9.2.17 Connected-as-a-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYO LOW TO TGS LOW, I/O TRISTATE		8+120ns	Tcyc

NOTE:
I/O* = I/O, C/D, MSG, REQ

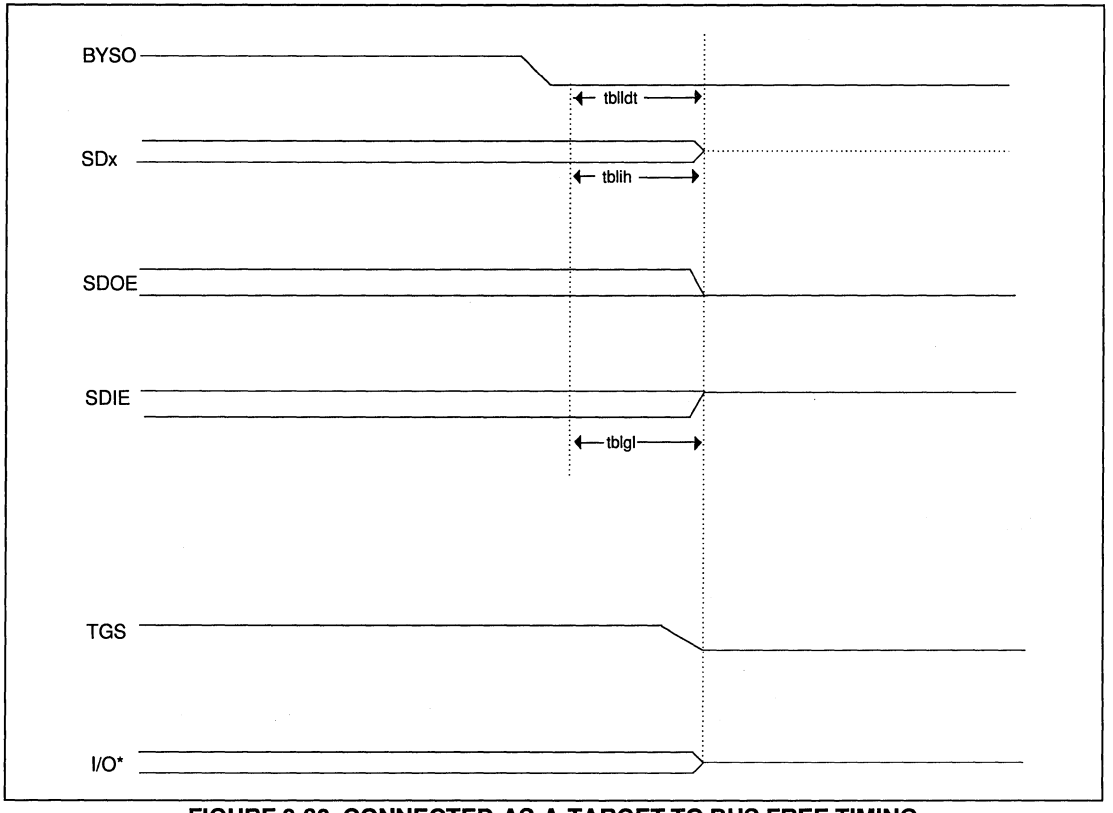

FIGURE 9-30. CONNECTED-AS-A-TARGET TO BUS FREE TIMING

WD33C93B

Enhanced SCSI Bus Interface Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DESCRIPTION

The 33C93B, a MOS/VLSI device implemented in Western Digital's CMOS process, operates from a single 5 Volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL compatible.

The 33C93B is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The 33C93B can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C93B interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor issues a command to the 33C93B to select the desired target. The 33C93B then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the host when it has succeeded by generating an interrupt. At this point, the 33C93B is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C93B receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C93B. The 33C93B transfers the SCSI command to the peripheral and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C93B also offers high-level Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the 33C93B is used in a peripheral system, the 33C93B operates primarily in a target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used in a host adapter. The target-role command set enables the 33C93B to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C93B has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

1.2 FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation and checking on both data ports, soft reset, and synchronous data transfers.
- Includes 48 mA drivers for direct connection to the SCSI bus.
- Operates in both initiator and target roles.
- Synchronous offset selectable from one to twelve bytes.
- Programmable timeout for selection and reselection.
- Support for SCSI-2 features:
  - Synchronous transfer rates up to 10 Mbytes/s for Fast SCSI transfers; up to 5 Mbyte/s for standard SCSI transfers.
  - Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands provide support for queue tag messages and target routine identify messages.
- Special "Translate Address" command performs the Logical-to-Physical address mapping.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Burst data transfers up to 4096 bytes.
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Single +5 V supply.
- Available in 44-pin chip carrier or 40-pin DIP.
- Low-power CMOS design.

1.3 DIFFERENCES BETWEEN THE 33C93A AND 33C93B

The 33C93B delivers the same functionality as the 33C93A as well as additional features to support SCSI-2 and improve system performance. Unless the device is configured with the RAF bit in the OWN ID register set, the 33C93B is completely backward compatible to the 33C93A; consequently, in most applications, it may replace the 33C93A with no modification to the hardware or the firmware.

The 33C93B has grouped several recently added features of the 33C93A with two 33C93B-only enhancements into a mode enabled by configuring the device with the RAF bit set. Section 4.3.2 describes this new mode. The first two features---the loading of the microcode revision on a soft reset condition and the aborting of a target Receive command upon the detection of the SCSI Attention condition or of a parity error---existed in the 33C93A design. The 33C93B design has added to this mode the ability to detect possible data corruption and unexpected disconnects from the SCSI bus when operating as a target.

To support SCSI-2, the combination commands Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive optionally send or receive Queue-tag messages at appropriate points in the SCSI bus sequence. The host via two bits in the DESTINATION ID register and the newly added QUEUE TAG register provides information which the first two commands use to generate and check these messages. Wait-for-Select-and-Receive, through the same locations, relays information to the host regarding the type of Queue-tag message received, including whether the initiator sent a message or not, and the actual queue tag.

These commands also support the LUNTAR bit in the Identify message. By setting the corresponding bit in the TARGET LUN register, the host enables the Select-and-Transfer and Reselect-and-Transfer commands to send an Identify message for a target routine. In the case of Select-and-Transfer, setting this bit also enables the 33C93B to accept automatically an Identify message with the LUNTAR bit set. The host also has the option to let the Wait-for-Select-and-Receive command receive a target routine Identify message and proceed to the next phase or to interrupt the host so that it may reject the message when the application does not support target routines.

The last new feature pertaining to SCSI-2 relates to Fast SCSI. When the 33C93B has an input clock between 16 MHz and 20 MHz, by controlling the Fast SCSI Select (FSS) bit in the SYNCHRONOUS TRANSFER register, the host can select between normal synchronous transfers which reach a maximum transfer rate of 5 MB/s and Fast synchronous transfers with a peak rate of 10 MB/s on both the SCSI and host DMA interfaces.

The final addition to the 33C93B is the FIFO Full/Empty (FFE) bit in the AUXILIARY STATUS register to be used primarily during polled I/O transfers. As its name suggests, this bit reflects the full or empty state of the FIFO depending on the direction of the transfer. If the host is writing data to the FIFO, the 33C93B sets this bit when the FIFO is empty, indicating that the host may write up to twelve bytes to the FIFO without having to poll the DBR bit before writing each byte. Similarly, when the host is reading data from the FIFO, the 33C93B sets this bit when the FIFO is full, indicating that the host may read the DATA register twelve times without polling DBR before each read. Some restrictions do apply when using this bit, and they are described in Section 3.1.22.

2.0 PIN DESCRIPTIONS

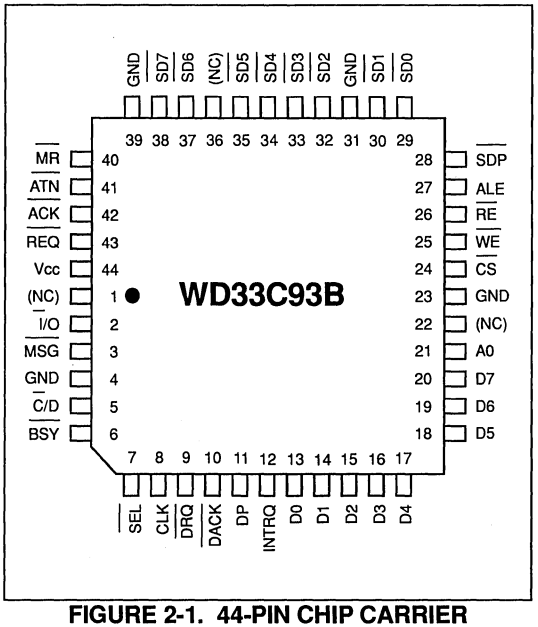

FIGURE 2-1. 44-PIN CHIP CARRIER

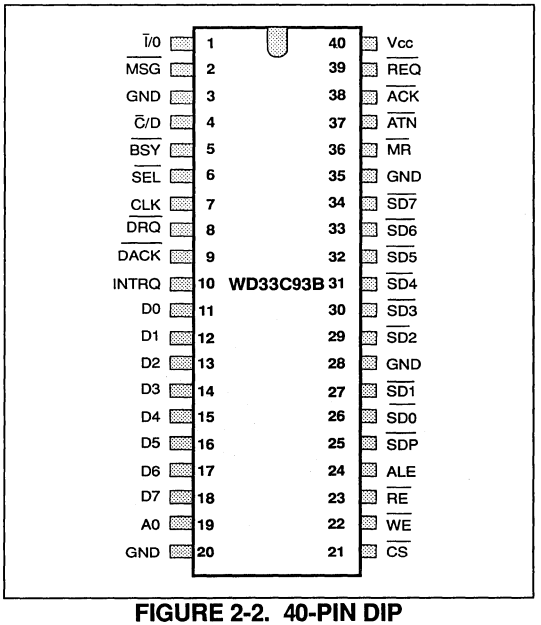

FIGURE 2-2. 40-PIN DIP

2.1 PROCESSOR/DMA INTERFACE

NAME	I/O	DESCRIPTION
CLK	I	8-20 MHz square wave clock
MR	I	Reset is an active-low input which forces the 33C93B into an idle state and forces all SCSI signals to the negated state.
INTRQ	O	Interrupt Request to the external microprocessor indicates a command completion/termination or a need to service the SCSI interface. Reading the SCSI STATUS register clears this bit.
RE	I/O	Read Enable is an active-low input used with CS- to read a register or with DACK- to access the DATA register in DMA mode. In WD Bus mode, it is used as an output to read data from a sector buffer. (TRI-STATE).
WE-	I/O	Write Enable is an active-low input used with CS- to write a register or with DACK- to access the DATA register in DMA mode. In WD Bus mode, it is used as an output to write data to a sector buffer. (TRI-STATE)
CS	I	Chip Select is an active-low input which qualified RE- and WE- when acces-sign a register. This signal must be inactive during a DMA cycle (DACK- active in DMA and Burst DMA mode or DRQ active in WD Bus mode).
A0	I	Address Pin A0 is used to access the internal registers for non-multiplexed address/data busses (i.e.; the ALE pin is grounded). The address of the desired register is loaded into the address register during a write cycle with A0=0. The selected register is then accessed when A0=1.

TABLE 2-1. SIGNAL DESCRIPTIONS

NAME	I/O	DESCRIPTION
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C93B register from the data bus. For indirect addressing, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
$\overline{\text{DACK}}$ ($\overline{\text{RCS}}$)	I/O	DMA Acknowledge is an active-low input used for interfacing to an external DMA controller (e.g. 8237). When $\overline{\text{DACK}}$ is low, all bus transfers are to or from the DATA register regardless of the contents of the ADDRESS register. In WD Bus mode this pin, an open-drain output, functions as a RAM Chip Select to the sector buffer. $\overline{\text{RE}}$ and $\overline{\text{WE}}$ are outputs when $\overline{\text{RCS}}$ is active. Regardless of the host DMA mode selected, this pin should be pulled via external circuitry (e.g. a pullup resistor) to an inactive state and should not be left floating.
$\overline{\text{DRQ}}$	I/O	Data Request is an active-low output when used for interfacing to an external DMA controller and an active-high input when in WD Bus mode. In the first application, $\overline{\text{DRQ}}$ and $\overline{\text{DACK}}$ form the handshake for the DMA data transfers. In Burst mode, $\overline{\text{DRQ}}$ remains low so long as there is data to transfer; in Single-byte DMA mode, $\overline{\text{DRQ}}$ toggles for each byte. Since this pin is an open drain output, a pullup resistor may be required when operating in these modes. In WD Bus mode, this pin becomes the DRQ input. A high level on this pin enables the 33C93B to perform burst transfers; a low level inhibits transfers by deasserting $\overline{\text{RCS}}$ and disabling the $\overline{\text{RE}}$ and $\overline{\text{WE}}$ outputs.
D7 - D0	I/O	Processor data bus.
DP	I/O	Data Parity is used only for checking and generating parity during data transfers.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

2.2 SCSI INTERFACE

NAME	I/O	DESCRIPTION
$\overline{ATN}$	I/O	$\overline{ATN}$ is an output in the initiator role and an input in the target role. Its assertion indicates the ATTENTION condition.
$\overline{REQ}$	I/O	$\overline{REQ}$ is an input in the initiator role and an output in the target role. It indicates a request for a data transfer.
$\overline{ACK}$	I/O	$\overline{ACK}$ is an output in the initiator role and an input in the target role. It indicates an acknowledgement of a data transfer.
$\overline{MSG}$	I/O	$\overline{MSG}$ is an input in the initiator role and an output in the target role. The target asserts this signal when requesting message information.
$\overline{C/D}$	I/O	$\overline{C/D}$ is an input in the initiator role and an output in the target role. It specifies whether CONTROL or DATA information is on the SCSI data bus.
$\overline{I/O}$	I/O	$\overline{I/O}$ is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an initiator.
$\overline{SD7}$	I/O	SCSI data bus.
$\overline{SD0}$	I/O	SCSI data bus.
$\overline{SDP}$	I/O	SCSI data bus parity signal.
$\overline{BSY}$	I/O	$\overline{BSY}$ is asserted when the 33C93B is attempting to arbitrate for the SCSI bus or when connected as a target.
$\overline{SEL}$	I/O	$\overline{SEL}$ is asserted when the 33C93B is attempting to select or reselect another SCSI device.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)

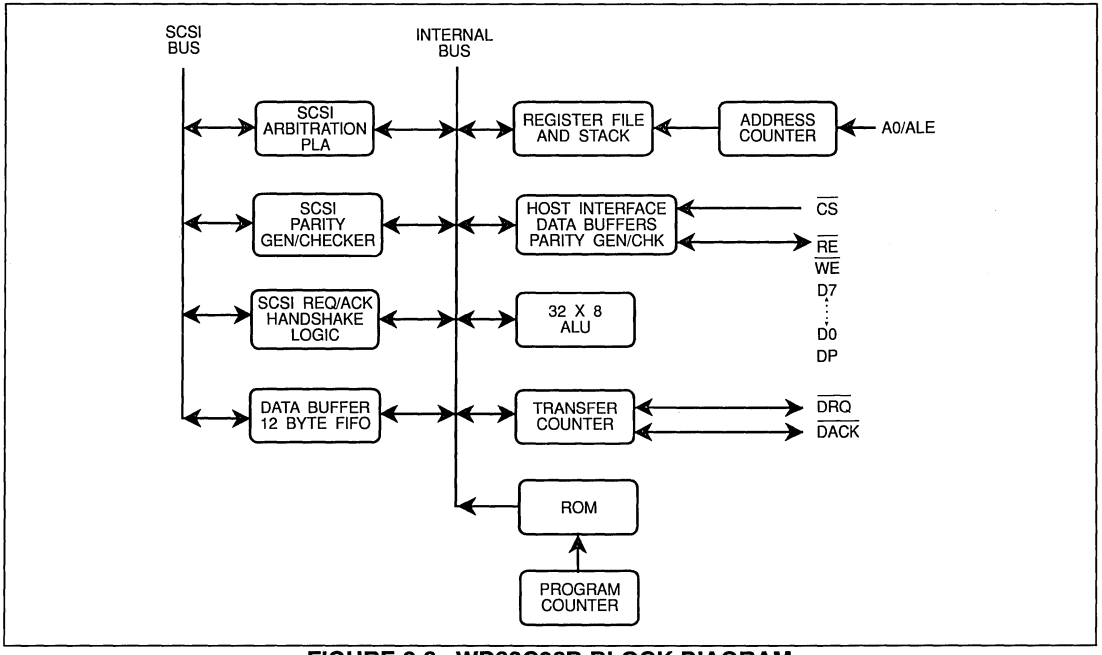

FIGURE 2-3. WD33C93B BLOCK DIAGRAM

3.0 WD33C93B REGISTERS

A0	R/W	REGISTER ACCESSED		ADDRESS (HEX)
0	R	Auxiliary Status Register		XX
0	W	Address Register		XX
1	R/W	Own ID Register	/CDB Size	00
1	R/W	Control Register		01
1	R/W	Timeout Period Register		02
1	R/W	Total Sectors Register	/CDB 1st	03
1	R/W	Total Heads Register	/CDB 2nd	04
1	R/W	Total Cylinders Register (MSB)	/CDB 3rd	05
1	R/W	Total Cylinders Register (LSB)	/CDB 4th	06
1	R/W	Logical Address (MSB)	/CDB 5th	07
1	R/W	Logical Address (2nd)	/CDB 6th	08
1	R/W	Logical Address (3rd)	/CDB 7th	09
1	R/W	Logical Address (LSB)	/CDB 8th	0A
1	R/W	Sector Number Register	/CDB 9th	0B
1	R/W	Head Number Register	/CDB 10th	0C
1	R/W	Cylinder Number (MSB) Register	/CDB 11th	0D
1	R/W	Cylinder Number (MSB) Register	/CDB 12th	0E
1	R/W	Target LUN Register		0F
1	R/W	Command Phase Register		10
1	R/W	Synchronous Transfer Register		11
1	R/W	Transfer Count Register (MSB)		12
1	R/W	Transfer Count Register (2nd Byte)		13
1	R/W	Transfer Count Register (LSB)		14
1	R/W	Destination ID Register		15
1	R/W	Source ID Register		16
1	R	SCSI Status Register		17
1	R/W	Command Register		18
1	R/W	Data Register		19
1	R/W	Queue Tag Register		1A

NOTE:
1. All unused bits of a defined register are reserved and must be zero.
2. Reading an undefined or unavailable register results in an all-ones data bus output.
3. Register addresses are determined by the ADDRESS register bits AR7 through AR0.
4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored, and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at 1F hex.
5. See section 3.2 for a description of how reset affects the internal registers.

TABLE 3-1. REGISTER MAP

3.1 REGISTER DESCRIPTIONS

3.1.1 Auxiliary Status Register

The AUXILIARY STATUS register, a read-only register, contains general status information not directly associated with the interrupt condition. The host may access the AUXILIARY STATUS register at any time except during DMA accesses. (DACK asserted in DMA/Burst mode or RCS asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	O	FFE	PE	DBR

Bit 0 DBR-DATA BUFFER READY
DATA BUFFER READY indicates to the processor whether or not the DATA register is available for reading or writing. During a Send command or a Transfer Info command which transmits data over the SCSI bus, the 33C93B sets this bit when ready to take a byte from the host; it resets this bit when the processor writes the byte to the DATA register. During a Receive command or a Transfer Info command which receives data over the SCSI bus, the 33C93B sets DBR when it receives a byte and resets DBR when the processor reads the byte from the DATA register.

Bit 1 PE-PARITY ERROR
PARITY ERROR status indicates that the 33C93B received a byte with even parity during a transfer. SCSI parity checking is always enabled; host parity checking is enabled via the EHP bit in the OWN ID register Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTRO register. Issuing a command clears the PE bit.

Bit 2 FFE -FIFO FULL/EMPTY
FIFO FULL/EMPTY indicates when the FIFO is full or empty depending on the direction of the transfer. (see 3.1.22)

Bit 4 CIP -COMMAND IN PROGRESS
COMMAND IN PROGRESS indicates that the 33C93B is interpreting the last command entered into the COMMAND register which is therefore unavailable.

Bit 5 BSY-BUSY
BUSY indicates that a Level II command is currently executing, so the host may only access the COMMAND register (when CIP = 0),the DATA register, and the AUXILIARY STATUS register. When this bit is set, the host should not issue a Level II command.

Bit 6 LCI -LAST COMMAND IGNORED
LAST COMMAND IGNORED indicates that the 33C93B ignored a command because the host issued it just prior to or concurrent with a pending interrupt.

Bit 7 INT-INTERRUPT PENDING
INTERRUPT PENDING reflects the state of the INTRQ pin. When set, the host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

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3.1.2 Address Register

The ADDRESS register, a write-only register, holds the address of the register to be accessed. Registers in the 33C93B may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In this mode, the falling edge of the ALE signal latches the contents of the host data bus into the ADDRESS register. The CS and WE or RE signals typically follow to access the selected register. When using direct addressing, the A0 pin should be connected to ground, and the AUXILIARY STATUS register is located at address 1F hex.
- Indirect addressing (separate address/data busses). This method, enabled by tying ALE to ground, requires two separate cycles for a register access. The first cycle loads the desired address into the ADDRESS register by writing (CS and WE asserted) to the 33C93B with A0=0.The second cycle, with A0=1, then reads (CS and RE asserted) or writes (CS and WE asserted) the selected register. Every cycle with A0=1 increments the ADDRESS register except when accessing the DATA or COMMAND registers. In indirect addressing, the AUXILIARY STATUS

register is accessed by performing a read ($\overline{CS}$ and $\overline{RE}$ asserted) with A0=0.

3.1.3 Own ID/CDB Size Register

The OWN ID/CDB SIZE register, in its first mode, contains information which the Soft Reset command uses to configure the device. Following a hardware reset, the host, before issuing any other command, must initialize this register and issue the Reset command to set the clock divisor and the SCSI bus ID of the device and to enable various sets of features and host bus parity checking.

In the second mode, bits 3-0 of this register specify the SCSI CDB size if the command group is unknown (i.e. not a group 0, group 1, or group 5 SCSI command) to the 33C93B during the Select-and-Transfer and Wait-for-Select commands. This mode is enabled only when advanced features (see 4.3.1) have been selected.

7	6	5	4	3	2	1	0
FS1	FS0	RAF	EHP	EAF	ID2	ID1	ID0

Bit 0-2 IDn- SCSI ID BITS
SCSI ID Bits 0-2 set the SCSI bus ID that the 33C93B uses during arbitration and selection.

Bit 3 EAF-ENABLE ADVANCED FEATURES
ENABLE ADVANCED FEATURES, when set, enables functions described in section 4.3.1.

Bit 4 EHP-ENABLE HOST PARITY
ENABLE HOST PARITY enables odd parity checking on the host bus. The PE bit in the AUXILIARY STATUS register will then also indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will have effect during transfers. When host parity is disabled, the PE bit is not set when a parity error occurs on the host bus,and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 RAF-REALLY ADVANCED FEATURES
REALLY ADVANCED FEATURES, when set, enables features described in section 4.3.2.

Bit 6-7 FSn-FREQUENCY SELECT
FREQUENCY SELECT 0-1 select the divisor that is applied to the input clock. The divided clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and their corresponding divisors. An incorrect divisor for the input clock may result in violation of SCSI bus timing specifications.

INPUT CLOCK FREQUENCY (MHz)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
XX	1	1	Undefined

Note that a clock rate between 10 MHz and 12 MHz should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is given in Section 6.

3.1.4 Control Register

The CONTROL register consists of option bits which affect response to parity errors and to the SCSI attention condition, suppress interrupts, allow command chaining, and select the mode of DMA transfer.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR
The HALT on SCSI PARITY ERROR bit enables the 33C93B to terminate a Receive or Transfer Info command if a parity error occurs on an incoming SCSI data byte. Asynchronous transfers check parity on every byte; synchronous data transfers check parity on 4096-byte boundaries in most cases. In the initiator role, the 33C93B responds to a SCSI parity

error by leaving the $\overline{ACK}$ pin asserted to inhibit any additional data transfers (REQs) by the target and to facilitate error handling with the target. If Immediate Halts are enabled, a SCSI parity error during a synchronous Receive or Reselect-and-Receive command will abort the transfer before the 4096-byte boundary.

Bit 1 HA-HALT on ATTENTION
The HALT on ATTENTION bit (target mode only) enables the 33C93B to terminate a Send or Receive command if the initiator asserts $\overline{ATN}$. The 33C93B normally tests for the $\overline{ATN}$ condition before the start of a data transfer, on 4096 byte boundaries, and after the end of the transfer. If the Immediate Halt feature is enabled, an Abort command will be issued upon recognition of the $\overline{ATN}$ condition. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT
The INTERMEDIATE DISCONNECT INTERRUPT bit, when set in the initiator role, causes the 33C93B to terminate a Select-and-Transfer command and generate an 85 hex interrupt upon a proper target disconnect. When this bit is reset, a valid disconnect will not cause the 33C93B to generate an interrupt, and command execution proceeds. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. In the target role, the IDI bit selects combination command execution options. Refer to Section 4 for more details.

Bit 3 EDI-ENDING DISCONNECT INTERRUPT
The ENDING DISCONNECT INTERRUPT bit, when set, delays the 16 hex interrupt which normally follows receipt of the Command-Complete message during a Select-and-Transfer command until after the target disconnects, replacing the 85 hex interrupt. This bit also enables chaining between certain target-role combination commands to reduce host system overhead. Refer to Section 4 for more details.

Bit 4 HHP-HALT on HOST PARITY ERROR
The HALT on HOST PARITY ERROR bit allows the 33C93B to terminate a Send or Transfer command if a parity error occurs on an incoming host data byte. The 33C93B checks for host parity errors according to the sames rules it uses when checking for SCSI parity errors. However, a host parity error will not leave the $\overline{ACK}$ signal asserted.

Bit 5-7 DMx-DMA MODE SELECT
The DMA MODE SELECT bits 2-0 select the host bus transfer mode to be used during a Data phase. The following table describes the different DMA modes and specifies the state of these bits to select each mode:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	POLLED I/O MODE or no DMA enabled. The host must poll for DBR in the AUXILIARY STATUS register and then, depending on the direction of the transfer, read or write the DATA register.
0	0	1	BURST MODE or demand-mode DMA. In this mode, the $\overline{DRQ}$ signal will remain active so long as data or space exists in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting $\overline{DACK}$ and pulsing $\overline{RE}$ or $\overline{WE}$ to transfer the data.
0	1	0	WD-BUS MODE or Direct Buffer Access (DBA) mode. In this mode, the 33C93B acts as a bus master, and all data access signals reverse their directions. The $\overline{DRQ}$ pin becomes the DRQ input, which when high, enables the 33C93B to drive the buffer control signals. The $\overline{DACK}$ pin becomes the $\overline{RCS}$ output and serves as a chip select for the buffer. The $\overline{RE}$ and $\overline{WE}$ pins become outputs which drive the read and write functions of the RAM buffer. Transfers will continue in a burst manner until the transfer is complete or until the external buffer logic pauses the transfer by negating the DRQ signal. One transfer may occur after DRQ drops and then the $\overline{DACK}$, $\overline{RE}$, and $\overline{WE}$ signals will tristate.
1	0	0	DMA MODE or Single-byte DMA. In this mode,a $\overline{DRQ}$/$\overline{DACK}$ handshake occurs for each byte.The DMA controller transfers the byte by asserting $\overline{WE}$ or $\overline{RE}$ while asserting $\overline{DACK}$.

3.1.5 Timeout Period Register

The TIMEOUT PERIOD register stores a user-selected, 8-bit value which determines the timeout period for selection and reselection attempts. The timeout period specifies how long the 33C93B will wait for a response (i.e. assertion of the BSY signal) after it has begun the Selection phase (asserted $\overline{SEL}$ and negated $\overline{BSY}$) before terminating the command. Loading this register with zero disables the timeout feature. For a desired timeout period, the register value depends upon the input clock frequency, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} * \text{Ficlk}}{80}$$

where Tper = the desired timeout period in milliseconds; Ficlk = the input clock frequency at the MCK pin in megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as it is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the minimum timeout requirement is met.

3.1.6 Command Descriptor Block Registers

The COMMAND DESCRIPTOR BLOCK registers hold the SCSI command bytes to be sent during Command phase of a Select-and-Transfer command and the command bytes received during the Command phase of a Wait-for-Select-and-Receive command.

The Send-Status-and-Command-Complete command uses the contents of the CDB11 register as the returned status and determines the type of the Command-Complete message to send from the contents of the CDB12 register. Bit 0 of CDB12 selects whether the command sends a simple Command-Complete message bit 0=0) or a Linked-Command-Complete message (bit 0=1). In the latter case, bit 1 of CDB12, the FLAG bit,

specifies whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) message is sent.

3.1.7 Total Sectors Register

The TOTAL SECTORS register stores an 8-bit value specifying the total number of sectors per track for the Translate Address command.

3.1.8 Total Heads Register

The TOTAL HEADS register stores an 8-bit value specifying the total number of heads for the Translate Address command.

3.1.9 Total Cylinders Register

The TOTAL CYLINDERS register stores a 16-bit value specifying the total number of cylinders for the Translate Address command.

3.1.10 Logical Address Register

The LOGICAL ADDRESS register stores the 32-bit logical address to be translated by the Translate Address command.

3.1.11 Sector Number Register

The SECTOR NUMBER register will contain the resulting physical sector number following a Translate Address command.

3.1.12 Head Number Register

The HEAD NUMBER register contains the resulting head number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, this register should contain the number of spare sectors per cylinder prior to issuing the Translate Address command. A value of zero indicates no compensation. With compensation, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15.

3.1.13 Cylinder Number Register

The CYLINDER NUMBER register contains a 16-bit value specifying the resulting cylinder number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, the Translate Address command expects this register to contain the number of sectors per cylinder after allowing for the spares, i.e. (sectors/track * heads - spares/cylinders).

3.1.14 Target LUN Register

The TARGET LUN register holds the Logical Unit Number (LUN) and other target status information during various 33C93B commands and sequences.

The Select-and-Transfer commands use the contents of this register and the SOURCE ID register to generate and check Identify messages. In addition, these commands also store the returned status byte from the target in this register. For proper operation of the Select-and-Transfer commands, the host should not set the TLV bit in this register.

In advanced mode, the Select-and-Transfer commands, in the event of an unexpected reselection, place the logical unit number (TRN=0) or the target routine number (TRN=1) of a reselecting target in this register. The TLV and DOK bits will be zero.

The Wait-for-Select-and-Receive command places a copy of a received Identify message in this register. If the TLV bit is zero, the initiator did not send a valid Identify message. If the TLV bit is one, the initiator sent a valid Identify message, and the DOK bit will then indicate whether or not the initiator has enabled disconnects. The Wait-for-Select-and-Receive command will accept an Identify message with the TRN bit set only if the host issues the command with the SBT bit in the COMMAND register set.

The Reselect-and-Transfer commands use only the LUN portion and the TRN bit of this register to generate the Identify message. The TLV and DOK bits are not used.

7	6	5	4	3	2	1	0
TLV	DOK	TRN	0	0	TL2	TL1	TL0

3.1.15 Command Phase Register

The COMMAND PHASE register indicates which phases of a combination command have completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and decide how to respond to it.

When resuming a combination command, the contents of this register specify from which point to restart the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

3.1.16 Synchronous Transfer Register

The contents of the SYNCHRONOUS TRANSFER register specify the maximum transfer rate and the transfer mode for a SCSI data phase.

For information phases other than a Data phase or when the selected offset is zero (OF3=OF2=OF1=OF0=0), the 33C93B performs asynchronous transfers. A non-zero offset value, which should be twelve or less, selects synchronous data transfers and determines the effective FIFO depth. This value is typically determined through negotiation (as defined in the SCSI standard) with the other SCSI device.

The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI data transfers and, in WD-Bus mode, the transfer period and the width of the RE-/WE- strobes for host transfers; for non-data transfers, the transfer period defaults to six periods. The period is defined in terms of the internal clock cycle time, which depends upon the input clock, the divisor selected in the OWN ID register, and the setting of the FSS bit.

The FSS bit has effect only when operating with an input clock frequency of 16-20 MHz, i.e. the divisor set to 4. Setting this bit enables Fast SCSI transfers, doubling the maximum transfer rate for synchronous transfers. For example, with a 20 MHz input clock and a transfer period of 2, the normal maximum transfer rate (FSS=0) would be 5 MB/s; the Fast SCSI transfer rate (FSS=1) would be twice this value or 10 MB/s. The FSS bit does not affect the rate of asynchronous transfers.

7	6	5	4	3	2	1	0
FSS	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx - OFFSET

The OFFSET bits specifies the desired offset according to the following table:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0 *
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	X	Undefined

* Asynchronous data phase transfers.

Bit 4-6 TPx - TRANSFER PERIOD

The TRANSFER PERIOD bits select the desired desired transfer period according to the following table:

6	5	4	SCSI/WD-BUS TRANSFER PERIOD	(SCSI REQ/ACK Synchronous Pulse Width and WD-BUS RE- /WE- Pulse Width
0	0	X	8 cycles	(4 cycles)
0	1	0	2 cycles	(1 cycle)
0	1	1	3 cycles	(1 cycle)
1	0	0	4 cycles	(2 cycles)
1	0	1	5 cycles	(3 cycles)
1	1	0	6 cycles	(4 cycles)
1	1	1	7 cycles	(4 cycles)

The 'cycle' referred to above is the period of the internal data transfer clock. For asynchronous transfers or for synchronous transfer when the input clock frequency is less than 16 MHz, it is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{\text{DIVISOR (from OWN ID)}}{2 * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

For synchronous transfers when the input clock frequency is 16 MHz or greater, the cycle time is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{2}{(\text{FSS}+1) * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

Bit 7 FSS - FAST SCSI SELECT

The FAST SCSI SELECT bit under the conditions mentioned above enables the doubling of the internal clock frequency resulting in a synchronous transfer rate up to 10 MB/s.

3.1.17 Transfer Count Register

The TRANSFER COUNT register, a 24-bit register, stores a preset value for the internal transfer counter. A Send, Receive, or Transfer Info command causes the 33C93B to load this preset value into the internal transfer counter, which then decrements as each data byte is transferred over the SCSI bus and causes a "successful completion" interrupt when it reaches zero.

Loading the TRANSFER COUNT register with zeros prior to issuing these command or issuing the command with the SINGLE-BYTE TRANSFER bit set in the COMMAND register disables the counter function. If the counter is disabled, the Send, Receive, or Transfer Info command will complete when a single byte has been transferred.

In combination commands, this register specifies the number of bytes to be transferred during a Data phase. A zero value indicates the lack of a Data phase.

After the completion of any successful transfer, including commands issued in Single Byte Transfer mode, the TRANSFER COUNT register will be zero.

When a transfer halts because of an error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred over the SCSI bus, including any bytes present in the FIFO at the time of the interruption. The FIFO clearing process may cause the TRANSFER COUNT register to differ with the host DMA controller count, because some bytes may have been transferred into the FIFO but not to the SCSI bus.

3.1.18 Destination ID Register

The DESTINATION ID register stores the encoded SCSI bus ID of the device to be selected or reselected when a Select or Reselect command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	DF	TG1	TG0	DI2	DI1	DI0

Bit 2-0 DIx - DESTINATION ID
Destination ID bits 2-0 specify which SCSI device to select or reselect.

Bit 3-4 TGx - TAG MESSAGE
The TAG MESSAGE bits select which tag message code to send during Select-and-Transfer and identify which tag message code was received by the Wait-for-Select-and-Receive command. In addition, the Reselect-and-Transfer commands send a Simple-Queue Tag message following the Identify message if either of these bits are set.

4	3	MESSAGE RECEIVED OR SENT
0	0	No Message
0	1	SIMPLE QUEUE TAG (20H)
1	0	HEAD OF QUEUE TAG (21H)
1	1	ORDERED QUEUE TAG (22H)

Bit 5 DF -DISABLE FEATURE
DISABLE FEATURE, when set, disables Data phase direction checking in advanced mode and inhibits the normally automatic link from Send-Status-and-Command-Complete to the command fetch portion of Wait-for-Select-and-Receive when a Linked-Command-Complete message is sent.

Bit 6 DPD - DATA PHASE DIRECTION
DATA PHASE DIRECTION, when advanced features are enabled (see 4.3.1), specifies the expected direction of the SCSI Data phase of a Select-and-Transfer command. When this bit is zero, the expected direction is out (to the target), and when this bit is one, the expected direction is in (from the target). An unexpected data phase error will occur if the actual direction does not match the setting of this bit.

Bit 7 SCC - SELECT COMMAND CHAIN
SELECT COMMAND CHAIN selects which command will follow a Reselect-and-Transfer command when chaining is enabled (EDI=1). When this bit is zero, a Send-Status-and-Command-Complete command will follow; when this bit is one, a Send-Disconnect-Message command follows.

3.1.19 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C93B. It also contains bits that enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bit 2-0 SIx - SOURCE ID
SOURCE ID Bits 2-0, valid only if the SIV bit is set, indicate the SCSI bus ID of the device that selected or reselected the 33C93B.

Bit 3 SIV - SOURCE ID VALID
SOURCE ID VALID is set to one when the 33C93B is selected or reselected and the other SCSI bus device asserted its own bus ID bit during the Selection/Reselection phase. This bit is zero if only the bus ID bit of the 33C93B was asserted.

Bit 5 DSP DISABLE SELECT PARITY
DISABLE SELECT PARITY, when set, causes the 33C93B to ignore the bus

parity when responding to selection or reselection.

Bit 6 ES - ENABLE SELECTION
ENABLE SELECTION, when set, allows the 33C93B to respond to selection by another device on the SCSI bus.

Bit 7 ER - ENABLE RESELECTION
ENABLE RESELECTION, when set, allows the 33C93B to respond to reselection by another device on the SCSI bus.

3.1.20 SCSI Status Register

The SCSI STATUS register, a read-only register, holds a value which indicates the cause of the most recent INTRQ assertion. The 33C93B asserts INTRQ whenever a condition occurs that requires intervention by the host. For example,

- the 33C93B has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

After assertion of INTRQ, the contents of this register will not change until the host reads the register or until the 33C93B has been reset.

7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx - SCSI STATUS
SCSI STATUS bits 0-3 are status qualifiers with meanings that depend upon the upper (4-7) status bits.

Bit 4-7 SSx - SCSI STATUS
SCSI STATUS bits 4-7 define the type of interrupt that occurred. The following table describes the various types:

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STATUS	CODE	GROUP MEANING
0000	xxxx	The 33C93B is in a reset state.
0001	xxxx	A 33C93B command has completed successfully.
0010	xxxx	A 33C93B command has paused or was aborted.
0100	xxxx	A 33C93B command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the state---Disconnected, Target, or Initiator---from which the Status Code can occur. The MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus; a zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The table on the right summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

STATUS	CODE	STATE	SPECIFIC MEANING
0000	0000	DTI	33C93 Reset. The device has been hard reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C93B is disconnected.
0000	0001	DTI	33C93B Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the 33C93B is disconnected.

TABLE 3-2. RESET STATE INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0001	0000	D	A Reselect command completed successfully. The new state of the 33C93B is connected as a target.
0001	0001	D	A Select command completed successfully. The new state of the 33C93B is connected as an initiator.
0001	0010	-	Reserved for future use.
0001	0011	T	A Receive, Send, Reselect-and-Transfer, Wait- for-Select-and-Receive, Send-Status-and-Command-Complete, or Send-Disconnect-Message command completed successfully (ATN is not asserted).
0001	0100	T	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, or Send-Status-and- Command-Complete command completed successfully (ATN is asserted).
0001	0101	DT	A Translate Address command completed successfully.
0001	0110	I	A Select-and-Transfer command completed successfully.
0001	0111	-	Reserved for future use.
0001	1MCI	I	A Transfer Info (non-Message-In phase) command completed successfully. MCI defines the new information type (SCSI bus phase) requested.

TABLE 3-3. SUCCESSFUL COMPLETION INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0010	0000	I	A Transfer Info (Message In phase) command has paused with ACK asserted, giving the host the opportunity to reject the message.
0010	0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select, Reselect, or Wait-for-Select-and-Receive command aborted.
0010	0011	T	A Receive or Send command aborted, or a Wait-for-Select-and-Receive detected an error in the Identify message. (ATN is not asserted).
0010	0100	T	A command aborted or halted due to assertion of ATN, or a Wait-for-Select-and-Receive detected an error in the Identify message. (ATN is asserted).
0010	0101	T	A transfer has aborted because of a violation of the data transfer protocol, possibly corrupting the data.
0010	0110	I	An I/O process with a queue tag which does not match the value in the QUEUE TAG register reselected the 33C93B. ACK has been left asserted.
0010	0111	I	A target whose SCSI bus ID does not match the ID in the DESTINATION ID register reselected the 33C93B or the following Identify message did not match the LUN in the TARGET LUN register. ACK has been left asserted following the Identify message, and the bus ID and LUN of the reselecting target are available in the SOURCE ID and TARGET LUN registers. This status only occurs when executing a Select-and-Transfer in advanced mode.
0010	1MCI	-	Reserved for future use.

TABLE 3-4. PAUSED OR ABORTED INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
0100	0000	DTI	An invalid command was issued.
0100	0001	TI	An unexpected disconnect occurred. The new state of the 33C93B is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C93B is disconnected.
0100	0011	TI	A parity error caused a command to terminate ($\overline{ATN}$ is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	T	A parity error caused a command to terminate ($\overline{ATN}$ is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	DT	A Translate Address command did not complete successfully. The Logical Address exceeded the disk boundaries.
0100	0110	I	A target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the 33C93B during a Select-and-Transfer command. This interrupt occurs when the 33C93B is not in advanced mode. The state of the 33C93B is connected as an initiator.
0100	0111	I	A status byte with a parity error was received during Select-and-Transfer.
0100	1MCI	I	An unexpected information phase was requested. MCI defines the SCSI bus phase requested. This interrupt typically occurs when the phase changes before the Transfer Count reaches zero during a Transfer Info command or when an unexpected phase sequence occurs during a Select-and-Transfer command.

TABLE 3-5. TERMINATED INTERRUPTS

STATUS	CODE	STATE	SPECIFIC MEANING
1000	0000	D	The 33C93B has been reselected. The new state of the 33C93B is connected as an initiator.
1000	0001	D	The 33C93B has been reselected in advanced mode. The Identify message from the target must be read from the DATA register. The ACK signal is asserted. The new state of the 33C93B is connected as an initiator.
1000	0010	D	The 33C93B has been selected (ATN was not asserted). The new state of the 33C93B is connected as a target.
1000	0011	D	The 33C93B has been selected (ATN was asserted). The new state of the 33C93B is connected as a target.
1000	0100	T	The ATN- signal has been asserted.
1000	0101	TI	The target has disconnected. The new state of the 33C93B is disconnected.
1000	0110	-	Reserved for future use.
1000	0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not of a known command group. The host can examine the CDB1 register to determine from the opcode the number of command bytes expected. The new state of the 33C93B is connected as a target. (Advanced mode only)
1000	1MCI	I	The REQ signal has been asserted while the 33C93B was in an idle initiator state. The information phase type should be examined. MCI defines the information phase (SCSI bus phase) requested.

TABLE 3-6. SERVICE REQUIRED INTERRUPTS

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3.1.21 Command Register

The COMMAND register is used to issue the 33C93B commands. The host should never write to this register when the CIP or INT bits (in AUXILIARY STATUS) are set and should never issue a Level II command when the BSY bit is set.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register affects the information transfer commands by disabling the TRANSFER COUNT register and specifying that only one byte is to be transferred. The previous contents of the TRANSFER COUNT register are not preserved.

The SBT bit also affects the Wait-for-Select-and-Receive command. Normally, this command does not accept as valid an Identify message with the LUNTAR bit (bit 5) set, which occurs when the initiator wishes to communicate with a target routine. Issuing the command with the SBT bit set allows it to accept an Identify message for a target routine.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

3.1.22 Data Register

The DATA register provides an interface between the internal twelve byte FIFO and the host. During any type of information phase, the host may access this register with the processor, and during a SCSI Data phase, the host may also access this register through the DMA/WD interface.

The processor, except in one case, should only access the DATA register when the DBR bit in the AUXILIARY STATUS register is true. The exception occurs when the 33C93B is reselected while operating in advanced mode: the processor must retrieve the Identify message from the target by reading the DATA register.

The FFE bit in the AUXILIARY STATUS register enables the host to avoid polling DBR in some cases. This bit, when the host writes to the FIFO, acts as a FIFO empty indicator; thus, when set, the host can safely write up to eleven bytes to the FIFO without polling for DBR between each write. Similarly, when the transfer direction is to the host, the FFE bit indicates the FIFO full condition, and the processor can safely read twelve bytes from the FIFO without checking for DBR before each read. In both cases, the host should consider the FFE bit valid only when DBR is set.

Two exceptions do exist, however, both when writing to the DATA register. First, after the initial setting of the FFE and DBR bits in response to a Transfer Info or Send command, the host may write twelve bytes to the FIFO without causing a FIFO overrun. Second, because the 33C93B splits a Transfer Info command into two separate transfers when responding to a message out phase, the host must not write the last message byte to the DATA register until the 33C93B specifically requests that byte. For instance, if the host wishes to send a (five-byte) Synchronous Data Transfer Request message, the first set of writes should contain only the first four bytes of the message. The host must then poll for DBR before writing the final byte.

The processor normally should not access the DATA register during a Data phase unless the host has selected polled I/O mode by setting all of the DMA MODE SELECT bits in the CONTROL register to zero. In exceptional cases, such as aborting a transfer, the host may wish to switch to polled I/O accesses. In this case, the processor may access the DATA register but must guarantee that the DMA interface is inactive, i.e. DACK inactive in the DMA and Burst DMA modes and RCS deasserted in WD Bus mode.

3.1.23 Queue Tag Register

The QUEUE TAG register holds the second byte of the Tag messages associated with the Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands.

The Select-and-Transfer and Reselect-and-Transfer commands send the contents of this register as the second byte of the Tag message during the Tag message out phase.

The Select-and-Transfer and Wait-for-Select-and-Receive commands place the received queue tag byte into this register during the Tag message in phase. The Select-and-Transfer commands, furthermore, compare the received byte with the previous contents of the register and generate an interrupt in the case of a mismatch.

3.2 RESET CONDITIONS

3.2.1 Hardware Reset

A hard reset, caused by assertion of the $\overline{MR}$ signal, will result in the following conditions:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.

The hard reset does NOT affect the following host accessible registers:

- Registers 01 hex through 15 hex;
- SOURCE ID (16 hex) register bits 0-3;
- COMMAND register (18 hex);

NOTE: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to reset the 33C93B (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR signal to recover from the SCSI reset condition.

3.2.2 Software Reset

A soft reset, caused by executing the Reset command, will result in the following conditions:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and operating mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

4.0 COMMANDS

4.1 COMMAND LIST

COMMAND CODE (HEX)	COMMAND	VALID	LEVEL
00	Reset	D, T, I	I
01	Abort	D, T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T, I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D, I	II
09	Select-without-ATN-and-Transfer	D, I	II
0A	Reselect-and-Receive-Data	D, T	II
0B	Reselect-and-Send-Data	D, T	II
0C	Wait-for-Select-and-Receive	D, T	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D, T, I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D, T	II
20	Transfer Info	I	II

33C93B States:
D = Disconnected
T = Connected as a target
I = Connected as an initiator

Command Levels:
I = Level I command
II = Level II command

TABLE 4-1. COMMAND LIST

4.2 33C93B COMMAND TYPES

The 33C93B command set consists of two types of commands: Level I and Level II commands. Level I commands, except for the Reset and Abort commands, do not generate interrupts upon their completion; Level II commands always terminate with an interrupt. The host may issue a Level I command while a Level II command is executing. Issuing a Level II command while another Level II command is executing will cause unpredictable behavior of the part.

The 33C93B operates in one of three "states" at any one time: disconnected, connected as a target, or connected as an initiator. In each state, the 33C93B recognizes only certain commands as valid, as indicated in the command list above. An attempt to issue a Level II command invalid for the present 33C93B state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

There are two types of Level II commands. 'Simple' Level II commands perform a single operation (e.g. selection) or single phase (e.g. Command phase). 'Combination' Level II commands combine multiple phases into a single 33C93B command to minimize interrupt overhead.

The initiator combination commands expect the target to follow common SCSI bus phase sequences. Any deviation causes an interrupt.

The EDI and IDI bits in the CONTROL register and the SCC bit in the DESTINATION ID register enable and control chaining of target combinations command. Linking commands further decreases interrupt overhead by creating longer phase sequences. When using command chaining, the host must initialize all commands in the chain prior to starting the sequence.

4.3 33C93B SPECIFIC FEATURES

The 33C93B incorporates two sets of features, both of which cause it to be incompatible with the original 33C93 design and one which causes it to be incompatible with the 33C93A device. Both the 33C93A and 33C93B implement the 'advanced mode' features. Both devices, moreover, implement two features included in the 'really advanced' set of functions; however, in this mode, the 33C93B also generates additional interrupts, described below, making it incompatible with the 33C93A.

Upon completion of a hardware reset, both sets of features are disabled. The host enables them by soft resetting the 33C93B with the EAF and RAF bits in the OWN ID register set appropriately. An advanced mode reset results in a 01 hex being loaded into the SCSI STATUS register instead of the 00 hex which normally results from a reset. This difference gives the host a method to deduce that a 33C93B is installed as opposed to a 33C93.

4.3.1 Advanced Mode Features

Unexpected Reselection:
When in normal (33C93) mode, a reselection when idle (ER=1) or a reselection during a Select-and-Transfer command by an target whose ID does not match the one in the DESTINATION ID register causes an interrupt immediately after the reselection handshake finishes. In advanced mode, the 33C93B will continue to the Message In phase to fetch the Identify message. If the 33C93B was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the 33C93B was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the logical unit number will be in the TARGET LUN register. In both cases, the SOURCE ID register will contain the SCSI bus ID of the reselecting target, and the ACK signal remains asserted so that the Identify message may be rejected if desired.

Any message other than a valid Identify message will result in an unexpected message in phase interrupt. If the unexpected reselection occurs during a Select-and-Transfer command, a parity error will cause an unexpected message in phase interrupt only if the halt-on-SCSI-parity-error feature is enabled. If reselected from an idle state, the 33C93B will halt on a parity error regardless of the setting of the HSP bit. The host can retrieve the byte with the Transfer Info command.

Unknown SCSI Command Groups:
The length of a SCSI Command Descriptor Block is determined by the group code, found in bits 7-5 of the first command byte. The SCSI standard (X3.131-1986) defines Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands respectively as six, ten, and twelve byte commands. All other command groups are undefined by that standard. In normal mode, the 33C93B assumes a length of six bytes for these undefined groups when executing a Select-and-Transfer or Wait-for-Select-and-

Receive command. In advanced mode, the 33C93B behaves as follows:

- Select-and-Transfer: When sending a command from an unknown group, the host must load the expected command length into the CDB SIZE register before issuing the Select-and-Transfer. The 33C93B uses this value to make sure the correct number of bytes are transferred in the Command phase.
- Wait-for-Select-and-Receive: When receiving the CDB from the initiator, the 33C93B examines the first CDB byte to determine the command group. An undefined group results in an interrupt with the SCSI STATUS register set to 87 hex and the COMMAND PHASE register set to 31 hex. The host may examine the byte, available in the CDB 1ST register, to determine the TOTAL command length, which it then places into the CDB SIZE register, before resuming the Wait-for-Select-and-Receive command.

  After this interrupt, the 33C93B will only accept a Resume Wait-for-Select-and-Receive, Abort, Disconnect, or Reset command. All other commands are invalid. While the host processes the interrupt, the 33C93B continues to transfer the first six bytes of the SCSI command into its internal FIFO.

Data Phase Direction:
Normally during a Select-and-Transfer command, the target solely determines the direction of the Data phase. The 33C93B will not detect a mismatch between this direction and the one expected by the host and will proceed with the transfer. In advanced mode, the 33C93B compares the DPD bit in the DESTINATION ID register with the state of the I/O- signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with an 'unexpected phase' status in the SCSI STATUS register. Setting the DF bit in the DESTINATION ID register disables this feature.

Microcode Revision:
The 33C93B will load the revision number of the microcode into the CDB1 register during the reset sequence when really advanced features are enabled.

Immediate Halt:
The 33C93B normally checks for parity errors during a synchronous transfer and for the attention condition during both asynchronous and synchronous transfer on 4096-byte boundaries. With really advanced features enabled, the 33C93B continuously checks for these conditions and upon detecting one issues an Abort command.

Protocol Error:
The 33C93B, if it detects a possible transfer corruption caused by noise on the REQ- and ACK- signals, will abort a Send or Receive command and generate a 25 hex interrupt. The detection scheme can not catch all possible failures due to the nature of the SCSI transfer protocols; however, this feature does provide some protection against data integrity faults.

Unexpected Bus Free Interrupts:
The 33C93B will generate either an 85 hex interrupt or a 41 hex interrupt in the event that a glitch on the SEL- signal causes the device to disconnect from the SCSI bus.

4.4 LEVEL I COMMANDS

4.4.1 Reset (00 hex)

The Reset command initializes the 33C93B according to the contents of the OWN ID register and as described in the RESET CONDITIONS section. The host may issue the Reset command while in any state, forcing the 33C93B into a disconnected state; any command executing at that time will terminate. Upon completion of the Reset command, the 33C93B will generate an interrupt with the SCSI STATUS register containing a 00 hex or a 01 hex depending upon the contents of the OWN ID register at the time of the reset.

4.4.2 Abort (01 hex)

The Abort command is valid in the disconnected and connected-as-a-target states. The Abort command has different effects depending on the current state and the command that is currently executing, as described below:

- Disconnected State: In this state, the Abort command will halt a selection or reselection attempt of a Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command or will halt the Wait-for-Select-and-Receive command before selection. Aborting a selection or reselection attempt before the 33C93B has won arbitration immediately returns the 33C93B to an idle state and generates a "paused/aborted" interrupt. If the 33C93B has already won arbitration, the Abort command causes the 33C93B to remove the Bus ID bits from the SCSI bus while maintaining assertion of SEL. If the target does not respond within at least 200 µs by asserting BSY-, the 33C93B will go to a Bus Free condition and generate a "paused/ aborted" interrupt. If the target does respond within this time period, a "successful completion" interrupt will result instead.

  The Abort command, in addition, will terminate a Select- and-Transfer command if the target has disconnected from the bus. The 33C93B will generate an 85 hex interrupt and will be in the Disconnected state. If the target is still connected at the time the Abort command is recognized, the command will be ignored.

- Target State: In this state, the Abort command will terminate a Receive or Send command or the Data phase portion of a Reselect-and-Transfer command. The following rules apply when issuing an Abort:

  - During a Send or Reselect-and-Send command, the 33C93B removes the data request (DRQ-, DBR, etc.) at an arbitrary time during the abort procedure. The host must NOT service any data request once it has written the Abort command to the COMMAND register until the 33C93B generates an interrupt. Abort processing will not complete until the contents of the FIFO are flushed to the SCSI bus.
  - During a Receive or Reselect-and-Receive command, the host must CONTINUE to service any data request from the 33C93B. Abort processing will not complete until the contents of the FIFO are flushed to the host.

    After completion of the Abort command, the TRANSFER COUNT register contains the number of bytes that were not transferred across the SCSI bus. The 33C93B remains in the connected-as-a-target state and will accept any target mode command, including a resume of the aborted command.

4.4.3 Disconnect (04 hex)

The Disconnect command, valid in the initiator and target states, immediately terminates an active Level II command, causes the immediate release of all bus signals, and returns the 33C93B to a disconnected state. In the target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the initiator role, this command can be used to release the bus following a timeout condition.

4.4.4 Assert ATN (02 hex)

The Assert ATN command, valid only when connected as an initiator, allows the initiator to inform the target that it has a message pending. The target should respond with a Message Out Phase. ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C93B to assert ATN automatically prior to the release of SEL.

4.4.5 Negate ACK (03 hex)

The Negate ACK command causes the 33C93B to release ACK which for some reason it has held active. Holding ACK active allows the host to respond to information it has just received before the target continues the current phase or proceeds to the next one. The 33C93B, therefore, does not negate ACK before generating an interrupt in the following cases:

- after successful completion of a Message-In Transfer Info command;

- after detection of a parity error on any received SCSI information when the HALT on SCSI PARITY ERROR (HSP) bit is set;
- after unexpected reselection in advanced mode;
- after reception of a save-data-pointer message during a Select-and-Transfer command;
- after reselection by a process with a queue tag which differs from the contents of the QUEUE TAG register; and
- after reception of a status byte with a parity error during a Select-and-Transfer command.

$\overline{ACK}$ negates automatically for all initiator transfers other than Message In transfers. Host parity errors, moreover, do not affect the $\overline{ACK}$ signal.

Before completing a Message In phase, the initiator, upon examining the message, may decide to reject it and send a "MESSAGE REJECT" message to the target or, upon detecting a parity error in the message, may decide to send a "MESSAGE PARITY ERROR" message to the target. Similarly, if a parity error causes a transfer command to terminate, the initiator may wish to send an "INITIATOR DETECTED ERROR" message to the target. In all cases, the initiator signals its intent to send a message by asserting ATN before issuing the Negate ACK command.

4.4.6 Set IDI (0F hex)

The Set IDI command provides support for overlapped SCSI operations in the initiator role. The host may start a SCSI operation with the IDI bit reset, allowing the 33C93B to handle target disconnects and reconnects and thus minimizing the interrupt handling overhead. When it wishes to start a second operation, the host issues the Set IDI command so that if the current target disconnects and releases the SCSI bus, the 33C93B will produce an interrupt. The host may now start the second operation without having had to wait for the first operation to complete.

4.5 SIMPLE LEVEL II COMMANDS

4.5.1 Select-with-ATN (06 hex)

Select-with-ATN, valid only in the disconnected state, instructs the 33C93B to select a target. Before issuing this command, the host should write the SCSI Bus ID of the target device into the DESTINATION ID register. The Select-with-ATN command causes the 33C93B to begin bus arbitration. If another device selects or reselects the 33C93B during arbitration, the Select-with-ATN command aborts and a "service required" interrupt (8x hex) will occur.

Should the 33C93B win the arbitration, it asserts SEL and ATN, places the target and initiator Bus IDs on the SCSI data bus, and then deasserts BSY. At this time, a timeout sequence begins, its length determined by the value in the TIMEOUT PERIOD register. If the target does not respond with BSY within the allotted time, the 33C93B begins a selection abort sequence as described in the Abort command description. If the target has not responded by the end of this sequence, the Select-with-ATN command terminates. If the target responds before the timeout period has elapsed or before the selection abort sequence completes, the 33C93B negates the SEL signal, enters the connected-as-an-initiator state, and generates a "successful completion" interrupt.

A successful abort of Select-with-ATN, either through a timeout or through the Abort command, leaves the 33C93B disconnected from the SCSI bus and results in a "paused/aborted" interrupt.

4.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with- ATN command except that ATN is not set during the Selection Phase.

4.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O- signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C93B being connected as a target.

4.5.4 Receive (10-13 hex)

The four Receive commands---Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out---differ from each other only by the state of the C/D and MSG pins and the type of data that is transferred. These commands, valid only in the target role, correspond to those SCSI information phases where the I/O pins is not asserted; the type of the Receive command selected determines the state of the C/D and MSG outputs according to the following chart (1=asserted):

RECEIVE	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Receive	Command	10	0	1	0
Receive	Data	11	0	0	0
Receive	Message Out	12	1	1	0
Receive	Unspecified Info Out	13	1	0	0

A Receive command will complete or terminate under any of the following conditions:

- The host has read the specified number of bytes from the DATA register;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-SCSI-Parity is enabled;
- The 33C93B detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR.

Any conclusion of a Receive command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected-as-a-target state and the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of a Receive Data command, the 33C93B evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.5 Send (14-17 hex)

The four Send commands---Send Status, Send Data, Send Message, and Send Unspecified Info---like the four Receive commands, differ from each other only by the state of the C/D and MSG pins and the type of data that is transferred. These commands, valid only in the connected-as-a-target state, correspond to those SCSI phases where the I/O- pin is asserted; the type of Send command selected determines the state of the C/D and MSG outputs according to the following chart (1=asserted):

SEND	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Send	Status	14	0	1	1
Send	Data	15	0	0	1
Send	Message In	16	1	1	1
Send	Unspecified Info Out	17	1	0	1

A Send command will complete or terminate under any of the following conditions:

- The initiator has acknowledged receipt of the specified number of bytes;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-Host-Parity is enabled;
- The 33C93B detects $\overline{ATN}$ when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR.

Any conclusion of a Send command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected-as-a-target state and

the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of the Send Data command, the 33C93B evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.6 Transfer Info (20 hex)

The Transfer Info command allows the host to send and receive data, command, status, and message information when operating in the connected-as-an-initiator state.

The first $\overline{REQ}$ assertion following connection as an initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the target, and then issue a Transfer Info command in response. The 33C93B will also generate an interrupt each time the target device requests a new type of information transfer phase.

The processor either should initialize the TRANSFER COUNT register prior to issuing this command or issue the command with the SBT bit in the COMMAND register set. Also, if responding to a request for a Data phase, the processor should set the DMA mode select bits in the CONTROL register and specify the offset and transfer period in the SYNCHRONOUS TRANSFER register before issuing the Transfer Info command.

Behavior of the DBR status bit during Transfer Info depends upon the direction of the transfer. When the bytes move from the initiator to the target, i.e. an out phase, the DBR bit is set whenever the FIFO can accept additional data from the host. When the transfer proceeds in the opposite direction, DBR set indicates that the FIFO contains data available for the host to read.

The Transfer Info command normally terminates or pauses after the specified number of bytes has been sent or received. For a non- Message-In transfer, the 33C93B will generate a "successful completion" interrupt after the target asserts REQ to begin a new phase. For a message-in transfer, the 33C93B does not wait for the next phase but instead leaves ACK asserted and generates a "paused/aborted" interrupt. The processor can then assert ATN if it intends to reject the message before negating ACK.

The Transfer Info command may terminate for a number of different reasons which are listed below:

- The host issues a Disconnect command;
- The 33C93B resets in response to the assertion of MR or the Reset command;
- The target negates the $\overline{BSY}$ signal;
- The target unexpectedly changes phase, i.e. before the specified number of bytes have been transferred; or
- The incoming data has a parity error and the corresponding halt-on-parity-error bit is set.

The Disconnect command, the hard and soft resets, and the negation of BSY will leave the 33C93B in a idle, disconnected state, and in these cases, the value in the TRANSFER COUNT register will not accurately reflect the number of bytes that did not transfer across the SCSI interface. Except for the issuance of the Disconnect command, these occurrences will result in an interrupt.

The 33C93B checks for a parity error on each byte it receives; however, for synchronous transfers, the internal microcontroller will not recognize an error until the transfer reaches a 4096- byte boundary. The response to the parity error, furthermore, depends upon the direction of the transfer. If the parity error occurs on received SCSI data, the 33C93B will halt the SCSI interface, leaving ACK asserted to halt the target, and generate a "terminated" interrupt once the host has flushed any remaining bytes from the FIFO. Similarly, if the error occurs on data received on the host interface, the 33C93B will halt the host interface and generate a "terminated" interrupt after any bytes remaining in the FIFO are flushed to the SCSI bus; the ACK signal, however, will not remain asserted. In both cases, the TRANSFER COUNT register will indicate the number of bytes that did not successfully transfer to or from the target.

If it detects a parity error but the appropriate halt-on-parity-error bit is not set, the 33C93B will indicate the error by setting the PARITY ERROR bit in the AUXILIARY STATUS register but will not terminate the Transfer Info command.

An unexpected phase change will cause a "terminated" interrupt, and as in the case of a parity error, the TRANSFER COUNT register contains the number of bytes yet to be transferred. If an unexpected phase change occurs during a SCSI synchronous transfer, the host should test the PARITY ERROR bit in the AUXILIARY STATUS register, as the phase change most likely occurred before the internal microcontroller recognized the parity error. In the asynchronous case, the 33C93B stops on the byte with the error; therefore, it will always detect a parity error before a phase change in this mode.

4.5.7 Translate Address (18 hex)

The Translate Address Command performs a logical-address to physical-address translation to facilitate processing of certain SCSI commands involving logical addresses up to 32 bits in length. To perform this mapping, the processor first loads the logical address into the LOGICAL ADDRESS register, the disk parameters into the TOTAL CYLINDER NUMBER, TOTAL HEAD NUMBER, and TOTAL SECTOR NUMBER registers, and zeros into the HEAD NUMBER and CYLINDER NUMBER registers. It then issues the Translate Address command, and upon receiving a "successful completion" interrupt, reads the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUMBER registers to obtain the logical address.

The Translate Address command can also compensate for spare sectors. To use this feature, the host, instead of zeroing the HEAD NUMBER and CYLINDER NUMBER registers, should load the number of spare sectors per cylinder into the HEAD NUMBER register and the logical number of sectors per cylinder into the CYLINDER NUMBER register prior to issuing the command.

An overflow during any calculation will result in a "terminated" interrupt.

4.6 COMBINATION LEVEL II COMMANDS

4.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C93B's internal microprocessor to manage the low-level SCSI protocol. Use of these command may result in as few as one interrupt per SCSI operation. Select-and-Transfer commands, used when in an initiator role, typically consist of at least the following SCSI phases: an Arbitration phase, a Selection phase, a Command phase, a Status phase, and a Command-Complete Message phase. These commands optionally include Data and additional Message In phases.

The Select-and-Transfer commands expect the target to follow a certain sequence of SCSI bus phases, and any deviation from this expected protocol results in a "terminated" interrupt. As the different phases complete, the 33C93B updates the COMMAND PHASE register, so upon termination of the command, the host processor may examine this register to identify the cause of the termination and the state of the SCSI operation.

The two Select-and-Transfer commands differ from each other only by whether or not the 33C93B asserts ATN pin during the Selection phase. The ability to assert ATN during Selection supports the SCSI message protocol which calls for an Identify Message Out phase following the selection. When executing a Select-with-ATN-and-Transfer command, the 33C93B expects the target to request a Message Out phase immediately following selection, whereas for a Select-without-ATN-and-Transfer command, it expects the target to begin the Command phase once selection completes.

The 33C93B begins the Select-and-Transfer command by arbitrating for the bus and selecting a target just as during a Select command. If the target does not respond before a timeout occurs, the Select-and-Transfer command halts and generates an interrupt. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the selection is successful, no interrupt is generated, and the COMMAND PHASE register will be set to a 10 hex.

After completing the Selection phase, the 33C93B begins a Message Out phase if ATN has been

asserted or a Command phase if not. When the target requests a Message Out phase, the 33C93B responds by automatically sending an Identify message byte, which it generates by exclusive-ORing the contents of the TARGET LUN register with 80 hex if the ENABLE RESELECTION bit in the SOURCE ID register is reset or with C0 hex if the bit is set. After it has sent the Identify message, the 33C93B will set the COMMAND PHASE register to 20 hex.

Normally, bit 6 of the Identify message mirrors the state of the ENABLE RESELECTION bit; however, the host may occasionally wish to allow the 33C93B to respond to a reselection attempt but not enable target disconnects during another SCSI operation. Setting both the ENABLE RESELECTION bit and the DOK bit of the TARGET LUN register allows the 33C93B to respond to reselection but results in an Identify message byte which does not enable target disconnects.

Following the Identify message out, if bits 3 or 4 of the DESTINATION ID register specify a tag message and if ATN- is asserted, the 33C93B expects the target to request the first byte of a tag message. It responds to this request by sending the selected tag message code and incrementing the COMMAND PHASE register. The 33C93B now expects the target to ask for the second byte and services this request by sending the contents of the QUEUE TAG register and incrementing the COMMAND PHASE register to 22 hex.

The 33C93B expects a Command phase to follow the Message Out phase or, if ATN is not asserted during selection, the Selection phase. The 33C93B obtains the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and sends either six, ten, or twelve bytes of command information depending on the first byte of the SCSI command. The Select-and-Transfer commands support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands. The length of any other command defaults to six bytes unless advanced mode is enabled (see 7.3.1). The COMMAND PHASE register, set to 30 hex before the first Command byte is sent, increments with each byte transferred, so for a twelve-byte CDB command, the COMMAND PHASE register will contain 3C hex when all bytes of the CDB have been transferred.

After the Command phase, the 33C93B anticipates a Data phase if the TRANSFER COUNT register contains a non-zero value, a Status phase if this register contains zero, or, in either case, a Message In phase if the ENABLE RESELECTION bit is set and the DOK bit is not. The 33C93B assumes a pending disconnection if the target requests a Message In phase. Thus, when enabled, the 33C93B expects to receive either a Save-Data-Pointer message (02 hex) or a Disconnect message (04 hex). If a message byte has a parity error and the HSP bit is set or if the target sends an unsupported message, the 33C93B will generate a "terminated" interrupt, alerting the processor of this fact and allowing it to retrieve the message byte via the Transfer Info command.

Reception of a correct Save-Data-Pointer message results in a "paused/aborted" interrupt, terminating the Select-and-Transfer command with the COMMAND PHASE register set to 41 hex. The processor can then save the SCSI data pointer before resuming the Select-and-Transfer command.

A Disconnect message, on the other hand, will not cause an interrupt; instead, command execution continues with the COMMAND PHASE register set to 42 hex and with Bus Free as the next expected phase. The 33C93B updates the COMMAND PHASE register to 43 hex when the target actually disconnects and, if the IDI bit is set, suspends the Select-and-Transfer command with an 85 hex interrupt. If, however, the IDI bit is reset, the 33C93B sits in an idle state, waiting for the target to reconnect. Reselection by the original target generates no interrupt and increments the COMMAND PHASE register to 44 hex; reselection by a different target will cause a "terminated" interrupt. In advanced mode, this interrupt will not occur until the 33C93B has also received the Identify message from the target and placed the logical unit number in the target LUN register.

Following the original target reselection, the 33C93B expects an Identify Message In phase from the target. This single-byte message should be of the binary form: 10r00ttt, where r and ttt match the corresponding bits in the TARGET LUN register. Successful completion of this phase results in the COMMAND PHASE register being updated to 45 hex or 70 hex depending upon whether or not the 33C93B expects a tag message, deduced from the settings of the TG0 and TG1 bits of the DESTINATION ID register.

The target, in the latter case, should send a Simple Queue tag message immediately after the Identify

message. Upon receiving and validating the message byte, the 33C93B increments the COMMAND PHASE register and awaits the second message byte from the target. When it receives this byte, the 33C93B sets the COMMAND PHASE to 45 hex and then compares the byte to the contents of the QUEUE TAG register. If the two values match, command execution proceeds; if the two values differ, the 33C93B stores the received byte in the QUEUE TAG register, generates a "Different Process Reselected" interrupt (26 hex) and terminates the Select-and-Transfer command.

The 33C93B anticipates a data phase immediately after the Command phase or after successfully receiving the proper messages after reselection. To handle the Data phase, the Select-and-Transfer command effectively performs a Transfer Info command. The contents of the TRANSFER COUNT register determines the number of bytes to transfer; the value in the SYNCHRONOUS TRANSFER register specifies the type and minimum period of the transfers on the SCSI interface; and the DMA mode select bits in the CONTROL register specify the protocol to follow on the host interface.

Any number of disconnection/reconnection cycles may occur during the data transfer so long as the target follows the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45,70,71) with each disconnection and subsequent reconnection until all of the data has been transferred, at which point it is set to 46 hex. During the data transfer, a disconnection will cause an interrupt regardless of the setting of the IDI bit to allow the host to reinitialize the external DMA controller.

The start of the Status phase, assuming the transfer count has reached zero, advances the COMMAND PHASE register to 47 hex. If the status byte has no parity error or if the HSP bit is not set, the internal microcontroller places the byte in the TARGET LUN register and updates the COMMAND PHASE register to 50 hex. If the byte contains an error, a 27 hex interrupt will occur, and the command will terminate with ACK asserted.

The 33C93B expects the target to send a Command-Complete message (00 hex) to indicate that the SCSI operation has completed. Upon receiving this message, the 33C93B sets the COMMAND PHASE register to 60 hex, and if the EDI bit is reset, generates "successful completion" interrupt. The processor should then read the TARGET LUN register to examine the target status. Another interrupt will occur when the SCSI bus goes to the Bus Free state or when the target again asserts REQ- to begin a new information transfer phase (as in SCSI linked commands). Setting the EDI bit suppresses the "successful completion" interrupt until the target disconnects from the SCSI bus.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Select-and-Transfer commands and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C93B is in the disconnected state.
10	The target has been selected. The 33C93B is now in the connected-as-an-initiator state.
20	An Identify message has been sent to the target.
21	The Tag message code has been sent to the target.
22	The Queue tag has been sent to the target.
30	Command phase has started, no bytes transferred.
3X	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI Bus Free) following a successful transfer of a Disconnect message. The 33C93B is now in the disconnected state.
44	The 33C93B has been reselected by the target with a SCSI bus ID which matches the value in the DESTINATION ID register. The 33C93B is now in the connected as an initiator state.
45	The 33C93B has received an matching Identify message and, if expected, a matching Tag message from the target.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to or from the target during the Data phase.
47	The target has begun a Receive Status phase.
50	The 33C93B has successfully received a Status byte from the target and stored it in the TARGET LUN register.
60	The 33C93B has successfully received a Command-Complete message from the target.
70	The 33C93B has received an Identify message from the target, and the Logical Unit Number matches the value in the TARGET LUN register. A tag message is expected.
71	The 33C93B has received a Simple-Queue Tag message.

TABLE 4-2. SELECT-AND-TRANSFER COMMANDS

The host processor may resume a Select-and-Transfer sequence by issuing the command when the 33C93B is in the Connect-as-an-initiator state. When resuming the Select-and-Transfer, the 33C93B examines the COMMAND PHASE register to determine where to restart execution of the command. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, supports multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after target selection is complete.
20	Resume after Identify message out. Command or message phases are expected; an implied Negate ACK occurs.
22	Resume after Tag message out. Command phase is expected; an implied Negate ACK occcurs.
30	Resume when Command phase has begun (REQ- asserted).
41	Resume after Command phase or after a Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a target. An Identify Message In expected.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the Data phase has completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the target; an implied Negate ACK occurs.
70	Resume to receive a Simple-Queue Tag message. An implied Negate ACK occurs.

TABLE 4-3. SELECT-AND-TRANSFER COMMANDS

4.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands consist of the Reselect-and- Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C93B to execute certain common SCSI bus phase sequences as a target following a Reselection phase. These phases, determined by which command is sent and the setting of the EDI bit in the CONTROL register and the SCC bit in the DESTINATION ID register, are summarized below. Refer to the descriptions of the Send-Status-and-Command-Complete and Send- Disconnect-Message commands for details on those sequences.

- Reselect-and-Receive command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Completion interrupt.
- Reselect-and-Send command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Completion interrupt.
- Reselect-and-Receive command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Status-and-Command-Complete
- Reselect-and-Send command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;

  - Chain to Send-Status-and-Command-Complete;
- Reselect-and-Receive command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Disconnect-Message;
- Reselect-and-Send command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Disconnect-Message;

The Message In phase consists of an Identify message and, if bits 3 and 4 in the DESTINATION ID register are not both zero, a Simple-Queue Tag message. The commands send the contents of the QUEUE TAG register as the second byte of the Tag message.

If the reselection attempt times out during a Reselect-and-Transfer command, if ATN is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will terminate with the appropriate status. In this case, the COMMAND PHASE register will indicate the last successfully completed phase. If these conditions do not occur and all phases complete normally, the command will end with a "successful completion" interrupt at this point if EDI=0. However, if EDI=1, no interrupt is generated and command chaining occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Reselect-and-Transfer commands and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C93B is in the disconnected state.
10	The 33C93B has successfully reselected the initiator. The 33C93B is now in the connected as a target state.
20	The Identify message has been successfully sent to the initiator.
46	The requested data transfer has been completed.

TABLE 4-4. RESELECT-AND-TRANSFER COMMANDS

The host processor may resume a Reselect-and-Transfer sequence by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming, the 33C93B examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command. This feature in conjunction with the capability to chain to other combination commands allows longer SCSI bus sequences to be performed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

TABLE 4-5. RESELECT-AND-TRANSFER COMMANDS

4.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C93B to idle until it is selected by an initiator, at which time the 33C93B will enter the target mode and automatically request message and command information. Optionally, the 33C93B will then disconnect if it receives a SCSI read command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase and minimizes bus-connect time during SCSI read commands.

If the initiator asserts $\overline{ATN}$ during the Selection phase, the 33C93B first executes an implied "Receive Message Out" command to get the Identify message and the Tag message, if any, from theinitiator. The 33C93B stores the Identify message byte in the TARGET LUN register; it encodes the Tag message code into bits 3 and 4 of the DESTINATION ID register and places the queue tag into the QUEUE TAG register. Normally, the Wait-for-Select-and-Receive command rejects an Identify message with the LUNTAR bit (bit 5) set; however, issuing this command with the SBT bit in the COMMAND REGISTER set allows the 33C93B to accept an Identify message for a target routine.

The 33C93B executes an implied "Receive Command" following the Selection phase or Identify Message In phase and stores the SCSI command information in the CDB registers. It determines the number of command bytes to request from the SCSI group code in the first byte of the CDB.

At this point, a "successful completion" interrupt normally will occur to allow the local processor to interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the host enables the 33C93B to perform an automatic disconnect when it receives a SCSI read command. Thus, when EDI=1 and the 1st CDB byte received contains a six, ten, or twelve byte read command code, the 33C93B will suppress the interrupt and chain to the Send-Disconnect-Message command. Completion of this sequence causes an interrupt and normally indicates a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If the message or command information received from the initiator is invalid, the Wait-for-Select-and-Receive command will be terminated and the appropriate status reported. As usual, the COMMAND PHASE register will indicate which phases of the command completed before the error condition occurred.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Wait-for-Select-and-Receive command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C93B has not been selected. The 33C93B is in the disconnected state.
10	The 33C93B has been successfully selected by the initiator. The 33C93B is now in the connected-as-a- target state.
20	The 33C93B has received a message byte (Identify) from the initiator. The TARGET LUN register holds the byte.
21	The 33C93B has received a message byte (Tag code) from the initiator. The QUEUE TAG register contains the byte.
22	The 33C93B has received a message byte (Queue Tag) from the initiator. The QUEUE TAG register contains the byte.
30	The 33C93B is ready to begin Command phase. The SCSI bus phase lines and REQ- have not been asserted.
31	The 33C93B has transferred one command byte from the initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The 33C93B has transferred x command bytes from the initiator.

TABLE 4-6. WAIT-FOR-SELECT-AND-RECEIVE COMMANDS

A "paused/aborted" interrupt in conjunction with command phases 20 and 21 indicate that the respective message byte was not valid. A parity error in the Identify message results in the appropriate interrupt and the COMMAND PHASE register set to 10 hex. This combination allows the host to retry the transfer by merely reissuing the command to resume the operation from the proper phase. A parity error in the other two message bytes results in a command phase of 21 or 22, indicating which byte contained the error.

The host processor may resume the Wait-for-Select-and-Receive command by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming this command, the 33C93B examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the initiator is complete. Start with Identify Message Out if ATN is asserted; otherwise, start with Command phase.
20	Resume after a Message Out; check the received message in the TARGET LUN register for a valid Identify message.
21	Resume after Identify message verified. Start with Tag Message Out if ATN is asserted; otherwise, start with Command phase.
30	Resume after Identify Message Out. Start with Command phase.
31	Resume after the 33C93B has transferred one command byte from the initiator. This resume point is used only when an unknown group code has been detected in advanced mode and the command size has been loaded into the OWN ID register.

TABLE 4-7. WAIT-FOR-SELECT-AND-RECEIVE COMMANDS

4.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command, valid in the target role, combines the Status and the Command-Complete Message phases used to complete a SCSI operation into one command. This command also supports linked SCSI operations by optionally sending a Linked-Command-Complete message after the transferring the status byte. Bits in the CDB12 register corresponding to the standard linked command control bits in the CDB control the choice of Linked-Command-Complete messages.

Before issuing this command, the host loads the status byte into the CDB11 register and the link control bits from the current CDB into the CDB12 register. Note that the bits used by the 33C93B are identical in meaning to the SCSI standard link control bits. Consequently, the host processor may simply load the control byte from the current SCSI command into CDB12 to obtain the correct function. As the command execution progresses, the COMMAND PHASE register will update to indicate the last phase completed.

The possible sequences caused by this command are as follows:

- CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex), followed by a transition to bus free. A "successful completion" interrupt now occurs.
- CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked-Command-Complete message (0A hex). If the DF bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.
- CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked-Command-Complete-with-Flag message (0B hex). If the DF bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.

Assertion of ATN- when HA=1, assertion of $\overline{MR}$, or execution of a Disconnect or Reset command will terminate this command.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Status-and-Command-Complete command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

TABLE 4-8. SEND-STATUS-AND-COMMAND-COMPLETE COMMANDS

The host processor may resume the Send-Status-and-Command-Complete command by loading the appropriate value into the COMMAND PHASE register prior to issuing the command. This feature, in conjunction with the capability to chain to other combination commands, allows for a single command to invoke longer SCSI bus sequences.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if selected to do so.

TABLE 4-9. SEND-STATUS-AND-COMMAND-COMPLETE COMMANDS

4.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command, a target-mode command, instructs the 33C93B to send a Disconnect message and then to deassert the $\overline{BSY}$ signal, causing a logical disconnection of the device from the SCSI bus. Also, a Save-Data-Pointer message will precede the Disconnect message if the host sets the IDI bit prior to issuing this command.

Assertion of $\overline{ATN}$ when HA=1, assertion of $\overline{MR}$, or execution of a Disconnect or Reset command will terminate this command. The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Disconnect-Message and their meanings relative to command termination.

COMMAND PHASE	MEANING
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C93B is now in the disconnected state.

TABLE 4-10. SEND-TO-DISCONNECT-MESSAGE COMMANDS

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND ..... -0.5 V to +7.0 V
Operating temperature ..... 0° to 70° C
Storage temperature ..... -55° to +125° C
Power dissipation ..... 500 mW
Input Static Discharge Protection ..... 1200 V pin to pin

DC OPERATING CHARACTERISTICS ..... Ta = 0° to 70° C,
..... VCC = +5 V ± - 0.25 V, GND = 0 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		10	uA	VIN = .4 to VCC
IOL1	SCSI Output Leakage (Inactive)		50	uA	VOUT = .5 to VCC
IOL2	Output Leakage (Tri-state)		10	uA	VOUT = .4 to VCC
VIH	Input High Voltage	2.0	5.0	V	
VIL	Input Low Voltage	-.25	0.8	V	
VIHYS	Schmitt Trigger Input Hysteresis (All SCSI Pins)	0.3		V	
VOH	Output High Voltage	2.4		V	IO = -400 uA
VOL1	SCSI Output Low Voltage (1)		0.5	V	IO = 48.0 mA
VOL2	Output Low Voltage (All Others)		0.4	V	IO = 4.0 mA
ICC	Supply Current		36	mA	Ta = +25° C

(1) $\overline{REQ}$ and $\overline{ACK}$ will sink 57 mA at 0.5 volts.

6.0 TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0° to 70° C) and voltage (4.75 to 5.25 Volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads. Additionally, open-drain outputs DRQ and DACK are tested with 10 mA current source pull-ups as loads.

The SCSI asynchronous timings, furthermore, assume that the minimum assertion and deassertion times specified for the chosen transfer period have been met. For example, with a transfer period of four, the 33C93B, acting as a target, will assert REQ for at least 200 ns. If the initiator takes more than 200 ns from the leading edge of REQ to assert ACK, then the 33C93B will release REQ within 175 ns. However, if the initiator responds with ACK within 200 ns of REQ, the 33C93B may not meet the 175 ns maximum.

These timings, moreover, apply only during a burst and assume that the FIFO has space or data available to allow the burst to continue. For instance, the time from the REQ in low to ACK out low for the first byte of a new phase or of a 4096-byte burst will depend on the time needed by the 33C93B and possibly the host microprocessor to respond to the new phase or to set up for the next 4096-byte block. Clearly, the 33C93B can not meet the175 ns timing in these situations. In addition, the internal microcontroller controls the handshaking of messages bytes, like the Identify and Disconnect messages, during execution of the combination commands, and again, in these cases, the 33C93B will not meet the asynchronous transfer timings given in the following tables.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time Tcyc. The cycle time depends upon the input clock frequency, the clock divisor selected, and, for synchronous transfers and if the input clock frequency is 16 MHz or greater, the setting of the FSS bit in the SYNCHRONOUS TRANSFER register. Section 6.2.16 provides the details on calculating Tcyc for a given set of these parameters. For normal SCSI transfers, the resulting clock has a frequency from 4 MHz to 5 MHz; for fast SCSI transfers, the frequency falls in the range from 8 MHz to 10 MHz. For non-transfer timings, such as those pertaining to arbitration and bus release, Tcyc corresponds to the value for normal SCSI transfers.

6.1 PROCESSOR/DMA INTERFACE

6.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	CLOCK PERIOD	50	125	ns
tch	CLOCK HIGH	20		ns
tcl	CLOCK LOW	20		ns

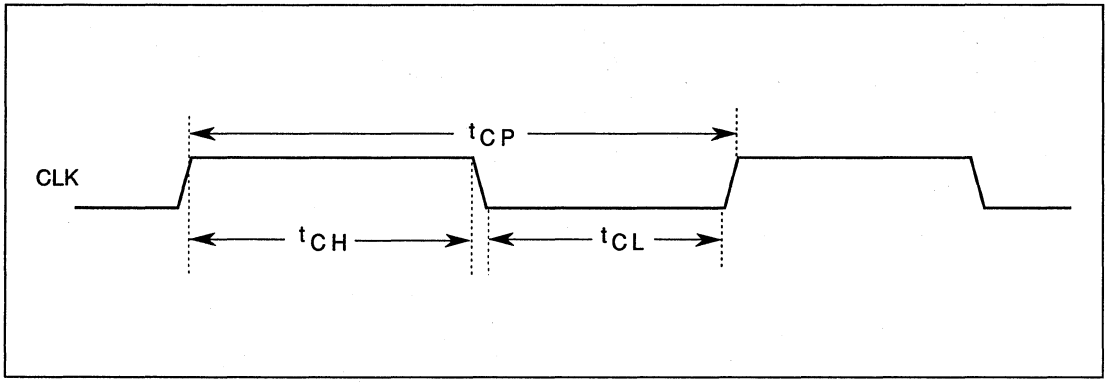


FIGURE 6-1. CLOCK TIMING

6.1.2 MR-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	$\overline{\text{MR}}$ PULSE WIDTH	1		us

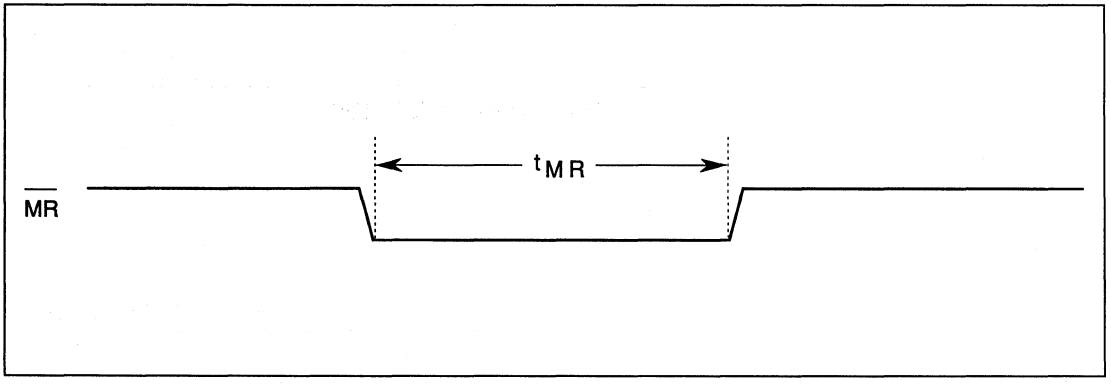


FIGURE 6-2. MR- TIMING

6.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 VALID TO $\overline{WE}$ LOW	0		ns
tclwl	$\overline{CS}$ LOW TO $\overline{WE}$ LOW	0		ns
twe	$\overline{CS}$ LOW, $\overline{WE}$ LOW TIME	120		ns
tdvwh	DATA VALID TO $\overline{WE}$ HIGH	70		ns
twhai	$\overline{WE}$ HIGH TO $\overline{A0}$ INVALID	0		ns
twhch	$\overline{WE}$ HIGH TO $\overline{CS}$ HIGH	-5		ns
twhdi	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
twhw1	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns

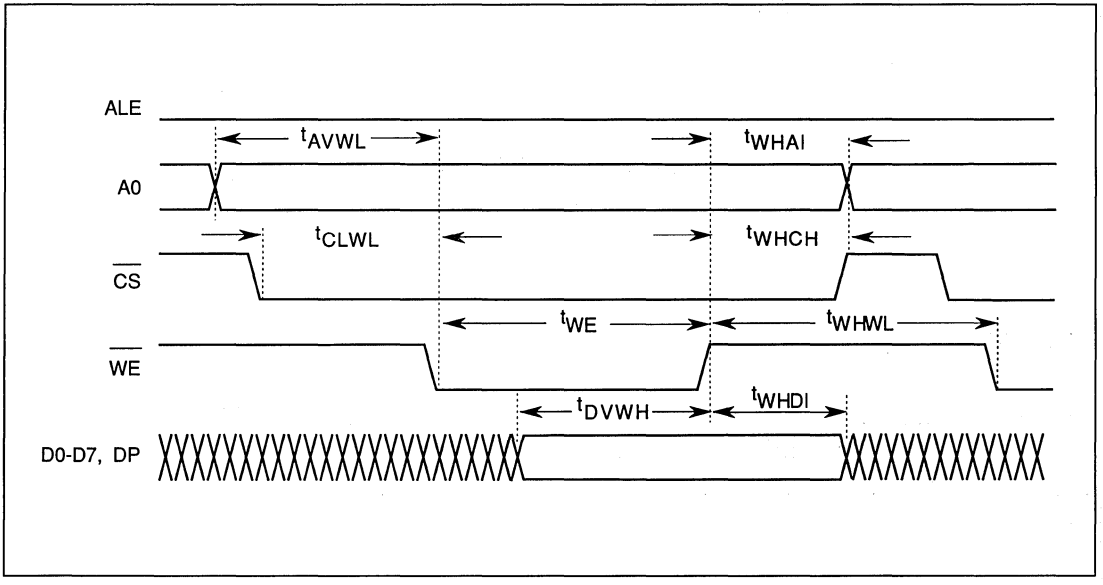


FIGURE 6-3. PROCESSOR WRITE TIMING

6.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 VALID TO $\overline{RE}$ LOW	0		ns
tclrl	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
tre	$\overline{CS}$ LOW, $\overline{RE}$ LOW TIME	180	10000	ns
trldv	$\overline{RE}$ LOW TO DATA VALID		162	ns
trhch	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	-5		ns
trhdi	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns
trhrl	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns
trhai	$\overline{RE}$ HIGH TO A0 INVALID	0		ns

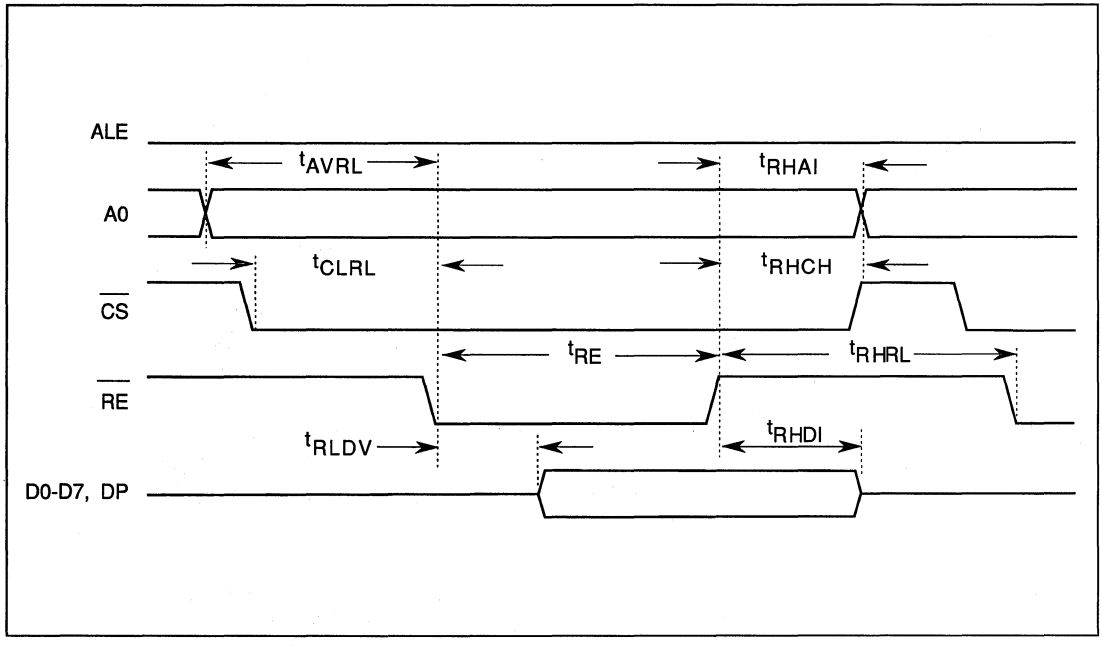


FIGURE 6-4. PROCESSOR READ TIMING

6.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALUE TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talwl	ALE LOW TO $\overline{WE}$ LOW	90		ns
tclwl	$\overline{CS}$ LOW TO $\overline{WE}$ LOW	0		ns
twe	$\overline{CS}$ LOW, TO $\overline{WE}$ LOW TIME	120		ns
tdvwh	DATA VALID TO $\overline{WE}$ HIGH	70		ns
twhch	$\overline{WE}$ HIGH TO $\overline{CS}$ HIGH	-5		ns
twhdi	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
twhwl	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns
tahal	ALE HIGH TO ALE LOW	40	1000	ns

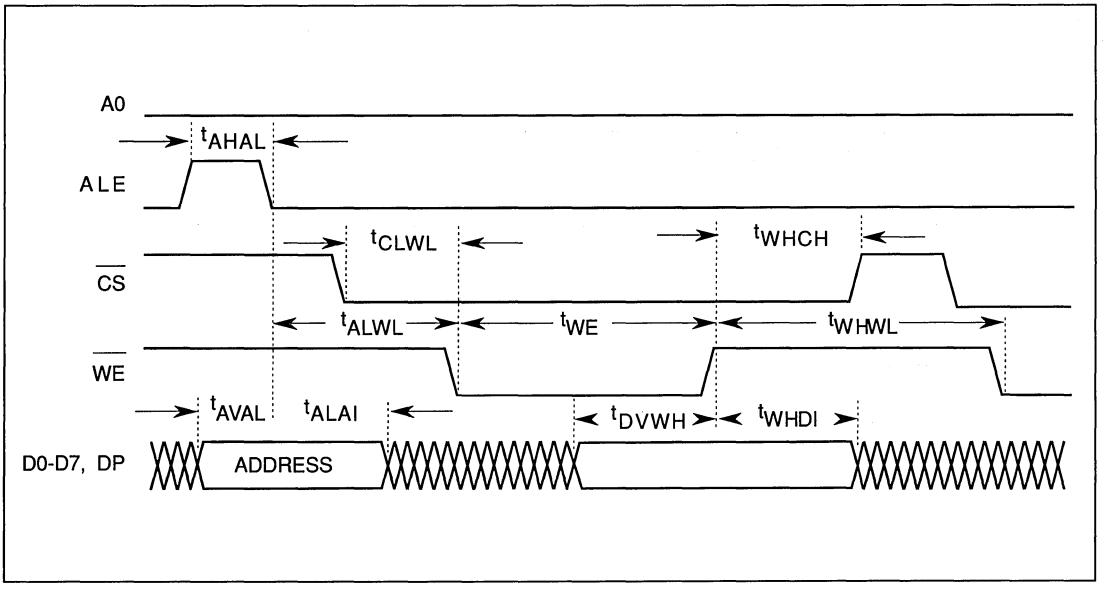


FIGURE 6-5. PROCESSOR WRITE (DIRECT) TIMING

6.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talrl	ALE LOW TO $\overline{RE}$ LOW	30		ns
tclrl	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
tre	$\overline{CS}$ LOW, $\overline{RE}$ LOW TIME	180	10000	ns
trldv	$\overline{RE}$ LOW TO DATA VALID		162	ns
trhch	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	-5		ns
trhdi	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns
trhrl	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns
tahal	ALE HIGH TO ALE LOW	40	1000	ns

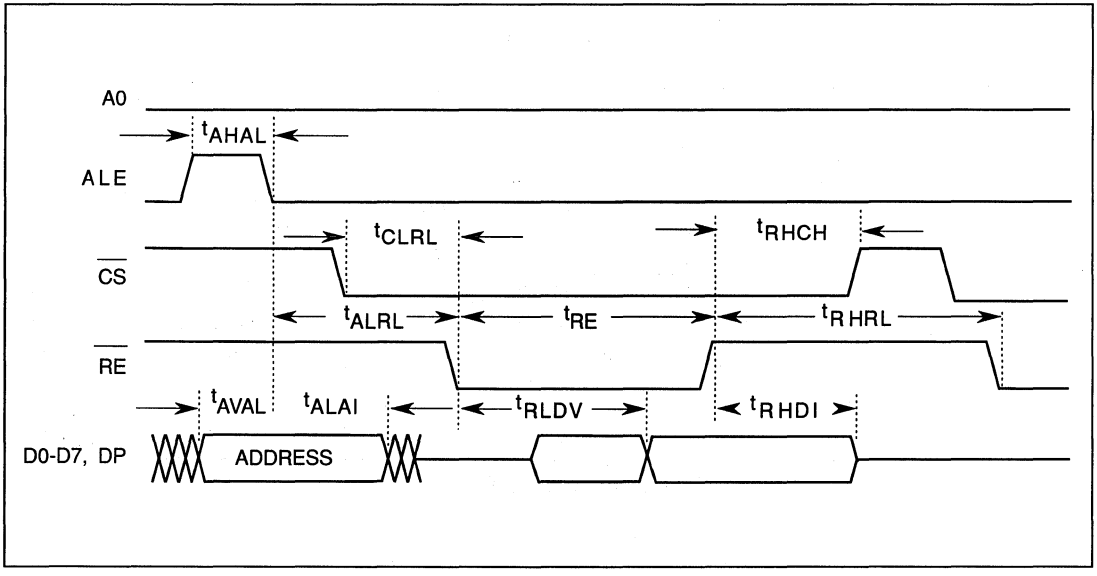


FIGURE 6-6. PROCESSOR READ (DIRECT) TIMING

6.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	$\overline{\text{DACK}}$ LOW TO $\overline{\text{WE}}$ LOW	0		ns
tdlqh	$\overline{\text{DACK}}$ LOW TO $\overline{\text{DRQ}}$ HIGH		75	ns
twr	$\overline{\text{WE}}$ PULSE WIDTH	50		ns
twhwl	$\overline{\text{WE}}$ HIGH TO $\overline{\text{WE}}$ LOW	100		ns
tdvwh	DATA VALID TO $\overline{\text{WE}}$ HIGH	25		ns
twhdh	$\overline{\text{WE}}$ HIGH TO $\overline{\text{DACK}}$ HIGH	0		ns
twhdi	$\overline{\text{WE}}$ HIGH TO DATA INVALID	0		ns
tdhql	$\overline{\text{DACK}}$ HIGH TO $\overline{\text{DRQ}}$ LOW	0		ns

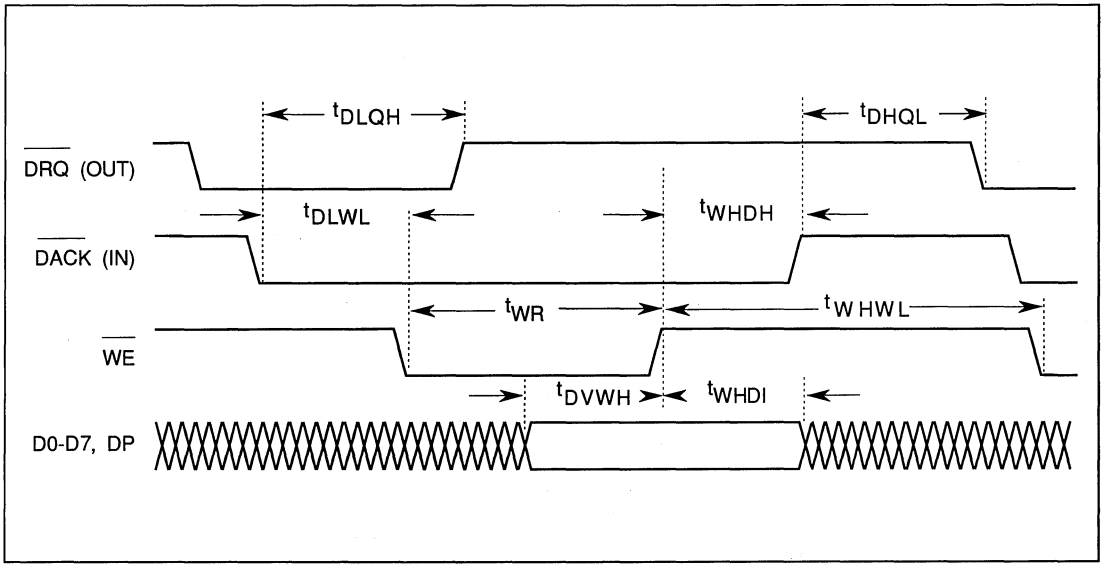


FIGURE 6-7. DMA WRITE TIMING

6.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	$\overline{\text{DACK}}$ LOW TO $\overline{\text{RE}}$ LOW	0		ns
tdlqh	$\overline{\text{DACK}}$ LOW TO $\overline{\text{DRQ}}$ HIGH		75	ns
trd	$\overline{\text{RE}}$ PULSE WIDTH	80		ns
trhrl	$\overline{\text{RE}}$ HIGH TO $\overline{\text{RE}}$ LOW	100		ns
trldv	$\overline{\text{RE}}$ LOW TO DATA VALID		70	ns
trhdh	$\overline{\text{RE}}$ HIGH TO $\overline{\text{DACK}}$ HIGH	0		ns
trhdi	$\overline{\text{RE}}$ HIGH TO DATA INVALID	5	40	ns
tdhql	$\overline{\text{DACK}}$ HIGH TO $\overline{\text{DRQ}}$ LOW	0		ns

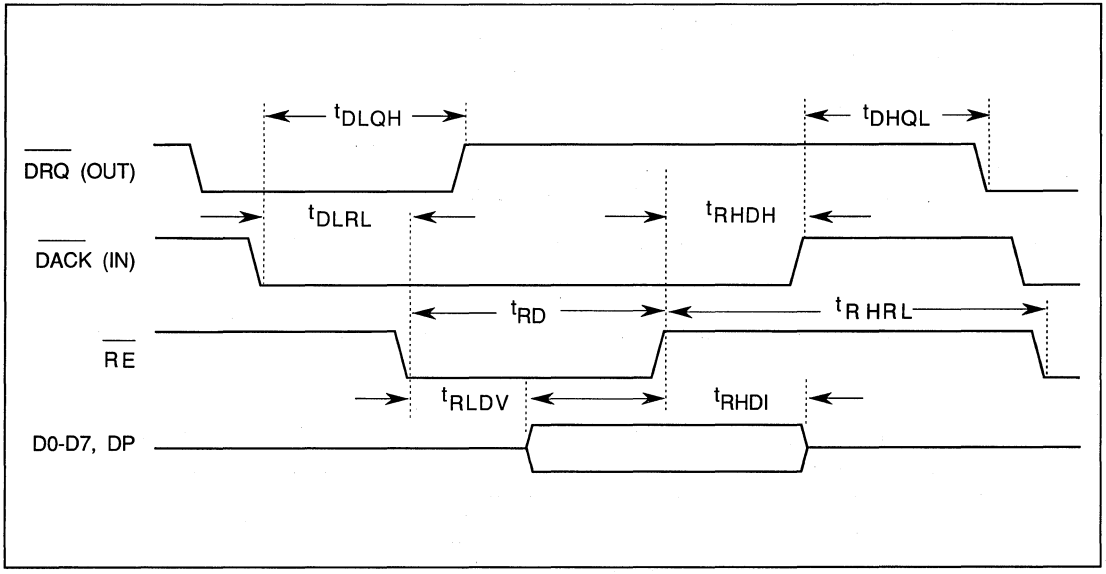


FIGURE 6-8. DMA READ TIMING

6.1.9 WD-BUS Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO $\overline{RCS}$ LOW	0	40	ns
tslwv	$\overline{RCS}$ LOW TO $\overline{WE}$ VALID	-5	20	ns
two	$\overline{WE}$ PULSE WIDTH (1)	1-10 ns		Tcyc
twhwl	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW (A)	1-10 ns		Tcyc
twldv	$\overline{WE}$ LOW TO DATA VALID		20	ns
twhdi	$\overline{WE}$ HIGH TO DATA INVALID	1-		ns
tqlsh	DRQ LOW TO $\overline{RCS}$ TRI-STATE	8	10	Tcyc
tshwi	$\overline{RCS}$ TRISTATE TO $\overline{WE}$ INVALID		100	ns
twhsh	$\overline{WE}$ HIGH TO $\overline{RCS}$ TRI-STATE	0		ns
tslwl	$\overline{RCS}$ LOW TO $\overline{WE}$ LOW	60		ns
twlql	$\overline{WE}$ LOW TO DRQ LOW (2)		55	ns
tslql	$\overline{RCS}$ LOW TO DRQ LOW (3)		75	ns

(1) Two + Twhwl = 2*Tcyc

(2) Guarantees that only one more byte will be transferred.

(3) Guarantees that only one byte will be transferred.

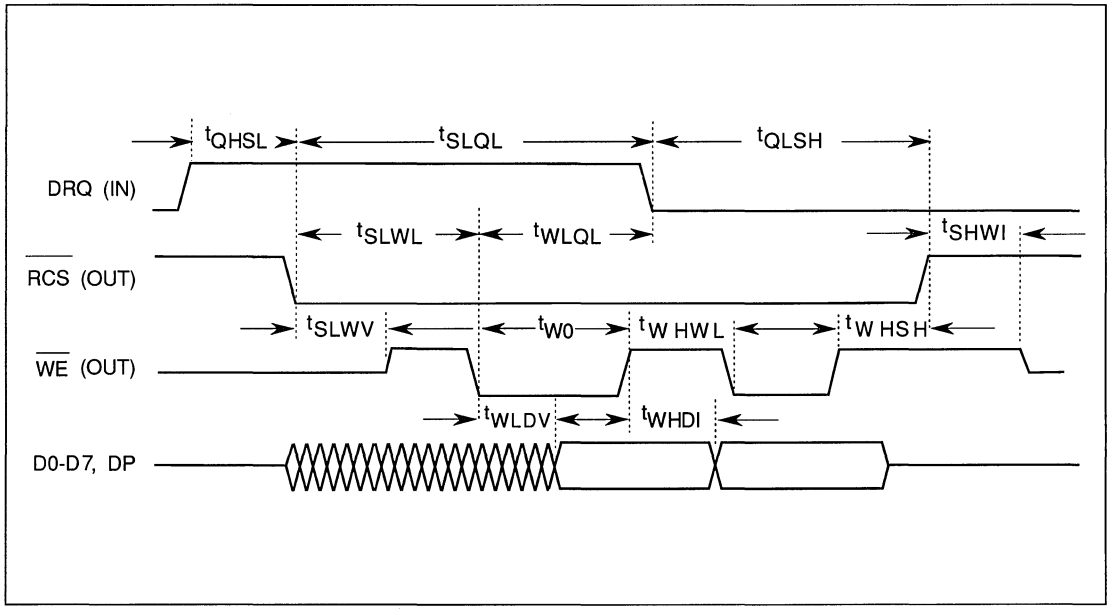


FIGURE 6-9. WD BUS BUFFER WRITE TIMING

6.1.10 WD-BUS Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO $\overline{RCS}$ LOW	0	40	ns
tslrv	$\overline{RCS}$ LOW TO $\overline{RE}$ VALID	-5	20	ns
tro	$\overline{RE}$ PULSE WIDTH (1)	1-10 ns		Tcyc
trhrl	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW (1)	1-10 ns		Tcyc
tdvrh	DATA VALID TO $\overline{RE}$ HIGH	20		ns
trhdi	$\overline{RE}$ HIGH TO DATA INVALID	0		ns
tqlsh	DRQ LOW TO $\overline{RCS}$ TRI-STATE	8	10	Tcyc
tshri	$\overline{RCS}$ TRISTATE TO $\overline{RE}$ INVALID		100	ns
trhsh	$\overline{RE}$ HIGH TO $\overline{RCS}$ TRI-STATE	0		ns
tslrl	$\overline{RCS}$ LOW TO $\overline{RE}$ LOW	60		ns
trlql	$\overline{RE}$ LOW TO DRQ LOW (2)		55	ns
tslql	$\overline{RCS}$ LOW TO DRQ LOW (3)		75	ns

(1) Tro + Trhrl = 2*Tcyc

(2) Guarantees that only one more byte will be transferred.

(3) Guarantees that only one byte will be transferred.

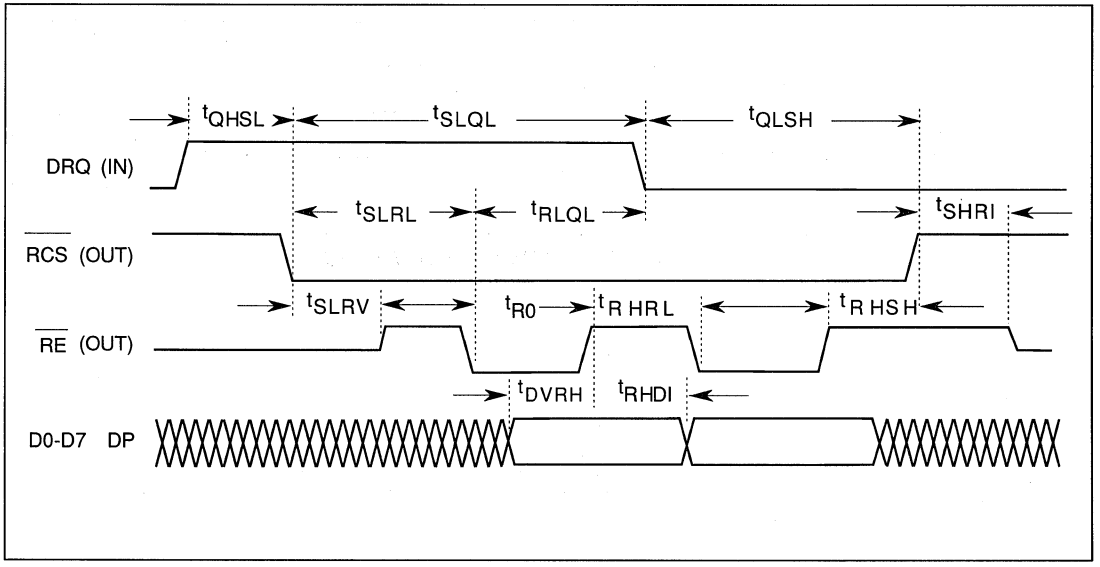


FIGURE 6-10. WD BUS BUFFER READ TIMING

6.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	$\overline{DACK}$ LOW TO $\overline{WE}$ LOW	0		ns
twlqh	$\overline{WE}$ LOW TO $\overline{DRQ}$ HIGH		50	ns
twr	$\overline{WE}$ PULSE WIDTH	30		ns
twhwl	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	30		ns
tdvwh	DATA VALID TO $\overline{WE}$ HIGH	18		ns
twhdh	$\overline{WE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
twhdi	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
tdhql	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	0		ns

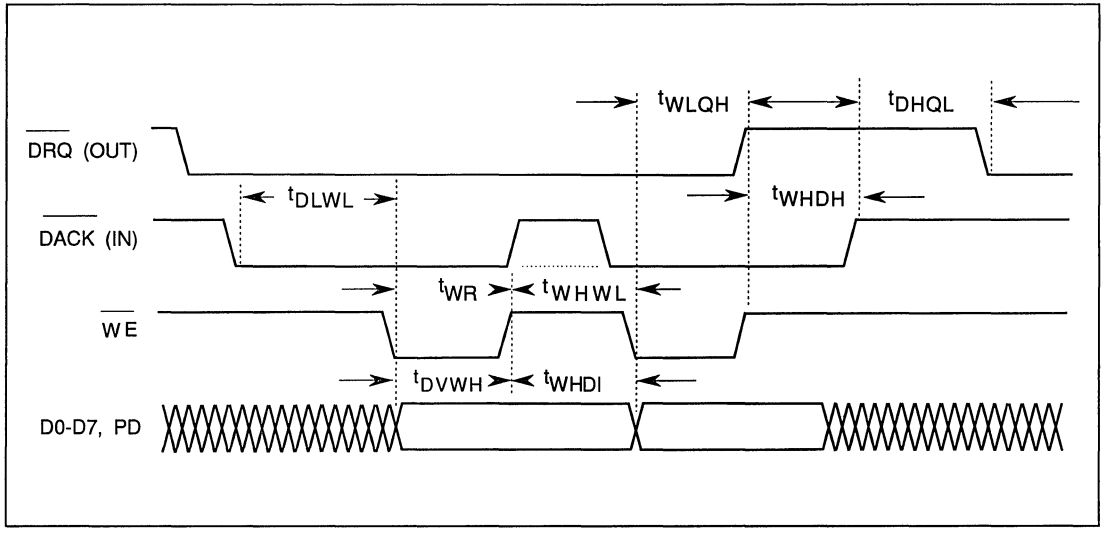


FIGURE 6-11. BURST DMA WRITE TIMING

6.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	$\overline{DACK}$ LOW TO $\overline{RE}$ LOW	0		ns
tdldv	$\overline{DACK}$ LOW TO DATA VALID	50		ns
trlqh	$\overline{RE}$ LOW TO $\overline{DRQ}$ HIGH		60	ns
trd	$\overline{RE}$ PULSE WIDTH	30		ns
trhrl	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	30		ns
trhdv	$\overline{RE}$ HIGH TO DATA VALID		80	ns
trhdh	$\overline{RE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
trhdi	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns
tdhql	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	0		ns

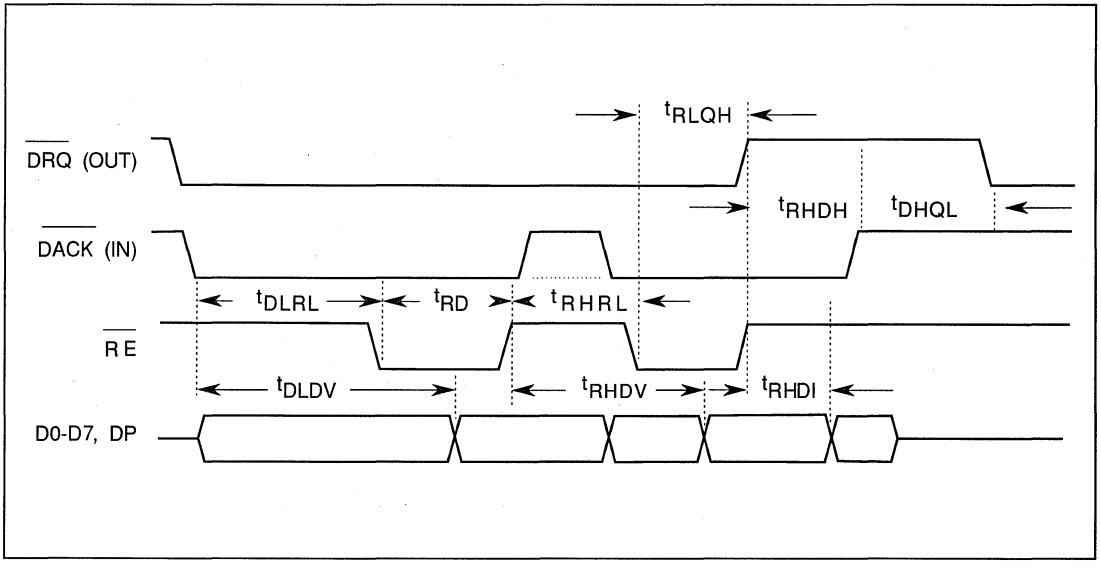


FIGURE 6-12. BURST DMA READ TIMING

6.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ HIGH TO $\overline{RE}$ LOW	0		ns
tri	$\overline{RE}$ PULSE WIDTH	180		ns
trhil	$\overline{RE}$ HIGH TO INTRQ LOW	0	100	ns
tilih	INTRQ LOW TO INTRQ HIGH	100		ns

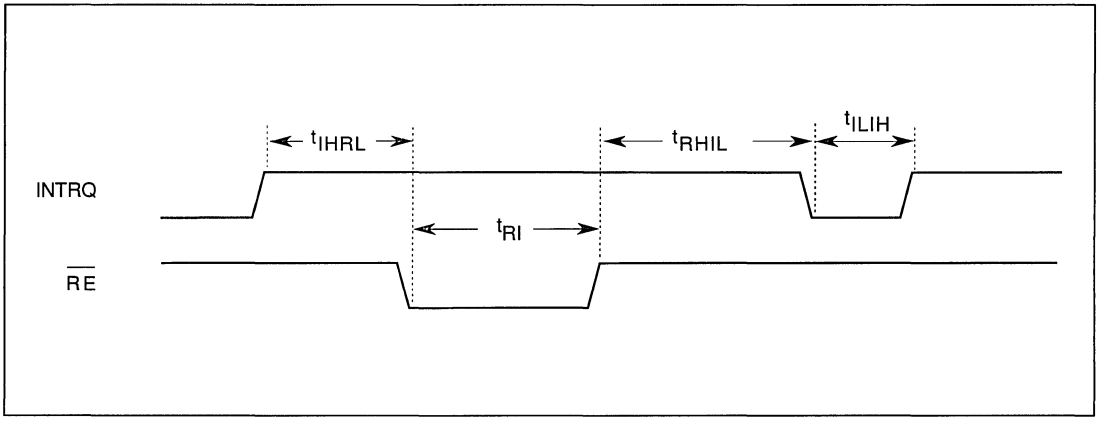


FIGURE 6-13. INTRQ TIMING

6.2 SCSI INTERFACE

6.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhbl	$\overline{BSY}$, $\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT LOW	12	16	cyc
tblio	$\overline{BSY}$ OUT LOW TO BUS ID OUT	-50	50	ns
tblsl	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ OUT LOW	2.2		us

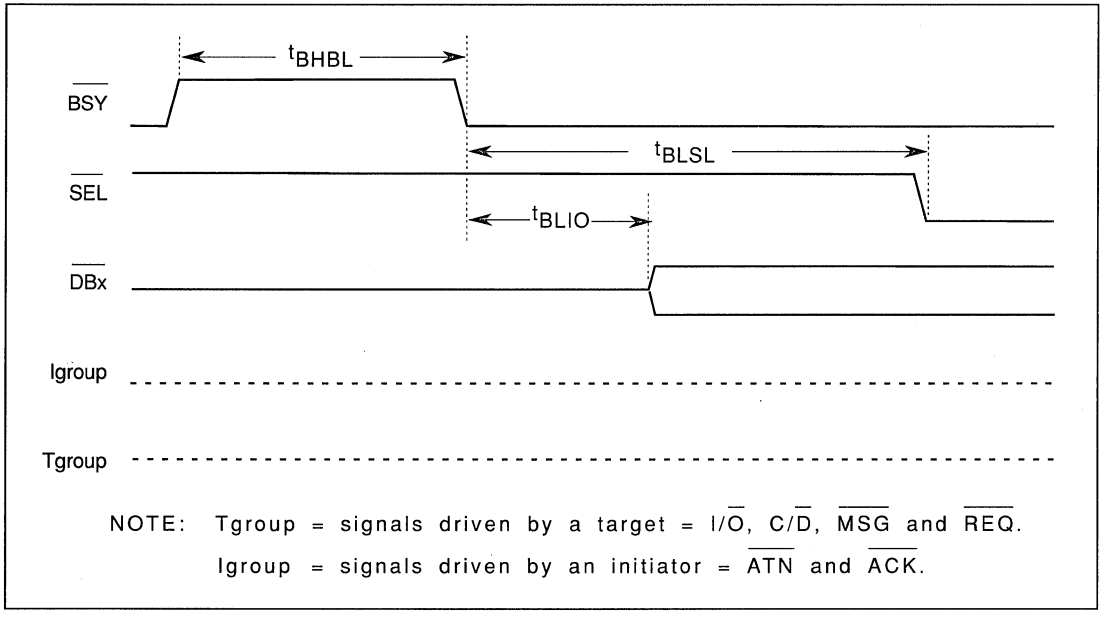


FIGURE 6-14. ARBITRATION TIMING

6.2.2 Selecting A Target (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	SEL- OUT LOW TO "OR-ED" ID OUT	1.2		us
tovao	"OR-ED" ID OUT VALID TO ACK , ATN OUT	100		ns
taobh	ACK , ATN OUT VALID TO BSY OUT HIGH	100		ns
tbhbv	BSY OUT HIGH TO BSY IN LOW VALID	400		ns
tblsh	BSY IN LOW TO SEL OUT HIGH	100		ns

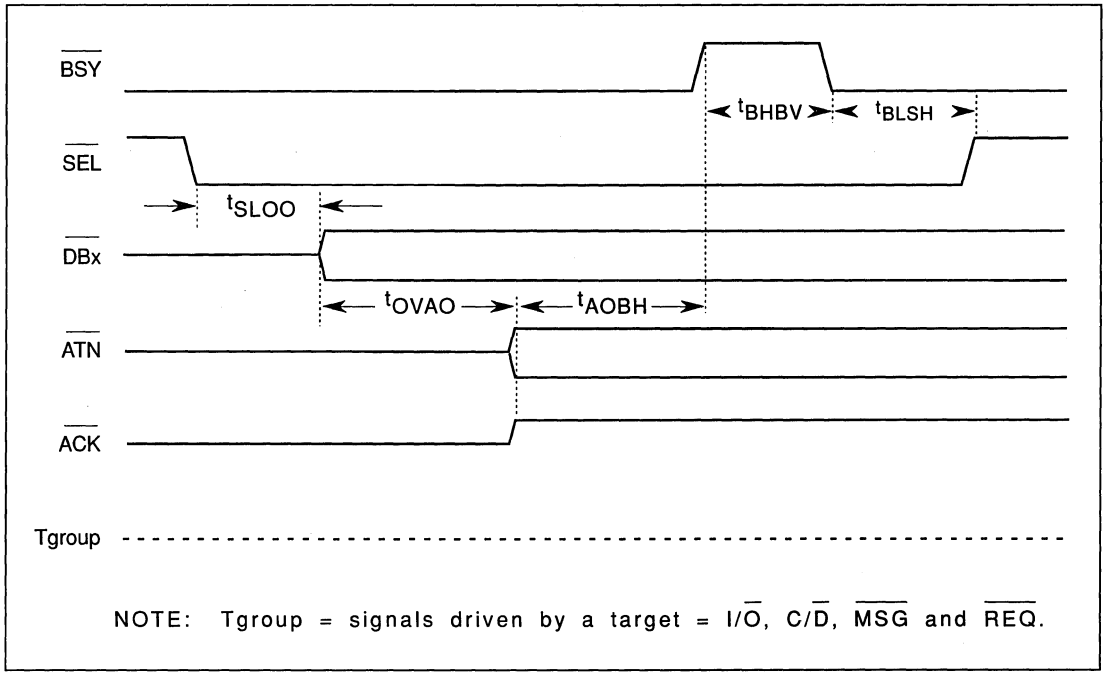
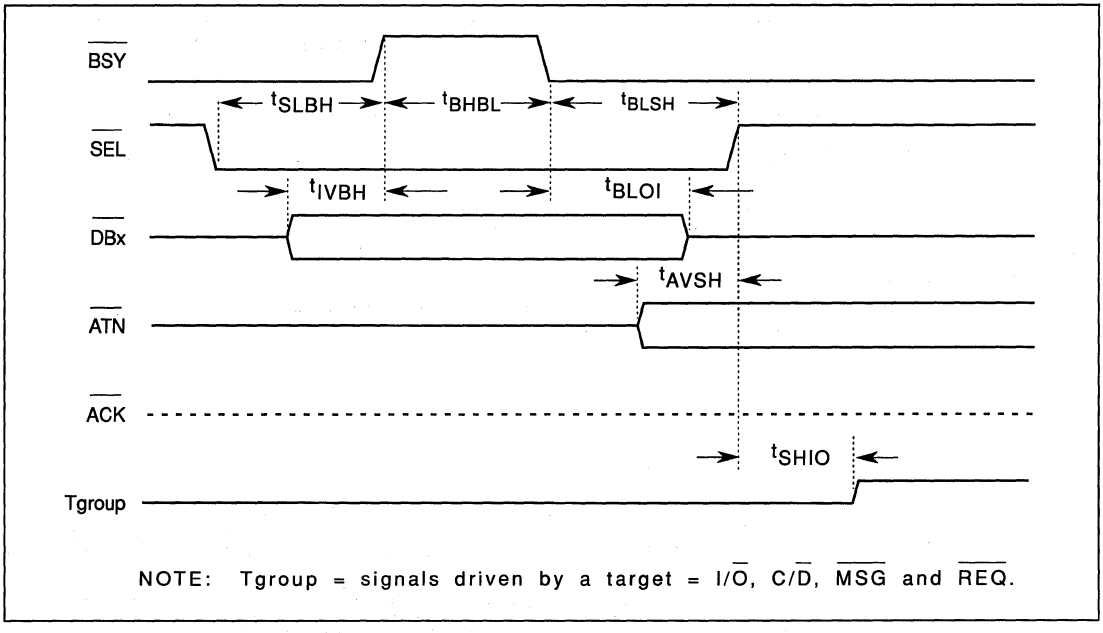


FIGURE 6-15. TIMING-INITIATOR SELECTING A TARGET

6.2.3 Response To Selection (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
tivbh	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
tbhbl	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO $\overline{BSY}$ OUT LOW	0.4	200	us
tbloi	$\overline{BSY}$ OUT LOW TO "OR-ED" ID INVALID IN	0		ns
tblsh	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
tavsh	$\overline{ATN}$ VALID IN TO $\overline{SEL}$ IN HIGH	0		ns
tshio	$\overline{SEL}$ IN HIGH TO Tgroup OUT	100		ns

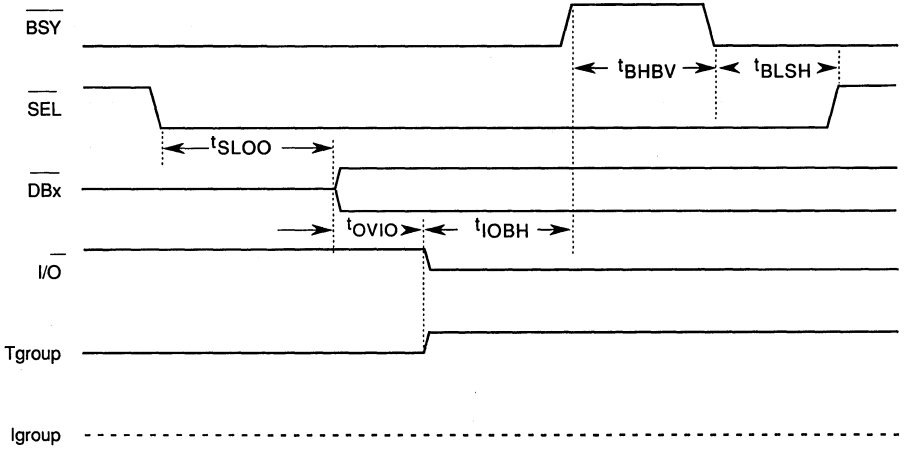


NOTE: Tgroup = signals driven by a target = I/$\overline{O}$, C/$\overline{D}$, $\overline{MSG}$ and $\overline{REQ}$.

FIGURE 6-16. TIMING-TARGET RESPONSE

6.2.4 Reselecting An Initiator (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	$\overline{SEL}$ OUT LOW TO "OR-ED" ID OUT	1.2		us
tovio	"OR-ED" ID OUT VALID TO I/O AND Tgroup OUT VALID	100		ns
tiobh	I/O AND Tgroup OUT VALID TO $\overline{BSY}$ OUT HIGH	100		ns
tbhbv	$\overline{BSY}$ OUT HIGH TO $\overline{BSY}$ IN LOW VALID	400		ns
tblsh	$\overline{BSY}$ IN LOW TO $\overline{SEL}$ OUT HIGH	100		ns

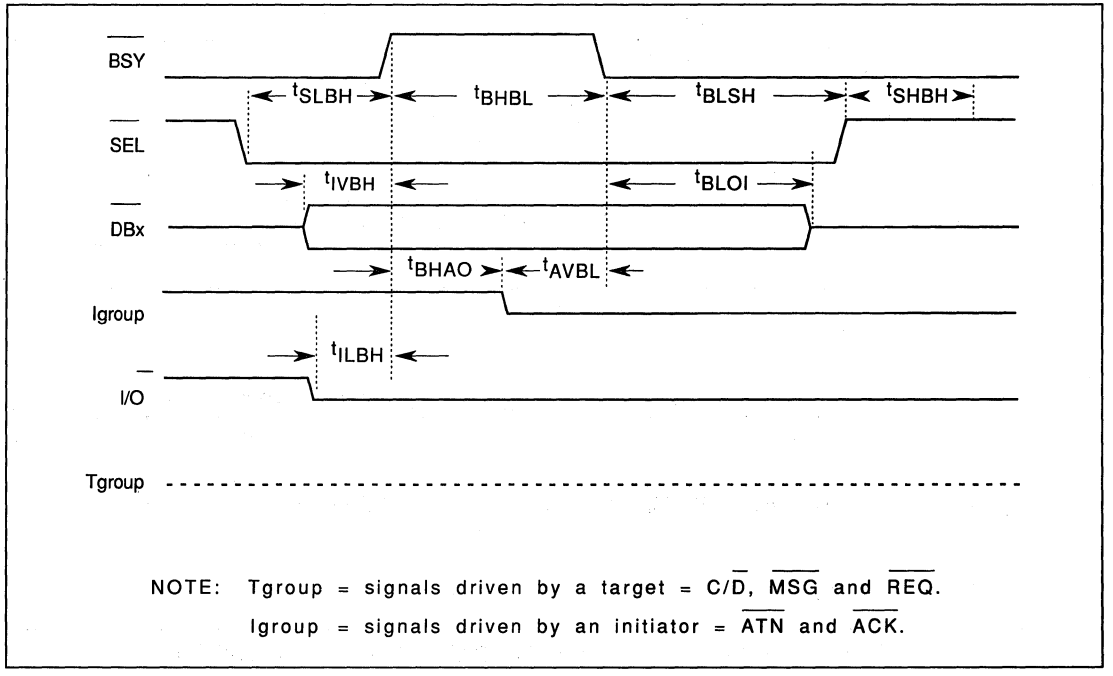


NOTE: Tgroup = signals driven by a target = C/$\overline{D}$, $\overline{MSG}$ and $\overline{REQ}$.
Igroup = signals driven by an initiator = $\overline{ATN}$ and $\overline{ACK}$.

FIGURE 6-17. TIMING-RESELECTING A TARGET

6.2.5 Response To Reselection (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
tivbh	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
tilbh	I/I- IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
tbhao	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO Igroup OUT	100		ns
tavbl	Igroup VALID OUT TO $\overline{BSY}$ OUT LOW	100		ns
tbhbl	$\overline{BSY}$ IN HIGH TO $\overline{BSY}$ OUT LOW	0.4	200	ns
tbloi	$\overline{BSY}$ OUT LOW TO "OR-ED" ID INVALID IN	0		ns
tblsh	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
tshbh	$\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT HIGH	0		ns

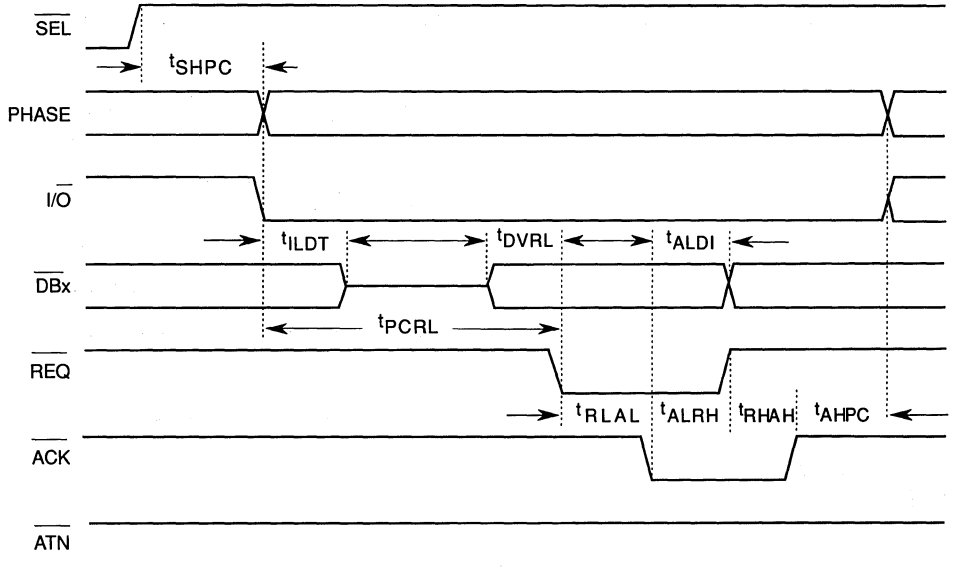


NOTE: Tgroup = signals driven by a target = $\overline{C/D}$, $\overline{MSG}$ and $\overline{REQ}$.
Igroup = signals driven by an initiator = $\overline{ATN}$ and $\overline{ACK}$.

FIGURE 6-18. TIMING-RESELECTION AS INITIATOR

6.2.6 Receive Asynchronous Information Transfer In (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
tildt	$\overline{I/O}$ IN LOW TO DATA BUS TRI-STATE	0	125	ns
tpcrl	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
tdvrl	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
trlal	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
tadli	$\overline{ACK}$ OUT LOW TO DATA INVALID IN	0		ns
talrh	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
trhah	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
tahpc	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns



NOTE: Phase = signals that define the bus = $\overline{C/D}$ and $\overline{MSG}$

FIGURE 6-19. TIMING-ASYNCHRONOUS TRANSFER IN AS INITIATOR

6.2.7 Send Asynchronous Information Transfer In (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
tildo	$\overline{I/O}$ OUT LOW TO DATA OUT	800		ns
tdvrl	DATA OUT VALID TO $\overline{REQ}$ OUT LOW	55		ns
tpcrl	PHASE CHANGE OUT TO $\overline{REQ}$ OUT LOW	500		ns
trlal	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
talrh	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
taldi	$\overline{ACK}$ IN LOW TO DATA OUT INVALID	0		ns
trhah	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
tahpc	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	100		ns
tahrl	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns

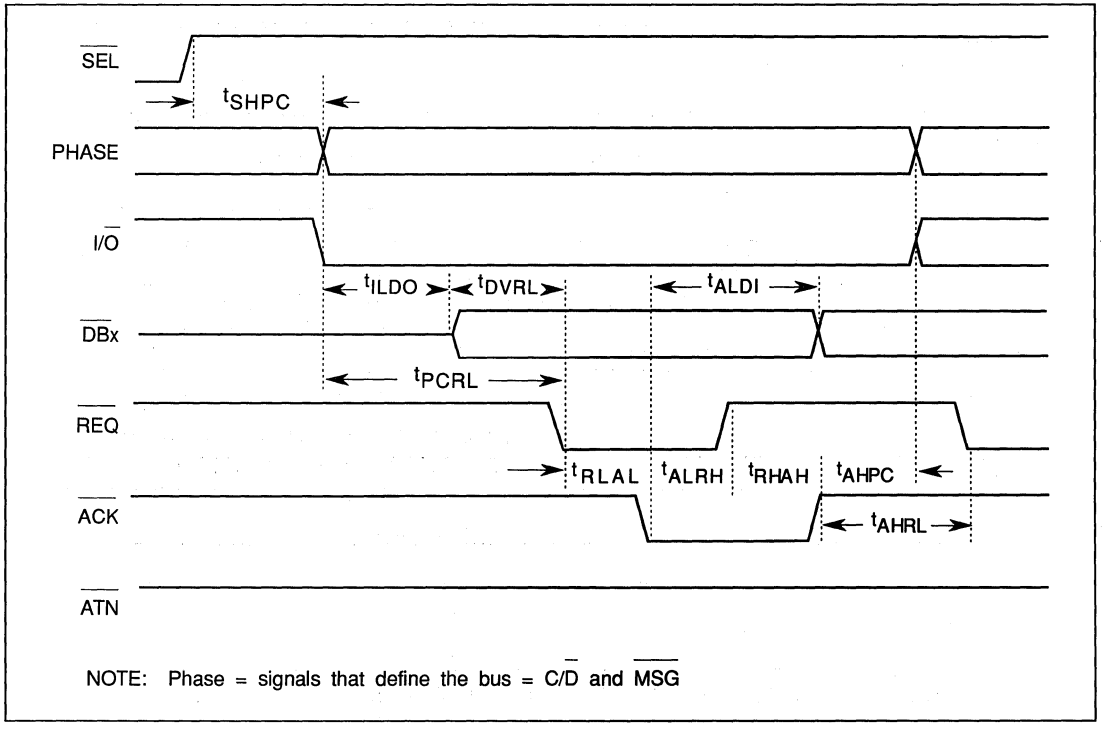
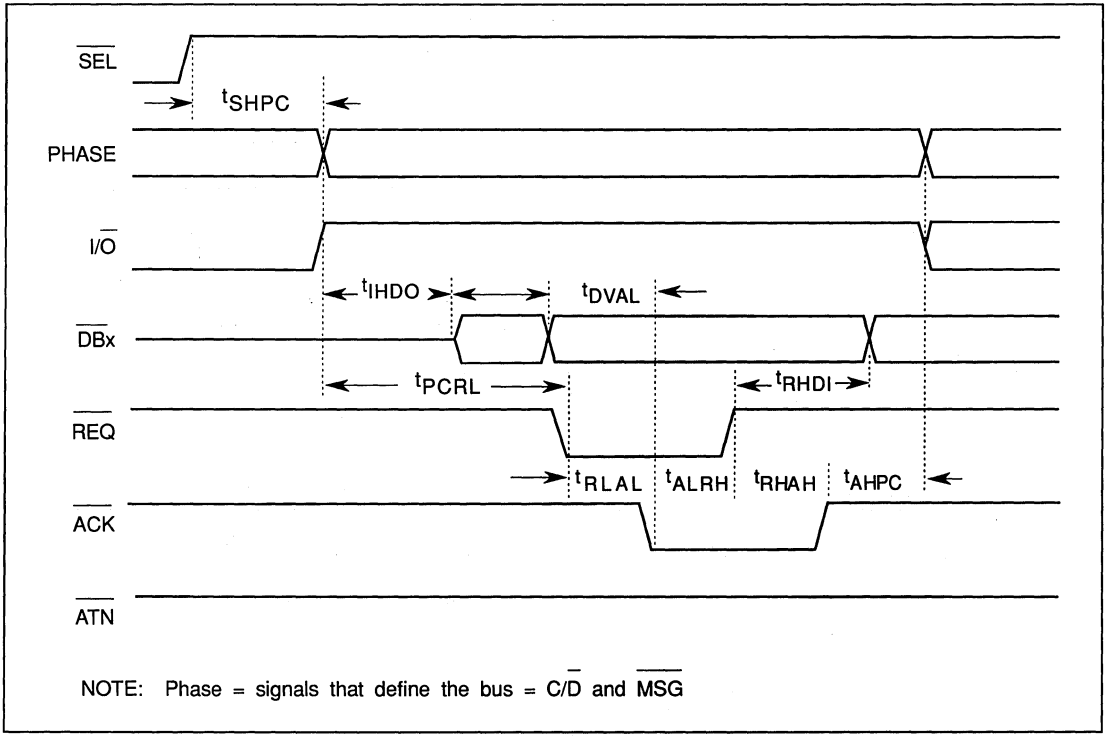


FIGURE 6-20. TIMING-ASYNCHRONOUS TRANSFER IN AS TARGET

6.2.8 Send Asynchronous Information Transfer Out (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
tihdo	$\overline{I/O}$ IN HIGH TO DATA OUT	0		ns
tpcrl	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
trlal	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
tdval	DATA OUT VALID TO $\overline{ACK}$ OUT LOW	55		ns
talrh	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
trhah	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
trhdi	$\overline{REQ}$ IN HIGH TO DATA OUT INVALID	0		ns
tahpc	$\overline{ACK}$ OUT HIGH TO PHASE IN CHANGE	0		ns



NOTE: Phase = signals that define the bus = C/D and MSG

FIGURE 6-21. TIMING-ASYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.9 Receive Asynchronous Information Transfer Out (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
tihdt	$\overline{I/O}$ OUT HIGH TO DATA BUS TRISTATE		0	ns
tpcrl	PHASE CHANGE TO $\overline{REQ}$ OUT LOW	500		ns
trlal	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
tdval	DATA IN VALID TO $\overline{ACK}$ IN LOW	0		ns
talrh	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
trhdi	$\overline{REQ}$ OUT HIGH TO DATA IN INVALID	0		ns
trhah	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
tahpc	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns
tahrl	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns

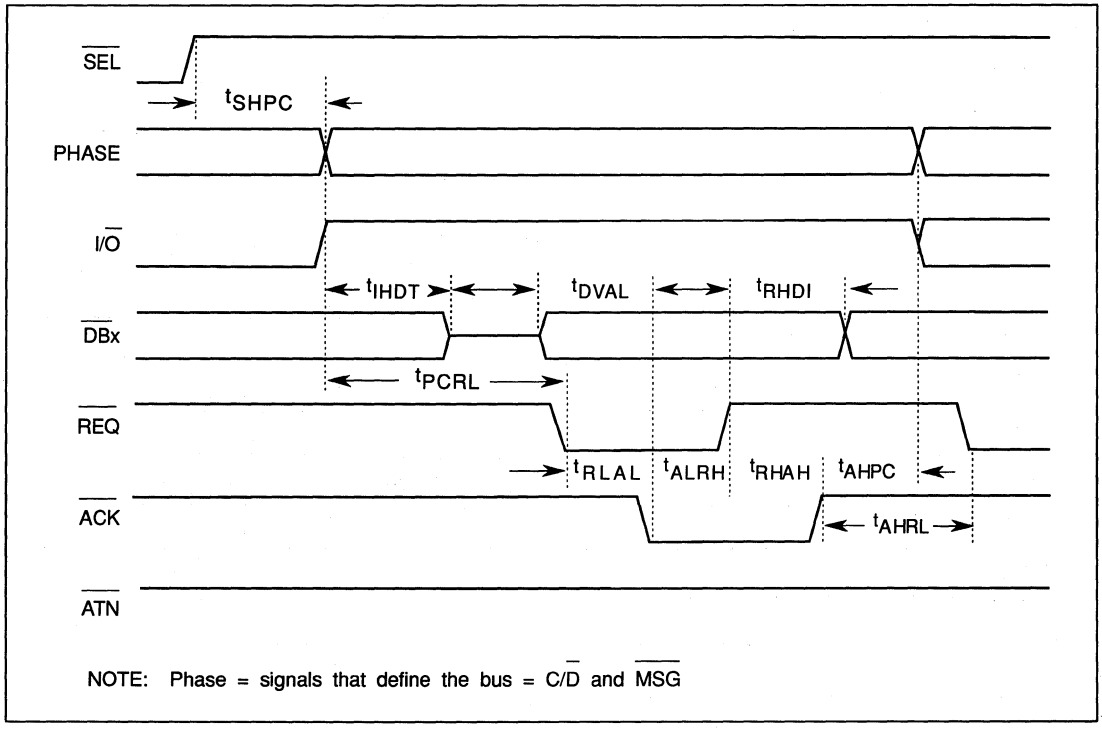


FIG.6-22. TIMING-RECEIVE ASYNCHRONOUS TRANSFER OUT AS TARGET

6.2.10 Receive Synchronous Information Transfer In (5 and 10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
trldi	$\overline{REQ}$ IN LOW TO DATA INVALID	30		ns
trcyc	$\overline{REQ}$ IN CYCLE TIME	100		ns
trlrh	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	30		ns
trhrl	$\overline{REQ}$ IN HIGH TO $\overline{REQ}$ IN LOW	30		ns
talah	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.6.

(1) Tahal + Talah = 2*Tcyc

23

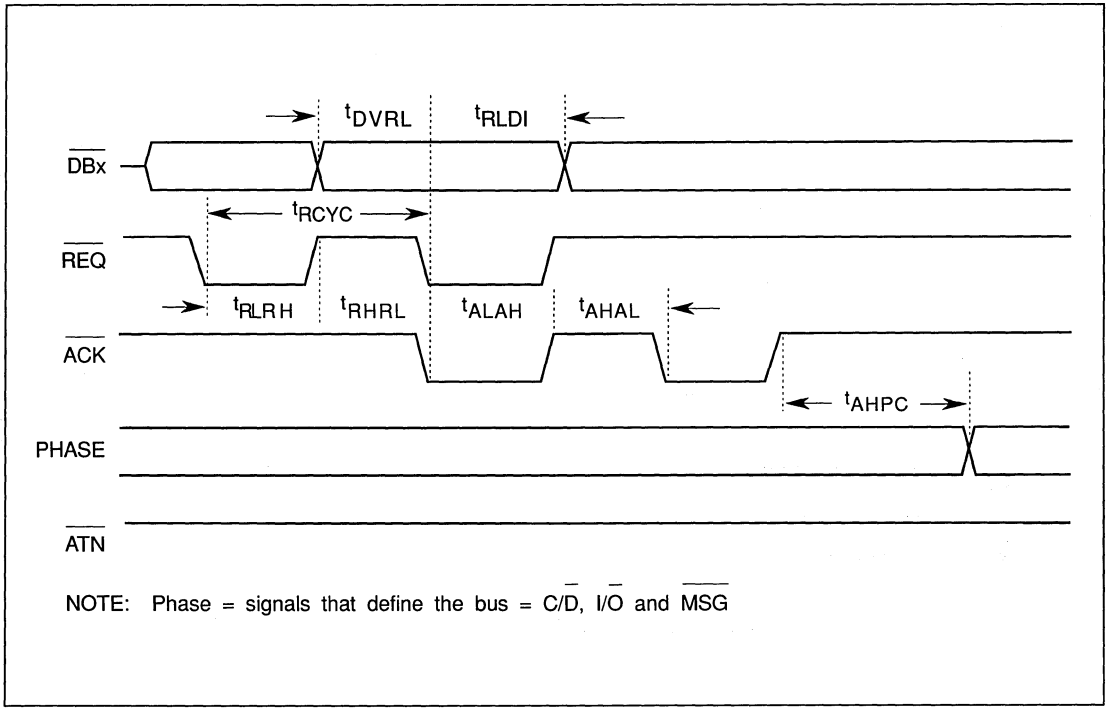


FIG.6-23.TIMING-RECEIVE SYNCHRONOUS TRANSFER IS AN INITIATOR

6.2.11a Send Synchronous Information Transfer In (5 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID OUT TO $\overline{REQ}$ OUT LOW	55		ns
trldi	$\overline{REQ}$ OUT LOW TO DATA INVALID	100		ns
trlrh	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ OUT HIGH TO REQ- OUT LOW (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ IN CYCLE TIME	200		ns
talah	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	50		ns
tahal	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	50		ns
tahpc	$\overline{ACK}$ IN HIGH TO PHAS CHANGE OUT	0		ns

PARAMETERS tshpc, tildo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.7.

(1) Trhrl + Trlrh = 2*Tcyc

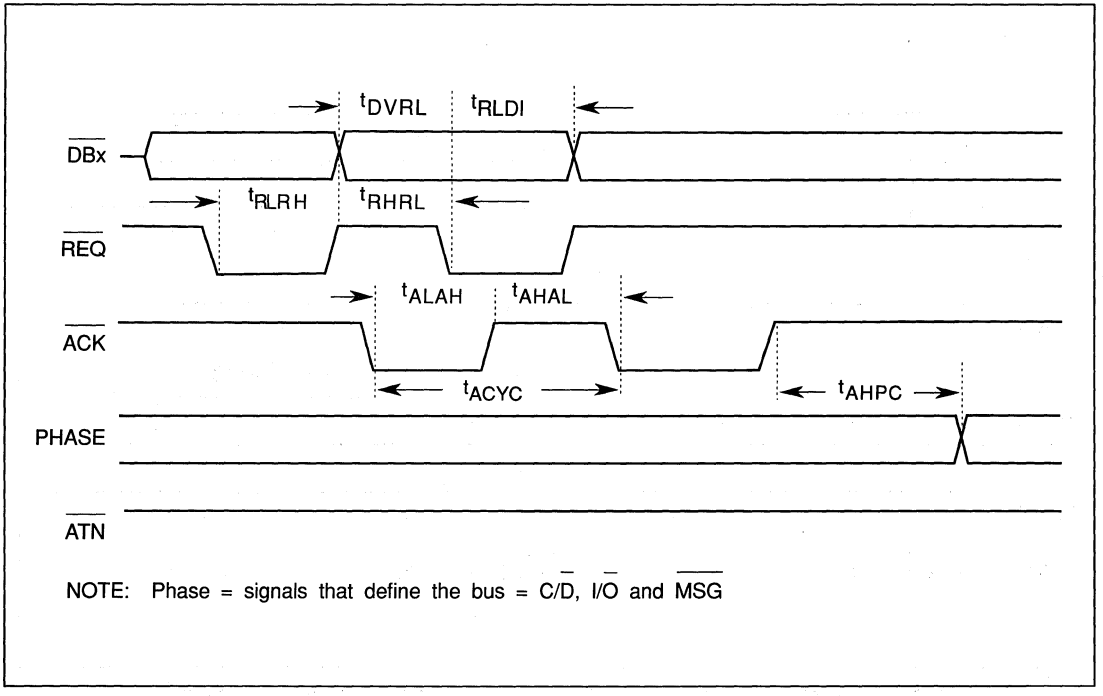


FIGURE 6-24. TIMING-SEND SYNCHRONOUS TRANSFER IN AS TARGET

6.2.11b Send Synchronous Information Transfer In (10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID OUT TO $\overline{REQ}$ OUT LOW	25		ns
rtrldi	$\overline{REQ}$ OUT LOW TO DATA INVALIF	35		ns
trlrh	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ IN CYCLE TIME	100		ns
talah	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	30		ns
tahal	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	30		ns
tahpc	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tildo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.7.

(1) Trhrl + Trlrh = 2*Tcyc

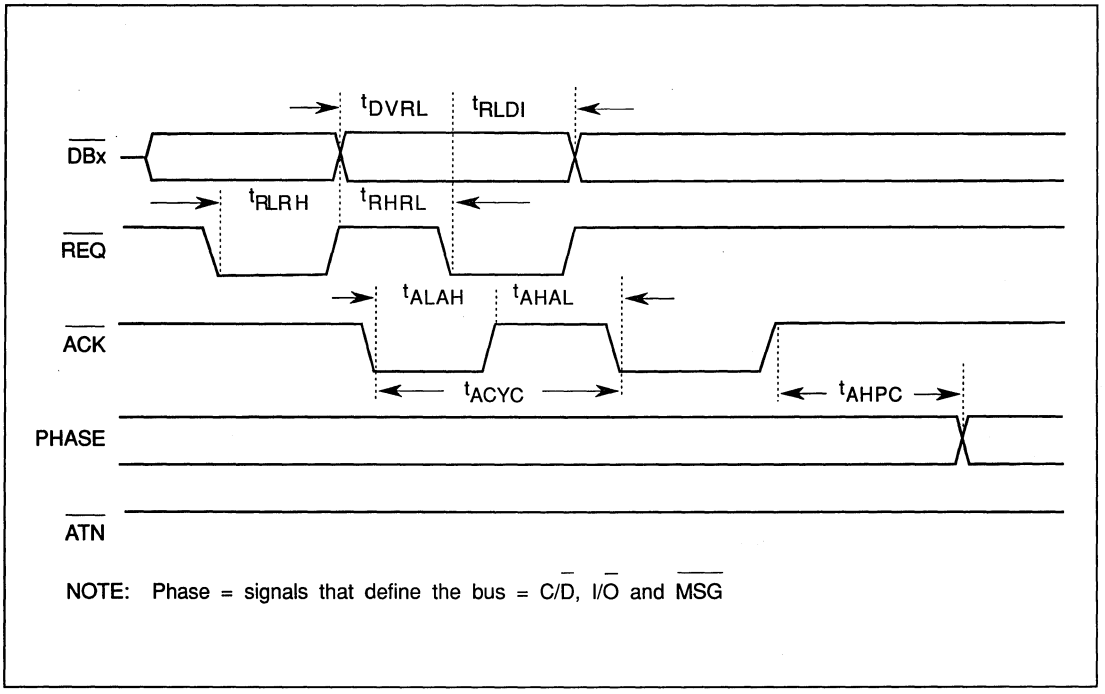


FIGURE 6-25. TIMING-SEND SYNCHRONOUS TRANSFER IN AS TARGET

6.2.12a Send Synchronous Information Transfer Out (5 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID OUT TO $\overline{ACK}$ OUT LOW	55		ns
taldi	$\overline{ACK}$ OUT LOW TO DATA INVALID	100		ns
trcyc	$\overline{REQ}$ IN CYCLE TIME	200		ns
trlrh	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	50		ns
trhrl	$\overline{REQ}$ IN HIGH TO $\overline{REQ}$ IN LOW	50		ns
talah	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns

PARAMETERS tshpc, tihdo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.8.

(1) Tahal + Talah = 2*Tcyc

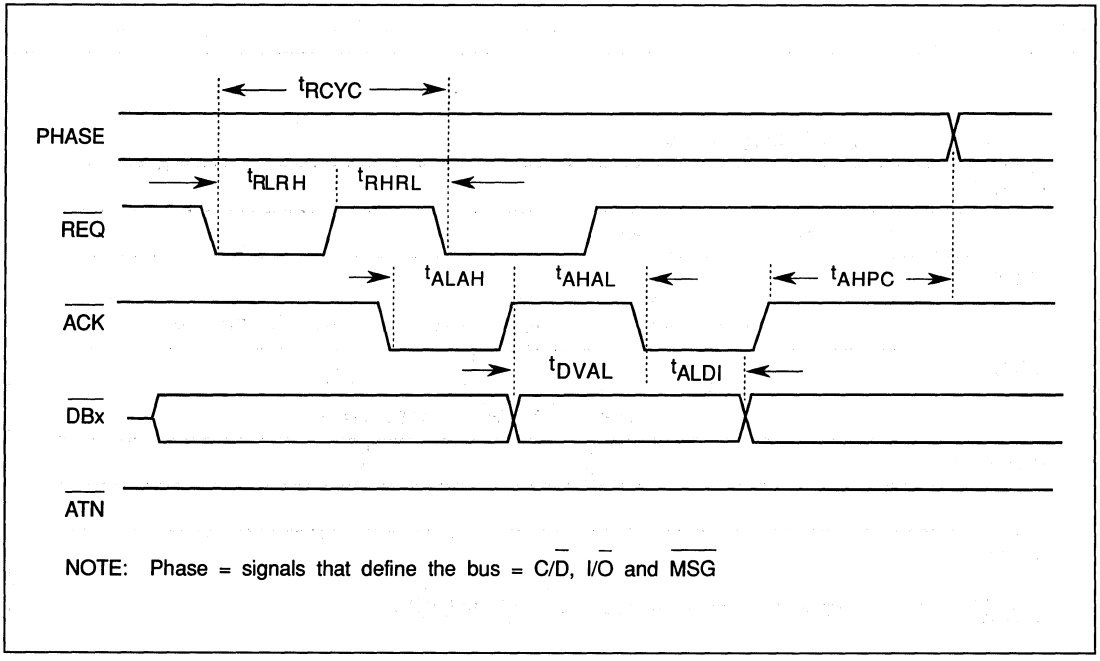


FIG. 6-26. TIMING-SEND SYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.12b Send Synchronous Information Transfer Out (10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID OUT TO $\overline{ACK}$ OUT LOW	25		ns
taldi	$\overline{ACK}$ OUT LOW TO DATA INVALID	35		ns
trcyc	$\overline{REQ}$ IN CYCLE TIME	100		ns
trlrh	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	30		ns
trhrl	$\overline{REQ}$ IN HIGH TO $\overline{REQ}$ IN LOW	30		ns
talah	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH (1)	1-10 ns		Tcyc
tahal	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW (1)	1-10 ns		Tcyc
tahpc	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns

PARAMETERS tshpc, tihdo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.8.

(1) Tahal + Talah = 2*Tcyc

23

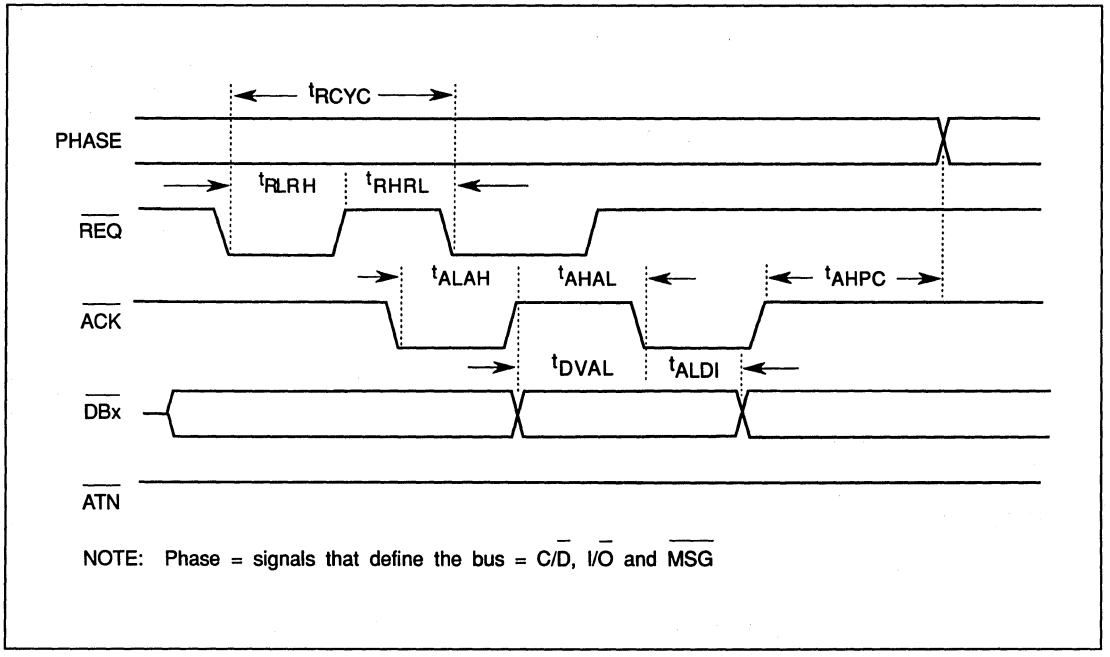


FIG. 6-27. TIMING-SEND SYNCHRONOUS TRANSFER OUT AS INITIATOR

6.2.13 Receive Synchronous Information Transfer Out (5 and 10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID IN TO $\overline{ACK}$ IN LOW	0		ns
taldi	$\overline{ACK}$ IN LOW TO DATA INVALID	30		ns
trlrh	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH (1)	1-10 ns		Tcyc
trhrl	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW (1)	1-10 ns		Tcyc
tacyc	$\overline{ACK}$ IN CYCLE TIME	100		ns
talah	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	30		ns
tahal	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	30		ns
tahpc	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tihdt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.9.

(1) Trhrl + Trlrh = 2*Tcyc

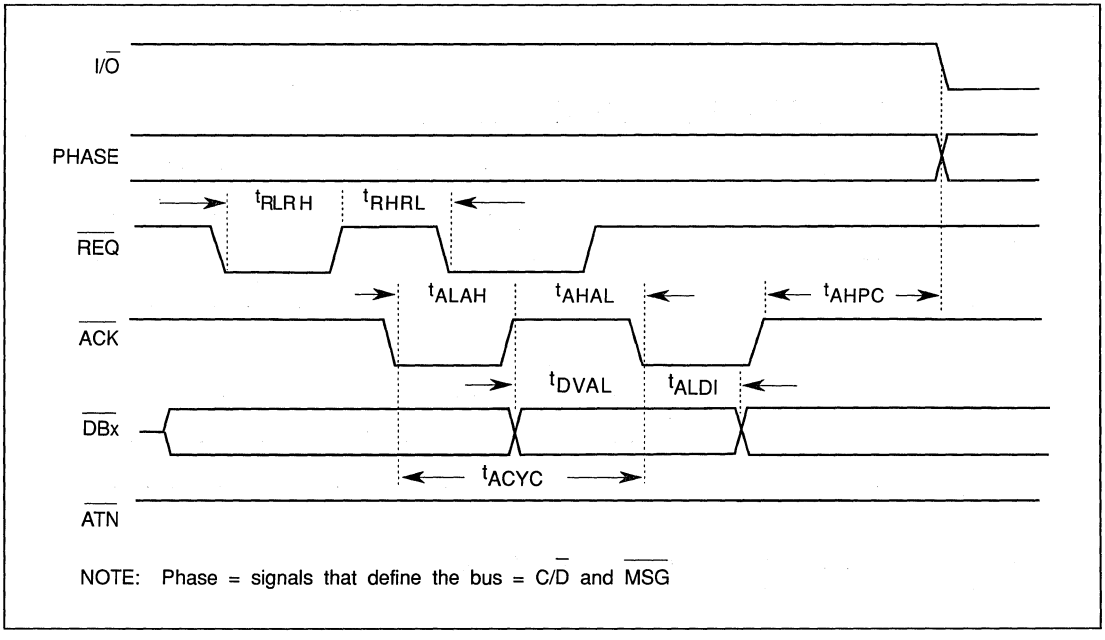


FIG. 6-28. TIMING-RECEIVE SYNCHRONOUS TRANSFER OUT AS TARGET

6.2.14 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ HIGH, DATA TRI-STATE		6+50 ns	Tcyc

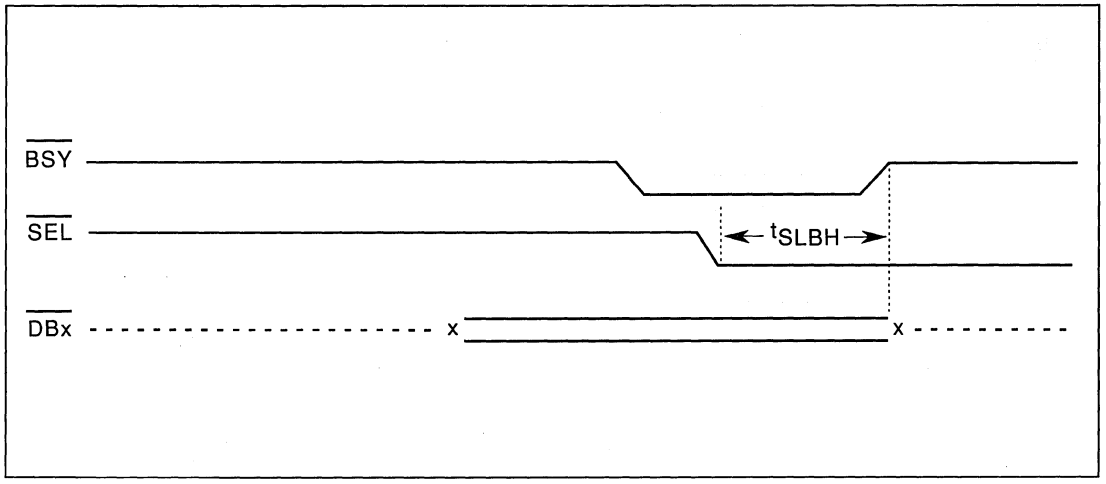


FIGURE 6-29. ARBITRATION TO BUS FREE TIMING

6.2.15 Selection (As An Initiator) Or Reselection (As A Target) To Bus Free (Selection Timeout)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	TIMEOUT OR ABORT TO DATA BUS CLEARED	0		ns
tdcsh	DATA BUS CLEARED TO $\overline{SEL}$ OUT HIGH	201		us
tshdt	$\overline{SEL}$ OUT HIGH TO DATA BUS TRI-STATE		800	ns
tshih	$\overline{SEL}$ OUT HIGH TO cntl TRI-STATE		800	ns

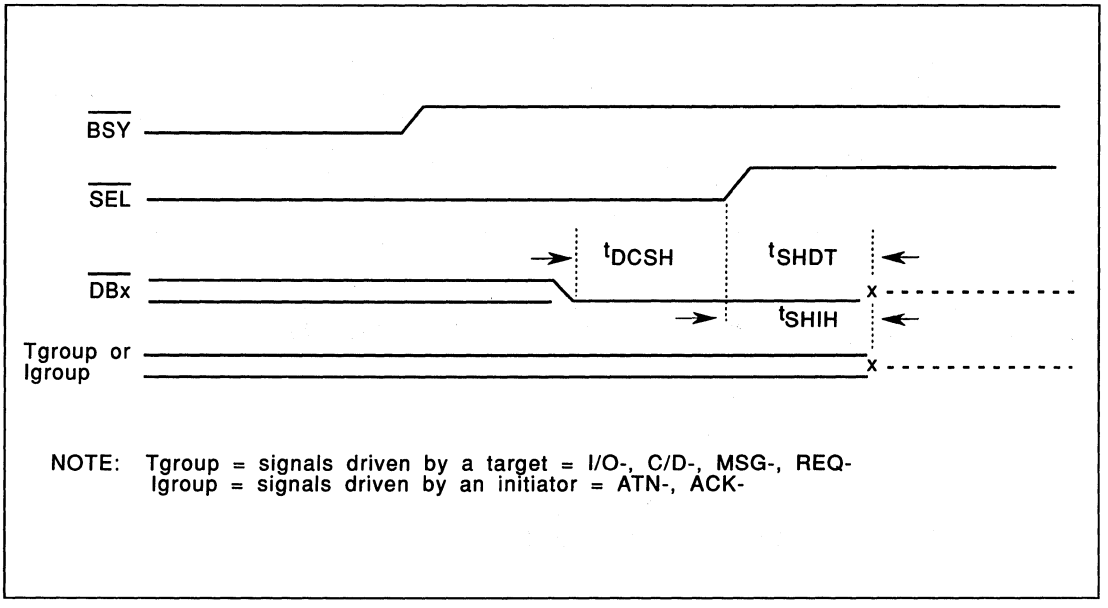


FIGURE 6-30. TIMING-SELECTION TO BUS FREE

6.2.16 Connected-As-An-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	$\overline{BSY}$ IN HIGH TO DATA BUS TRI-STATE		8+75 ns	Tcyc
tbhgt	$\overline{BSY}$ IN HIGH TO Igroup TRI-STATE		8+75 ns	Tcyc

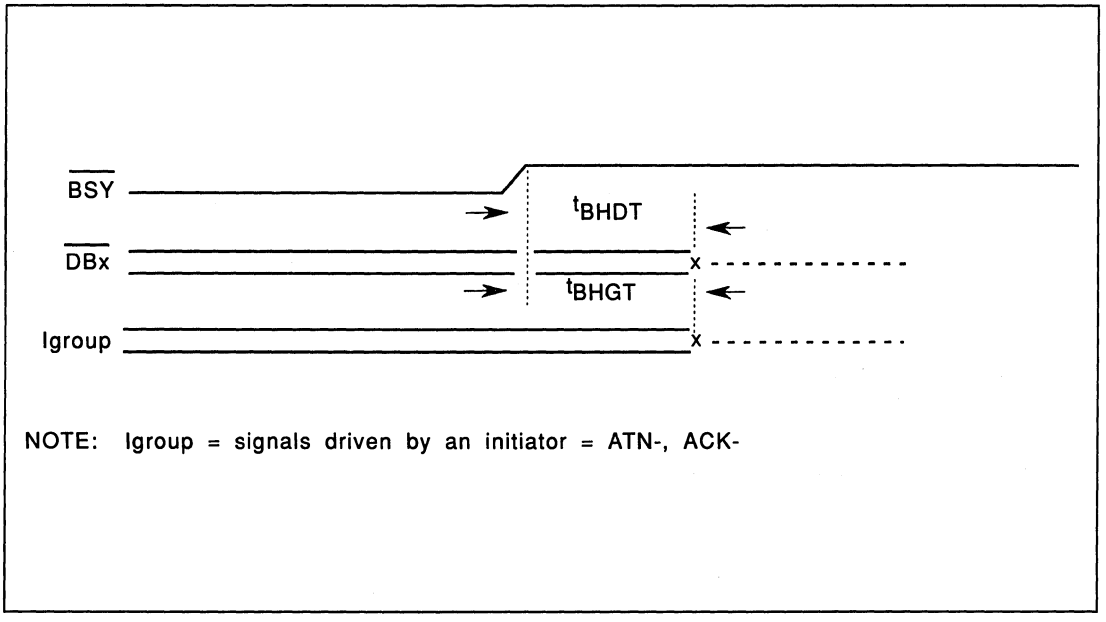


FIGURE 6-31. TIMING-INITIATOR TO BUS FREE

6.2.17 Connected-As-A-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	$\overline{BSY}$ OUT HIGH TO DATA BUS TRI-STATE		8+75 ns	Tcyc
tbhgt	$\overline{BSY}$ OUT HIGH TO Tgroup TRI-STATE		8+75 ns	Tcyc

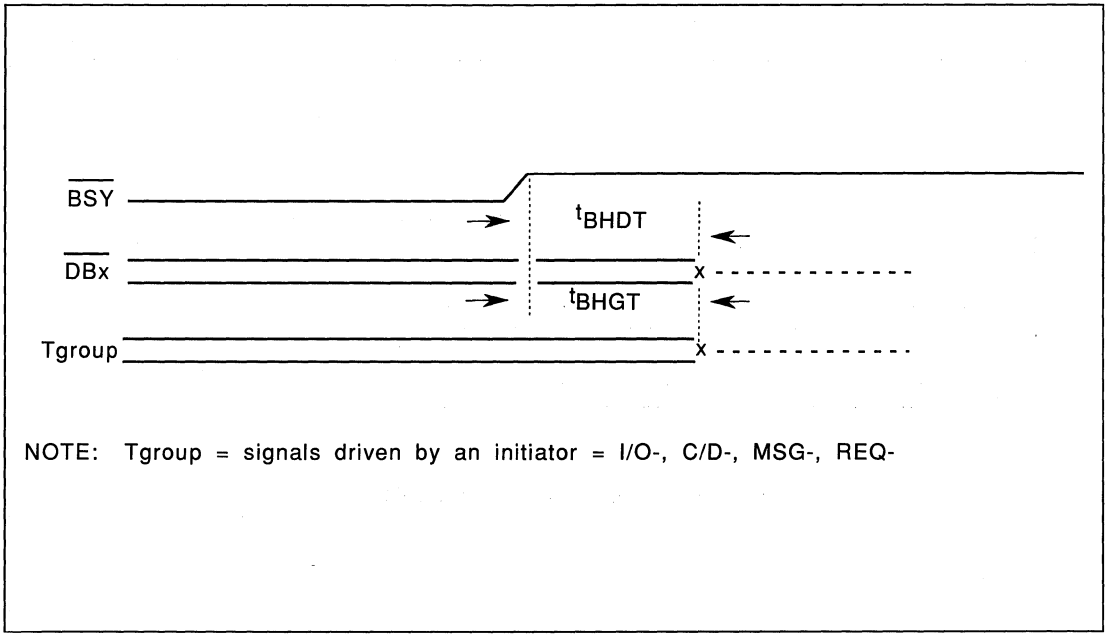
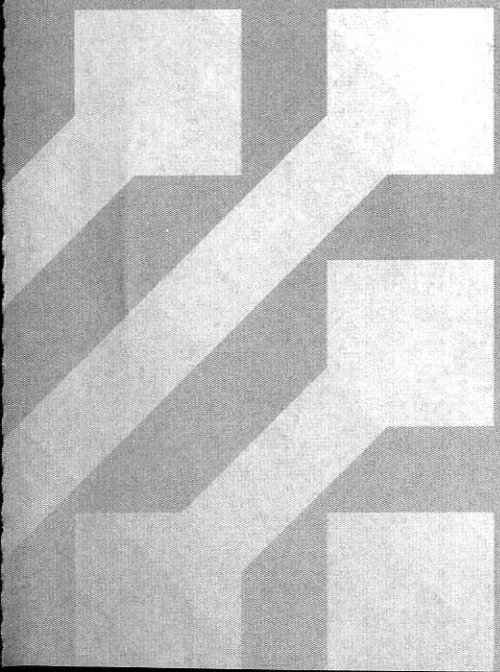


FIGURE 6-32. TIMING-TARGET TO BUS FREE

WD33C95A, WD33C96A Enhanced Single-ended and Differential SCSI Bus Interface Controller



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1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes two versions of a single chip VLSI SCSI bus controller. The WD33C96A is a 100-pin device that can act only as a single-ended SCSI controller, and the WD33C95A is a 132-pin device that can act as both a single-ended and a differential SCSI controller.

In this document, the term ESBC (Enhanced SCSI bus controller) is used as a term when referring to both parts.

The ESBC can perform both as an initiator and target. The data path for this device is programmable to be either 8- or 16-bits wide. All the features and timings described below are preliminary and subject to change without notice.

1.2 REFERENCE DOCUMENTS

The following reference documents may be of help:

- Draft proposed American National Standards for Information Systems-Small Computer System Interface-2 (SCSI-2), X3T9.2 Task Group number X3T9/89-042 revision 10c dated March 2, 1990.
- WD33C92A SCSI Protocol Chip Specification 96-105393.
- WD61C40A Series Intelligent Disk Controller and Buffer Manager Chip Specification.

1.3 FEATURES

- High speed (10MT/s) SCSI bus transfers, 8- or 16-bits wide
- Minimum SCSI bus latency/overhead
- Automatic response to a bus initiated selection/reselection
- Flexible combination commands through writeable control store
- Automatic decoding of the transfer length of commands
- 16-word FIFO to support synchronous offset up to 16-words or 32-bytes
- Programmable synchronous transfer period
- Includes single-ended 48 mA drivers for SCSI interface
- Includes control signals to support external differential drivers and receivers
- Supports low-level SCSI bus control
- Efficient interaction with the WD61C40A series with less microprocessor overhead
- Supports fast DMA transfers up to 10M transfers/second
- Supports host adapter application on the motherboard
- Flexibility to support most DMA controllers or buffer managers
- Dedicated 8-bit port for high speed microprocessor
- Pipelined 24-bit transfer counter (two-level)
- Transfers may be specified in bytes or logical blocks
- Minimum microprocessor intervention required
- Single +5 volt supply with low power mode
- 100-pin PQFP package for single-ended interface
- 132-pin package for differential interface
- Target-mode LRC generation/checking

1.4 GENERAL DESCRIPTION

The ESBC is a high performance CMOS VLSI device that controls data transfers between the SCSI bus and the local data buffer.

2.0 ARCHITECTURE

2.1 PERFORMANCE

The SCSI and DMA interfaces are independently programmable between 16- and 8-bits wide. The interface can transfer data at a rate up to 10M transfers/second, that is 20 MByte/s mode in 16-bit mode. The total time required to perform arbitration, selection, command transfer, and message transfer is less than 20 µs. The ESBC includes a dedicated 8-bit port for a high performance microprocessor, such as 25 MHz 80C188/186 and 16 MHz 80C196. The ESBC requires supervision from the microprocessor only in exception conditions. The device includes a 16 by 18-bit FIFO to support an offset of 16-words or 32-bytes in a SCSI synchronous transfer.

2.2 FLEXIBILITY

The ESBC handles SCSI protocol and data transfer through a 128-word Writeable Control Store (WCS), allowing the user to program any sequence of bus phases on the SCSI bus. The ESBC can act as a target as well as an initiator. The WCS has enough capacity to fit both initiator and target instruction sequences. The device can interface with various buffer managers, such as the WD60C40, WD60C40A, WD61C40 series, and the WD42C22. It can also interface with various types of DMA controllers.

2.3 MICROPROCESSOR INTERFACE

The device has a dedicated microprocessor interface. This port supports 8-bit microprocessors with a multiplexed address/data AD[0-7] bus. The microprocessor can access the internal registers and FIFO through this port. The ESBC can interface with various high performance microprocessors, such as 80C196, 80C188, and 80C186. $\overline{RE}$ and $\overline{WE}$ control access through this port.

The ESBC has another access mode, where the microprocessor can access the internal registers through DMA bus pins BD[0-7]. This mode is useful in applications where a dedicated microprocessor is not available and the ESBC is controlled directly by the main processor. The microprocessor accesses the internal registers in 8-bit mode; only the lower DMA port is used. The register address is supplied into the AD bus (dedicated microprocessor bus). $\overline{DRE}$ and $\overline{DWE}$ control the access. $\overline{DACK}$ must not be active.

2.4 DMA INTERFACE

The on-board DMA controller is programmable to act as bus master or slave. The polarity of DRQ and DACK is also programmable to be active high or low. The data can be transferred in 8- or 16-bit mode. The maximum transfer rate is 10M transfers/s. The ESBC automatically performs byte/word conversions.

2.5 DUAL PORT REGISTERS

The ESBC uses a 32-word by 9-bit (8-bit plus parity) Dual Port Register to store special information such as commands, messages and status. The information is transferred between the SCSI bus and the registers under control of the WCS sequence. The microprocessor can randomly access these registers like any other register. The dual port structure allows simultaneous accesses by the microprocessor and the WCS as long as they do not access the same address location. If both the microprocessor and the WCS simultaneously access the same location, the integrity of the data cannot be guaranteed. The microprocessor must keep track of which portion of the Dual Port Register is not accessible.

2.6 DIFFERENTIAL DRIVER CONTROL

One configuration of the ESBC, the WD33C95A, provides all signals needed for interface to a 8- or 16-bit differential SCSI bus. All commonly used SCSI interface devices are supported.

2.7 POWER MANAGEMENT

The ESBC automatically goes into a power-down mode when the WCS has not been active and the device has not been accessed for a period of time defined in the SLEEP register. A wakeup time of less than 200 ns is required to return to full operating speed.

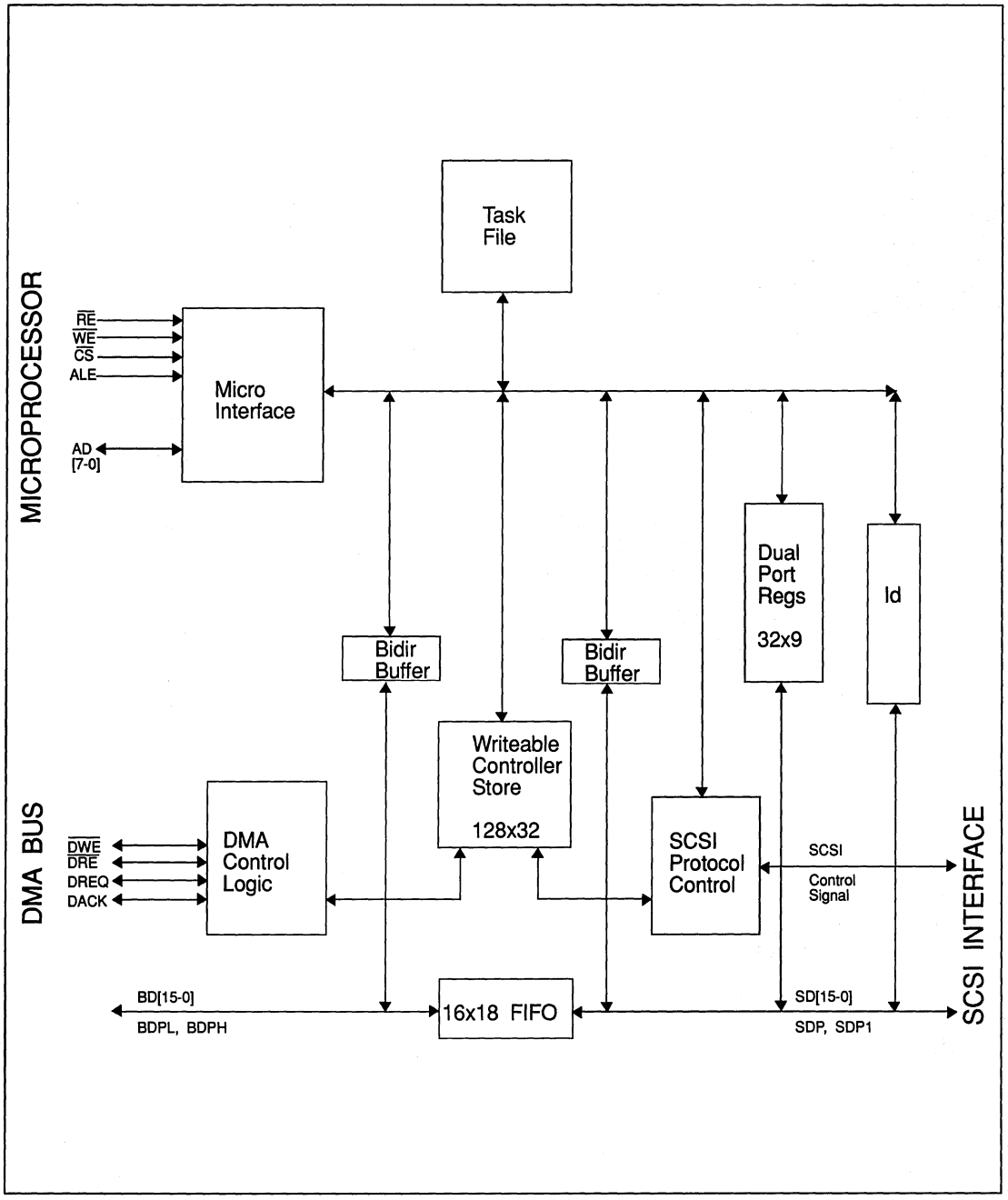

FIGURE 2-1. ESBC BLOCK DIAGRAM

2.8 TESTABILITY

The ESBC includes several features to improve testability of the device:

- All registers are readable
- WCS RAM is readable and writeable by the microprocessor
- Hystersis test for the input buffers of the SCSI signals
- Wire bond/pin solder checking
- BIST for the WCS, DPR and FIFO register files

2.9 COMPATIBILITY with WD33C93 FAMILY

The architecture of the ESBC is substantially different from that of the WD33C93 family. However, the ESBC has the ability to emulate all the combination commands supported by the WD33C93. In addition, the firmware that controls the device may be adapted to support higher performance through pipelining.

3.0 SIGNAL DESCRIPTION

This section contains two figures and accompanying tables which describe the signal to pin locations.

In addition there is a detailed description of each signal.

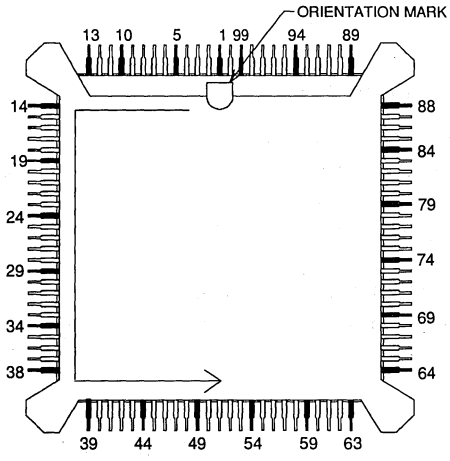

FIGURE 3-1. 100-PIN PACKAGE

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-GND	26-N.C.	51-BD10	76-VCC
2-I/O	27-N.C.	52-BD11	77-SD11
3-MSG	28-VCC	53-BD12	78-N.C.
4-C/D	29-GND	54-BD13	79-SD10
5-GND	30-AD0	55-BD14	80-GND
6-ACK	31-AD1	56-BD15	81-SD9
7-REQ	32-AD2	57-BDPH	82-N.C.
8-GND	33-AD3	58-GND	83-SD8
9-RST	34-AD4	59-DRE	84-GND
10-ATN	35-AD5	60-DWE	85-SD7
11-BSY	36-AD6	61-DRQA	86-N.C.
12-SEL	37-AD7	62-DRQB	87-SD6
13-VCC	38-VCC	63-VCC	88-VCC
14-GND	39-GND	64-GND	89-GND
15-CLK	40-BD0	65-DACKA	90-SD5
16-MUX	41-BD1	66-DACKB	91-SD4
17-DIRECT	42-BD2	67-N.C.	92-GND
18-CS	43-BD3	68-N.C.	93-SD3
19-WE	44-BD4	69-SD15	94-SD2
20-RE	45-BD5	70-N.C.	95-GND
21-ALE	46-BD6	71-SD14	96-SD1
22-HRST	47-BD7	72-GND	97-SD0
23-RDY	48-BDPL	73-SD13	98-GND
24-RSTF	49-BD8	74-N.C.	99-SDP1
25-INT	50-BD9	75-SD12	100-SDP

TABLE 3-1. WD33C96A PIN ASSIGNMENTS

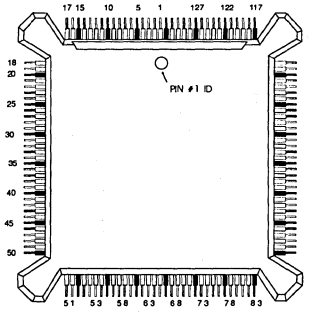

FIGURE 3-2. 132-PIN PACKAGE

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-C/D	34-SD1OE	67-BD9	100-SD11
2-GND	35-SD2OE	68-BD10	101-SD11OE
3-ACK	36-SD3OE	69-N.C.	102-SD10OE
4-REQ	37-SD4OE	70-BD11	103-SD10
5-GND	38-DIFFSENS	71-BD12	104-GND
6-RSTIN	39-VCC	72-GND	105-SD9
7-RST	40-GND	73-BD13	106-SD9OE
8-ATN	41-AD0	74-BD14	107-SD8OE
9-N.C.	42-AD1	75-N.C.	108-SD8
10-BSYIN	43-AD2	76-BD15	109-GND
11-BSY	44-AD3	77-BDPH	110-SD7
12-SELIN	45-N.C.	78-GND	111-N.C.
13-SEL	46-AD4	79-DRE	112-SD7OE
14-IGS	47-AD5	80-DWE	113-SD6OE
15-N.C.	48-AD6	81-DRQA	114-SD6
16-TGS	49-AD7	82-DRQB	115-SD5OE
17-VCC	50-VCC	83-VCC	116-VCC
18-GND	51-GND	84-GND	117-GND
19-CLK	52-BD0	85-N.C.	118-SD5
20-SE	53-BD1	86-DACKA	119-SD4
21-MUX	54-N.C.	87-DACKB	120-GND
22-DIRECT	55-BD2	88-N.C.	121-SD3
23-CS	56-BD3	89-SD15	122-SD2
24-WE	57-GND	90-SD15OE	123-GND
25-RE	58-BD4	91-SD14OE	124-SD1
26-ALE	59-BD5	92-SD14	125-SD0
27-HRST	60-N.C.	93-GND	126-GND
28-N.C.	61-BD6	94-SD13	127-SDP1
29-N.C.	62-BD7	95-SD13OE	128-SDP
30-RDY	63-GND	96-N.C.	129-SDPOE
31-RSTF	64-BDPL	97-SD12OE	130-GND
32-INT	65-BD8	98-SD12	131-I/O
33-SD0OE	66-N.C.	99-VCC	132-MSG

TABLE 3-2. WD33C95A PIN ASSIGNMENTS

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
MICROPROCESSOR INTERFACE				
30-37	41-44 46-49	AD[0-7]	I/O	**Microprocessor Address/Data Bus**
21	26	ALE	I	**Address Latch Enable** The falling edge of ALE is used to latch the address of the desired register.
18	23	$\overline{CS}$	I	**Chip Select** $\overline{CS}$ is active low and is used to qualify $\overline{RE}$ and $\overline{WE}$ when the microprocessor is accessing a register.
17	22	DIRECT	I	Selects direct microprocessor access protocol.
22	27	$\overline{HRST}$	I	**Hardware Reset**
25	32	INT	O	**Interrupt Request** INT is active high, and is asserted to indicate an error condition or completion of a command.
16	21	MUX	I	Selects multiplexed microprocessor address/data protocol.
23	30	RDY	O	**Chip Ready** RDY is an open-drain output. RDY will be pulled low whenever the device is being accessed and is not ready to end the bus access cycle.
20	25	$\overline{RE}$	I	**Read Enable** This signal is active low and is used with $\overline{CS}$ to read the registers.
24	31	RSTF	O	**SCSI Reset Follower** RSTF is a debounced version of $\overline{RST}$/RSTIN. It is active high, and will be asserted as long as a valid SCSI reset is detected.
N/A	20	SE	I	Single-ended SCSI select. (10K pullup)
19	24	$\overline{WE}$	I	**Write Enable** This signal is active low and is used with $\overline{CS}$ to write the registers.
DMA INTERFACE				
40-47	52,53,55, 56,58,59, 61,62	BD[0-7]	I/O	**DMA Bus** The lower 8 bits of the DMA bus.
48	64	BDPL	I/O	Parity for BD[0-7].

TABLE 3-3. SIGNAL DESCRIPTION

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
49-56	65,67,68 70, 71,73 74,76	BD[8-15]	I/O	**DMA Bus** DMA bus for upper 8 bits.
57	77	BDPH	I/O	Parity for BD[8-15].
65	86	DACKA	I/O	**Port A DMA Acknowledge** This pin is used to acknowledge DMA requests on port A.
66	87	DACKB	I/O	**Port B DMA Acknowledge** This pin is used to acknowledge DMA requests on port B.
59	79	$\overline{DRE}$	I/O	**DMA Read Enable** This signal is active low, and is used to strobe on the DMA bus.
61	81	DRQA	I/O	**Port A DMA Request** This pin is used to request DMA transfers on port A.
62	82	DRQB	I/O	**Port B DMA Request** This pin is used to request DMA transfers on port B.
60	80	$\overline{DWE}$	I/O	**DMA Write Enable** This signal is active low, and is used to strobe data on the DMA bus.
SCSI INTERFACE				
6	3	$\overline{ACK}$	I/O	**Data Acknowledge**
10	8	$\overline{ATN}$	I/O	**Attention**
11	N/A	$\overline{BSY}$	I/O	**Busy** Bidirectional busy signal.
N/A	11	BSY	O	**Busy** Output busy signal.
N/A	10	$\overline{BSYIN}$	I/O	**Busy** Input busy signal.
4	1	$\overline{C}$/D	I/O	**Command/Data** Command/data select.
N/A	38	DIFFSENS	I	**Differential SCSI Sense** (10K pullup)
2	131	$\overline{I}$/O	I/O	**Input/ Output** Select input or output direction.
N/A	14	IGS	I/O	**Initiator Group Select** Asserted whenever the WD33C95A is connected as an initiator.

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
3	132	$\overline{\text{MSG}}$	I/O	**Message** Selects message phase.
7	4	$\overline{\text{REQ}}$	I/O	**Data Request**
9	N/A	$\overline{\text{RST}}$	I/O	**SCSI Reset** Resets SCSI bidirectional signal.
N/A	7	RST	O	**SCSI Reset** Resets SCSI output only signal.
N/A	6	$\overline{\text{RSTIN}}$	I	**SCSI Reset** Resets SCSI input only signal.
85, 87, 90, 91, 93, 94, 96, 97	110,114, 118, 119, 121, 122, 124, 125	$\overline{\text{SD[0-7]}}$	I/O	**SCSI Data** Lower byte (0-7) SCSI data signals.
100	128	$\overline{\text{SDP}}$	I/O	Parity for $\overline{\text{SD[0-7]}}$
69, 71 73, 75 77, 79 81, 83	89, 92, 94, 98, 100, 103 105, 108	$\overline{\text{SD[8-15]}}$	I/O	**SCSI Data** Upper byte (8-15) SCSI data signals.
99	127	$\overline{\text{SDP1}}$	I/O	Parity for $\overline{\text{SD[8-15]}}$
N/A	33-37, 90-91, 95, 97, 101,102, 106,107, 112,113, 115	SDOE[0-15]	O	**Output Enable** These output enables are active high.
N/A	129	SDPOE	O	**Output Enable** Output enable for SDP and SDP1
12	N/A	$\overline{\text{SEL}}$	I/O	**Select** Bidirectional select.
N/A	13	$\overline{\text{SEL}}$	O	**Select** Output only select.
N/A	12	SELIN	I	**Select** Input only select
N/A	16	TGS	O	**Target Group Select** High whenever a target.

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
		MISCELLANEOUS		
15	19	CLK	I	**INPUT CLOCK** 20 MHz to 50 MHz
13, 28, 38, 63, 76, 88	17, 39, 50, 83, 99, 116	VCC	--	**Power Supply** +5V Power Supply Pins
1, 5, 8, 14, 29, 39, 58, 64, 72, 80, 84, 89, 92, 95, 98	2, 5, 18, 40, 51, 57, 63, 72, 78, 84, 93, 104, 109, 117, 120, 123, 126, 130	GND	---	**GROUND PINS**

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

A.0 GLOSSARY AND CONVENTIONS

The following is a list of terms and conventions used throughout the ESBC data sheet.

A.1 GLOSSARY

TERM	MEANING
00x00	Hexadecimal number
CDB	Command Descriptor Block
DMA	Direct Memory Access
DPR	Dual Port Register
FIFO	First In First Out Memory
HLR	High Level Response bits (SELH, RSELH, AUTOR)
LLR	Low Level Response bits (SELL, RSELL)
LSB	Least Significant Bit
MSB	Most Significant Bit
RAM	Random Access Memory
SRS	Reselection Response Sequence
WCS	Writeable Control Store

A.2 CONVENTIONS

TERM	CONVENTION
asserted	the signal is driven active by the ESBC
negated	the signal is driven inactive by the ESBC
released	the signal is released by the ESBC; external bias circuitry will bring the signal to the inactive state
micro	refers to the microprocessor controlling the ESBC
DMAC	refers to the DMA controller connected to the DMA port

A.3 RESERVED REGISTERS

All registers marked as "Reserved" must not be written, and if read, will produce either 0's or 1's.

All bits marked as "Reserved" must only be written with 0's, and if read, will produce either 0's or 1's.

WD37C65C

Floppy Disk Subsystem Controller Device

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1.0 INTRODUCTION

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates the following functions: formatter/controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy drive.

The WD37C65C is functionally compatible pin-for-pin with the WD37C65A/B. In addition the WD37C65C supports a power down mode for laptop and portable systems. Refer to Table 16-6 for a descripion of functional differences between the WD37C65A/B and the WD37C65C.

On the disk drive interface, the WD37C65C includes data separation designed to address high performance error rates on floppy disk drives. It contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write precompensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the WD37C65C, these functions are latched into registers addressed within the I/O mapping of the system. The WD37C65C has eight internal registers. The eight bit main status register contains status information about the WD37C65C and may be accessed any time. Another four status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65C.

All Clock Generation: SCLK - Sampling Clock, WCLK-Write Clock, and MCLK - Master Clock, are included in the WD37C65C. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the WD37C65C. The first at 32 MHz that handles all standard data rates (1MB/sec, 500, 250, and 125 kb/sec or 16MHz to handle 500, 250, and 125 Kb/sec). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.

Some AT compatibles use two-speed disk drives. If a two-speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

1.1 FEATURES

- IBM PC AT compatible format (single and double density)
  - —Provides "on chip" floppy control and operations
  - —Provides required signal qualification to DMA channel when in PC AT mode
  - —BIOS compatible
  - —Supports dual speed spindle drives
- CMOS low power consumption (typically 300 mW at 32 MHz)
- Power down mode with low standby current (ICC = 100µA maximum)
- Address mark detection circuitry (internal to floppy disk controller)
- Multi-sector and multi-track transfer capability
- Direct floppy disk drive interface (no buffers needed)
  - —48 mA sink output drivers
  - —Schmitt Trigger line receivers

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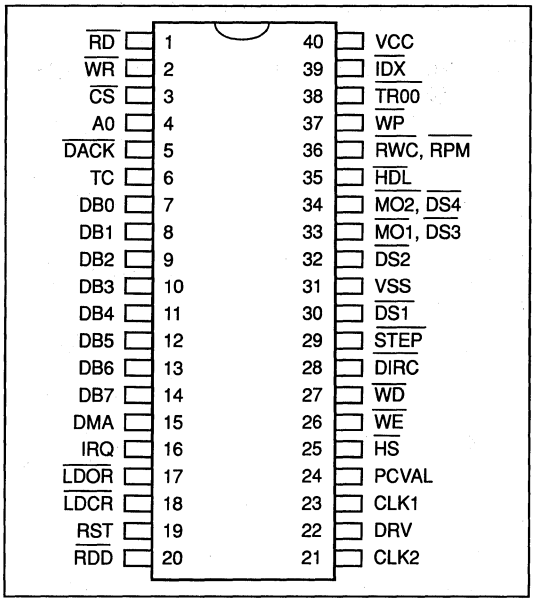
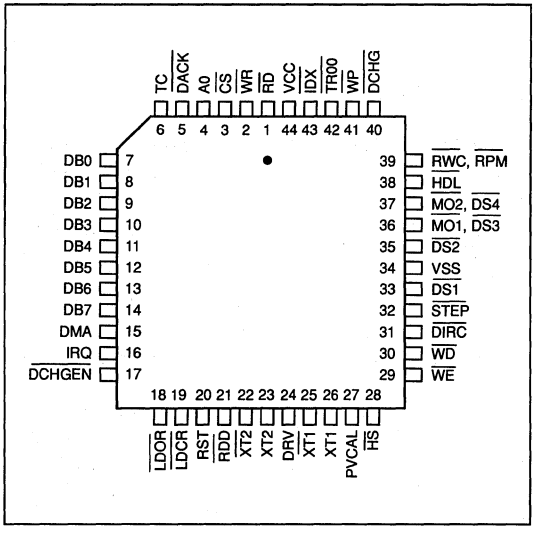
- Compatible with PD8080/85, PD8086, 8088, 80286, 80386SX, 80386, and PD780 (Z80) microprocessors
- On chip clock generation
- Two TTL clock inputs for 40-pin DIP
- Two XTAL oscillator circuits for 44-pin PLCC
- Automatic write precompensation
  - —Disable option
  - —Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator
  - —Industry standard error rates of 10<E-9
  - —Data rates of 125, 250, 300, 500 Kbits/second and 1Mbit/second
  - —Option to select 150 Kbits/second FM and 300 Kbits/second MFM data rates only
- Enhanced host interface
  - —20 LSTTL output drive capability
  - —TTL Schmitt trigger inputs
- User programmable track stepping rate and head load/unload times
- Supports four floppy or Micro Floppydisk drives with external decode logic
- Data transfer in DMA or non-DMA mode
- Parallel seek operation on a maximum of four drives
- Internal power up reset circuitry
- Single +5V DC power supply



40 PIN DIP



44 PIN PLCC

2.0 SIGNAL DESCRIPTIONS

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 /1	$\overline{RD}$	$\overline{READ}$	I	Control signal for transfer of data or status onto the data bus by the WD37C65C.
2/2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data from the bus into the WD37C65C Buffer Register.
3/3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (=1) or status (=0) information. (A0 = logic 0 during $\overline{WR}$ is illegal except in Power Down mode.)
5/5	$\overline{DACK}$	$\overline{DMA\ ACKNOWLEDGE}$	I	Used by the DMA controller to transfer data from the WD37C65C onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In Special or AT/EISA mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL-COUNT	I	This signal indicates to WD37C65C that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in AT/EISA mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA host operation. Programmed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
7-14/ 7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register. This pin is driven in the Base mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or AT/EISA mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
/17	$\overline{\text{DCHGEN}}$*	$\overline{\text{DISK CHANGE ENABLE}}$	I	This input must be at Logic = 0 to enable $\overline{\text{DCHG}}$ input status at pin 40 to be placed on bit 7 of the data bus during a $\overline{\text{RD}}$ = 0 of $\overline{\text{LDCR}}$ = 0. It has Internal pull-up.
17/18	$\overline{\text{LDOR}}$	$\overline{\text{LOAD OPERATIONS REGISTER}}$	I	Address decode which enables the loading of the Operations Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the data bus into the Operations Register.
18/19	$\overline{\text{LDCR}}$	$\overline{\text{LOAD CONTROL REGISTER}}$	I	Address decode which enables loading of the Control Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	$\overline{\text{RST}}$	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
20/21	$\overline{\text{RDD}}$	$\overline{\text{READ DISK DATA}}$	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6MHz for 300 kb/s, and can only be selected from the Control Register.
/22	$\overline{\text{XT2}}$	$\overline{\text{XTAL2}}$	0	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 23.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a twospeed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1% or 32MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	$\overline{\text{XT1}}$	$\overline{\text{XTAL1}}$	0	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs are used at pin 26.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16MHz or 32MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
24/27	PCVAL	PRECOMPEN-SATIONVALUE	I	Precompensation value select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125ns, Logic 0 = 187ns. If the defeat option is used, PCVAL is unimportant and precompensation is disabled.
25/28	$\overline{HS}$	$\overline{HEAD\ SELECT}$	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 = side 0. Logic 0 = side 1.
26/29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27/30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O	This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
28/31	$\overline{DIRC}$	$\overline{DIRECTION}$	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion. Logic 0 = inward motion.
29/32	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 1}$ in AT/EISA mode. It enables the interface to this disk drive. This signal comes from the Operations Register. In Base, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND	--	Ground.
32/35	$\overline{DS2}$	$\overline{DRIVE\ SELECT\ 2}$	0	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 2}$ in AT/EISA mode, enables the interface to this disk drive. This signal comes from the Operations Register. In Base or the Special mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$	0	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.

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*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	0	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output, when active low, causes a REDUCED WRITE CURRENT, when bit density is increased toward the inner tracks, becoming active when tracks >28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
/40	$\overline{DCHG}$*	$\overline{DISK\ CHANGE}$	I	This Schmitt Trigger (ST) input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This ST input senses status from the disk drive indicating active low when a diskette is WRITE PROTECTED.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This ST input senses status from disk drive, indicating active low when the head is positioned over the outermost track, TRACK 00.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC	--	Input power supply.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

3.0 ARCHITECTURE

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates: formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

Figure 3-1 illustrates a block diagram of the WD37C65C Floppy Disk Subsystem Controller.

Figure 3-2 illustrates a typical WD37C65C system.

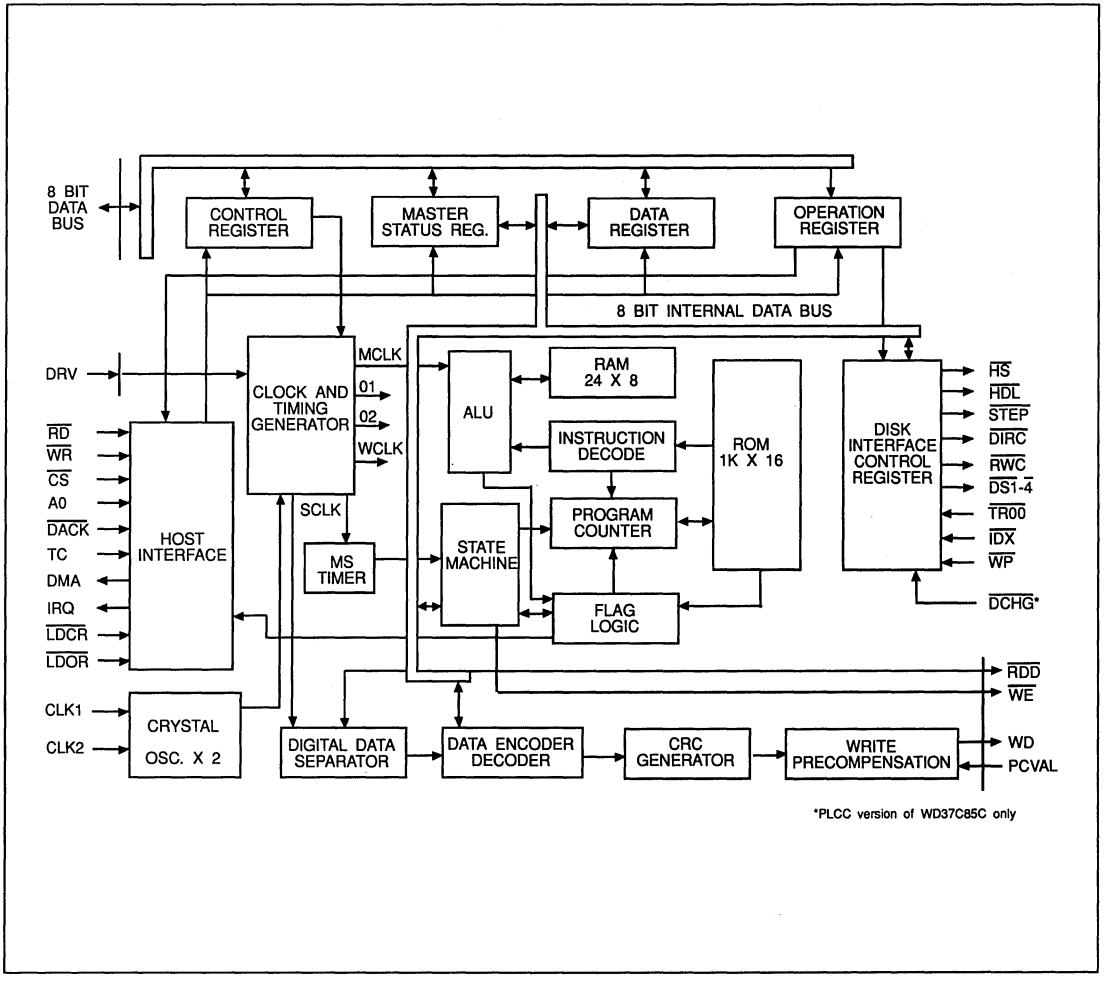

FIGURE 3-1. WD37C65C BLOCK DIAGRAM

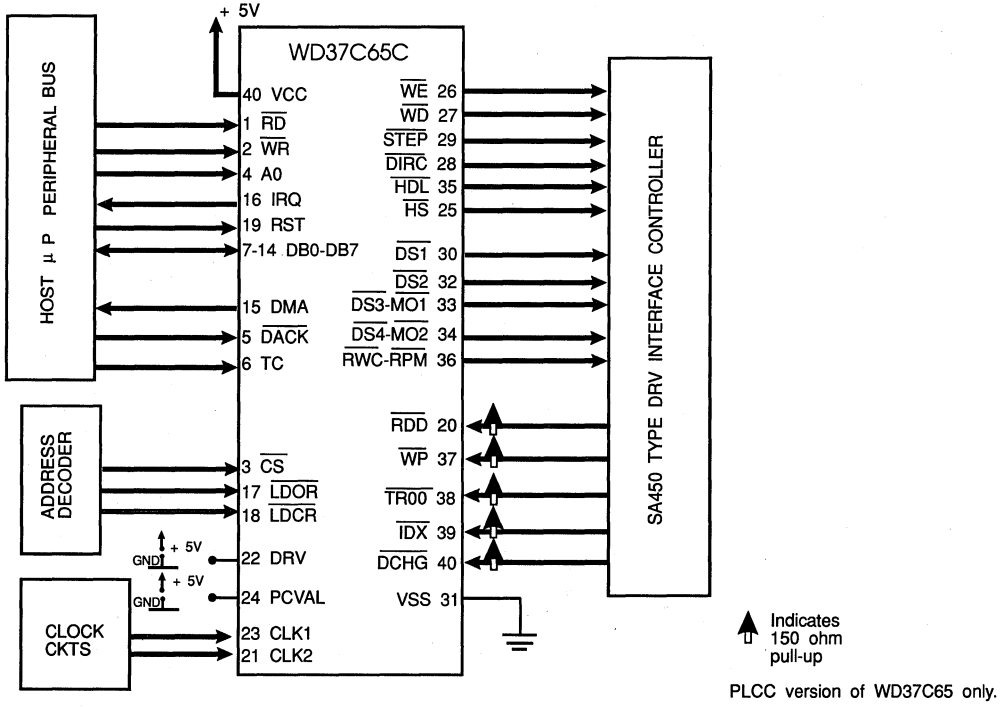

FIGURE 3-2. TYPICAL WD37C65 SYSTEM

4.0 HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes, IRQ and DMA request are tri-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12 µs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65C. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD37C65C. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65C is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12µs.

During the Execution phase, the Main Status Register need not be read. If the WD37C65C is in the non-DMA Mode, then the receipt of each data byte (WD37C65C is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal (RD = 0) clears the interrupt and sends the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 µs for the MFM mode and 27 µs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65C is in the DMA mode, no interrupt signals are generated during the Execution phase. The WD37C65C generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both DACK=0 (DMA Acknowledge) and an RD=0 (Read signal). When the DMA Acknowledge signal goes low (DACK=0), the DMA Request is cleared (DMA= 0) If a Write Command has been issued, then a WR signal will appear instead of RD. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ = 0).

Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65C will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive DACK.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect durinq DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to Vcc. Note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD37C65C will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65C contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only afler completing a command. The particular command that has been executed

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determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65C to form the Command phase, and are read out of the WD37C65C in the Result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65C, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65C is ready for a new command.

5.0 CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches the two LSBs of the data bus upon receiving LDCR and WR. CS should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 Kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchless" or the device will need to be reset. Table 5-1 and Table 5-2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

The WD37C65C optionally supports 150 kb/s FM data transfer rate. The Control Register configuration is shown in Table 5-3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44pin PLCC) or pin 23 (40 pin DIP). Only two data transfer rates can be selected with this configuration: 150 kb/s FM and 300 kb/s MFM.

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA MODE)
0	0	x	500 K	MFM	1
0	0	x	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	250 K	MFM, RST Default	1
1	0	x	125 K	FM, RST Default	1

TABLE 5-1. CONTROL REGISTER CONFIGURATION - 16 MHZ

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISAMODE)
0	0	x	1 M	MFM	1
0	0	x	500 K	FM	1
0	1	0	500 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	500 K	MFM, RST Default	1

TABLE 5-2. CONTROL REGISTER CONFIGURATION - 32 MHz

In AT/EISA mode, write precompensation can be disabled by a logic high on bit 2 of the Control Register. (See Table 5-4).

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA MODE)
0	0	x	300 K	MFM	1
0	0	x	150 K	FM	1

TABLE 5-4. CONTROL REGISTER CONFIGURATION - OPTIONS

Bit	SIGNAL NAME AND FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	0	None
1	Data Rate	0	None
2	No Write Precompensation	0	None
3-7	Reserved	None	None

TABLE 5-3. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

6.0 MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The WD35C65C provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the WD37C65C. See Master Status Register 1.

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65C. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a Command or Result phase and the setting of DIO and RQM is 12 µs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24 µs. If 1 Mb/s is selected, the delay is 6 µs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12 µs. The maximum time from the trailing edge of the last RD in the result phase to when DB4 (FDC busy) goes low is 12 µs.

The bits in the Master Status Register are listed in Table 6-1. The bits in Status Register 0 are listed in Table 6-2.The bits in Status Register 1 are listed in Table 6-3.The bits in Status Register 2 are listed in Table 6-4.The bits in Status Register 3 are listed in Table 6-5.

6.1 MASTER STATUS REGISTER 1 (MSR1--WRITE ONLy)

The WD37C65C will enter power down mode, when bit 0 of MSR1 is set to logical "1" and the following conditions are met:

1. The RST pin to the FDC is inactive.

2. Bit 2 in the Operations Register is "SRST/= 1".

3. The WD37C65C is awaiting a command from the host.

The WD37C65C can also be programmed with external logic to automatically enter power down mode a few msec after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit 0 of MSR1 register to logic 0.
The bits in the Master Status Register are listed in Table 6-2.

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BIT	SIGNAL NAME & FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 6-1. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIG.

BIT NO.	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and '"direction" to the processor.

TABLE 6-2. STATUS REGISTER 0 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	INTERRUPT CODE	IC	D7=0 and D6=0. Normal termination of command was completed and properly executed. D7=0 and D6=1. Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
D6	---	---	D7=1 and D6=0. Invalid command issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
†D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur after 77step pulses per Recalibrate Command, then this flag is set.
†D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

TABLE 6-3. STATUS REGISTER 1 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	---	---	Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3	---	---	Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 6-4. STATUS REGISTER 2 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	---	---	Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of * * *C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

TABLE 6-5. STATUS REGISTER 3 BITS

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BIT NO.	NAME	SYMBOL	DESCRIPTION
†D7	---	---	Not used. Will always be logic 0.
D6	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
†D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
†D3	WRITE PROTECTED	$\overline{WP}$	This bit is used by the WD37C65C to indicate the status of the WRITE PROTECTED signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

TABLE 6-6. MASTER STATUS REGISTER BITS

* CRC - Cyclic Redundancy Check

* * IDR - Internal Data Register

* * * C - Cylinder

† - Different from NEC765

7.0 DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals RD, WR, and A0 are shown in Table 7-1.

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

TABLE 7-1. MASTER STATUS AND DATA REGISTERS RELATIONSHIPS

8.0 OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR and WR. CS should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8-1 represents the Operations Register.

NO.	SYMBOL	DESCRIPTION
OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1 is active. If high and MOEN2 = 1, then DS2 is active, but only in the AT/EISA mode.
OR1	(x)	This must be a logic O for DS1 and DS2 to become active.
OR2	SRST	Soft reset, active low.
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ outputs and DACK input.
OR4	MOEN1	Motor On enable, inverted output M01 is active only in AT/EISA mode.
OR5	MOEN2	Motor On enable, inverted output M02 is active only in AT/EISA mode.
OR6	(X)	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/EISA mode (0).

TABLE 8-1. OPERATIONS REGISTER

9.0 BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

9.1 BASE MODE

After a hardware reset, RST active, the WD37C65C will be held in soft reset, SRST active, with the normally driven signals, DMA request and IRQ request outputs tri-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, DS1 to DS4, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC represents Reduce Write Current and is indicative of when write precompensation is necessary.

9.2 SPECIAL MODE

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST to be active. Then a read of the Control Register address, LDCR and RD, places the device in Special mode. The DS1 through DS4 is again offered in this mode, as is RWC.

9.3 AT/EISA MODES

For AT/EISA compatibility, users write to the Operations Register, LDOR and WR; this action, performed after a hardware reset, or in the Base mode, initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST are supported and compatible with the current BIOS. RWC pin function is now RPM so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive. Figure 9-1 illustrates the relationship among the three modes.

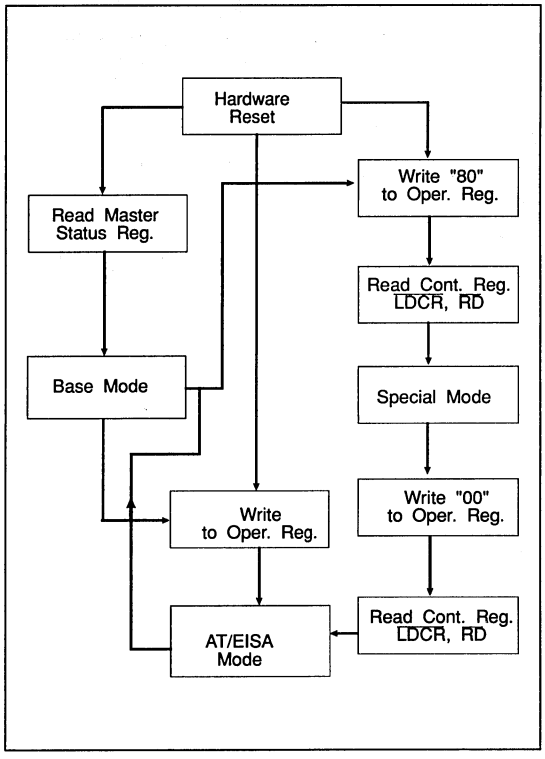

FIGURE 9-1. FLOW DIAGRAM BASE, SPECIAL & AT/EISA MODES

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10.0 POLLING ROUTINE

After any reset the WD37C65C, (a hard RST or soft SRST), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the WD37C65C polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65C occurs continuously between commands. Each drive is polled every 1.024ms, except during the READ/WRITE commands. For mini-floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 10-1 illustrates the Drive Select Polling Timing.

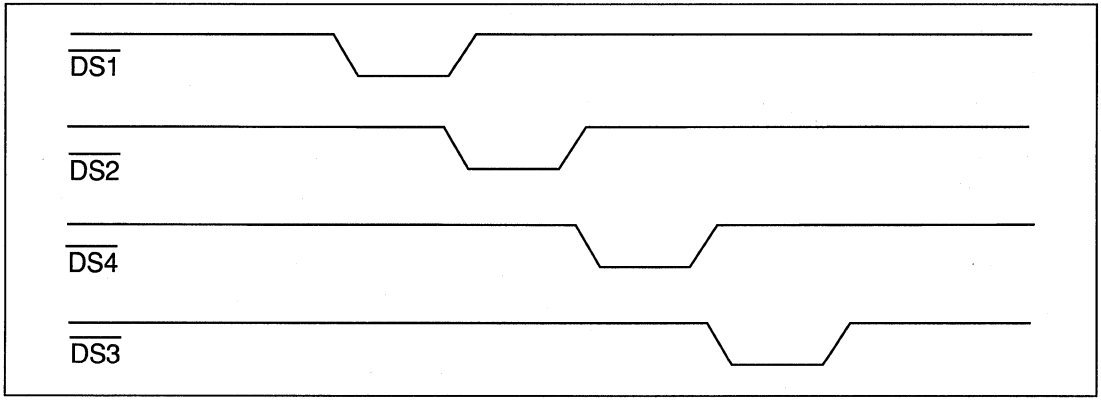

FIGURE 10-1. DRIVE SELECT POLLING TIMING

11.0 DEVICE RESETS

The WD37C65C supports both hardware reset (RST) pin (19) and a software reset (SRST) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250kb MFM (or 125kb FM, code dependent) as the data rate (16 MHz input clock). The default data rate for a 32 MHz input clock is 500kb MFM. SRST will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. RST, when active, will disable the high current driver outputs to the disk drive. RST and SRST will not affect the values set for the internal timers - HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

12.0 DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 3-1 illustrates the WD92C32 used as the Data Separator in the WD37C65C system. Figure 13-1 illustrates the WD92C32 simplified block diagram. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

13.0 WRITE PRECOMPENSATION

The WD37C65C maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24) = 1, all data will be precompensated by ± 125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187ns precompensation will be generated. For frequencies other than 16 MHz or 32 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard 300 kb/s data rate using CLK2 is chosen, the MFM precompensation will always be two clock cycles. For 9.6 MHz, this is ± 208ns. In this case, the PCVAL function is disabled.

Write precompensation can be disabled by bit 2 of the Control Register for the AT/EISA. The PCVAL input to WD37C65C is ignored if there is no write precompensation.

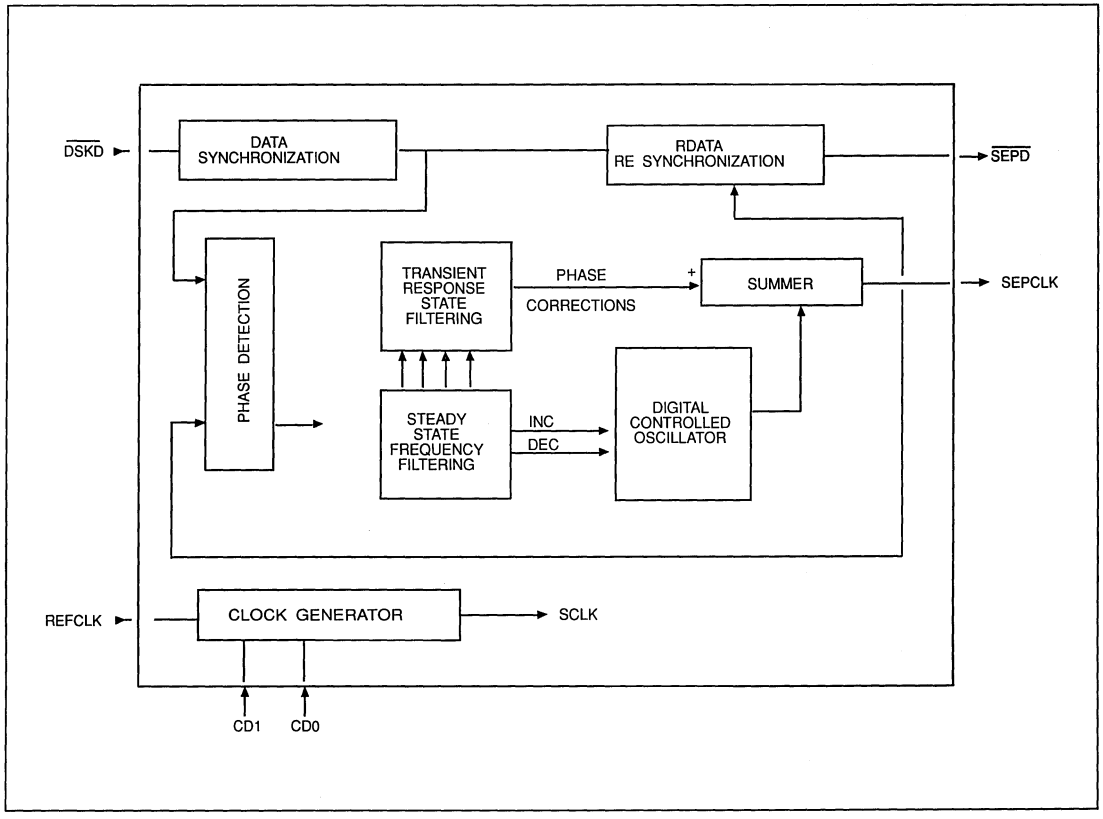

FIGURE 13-1. WD92C32 SIMPLIFIED BLOCK DIAGRAM

14.0 CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65C. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{\text{MCLK}}$ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 14-1 presents the Clock Data Rate.

Figure 14-1 illustrates the XTAL oscillator circuits for the 44-pin PLCC configuration.

In power down mode the XTAL oscillator and the clock circuitry are turned off.

DATA RATE	CODE	SCLK MHz	MCLK MHz	WCLK
1 Mb/s	MFM	32.0	8.0	2.0 MHz
500 kb/s	MFM	16.0	4.0	1.0 MHz
500 kb/s	FM	16.0	8.0	1.0 MHz
250 kb/s	FM	8.0	4.0	500 KHz
250 kb/s	MFM	8.0	2.0	500 KHz
125 kb/s	FM	4.0	2.0	250KHz
300 kb/s	MFM	9.6	2.4	600 KHz

TABLE 14-1. CLOCK DATA RATE

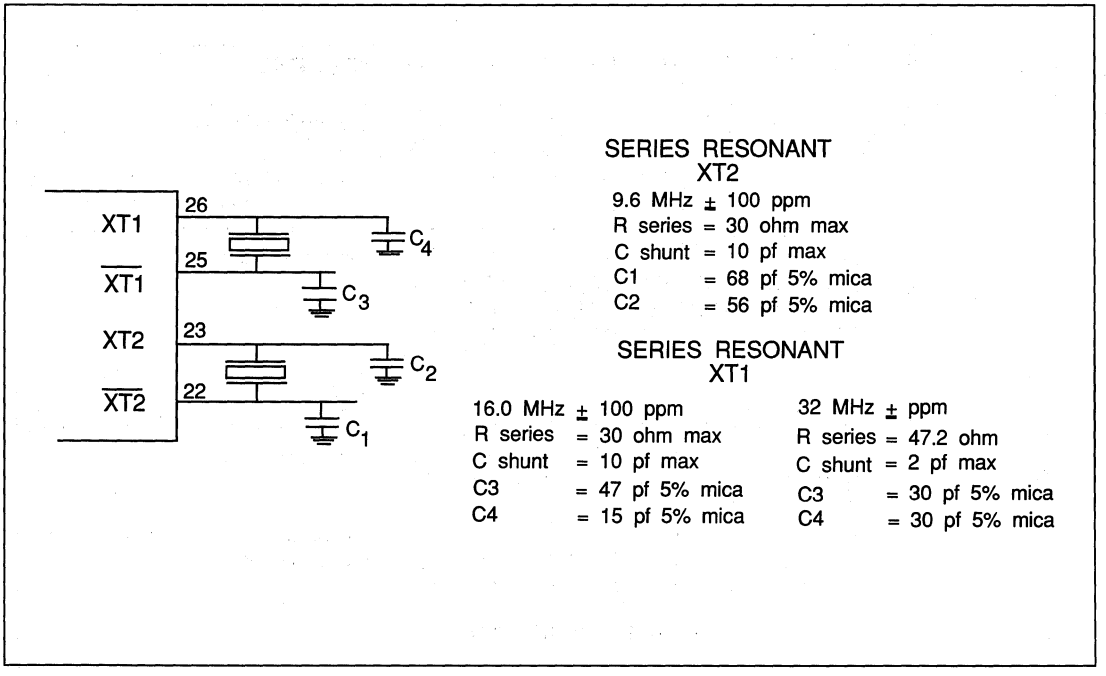

FIGURE 14-1. CRYSTAL OSCILLATOR CIRCUITS FOR 44-PIN PLCC

15.0 COMMAND PARAMETERS

The WD37C65C is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

Command phase - The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor

Execution phase - The FDC performs the operation it was instructed to do.

Result phase - After completion of the operation, status and other housekeeping information are made available to the processor.

Table 15-1 lists the 15 WD37C65C commands.

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK

TABLE 15-1. WD37C65C COMMANDS

Tables 15-1 through 15-16 are presented to show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15-2. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15-3.READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15-4. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-5. WRITE DELETED DATA

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PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US1	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-6. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information read during
	R	R	R	R	R	R	R	R	R	Execution Phase from floppy
	R	N	N	N	N	N	N	N	N	disk.

TABLE 15-7. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	N	N	N	N	N	N	N	N	Bytes/Sector
	W	SC	SC	SC	SC	SC	SC	SC	SC	Sectors/Track
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	Gap 3
	W	D	D	D	D	D	D	D	D	Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	In this case, the ID information
	R	R	R	R	R	R	R	R	R	has no meaning.
	R	N	N	N	N	N	N	N	N	

TABLE 15-8. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-9. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-10. SCAN LOW OR EQUAL

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PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution.
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15-11. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 15-12. RECALIBRATE

The WD37C65C issues 77 step pulses, the same as the NEC765.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information about the FDC
	R	PCN	PCN	PCN	PCN	PCN	PCN	PCN	PCN	at the end of seek operation

TABLE 15-13. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT	
	W	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND	

TABLE 15-14. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R	ST3	ST3	ST3	ST3	ST3	ST3	ST3	ST3	Status information about the FDC.

TABLE 15-15.SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	NCN	NCN	NCN	NCN	NCN	NCN	NCN	NCN	
EXECUTION										Head is positioned over proper cylinder on the diskette.

TABLE 15-16. SEEK

Table 15-17 defines, in alphabetical order, the symbols used in Command Tables 15-1 through 15-16.

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1 as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.

TABLE 15-17. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	---	During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

TABLE 15-17. COMMAND SYMBOL DESCRIPTIONS (CONTINUED)

16.0 COMMAND DESCRIPTIONS

16.1 READ DATA

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number("R") stored in the ID Register(IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes/sector). Table 31 lists the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes /Sect or N	Maximum Transfer Capacity (Bytes/Sector) Number of Sectors	Final Sector Read From Diskettes
0 0	0 1	00 01	(128)(26)=3,328 (256)(26)=6,656	26 at Side 0 or 26 at Side 1
1 1	0 1	00 01	(128)(52)=6,656 (256)(52)=13,312	26 at Side 1
0 0	0 1	01 02	(256)(15)=3,840 (512)(15)=7,680	15 at Side 0
1 1	0 1	01 02	(256)(30)=7,680 (512)(15)=15,360	15 at Side 1
0 0	0 1	02 03	(512)(8)=4,096 (1024)(8)=8,192	8 at Side 1 or 8 at Side 1
1 1	0 1	02 03	(512)(16)=8,192 (1024)(16)=16,384	8 at Side 1

TABLE 16-1. TRANSFER CAPACITY

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskene. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM mode, and every 13 µs in the MFM mode, or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 16-2 shows the values for C, H, R, and N, when the processor terminates the command.

MT	HD	Final Sector Transferred to Procesor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=0	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=0	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=0	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=0	NC

TABLE 16-2. C, H, R, AND N VALUES

Notes:
NC (No Change): The same value as the one at the beginning of command execution.
LSB (Least Significant bit): The least significant bit of H is complemented.

16.2 WRITE DATA

A set of nine bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation' until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 µs in the FM mode and every 13 µs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

16.3 WRITE DELETED DATA

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

16.4 READ DELETED DATA

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

16.5 READ A TRACK

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

16.6 READ ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

16.7 FORMAT A TRACK

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD37C65C for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formaning continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 16-3 shows the relationship between N, SC, and GPL for various sector sizes.

Format	Sector Size Bytes/sector	N	SC	GPL 1	GPL 2,3
8" Standard Floppy					
FM Mode	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" Minifloppy					
FM Mode	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" Sony Microfloppy					
FM Mode	128	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

TABLE 16-3. N, SC AND GPL RELATIONSHIP

Notes:
1. Suggested values of GPL in Read 0, Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexadecimal.
4 In MFM mode FDC cannot perform a Read/Write/format operation with 126 bytes/sector. (N=00)

16.8 SCAN COMMANDS

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP $_{-8}$ R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 16-4 shows the status of bits SH and SN under various conditions of Scan.

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Command	Status Register 2 Bit 2=SN	Bit 3=SH	Comments
Scan Equal	0	1	$D_{FFD}=D$ Processor
Scan Equal	1	0	$D_{FFD}\neq D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan Low or Equal	0	0	$D_{FFD}<D$ Processor
Scan Low or Equal	1	0	$D_{FFD}>D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan High or Equal	0	0	$D_{FFD}>D$ Processor
Scan High or Equal	1	0	$D_{FFD}<D$ Processor

TABLE 16-4. STATUS OF BITS SH AND SN

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 µs (FM mode) or 13 µS (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

16.9 SEEK

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150 µS, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

16.10 RECALIBRATE

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is

low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 step pulses have been issued, (for the WD37C65 and the WD37C65A) or 77 step pulses (WD37C65B/C), the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

16.11 SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands

2. Ready Line of FDD changes state

3. End of Seek or Recalibrate command

4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Seek End Bit 5	Interrupt Code Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

TABLE 16-5. INTERRUPT CAUSE

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD37C65C will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 16-1.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 =32 ms . . . $0F_{16}$ = 240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2ms, 02 = 4ms, 03 = 6ms . . . 7F = 254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32 MHz, then all time intervals are decreased by half.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

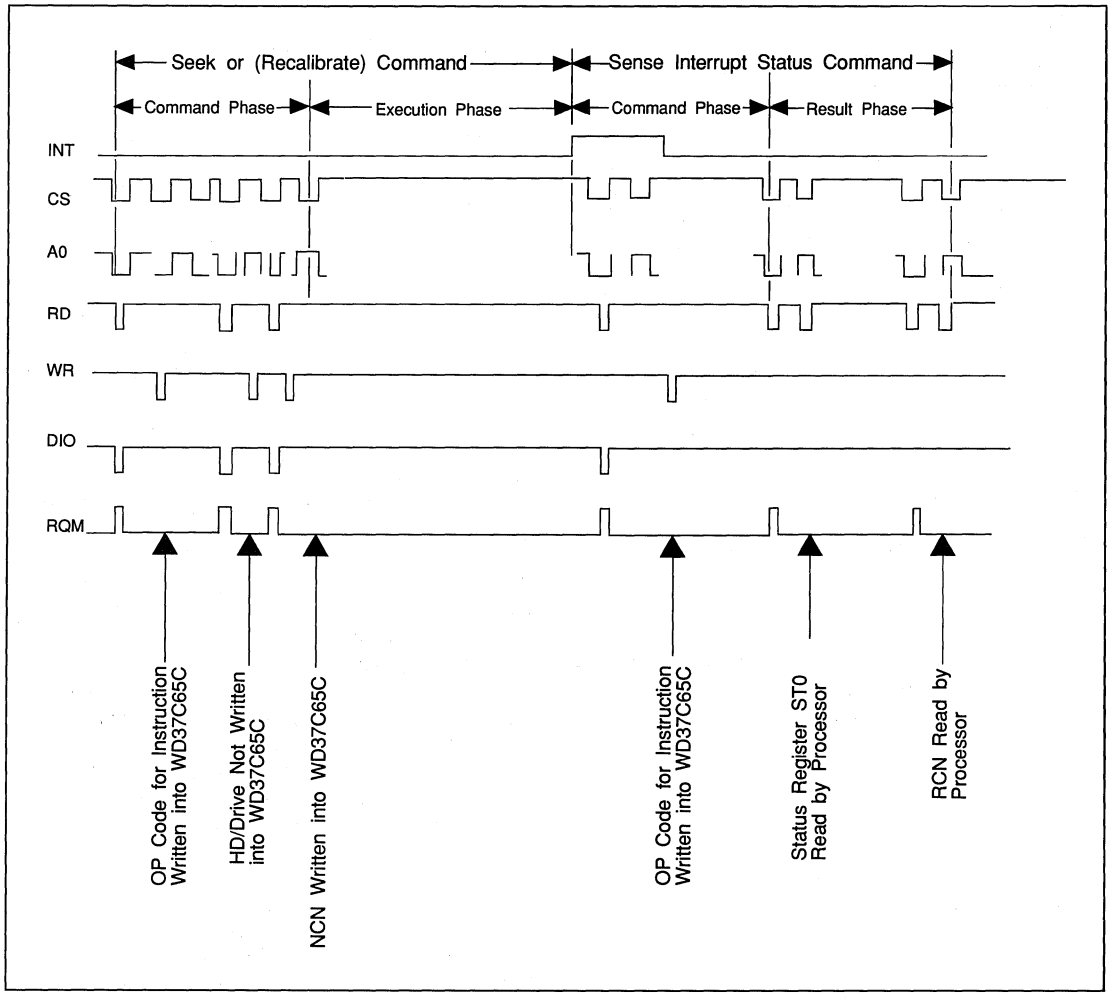

FIGURE 16-1. SEEK, RECALIBRATE, AND SENSE INTERRUPT

16.12 SENSE DRIVE STATUS

This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

16.13 INVALID

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD37C65C is in the Result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

GAP4a	SYNC	IAM	GAP 1	SYNC	IDAM	C		S		C	GAP 2	SYNC	DATA AM	DATA	C	GAP 3	GAP4b
40x	6x		26x	6x		Y	H	E	N	R	11x	6x		1	R	1	
FF	00	FC	FF	00	FE	L	D	C	O	C	FF	00	FB or F8		C		

Index ⟵ Repeat N Times ⟶

FIGURE 16-2. WD37C65C FM MODE FORMAT

GAP4a	SYNC	IAM		GAP 1	SYNC	IDAM		C		S		C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP4b
80x	12x	3x		50x	12x	3x		Y	H	E	N	R	22x	12x	3x	FB	1	R	1	
FF	00	C2	FC	FF	00	A1	FE	L	D	C	O	C	E	00	A1	F8		C		

Index ⟵ Repeat N Times ⟶

FIGURE 16-3. WD37C65C MFM MODE FORMAT

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No.	WD37C65/A/B	WD37C65/C
1.	2 XTAL oscillators. - 16 MHz for standard data rate (up to 500kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s PCAT)	2 XTAL oscillators. - 32 MHz for standard data rate (up to 1 Mb/s MFM) or 16 MHz for standard data rate (up to 500kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s AT/EISA)
2.	Supports data rate up to 500 Kb/s.	Supports data rate up to 1 Mb/s
3.	Does not support power down mode.	Supports power down mode feature, standby ICC = 100 µA max.
4.	PCVAL pin for selecting the precomp values.	PCVAL pin for selecting the precomp values and a feature to disable write precomp.

TABLE 16-6. DIFFERENCES BETWEEN WD37C65/A/B AND WD37C65C

17.0 DC ELECTRICAL SPECIFICATIONS

17.1 MAXIMUM RATINGS

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	-55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground	-0.3V to VCC +0.3V
Supply Voltage with respect to ground	7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

17.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground.

Operating temperature range (TA)	0°C (32°F) to 70°C (158F)
Power supply voltage (VCC)	+5V ± 10%

17.3 DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	+5VDC Power Supply	4.5	5.5	V
VIL	Input Low Voltage - Data Bus & XTOSC	---	0.8	V
VIH	Input High Volt - Data Bus & XTOSC	2.0	---	V
VILT	Input Low Threshold - Schmitt Trigger	0.8	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysterisis	0.45	---	V
VOL	Output Low- DBx,IRQ,DMA,; Io = 24.0mA	---	0.4	V
VOH	Output High - DBx,IRa,DMA,; Io = -5.0mA	2.8	---	V
VOLHC	Output Low - High Current; Io = 48.0mA	---	0.4	V
ILUL	Latch Up Current Low	40.0	---	mA

SYMBOL	PARAMETER	MIN	MAX	UNITS
ILUH	Latch Up Current High	-40.0	---	mA
ILL	Leakage Current Low	---	10.0	µA
ILH	Leakage Current High	---	-10.0	µA
ICC	Supply Current - 100 µA Source Loads	---	60.0	mA
ICCHL	Supply Current - 5.0 mA Source Loads	---	120.0	mA
ICCPDM	Supply Current in Power Down Mode	---	100.0	µA[1]
PD	Power Dissipation- ICC Max	---	600.0	mW[3]
PDHL	Power Dissipation - ICCHL Max	---	750.0	mW[2,3]
VPQR	Power Qualified Reset Threshold	2.8	4.35	V

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Note 1. Vin = VCC or GND, Io = O mA.

Note 2. Includes DBx, IRQ and DMA; Io = -5.0 mA source loads.

Note 3. Includes open drain high current drivers at Vol = 0.4V.

18.0 AC TIMING CHARACTERISTICS

The following notes apply to all parameters presented in this section:

1. TA = 0°C (32°F) to 70°C (158°F)
2. VCC = +5V ± 10%
3. CL = 100 pf
4. CY = CLK1 or XT1 period
5. MCY = MCLK period, dependent on selected data rate
6. WCY = WCLK period, dependent on selected data rate

SYMBOL	PARAMETER	MIN	MAX	UNITS
tCY	Clock Period	31	---	nS
tPH	Clock Active (High or Low)	13.5	---	nS
tR	Clock Rise Time (Vin 0.8 to 2.0)	---	2	nS
tF	Clock Fall Time (Vin 2.0 to 0.8)	---	2	nS
tAR	A0,$\overline{CS}$,$\overline{DACK}$ Set Up Time to $\overline{RD}$ Low	0	---	nS
tRA	A0,$\overline{CS}$,$\overline{DACK}$ Hold Time to RD High	0	---	nS
tRR	$\overline{RD}$ Width	90	---	nS
tRD	Data Access Time From $\overline{RD}$ Low	---	90	nS
tDF	DB To Float Delay From $\overline{RD}$ High	10	65	nS
tAW	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Set Up Time To $\overline{WR}$ Low	0	---	nS
tWA	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Hold Time From $\overline{WR}$ High	0	---	nS
tWW	$\overline{WR}$ Width	60	---	nS
tDW	Data Set Up Time To $\overline{WR}$ High	80	---	nS
tWD	Data Hold Time From $\overline{WR}$ High	0	---	nS
tRI	IRQ Reset Delay Time From $\overline{RD}$ High			1MCY +150nS
tWI	IRQ Reset Delay Time From $\overline{WR}$ High			1MCY +150nS
tMCY	DMA Cycle Time	52		MCY
tAM	DMA Reset Delay Time From $\overline{DACK}$ Low	---	140	nS
tMA	$\overline{DACK}$ Delay Time From DMA High	0	---	nS
tAA	$\overline{DACK}$ Width	90	---	nS
tTC	TC Width	60	---	nS
tRST	Reset Width - TTL Driven CLK1	60	---	nS
tSRST	Reset Width - Software Reset	5	---	MCY
tRDD	$\overline{RDD}$ Active Time Low	40	---	nS
tWDD	$\overline{WD}$ Write Data Width Low	1/2 (TYP)	---	WCY
tDST	$\overline{DIRC}$ Hold & Set Up To $\overline{STEP}$ Low	4	---	MCY
tSTU	$\overline{DSX}$ Hold Time From $\overline{STEP}$ Low	20	---	MCY
tSTP	$\overline{STEP}$ Active Time Low	24	---	MCY
tSC	$\overline{STEP}$ Cycle Time	132	---	MCY
tSTD	$\overline{DIRC}$ Hold Time After $\overline{STEP}$	96	---	MCY
tIDX	$\overline{IDX}$ Index Pulse Width	2	---	MCY
tMR	$\overline{RD}$ Delay From DMA	0	---	nS
tMW	$\overline{WR}$ Delay From DMA	0	---	nS

SYMBOL	PARAMETER	MIN	MAX	UNITS
tMRW	$\overline{RD}$ Or $\overline{WR}$ Response From DMA High	---	48	MCY
tCA	Chip Access Delay From RST Low - TTL	32	---	MCY
tCAS	Chip Access Delay From tSRST Low	40	---	MCY
tXCA	Chip Access Delay From RST-OSC XT1 at 16 MHz	500	---	µS
tXTS	XT2 Access Delay After RST 9.6 MHz	1000	---	µS
tTCR	TC Delay From Last DMA Or IRQ, $\overline{RD}$	0	192	MCY
tTCW	TC Delay From DMA Or IRQ, $\overline{WR}$	0	384	MCY
Tcycle	Clock Cycle	60	---	nS
Tp-high	Clock High	25	---	nS
Tp-low	Clock Low	25	---	nS
Trise	Rise Time	---	5	nS; Vin .8 to 2.0
Tfall	Fall Time	---	5	nS; Vin 2.0 to .8

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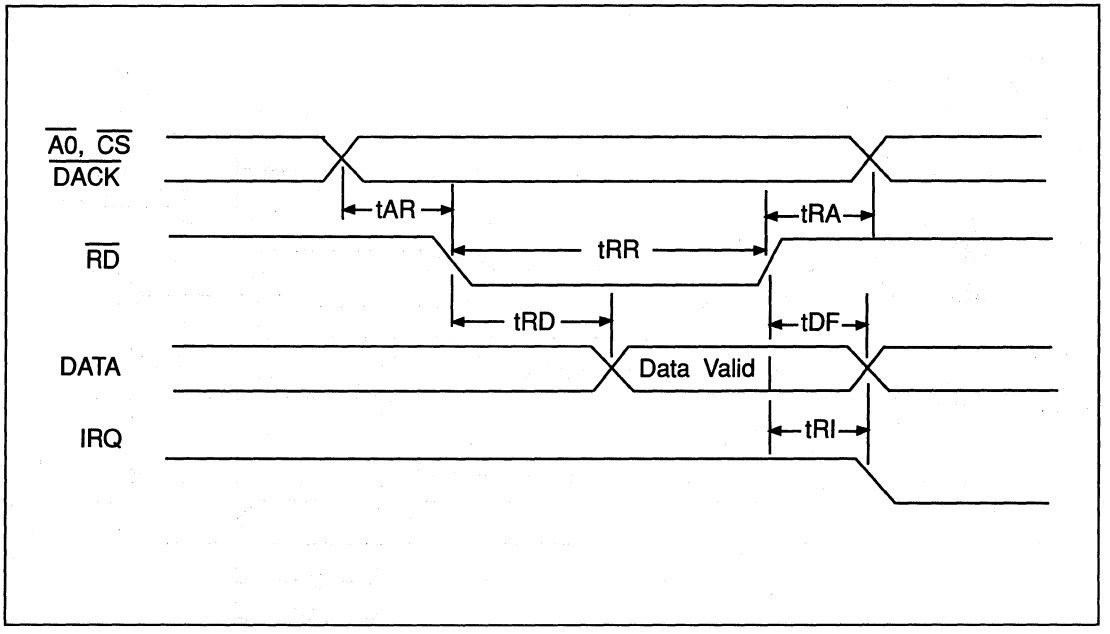

FIGURE 18-1. READ TIMING

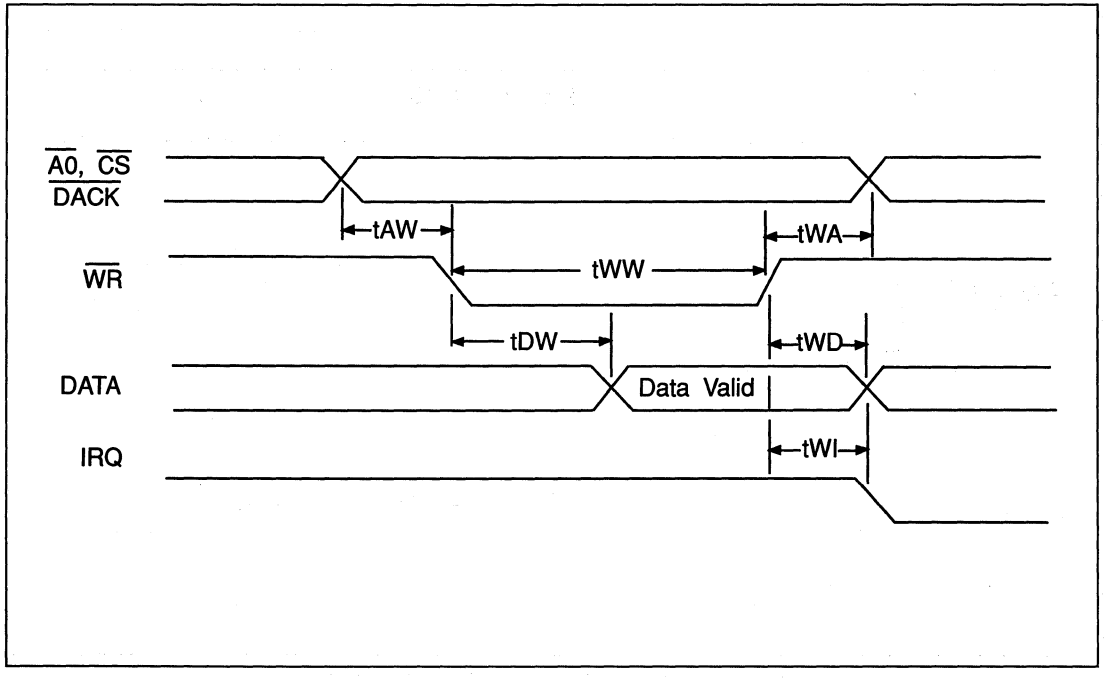

FIGURE 18-2. WRITE TIMING

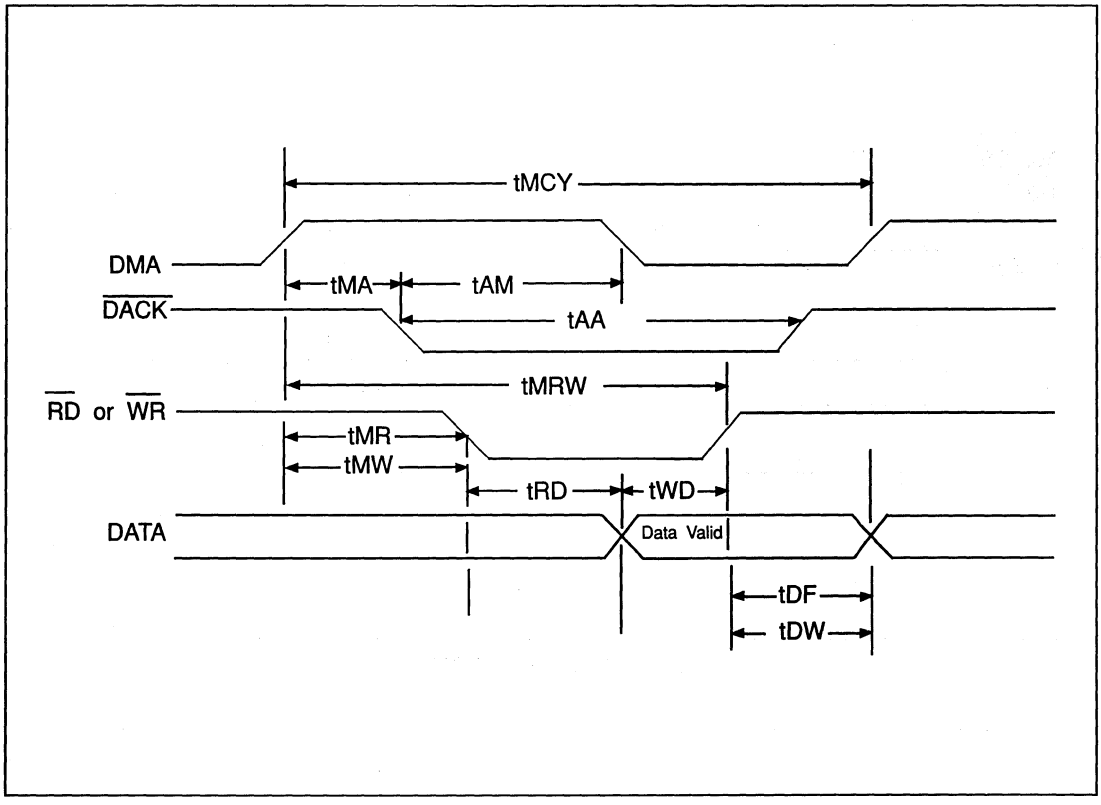

FIGURE 18-3. DMA TIMING

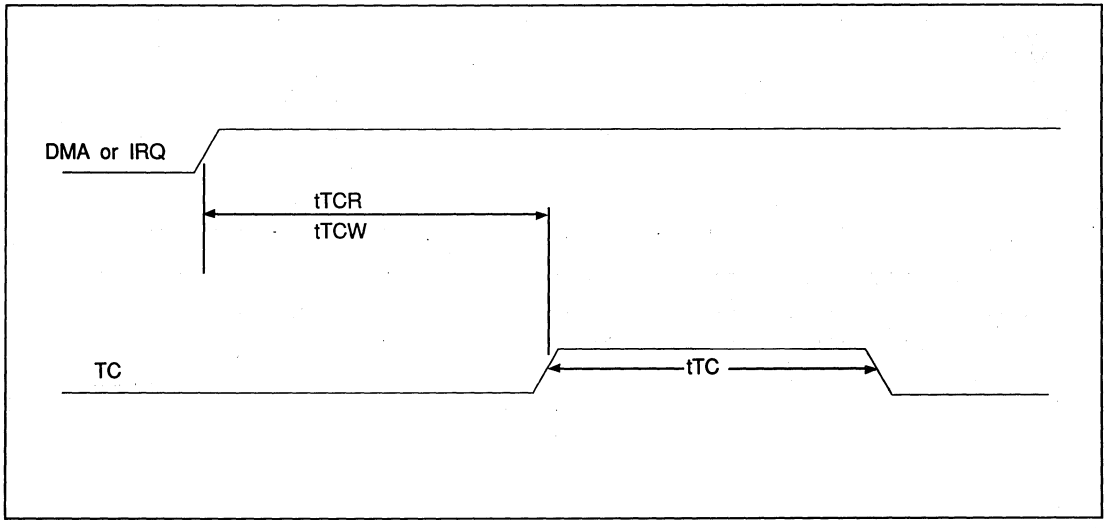

FIGURE 18-4. TERMINAL COUNT TIMING

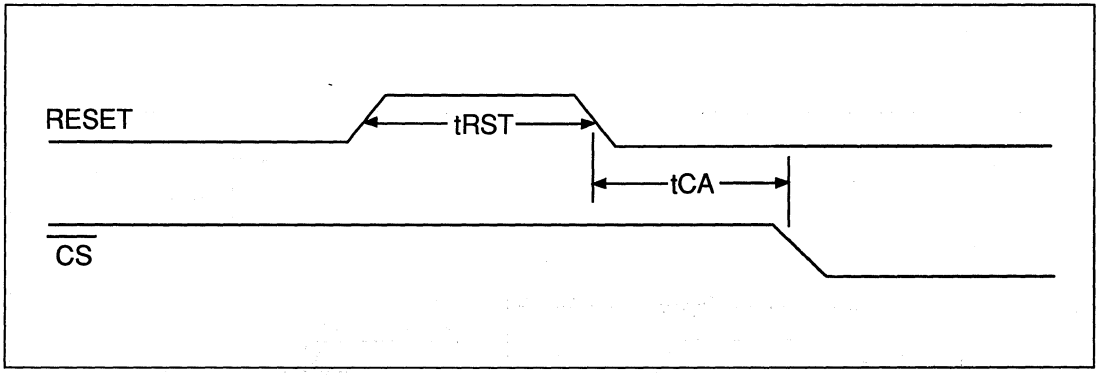

FIGURE 18-5. RESET TIMING

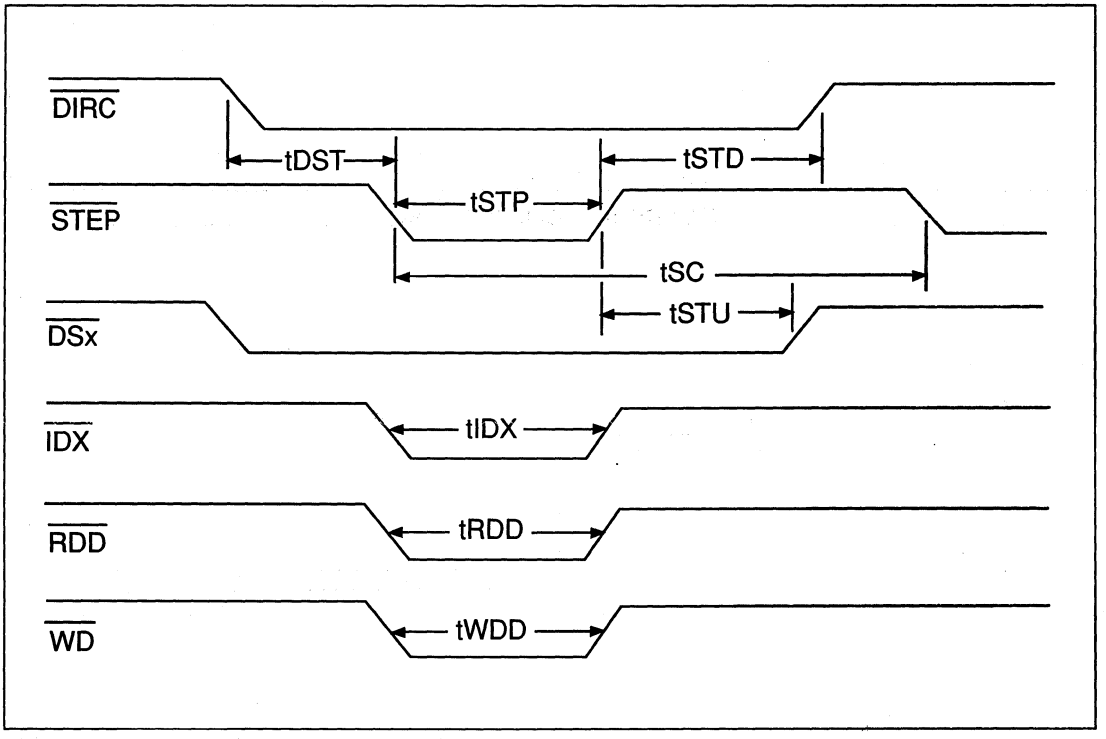

FIGURE 18-6. DISK DRIVE TIMING

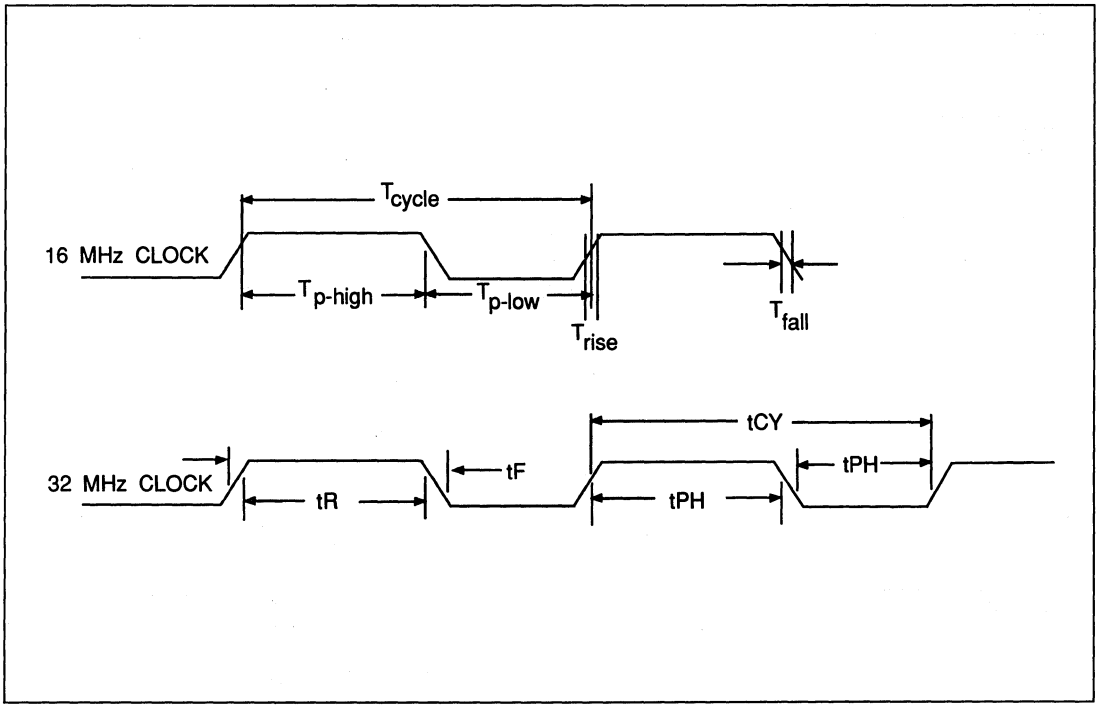

FIGURE 18-7. CLOCK TIMING

WD42C22C

Winchester Disk

Subsystem Controller Device

WESTERN DIGITAL

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1.0 INTRODUCTION

Western Digital's WD42C22C integrates a high performance, low cost Winchester formatter/controller, host interface, a buffer manager, and CRC/ECC generator/checker in a single 84-pin LSI device. Operating from a single +5V power supply, the WD42C22C is implemented in a low power CMOS design and is available in an 84-pin PLCC or PQFP (Figure 1). Figure 2 is a block diagram of the WD42C22C.

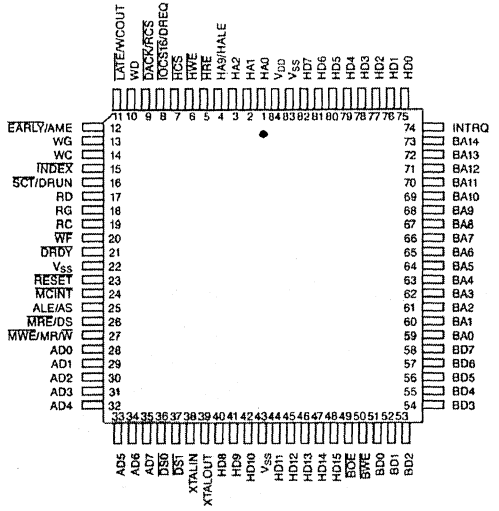

FIGURE 1. PIN DESIGNATION

1.1 FEATURES

- Enhanced host interface
  - IBM Personal Computer AT and XT port compatible
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 120 nsec static RAM (SRAM)
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 100 nsec SRAM
  - Selectable DMA or programmed I/O data transfers in all host interface modes
  - Host port slave mode compatible with ALE based peripherals such as the WD33C93 SBIC
  - Host transfer rates up to 4 Mwords/sec for AT, 4 MB/sec for XT, 10 MB/sec for SCSI
  - Internal 12 mA high current drivers for direct connection to the XT or AT system bus
- Advanced buffer manager
  - Supports 1:1 interleave **without** resorting to wait states
  - Direct interface for up to 32 KB of static RAM
  - Sustained RAM bandwidth up to 10 MB/sec
  - Pipelined host and disk address counters
  - Operates as either ring or scatter-gather buffer
  - Allows full track buffering and facilitates look ahead cacheing algorithms
  - Adaptable disk controller
  - Software selectable MFM, RLL 2,7, or NRZ disk interface
  - Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC
  - Software selectable 5, 11, or 22 bit error correction span
  - Software selectable default sector lengths of 128, 256, 512, and 1024 bytes
  - User programmable sector size up to 2048 bytes
  - Software selectable 3 bit or 4 bit head number field
  - Reads and writes at 1:1 Interleave regardless of the formatted interleave
  - 15 Mbs data transfer rate for MFM and RLL
  - 24 Mbs data transfer rate for NRZ
  - Supports hard or soft sectored formats
  - Supports "zero latency" read operations
  - Internal defect management of sector and track level alternates
  - Able to read ESDI defect list format
  - Supports sector servo schemes by disabling WRITE GATE over servo when formatting
  - Internal 48 mA drivers and Schmitt trigger input receivers for direct connection to the drive control cable
- Integrated support features
  - Programmable master/slave mode allows two Integrated Drive Electronics (IDE) disks on one connector
  - Supports both Intel-type(80xx) and Motorola-type(68xx) microcontrollers

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Internal power-qualified reset to detect low V_{DD}

- Low power sleep mode
- Available in 84-pin PLCC or 84-pin PQFP

1.2 DESCRIPTION

1.2.1 Enhanced Host Interface

The WD42C22C host interface port directly connects to the host system bus via internal 12 mA drivers. When operating in either AT or XT mode, all host control, data, and task file address lines directly connect to the WD42C22C. Mapping the device to the desired host system I/O addresses requires external address decode logic. Integrated I/O port compatible AT and XT task file registers assure system compatibility.

To satisfy requirements for faster system bus rates and data transfers, the WD42C22C can operate in 12 MHz or 16 MHz, 1 wait state I/O channels (0 wait state memory) of 286 or 386 microprocessors. DMA or PIO data operations transfer at a rate of 4 Mwords/sec (AT mode) or 4 MB/sec (XT mode). In addition to traditional single mode DMA, burst mode DMA transfers are also available.

An alternative host mode, slave mode, allows communication between the microcontroller and a peripheral device through the host interface. The slave device transfers data to the buffer RAM by

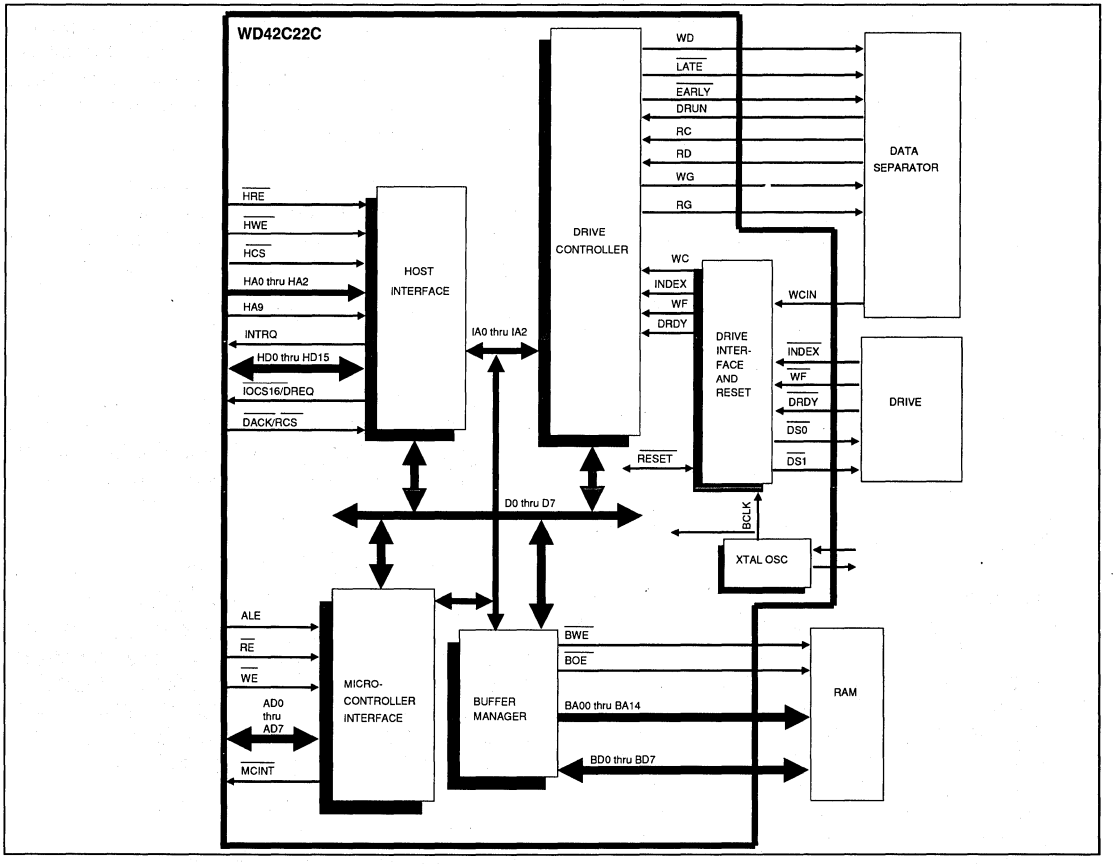

FIGURE 2. WD42C22C BLOCK DIAGRAM

using a slave DMA scheme such as the WD-BUS mode in the WD33C93 SCSI bus interface controller (SBIC).

1.2.2 Advanced Buffer Management

The WD42C22C contains an advanced buffer manager satisfying the interface requirements between a byte or word wide host interface bus and a high speed serial disk interface. Optimized for the block oriented data structures of a disk controller, the WD42C22C can manage multiple sector buffers up to 32 KB. Each sector buffer can be any size to 2055 bytes. Pipelined host and disk address counters enable sustained, simultaneous transfers on each port. Sufficient RAM buffer bandwidth is available to support 1:1 interleaved 20 Mb/sec disk transfers while simultaneously performing 16-bit host transfers at a rate in excess of 3 Mwords/sec. Achieving maximum RAM bandwidth requires using 70 nsec static RAM.

The pipelined structure of the buffer manager controls the buffer RAM in either a simple ring structure or a more advanced scatter-gather structure.

1.2.3 Adaptable Disk Controller

The WD42C22C's versatile design makes the device adaptable for a wide variety of disk interface operations. A designer can select from three data formats, MFM, RLL 2,7, or NRZ. Disk data rates range up to 15 Mbits/sec with MFM and RLL 2,7 encoding, while NRZ data rates range up to 24 Mbits/sec. To support varied data format requirements, the WD42C22C operates in hard or soft sectored mode with programmable sector sizes to 2048 bytes and programmable ID PLO, data PLO, and GAP lengths.

Software selectable retry algorithms and 32 or 56-bit ECC polynomials enhance data integrity. Data integrity can further be ensured through the use of the device's built-in advanced defect management. The WD42C22C can be programmed to automatically detect the presence of a previously assigned defective sector and identify the location of the alternate sector. This allows access to alternate sectors without the typical additional rotational latency associated with defect handling.

With the pipelined architecture of the buffer manager, the designer can program the disk controller to execute "zero-latency" multiple sector read operations. In this mode of operation, the WD42C22C immediately commences data transfer to the RAM buffer upon encountering the first sector on the desired track. All subsequent sectors transfer to the buffer within a single rotational period. Host transfers begin upon location of the first requested sector within the buffer. Simultaneous host and disk transfers continue until all sectors are read from the drive. Zero-latency operation makes available an entire track of data to the host within one rotational period from the time the host requested the data. This differs from traditional implementations which read the entire track within one rotational period after the first requested sector has been located. Zero latency read operations eliminate the typical one-half rotational period average latency required to locate the first sector in full track data transfers

The WD42C22C includes an internal power qualified reset circuit for power up and power down conditions. This circuit eliminates the need for costly external circuitry that traditionally performed this function.

The WD42C22C features a multiplexed address/data bus on the microcontroller interface port and supports both Intel (80XX) and Motorola (68XX) type microcontrollers. An internal circuit automatically determines the connected microcontroller and configures the ports for direct interfacing.

Internal 48 mA drivers and Schmitt triggers input receivers provide direct connection to the drive control cable. Programmable input polarities assist in integrated drive electronics (IDE) designs.

1.2.4 Flexibility of Application

As a result of its level of integration, a designer can create a wide variety of products. In addition to traditional stand alone Winchester controller boards, the WD42C22C is ideal for multi-function boards, direct system motherboards, and IDE applications. Special design considerations within the WD42C22C facilitate these applications.

1.2.5 Typical Application

With an external microcontroller, buffer RAM, and a data separator such as the WD10C22B, the

WD42C22C forms the basis of a Winchester disk controller product. For AT and XT applications, direct interfacing is available to the system bus. In these applications, the WD42C22C requires external address decoding to select the primary and secondary I/O address range of the WD42C22C. Other bus interfaces are supported via auxiliary bus controllers such as the WD33C93A SCSI Bus Interface Controller.

For ST506 (MFM) and ST412HP (RLL) applications, the WD42C22C directly connects to the WD10C22 data separator. (Like the WD42C22C, the WD10C22B supports both MFM and RLL encoding methods.) An external microcontroller implements interface specific control lines, e.g. the ST506's $\overline{\text{STEP}}$ and $\overline{\text{DIRECTION}}$ signals. For ESDI applications, the WD42C22C operates in NRZ mode.

1.2.6 Pin Descriptions

This section lists the pin number, signal name, and function for all the WD42C22C's pins. The pin descriptions are arranged by functions. Table 1 describes the pin designations for the host interface. Table 2 describes the pin designations for the local microcontroller interface. Table 3 describes the pin designations for the buffer interface. Table 4 describes the pin designations for the drive interface.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	HA0	HOST ADDRESS 0	I	Schmitt-triggered input. These four inputs are used to address the internal registers. Internal decoding of these address signals is a function of the AT/XT and HSMB mode bits. Port compatibility is maintained for both the AT and XT. In slave host mode HALE is used by the peripheral device to latch the address from HD0 through HD7.
2	HA1	HOST ADDRESS 1	I	
3	HA2	HOST ADDRESS 2	I	
4	HA9/ HALE	HOST ADDRESS 9/ HOST ALE	I/O	
5	$\overline{\text{HRE}}$	HOST READ ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HRE}}$ is asserted by the AT or XT with HCS to read an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It can also be asserted by the slave peripheral in DMA mode.
6	$\overline{\text{HWE}}$	HOST WRITE ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HWE}}$ is asserted by the AT or XT with HCS to write an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It is also asserted by the slave peripheral in DMA mode.
7	HCS	HOST CHIP SELECT	I/O	Schmitt-triggered input. HCS should be decoded from the AT or XT address bus and is used to qualify $\overline{\text{HRE}}$ and $\overline{\text{HWE}}$ for host accesses. In slave mode, HCS is asserted when the local microcontroller is accessing the slave device address space.
8	$\overline{\text{IOCS16}}$/ DREQ	I/O CHIP SELECT 16/ DMA REQUEST	O	This output is programmable to function as the AT bus signal $\overline{\text{IOCS16}}$ when the PIO mode is selected or as a DMA Request signal (DREQ) in the DMA mode. This output is tri-stated at power-up and remains tri-stated until the interface mode is set by the local microcontroller. $\overline{\text{IOCS16}}$ is an open-drain ouput. DREQ is a tri-state output.
9	$\overline{\text{DACK}}$/ $\overline{\text{RCS}}$	DMA ACKNOWLEDGE/ $\overline{\text{RAM CHIP SELECT}}$	I	Schmitt-triggered input. $\overline{\text{DACK}}$ is asserted by the host in response to the DREQ signal assertion in order to complete the DMA handshake. $\overline{\text{RCS}}$ is used in slave mode to qualify host data transfers to/from the FIFO.

TABLE 1. HOST INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
23	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I/O	Open-drain output and Schmitt input, can be wire-ORed with an external reset. The WD42C22C resets all logic except the Task File when this input is asserted. On power-up, or when requested by the host, this output is asserted.
75 thru 82, 40, 41, 42, 44 thru 48	HD0 thru HD15	HOST DATA 0 thru HOST DATA 15	I/O	Schmitt-triggered inputs. These 16 pins are used during host 16-bit data transfers, and the lower eight bits (HD0-HD7) are used for byte-wide host data transfers as well as all command and status information transfers.
74	INTRQ	INTERRUPT REQUEST	I/O	INTRQ indicates to the AT or XT that a data blocktransfer is requested or a command has been completed. In slave host mode INTRQ is asserted by the slave peripheral device.
83	V_{SS}	GROUND		Ground.
84	V_{DD}	+5V		+5V

TABLE 1. HOST INTERFACE PIN DESCRIPTION (CONT'D)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
22	V_{SS}	GROUND		Ground.
24	$\overline{MCINT}$	µCONTROLER INTERRUPT	O	This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, $\overline{MCINT}$ is asserted when the controller is selected.
25	ALE/AS	ADDRESS LATCH ENABLE/ ADDRESS STROBE	I	Schmitt-triggered input. ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0). AS is used for this function when tied to a Motorola type microcontroller.
26	$\overline{MRE}$/DS	µCONTROLLER READ ENABLE /DATA STROBE	I	Schmitt-triggered input. $\overline{MRE}$ is asserted by the local microcontroller to read an internal register or the buffer. DS is used in Motorola type microcontrollers to enable the data transfer.
27	$\overline{MWE}$/ MR/W	µCONTROLLER WRITE ENABLE/ uC READ/WRITE	I	Schmitt-triggered input. $\overline{MWE}$ is asserted by the local microcontroller to write an internal register or the buffer. MR/W is used by Motorola type microcontrollers to set the direction of data transfers.
28 thru 35	AD0 thru AD7	ADDRESS/DATA 0 thru ADDRESS/DATA 7	I/O	Schmitt-triggered inputs. These multiplexed address/data lines are used to load the register/buffer address on the falling edge of ALE, and are used for data transfers to/from the local microcontroller.
43	V_{SS}	GROUND		Ground.

TABLE 2. LOCAL MICROCONTROLLER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
38	XTALIN	CRYSTAL INPUT	I	Crystal oscillator input. The crystal frequency is twice the buffer data rate.
39	XTALOUT	CRYSTAL OUTPUT	O	Crystal oscillator output.
49	$\overline{BOE}$	$\overline{BUFFER}$ OUTPUT ENABLE	O	$\overline{BOE}$ is asserted by the chip to read data from the external SRAM buffer.
50	$\overline{BWE}$	$\overline{BUFFER}$ WRITE ENABLE	O	$\overline{BWE}$ is asserted by the chip to write data into the external SRAM buffer.
51 thru 58	BD0 thru BD7	BUFFER DATA 0 thru BUFFER DATA 7	I/O	Schmitt-triggered. Buffer data bus, which connects directly to a static RAM.
59 thru 73	BA0 thru BA14	BUFFER ADDR 0 thru BUFFER ADDR 14	I/O	Buffer address bus, for direct connection to 32 KB of SRAM. In XT mode, also used to read jumper configuration data in Read Configuration Mode. In input mode, there is a low current internal pulldown.

TABLE 3. BUFFER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
10	WD	WRITE DATA	O	WD is the MFM/NRZ write data written to the disk. It is shifted out at a rate determined by write clock. MFM write data should be synchronized by a D flip flop clocked at 10 MHz (for 5 Mbs operation).
11	LATE/ WCOUT	LATE/ WCOUT	O O	LATE is used along with EARLY in the Write Precompensation circuitry to control the delay of WD. In NRZ mode WCOUT is write clock out which can be used to qualify WD in an ESDI application.
12	AME/ EARLY	ADDRESS MARK ENABLE/EARLY	O	In NRZ mode, this output is the Address Mark Enable signal for an ESDI drive. In MFM or RLL mode, this output is EARLY. EARLY and LATE are used in the Write Precompensation circuitry to control the delay of WD.
13	WG	WRITE GATE	O	WG is asserted when valid data is to be written to the disk. It enables write current to the head and is immediately de-asserted if a WRITE FAULT (WF) is detected.
14	WC	WRITE CLOCK	I	A clock used internally to control WD. (Up to 10 MHz for ST412, up to 15 MHz for ESDI).
15	INDEX	INDEX	I	Schmitt-triggered INDEX input for direct connection to the drive control cable.
16	SCT/ DRUN	SECTOR/ DATA RUN	I	Schmitt-triggered input. In hard sector mode, SCT is used to indicate the start of a sector. In soft sector NRZ mode, SCT indicates Address Mark Found. In soft sector MFM or RLL mode, DRUN indicates a sequence of MFM or RLL '0's or a sequence of MFM '1's has been detected.
17	RD	READ DATA	I	RD is MFM or NRZ read data from the drive. Data and clocks are separated internally for MFM data.
18	RG	READ GATE	O	RG is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
19	RC	READ CLOCK	I	RC is typically generated from an oscillator phase-locked to the read data.
20	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I	Schmitt-triggered. $\overline{WRITE\ FAULT}$ input for direct connection to the drive control cable.
21	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Schmitt-triggered. $\overline{DRIVE\ READY}$ input for direct connection to the drive control cable.
36	$\overline{DS0}$	$\overline{DRIVE\ SELECT\ 0}$	O	High-current open-drain $\overline{DRIVE\ SELECT}$ outputs for direct connection to the drive control cable.
37	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION (CONT'D)

2.0 ARCHITECTURE

2.1 POWER-QUALIFIED RESET

This integrated function is used to reliably initialize flip-flops to a predictable state during the application of V_{DD}. It causes the RESET output signal to be asserted until VDD reaches a given threshold. It also forces a reset if the V_{DD} falls below a specified threshold.

2.2 DRIVE INTERFACE LOGIC

The drive interface contains high-current 48 mA drivers for direct connection of the drive select outputs to the drive control cable. Schmitt trigger input receivers connect the drive interface logic directly to the control cable inputs.

2.3 DRIVE CONTROLLER ORGANIZATION

The controller is composed of the following major sections:

- PLA Control
- CRC/ECC Logic
- MFM/RLL Decoding
- Address Mark Detector
- Buffer and DMA Control
- Task Register File

The controller is designed to operate with 2 clock inputs, READ CLOCK (RC) and WRITE CLOCK (WC). The PLA controller, processor interface, and buffer control sections use the write clock input. The clock inputs are used for MFM, RLL, or NRZ decoding. The clock frequency is 10 MHz for a 10 Mbs data rate.

The controller reads or writes disk data to a 15 Mbs rate for MFM and RLL and 24 Mbs for NRZ. The RLL implementation is a (2,7,2,4,3) code based on the IBM 3370 code. The only difference lies in the assignments of the code words to the 7 different data streams possible. Error propagation for a single bit error is limited to 4 bits.

When programmed in the NRZ mode, the WD42C22C qualifies NRZ disk data using the Sector / Address Mark Detect signal, and also modifies the RG and WG signals to meet ESDI specifications.

In all modes, the length of the PLO sync and gap fields are software programmable. The ID PLO sync field length, the Gap1/Gap3 length, the Gap1/Gap3 data bytes and the ID CRC pad bytes are programmable during the format command. The data PLO sync field length and the data CRC/ECC pad bytes are programmable during the Write command.

Figure 3 is a block diagram of the drive controller section of the WD42C22C.

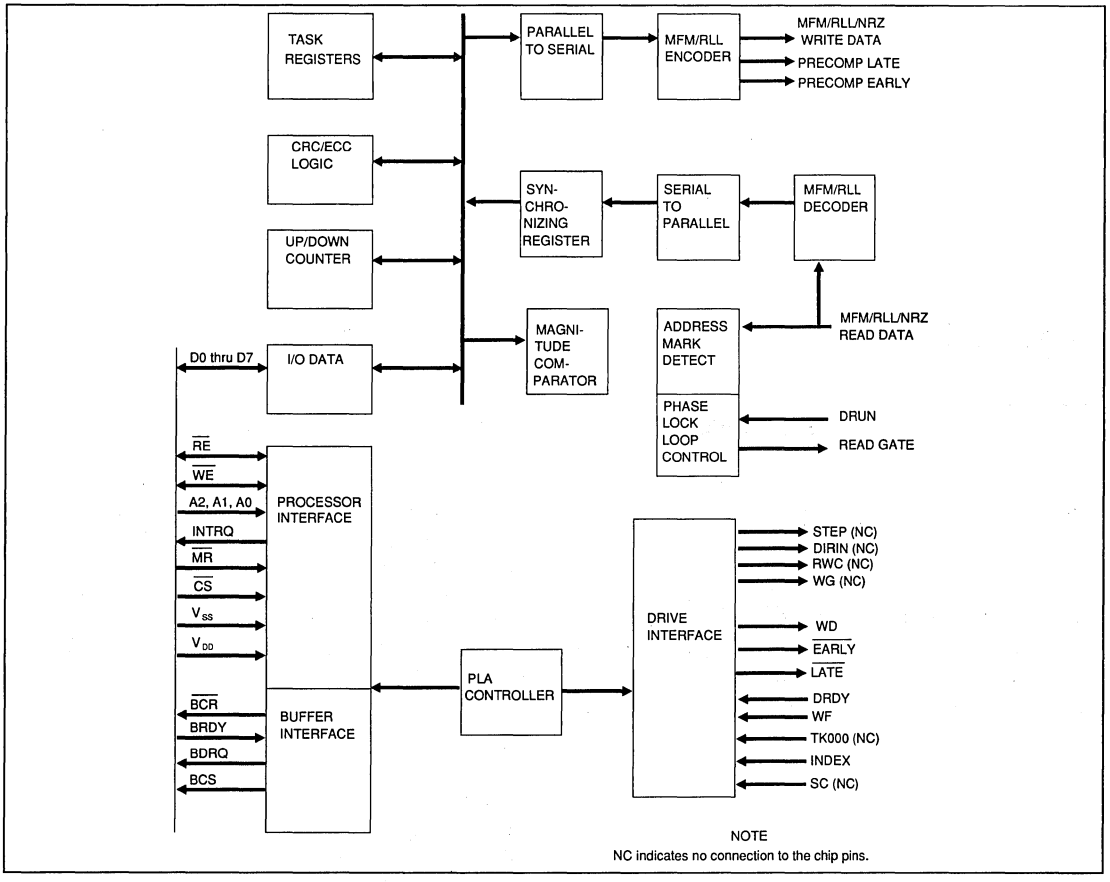

FIGURE 3. DRIVE CONTROLLER BLOCK DIAGRAM

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2.4 PROGRAMMABLE LOGIC ARRAY (PLA) CONTROLLER

The Programmabla Logic Array (PLA) controller interprets commands, e.g. write, read format, etc. This circuitry's operation is synchronized with the WC input. The PLA controller is started when a command is written into the command register. It generates control signals and operates in a handshake mode when communicating with the MFM/RLL decoding block. The MFM/RLL decoding block uses the RC input which may be asynchronous to WC.

2.5 MAGNITUDE COMPARATOR

An 11-bit magnitude comparator calculated drive step direction and number of step pulses between present cylinder position and desired position in earlier Winchester controller versions. This comparator is **not** used in the WD42C22C. A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

2.6 CRC/ECC GENERATOR AND CHECKER

The CRC/ECC generator computes and checks the cyclic redundancy check characters appended to the ID and data fields written on the disk. The CRC mode of operation, defined by the SDH register (bit 7 set to 0) provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it. (Bit 7 of the SDH register will not implement CRC mode for data fields when RLL mode is selected.) The CRC polynomial used is:

$$X^{16} + X^{12} + X^5 + 1$$

The CRC register is preset to all ones before computation starts.

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by setting bit 4 of the error register. If the failure is in the data field, bit 6 of the error register is set.

A 32 bit or 56 bit ECC polynomial may be selected instead of the CRC polynomial for the data field. The CRC/ECC selection is controller by bit 7 of the SDH register when the controller is in MFM or NRZ modes. CRC is selected when bit 7 of the SDH register is 0 in MFM or NRZ modes. ECC is selected when bit 7 of the SDH register is 1 in MFM or NRZ modes. Bit 2 in the set parameter command selects either the 32 bit or 56 bit polynomial. RLL mode defaults to the 56 bit polynomial. The CRC or 32 bit ECC options are **not** usable in RLL mode.

The ECC mode of operation (SDH bit 7 = 1) is only applicable to the data field. This feature built into the WD42C22C provides the user with the ability to detect and correct errors in the data field automatically.

The following is a summary of the parameters considered when ECC is used:

- 1. SDH register bit 7.
- 2. Read and write command bit 1 (L).
- 3. Compute correction command.
- 4. Set parameter command.
- 5. Error occurred, bit 0 of the status register.
- 6. On any ECC error the controller stops regardless of the T bit. (Refer to the read command description.)

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode, for MFM and NRZ only.

When an ECC error is detected, no attempt is made to correct it and bit 0 of the status register and bit 6 of the error register are set. The user now has two choices:

- 1. Ignore the error and make no attempt to correct it.
- 2. Use the compute correction command to determine the pattern and location of the error, and correct it within the user's program.

When implementing the compute correction command, use it before executing commands that alter the content of the ECC register. The read, write, scan, and format commands can alter the syndrome and make correction impossible. If the compution correction command determines that the error is uncorrectable, then the error bits in the status register and error register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The 32-bit ECC polynomial is:

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$$

and is the same one used in the WD1002, WD1003, and WD1006 controller boards. The 32-bit ECC polynomial has an 11 bit maximum single burst correction span. The reverse 32-bit ECC polynomial is:

$$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$$

The non-detection probability for the 32-bit ECC polynomial is:

$$2.3\ (E\text{-}10),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

and the miscorrection probability is:

$$1.57\ (E\text{-}5),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

The 56-bit ECC polynomial is:

$$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^8 + 1$$

The 56-bit ECC polynomial has a 22 bit maximum single burst correction span.

The reverse 56-bit ECC polynomial is:

$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$

The non-detection probability for the 56-bit ECC polynomial is:

1.39 (E-17), $r^{\dagger} = 519 \times 8$, $b^{\dagger} = 11$

and the miscorrection probability is:

5.84 (E-11), $r^{\dagger} = 519 \times 8$, $b^{\dagger} = 11$

The set parameter command selects the number of bits in the correction span, through the use of bit 0.

Read and write commands, with the L bit (bit 1) set to one, are referred to as read long and write long commands. With these commands, no ECC or CRC characters are generated or checked by the WD42C22C. In effect, the four or seven bytes are handled as an additional four or seven bytes of data which pass through the data buffer. With proper use of the write, read long, write long, and read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

For CRC/ECC calculations, the CRC/ECC register is initialized to all 1's. For CRC/ECC purposes only, the address mark byte has a value of "A1" and is included in the CRC/ECC calculations.

2.7 MFM/RLL ENCODING AND MFM/RLL DECODING

The MFM/RLL encoding section receives 8-bit parallel data and generates either MFM or RLL write data depending on the K option in the load parameter block command. This section operates with a write clock having a frequency of the desired bit rate. The write clock need not be synchronized to read clock (RC).

Data bytes are written to the drive most significant bit first. The MFM/RLL decoding section generates 8 bit binary data from MFM or RLL read data once an address mark has been detected. Table 5 lists the RLL coding rules followed by the controller.

NRZ Data				RLL Code Word Output	
First Bit		Last Bit		First Bit	Last Bit
1	1	X	X	1 0 0 0	X X X X
1	0	X	X	0 1 0 0	X X X X
0	1	1	X	0 0 1 0	0 0 X X
0	1	0	X	0 0 0 1	0 0 X X
0	0	0	X	1 0 0 1	0 0 X X
0	0	1	1	0 0 0 0	1 0 0 0
0	0	1	0	0 0 1 0	0 1 0 0

TABLE 5. RLL CODING RULES

When NRZ mode is selected, the MFM/RLL encode and decode logic is bypassed. NRZ read data is clocked in on the rising edge of Read Clock and NRZ write data is clocked out on the rising edge of WC.

2.8 ADDRESS MARK DETECTOR

An address mark is a unique 2 byte code placed at the beginning of each ID field or data field. A series of zero bytes always precedes each address mark. The address mark detector section begins searching for an address mark when synchronization has been lost after a series of zero bytes is detected. The detection of an address mark establishes resynchronization.

The address mark is composed of a 2 byte sequence. The first byte is used for resynchronization and the second byte specifies ID or data field. For the MFM mode, the first byte is an $A1_{16}$ byte with missing clock (data = A1, clock = 0A). The second byte is encoded with normal MFM rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In RLL mode, the first byte is a unique code which violates normal RLL coding rules but does not violate the 2,7 timing rule. The RLL address mark pattern is 1000 0000 1001 0000 (8090_{16}). The second byte is encoded with normal RLL rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In NRZ mode, an NRZ A1 byte establishes byte synchronization. When the WD42C22C is used to control an ESDI (NRZ) drive, the Sector Pulse (Address Mark Found) signal will qualify read data to prevent false address mark detection.

2.9 CONTROLLER TO DATA SEPARATOR INTERFACE

The read interface section generates READ GATE (RG) from signals sent by the PLA controller and by the DRUN input. In this system, raw read data from the drive is presented to the RD in put. RG is low when the controller is not inspecting read data. When a read command is started and a search begins for an address mark, DRUN from the data separator is examined. Since each address mark should be preceded by approximately 12 bytes of zeroes, RG is activated when a sequence of zeroes is detected by DRUN and read data is examined until either an address mark is detected or a non-zero byte which is not an address mark is detected. If an address mark was detected, and it was preceded by at least 8 bytes of zeroes, read gate is held high and the ID or data field can be read.

If a non-zero non-address mark byte was detected, then RG is dropped for at least 2 byte times, allowing the phase lock loop to resynchronize with WC, before inspecting DRUN input again. If the desired ID field was read, then the sector transfer can be made. If a data field was detected or if the ID bytes did not match, or if an address mark was not preceded by eight bytes of zeroes with six coming after RG on, then RG is lowered and DRUN is inspected again for a sequence of zeroes.

Figures 4 illustrates the PLL control sequence for the ID field. Figure 5 illustrates the PLL control sequence for the data field.

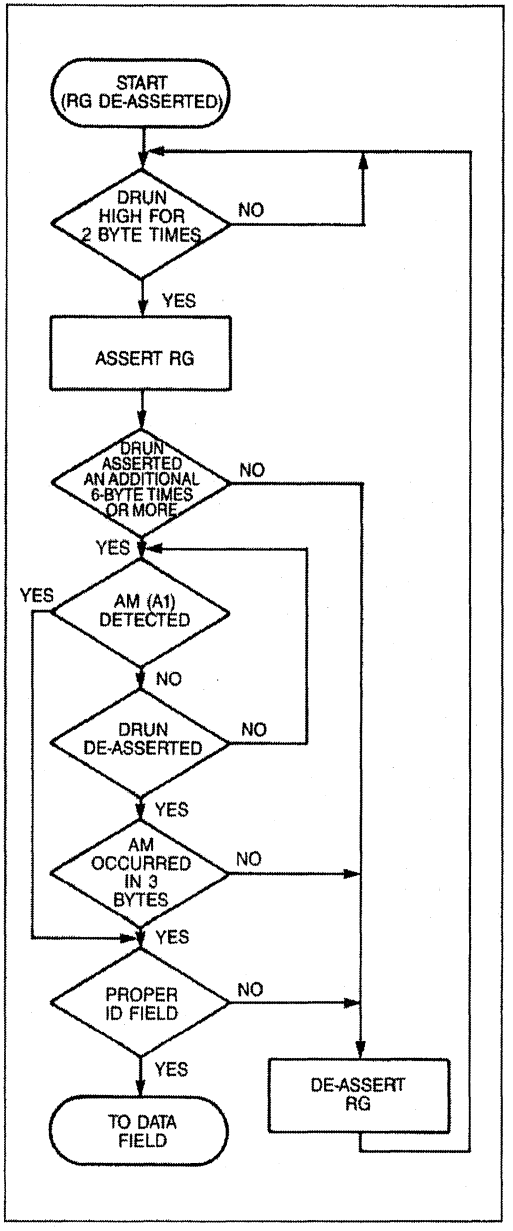

FIGURE 4. PLL CONTROL (ID FIELD)

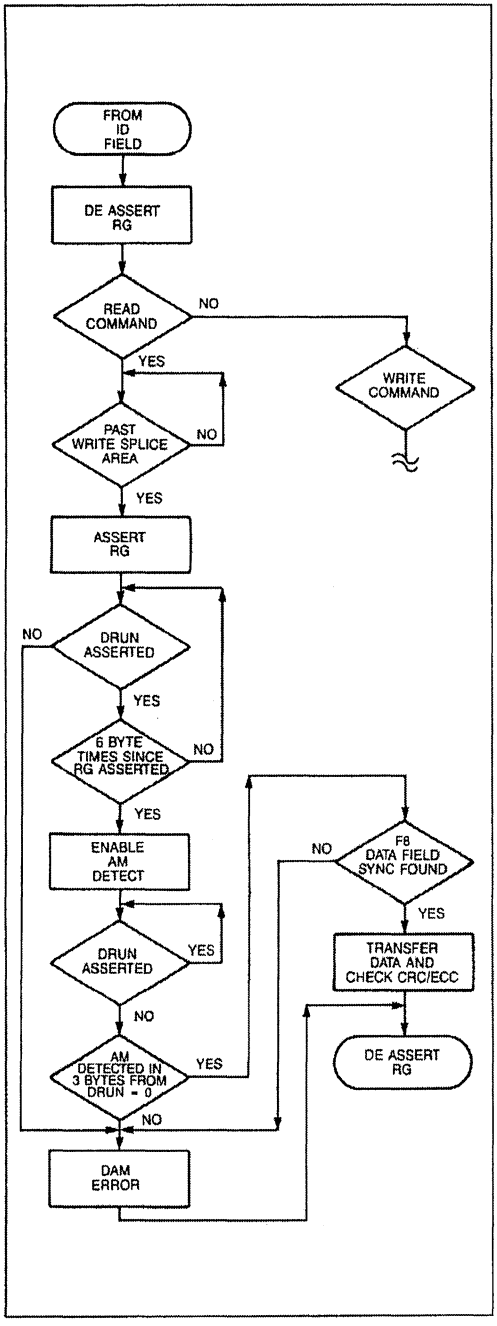

FIGURE 5. PLL CONTROL (DATA FIELD)

The write precompensation circuitry, in the controller to the drive interface, reduces the effects one bit has on another. There are two parts to write precompensation logic, reduced write current (RWC) and shifting of the bits as they are written. The RWC is **NOT** controlled by the drive controller. The local microcontroller should specify when the write current is reduced by asserting its own RWC output.

The shifting of the data bits is controlled by the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs. These two outputs should be used to delay the output as follows in Table 6:

$\overline{\text{EARLY}}$	$\overline{\text{LATE}}$	DELAY
0	1	no delay
1	1	one unit delay
1	0	two units delay

TABLE 6. EARLY AND LATE DELAYS

The $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs are generated according to the rules in Tables 7 (RLL) and 8 (MFM or NRZ).

RLL Coded Data Pattern			
Preceding Bits	Comp. Bit	Following Bits	Precomp
X 1 0 0	1	0 0 0 X	EARLY
X 0 0 0	1	0 0 0 X	None
X 0 0 0	1	0 0 1 X	LATE
0 1 0 0	1	0 0 1 0	None

TABLE 7. EARLY AND LATE GENERATION (RLL MODE)

MFM Coding - NRZ Data Pattern			
Preceding Bits	Comp. Bit	Following Bits	Precomp
X X X 1	1	0 X X X	EARLY
X X X 0	1	1 X X X	LATE
X X 0 0	0	1 X X X	EARLY
X X 1 0	0	0 X X X	LATE

TABLE 8. EARLY AND LATE GENERATION (MFM - NRZ)

3.0 INTERFACE PORTS AND TASK FILES

3.1 HOST INTERFACE ORGANIZATION

The WD42C22C's host interface directly connects to the IBM XT or IBM AT system bus as well as the system bus of any XT or AT compatible. The WD42C22C has high current drivers which allow it to be directly connected to the system bus.

The register configuration for the host interface is dependent on the state of the AT/XT control bit in the interface control register which is written by the local microcontroller.

There is an additional slave host mode. In this mode, the microcontroller communicates to a peripheral device with up to 32 registers through the host interface. The slave device can transfer data to/from the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the SBIC.

The sequence that the microcontroller follows to transfer data between the buffer RAM and the host is defined under the buffer manager description.

3.2 XT HOST INTERFACE

To put the WD42C22C in the XT compatible interface mode the local microcontroller resets the AT/XT control bit. In this mode, HCS should be active when I/O ports 320 (hex) through 323 (hex) are addressed. (XT I/O ports 320 through 323 are primary ports. XT I/O ports 324 through 327 are secondary ports. Unless otherwise noted, information regarding the primary ports is identical to information on secondary ports.) Table 9 lists the port descriptions for this mode.

HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
X	X	0	0	Read data	Write data
X	X	0	1	Hardware status	Hardware reset
X	X	1	0	Drive configuration	Drive select
X	X	1	1	NOT USED	DMA and interrupt control

TABLE 9. XT PORT DESCRIPTIONS

3.2.1 Read Data Port (HA1 Thru HA0 = 0, Read)

The read data port is used to send data and status to the host processor. The data read from this port comes from the buffer RAM under the control of the buffer manager.

3.2.2 Write Data Port (HA1 Thru HA0 = 0, Write)

The write data port is used to send commands and data from the host to the drive controller. The data is written to the buffer RAM under the control of the buffer manager.

3.2.3 Hardware Status (HA1 Thru HA0 = 1, Read)

This port contains the controller hardware status. It can be read by the host at any time. Bit 7, bit 6, bit 2, and bit 1 are written by the local microcontroller. Bit 5, bit 4, bit 3, and bit 0 are controlled by internal logic. The bits are defined as follows:

Bit							
7	6	5	4	3	2	1	0
X	X	IRQ	DRQ	XBSY	C/D	I/O	REQ

3.2.3.1 Bit 5 Interrupt Request

This bit signifies that an interrupt is pending. IRQ reflects the state of the INTRQ output. The INTRQ pin is tri-stated and the IRQ status bit and internal interrupt flip-flop are reset when the host disables the interrupt or when the WD42C22C is reset, either by the host or by asserting master reset.

3.2.3.2 Bit 4 Dma Request

This bit signals that the WD42C22C is ready for a DMA transfer to take place. The direction of the transfer is determined by the I/O bit. This bit reflects the state of the DREQ output.

3.2.3.3 Bit 3 XT Busy

This bit indicates that the WD42C22C is busy executing a command and is unable to accept another command. This bit is set by during a reset.

3.2.3.4 Bit 2 Command / $\overline{\text{Data}}$

This bit tells the host which type of transfer is expected at the read and write data ports. C/D set to 1 indicates that a command or status transfer is expected. C/D set to 0 indicates that a data transfer is expected.

3.2.3.5 Bit 1 Input / $\overline{\text{Output}}$

This bit tells the host the direction of transfer for the two data ports. I/O set to 1 indicates an input (read) by the host and I/O set to 0 indicates an output (write) by the host.

3.2.3.6 Bit 0 Request

This bit is one of the handshaking signals between the host and WD42C22C. When transferring data to/from, the WD42C22C's read data and write data ports by the host, assertion of this bit informs the host that the WD42C22C is ready for the transfer.

3.2.4 Controller Reset (HA1 Thru HA0 = 1, Write)

When this port is written, regardless of the data written, the RESET output is asserted if enabled. If the reset has been disabled by the local microcontroller, then writing to this port asserts MCINT and the local microcontroller is responsible for resetting the logic on the drive controller board.

3.2.5 Drive Configuration Information (HA1 Thru HA0 = 2, Read)

This register, when read, informs the host about the configuration of the drive(s) attached. This configuration information is written by the local microcontroller.

3.2.6 Controller Select (HA1 Thru HA0 = 2, Write)

When this port is written, regardless of the data written, the MCINT output is asserted to inform the local microcontroller that the controller board has been selected.

3.2.7 DMA and Interrupt Mask (HA1 Thru HA0 = 3, Write)

This port enables or disables the DMA and interrupt to the host. When IRQEN is set to 1, then interrupts to the host are enabled. This bit is cleared when the WD42C22C is reset. The INTRQ line is tri-stated and the host interrupt is cleared when the interrupts are disabled. When DRQEN is set to 1, then DMA requests to the host are enabled. This bit is cleared when the WD42C22C is reset.

Bit							
7	6	5	4	3	2	1	0
X	X	X	X	X	X	IRQ EN	DRQ EN

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ABSY	HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
					AT TASK FILE COPY	
0	0	0	0	0	Read Data (16 bits)	Write Data (16 bits)
0	0	0	0	1	Host Error Register	Write Precomp Cylinder
0	0	0	1	0	Sector Count	Sector Count
0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	1	0	SDH	SDH
0	0	1	1	1	Host Status Register	Host Command Register
1	0	X	X	X	Host Status Register	INVALID
					CONTROL PORTS	
X	1	1	1	0	Alternate Status Register	Fixed Disk Register
X	1	1	1	1	Digital Input Register*	NOT USED

*Bit 7 is tri-stated when the digital input register is read to accomodate the floppy disk change status.

TABLE 10. AT MODE PORT DESCRIPTIONS

3.3 AT HOST INTERFACE

To put the WD42C22C in the AT compatible interface mode, the AT/XT control bit is set by the local microcontroller. The HCS chip select should be active when I/O ports $1F0_{16}$ through $1F7_{16}$ and $3F6_{16}$ and $3F7_{16}$ are addressed for primary addressing and for I/O ports 170_{16} through 177_{16} and 376_{16} and 377_{16} for secondary addressing. Only address signals HA8 through HA3 and AEN need to be decoded to generate HCS. Table 10 describes the ports for AT mode as follows:

When port 0 is accessed the $\overline{\text{IOCS16}}$ output is asserted when in AT programmed I/O mode. All buffer data transfers are 16 bits. The ECC byte transfers in a long mode (read or write) are 8 bit transfers. All other register transfers are 8 bits.

Registers 1 through 7 are an identical copy of the drive controller task registers 1 through 7. These registers can be read or written by the host only when the ABSY status bit is not active. Any attempt by the host to read the AT task file copy while ABSY is active results in the host status register being read. The AT task file copy registers cannot be written by the host while ABSY is active.

3.3.1 Error Register (HA9, HA2 Thru HA0 = 01, Read)

The error register is read only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	0	IDNF	0	AC	TK0	DMNF

3.3.1.1 Bit 7 Bad Block

A bad block address mark has been detected when trying to read or write that sector. The data field will not be read or written.

3.3.1.2 Bit 6 CRC/ECC Data Field Error

An uncorrectable ECC error or a CRC error was detected in the data field.

3.3.1.3 Bit 5 Reserved

Not used, forced to zero.

3.3.1.4 Bit 4 ID Not Found

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For read and write sector commands, with the retry disable bit reset, this bit indicates that after 10 index pulses, an auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set, then no matching ID field was found after 2 index pulses; no auto-scan or auto-seek is performed.

3.3.1.5 Bit 3 Reserved

Not used, forced to zero.

3.3.1.6 Bit 2 Aborted Command

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.3.1.7 Bit 1 Track 0 Error

This bit, when set, indicates an error detecting Track 0 during a restore.

3.3.1.8 Bit 0 Data Address Mark Not Found

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.3.2 Write Precomp Cylinder Register (HA9, HA2 Thru HA0 = 01, Write)

This register is used to control the Reduce Write Current (RWC) signal going to the drive. RWC is turned on if the present position cylinder number is greater than or equal to the 4 times the write precomp cylinder number. If the write precomp cylinder number is FF_{16}, then the RWC is never asserted.

3.3.3 Sector Count (HA9, HA2 THRU HA0 = 02, Read/Write)

This register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count is decremented and the sector number is incremented after each sector transfer between the buffer and host or drive.

3.3.4 Sector Number (HA9, HA2 Thru HA0 = 03, Read/Write)

The sector number register is used to hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.

3.3.5 Cylinder Number Low And High Registers (Cylinder Number Low: HA9, HA2 Thru HA0 = 04, Read/Write. Cylinder Number High: HA9, HA2 Thru HA0 = 05, Read/Write)

These registers specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047. Cylinder number low register holds the 8 least significant bits of the desired cylinder number. Cylinder number high register holds the three most significant bits of the desired cylinder number in bits 0 through 2. Bits 3 through 7 are not normally used in disk controller boards. These bits are latched when writing to this register. This means that all 8 bits can be used to transfer information between the host and the local microcontroller.

3.3.6 SDH Register (HA9, HA2 Thru HA0 = 06, Read/Write)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode.

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	0	SS	Drive Number	Head Number			

3.3.6.1 Bit 7 ECC/CRC Select

This bit is set for data field ECC mode. It is reset for data field CRC mode.

3.3.6.2 Bit 5 Sector Size

Bit 5 (SS0) is used to select sector size. If SS0 = 0, then the sector size is 256 bytes and if SS0 = 1, then the sector size is 512 bytes.

3.3.6.3 Bit 4 Drive Select

Bit 4 specifies the desired drive number. This bit also determines which of the two internal drive status registers are read when the host accesses the host status register or alternate status register. If DS = 0, the host receives drive zero status. If DS = 1, then the host receives drive one status.

3.3.6.4 Bits 3 Thru 0 Head Number

Bits 3, 2, 1 and 0 specify the desired head number.

3.3.7 Host Status Register (HA9, HA2 Thru HA0 = 7, Read)

The status register reads only and reflects the status of the controller as well as the status of certain drive control lines. Some of the status bits are controlled by the local microcontroller. Drive status comes from two registers in the WD42C22C, one for each drive. Bit 4 of the SDH register in the AT task file copy controls which of the two registers is read when the host reads this port. Reading of the status register by the host resets INTRQ. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
ABSY	RDY	WF	SC	DRQ	DWC	IDX	ERR

3.3.7.1 Bit 7 AT Busy

This bit is set to 1 when the controller is accessing the disk. ABSY is activated by the start of a command (writing into the host command register). It is deactivated at end of all commands by the local microcontroller. This bit is also set during a reset.

3.3.7.2 Bit 6 Drive Ready

This bit reflects the state of the DRDY drive status pin. Any command aborts if DRDY is low. This bit is written by the local microcontroller.

3.3.7.3 Bit 5 Write Fault

This bit reflects the state of the WF drive status pin. Any command aborts if WF is high. This bit is written by the local microcontroller.

3.3.7.4 Bit 4 Seek Complete

This bit reflects the state of the SC signal coming from the drive. This bit is written by the local microcontroller.

3.3.7.5 Bit 3 Data Request

This bit is asserted when the host should be transferring data between the RAM buffer and host. This bit is controlled by the buffer manager.

3.3.7.6 Bit 2 Data Was Corrected

This bit indicates that an error in the data field was detected and corrected. The buffer contains corrected data. This bit is written by the local microcontroller.

3.3.7.7 Bit 1 Index

This bit reflects the state of the INDEX pin.

3.3.7.8 Bit 0 Error

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is active. This bit is written by the local microcontroller.

3.3.8 Host Command Register (HA9, HA2 Thru HA0 = 7, Write)

The command to be executed is written into this register. Writing this register sets ABSY in the status register and asserts the MCINT pin going to the local microcontroller. The command latches in a register which the local microcontroller reads. Writing this register resets INTRQ.

3.3.9 Alternate Status Register (HA9, HA2 Thru HA0 = E, Read)

This register is the same as the host status register (7) but mapped at a different address. Refer to page 23 for the bit description.

3.3.10 Fixed Disk Register (HA9, HA2 Thru HA0 = E, Write)

The fixed disk register is used by the host to control some of the internal functions of the WD42C22C. Bit 0 and bits 4 through bit 7 are reserved for future definition. These bits are currently not used in the AT protocol but they are implemented in the WD42C22C, i.e. the fixed disk register passes 8 bits between the host and the local microcontroller. The host should write zeroes to these bits in AT mode. The fixed disk register is coded as follows:

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.3.10.1 Bit 3 Head Select 3 Enable

When HS3EN = 1, then HEAD SELECT 3 is asserted by the local microcontroller. When HS3EN = 0, then RWC is asserted by the local microcontroller.

3.3.10.2 Bit 2 Reset

Writing a 1 to this bit resets the WD42C22C. The RESET output is asserted and remains asserted until this bit is written back to 0. This bit must be on for a minimum of 5.0 µsec. If reset has been disabled by the local microcontroller then writing a '1' to this bit only resets the WD42C22C. RESET is not asserted in this case. The WD42C22C asserts MCINT and the local microcontroller is responsible for resetting the drive controller board logic.

3.3.10.3 Bit 1 $\overline{\text{Interrupt Enable}}$

When $\overline{IEN}$ = 0, then the INTRQ output to the host is enabled. When $\overline{IEN}$ = 1, then the INTRQ output to the host is disabled. Disabling interrupts does NOT reset an existing interrupt but inhibits all further interrupts. Any interrupts pending when this bit is set causes the INTRQ output to be asserted. A system master reset does NOT affect the $\overline{IEN}$ bit but resets any existing interrupt. The internal power qualified reset sets $\overline{IEN}$ to 0. When interrupts are disabled, then the INTRQ pin is tri-stated.

A D 7	A D 6	A D 5	A D 4	A D 3	A D 2	A D 1	A D 0	READ PORT	WRITE PORT
DISK CONTROLLER TASK FILE									
0	0	0	X	X	X	X	X	BUS TRISTATE	NOT USED
0	0	1	0	0	0	0	0	INVALID	INVALID
0	0	1	0	0	0	0	1	Error Register	PLO Length
0	0	1	0	0	0	1	0	Sector Count	Sector Count
0	0	1	0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	0	0	1	1	0	SDH	SDH
0	0	1	0	0	1	1	1	Status Register	Command Register
XT									
0	0	1	0	1	1	0	1	Hardware Status	Hardware Status
0	0	1	0	1	1	1	0	NOT USED	Drive Configuration
BUFFER MANAGER									
0	0	1	1	0	0	0	0	Host Buffer Pointer Low	Host Buffer Pointer Low
0	0	1	1	0	0	0	1	Host Buffer Pointer High	Host Buffer Pointer High
0	0	1	1	0	0	1	0	Host Transfer Count Low	Host Transfer Count Low
0	0	1	1	0	0	1	1	Host Transfer Count High	Host Transfer Count High
0	0	1	1	0	1	0	0	Disk Buffer Pointer Low	Disk Buffer Pointer Low
0	0	1	1	0	1	0	1	Disk Buffer Pointer High	Disk Buffer Pointer High
0	0	1	1	0	1	1	0	Microcontroller RAM Access	Microcontroller RAM Access
0	0	1	1	0	1	1	1	Buffer Status	Buffer Control

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP

3.3.11 Digital Input Register (HA9, HA2 Thru HA0 = F, Read)

The digital input register is used by the host to determine the state of WRITE GATE and the drive selects and head selects. Bit 5 is written by the local microcontroller when HS3EN (bit 3 of the fixed disk register) is set to zero. Bit 5 comes from bit 3 of the host SDH register with HS3EN set to one. Bits 0 through bit 4 also come from the host SDH register. When this register is read by the host, then HD7 (pin 82) is tri-stated. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
X	$\overline{WG}$	$\overline{HS3/RWC}$	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS2}$	$\overline{DS1}$

ABSY	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	READ PORT	WRITE PORT
MISC.										
X	0	0	1	1	1	0	0	0	Interface Status	Interface Control
X	0	0	1	1	1	0	0	1	Configuration Status Low	NOT USED
X	0	0	1	1	1	0	1	0	Configuration Status High	NOT USED
X	0	0	1	1	1	0	1	1	Drive Interface Status	Drive Interface Control
X	0	0	1	1	1	1	0	0	Alternate Sector Number	NOT USED
AT INTERFACE										
X	0	0	1	0	1	0	1	0	AT Control Register	AT Control Register
X	0	0	1	1	1	1	0	1	Drive 0 Status	Drive 0 Status
X	0	0	1	1	1	1	1	0	Drive 1 Status	Drive 1 Status
X	0	0	1	1	1	1	1	1	Fixed Disk Register	Digital Input Register
AT INTERFACE (TASK FILE COPY)										
1	0	1	0	0	0	0	0	1	Write Precomp Cylinder	Error Register
1	0	1	0	0	0	0	1	0	Sector Count	Sector Count
1	0	1	0	0	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
1	0	1	0	0	0	1	0	1	Cylinder Number High	Cylinder Number High
1	0	1	0	0	0	1	1	0	SDH	SDH
1	0	1	0	0	0	1	1	1	Command Register (from Host)	NOT USED
SLAVE HOST										
0	0	1	0	0	0	X	X	X	INVALID	INVALID
X	0	1	0	0	1	0	0	0	INVALID	Slave Address Port for reads
X	0	1	0	0	1	0	0	1	Slave Read Data	Slave Write Data
X	0	1	0	0	1	0	1	0	INVALID	Slave Address Port for writes
X	0	1	0	0	1	X	X	X	INVALID	NOT USED
X	0	1	0	1	X	X	X	X	INVALID	NOT USED
X	0	1	1	X	X	X	X	X	BUS TRISTATE	NOT USED
X	1	X	X	X	X	X	X	X	BUS TRISTATE	NOT USED

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP (CONT'D)

3.3.11.1 Bit 6 Write Gate On

This bit reflects the state of the $\overline{WG}$ output pin.

3.3.11.2 Bit 5 Head Select 3/ Reduce Write Current

This bit reflects the state of the $\overline{HS3}/\overline{RWC}$ drive control output. The $\overline{RWC}$ bit is written

by the local microcontroller. $\overline{HS3}$ comes from the SDH register bit 3.

3.3.11.3 Bit 4, Bit 3, And Bit 2 Head Selects

These bits reflect the states of the $\overline{HS2}$, $\overline{HS1}$, $\overline{HS0}$, and drive control outputs respectively. These bits are controlled by SDH register bits 2 through 0 respectively.

3.3.11.4 Bit 1 And Bit 0 Drive Selects

These bits indicate which drive is currently being selected by the host. They are controlled by the SDH register bit 4.

3.4 SLAVE HOST INTERFACE

In slave mode, the WD42C22C host interface can be hooked up to a peripheral device such as the WD33C93 (SBIC). The microcontroller reads and writes the peripheral device through the WD42C22C using the ports as follows:

ABSY	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	READ PORT	WRITE PORT
X	0	1	0	0	1	0	0	0	Bus tri-state	Slave address port for reads
X	0	1	0	0	1	0	1	0	Bus tri-state	Slave address port for writes
X	0	1	0	0	1	0	0	1	Slave read data	Slave write data

The slave peripheral connects to the WD42C22C using an ALE type interface. Register reads and writes are always 8-bit. The procedure to read or write a slave peripheral register is to first write the register number to the slave address port before the register contents are read or written. This address must always be written before each register access even when consecutively accessing the same register two or more times.

Data transfers between the peripheral device and the WD42C22C are WD-bus mode and can be either 8-bit or 16-bit and is controlled by the H16/8 bit (bit 1 of the auxilliary buffer control register). The slave mode is enabled by the HSMB bit (bit 6 of the auxilliary buffer control register).

3.5 LOCAL MICROCONTROLLER INTERFACE ORGANIZATION

The local microcontroller controls the host interface mode (AT or XT) and controls the buffer manager and the drive controller. The local microcontroller is usually in a sleep state until it is told to do something by the assertion of the $\overline{MCINT}$ output. In the XT mode, $\overline{MCINT}$ is asserted when the controller is selected. In the AT mode, $\overline{MCINT}$ is asserted when the host writes to the command register. In slave host mode, $\overline{MCINT}$ is asserted when the slave peripheral device asserts its INTRQ signal. $\overline{MCINT}$ is also asserted at the end of each host or disk transfer regardless of the interface mode.

The local microcontroller can have either the Intel-type (8051) or the Motorola-type (68HC11) interface. The WD42C22C has a built-in MOtorola-inTEL (MOTEL) circuit which can sense the processor interface type and can therefore be directly interfaced to either type processor.

Table 11 lists the register map for the local microcontroller.

3.6 DISK CONTROLLER TASK FILE (AD7 THRU AD0 = 20 THRU 27)

3.6.1 Error Register (AD7 Thru AD0 = 21, READ)

The error register reads only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	RIDF	IDNF	0	AC	0	DMNF

3.6.1.1 Bit 7 Bad Block

A bad block address mark has been detected when trying to read or write that sector. The data field is not be read or written.

3.6.1.2 Bit 6 CRC/ECC Data Field Error

A CRC error in the data field has been detected when in CRC mode. In ECC mode, data errors were detected in the data.

3.6.1.3 Bit 5 Relocation ID Found

This bit is set if a relocation ID is found after detecting the bad block mark in the desired sector's ID field. This bit is only valid if the R option is used in the set parameter command.

3.6.1.4 Bit 4 ID Not Found

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For a scan ID command, this bit is set after 10 index pulses if the retry disable bit is not set. Otherwise, IDNF is set after 2 index pulse if no ID was found. For read and write sector commands with the retry disable bit set, this bit indicates that after 10 index pulses, auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set and no matching ID field was found after 2 index pulses, then no auto-scan or auto-seek is performed.

3.6.1.5 Bit 3 Reserved

Not used, forced to zero.

3.6.1.6 Bit 2 Aborted Command

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.6.1.7 Bit 1 Reserved

Not used in WD42C22C, forced to zero.

3.6.1.8 Bit 0 Data Address Mark Not Found

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.6.2 PLO Length Register (AD7 Thru AD0 = 21, Write)

This register is used for two purposes:

- 1. To determine the length of the Data PLO sync field during write commands and to determine the length of the ID PLO sync field during format commands. The contents of this register regulates the PLO field size in all data coding modes.
- 2. To load a value in the internal GAP register. During the load parameter block command, the contents of the lower six bits of the PLO length register are transferred to the internal GAP register. In hard sector NRZ (ESDI) mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the leading edge of READ GATE. In hard sector MFM or RLL mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the falling edge of the internally generated DRUN signal. In hard sector MFM or RLL mode, RG is asserted 2 byte times after INDEX or SECTOR. This GAP register is altered by loading the desired GAP register value into the PLO length register and then issuing a load parameter block command.

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3.6.3 Sector Count (AD7 Thru AD0 = 22, Read/Write)

Bit							
7	6	5	4	3	2	1	0
NUMBER OF SECTORS/GAP VALUE SECTOR WITH BAD BLOCK							

This register is used for three purposes:

- 1. The sector count register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count decrements

and sector number increments after each sector transfer to or from the buffer.

- 2. To load a value into the internal gap value register. During the load parameter block command the contents of this register are transferred into an internal gap value register. This gap value register specifies the data byte written into the gaps during format commands.
- 3. To specify to the microcontroller the sector number where a bad block bit was detected if relocation ID searches are enabled. If the R option is set in a set parameter command, then during read and write commands if a bad block is detected, the WD42C22C searches for a special ID field containing relocation information. When the command terminates due to a bad block, then the sector number of the sector with the bad block is returned to the microcontroller in this register. This is true whether or not the relocation information is detected.

3.6.4 Sector Number (AD7 Thru AD0 = 23, Read/Write)

Bit							
7	6	5	4	3	2	1	0
SECTOR NUMBER / GAP SIZE							

The sector number register has three uses:

- 1. To hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.
- 2. To control the Gap 1 and Gap 3 sizes during format commands. The sector number holds the number of gap bytes minus three for format (number of gap bytes minus six for NRZ mode).
- 3. To load a value into the internal pad value register. During the load parameter block command, the contents of this register are transferred into an internal pad value register. This pad value register specifies the data byte written into the ID and DATA pads during format and write commands

3.6.5 Cylinder Number Registers (Cylinder Number Low: AD7 Thru AD0 = 24, Read Write Cylinder Number High: AD7 Thru AD0 = 25, Read/Write)

This register has two functions:

- 1. To specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047.
- 2. The cylinder number register is used during a load parameter block command to specify the desired sector size if a non-standard sector size is desired and to specify the offset for a write ID command. To load the internal sector size register, write in the desired sector size into the cylinder registers. Next, issue a load parameter block command. Set U=1 to enable the programmable sector size or programmable write ID offset.

3.6.6 Cylinder Number Registers (Cylinder Number Low: AD7 Thru AD0 = 24, Read/Write Cylinder Number High: AD7 Thru AD0 = 25, Read/Write)

Cylinder number low register holds the 8 least significant bits of the desired cylinder number or the 8 least significant bits of the desired sector size.

Cylinder number high register holds the three most significant bits (bits 0 through 2) of the desired cylinder number or the three most significant bits of the desired sector size. Bits three through seven of the cylinder number high register are not used and must be set to zero.

3.6.7 SDH Register (AD7 Thru AD0 = 26, Read/Write)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode. There are two SDH modes available, three or four bit head number. Three bit head mode is the default after a master reset. Setting the H bit in the set parameter command engages the four bit head mode.

3.6.7.1 SDH Register, Three-Bit Head Number

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	0	Head #		

3.6.7.2 SDH Register, Four-Bit Head Number

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	Head #			

3.6.7.3 Bit 7 ECC/CRC Select

This bit is set for data field ECC mode. It is reset for data field CRC mode. In RLL mode, this bit is ignored. RLL mode always uses 7-byte ECC. The CRC/ECC flag bit is not written on the disk at format time. The bad block flag is written on the disk in its place.

3.6.7.4 Bit 6 and Bit 5 Sector Size

Bits 6 and 5 contain sector size bits. These bits are written on the disk at format time. These bits should be 0 if programmable sector size is used. These bits are reserved for special flags in programmable sector size mode. The possible sector sizes and their selection codes are as follows:

SS1	SS0	Sector Size
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field
1	1	128 byte data field

The sector sizes can be optionally specified to be any value between 100 and 2048 bytes by using the load parameter block command. The user is responsible for validating the effectiveness of the ECC for sector sizes over 1056 bytes.

3.6.7.5 Bit 4 and Bit 3 Reserved Bit 4 Drive Number Reserved

Reserved. Set to 0.

3.6.7.6 Bit 2, Bit 1, And Bit 0 Three Bit Head Number Bit 3, Bit 2, Bit 1, And Bit 0 Four Bit Head Number

Bits 2, 1, and 0 specify the desired head number in the three bit mode. Bits 3, 2, 1, and 0 specify the desired head number in four bit mode. The local microcontroller is responsible for outputting these bits to the drive.

NOTE

These bits are written on the disk at format time. The SDH byte written in the ID field during a format command is NOT the same as the SDH register. The SDH format byte is shown below:

3.6.7.7 SDH ID Field Format Byte (Three Bit Head Mode)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	0	Head #		

3.6.7.8 SDH ID Field Format Byte (Four Bit Head Mode)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	Head #			

3.6.8 Status Register (AD7 Thru AD0 = 27, Read)

The status register is read only and reflects the status of the controller as well as the status of certain drive control lines. If command in progress (bit 1) is set then no other register reads are valid and none of the other register bits are valid. The status register contents are returned for any read and all writes are disabled. The description of the

status register bits follows:

Bit							
7	6	5	4	3	2	1	0
0	RDY	WF	1	0	0	0	ERR

3.6.8.1 Bit 7 Always 0

This bit is always zero when the microcontroller has access to this status register.

3.6.8.2 Bit 6 Drive Ready

This bit reflects the status of the DRDY. Any command aborts if DRDY is low.

3.6.8.3 Bit 5 Write Fault

This bit reflects the state of the WF pin. Any command aborts if WF is high.

3.6.8.4 Bit 4 Always 1

This bit reflects the state of the SC input to the drive controller. This signal is internally tied to V_{DD}.

3.6.8.5 Bit 3 Always 0

This bit reflects the state of the BDRQ signal that goes between the drive controller and the buffer manager. It is always zero when the microcontroller has access to this status register.

3.6.8.6 Bit 2 Not Used

Forced to 0

3.6.8.7 Bit 1 Always 0

This bit reflects the state of the command in progress signal in the drive controller. It is always zero when the microcontroller has access to this status register.

3.6.8.8 Bit 0 Error

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is asserted.

Drive ready and write fault bits reflect the state of their associated input pins. The states of these status register bits are latched at the end of the command and are unlatched after the first status register read. Reading the status register results in the disk controller interrupt being reset.

3.6.9 Command Register (AD7 Thru AD0 = 27, Write)

The command to be executed is written into this register. Writing this register sets the internal BUSY and CIP signals and causes the controller to start executing the desired command. Writing this register resets the disk controller interrupt (DCI bit in the interface status register).

3.7 XT Interface Ports

3.7.1 XT Host Hardware Status (AD7 Thru AD0 = 2D, Read/Write)

Bits 7, 6, 2, and 1 of this register are written by the local microcontroller and read by the host. The other bits reflect the state of certain hardware signals. This register is readable and valid in all host modes.

Bit							
7	6	5	4	3	2	1	0
1	1	IRQ	DRQ	XBSY	C/$\overline{D}$	I/$\overline{O}$	REQ

3.7.1.1 Bits 6 And 7 Undefined

These bits are currently undefined in the XT protocol and read as 1.

3.7.1.2 Bit 5 Interrupt Request

This bit reflects the state of the INTRQ output. This bit can NOT be written by the microcontroller.

3.7.1.3 Bit 4 DMA Request

This bit reflects the state of the DREQ output. This bit can NOT be written by the microcontroller.

3.7.1.4 Bit 3 XT Busy

This bit reflects the state of the internal XT BUSY flipflop. This bit is set by during a reset and is set when the WD42C22C is selected in XT mode. This bit can NOT be written by the microcontroller.

3.7.1.5 Bit 2 Command / $\overline{\text{Data}}$

This bit tells the host which type of transfer is expected at the read data and write data ports. C/D = 1 indicates that a command or status transfer is expected and C/D = 0 indicates that a data transfer is expected. This bit is written by the microcontroller.

3.7.1.6 Bit 1 Input / $\overline{\text{Output}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{\text{O}}$ = 1 indicates an input (read) by the host and I/$\overline{\text{O}}$ = 0 indicates an output (write) by the host. This bit is written by the microcontroller.

3.7.1.7 Bit 0 Request

This bit indicates the state of the internal host transfer enable. This bit is active when the buffer manager is transferring data between the RAM and the host. This bit can NOT be written by the microcontroller. This bit is identical to the DRQ in the drive zero status and drive one status registers used in AT mode.

3.7.2 Host Drive Configuration (AD7 Thru AD0 = 2E, Write)

This register is used to write the drive configuration information that is read by the host.

3.7.3 Buffer Manager Registers (AD7 Thru AD0 = 30 Thru 37) Host Buffer Pointer Low (AD7 Thru AD0 = 30, Read/Write) Host Buffer Pointer High (AD7 Thru AD0 = 31, Read/Write)

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BITS OF HOST BUFFER POINTER						

The host buffer pointer low register contains the least significant byte of the host buffer pointer. The host buffer pointer high register contains the seven most significant bits of the host buffer pointer. The host buffer pointer is used as the base address for the internal host buffer counter. The contents of the host buffer pointer registers are transferred to the host buffer pointer counter under the control of the buffer control register.

When the AHBP bit is set in the control register, then the pointer register is transferred to the pointer counter when the transfer counter reaches zero. If the transfer count is already zero, then the transfer occurs immediately. This allows a pending transfer to be queued behind the current transfer. When the pointer is transferred to the counter, the AHBP buffer status bit resets.

3.7.4 Host Transfer Count Low (AD7 Thru AD0 = 32, Read/Write Host Transfer Count High (AD7 Thru AD0 = 33, Read/Write)

The host transfer count low register contains the least significant byte of the host transfer count. The host transfer count high register contains the most significant bits of the host transfer count. The transfer count controls the number of bytes that are to be transferred on the host interface. The transfer count register is transferred to the internal transfer counter at the same time that the host buffer pointer register is transferred to the host buffer pointer counter. The transfer counter is 12 bits long which gives a maximum transfer

count of 4095 bytes.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST TRANSFER COUNT							

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	MS BITS OF HOST TRANSFER COUNT			

3.7.5 Disk Buffer Pointer Low (AD7 Thru AD0 = 34, Read/Write) Disk Buffer Pointer High (AD7 Thru AD0 = 35, Read/Write)

The disk pointer low register contains the least significant byte of the disk buffer pointer. The disk pointer high register contains the seven most significant bits of the disk buffer pointer. The disk buffer pointer is used as the base address for the internal disk buffer counter. The contents of the disk buffer pointer registers are transferred to the disk buffer pointer counter under the control of the buffer control register. When the ADBP bit is set in the control register, then the pointer is transferred to the counter when the drive controller sets DRQI to 1 (bit 1) in the interface status register (38_{16}). This allows a pending transfer to be queued behind the current transfer. When the pointer register is transferred to the counter, the ADBP bit in the buffer status resets. If ADBP=0 when the drive controller sets DRQI to 1, then the drive controller stops transferring data to the buffer and discontinues the command until ADBP sets.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF DISK BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BYTE OF DISK BUFFER POINTER						

3.7.6 Microcontroller RAM Access Port (AD7 Thru AD0 = 36, Read/Write)

This port is used by the local microcontroller to access the buffer RAM. Accesses to this port go through the drive controller's FIFO. These accesses are enabled by the MAC bit in the drive interface control register. The DRWB bit in the buffer manager control register controls the direction of the accesses.

3.7.7 Buffer Control Register (AD7 Thru AD0 = 37, Write)

This register is used to control the buffer manager.

Bit			
7	6	5	4
AT/$\overline{XT}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.7.1 Bit 7 AT / $\overline{XT}$ INterface Control

This bit, along with HSMB, in the auxilliary buffer control register, controls the host interface type. If AT/$\overline{XT}$ = 0, then the interface is XT type if HSMB = 0. If AT/$\overline{XT}$ = 1, then the interface is AT type if HSMB = 0. This bit has no meaning if HSMB = 1. The RESET input and the host soft reset does not affect this bit.

3.7.7.2 Bit 6 Read Configuration

When this bit is set, all buffer address outputs are placed in a medium impedence state with each buffer address pin having a 180 µA current source pulldown. The buffer manager should be idle when this mode is enabled. This mode is used to read configuration switch information. The microcontroller should wait 100 µsec after setting this bit before reading the configuration registers. This bit resets when $\overline{RESET}$ is asserted.

3.7.7.3 Bit 5 Reset Transfer Counter

When this bit is set, the internal transfer counter and the host FIFO pointers reset. This bit resets after the transfer counter and FIFO reset.

3.7.7.4 Bit 4 Arm Host Buffer Pointer

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then when the internal transfer counter reaches zero the host buffer pointer is transferred to the internal host buffer counter and the host transfer count is transferred to the internal transfer counter. This bit is reset by the WD42C22C after the host pointer and count registers are transferred. This bit resets when RESET is asserted.

3.7.7.5 Bit 3 Host Read / Write

This bit controls the direction of the host data transfers. It is used internally to control the direction of the FIFO. When HRWB = 0, then the host writes to the WD42C22C. When HRWB = 1, then the host reads from the WD42C22C.

3.7.7.6 Bit 2 Disk Read / Write

This bit controls the direction of the disk or local microcontroller data transfers. It is used internally to control the direction of the disk FIFO. When DRWB = 0, then the disk controller or local microcontroller writes to the buffer RAM. When DRWB = 1, then the disk controller or local microcontroller reads from the buffer RAM. When the microcontroller accesses the buffer RAM, then this bit should be written before the ADBP bit is set.

3.7.7.7 Bit 1 Burst DMA Enable

When BDEN = 1 and HDMA = 1 in the auxilliary buffer control register, then burst DMA transfers are enabled on the host interface.

3.7.7.8 Bit 0 Arm Disk Buffer Pointer

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then the disk buffer pointer is transferred to the internal disk buffer counter when the drive controller sets the BDRQ interrupt. This bit also enables the disk controller to continue to the next sector. This bit is reset by the WD42C22C after the pointer registers have been transferred. When the disk controller port is used by the local microcontroller to access the buffer RAM, then setting this bit resets the disk FIFO pointers and the next byte read or written by the microcontroller will be at the new address loaded into the disk buffer pointer.

3.7.8 Buffer Status Register (AD7 Thru AD0 = 37, Read)

This register reflects the status of the buffer manager logic.

Bit			
7	6	5	4
AT/XT	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.8.1 Bit 7 AT / XT Interface Mode

This status bit reflects the state of the AT/XT control bit defined above.

3.7.8.2 Bit 6 Read Configuration

This bit reflects the state of the read configuration control bit defined in the buffer manager control register.

3.7.8.3 Bit 5 Reset Transfer Counter

This bit reflects the state of the RXC control bit defined in the buffer control register.

3.7.8.4 BIT 4 Host Buffer Pointer Armed

This bit reflects the state of the AHBP control bit defined in the buffer control register.

3.7.8.5 Bit 3 Host Read / Write

This bit reflects the state of the HRWB control bit defined in the buffer control register.

3.7.8.6 Bit 2 Disk Read / Write

This bit reflects the state of the DRWB control bit defined in the buffer control register.

3.7.8.7 Bit 1 Burst DMA Enable

This bit reflects the state of the BDEN control bit defined in the buffer control register.

3.7.8.8 Bit 0 Disk Buffer Pointer Armed

This bit reflects the state of the ADBP control bit defined in the buffer control register.

3.7.9 AUxilliary Buffer Control Register (AD7 Thru AD0 = 2F, Write)

This register is used for additional control of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	X	H16/$\overline{8}$	SCKS

3.7.9.1 Bit 7 Host DMA

This bit controls the host data transfers to/from the buffer RAM. If HDMA = 1, then the data is transferred to the host via DMA regardless of the host interface selected. If HDMA = 0, the default, then data is transferred via programmed I/O.

3.7.9.2 Bit 6 Host Slave / $\overline{\text{Master}}$

When HSMB = 0, the default, then the host is a master which drives the WD42C22C in either XT or AT type interface. When HSMB = 1, then the host is a slave device which is controlled by the local microcontroller. The slave device can be addressed in either ALE or indirect mode. The SBIC is an example of a device which can be connected to the WD42C22C. The ALE mode supports up to 32 registers in the slave device. Data transfers occur via WD-BUS mode if HDMA = 1 and is an 8-bit transfer if H16/8 = 0 and a 16-bit transfer if H16/8 = 1. This bit resets upon power-up but not affected by RESET.

3.7.9.3 Bit 5 Burst Continuous

This bit, along with the HDMA bit, and the BDEN bit in the buffer control register control the bursting of data during DMA transfers. If BCNT = 1, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data continuously as long as the FIFOs can keep up. If BCNT = 0, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data in 8-byte or 16-byte maximum length bursts, for 8 and 16 bit host data bus width, respectively.

3.7.9.4 Bit 4 Intelligent Drive Decode

When IDD = 1, then the controller is assumed to be on an intelligent drive. The HD0-15, INTRQ, and DREQ/IOCS16 outputs are always tri-stated if the drive is not selected. If IDD = 0, the default, then the outputs are controlled normally. This bit resets upon power up but not affected by RESET.

3.7.9.5 Bit 3 Drive Select

This bit is used when IDD = 1 to control drive selection. If AT/$\overline{\text{XT}}$ =1, then the drive is considered selected when SDH register bit 4 equals DSEL. If AT/$\overline{\text{XT}}$ = 0, then the drive is considered selected if DSEL = 1 and not selected if DSEL = 0. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.6 Bit 1 Host 16 / $\overline{8}$ Bit

This bit controls the width of the data transfers on the host side. If H16/8 = 0, then the host data transfers are 8-bit. If H16/8 = 1, the host data transfers are 16-bit. This bit resets upon power up but not affected by RESET.

3.7.9.7 Bit 0 Synchronous Clock Switch

This bit is used to control the clocking of the drive controller so that ESDI drives can be changed or data rates can be changed without the need for external clock deglitching. When SCKS =1, the default, then the WD42C22C synchronously switches the drive controller to the internal buffer clock (BCLK). When SCKS = 0, the WD42C22C switches the drive controller back to WCLK. The switch occurs only if both clocks are present. The CKSRC status bit defined below indicates whether or not the switch occured. When RESET

is asserted, the buffer clock clocks the drive controller during the reset and SCKS is set. The microcontroller must switch the clock source to the WCLK input prior to issuing any commands to the drive controller.

3.7.10 Auxilliary Buffer Status Register (AD7 Thru AD0 = 2F, READ)

This register gives additional status of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	CKSC	H16/$\overline{8}$	SCKS

3.7.10.1 Bit 7 Host DMA

This bit reflects the state of the HDMA control bit defined in the auxilliary buffer control register.

3.7.10.2 Bit 6 Host Slave / $\overline{\text{Master}}$

This bit reflects the state of the HSMB control bit defined in the auxilliary buffer control register.

3.7.10.3 Bit 5 Burst Continuous

This bit reflects the state of the BCNT control bit defined in the auxilliary buffer control register.

3.7.10.4 Bit 4 Intelligent Drive Decode

This bit reflects the state of the IDD control bit defined in the auxilliary buffer control register.

3.7.10.5 Bit 3 Drive Select

This bit reflects the state of the DSEL control bit defined in the auxilliary buffer control register.

3.7.10.6 Bit 2 Clock Source

This bit indicates the source of the drive controller clock. If CKSRC = 1 and SCKS = 1, then the drive controller is being clocked by the buffer clock (BCLK). If CKSRC = 0 and SCKS = 0, then the drive controller is clocked by WCLK. If CKSRC = 1 and SCKS = 0 or CKSRC = 0 and SCKS = 1, then the clock source is undefined. CKSRC should not be checked until at least 10 clock periods after the SCKS has been written. The slower of BCLK and WCLK should be used in determining this delay.

3.7.10.7 Bit 1 Host 16 / $\overline{8}$

This bit reflects the state of the H16/$\overline{8}$ control bit defined in the auxilliary buffer control register.

3.7.10.8 Bit 0 Synchronous Clock Switch

This bit reflects the state of the SCKS control bit defined in the auxilliary buffer control register.

3.7.11 Interface Status Register (AD7 THRU AD0 = 38, READ)

This register is used to indicate the status of the WD42C22C. The bits are defined as follows:

Bit			
7	6	5	4
MINT	DCGI	RSTI	FEI
3	2	1	0
DCI	HPRI	DRQI	CWSI

3.7.11.1 Bit 7 Microcontroller interrupt

This bit is high if the $\overline{\text{MCINT}}$ output pin is asserted. MCINT is the logical OR of seven sources:

- 1. A host SDH register write
- 2. A host soft reset
- 3. A FIFO error
- 4. The disk controller interrupt signal
- 5. The host transfer count interrupt flip-flop
- 6. The disk controller BDRQ signal
- 7. The command write/select interrupt flip-flop.

If any of the bits 6 through 0 are set, then the MCINT bit is high.

3.7.11.2 Bit 6 Drive Change Interrupt

This bit sets when the host writes a new value to the SDH register bit 4 when AT mode is selected.

3.7.11.3 Bit 5 Soft Reset Interrupt

This bit sets if the host initiates a soft reset. This bit resets by writing the proper bit in the interface control register.

3.7.11.4 Bit 4 FIFO Error Interrupt

This bit sets if a FIFO overrun or underrun condition occurs during host or disk transfers. It resets by writing the proper bit in the interface control register.

3.7.11.5 Bit 3 Disk Controller interrupt

This bit reflects the state of the disk controller interrupt signal. This interrupt occurs at the end of a command. This bit resets either when the disk controller status (port 27_{16}) is read or when the disk controller command (port 27_{16}) register is written.

3.7.11.6 Bit 2 Host Pointer Ready interrupt

This bit reflects the state of the host transfer count interrupt flip-flop. This interrupt sets when the host transfer counter reaches zero and the FIFO is empty if the host pointer is not armed. It is also set when the host pointer pipeline register is loaded into the host pointer counter. It resets by writing the proper bit in the interface control register.

3.7.11.7 Bit 1 Disk BDRQ Interrupt

This bit reflects the state of the disk controller BDRQ signal. It sets when the disk controller starts a transfer between the disk controller and the sector buffer. It resets by writing the proper bit in the interface control register. If ADBP = 0 (bit 0 in the buffer control register, 37_{16}) when this bit first goes from 0 to 1, then DRQI and MCINT is not reset until after the microcontroller writes ADBP = 1.

3.7.11.8 Bit 0 Command Write / Select / Slave Interrupt

This bit informs the local microcontroller that a command has been written if the WD42C22C is in AT mode, that the WD42C22C has been

selected if it is in XT mode, or that the slave host device has issued an interrupt if in slave host mode. (Asserts INTRQ. A slave interrupt only triggers on rising edge of INTRQ.) This bit resets by writing the proper bit in the interface control register.

3.7.12 Interface Control Register (AD7 Thru AD0 = 38, Write)

This register is used to control various parts of the WD42C22C. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
SIRQ	RDCI	RSRI	RFEI
3	**2**	**1**	**0**
RBSY	RHRI	RDQI	RCWS

3.7.12.1 Bit 7 Set Interrupt

Writing a 1 to this bit generates a host interrupt if interrupts are enabled.

3.7.12.2 Bit 6 Reset Drive Change Interrupt

Writing a 1 to this bit resets the host SDH write interrupt flip-flop.

3.7.12.3 Bit 5 Reset Soft Reset interrupT

Writing a 1 to this bit resets the soft reset interrupt flip-flop. In AT mode, the microcontroller must wait for the RST bit (2) in the FDR register ($3F_{16}$) to be

reset by the host before this interrupt can be reset.

3.7.12.4 Bit 4 Reset FIFO Error interrupt

Writing a 1 to this bit resets the FIFO error interrupt flip-flop.

3.7.12.5 Bit 3 Reset Busy

Writing a 1 to this bit resets the BSY status bit in the hardware status register if XT mode is selected or it resets the ABSY status bit in the host status register if AT mode is selected. In AT mode, this bit should only be set at the very end of a command after the last DRQ is asserted to the host. Internal logic handles ABSY during buffer transfers to the host.

3.7.12.6 Bit 2 Reset Host Pointer Ready Interrupt

Writing a 1 to this bit resets the host pointer ready interrupt flip-flop.

3.7.12.7 Bit 1 Reset Disk BDRQ Interrupt

Writing a 1 to this bit resets the disk BDRQ interrupt flip-flop.

3.7.12.8 Bit 0 Reset Command Write / Select / Slave Interrupt

Writing a 1 to this bit resets the command write/select/slave interrupt flip-flop.

3.7.13 Configuration Status Registers (Low: AD7 Thru AD0 = 39, Read High: AD7 Thru AD0 = 3A, Read)

The configuration status registers are used to read the configuration jumpers on buffer address pins. When in read configuration mode, the buffer address lines have 300 µA current source pulldowns enabled. If there is no external pullup resistor on the buffer address line, then the state of the line is read as a 0. If a 13K external pullup resistor is connected to a buffer address line, then the state of the line is read as a 1. The configuration registers should not be read until 100 µsec after enabling read configuration mode, to allow the buffer address line voltages to reach their proper value. Register contents are undefined if not in read configuration mode.

Configuration status low

Bit							
7	6	5	4	3	2	1	0
BA7 THRU BA0							

Configuration status high

Bit							
7	6	5	4	3	2	1	0
0	BA14 THRU BA8						

3.7.14 Drive Interface Status (AD7 Thru AD0 = 3B, Read)

This register gives status information for the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	DRDY	WF	HDS	MAC	DRO	IPOL	DSN

3.7.14.1 Bit 7 Reset Drive Controller

This bit reflects the state of the reset drive controller control bit defined in the drive interface control register.

3.7.14.2 Bit 6 Drive Ready

This bit is set if the $\overline{\text{DRDY}}$ input is asserted by the drive. It can always be read by the local microcontroller regardless of the state of disk controller busy.

3.7.14.3 Bit 5 Write Fault

This bit is set if the $\overline{\text{WF}}$ input is asserted by the drive. It is always valid.

3.7.14.4 Bit 4 Host Drive Select

This bit reflects the state of bit 4 of register 46_{16}, the host copy of the SDH register. It is used by the host in AT mode as a drive select. If HDS = 0, then drive 1 is selected. If HDS = 1, then drive 2 is selected. This bit is always accessable to the microcontroller regardless of the state of ABSY.

3.7.14.5 Bit 3 Microcontroller Access Control

This bit reflects the state of the microcontroller access control bit defined in the drive interface control register.

3.7.14.6 Bit 2 Disable Reset Output

This bit reflects the state of the disable reset output control bit defined in the drive interface control register.

3.7.14.7 Bit 1 Input Polarity

This bit reflects the state of the input polarity control bit defined in the drive interface control register.

3.7.14.8 Bit 0 Disable Sector Number

This bit reflects the state of the disable sector number control bit defined in the drive interface control register.

3.7.15 Drive Interface Control (AD7 Thru AD0 = 3B, Write)

This register is used to control the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	X	X	X	MAC	DRQ	IPOL	DSN

3.7.15.1 Bit 7 Reset Drive Controller

When this bit is asserted, then the drive controller subsection of the WD42C22C resets. It is held reset as long as the bit is asserted. This bit is reset when RESET is asserted.

3.7.15.2 Bit 3 Microcontroller Access Control

When this bit is set, the microcontroller is tied to the buffer RAM through the disk controller's port. The microcontroller can then read or write the buffer by reading from or writing to the RAM access port (36_{16}). The DRWB bit in the buffer manager control port should be set to the proper state before this bit is set. When MAC = 1, then the disk controller task file (registers 21_{16} through 27_{16}) cannot be accessed by the microcontroller. If the microcontroller writes to these registers when MAC = 1, then the disk controller may not act properly. This bit resets when RESET is asserted. The proper sequence for the microcontroller to read/write the RAM is defined under the buffer manager description.

3.7.15.3 Bit 2 Disable Reset Output

When this bit is set, all host initiated soft resets are disabled. Instead of the RESET line being asserted on soft reset, only the MCINT line is asserted. It is the responsibility of the local microcontroller to properly reset the board hardware when this bit is set. This bit resets only during power-up.

3.7.15.4 Bit 1 Input Polarity

This bit is used to control the polarity of the INDEX, SCT, WF, and DRDY inputs. If IPOL= 0, the default, then the inputs are active low. If IPOL = 1, then the inputs are active high. In soft sector MFM and RLL modes, DRUN is always active high regardless of the state of IPOL.

3.7.15.5 Bit 0 Disable Sector Number

When this bit is set, then the drive controller does not compare the sector number coming from the drive with the desired sector number when reads or writes are performed. The drive controller instead writes the sector number coming from the drive into the sector number register in the drive controller task file. At the end of each sector, just prior to issuing DRQI or DCI, the drive controller always writes the sector number to the alternate sector number register. This bit resets when RESET is asserted.

3.7.16 Alternate Sector Number (AD7 Thru AD0 = 3C, Read)

When the disk controller interrupts the microcontroller, this register holds the sector number of the sector just read or written. It is always updated just prior to the disk BDRQ interrupt (DRQI) or the disk controller interrupt (DCI). It is initialized to FF_{16} at the start of every command. It is written regardless of the state of the DSN bit described above.

Bit							
7	6	5	4	3	2	1	0
NUMBER OF LAST SECTOR READ OR WRITTEN							

3.8 AT Interface Ports

3.8.1 AT Control Register (AD7 Thru AD0 = 2A, Read/Write)

This register controls the new auto-DRQ option for write, write long, and format commands.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADQ7	ADRQ

3.8.1.1 Bits 7 Through 2 Reserved

Set to 0.

3.8.1.2 Bit 1 Auto-DRQ 7 Byte ECC

When ADRQ = 1 and ADQ = 1, then 7 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 1 and ADQ7 = 0, then 4 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 0, then the ECC7 bit in the fixed disk register ($3F_{16}$) controls the number of ECC bytes transferred on read long and write long commands.

3.8.1.3 Bit 0 Auto-DRQ Enable

When ADRQ = 1 in AT mode, then the WD42C22C automatically sets up the first data transfer from the host for write, write long, and format commands. When ADRQ = 0, the local microcontroller must set up all data transfers to/from the host for all commands.

3.8.2 Drive Zero Status (AD7 Thru AD0 = 3D, Read/Write)

In PC/AT mode, bits 6, 5, 4, 2, and 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register are set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 0. The other bits of the host status are not affected by this register.

3.8.3 Drive One Status (AD7 Thru AD0 = 3E, Read/Write)

In AT mode, bits 6, 5, 4, 2, and bit 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register is set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 1. The other bits of the host status are not affected by this register.

3.8.4 Fixed Disk Register (AD7 Thru AD0 = 3F, Read)

This register contains the fixed disk register data written by the host.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.8.5 Digital Input Register (AD7 Thru AD0 = 3F, Write)

Bit 5 of this register is written by the local microcontroller and read by the host if the fixed disk register bit 3 is zero. This bit is inverted when this register is read by the host. If HS3EN is one, then bit 5 of this register comes from SDH register bit 3.

Bit							
7	6	5	4	3	2	1	0
ECCM	ECC7/ DDRQ	RWC	X	X	X	DS1	DS0

3.8.5.1 Bit 7 ECC Mode

In PC/AT mode, ECCMOD = 1 indicates that the data transferred to the host includes ECC. The ECC is transferred in bytes rather than in words. This bit is reset when RESET is asserted. This bit should not be set in XT or slave host modes.

3.8.5.2 Bit 6 ECC 7 Bytes/ Disable BDRQ

When ECCM = 1, then this bit determines the number of ECC bytes transferred to the host. If ECC7 = 1, then 7 bytes are transferred. Otherwise, 4 bytes are transferred. If ECCM = 0, then this bit controls whether or not the drive controller issues BDRQ interrupts. If DDRQ = 0, then the drive controller issues BDRQ interrupts. If DDRQ = 1, then the drive controller does not issue BDRQ interrupts. It should be noted that when BDRQ occurs, the buffer manager loads the disk pointer from its pipeline register and when no BDRQ occurs then the disk pointer keeps incrementing from one sector to the next. This bit resets when RESET is asserted.

3.8.5.3 Bit 5 Reduce Write Current

This bit is set by the microcontroller and indicates the state of the RWC signal going to the drive.

3.8.5.4 Bit 1 Drive Select 1

This bit controls the state of the $\overline{DS1}$ output pin. When DS1 = 0, then the $\overline{DS1}$ output is tri-stated and when DS1 = 1 the $\overline{DS1}$ output is low. This bit is reset when RESET is asserted.

3.8.5.5 Bit 0 Drive Select 0

This bit controls the state of the $\overline{DS0}$ output pin. When DS0 = 0, then the $\overline{DS0}$ output is tri-stated and when DS0 = 1 the the $\overline{DS0}$ output is low. This bit is reset when RESET is asserted.

3.8.6 AT Task File Copy (AD7 Thru AD0 = 40 Thru 47, Read/Write)

These registers are a copy of the disk controller task file. They are loaded by the host prior to the start of a command. The local microcontroller must read the command and interpret it and then copy the appropriate parameters from this task file copy to the actual drive controller task file (20_{16}-27_{16}). At the end of the command, the local microcontroller must update this task file copy before asserting INTRQ and resetting ABSY. The local microcontroller can only access these registers when ABSY=1.

4.0 BUFFER MANAGER ORGANIZATION

The buffer manager can control multiple sector buffers totalling up to 32 Kbytes. The buffer interface requires static RAMs. The sector buffers can be any size up to 2055 bytes, including ECC, and can be located at any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM simultaneously. The buffer manager handles the arbitration between the host interface and the drive controller. There is a FIFO in the host data interface that allows a sustained bandwidth of 4 Mwords/sec (8 Mbytes/sec) for 16-bit wide transfers and 8 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 10 Mbytes/sec.

When the local microcontroller wants to access the buffer RAM, it has to use the disk buffer manager logic. It first loads the desired starting address into the disk buffer pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (register 36_{16}), the data is read/written through the disk controller's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction as set by the DRWB control bit in the buffer control register.

Both address counters are pipelined. There are registers that can be loaded with the starting address of the next sector buffer while the current buffer is transferring. This allows noncontiguous buffers to be chained without any loss of RAM bandwidth between sectors.

4.1 ACCESSING BUFFER RAM FROM THE MICRO-CONTROLLER

The microcontroller can read and write the buffer RAM. To read the buffer RAM the procedure is:

1. Set DRWB = 1 (bit 2) in the buffer manager control Register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

The buffer manager begins reading data out of the RAM starting at the address specified in the disk pointer register and placing it into the FIFO. As the microcontroller reads from the RAM access port (36_{16}), sequential bytes from the buffer are transferred from the FIFO to the microcontroller.

The procedure to write to the buffer RAM is:

1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

As the microcontroller writes data to the RAM access port (36_{16}), the buffer manager transfers the bytes to sequential locations in the buffer RAM starting at the address specified in the disk pointer register.

NOTE

DRWB should not be changed while MAC = 1.

4.2 STARTING HOST TRANSFERS TO/FROM BUFFER RAM

Host transfers can be performed in several modes. The modes available and the setup required to establish each mode are as follows:

HDMA	BDEN	BCNT	H16/8-
1	0	X	0
8-bit wide single byte DMA			
1	0	X	1
16-bit wide single word DMA			
1	1	0	0
8-bit wide, 8-byte burst DMA			
1	1	0	1
16-bit wide, 16-byte burst DMA			
1	1	1	0
8-bit wide, continuous burst DMA			
1	1	1	1
16-bit wide, continuous burst DMA			
0	X	X	0
8-bit wide PIO			
0	X	X	1
16-bit wide PIO			

Bits HDMA (bit 7), BCNT(bit 5), and H16/$\overline{8}$ (bit 1) are in the auxilliary buffer manager control register ($2F_{16}$) and bit BDEN (bit 1) is in the buffer manager control register (37_{16}). All of these modes are available in both the XT and AT host configurations. All of the DMA modes are available in the slave host configuration.

To perform a Host read data transfer the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 1 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16}).
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and sets REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.
6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.
7. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is be asserted.
8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors, then go to 3.
9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

To perform a host write data transfer, the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 0 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16})
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and set REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.
6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.

7. Wait for second HPRI = 1 (bit 2) in the interface status register (38_{16}). MCINT is asserted.

8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors then go to 3.

9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

4.3 CONTROLLER COMMANDS

The WD42C22C Winchester command set contains twelve commands. Four commands (read sector, write sector, format, and set parameter) are directly executed through the command register. The remaining commands are not directly available to the host. These commands may be executed by the local microcontroller transparently to the host. Table 12 lists the commands and command codes.

COMMAND	7	6	5	4	3	2	1	0
Read Sector	0	0	1	0	0	M	L	T
Read Next Data	0	1	1	0	0	0	L	1
Write Sector	0	0	1	1	X	M	L	T
Write ID	1	0	1	1	F	0	A	T
Scan ID	0	1	0	0	0	0	0	T
Format Track	0	1	0	1	0	0	W	1
Format Single Sector	1	1	0	1	0	0	W	1
Compute Correction	0	0	0	0	1	P	0	0
Set Parameter	Z	0	0	R	0	E	H	S
Load Parameter Block	1	0	0	0	1	D	K	U
Sleep	1	0	0	1	1	0	0	0
Dump	1	0	1	0	I	B	L	1

Mnemonic definitions for Table 12:

TABLE 12. COMMAND AND COMMAND CODES

- M=0 Single sector read or write. Sector count is ignored.
- M=1 Multiple sector read or write. Used for 1:1 interleave.
- L=0 Normal mode, selected ECC or CRC functions performed.
- L=1 Sector extended by 4 or 7 bytes (depends on set parameter command. No ECC generated or checked.
- T=0 Enable retries.
- T=1 Disable retries.
- X=0 Write sector specified in sector number register.
- X=1 Write sector specified in first byte of the sector buffer.
- F=0 Write new ID immediately after current ID.
- F=1 Write new ID offset from current ID.
- A=0 Do not pulse AME when writing new ID.
- A=1 Pulse AME when writing new ID.
- W=0 Write gate stays asserted for entire track or sector.
- W=1 Write gate deasserted over all gaps during format.
- P=0 Transfer syndrome bytes to buffer and calculate error pattern bytes and transfer them to the buffer.
- P=1 Transfer syndrome bytes to the buffer but do not calculate error pattern bytes.
- Z=0 MFM or RLL mode.
- Z=1 NRZ mode. Mode used for ESDI drive interface.
- R=0 Disable relocation ID searches.
- R=1 Enable relocation ID searches.
- E=0 Sector extension for read long/write long 4 bytes. ECC generator/checker is 4 bytes.
- E=1 Sector extension for read long/write long 7 bytes. ECC generator/checker is 7 bytes.
- H=0 SDH register programmed for 3 head select bits.
- H=1 SDH register programmed for 4 head select bits.
- S=0 Error correction span 5 bits with 4 byte ECC or 11 bits with 7 byte ECC.
- S=1 Error correction span 11 bits with 4 byte ECC or 22 bits with 7 byte ECC.
- D=0 Select soft sector drive interface. Default after master reset.
- D=1 Select hard sector drive interface. In this mode, DRUN becomes a sector pulse input.

MODE	MODE CONTROL			OPTIONS														
	Z	D	K	M	T	L	X	A	F	R	S	E	H	P	U	W	I	B
RLL soft sector	?	0	0	x	x	x	x	x	x	x	x	*	x	x	x			
RLL hard sector	?	1	0	x	x	x	x	x	x	x	x	*	x	x	x	x	x	x
MFM soft sector	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
MFM hard sector	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRZ soft sector	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
NRZ hard sector	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

? Don't care, could be 0 or 1.
x These options are supported.
* These options have no effect.

TABLE 13. OPTION SUMMARY TABLE

- K=0 RLL data interface. Selection of this option disables the NRZ option. Defaults to this setting after master reset.
  K=1 Data interface is either MFM or NRZ.
- U=0 Use the standard sector sizes defined under the SDH register description.
  U=1 Select user defined sector size. The desired sector size is put into the cylinder registers prior to issuing a load parameter block command. The auxilliary set parameter command transfers the desired sector size from the cylinder registers to an internal sector size register.
- I=0 Dump two fields per sector. Dump 5 ID bytes and the number of data bytes set by the sector size.
  i=1 Dump only one field per sector. The sizeof the field is set by the sector size and type of field (ID versus data) is controlled by where RG is asserted.
- B=0 FE sync byte and zero preset CRC.
  B=1 A1 sync byte and ones preset CRC.

Table 13 summarizes the data formats and options supported by these formats.

4.4 COMMAND DESCRIPTIONS

4.4.1 Read Sector

If M = 0, then the sector specified in sector number register is read. If M = 1, then multiple records are read. If the sector count register = 0, then 256 sectors are read at the desired track.

If T=0, then ID searches are retried for 10 index pulses. DAM not found errors are not retried. There are no retries for CRC/ECC errors. If T=1, ID searches are retried for two index pulses.

If L=0, then normal CRC or ECC read commands are performed. If L=1, then the CRC or ECC check bytes are not computed but instead the CRC or ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 4 or 7 bytes. If ECC and retry modes have been selected and a data field error occurs there are no attempts to correct the data.

A bad block mark in the ID field sets the error bit and the data field is not read. If the R option in the set parameter command is set then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately

even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector umber where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of Cylinder where sector has been relocated
26	Head number of relocated sector

If DSN = 1 (bit 0) in the drive interface control register ($3B_{16}$) than the sector number is not compared when ID searches are performed. The WD42C22A reads the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be read into the buffer in one revolution.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue read command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number, and sector size code.
  10. When the proper sector ID is found, read sector data and place in buffer.
  11. Write sector number to alternate sector number register. If M = 0, then go to 10.
  12. Decrement sector count, increment sector number. If M = 1, and sector count = 0 then go to 13 else go to step 8.
  13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if ID field not found or if ID field matches, but CRC check fails, and after retry procedure.
- Bad block set if attempt was made to read a sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.
- Data CRC/ECC set if data field CRC or ECC check fails. No attempt is made to correct ECC errors.
- Data AM not found in set if data address mark not found.

4.4.2 Read Next Data

The read next data command finds the next data field and places it in a buffer. If the WD42C22C detects that the drive number changed since the last read command, then an auto-scan ID is performed and step pulses are issued to update the present cylinder position.

All searches for a data field are retried for two index pulses, but if a data ECC error is detected there are no retries. If after reading the correct ID field, the data address mark is not found a DAM error is set.

The L flag controls the ECC check bytes. If L=0, then the data field is read and ECC is checked. If L=1, then the ECC check bytes are not computed. Instead, the ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 7 bytes.

NOTE

This command supports only soft sector MFM and RLL mode and is implemented for backward compatibility with the WD5011 and WD5011A.

Command Flow :

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  4. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  5. Set MAC=0 in the drive interface control register.
  6. Issue read next data command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Set DRQ status bit, activate BDRQ signal to buffer manager. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Find next data field, read sector data and place in buffer. If data mark error, try data field search again until 2 index pulses occur.
  10. Copy sector number register to alternate sector number register ($3C_{16}$). Set DCI (bit 3) in the interface status register (38_{16}). MCINT is asserted.
- MICRO:
  11. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- Data CRC/ECC set if data field CRC or ECC check fails. No correction is attempted.
- Data AM not found is set if data address mark not found after 2 index pulses of looking for any data field.

4.4.3 Write Sector

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write total number of sectors specified by sector count register if M = 1. Sectors are written in numerical order. If M = 0, then sector count is ignored and only one sector is written. The data field PLO sync field is nominally 12 bytes long but is extended by the PLO register.

If T = 0, then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If L = 0, then normal CRC or ECC write sector commands are performed. If L = 1, then the CRC or ECC check bytes are not computed and written to the disk but instead, 4 or 7 additional bytes are

read from the buffer and written to the disk immediately after the data field.

If X = 0, then the controller searches for the sector number in the sector number register and increments the sector number register and the end of each sector if M = 1. If X = 1, then the controller searches for the sector specified in the first byte of the sector buffer. The controller reloads the sector number register from the first byte of each subsequent sector buffer if M = 1. This allows a track formatted with interleave to be written in one revolution.

A bad block mark in the ID field sets the error bit and the data field is not be written. If the R option in the set parameter command is set, then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector number where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of cylinder where sector has been relocated
26	Head number where sector has been relocated

If DSN = 1(bit 0) in the drive interface control register ($3B_{16}$) then the sector number is not compared when ID searches are performed. The WD42C22C writes the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be written into the buffer in one revolution. This option is only useful when doing the initial write-after-format to place 00 in the data fields.

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue write command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQ is enabled.) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number and sector size code.
  10. When the proper sector ID is found, write buffer data to sector.
  11. Write sector number to alternate sector number register ($3C_{16}$). If M = 0 then go to 13.
  12. Decrement sector count, increment sector number. If M = 1 and sector count = 0 then go to 13 else go to step 8.
  13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

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- MICRO: 14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if write sector attempted on any sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.

4.4.4 Write ID

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write 4 bytes to create an ID field. The PLO sync field prior to this new ID field is nominally 12 bytes long but is extended by the PLO register. A value of 0 results in a 2048 byte PLO field and should not be used.

If T = 0 then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If F = 0, then the new ID is written immediately after the ID field of the desired sector. If F = 1, then the new ID field is written offset from the desired sector ID with the offset determined by the internal sector size register. A load parameter block command will have to be issued to set the offset value and another load parameter block will be needed to set the sector size back to the correct value if the programmable sector size option is being used. An offset of up to 2048 is allowed. This option can be used to reformat a single sector in soft sector mode.

If A = 0, then the AME output is held low during the write ID command. If A = 1, then the AME output is pulsed at the start of the PLO field before the new ID being written. This option, together with the F option, can be used to reformat a single sector in soft sector NRZ mode.

The four bytes in the buffer (F = 0) should be as follows:

BYTE 0: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 1: Low byte of cylinder number

BYTE 2: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 3: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

The five bytes in the buffer (F = 1) should be as follows:

BYTE 0: Sector Number

BYTE 1: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 2: Low byte of cylinder number

BYTE 3: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 4: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

RF should be set to 1 if the new ID being written is to be a special relocation ID for mapping a defective sector to a new position.

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the ID buffer data into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.

4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC = 0 in the drive interface control register.
6. Issue Write ID command to WD42C22C.

- WD42C22C: 7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.

- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).

- WD42C22C: 9. Search for head, cylinder, sector number and sector size code.
10. When the proper sector ID is found, write buffer data to sector.

- WD42C22C:11. Write sector number to alternate sector number register. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

- MICRO: 12. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write Fault and aborted command set if WF pin activated.
- ID not Found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if bad block bit detected in ID of desired sector.

4.4.5 Scan ID

When the next ID field of the present track is encountered, cylinder number, sector size, head number and sector number are loaded into the respective registers.

Command Flow:

- MICRO: 1. Issue Scan ID command to WD42C22C.

- WD42C22C 2. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
3. Search for next ID field and read 4 ID bytes into respective registers. Search for ID field for up to 10 index pulses if T=0, up to 2 index pulses if T=1.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

- MICRO: 5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin active.
- Bad Block set if bad block mark detected.
- ID not found if no ID fields are found.
- Relocation ID found if R option enabled and relocation ID detected.

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4.4.6 Format Track

This command formats one track using parameters loaded in the task registers file and in buffer memory.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector numbers are taken from buffer memory. The total number of sectors formatted is specified by the sector count register. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register if B = 1. The data PLO field length is 12 bytes during format.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads

comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector addresses have been loaded into the buffer then the command register is loaded with the format command. When the BRDY signal is activated by the buffer manager, the specified number of sectors are written. The block marks and sector numbers are read from the buffer as needed. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

Write Gate is turned on and off within 4 bit times after index if NRZ or hard sector mode is selected or within 6 bit times otherwise. In RLL mode, Gap1/Gap3 data should be programmed to be 33_{16} with the load parameter command. The W option controls the state of WRITE GATE over the gaps. If W=1, WRITE GATE turns off over the gaps.

The sum of the number of bytes in both the Gap1/Gap3 and ID PLO field must be greater than or equal to 25 bytes to achieve 1:1 interleave.

The interleave table contains the bad block marks and sector numbers for the track. If there is a bad sector and it is desired for the controller to just skip over it, then the bad block mark for that sector position should be set to 80_{16} and the sector number for that sector should be set to FF_{16}. If it is desired to map the bad sector then the bad block mark for that sector should be set to 80_{16} and the sector number for that sector should be set to the correct value for that position in the interleave table. The R and U options should be set in the set parameter and load parameter block commands. A write ID command then places the relocation information for that sector onto the drive.

The interleave table format is:

- BYTE 0: 1st sector's block mark (00_{16} or 80_{16})
- BYTE 1: 1st sector's sector number
- BYTE 2: 2nd sector's block mark (00_{16} or 80_{16})
- BYTE 3: 2nd sector's sector number

  .
  .
  .

- BYTE 2n: nth sector's block mark (00_{16} or 80_{16})
- BYTE 2n+1: nth sector's sector number

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16})
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the buffer control register.
  6. Issue format command to WD42C22C.

- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.

- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).

- WD42C22C:
  9. Write gap.
  10. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.

11. Decrement sector count register. If sector count = 0, then go to step 12, else go to step 9.
12. Write Gap until leading edge of index pulse.
13. De-assert Write Gate.
14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO:
15. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

Note

Gap length written on disk is 3 bytes longer than gap value specified in sector number register.

4.4.7 Format Single Sector

This command formats one sector using parameters loaded in the task register file and in buffer memory. This command only applicable to hard sector mode.

WRITE GATE is turned on and off within 4 bit times after index or sector if NRZ mode is selected or within 6 bit times otherwise. The W option controls the state of WRITE GATE over the gaps. Setting W to 1 turns off WRITE GATE over the gaps.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector number are taken from buffer memory. The physical sector position to be formatted is specified by the sector count register. If sector count = 1, then the first sector after index is formatted. For sector count = 2, the second sector after index is formatted, and so on. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector number loaded into the buffer, then the command register is loaded with the format single sector command. When the BRDY pin is activated by the buffer manager, the controller then looks for the start of the desired sector. The bad block mark and sector number are read from the buffer. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

The data for the buffer is:
- BYTE 0: bad block mark (00_{16} or 80_{16})
- BYTE 1: sector number of formatted sector.

Command Flow:

• MICRO:
1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC=0 in the drive interface control register.
6. Issue format single sector command to WD42C22C.

• WD42C22C:
7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.

- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C: 9. Decrement sector count. If sector count = 0 go to 11, else go to 10.
  10. Wait for SECTOR pulse, then go to 9.
  11. Assert WRITE GATE. Write gap.
- WD42C22C:12. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.
  13. Write gap until leading edge of SECTOR pulse.
  14. De-assert Write Gate.
  15. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 16. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

4.4.8 Compute Correction

This command is used to compute the pattern and location of a single burst error. It is used after a read sector command has detected a data field ECC error. The compute correction command first writes the four or seven syndrome bytes into the buffer. It then processes the syndrome bytes to compute the error pattern and error location. The error location and error pattern bytes are written into the buffer. Either four or seven error pattern bytes are written to the buffer depending on the ECC length selected. The error pattern bytes are automatically byte aligned.

The P option is used to control whether or not the error pattern bytes are calculated. If P = 0, then the error pattern bytes are calculated and sent to the buffer. If P = 1, then the error pattern bytes are not calculated. Only the syndrome byte is transferred to the buffer. This option facilitates firmware algorithms that require a matching syndrome before a correction is made. In this case, the firmware calculates the error pattern, corrects the error, and saves the syndrome after initially detecting the error. Then, the firmware dumps and compares the syndrome on the second read of the same sector. An ECC error can now be corrected in one revolution of the disk compared to three revolutions required by earlier WD1010 and WD2010 based controllers.

The error pattern and error location bytes are not valid if the error is found to be uncorrectable. An uncorrectable error is indicated by the appropriate bits in the status and error register.

The buffer contents contains the following information:

- SYNDROME BYTE (MSB)
- SYNDROME BYTE
- SYNDROME BYTE
- SYNDROME BYTE (LSB if 4 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (LSB if 7 byte ECC)
- BYTE OFFSET (MSB)
- BYTE OFFSET (LSB)
- ERROR PATTERN (MSB)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 4 byte ECC)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 7 byte ECC)

If the byte offset is 0, then the first data byte of the sector should be exclusive OR'ed with the first error pattern byte (MSB). Each succeeding data byte exclusive OR'ed with the succeeding error pattern byte until the fourth data byte is exclusive OR'ed with the fourth error pattern byte (LSB). Exclusive OR the first two error pattern bytes for 5 bit spans. Exclusive OR the first three error pattern bytes for 11 bit spans. Exclusive OR the first four error pattern bytes for the 22 bit span.

Command Flow:

- MICRO: 1. Set DRWB=0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the error correction data buffer into the disk buffer pointer

registers (34_{16} & 35_{16}).

3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC=0 in the drive interface control register.
6. Issue compute correction command to WD42C22C.

• WD42C22C: 7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.

8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.

• MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).

• WD42C22C: 9. Transfer contents of the four (or seven) byte ECC register to buffer, most significant byte first.

10. Clock the ECC register. Stop if correctable pattern found or if number of clocks exceeds sector size. If number of clocks exceeds sector size, set error bit of status register and ECC error of error register.
11. Transfer byte count to buffer (2 bytes). Transfer 4 bytes of error pattern to buffer if 4 byte ECC. Transfer 7 bytes of error pattern 7 byte ECC.
12. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO: 13. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

• CRC/ECC flag set if data field error length exceeds correction span.

NOTE

Default 11 bit correction span after master reset if 7-byte ECC or 5 bit correction span if 4-byte ECC.

4.4.9 Set Parameter

The E bit is used to select either 4 byte or 7 byte sector extension for read long and write long commands. It also selects either a 4 or 7 byte internally generated ECC. A 7 byte sector extension and 7 byte ECC are the default after a master reset (due to RLL default). If E is 0, then a 4 byte sector extension and 4 byte ECC are selected if MFM or NRZ mode. If E is 1, then a 7 byte sector extension and 7 byte ECC are selected.

The H bit selects either 3 or 4 head select bits in the SDH register. If H=0, then 3 head select bits are written or compared in the ID fields on the drive. If H=1, then 4 head select bits are written or compared in the ID fields on the drive. The default after master reset is 3 head select bits.

The S bit is used to select either a 5 bit or 11 bit correction span if 4 byte ECC and an 11 bit or 22 bit correction span if 7 byte ECC. An 11 bit correction span for 7 byte ECC is the default parameter following master reset. If S is 0, then a 5 bit correction span is selected if 4 byte ECC, 11 bit correction span if 7 byte ECC. If S is 1, then an 11 bit correction span is selected if 4 byte ECC, 22 bit correction span if 7 byte ECC.

The Z bit is used to select MFM, RLL, or NRZ mode. If K=0 in the load parameter block command, then RLL coding is selected regardless of the state of Z. If Z is 0 and K is 1, then MFM coding is selected. If Z is 1 and K = 1, then NRZ coding is selected.

The R option is used to enable relocation ID searches. If R=1 for read and write sector commands and a bad block mark is detected in the desired sector's ID, then the WD42C22C searches for a special ID field containing relocation information immediately after the desired sector's ID. This special ID field is placed using the write ID command. When the R option is used, then the U option must be set to 1 in the load parameter block command.

Command Flow:

- MICRO: 1. Issue set parameter command to WD42C22C.
- WD42C22A: 2. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
3. Set or reset internal parameter flip-flop.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.10 Load Parameter Block

The D bit is used to indicate the sectoring mode. If D = 0, the default after a master reset, then soft sector mode is selected. If D = 1, then hard sector mode is selected. In hard sector mode, the PLO length register is transferred to the internal GAP length register during the load parameter block command. This GAP register is used to control the delay from INDEX/SECTOR to READ GATE on.

The K bit selects the data interface mode. If K=0, the default after a reset, then RLL mode is selected. If K=1, then the interface is either MFM or NRZ as selected by the set parameter command.

The U bit selects the sector size options. If U=0, then the sector sizes are 128, 256, 512, and 1024 depending on the contents of the SDH register. If U=1, then the sector size is defined by the user. The cylinder registers are loaded with the desired sector size prior to issuing the load parameter block command.

In addition, the load parameter block command is used to load several internal parameters for format, read, and write commands. The task file is loaded with these parameters prior to the start of the command. The registers loaded and the corresponding parameters are:

REGISTER	PARAMETER
21	Delay from INDEX/SECTOR to RG
22	Data written in GAPS
23	Data written in PADS
24	LS byte of sector size, LS byte of offset for write ID command
25	3 MS bits of sector size, 3 MS bits of offset for write ID command

Command Flow:

- MICRO: 1. Load parameters into task file.
2. Issue load parameter block command to WD42C22C.
- WD42C22C: 3. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
4. Set or reset internal parameter flip-flop.
5. Copy cylinder registers to internal sector size register. Copy PLO register to internal GAP register. Copy sector count register to internal GAP data register. Copy sector number register to internal PAD data register.
6. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 7. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.11 Sleep

The sleep command places the WD42C22C in a low power standby mode. When the sleep command is issued, the disk controller section clocks are disabled and only the buffer manager and host interface logic is enabled. The disk controller can be brought out of the sleep mode by setting RDC = 1 (bit 7) in the disk controller control register ($3B_{16}$) or by resetting the entire WD42C22C. The microcontroller should **NEVER** attempt to read or write the drive controller task file (registers 21_{16} through 27_{16}) while the drive controller is in the sleep mode.

Command Flow:

- MICRO: 1. Issue sleep command to WD42C22C.
- WD42C22C: 2. Write FF to the alternate sector number register ($3C_{16}$).
  3. Disable drive controller clocks.
- MICRO: 4. Wake up disk controller by setting RDC=1 or by resetting the WD42C22C.

Error Flags:

- None.
-

4.4.12 Dump

The dump command sends data off the media regardless of matching ID fields and regardless of the format. The command can dump an ID field, a data field, or both. Dump retrieves all the ID fields from index to index to determine the interleave. Dump can also read the ESDI standard defect list. The command dumps data starting at the first byte after the A1 sync byte for WD format or the first byte after the FE sync byte for ESDI format. This command can only do multisector dumps in hard sector mode.

The command is assumed to be a multisector command. To read just one sector as in an ESDI defect list read, then the sector count must be set to one. There are three options.

The I option controls the number of fields that are dumped for each sector. If I = 0, then two fields (ID and data) are dumped for each sector. If I = 1, then only one field is dumped for each sector. The type of field is determined by the read gate delay and the sector size. The sector size should be programmed to 1 less than the number of bytes to be dumped for the sector.

The B option controls the sync byte and CRC preset. If B = 0, then the sync byte is assumed to FE and the CRC is preset to all zeroes. If B = 1, then the sync byte is assumed to be A1 and the CRC is preset to all ones.

The L option selects either CRC or no CRC checking. If L = 0, then CRC is checked. If L = 1, then either four or seven check bytes are transferred to the buffer depending on the extension selected by the set parameter command. If L = 1, then I should also be set to 1. B does not affect the L option.

The PLO register controls the read gate delay for the first sector. READ GATE turns on x + 5 + CL bytes after the index pulse. Read gate for subsequent sectors is controlled as in normal read and write commands.

Use the dump command to read an ESDI defect list as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 255 for 256 byte sector.
3. Issue A1 command.

Use the dump command to dump the track interleave for WD format as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 4.
3. Set sector count = number of sectors per track.
4. Issue AD command.

Use the dump command to dump all the data fields on a track for WD format as follows:

1. Set PLO register = read gate delay to start of data PLO - 5.
2. Set sector size = actual number of bytes per sector.
3. Set sector count = number of sectors per track.
4. Issue AF command or AB command.

In this case, the F8 second data sync byte is transferred to the buffer. The buffer requires one extra byte per sector.

One BRDQ interrupt occurs at the very beginning of the command. Therefore, the buffer must be contiguous and large enough to handle all the dumped sectors.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the buffer into the disk buffer pointer register (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue dump command to WD42C22C.
- WD42C22C
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Wait for index.
  10. If I=1, then go to 12 else go to 11.
  11. Search for sync byte. When found, dump 5 data bytes into buffer.
  12. Search for sync byte. When found, dump programmed number of bytes into the buffer.
  13. Decrement sector count. If sector count = 0, then go to 14 else go to step 10.
  14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  15. Read disk controller status register (27_{16}) and errror register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if I = 0 and index detected while searching for an ID field or if CRC of ID field doesn't zero.
- Data AM not found is set and index is detected while searching for a data field. If I=0 or when searching for either an ID or data field when I = 1.
- Data CRC if the data field CRC doesn't zero when I = 0 or if either an ID or data field CRC doesn't zero when I = 1.

5.0 ELECTRICAL AND TIMING SPECIFICATIONS

5.1 MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (ground) ..... +5 V ± 5%

Max voltage on any pin with respect to V_{SS} ..... -0.5V to 5.5

Operating temperature (T_A) ..... 0°C (32°F) to 70°C (158°F)

Storage temperature ..... -55°C (-67°F) to 125°C (257°F)

NOTE

Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

5.2 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	µA	V_{IN} = 0.4 to V_{CC}
I_{OZ}	Tri-state and open drain output leakage		±10	µA	V_{OUT} = 0.4 TO V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=2.0mA
I_{CC}	Supply Current		100	mA	All outputs open.
I_{CCS}	Supply Current (Standby Mode)		25	mA	All inputs at V_{DD} or V_{SS}, disk controller sleep mode, 15 MHz crystal.
For pins 75 thru 82, 40 thru 42, 44 thru 48, 74, 8					

TABLE 14. DC OPERATING CHARACTERISTICS

(HD0 thru HD15, INTRQ, DREQ):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-5mA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=12mA

For pin 8 ($\overline{IOCS16}$, AT PIO mode only):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=20.0mA

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For pins 10, 11, and 12 (WD, EARLY, LATE):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4			I_O=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0mA

For pin 22 ($\overline{RESET}$)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0 mA and VDD at spec. IO=2.0 mA and VDD at VRST2 max VRST3 max.

For pins 36, 37 ($\overline{DS0}$, $\overline{DS1}$):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=48.0 mA

For pins 59-73 (BA0-B14)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PD}	Pulldown Current in read config. mode	40	160	µA	V_{OUT}=2.4V

For pins 5, 6, 9 ($\overline{HRE}$, $\overline{HWE}$, and $\overline{DACK}$ in slave host mode) and pins 40-42, 44-48 (HD8 through HD15 in 8-bit host mode):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PU}	Pullup Current	100	2000	µA	V_{OUT}=0.4 V, V_{DD}=5.25 V

For pin 38 (XTALIN when driven by external osc.):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	3.5		V	
VIL	Input Low Voltage		1.0	V	

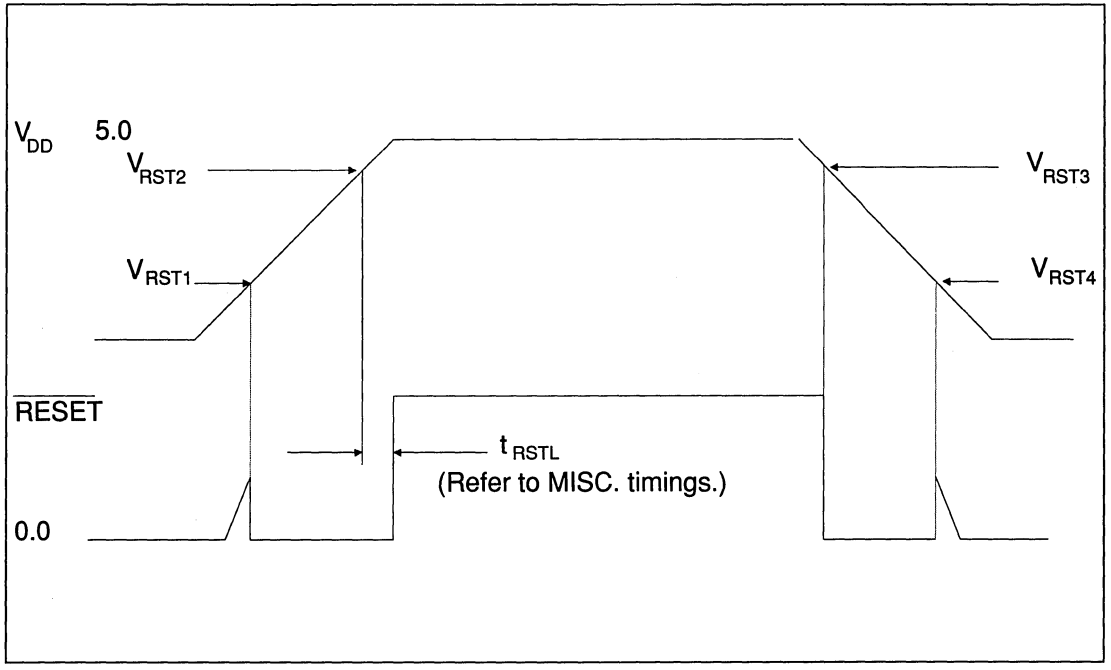

FIGURE 6. POWER QUALIFIED RESET VOLTAGE THRESHOLD

For pins 1-7, 9, 15, 16, 20, 21, 23, 25-35, 40-42, 44-48, 51-58, 59-73, 74, 75-82 (HA0-HA2, HA9, $\overline{HRE}$, HWE, HCS, DACK, INDEX, SCT, WF, DRDY, RESET, ALE, MRE, MWE, AD0-AD7, HD8-HD15, BD0-BD7, BA0-BA15, INTRQ, HD0-HD7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VIH / VIL	Input Voltage Hysteresis	400		mV	

For pin 84 (V_{DD})

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{RST1}	Power Qualified Reset	0.0	2.0	V	See Figure 7.
V_{RST2}	Voltage Threshold	2.5	4.6	V	
V_{RST3}		2.5	4.6	V	
V_{RST4}		0.0	2.0	V	

5.3 AC TIMING CHARACTERISTICS

NOTE

Load capacitance=50 pF each for all other outputs. Timings must be derated for larger load capacitances.

For pins 14, 16, 17, 19 (WC, DRUN, RD, RC):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{RS}	Rise Time		10	nsec	10% to 90%

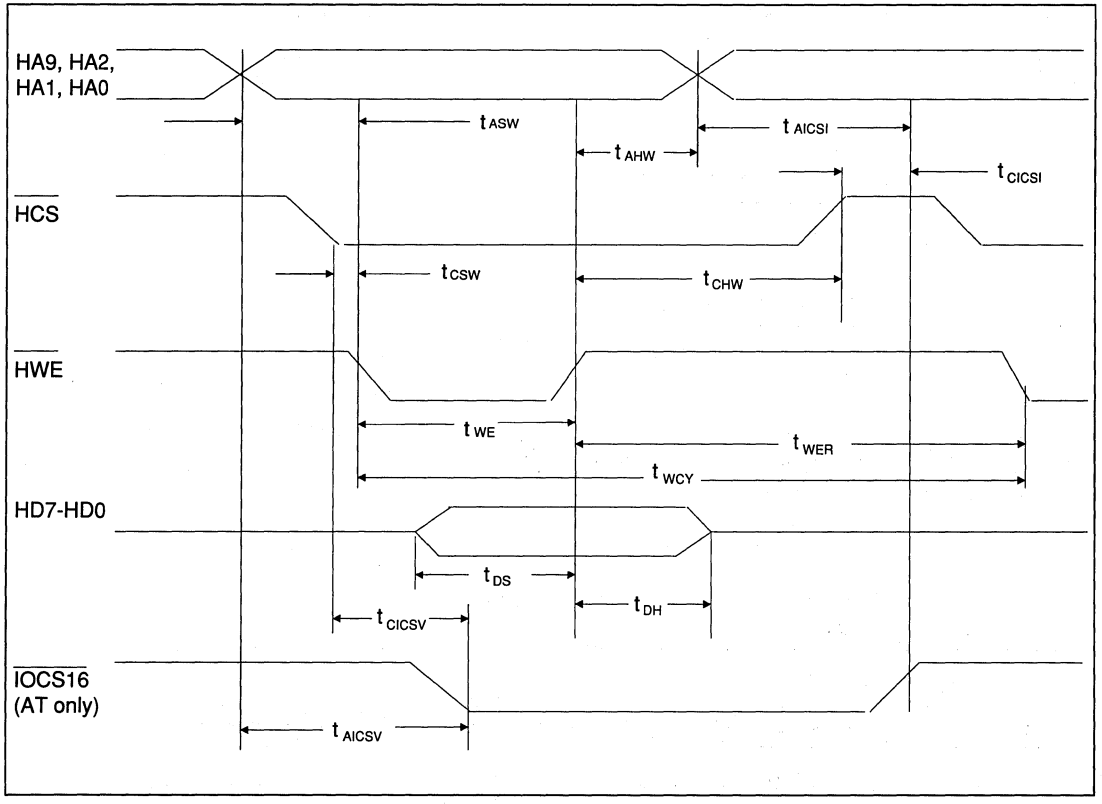

FIGURE 7. AT/XT HOST PROGRAMMED I/O WRITE TIMING

NOTE

A write occurs during the overlap of $\overline{HCS}$ and $\overline{HWE}$.

5.3.1 AT/XT Host Programmed I/O Write Timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASW}	Address Setup to $\overline{HWE}$ Low	30		ns	
t_{CSW}	$\overline{HCS}$ Setup to $\overline{HWE}$ Low	10		ns	
t_{DS}	Data Setup to $\overline{HWE}$ High	30		ns	Port 0 only.
t_{WE}	$\overline{HWE}$ Pulse Width	75		ns	Port 0 only.
t_{DS}	Data Setup to $\overline{HWE}$ High	50		ns	All other ports.
t_{WE}	$\overline{HWE}$ Pulse Width	100		ns	All other ports
t_{DH}	Data Hold from $\overline{HWE}$ High	15		ns	
t_{AHW}	ADDR Hold from $\overline{HWE}$ High	20		ns	
t_{CHW}	$\overline{HCS}$ Hold from $\overline{HWE}$ High	10		ns	
t_{WER}	$\overline{HCS}$ and $\overline{HWE}$ Inactive	20		ns	
t_{WCY}	Write Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16MHz (X=t_{XTAL})
t_{WCY}	Write Cycle Time	150		ns	All other ports
t_{CICSV}	$\overline{IOCS16}$ valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ valid from address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ inactive from $\overline{HCS}$		35	ns	Test circuit 1.
t_{AICSI}	$\overline{IOCS16}$ inactive from address		45	ns	Test circuit 1.

TABLE 15. AT/XT HOST PROGRAMMED I/O WRITE TIMING

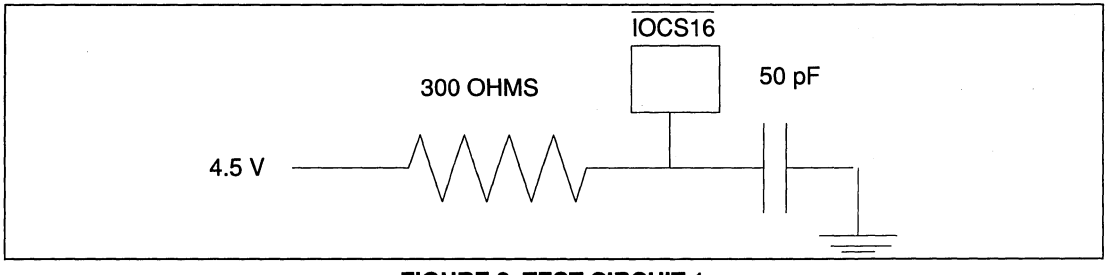

FIGURE 8. TEST CIRCUIT 1

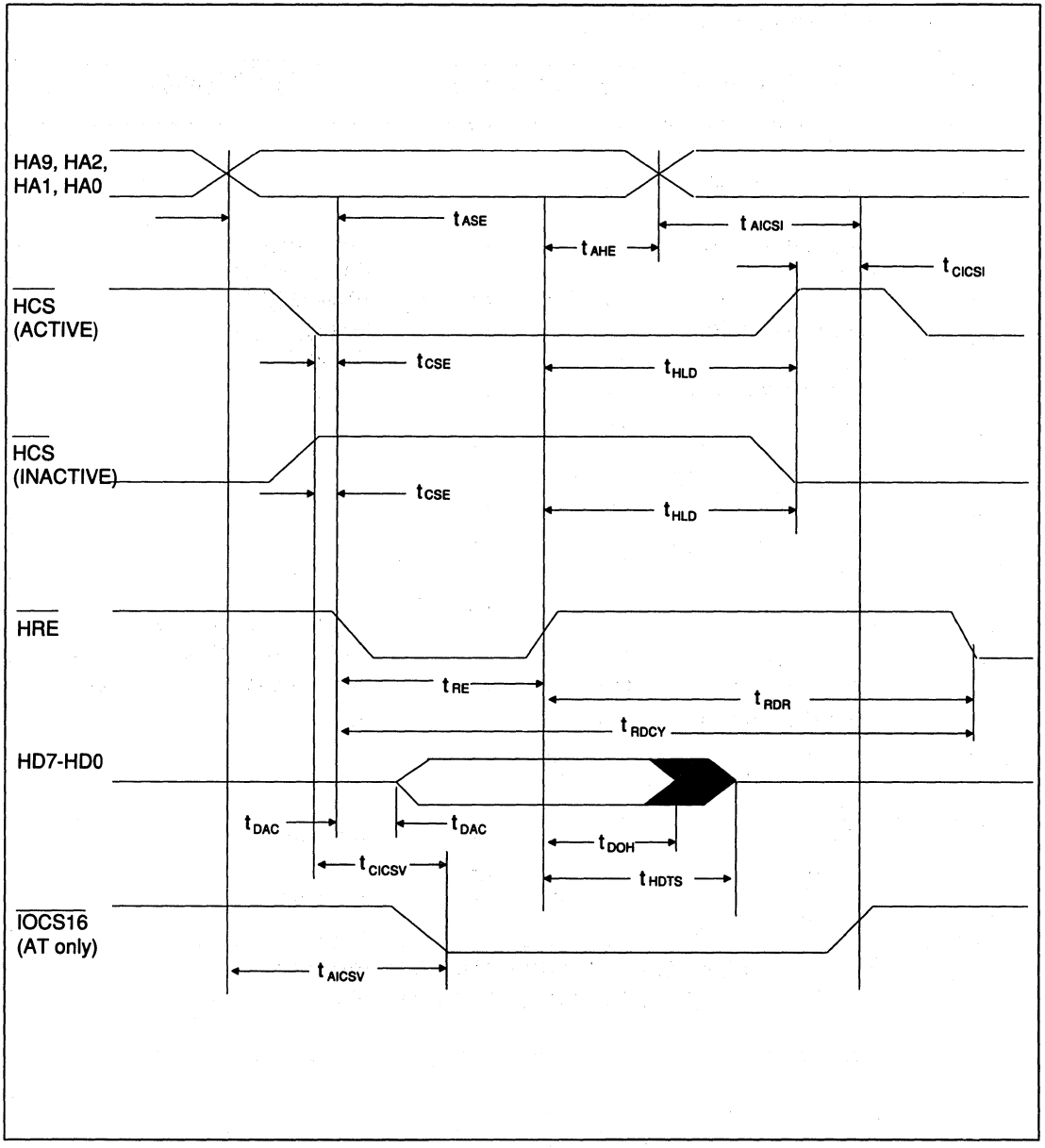

FIGURE 9. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.2 AT/XT Host Programmed I/O Read Timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{HRE}$ Low	30		ns	
t_{CSE}	$\overline{HCS}$ Setup to $\overline{HRE}$ Low	10		ns	
t_{DAC}	Data Valid from $\overline{HRE}$ Low		60 70 100	ns	Port 0, 8-bit. Port 0, 16-bit. All other ports.
t_{RE}	$\overline{HRE}$ Pulse Width	75 100		ns	Port 0 All other ports
t_{DOH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{HDTS}	Data Tri-state from HRE		50	ns	
t_{HLD}	Address, $\overline{HCS}$ Hold from HRE High	10		ns	
t_{RDR}	$\overline{HCS}$ and $\overline{HRE}$ Inactive	20		ns	
t_{RDCY}	Read Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16 MHz (X=t_{XTAL})
t_{RDCY}	Read Cycle Time	150		ns	All other ports.
t_{CICSV}	$\overline{IOCS16}$ Valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ Valid from Address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ Inactive from $\overline{HCS}$		35	ns	Test circuit 1
t_{AICSI}	$\overline{IOCS16}$ Inactive from Address		45	ns	Test circuit 1

TABLE 16. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.3 AT/XT Host DMA Write Timing

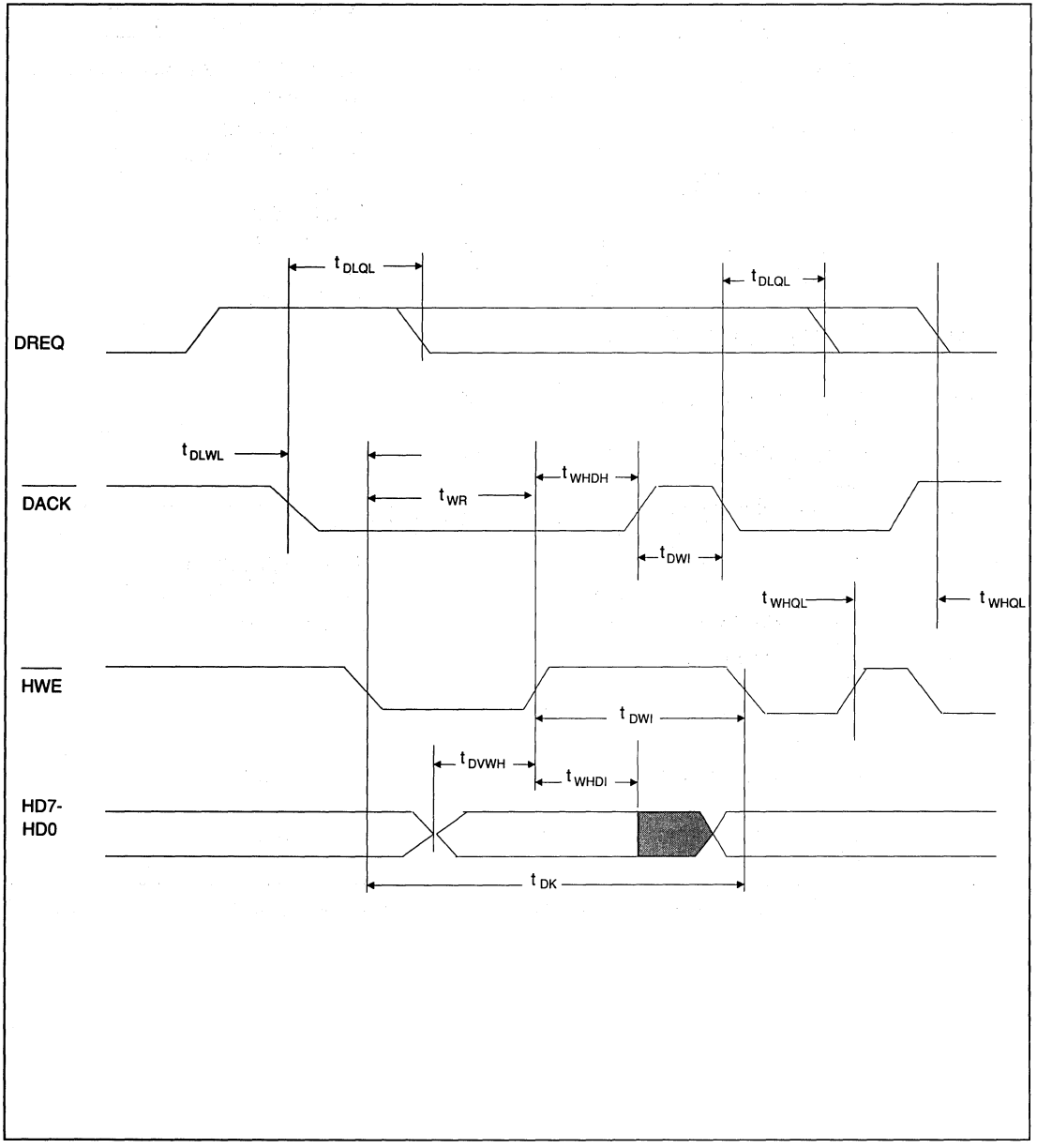

FIGURE 10. AT/XT HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{WHQL}	$\overline{HWE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First transfer count throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLWL}	$\overline{DACK}$ Low to $\overline{HWE}$ Low	0		ns	
t_{WR}	$\overline{HWE}$ Pulse Width	80		ns	
t_{DVWH}	Data Valid to $\overline{HWE}$ High	30		ns	
t_{WHDH}	$\overline{HWE}$ High to $\overline{DACK}$ High	0		ns	
t_{WHDI}	$\overline{HWE}$ High to Data Invalid	15		ns	
t_{DWI}	$\overline{DACK}$ and $\overline{HWE}$ Inactive	20		ns	

TABLE 17. AT/XT DMA WRITE TIMING

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5.3.4 AT/XT Host DMA Read Timing

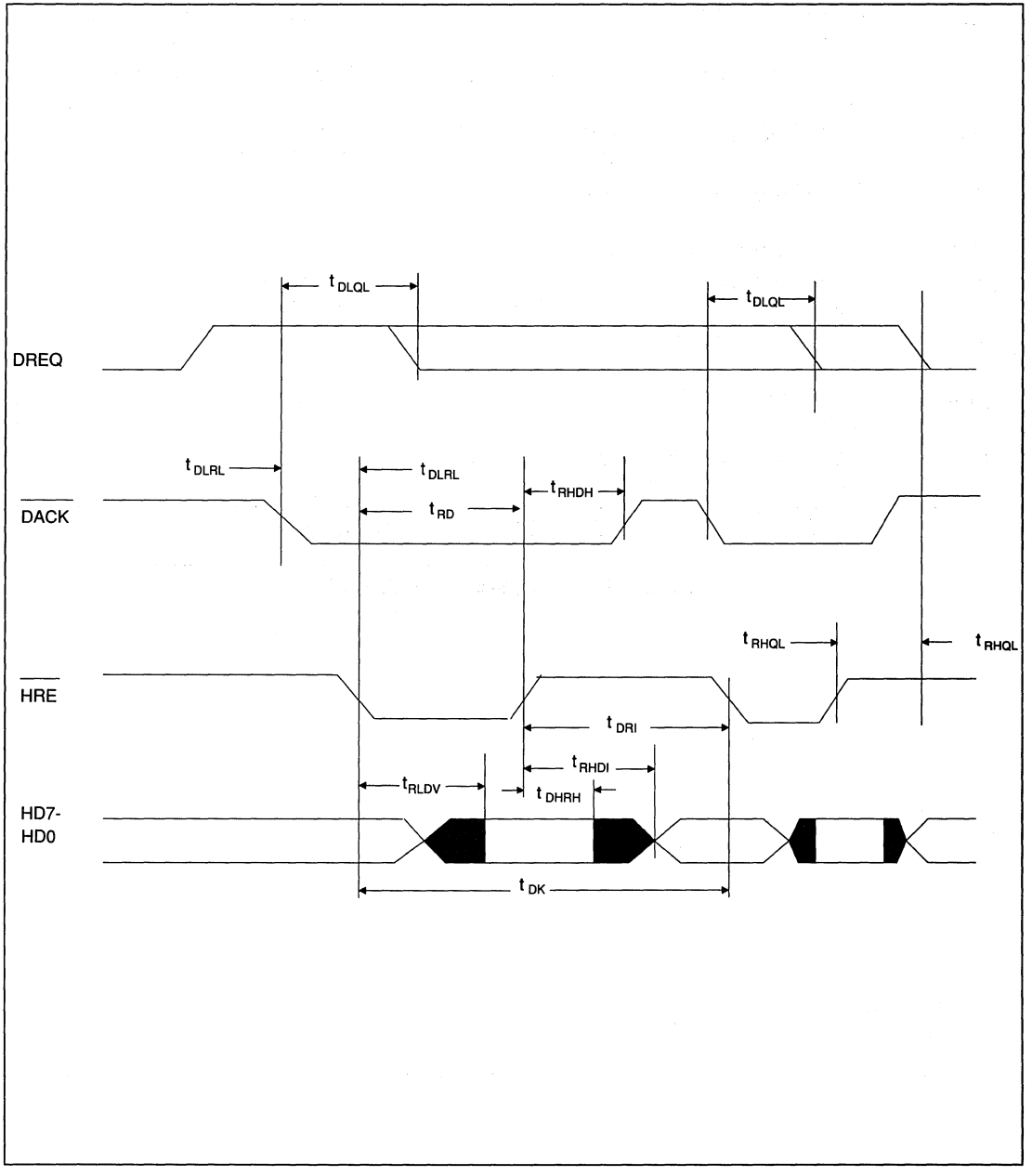

FIGURE 11. AT/XT HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{RHQL}	$\overline{HRE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First TC throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLRL}	$\overline{DACK}$ Low to $\overline{HRE}$ Low	0		ns	
t_{RD}	$\overline{HRE}$ Pulse Width	80		ns	
t_{RLDV}	$\overline{HRE}$ Low to Data Valid		60 70	ns	8-bit mode 16-bit mode
t_{RHDH}	$\overline{HRE}$ High to $\overline{DACK}$ High	0		ns	
t_{DHRH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{RHDI}	$\overline{HRE}$ High to Data tri-state		50	ns	
t_{DRI}	$\overline{DACK}$ and $\overline{HRE}$ Inactive.	20		ns	

TABLE 18. AT/XT DMA READ TIMING

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5.3.5 Slave Host Write Timings

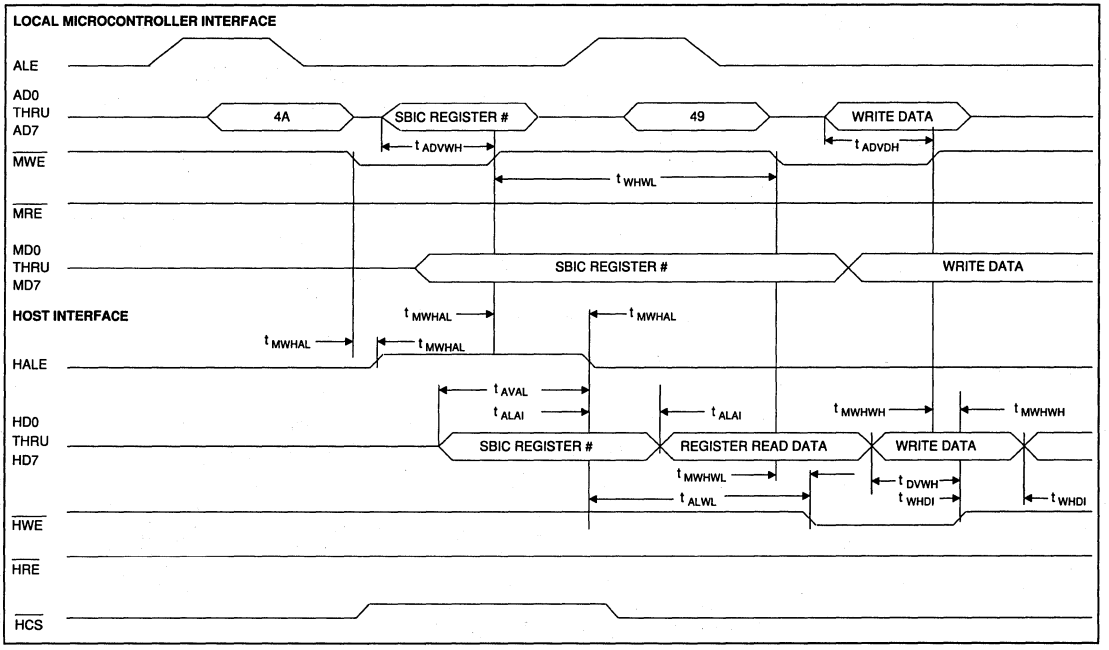


FIGURE 12. SLAVE HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHWL}	Address Port Write to Data Write Recovery Time	120	10000	ns	
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{ALAI}	HD Address Hold From HALE low	0		ns	
t_{ALWL}	HALE Low To $\overline{HWE}$ Low	90		ns	
t_{DVWH}	HD Valid to $\overline{HWE}$ High	70		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{WHDI}	HD Inactive from $\overline{HWE}$	0		ns	
t_{MWHWL}	$\overline{MWE}$ Low to HWE Low		150	ns	
t_{MHWH}	MWE High to HWE High		150	ns	

TABLE 19. SLAVE HOST WRITE TIMING

5.3.6 Slave Host Read Timings

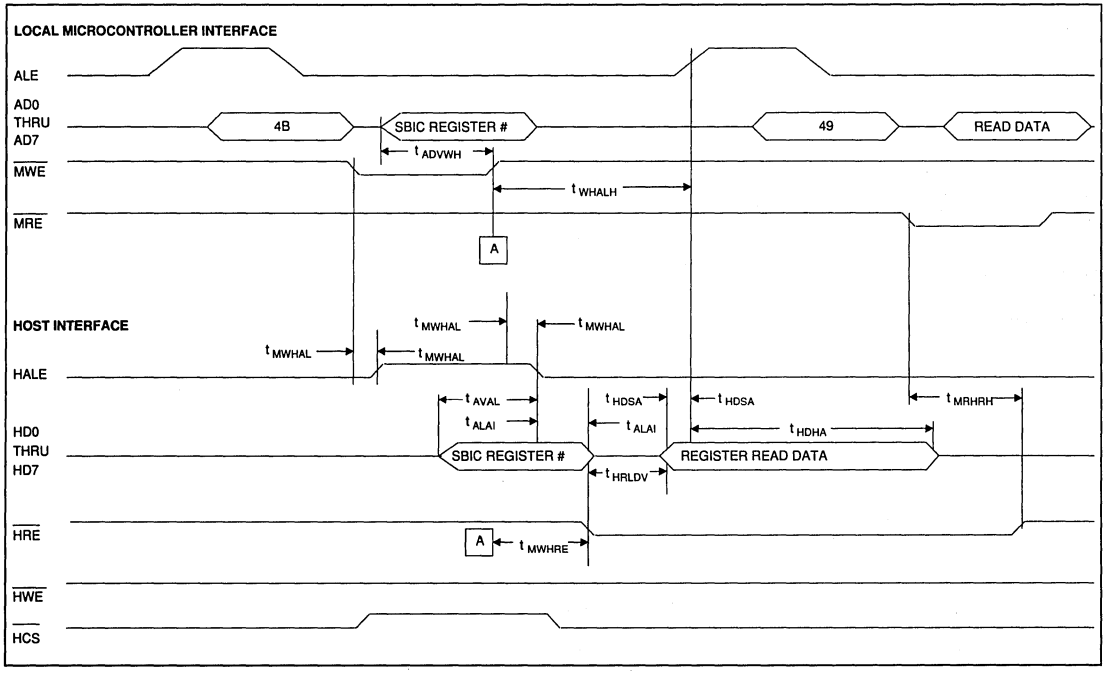


FIGURE 13. SLAVE HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHALH}	Address Port Write to ALE High Read Recovery Time	400	10000	ns	t_{HRLDV}=210 ns
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{MWHRE}	$\overline{MWE}$ to $\overline{HRE}$ Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns.
t_{ALAI}	HD Address Hold from HALE Low	0		ns	
t_{HDSA}	HD Data **Setup to** ALE High	40		ns	
t_{HDHA}	HD Data **Hold from** ALE High	40		ns	
t_{MRHRH}	$\overline{MRE}$ Low to $\overline{HRE}$ High Delay	0		ns	
t_{HRLDV}	HRE Low to HD Data Valid Delay				t_{HRLDV} is a function of the slave peripheral device and only affects t_{WHALH}. $t_{WALH} = t_{MWHRE} + t_{HRLDV} + t_{HDSA}$

TABLE 20. SLAVE HOST READ TIMING

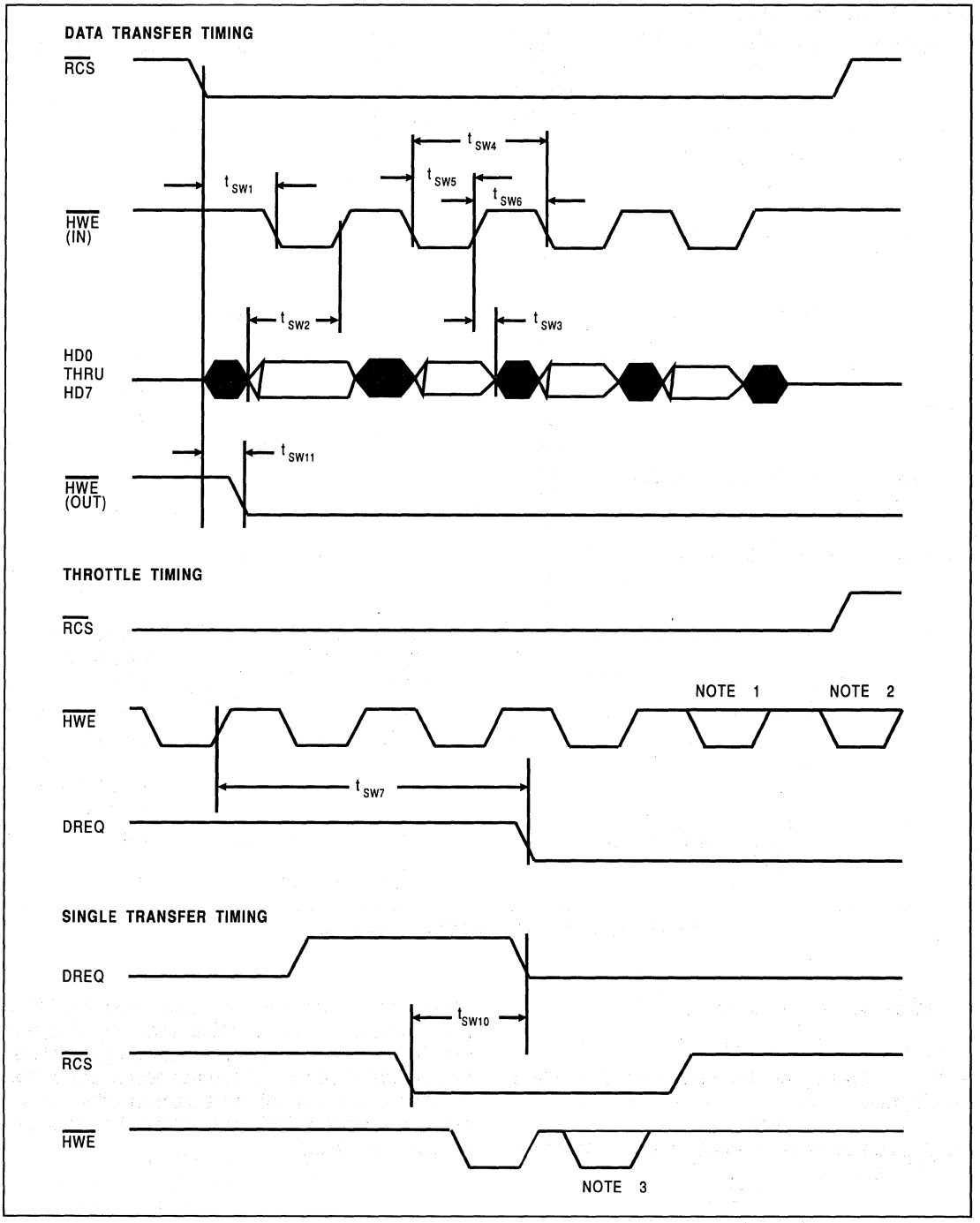


FIGURE 14. SLAVE HOST DMA WRITE TIMING

5.3.7 Slave Host DMA Write Timing

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to $\overline{HWE}$ First Transfer of Burst	0 0 0		ns	
t_{SW2}	HD Valid to $\overline{HWE}$ Rising	30 30 30		ns	
t_{SW3}	$\overline{HWE}$ Rising to HD Invalid	15 15 15		ns	
t_{SW4}	$\overline{HWE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HWE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HWE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HWE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HWE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 21. SLAVE HOST DMA WRITE TIMING

The following notes apply to Figure 15.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although four transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

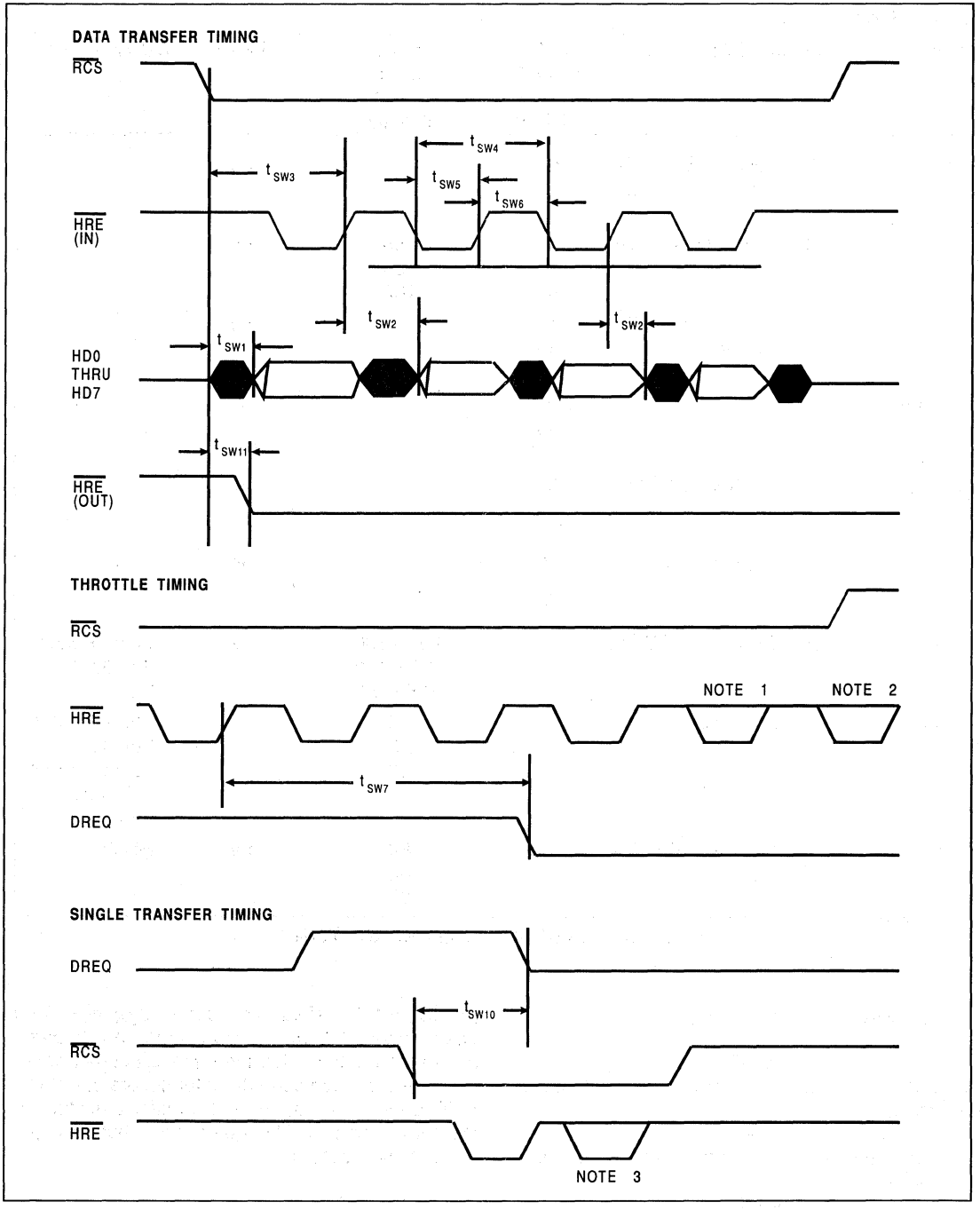


FIGURE 15. SLAVE HOST DMA READ TIMING

5.3.8 Slave Host DMA Read Timing

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to HD Valid First Transfer of Burst	0 0 0		ns	
t_{SW2}	$\overline{HRE}$ Rising to HD Valid	5 5 5	180 180 180	ns	
t_{SW3}	$\overline{RCS}$ Low to First $\overline{HRE}$ Rising Edge	140 140 100		ns	
t_{SW4}	$\overline{HRE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HRE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HRE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HRE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HRE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 22. SLAVE HOST DMA READ TIMING

The following notes apply to Figure 16.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although 4 transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

5.3.9 Buffer RAM Write Timing (Internal Oscillator; XTAL = 8 to 25 MHZ)

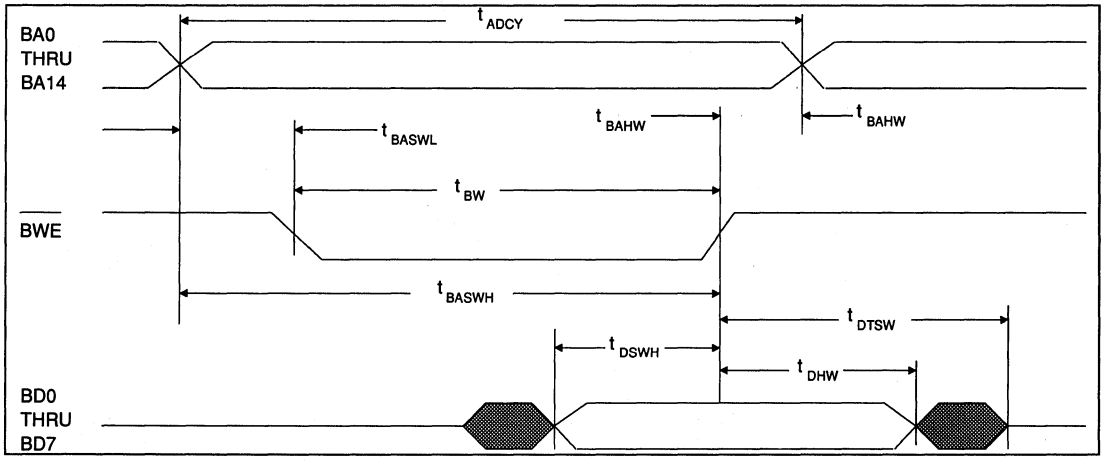


FIGURE 16. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN Bin 02 Bin 03 Bin 05	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35 $2*t_{XTAL}$-25		ns	Any XTAL
t_{BASWH}	Addres Setup to BWE High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Addres Setup to BWE Low	$0.5*t_{XTAL}$-20 $0.5*t_{XTAL}$-35 $0.5*t_{XTAL}$-20		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-35 $1.5*t_{XTAL}$-25		ns	Any XTAL
t_{BAHW}	Address Hold From BWE High	5 5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$1.5*t_{XTAL}$-40 $1.5*t_{XTAL}$-60 $1.5*t_{XTAL}$-35		ns	Any XTAL
t_{DHW}	Data Hold from BWE High	10 10 10		ns	Any XTAL
t_{DTSW}	Data Tri-state from BWE High		50	ns	Any XTAL

TABLE 23. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

5.3.10 Buffer RAM Read Timing (Internal Oscillator; XTAL = 8 to 20 MHZ)

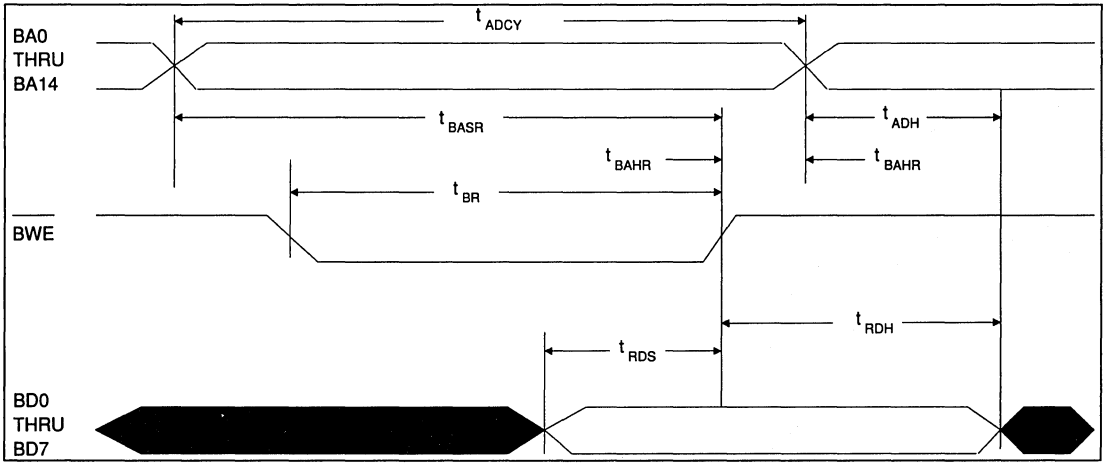


FIGURE 17. BUFFER READ TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to BOE High	72 125	ns	Max XTAL
t_{BASR}	Address Setup to BOE High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BR}	BOE Pulse Width	45 75	ns	Max XTAL
t_{BR}	BOE Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from BOE High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to BOE High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from BOE High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

- All timings in this table **only** are referenced to 1.5V levels.

TABLE 24. BUFFER READ TIMING (INTERNAL OSCILLATOR)

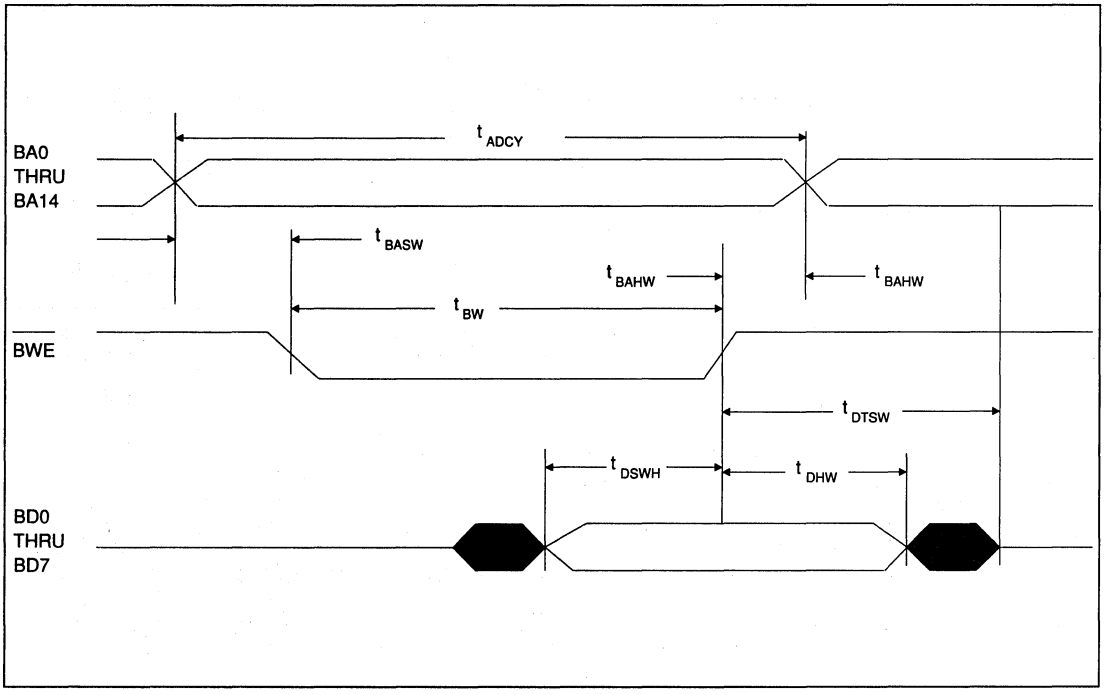


FIGURE 18. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

5.3.11 Buffer RAM Write Timing (External Oscillator; XTAL = 8 to 20 MHz)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125		ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	5 5		ns	Max XTAL/ 50% XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	t_{XCH}-20 t_{XCH}-35		ns	Any XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	60 105		ns	Max XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	55 85		ns	Max XTAL/ 50% XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$t_{XTAL}+t_{XCL}$-30 $t_{XTAL}+t_{XCL}$-35		ns	Any XTAL
t_{BAHW}	Address Hold from $\overline{BWE}$ High	5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	35 60		ns	Max XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$t_{XTAL}+t_{XCH}$-40 $t_{XTAL}+t_{XCH}$-60		ns	Any XTAL/ %50 XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10		ns	Any XTAL
t_{DTSW}	Data tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

- All timings in this table only are referenced to 1.5 V levels except t_{DHW}.

TABLE 25. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

5.3.12 Buffer RAM Read Timing (External Oscillator; XTAL=8 to 20 MHz)

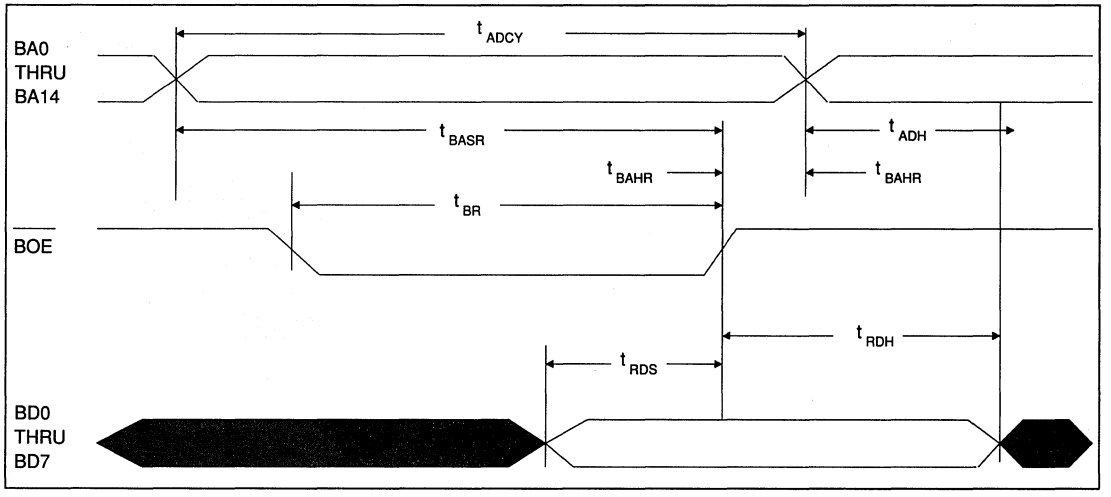


FIGURE 19. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL/50% XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to BOE High	72 125	ns	Max XTAL/50% XTAL
t_{BASR}	Address Setup to BOE High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	
t_{BR}	BOE Pulse Width	45 75	ns	Max XTAL/50% XTAL
t_{BR}	BOE Pulse Width	$t_{XTAL}+t_{XCH}$-30 $t_{XTAL}+t_{XCH}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from BOE High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to BOE High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from BOE High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

- All timings in this table referenced to 1.5 V levels.

TABLE 26. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

5.3.13 Microprocessor Write Timing (INTEL Bus)

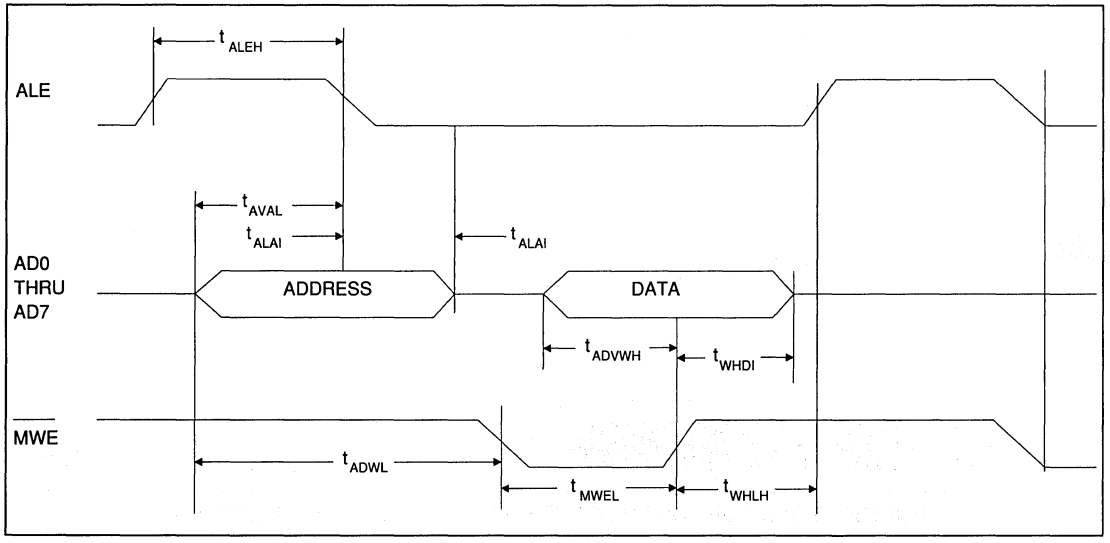


FIGURE 20. MICROPROCESSOR WRITE TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to ALE Low	15	ns	
t_{ALAI}	Address Hold from ALE Low	5	ns	
t_{ALEH}	ALE High Pulse Width	30	ns	
t_{ADVWH}	Data Setup to $\overline{MWE}$ High	50 130	ns	HSMB=0 HSMB=1
t_{WHDI}	Data Hold from $\overline{MWE}$ High	5	ns	
t_{MWEL}	$\overline{MWE}$ Low Pulse Width	75	ns	
t_{ADWL}	Address Valid to $\overline{MWE}$ Low	55	ns	
t_{WHLH}	$\overline{MWE}$ High to ALE High	10	ns	

TABLE 27. MICROPROCESSOR WRITE TIMING (INTEL BUS)

5.3.14 Microprocessor Write Timing (Motorola Bus)

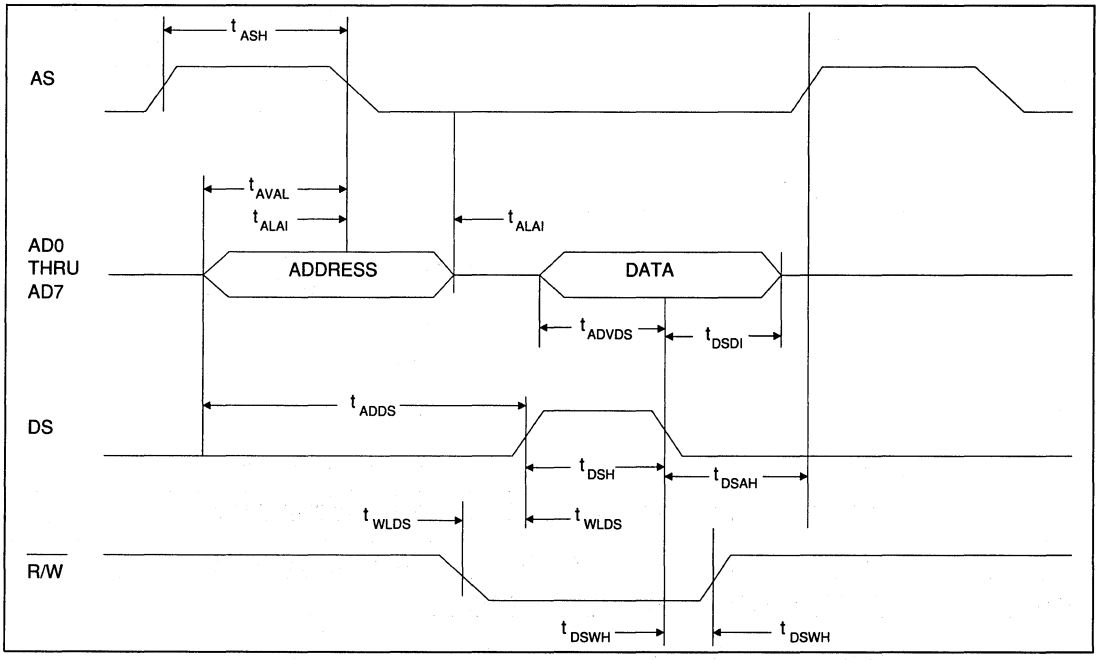


FIGURE 21. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to AS Low	15	ns	
t_{ALAI}	Address Hold from AS	5	ns	
t_{ASH}	AS High Pulse Width	30	ns	
t_{ADVDS}	Data Setup to DS Low	50 130	ns	HSMB=0 HSMB=1
t_{DSDI}	Data Hold from DS Low	5	ns	
t_{DSH}	DS High Pulse Width during Write	75	ns	
t_{WLDS}	R/$\overline{W}$ Low to DS High	5	ns	
t_{DSWH}	DS Low to R/$\overline{W}$ High	20	ns	
t_{ADDS}	Address High to DS High	55	ns	
t_{DSAH}	DS Low to AS High	10	ns	

TABLE 28. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

5.3.15 Microprocessor Read Timing (INTEL Bus)

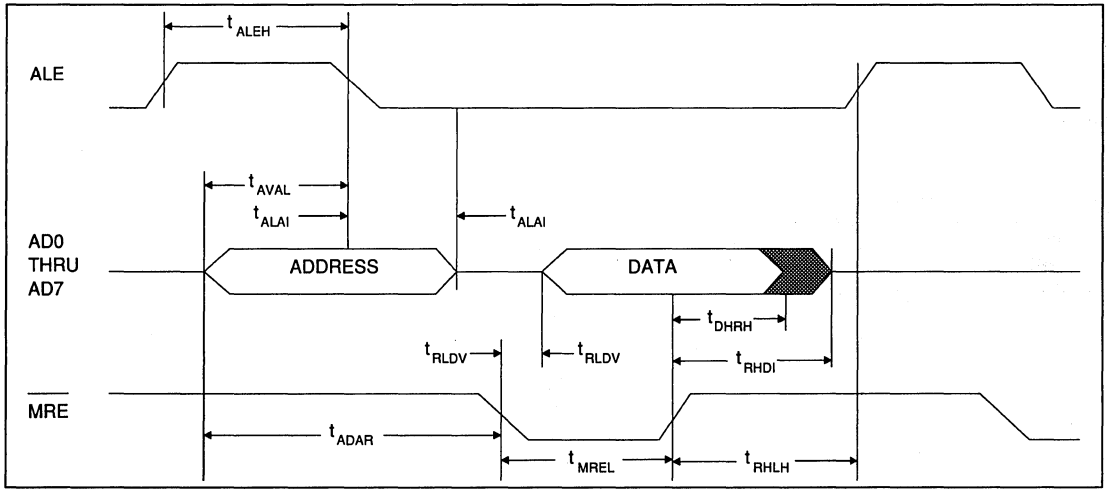


FIGURE 22. MICROPROCESSOR READ TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to ALE Low	15		ns
t_{ALAI}	Address Hold from ALE Low	5		ns
t_{ALEH}	ALE High Pulse Width	30		ns
t_{RLDV}	Data Valid from $\overline{MRE}$ Low		100	ns
t_{DHRH}	Data Hold from $\overline{MRE}$ High	10		ns
t_{RHDI}	Data Tri-state from $\overline{MRE}$ High		50	ns
t_{MREL}	$\overline{MRE}$ Low Pulse Width	100		ns
t_{ADAR}	Address Valid to $\overline{MRE}$ Low	55		ns
t_{RHLH}	$\overline{MRE}$ High to ALE High	10		ns

TABLE 29. MICROPROCESSOR READ TIMING (INTEL BUS)

5.3.16 Microprocessor Read Timing (Motorola Bus)

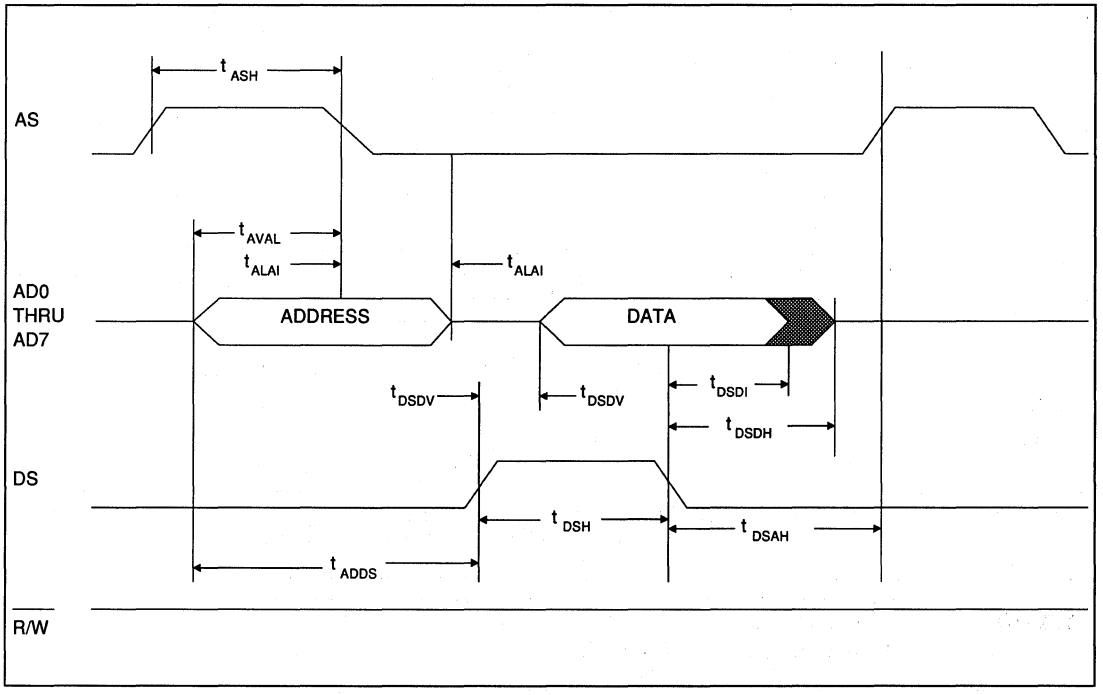


FIGURE 23. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to AS Low	15		ns
t_{ALAI}	Address Hold from AS Low	5		ns
t_{ASH}	AS High Pulse Width	30		ns
t_{DSDV}	Data Valid from DS High		100	ns
t_{DSDI}	Data Tri-state from DS Low		50	ns
t_{DSH}	DS High pulse Width during Read	100		ns
t_{ADDS}	Address Valid to DS High	55		ns
t_{DSAH}	DS Low to AS High	10		ns

TABLE 30. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

5.3.17 Write Data Timing (MFM/RLL Mode; WC 5 to 15 MHz)

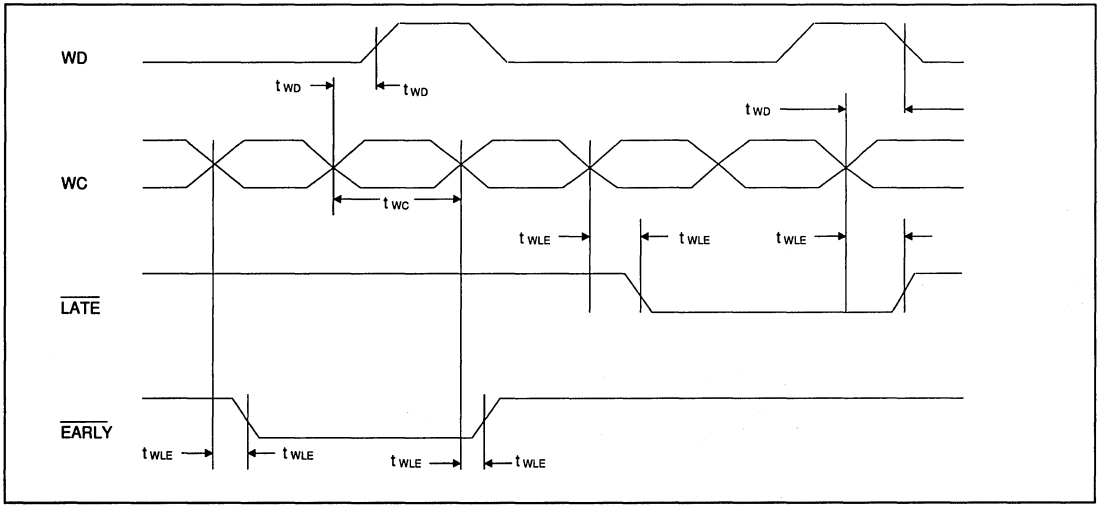


FIGURE 24. WRITE DATA TIMING (MFM/RLL MODE)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
		20 MHz		
		12 MHz		
t_{WC}	WC Pulse Width	28	500	ns
		45	500	
t_{WLE}	Early/Late Propagation	3	15	ns
		3	25	
t_{WD}	WD Propagation Delay	3	15	ns
		3	25	
t_{WCF}	WC Frequency	1	15	MHz
		1	10	

TABLE 31. WRITE DATA TIMING (MFM/RLL MODE)

26

5.3.18 Write Data Timing (NRZ Mode; WC 5 to 15 MHz)

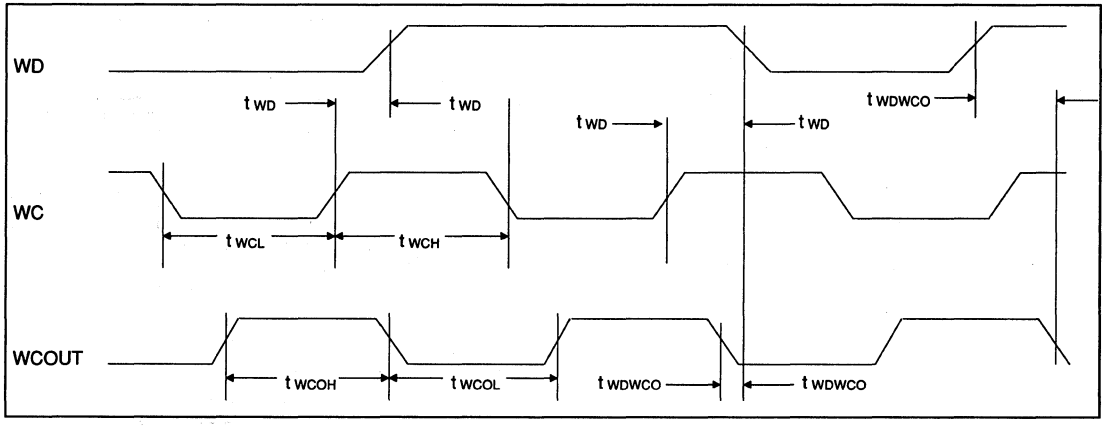


FIGURE 25. WRITE DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{WCL}	WC Pulse Width Low	20 27	500 500	ns
t_{WCH}	WC Pulse Width High	20 27	500 500	ns
t_{WLE}	Early/Late Propagation	3 3	15 25	ns
t_{WD}	WD Propagation Delay	3 3	15 25	ns
t_{WCF}	WC Frequency	1 1	22 16.5	MHz
t_{WCOL}	WCOUT Pulse Width Low	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOL}	WCOUT Pulse Width Low		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WCOH}	WCOUT Pulse Width High	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOH}	WCOUT Pulse Width High		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WDWCO}	WD Prop Delay from WCOUT	-5 -8	+5 +8	ns

TABLE 32. WRITE DATA TIMING (MFM/RLL MODE)

5.3.19 Read Data Timing (MFM/RLL Mode; RC/WC 5 to 15 MHz)

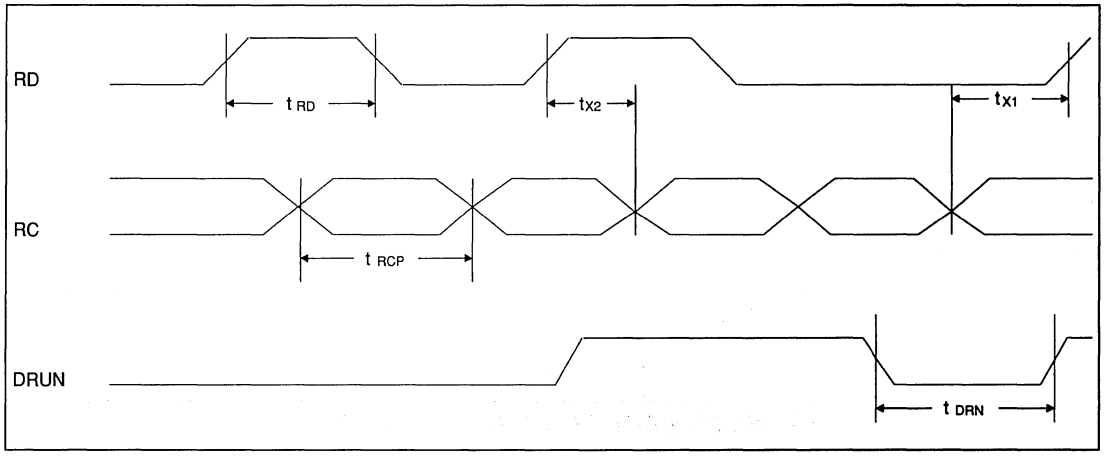


FIGURE 26. READ DATA TIMING (MFM/RLL)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	27 45	500 500	ns
t_{X1}	RC Transition to Next Leading RD	5 10		ns
t_{X2}	Leading RD to Next RC Transition	10 20		ns
t_{RD}	Read Data Pulse Width	20 30	t_{RCP} t_{RCP}	ns
t_{DRN}	DRUN Low Pulse Width	25 25		ns
t_{RCF}	RC Frequency	1 1	15 10	MHz

TABLE 33. READ DATA TIMING (MFM/RLL)

5.3.20 Read Data Timing (NRZ Mode; WC 5 to 20 MHz)

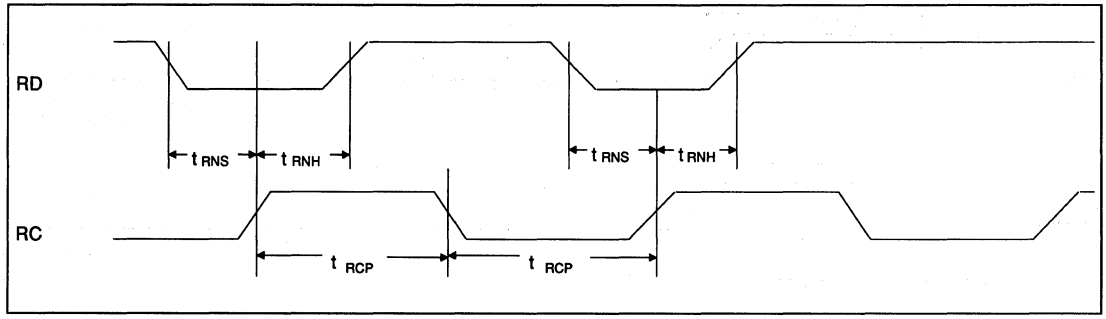


FIGURE 27. READ DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	20 27	500 500	ns
t_{RNS}	RD Setup to RC High	7 10		ns
t_{RNH}	RD Hold from RC High	7 10		ns
t_{RCF}	RC Frequency	1 1	22 16.5	MHz

TABLE 34. READ DATA TIMING (NRZ MODE)

5.3.21 Miscellaneous Timing

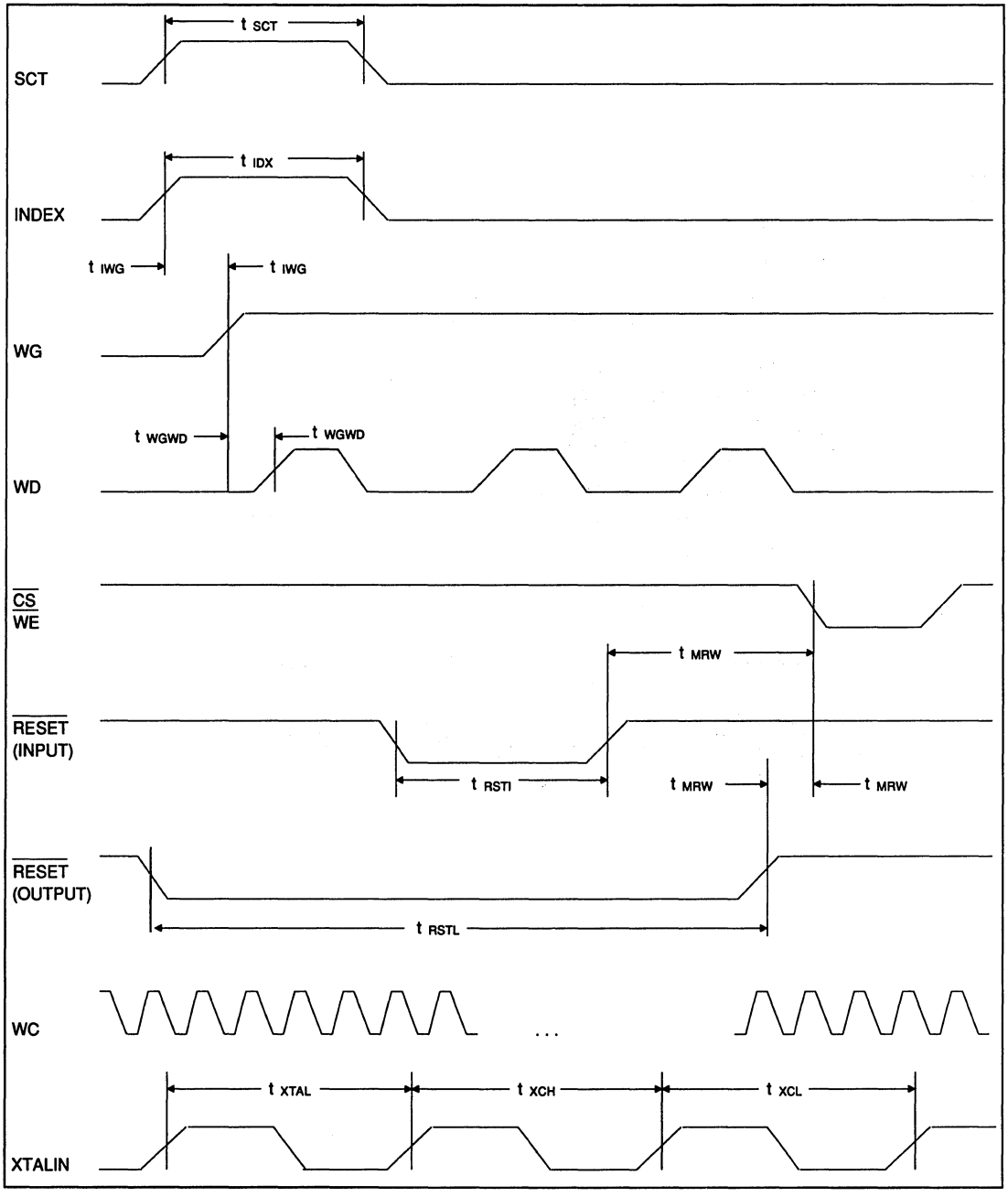


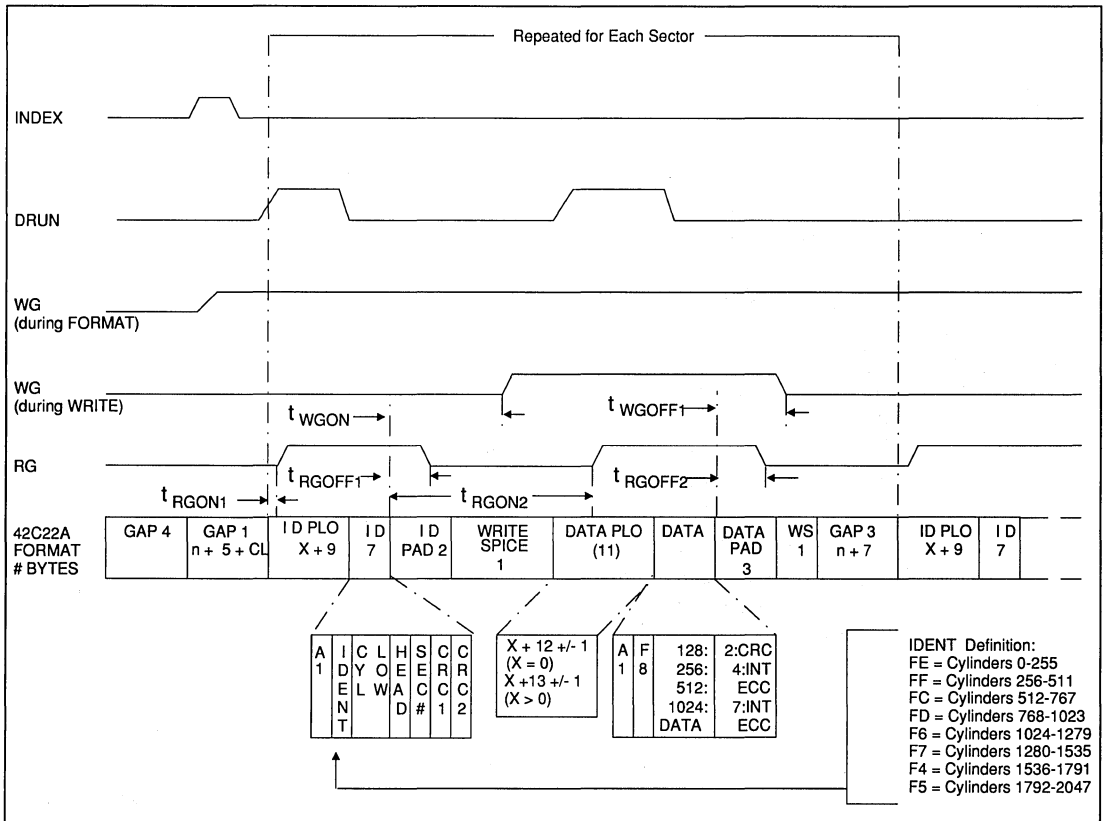
FIGURE 28. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{IDX}	Index Pulse Width	100		ns	
t_{SCT}	SCT Pulse Width	100		ns	
t_{IWG}	Index to write gate	0	4	WC periods	Gap data=33 in RLL mode. Any gap data in MFM and NRZ.
t_{WGWD}	Write gate to write data	0	4	WC periods	
t_{RSTI}	$\overline{\text{RESET}}$ in pulse width low	24		WC periods	
t_{MRW}	$\overline{\text{MR}}$ Trailing to Host Register Write	2.4		µs	
F_{RCWC}	Difference of RC Frequency from WC Frequency	-15%	+15%		
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	51.2		ms	XTAL=10 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	41.3		ms	XTAL=12.5 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	25.6		ms	XTAL=20 MHz
t_{XTAL}	Clock Period	50 70	125	ns	
t_{XCH}	Clock High Time	25 30		ns	
t_{XCL}	Clock Low Time	25 30		ns	

NOTE

t_{XTAL}, t_{XCH}, and t_{XCL} timings at 2.5 V levels.

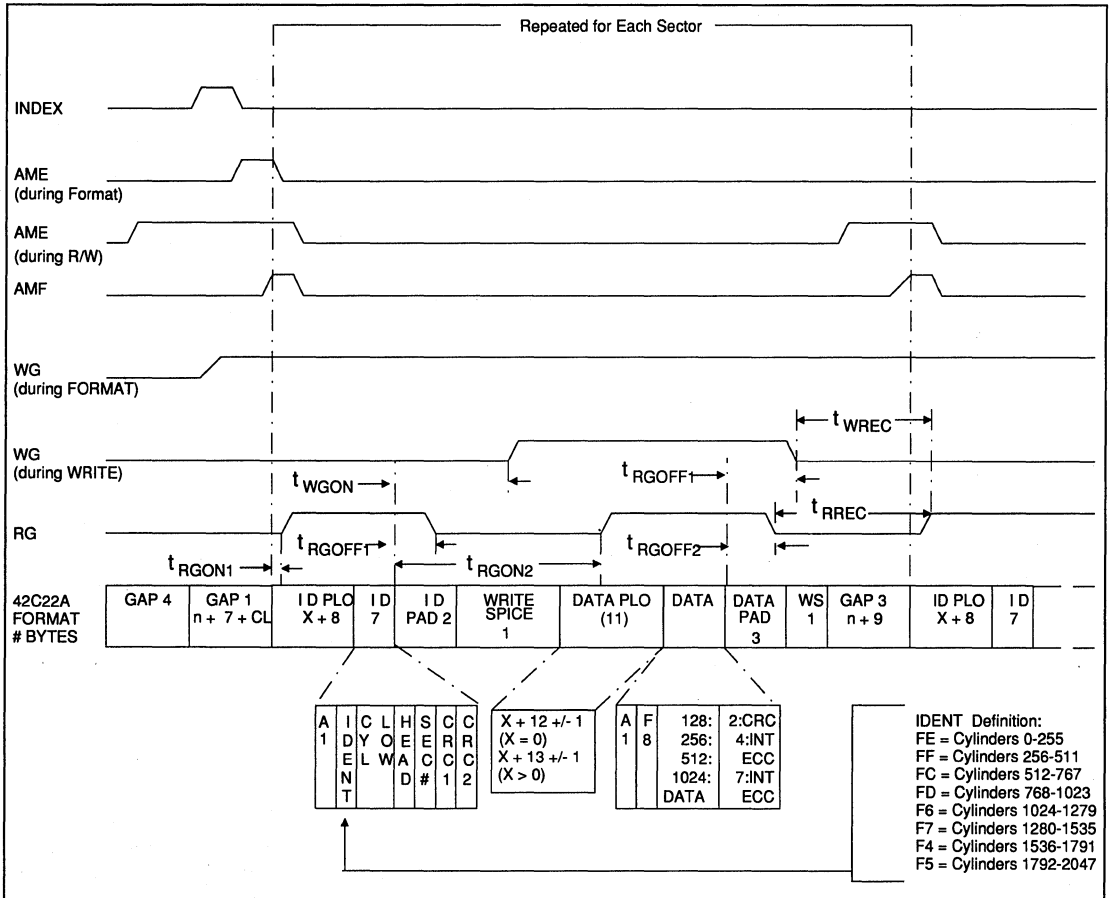
TABLE 35. MISCELLANEOUS TIMING



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.

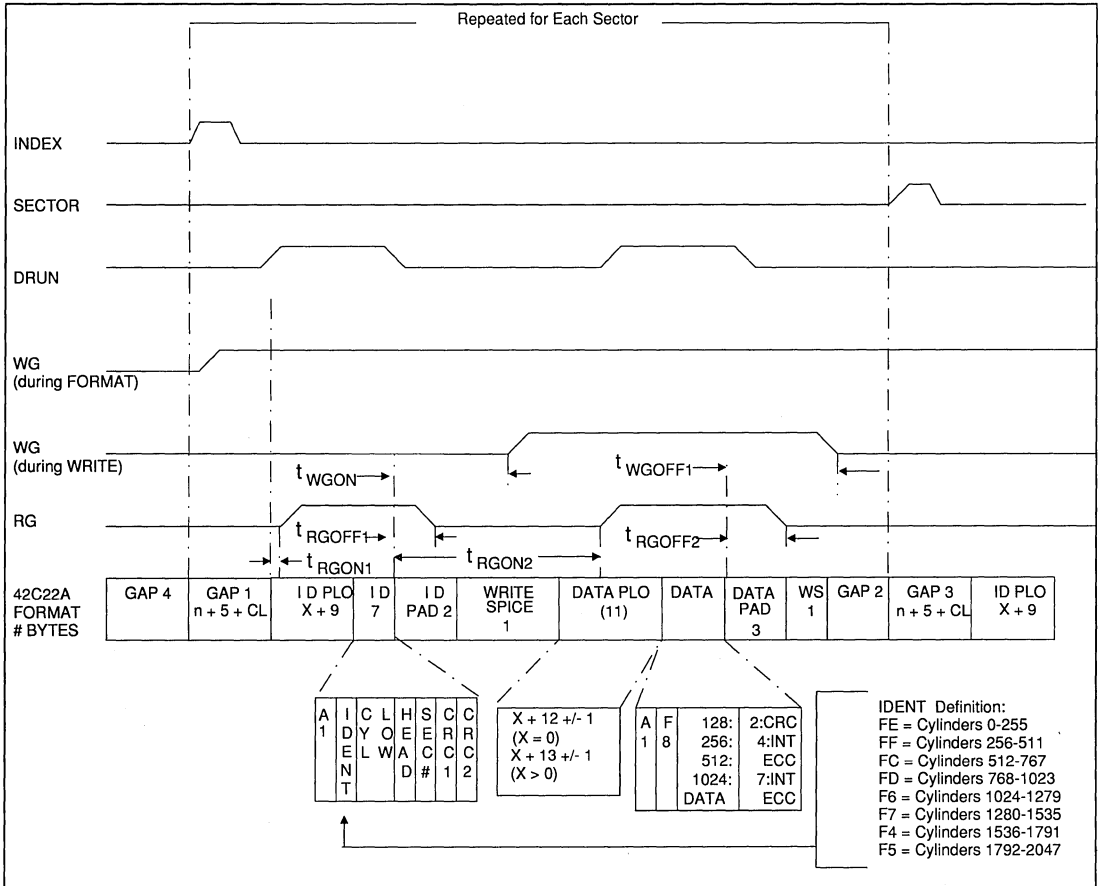
FIGURE 29. SOFT SECTOR MFM/RLL TRACK FORMAT



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = 3 ± 1 bit times with respect to AMF.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WRREC} = 21 to 35 bytes minimum. t_{RREC} = 23 bytes minimum.

FIGURE 30. SOFT SECTOR NRZ TRACK FORMAT

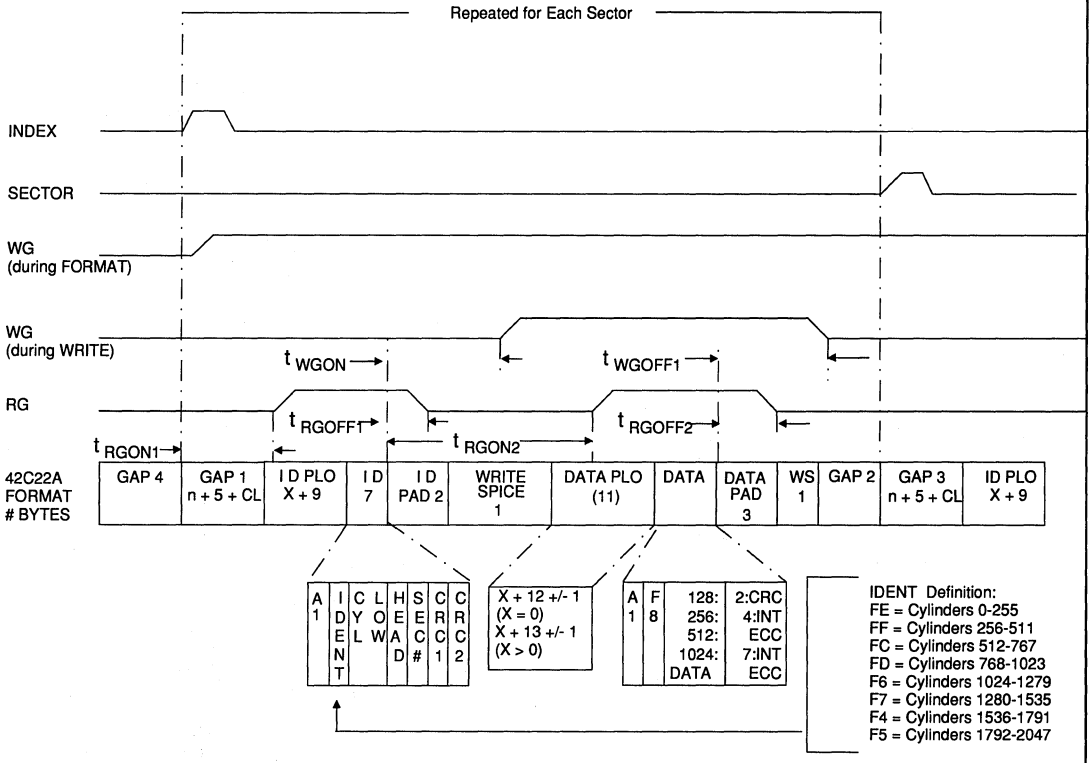


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during format. DRUN is tied to DRUNSCT during read and write.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 31. HARD SECTOR RLL/MFM TRACK FORMAT (WITH SOFT SECTOR READ/WRITE)

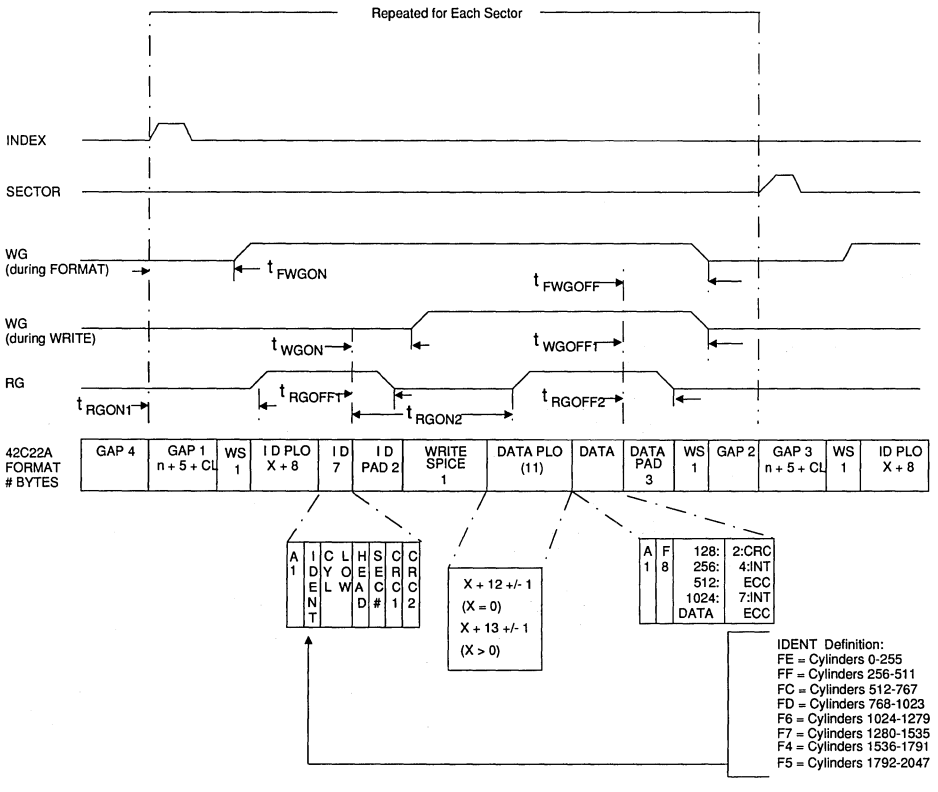


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

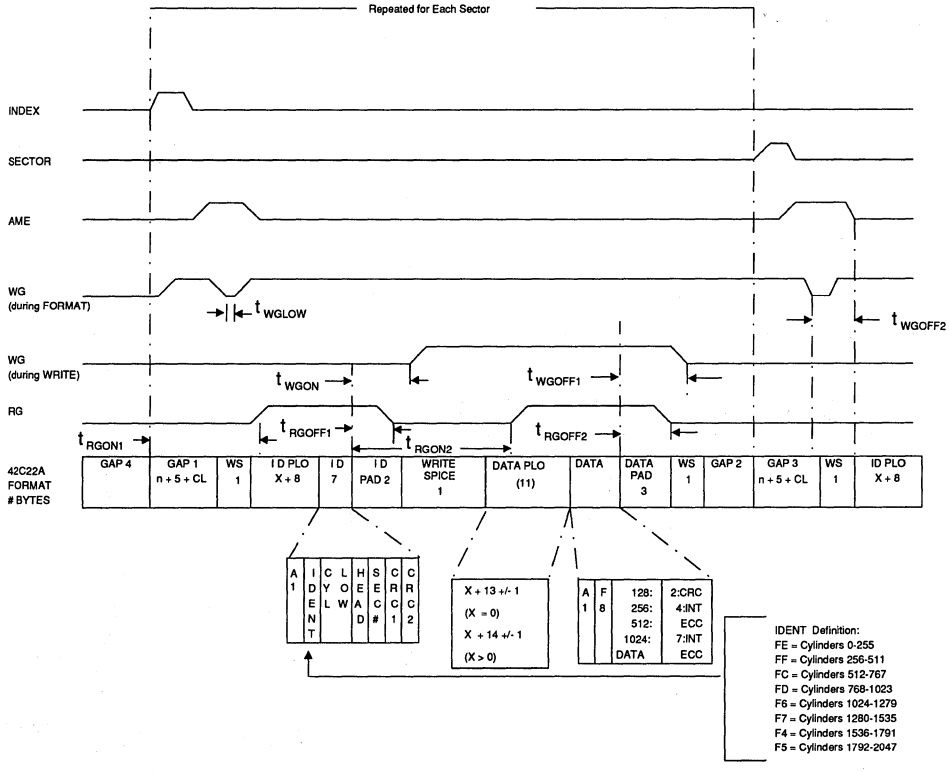
FIGURE 32. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND CONTINUOUS WG OPTION)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)
11. t_{FWGON} = n + 5 + CL byte times with respect to INDEX/SECTOR. t_{WGOFF} = 20 bit times with respect to WD out.

FIGURE 33. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND WG PULSE)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0.
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WGLOW} = 2 bit times. t_{WGOFF2} = 8 bit times. Both timings with respect to NRZWD out.
11. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 34. HARD SECTOR NRZ TRACK FORMAT

5.4 Package Diagrams

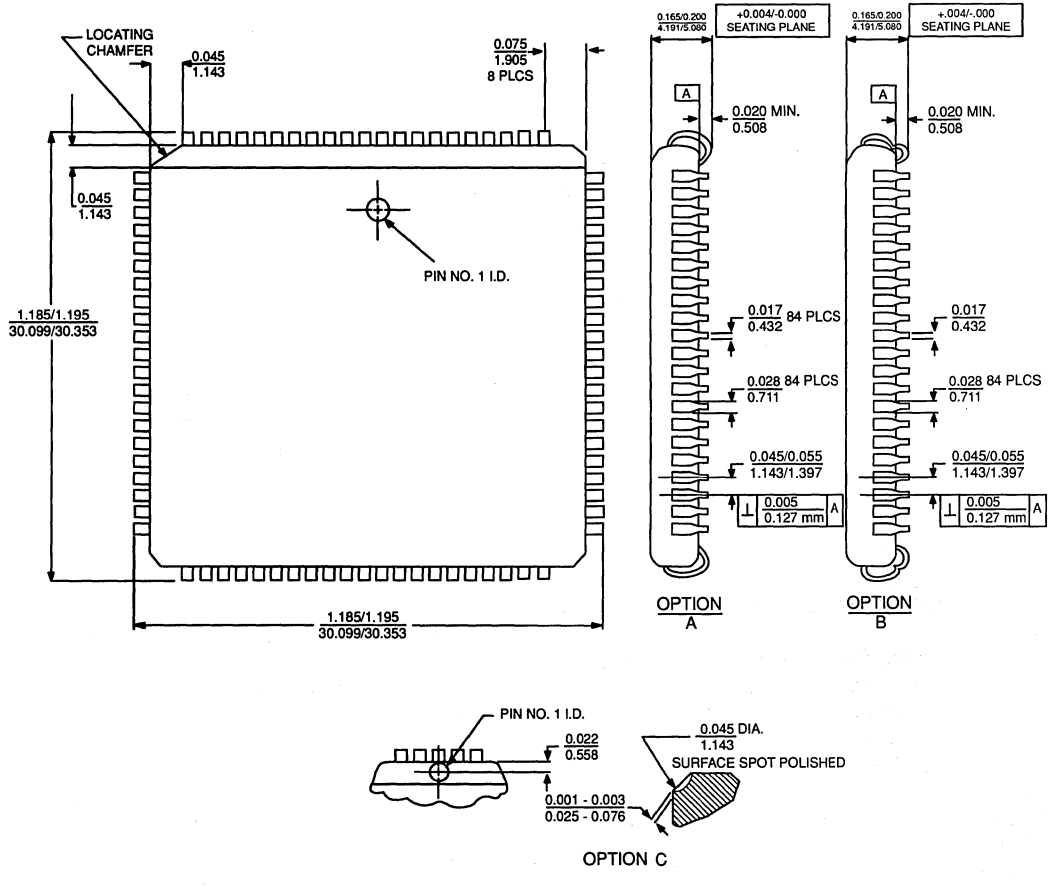


FIGURE 35. 84 LEAD PLCC

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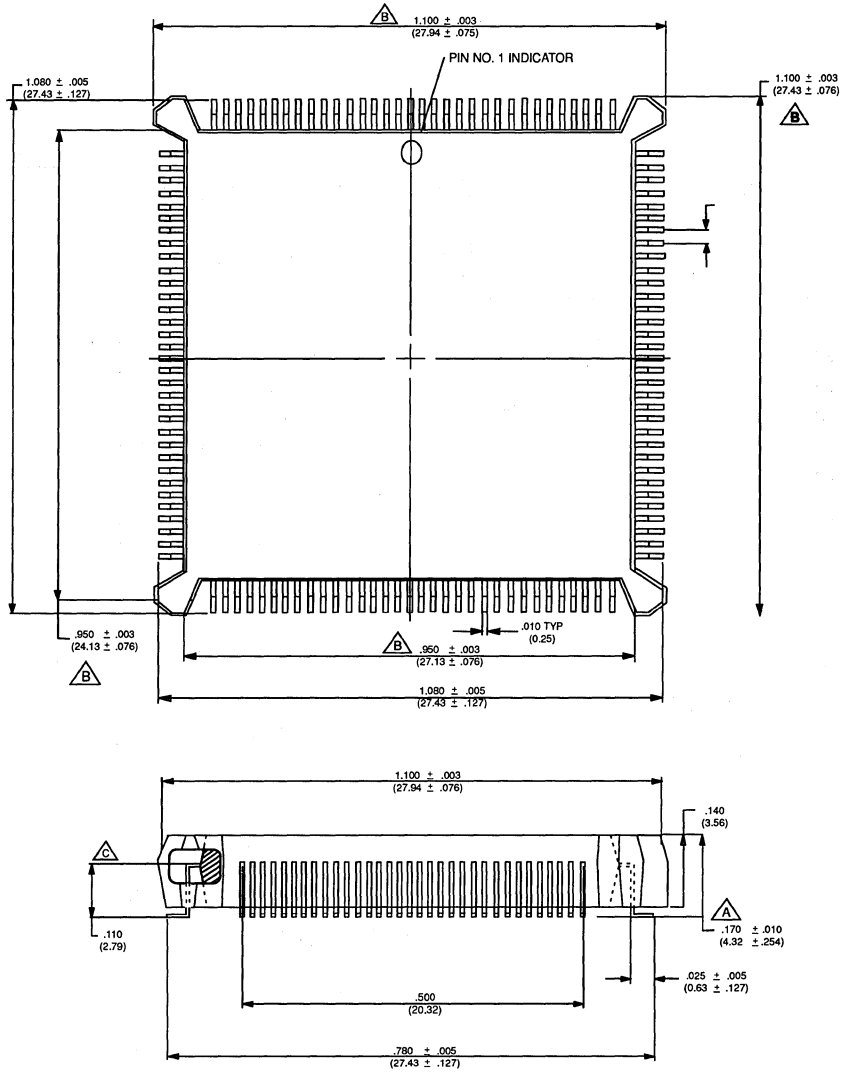

FIGURE 36. 84 LEAD PQFP

WD60C31B

Optical Disk Drive

Encoder/Decoder

WESTERN DIGITAL

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APPENDICES

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LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The WD60C31B is an encoder/decoder for optical disk drives. The primary functions of this device are the conversion of Non-return to Zero (NRZ) data to Run Length Limited (RLL 2:7) data, the conversion of RLL 2:7 data to NRZ data, the detection of a variety of special identifying marks on the media, and the detection of data error conditions.

This device supports the "Continuous/Composite" data format as proposed to the American National Standards Institute (ANSI X3B11) committee.

1.1 FEATURES

- Supports ANSI X3B11 format (5.25-inch and 3.5-inch formats)
- Converts RLL (2:7) data to NRZ data
- Converts NRZ data to RLL (2:7) data
- Track formatting
- Provides variable threshold voting for data address mark detection
- Sector mark detection (5 3 3 7 3 3 3 5)
- Programmable rotational speed tolerance of ±.5 % and ±1%
- ID address mark detection and generation (16 code bits)
- Data address mark generation and detection (48 code bits)
- Variable threshold voting for data address mark detection
- Resync generation and detection (16 code bits)
- Programmable resync window size
- Supports extended recovery techniques
- Write Only RAM Memory (WORM) flag generation and detection
- WD10C00 interface support
- Supports three on-the-fly Identification (ID) voting
- Automatically increments ID track and sector
- Supports track streaming
- Provides extensive error status

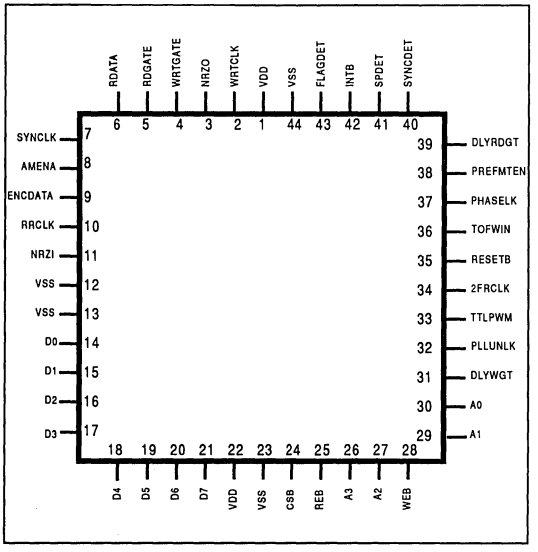

FIGURE 1-1. WD60C31B PIN DIAGRAM

1.2 PIN ASSIGNMENTS

The WD60C31B signals fall into four function groups:

- Disk controller interface (11 pins)
- Phase-locked loop (PLL) interface (11 pins)
- Microprocessor bus interface (17 pins)
- General support (5 pins)

Figure 1-1 is a pin diagram of the WD60C31B. Table 1-1 identifies each pin signal by number, and symbol. See Section 4.0 for a complete pin description.

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PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VDD	16	D2	31	DLYWGT
2	WRTCLK	17	D3	32	PLLUNLK
3	NRZ0	18	D4	33	TTLPWM
4	WRTGATE	19	D5	34	2FRCLK
5	RDGATE	20	D6	35	RESETB
6	RDATA	21	D7	36	TOFWIN
7	SYNCLK	22	VDD	37	PHASELK/PRDETB
8	AMENA	23	VSS	38	PREFMTEN
9	ENCDATA	24	CSB	39	DLYRDGT
10	RRCLK	25	REB	40	SYNCDET
11	NRZI	26	A3	41	SPDET
12	SEQOUT	27	A2	42	INTB
13	VSS	28	WEB	43	FLAGDET
14	D0	29	A1	44	VSS
15	D1	30	A0		

TABLE 1-1. WD60C31B PIN ASSIGNMENTS

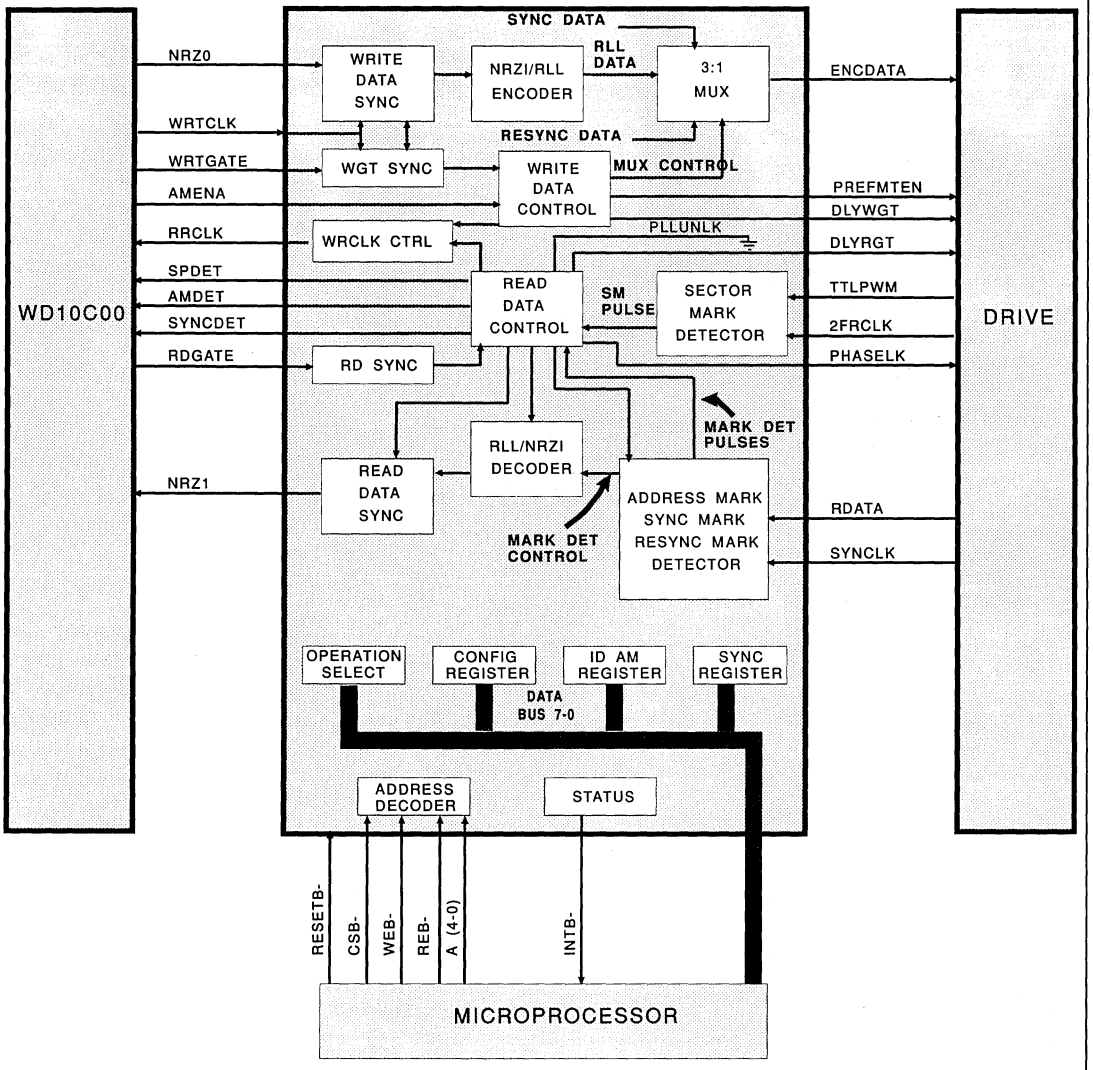

FIGURE 2-2. WD60C31B BLOCK DIAGRAM

2.0 WD60C31B ARCHITECTURE

As shown in Figure 2-1, the major functions within the WD60C31B are:

- Write data synchronization
- Write data encoding
- Write data control
- Read data synchronization
- Read data decoding
- Read data control
- Detection of address marks, sector marks, and sync and resync marks

The WD60C31B acts as a bridge between standard magnetic disk controller products and optical disk drive electronics. During write operations, the WD60C31B accepts serial NRZ data and modifies the code to create an RLL bit pattern for the optical drive. During read operations, the WD60C31B detects fields unique to the optical disk drive environment and by removing or inserting certain bit patterns it is able to decode RLL read data from the optical drive into NRZ serial data that can be handled by a standard magnetic disk controller such as the WD10C00.

The WD10C00 is a Very Large Scale Integration (VLSI), Winchester/optical disk controller device that provides data, status, and control signals for intelligent drive applications.

3.0 WD60C31B INTERFACES

3.1 DISK CONTROLLER INTERFACE

Serial NRZ data passes from the WD10C00 to the WD60C31B at a frequency of 15 Mbits/s along with the respective bit clock (WRCLK). Six control lines are associated with data transfer: three are generated by the disk controller (AMENA, WRTGATE, and RDGATE) and three are generated by the WD60C31B (SPDET, AMDET, and SYNCDET). The WD10C00 controls the direction and type of data transfer. The WD60C31B provides the proper NRZ data (along with its respective clock, RRCLK) to the WD10C00 and converts NRZ data from the WD10C00 to RLL data (ENCDATA) for the optical disk drive.

3.2 PLL INTERFACE

The phase-lock loop interface allows the WD60C31B to transfer serial RLL data to and from the optical dirve. This serial data, ENCDATA and RDATA, each are accompanied by their respective clocks, 2FRCLK and SYNCLK. TLPWM is unsynchronized serial data from the drive that is used to detect the optical media's sector mark. The PLL interface provides four control signals for the optical disk drive:

- Preformat Enable (PREFMTEN) controls the read channel gain.
- Delay Read Gate (DLYRGT) and Delay Write Gate (DLYWGT) are signals from the ADS10C00 that have been processed by the WD60C31B control circuitry.
- The Phase Lock (PHASELK) signal is an optional signal that can be used to change the gain of the phase-lock loop.

3.3 MICROPROCESSOR BUS INTERFACE

The WD60C31B has a generic microprocessor bus interface that allows it to be used with all popular 8-bit microprocessors. The microprocessor interface provides an 8-bit bidirectional data bus for the transfer of status, data and control signals to and from the WD60C31B. The read enable and write enable signals (REB, WEB) allow the microprocessor to access the internal registers selected by the address bus (A3 through A0). After requesting status information, the microprocessor receives an interrupt signal from the WD60C31B. This interrupt capability frees the microprocessor from constant polling of the WD60C31B. The master reset from the microprocessor resets all internal registers and tristates all outputs. The chip select (CSB) is the enable signal for the WD60C31B.

4.0 SIGNAL DESCRIPTION

PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
4	WRTGATE	Write Gate	I	A	Gates write data to the drive
3	NRZO	NRZ Data Input	I	A	NRZ serial data from the disk controller
2	WRTCLK	Write Clock	I	A	Write data input clock from disk controller (inversion of RRCLK)
11	NRZI	NRZ Data Output	O	B	NRZ serial data to disk controller
10	RRCLK	Read Clock	O	B	Multiplexed 2FRCLK / SYNCLK to disk controller
5	RDGATE	Read Gate	I	A	Enables read gate during a read operation
41	SPDET	Sector Pulse Detected	O	B	Indicates detection of a sector mark or the end of a SM window
40	SYNCDET	Sync Detected	O	B	Indicates detection of an address mark
43	FLAGDET	Flag/Gap Detected	O	B	Indicates detection of a flag field
8	AMENA	Address Mark Enable	I	A	Indicates the WD60C31 should write the Data Sync Mark
12	SEQOUT	Window Toggle	I	A	The WD10C00 indicates the location of the data field.

CKT TYP (Refer to Section 5.0 for more detail)
A = Input
B = Output

TABLE 4-1. DISK CONTROLLER INTERFACE

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PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
6	RDATA	Read data	I	A	Data from the PLL which is synchronized to 2XRCLK
7	SYNCLK	PLL clock	I	A	The PLL clock is derived from REFCLK during a write operation.
33	TTLPWM	Input data	I	A	Raw input from the heads
9	ENCDATA	Output data	O	B	Write data from the WD60C31B to the read/write heads
37	PHLK	PLL phase lock	O	B	Places PLL in phase mode
34	2FRCLK	Reference clock	I	A	PLL reference clock
31	DLYWGT	Delayed write gate	O	B	Buffered write gate to heads
39	DLYRDGT	Delayed read gate	O	B	Buffered read gate to PLL
36	TOFWIN	TOF window	O	B	Identifies the location of the mirror mark (1 or 2 byte times)
38	PREFMTEN	Preformat enable	O	B	Programmable signal which selects the gain of the read channel.
32	PLLUNLK	PLL unlock enable	I	C	Indicates when PLL is out of lock
CKT TYP (Refer to Section 5.0 for more detail) A = Input B = Output					

TABLE 4-2. PLL INTERFACE

PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
21-14	D7-D0	Data Bus	I/O	C	Eight-bit bidirectional data bus for transferring status, data and control of the WD60C31B
26, 27 29, 30	A3-A0	Address Bus	I	A	Nonmultiplexed address bus
25	REB	Read Enable	I	C	Read strobe for the internal registers in PIO
28	WEB	Write Enable	I	C	Write strobe for internal registers during PIO
24	CSB	Chip Select	I	A	Master chip enable for the WD60C31B
42	INTB	Interrupt Request	O	B	Output to microprocessor requesting a status transfer
35	RESETB	Master Reset	I	A	Master resets all internal

CKT TYP (Refer to Section 5.0 for more detail)
A = Input
B = Output
C = Bidirectional

TABLE 4-3. MICROPROCESSOR INTERFACE

PIN	NAME	SIGNAL	FUNCTION
1, 22	VDD	+5 Volts	Supply voltage
13, 23, 44	VSS	Ground	Digital ground

TABLE 4-4. GENERAL SUPPORT

5.0 ELECTRICAL SPECIFICATIONS

Non-operational:	
VDD	7.0V
Voltage with respect to VSS	-0.3V (minimum) +0.3V (maximum)
Storage temperature	-55°C to 150°C
Operational:	
VDD	5.0V ±0.5V
IDD (maximum)	150 mA at 30 MHz
Ambient temperature	0°C to 70°C

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Vih	High-level input voltage	2.0	V_{DD} +0.3	V	
Vil	Low-level input voltage	-0.3	0.8	V	
Vi	Input clamp voltage (low)	-0.5			
Ilh	Leakage current (high)	-10	+10	µA	$2.0 \leq Vi \leq V_{DD}$
Ill	Leakage current (low)	-10	+10	µA	$0.0 \leq Vi \leq 0.8$
Iluh	Latchup current (high)	-40		µA	
Ilul	Latchup current (low)		40	µA	
Note: Positive current is flow into the pin.					

TABLE 5-1. CIRCUIT A - OPERATING CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Ioh	High-level output current		-400	µA	Vo = 2.8V
Iol	Low-level output current	2.0		mA	Vo = 0.3V
Voh	High-level output voltage	2.8		V	Io = -400 µA
Vol	Low-level output voltage		0.3	V	Io = 2.0 mA
Iozh	Off state, high-level output current	-10	+10	µA	$2.0 \leq Vo \leq VDD$
Iozl	Off state, low-level output current	-10	+10	µA	$0.0 \leq Vo \leq 0.8V$

TABLE 5-2. CIRCUIT B - TRISTATE OUTPUT CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Ioh	High-level output current		-2.5	mA	Vo = 2.8V
Iol	Low-level output current	4.0		mA	Vo = 0.3V
Vih	High-level input voltage	2.4	VDD + 0.3	V	
Vil	Low-level input voltage	-0.3	0.8	V	
Vik	Input clamp voltage (low)		-0.5	V	
Voh	High-level output voltage	2.8		V	Ioh = -2.5 mA
Vol	Low-level output voltage		0.4	V	Iol = 6.0 mA
Iozh	Off state, high-level output current	-10	+10	µA	VCC = Maximum Vih = 2.8V
Iozl	Off state, low-level output current	-10	+10	µA	VCC = Maximum 0.0 ≤ Vo ≤ 0.8
Iluh	Latchup current (high)	-40		mA	
Ilul	Latchup current (low)		40	mA	
Iih	High-level input current	-10	+10	µA	VCC = Maximum Vih = 2.8V
Iil	Low-level input current	-10	+10	µA	VCC = Maximum Vil = .4V
Note: Positive current is current flow to the pin.					

TABLE 5-3. CIRCUIT C - BIDIRECTIONAL CHARACTERISTICS

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6.0 AC OPERATING CHARACTERISTICS

6.1 TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t1a	NRZO setup	10	
t1b	NRZO hold	10	
t1c	WRTCLK high	trlo-4.5	
t1d	WRTCLK low	trhi-4.5	
t1e	WRTCLK period	trp-4.5	
t2a	WRTGATE/RDGATE	10	
t2b	WRTGTE/RTGTE hold	10	
t3a	NRZI setup	trhi-4.5	
t3b	NRZI hold	trlo-4.5	
t4a	SYNCDET setup	trlo-4.5	
t4b	SYNCDET hold	trhi-4.5	
t5a	AMENA setup	10	
t5b	AMENA hold	10	
t6a	SPDET pulse width	2 x trp-4.5	
t6b	SPDET high delay	10	
t6c	SPDET low delay	10	
t7a	FLGDET pulse width	4 x trp-4.5	
t7b	FLGDET setup	trlo-4.5	
t7c	FLGDET hold	trhi-4.5	
t8a	Clock high	13	
t8b	Clock low	13	
t8c	Clock period	tclk	
t9a	RDATA setup	7	
t9b	RDATA hold	7	
t10a	DLYRGT low delay	12	40
t10b	DLYRGT high delay	12	40
t10c	PHASELK low delay	12	40
t10d	DLYRGT to PHASELK	0-63 2FRCLK	
t11a	ENCDATA low delay	12	25

TABLE 6-1. DISK CONTROLLER AND PLL TIMING

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t11b	ENCDATA high delay	12	25
t12a	PREFMTEN low delay	12	30
t13a	TOFWIN high delay	12	30
t13b	TOFWIN low delay	12	30
t13c	TOFWIN pulse width	0-15 2FRCLK	

Note: Unless otherwise specified, all time units are in nanoseconds.
trhi = clock high for the RRCLK output
trlo = clock low for the RRCLK output
trp = clock period of the RRCLK output
tclk = 2FRCLK clock input

TABLE 6-1. DISK CONTROLLER AND PLL TIMING (Continued)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t14a	Address valid to REB	20	
t14b	REB high to address change	0	
t14c	REB false to CSB false	0	
t14d	REB pusle width	100	
t14e	REB true to data valid		80
t14f	REB false to data hold	10	
t15a	Address valid to WEB true	20	
t15b	WEB high to address change	0	
t15c	WEB pulse width	100	
t15d	Data setup to WEB false	80	
t15e	WEB false to data hold	00	
t15f	WEB false output change		80
t15g	WEB false to CSB false	10	

TABLE 6-2. MICROPROCESSOR TIMING

6.2 DISK CONTROLLER TIMING

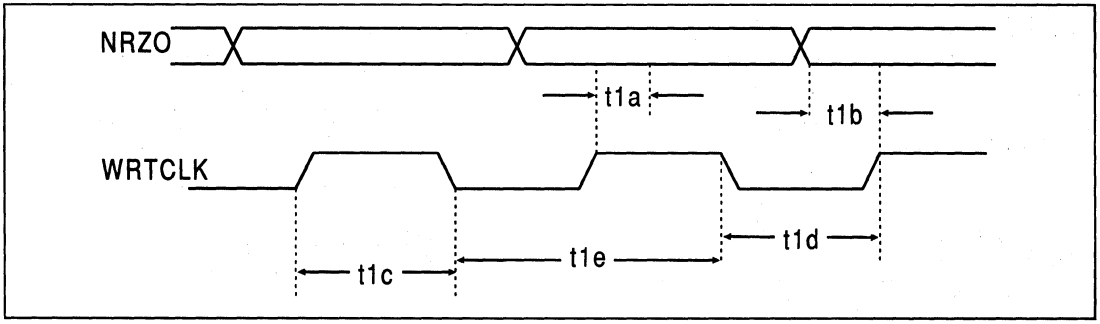

FIGURE 6-1. DISK CONTROLLER TIMING (NRZ0 TO WRTCLK)

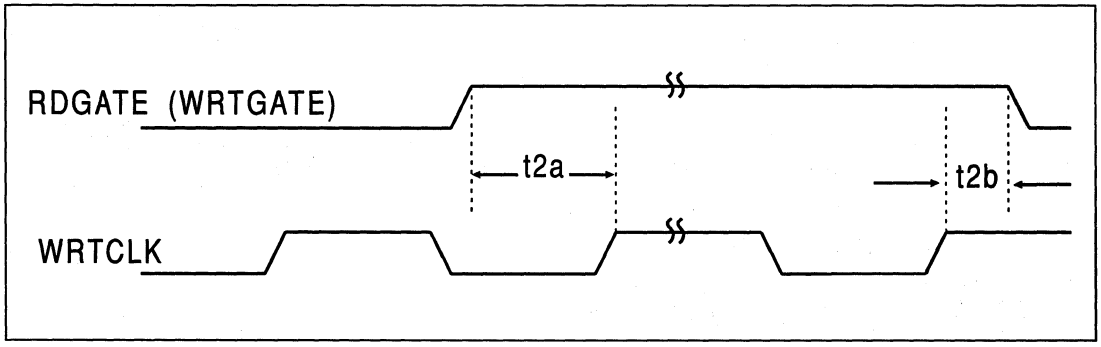

FIGURE 6-2. DISK CONTROLLER TIMING (WRTGATE/RDGATE)

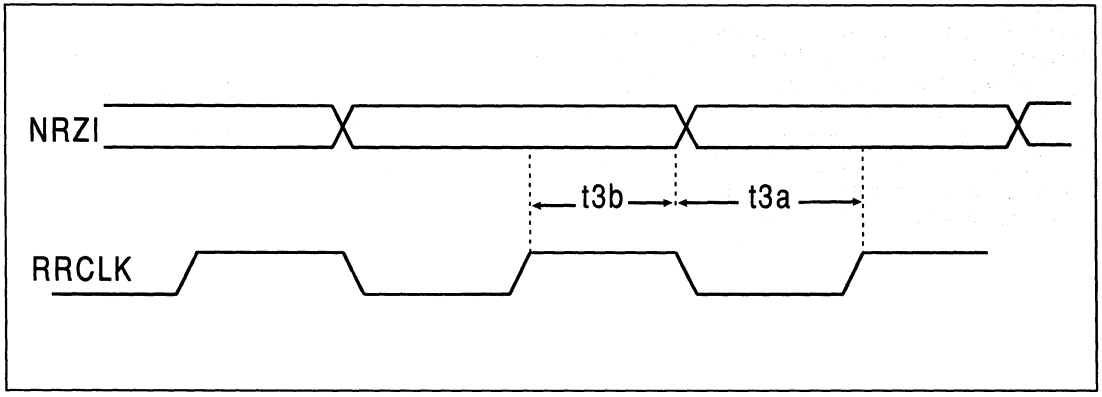

FIGURE 6-3. DISK CONTROLLER TIMING (NRZI TO RRCLK)

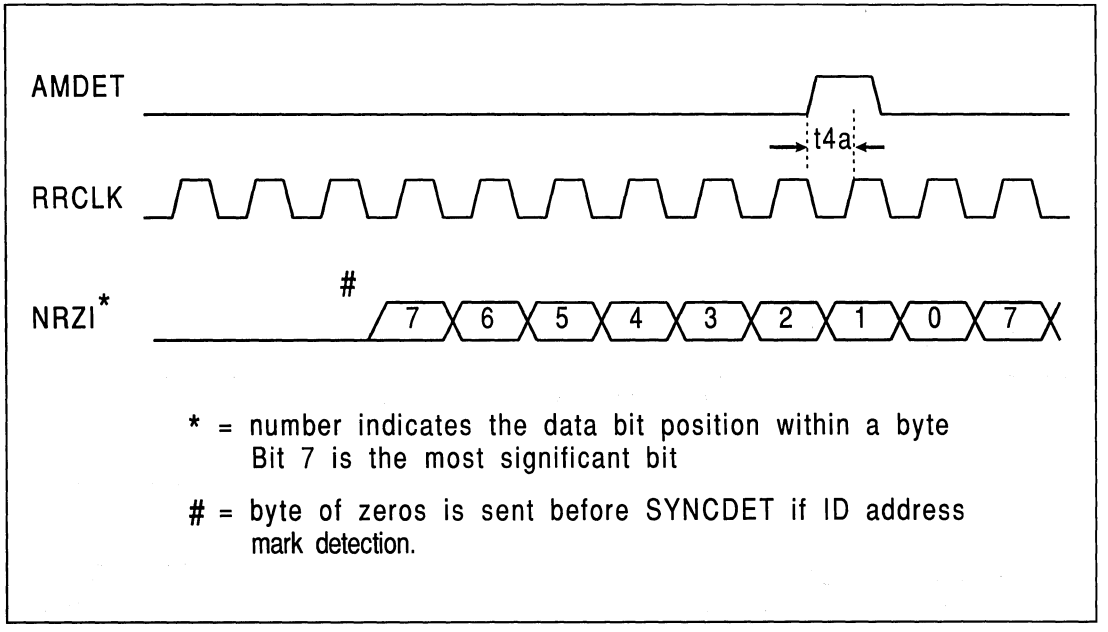

FIGURE 6-4. DISK CONTROLLER TIMING (SYNCDET)

NOTE

Sync Detected (SYNCDET) is generated whenever RDGATE is active and either the ID Address Mark (ID AM) or the Data Address Mark is detected. Whenever an ID Address Mark is detected, the SYNCDET is sent concurrently with the first byte of the 5-byte ID Address field. The 5-byte ID field is preceded by a NRZI byte of zeroes. During ID search, the SYNCDET is sent concurrently with this byte of zeroes. Whenever a Data Address Mark is detected, the SYNCDET is sent one byte before the first byte of the data field. A full byte of zeros is sent concurrently with the SYNCDET. This byte of zeros is handled in the WD10C00 as an address mark. SYNCDET, once active, remains active until RDGATE is dropped.

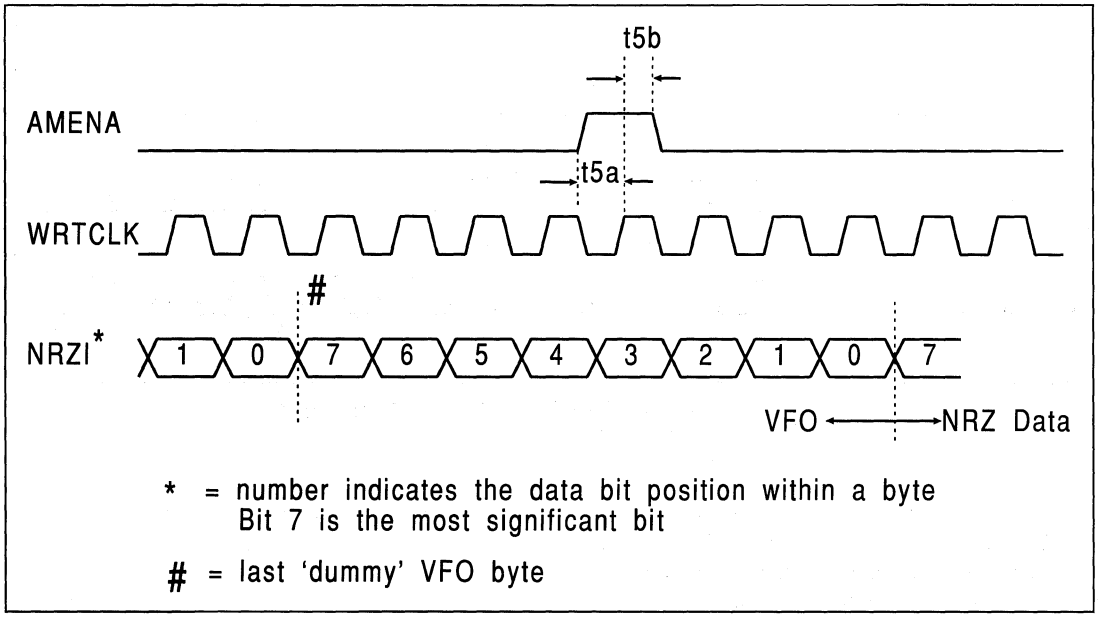

FIGURE 6-5. DISK CONTROLLER TIMING (AMENA)

NOTE

The data field of an optical drive contains four unique types of information. They are : 1) the VFO field, 2) the Data Address Mark, 3) the encoded user data, and 4) the Resync Marks. The WD10C00 and the WD60C31B share the responsibility of defining the type and quantity of information to be written on the media. In the case of the VFO field, the WD10C00 specifies the size of the VFO field, and the WD60C31B creates the unique high-frequency pattern. First, the WD10C00 raises WRTGATE. Then an NRZ data pattern of 1's is sent to the WD60C31B. This specifies the beginning of the VFO field. The WD60C31B writes a fixed RLL pattern on the disk. The WD10C00 must indicate the end of the VFO field. This is performed by sending the Address Mark Enable (AMENA) signal during the last byte. This signal initiates the writing of the previously programmed Data Address Mark (3 bytes). The WD60C31B then encodes the incoming NRZ data from the WD10C00 and injects the Data Resync Mark, another previously programmed pattern, into the encoded write data path. This operation continues for as long as WRTGATE is active or the end of sector is detected.

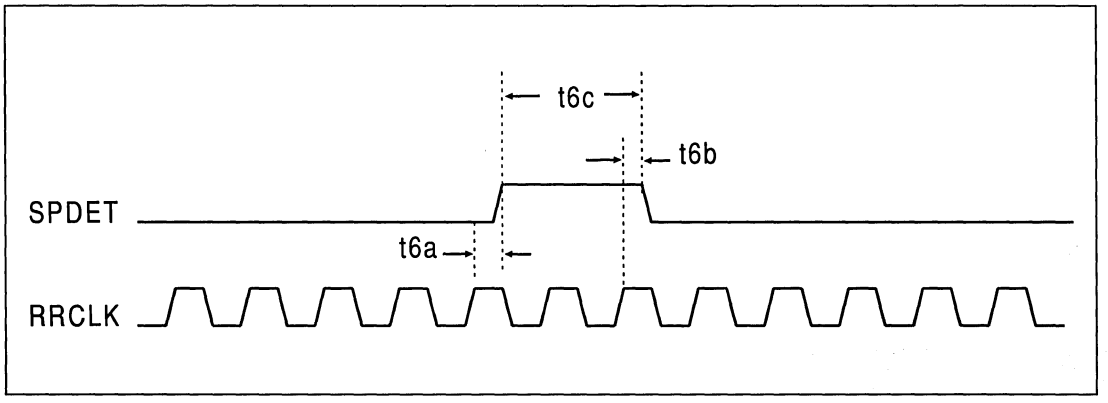

FIGURE 6-6. DISK CONTROLLER TIMING (SPDET)

NOTE

The Sector Pulse Detection (SPDET) signal occurs whenever a sector mark is detected. A SPDET also occurs whenever a sector mark has not been detected by a defined time. (One sector period plus 6 byte times.)

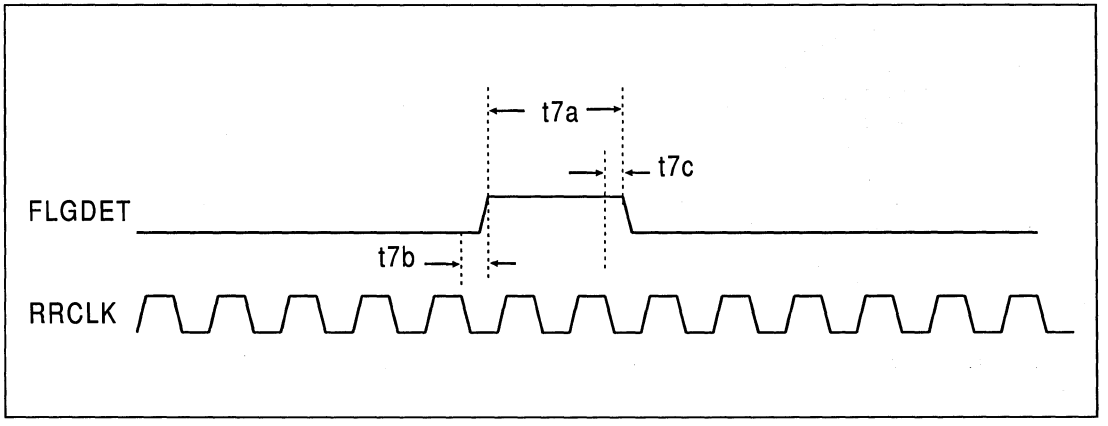

FIGURE 6-7. DISK CONTROLLER TIMING (FLGDET)

NOTE

A Flag Detect (FLGDET) pulse occurs if RDGATE is active and 1-1/2 bytes of the Flag pattern (high frequency '100') is detected.

6.3 PLL TIMING

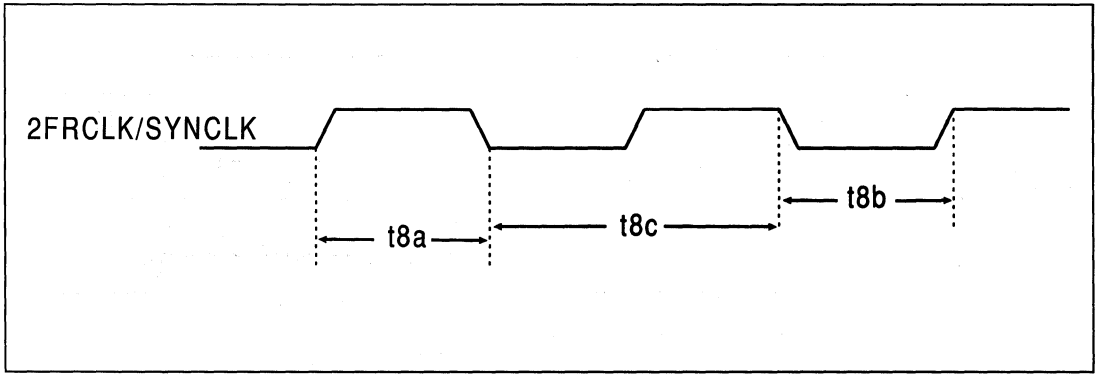

FIGURE 6-8. PLL TIMING (2FRCLK/SYNCLK)

NOTE

Both clocks must be glitch-free. The PLL must deliver a clock which does not violate the above timing. The is especially true of the SYNCLK which changes between the reference clock and the internally generated PLL clock when Read Gate is applied.

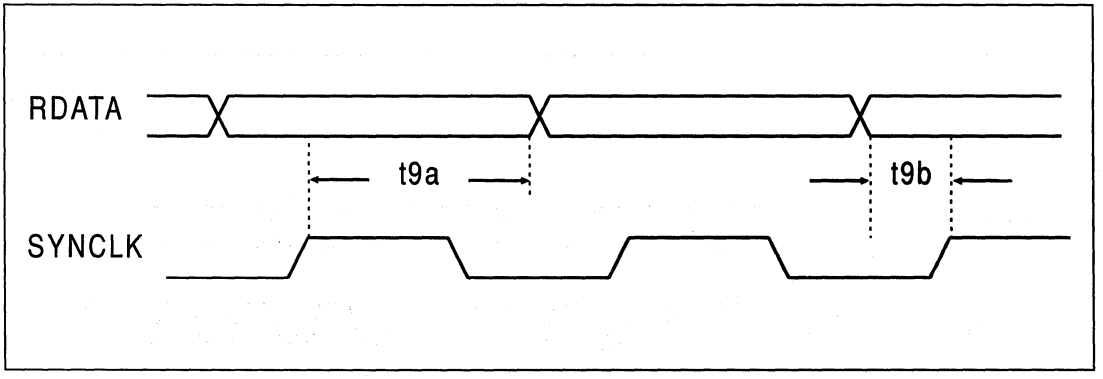

FIGURE 6-9. PLL TIMING (NRZI TO RRCLK)

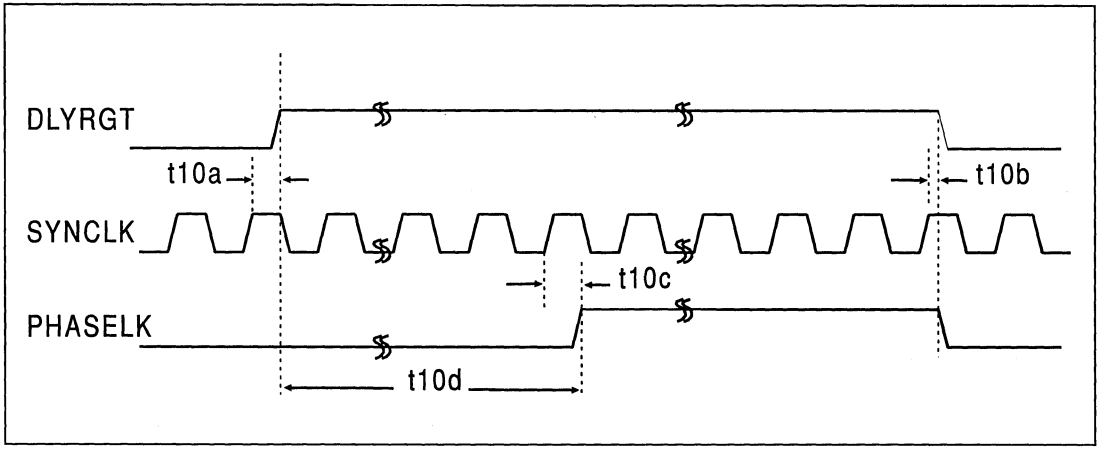

FIGURE 6-10. PLL TIMING (DLYRGT/PHASELK)

NOTE

The PHASELK signal controls the PLL modes. Whenever PHASELK is low, the PLL should be in high gain (or phase/frequency mode). Whenever PHASELK is high, the PLL should be in low gain (or phase mode). There is a delay of 1 to 64 SYNCLKs (+/-1 SYNCLK) from DLYRGT to PHASELK.

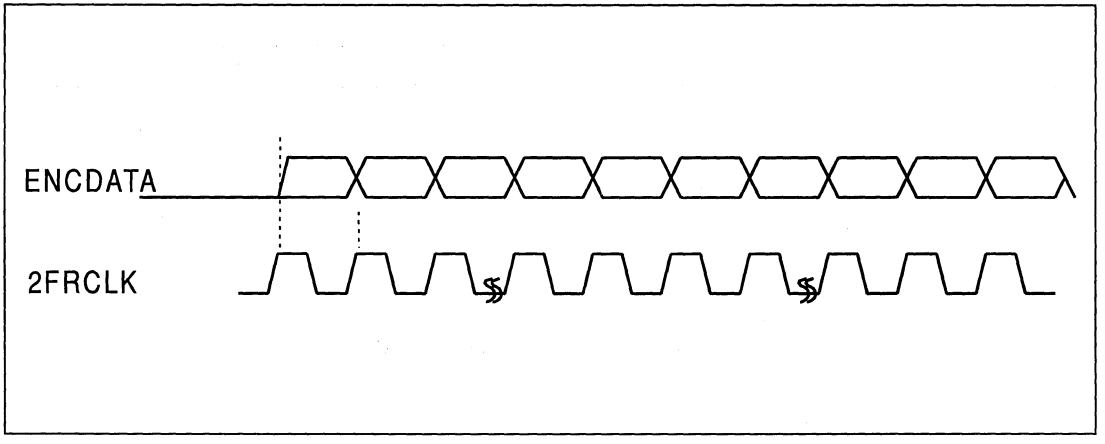

FIGURE 6-11. PLL TIMING (ENCDATA)

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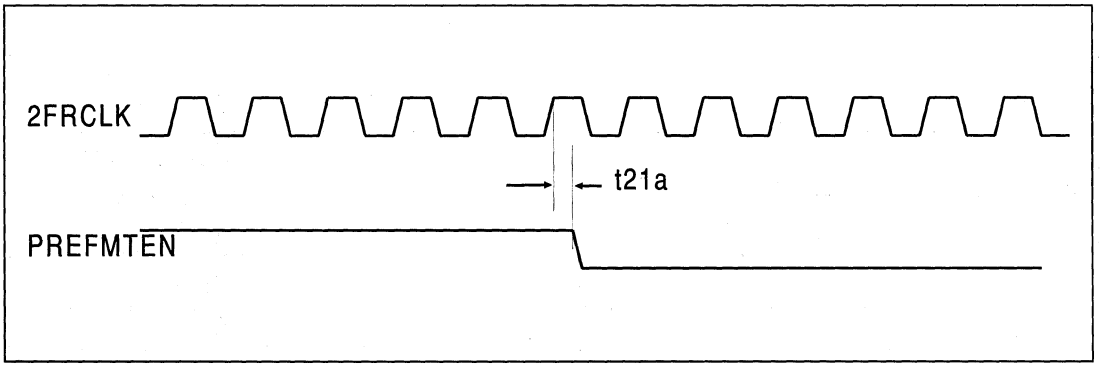

FIGURE 6-12. PLL TIMING (PREFMTEN)

NOTE

When enabled by the microprocessor, the Preformat Enable signal (PREFMTEN) acts as a read channel control line. This signal occurs whenever the drive is expecting to read the preformatted data (ID fields). This signal is continuously high for WORM drive applications. This signal, when enabled, is low 47 bytes after SPDET.

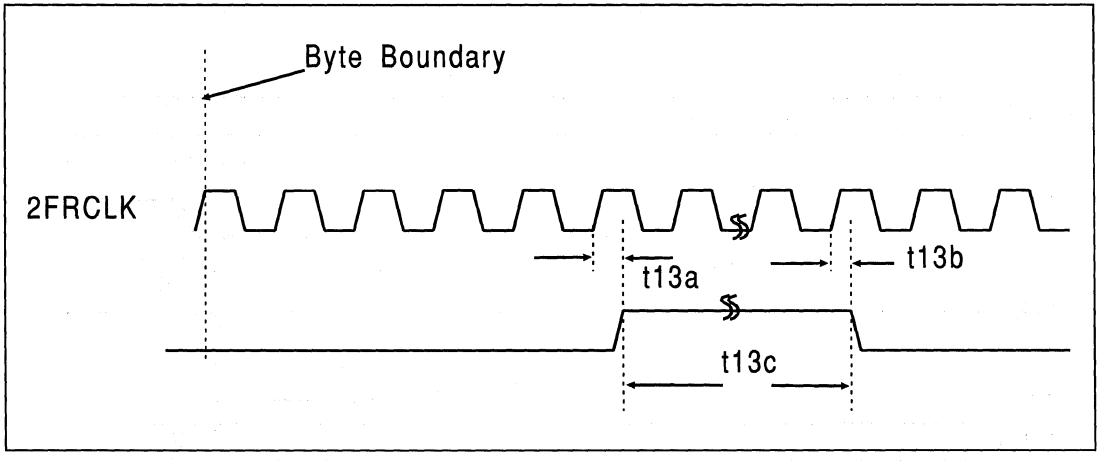

FIGURE 6-13. PLL TIMING (TOFWIN)

NOTE

The TOFWIN signal is used in optical servo systems which utilize the Mirror Mark / TOF Mark for servo alignment. TOFWIN is active 47 bytes after sector mark. This signal is active only if a sector mark is detected.

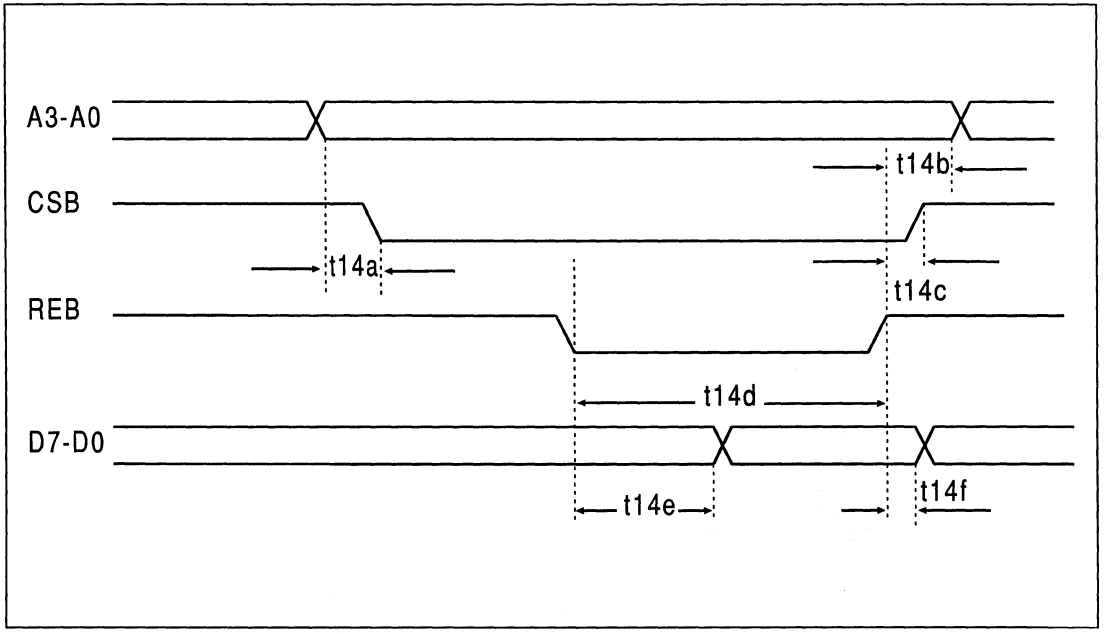

FIGURE 6-14. MICROPROCESSOR READ TIMING

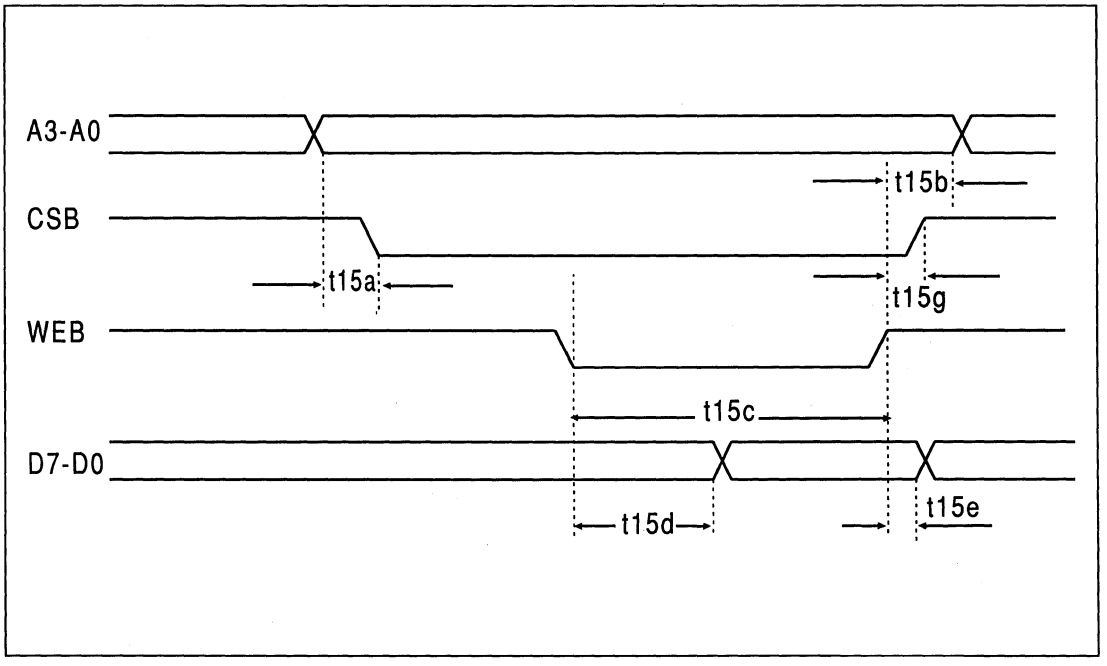

FIGURE 6-15. MICROPROCESSOR WRITE TIMING

7.0 REGISTERS

The WD60C31B has 21 read/write locations.

ADDRESS	WRITE FUNCTION	READ FUNCTION
X'0'	Configuration write	Configuration read
X'1'	Software reset	Operation error status
X'2'	Data resync MSB byte	Data resync MSB byte
X'3'	Data resync LSB byte	Data resync LSB byte
X'4'	ID address mark MSB byte	ID address mark MSB byte
X'5'	ID address mark LSB byte	ID address mark LSB byte
X'6'	Data sync bytes (6 bytes)	Pointer counter status
X'7'	Sync threshold/TOF size	Sync threshold/TOF size
X'8'	Data size/RESYNC limit	Data size/RESYNC error flag
X'9'	Data sync pointer reset	Future ID track/sector (3 bytes)
X'A'	Phase lock delay	Phase lock delay
X'B'	Secondary configuration	Secondary configuration
X'C'	Third configurtion	Third configuration
X'D'	ID preset track/sector (3 bytes)	ID preset track/sector (3 bytes)
X'E'	ID control	ID status (3 bytes)
X'F'	Sector/track	Sector/track

TABLE 7-1. REGISTER ADDRESS ASSIGNMENTS

7.1 CONFIGURATION READ/WRITE REGISTER: ADDRESS X'0'

7	6	5	4	3	2	1	0
FF	ID	SS	IE	WT	PE	M1	M0

FF= Enable Flag Field Detection
(Active state = 1)

This bit enables the flag detection logic. Eight rising edges of TTLPWM during an internally created flag window indicates a flag detection, and FLGDET goes active. In addition, all write operations are disabled until the next sector mark if a flag is detected. An interrupt is also generated if Bit 4 of this register is set.

ID = Enable ID Search Mode
(Active state = 1)

Normally, during a read opertion, the WD60C31B sends an AMDET (in the Bit 1 position) with the first byte of decoded RLL data after an ID address mark is detected. If the controller is trying to read the ID field, the concurrent byte is the Track High Byte. The WD10C00 uses the Track High Byte as an Address Mark byte and stores only the subsequent NRZI bytes in its internal register. If the Track High bytes do not match, the WD10C00 does not store the subsequent ID field. The programmer can activate this bit and perform another ID read operation. The WD60C31B moves the AMDET forward by eight RRCLKs and sends a byte of zeroes. The WD10C00 is then programmed to wait for SYNCDET and expect an Address Mark byte of zeros. This means that the WD10C00 will store the Track High Byte internally along with the subsequent bytes. This mode is

SS	SE35	IDW	BYTES/SECTOR	MODE DEFINITION
0	0	0	746	5.25" - 512 bytes
1	0	0	1360	5.25" - 1024 bytes
0	1	0	725	3.5" - 512 bytes
1	1	0	1394	3.5" - 1024 bytes
0	0	1	746	Auxilliary mode - 512
1	0	1	1360	Auxilliary mode - 1024

TABLE 7-2. SELECTION OF SECTOR SIZE

normally used after a seek operation to determine the head position.

SS = Select Sector Size
(Active state = 1)

When this bit is active, a sector size of 1024 data bytes is selected. When inactive, a sector size of 512 data bytes is selected. The Secondary Configuration Register further defines the total number of bytes per sector. Refer to Table 7-2.

IE = Enable Interrrupt
(Active state = 1)

This is the Master Interrupt Enable bit. An interrupt occurs as a result of any of the following conditions:

- Data Read Complete
  At the end of each data field read operation an interrupt is generated if interrupts are enabled and Bit 5 of of the ID Control/Status Register is set.
- Flag Field/WRTGATE Error
  This bit is set if a flag field is detected and a write operation is attempted in this sector. An interrupt is possible if Bit 7 of this register is set.
- Pseudo SPDET/WRTGATE Error
  This bit is set if a pseudo SPDET is generated and a write operation is attempted. An interrupt is generated if Bit 0 of the Third Configuration Register and Bit 4 of this register are set.
- Resync Threshold Exceeded Error
  If the programmed missing RESYNC counter equals or exceeds the programmed limit, this bit is set. An interrupt is generated if Bit 4 of the ID Control/Status Register and Bit 4 of this register are set.
- RDGATE/SPDET Error
  This bit is set if RDGATE is applied and a SPDET is generated. An interrupt is generated if Bit 4 of the Secondary Configuration Register and Bit 4 of this register are set.
- ID Miscompare Error
  If the on-the-fly ID detection logic is unable to meet the programmed ID threshold, an interrupt is generated concurrent to the transfer of an invalid ID AM byte transfer on the NRZI pin. Bit 4 of this register must be set.
- Read Stop Interrupt
  This bit is set when RDGATE is applied after the next SPDET. An interrupt is generated if Bit 7 of the Sector per Track Register and Bit 4 of this register are set.

WT = Internal Test Mode

This is used for IC testing purposes only.

PE = Preformat Enable Control

When set, this permits the PREFMTEN signal to go low 47 bytes after the sector mark. This is used in erasable media applications.

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M1,M0 = Select Data Recovery Mode

M1	M0	MODE
0	0	Normal data tranasfer
0	1	**Recovery Mode 1: Disable Data Sync Detection** During a data field read, a fixed number of data segments are sent as soon as read gate is active without waiting to detect the Data Sync Mark first. This mode is selected when the Sync Mark can't be detected, regardless of the Sync threshold. The number of data segments are determined by the Third Configuration Register.
1	0	**Recovery Mode 2: Invalid Code Bit Map with sync** The NRZ Data that is sent to the ADS10C00 is not the decoded RLL data. Instead, it is a map of the invalid RLL code bit of the data stream. An NRZI Bit 1 indicates an RLL violation.
1	1	**Recovery Mode 3: Invalid Code Bit Map with resync** This mode performs both RLL code violation mapping (Mode 2) and disabling of Data Sync detection (Mode 1).

The following interrupt functions have individual enables. In order for these interrupt functions to be enabled, both the general enable (Bit 4 of the Primary Configuration Register) and the specified enable must be set:

FUNCTION	INTERRUPT ENABLE
Data Read Complete	ID Control Status Register (Bit 5)
Resync Threshold Exceed Error	ID Control/Status Register (Bit 4)
RDGATE/ SPDET Error	Third Configuration Register (Bit 3)
ID Miscompare Error	ID control/Status Register (Bit 6)

The following functions do not have individual interrupt masks. The only individual control possible is to disable the function:

FUNCTION	FUNCTION ENABLE
Flag Field/ WRTGATE Error	Primary Configuration (Bit 7)
Pseudo SPDET/ WRTGATE Error	Third Configuration Register (Bit 0)
Read Stop Interrupt	Sector per Track Register (Bit 7)

7.2 SOFTWARE RESET/OPERATION ERROR STATUS: ADDRESS X'1'

Write:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

X = not applicable

The following status flags are reset when writing to Address X'1':

- Flag Detect Error Flag
- Read Complete Flag
- Pseudo Sector Mark Error Flag
- Resync Threshold Error Flag
- Missing Resync Error Flag
- RDGATE/SPDET Error Flag
- ID Miscompare Error Flag
- Read Stop Error Flag

Read:

7	6	5	4	3	2	1	0
IV	RDC	FLE	SE	IP	TE	RS	RD

Whenever Address X'1' is read, the following status flags are cleared and reinitialized.

IV = Invalid RLL Code Detected

RDC = Read Complete
(Active state = 1)

The RDC bit is set upon finishing a data field read operation. This bit is cleared at the end of each sector or if the programmer writes to Address 1. Enabling this bit and Bit 5 of the ID Control/Status Register generates an interrupt.

FLE = Flag Detect Error
(Active state = 1)

The FLE bit is set if the flag detection logic has been enabled, a flag has been detected, and WRTGATE is active. An interrupt is also generated if Bit 0 of the Primary Configuration Register is set. The FLE bit is cleared when the programmer writes to Address 1.

SE = Pseudo Sector Mark Error
(Active state = 1)

The SE bit is set when a Sector Mark is not detected, a pseudo SPDET is generated and WRTGATE is active for a given sector. An interrupt is also generated if Bit 0 of the Third Configuration Register is set. Writing to Address 1 clears the SE bit.

IP = Interrupt Pending
(Active state = 1)

TE = Resync Threshold Exceeded
(Active state = 1)

The number of missing resyncs as defined in the Resync Error Threshold Register has been equaled or exceeded in a single sector data field read. An interrupt is generated if TE is enabled and Bit 4 of the ID Control/Status Register is set. TE is cleared when the programmer writes to Address 1.

RS = Missing RESYNC Field Detected
(Active state = 1)

This bit indicates that at least one Resync byte has been missed. The RS bit is cleared by writing to Address 1.

RD = RDGATE/SPDET Error
(Active state = 1)

Read Gate is active when SPDET becomes active. This error flag generates an interrupt if enabled and Bit 3 of the Third Configuration Register is set.

7.3 RESYNC MOST SIGNIFICANT BYTE (MSB): ADDRESS X'2'

Write/read :

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

This register stores the Resync MSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the Resync mark within the RLL bit stream.

7.4 RESYNC LEAST SIGNIFICANT BYTE (LSB): ADDRESS X'3'

Write/read :

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This register stores the Resync LSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the Resync mark within the RLL bit stream.

7.5 ID ADDRESS MARK MSB: ADDRESS X'4'

Write/read:

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

The user programs the IDAM MSB by writing to this register.

7.6 ID ADDRESS MARK LSB: ADDRESS X'5'

Write/read:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The user programs the IDAM LSB by writing to this register.

7.7 DATA SYNC BYTES (6): ADDRESS X'6'

Write:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The microprocessor must write 6 bytes to fully program the data sync field value. The first byte must be the LSB. After each write to this location a counter is incremented. The counter value can be viewed by reading this location. It is important to maintain 2FRCLKs during the writing of this register. The 2FRCLKs should maintain the minimum pulse widths as defined in Section 6.3.

Read :

7	6	5	4	3	2	1	0
RSE	FID1	FID0	PID1	PID0	C4	C2	C1

RSE = Read Stop Interrupt

This bit is set at the next SPDET. RDGATE is blocked to the internal device; DLYRDGT is blocked to the drive electronics.

FID1 through FID0 = Future ID Pointer

This counter is incremented whenever the user reads the Data Sync Pointer/Future ID (Address = X'9'). The next expected Track High, Track Low, and Sector bytes must be read serially from this location. The programmer resets these bits when he writes to Address X'9'.

PID1 through PID0 = Present ID Pointer

This counter is incremented whenever the user r eads the ID Compare Preset Register (Address = X'D'). Writing to Address X'9' resets these bits.

C2 through C0 = Data Sync Counter

Number of bytes written to Data Sync register. This value is reset on soft reset (Address = X'9').

7.8 SYNC THRESHOLD/TOF SIZE: ADDRESS X'7'

Write/read:

7	6	5	4	3	2	1	0
T3	T2	T1	T0	M3	M2	M1	M0

T3 through T0: TOF window size (increment = one 2FRCLK)

M3 through M0: Sync Field Majority vote trigger point (Value range = 0 > 12 base 10)

The user sets the percentage of the Sync Mark that must be found before an AMDET is generated in the Data field. Each incremental value changes the correlation percentage by 8.33%.

7.9 RESYNC ERROR THRESHOLD/ DATA SEGMENT SIZE: ADDRESS X'8'

Write/read:

7	6	5	4	3	2	1	0
DS16	DS8	DS4	DS2	DS1	TD4	TD2	TD1

DS16 through DS1 = Data Segment length
Value range = 0 through 31 base 10

This field sets the quantity of data bytes between RESYNCS within the data field. The present formats define this field to be 14_{10} or 19_{10}. (DS16-DS1 = # of byte between resyncs minus 1)

TD4 through TD1 = Resync Error Threshold
Value range = 1 through 7, base 10

This field determines the number of resyncs that are detected within a single sector. When this value is reached or exceeded, the Resync Error Flag in the Status Register is set.

7.10 DATA SYNC POINTER RESET: ADDRESS X'9'

Write :

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Writing to this address location resets all internal pointers which are used for multiple write operation. The pointers that are affected are the Data Sync Write Pointer, Present ID Write/Read Pointers, and Future ID Read Pointer. The Data Sync Pointer selects which register is to be written when writing to location '06'. The Present ID Write/Read Pointers are two independent counters which determine the location of the initial ID compare values. The Future ID Read Pointer identifies which byte of the expected ID counter is being read. The 2FRCLK should be operating at this time.

Read:

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

If the autoincrement functions are enabled, the WD60C31B can perform ID compare operations for ID field bytes other than the original bytes. The user reads the internal counter which predicts the next ID field to be verified. To read all three bytes (Sector byte, Track Low byte, and Track High) the user must perform repeated reads of this location. The byte that is read is identified in the Data Sync Status Register (Address X'9').

7.11 PHASE LOCK DELAY: ADDRESS X'A'

Write/read:

7	6	5	4	3	2	1	0
FS	IDS	P5	P4	P3	P2	P1	P0

FS = Flag Window Select

This bit defines the placement of the internal flag window for flag field detection. The flag window, nominally 6 bytes, is placed with reference to the last ID read. This bit is "0" if the last ID read is predicted to be ID number 3. This bit is "1" if the last ID read is predicted to be ID number 2. During the ID read operation, the WD10C00 should generate an AMENA during the last byte of the last ID that is read, normally the second CRC byte. Generally, the AMENA should not be generated unless the ID field passes a bit for bit comparison. The WD60C31B then delays the appropriate number of byte times and opens the flag window.

IDS = ID Window Enable
(Active state = 1)

When active, the detection of the ID Address Marks is limited to three small windows, ± eight 2FRCLKs. This reduces the probability of false ID AM detection.

P5 through P0 = Programmable Phase Lock Delay from DLYRGT (Value range = 0 through 63)

The user can set the time difference between the Delayed Read Gate and the PHASELK output signal.

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7.12 SECONDARY CONFIGURATION: ADDRESS X'B'

Write/read:

7	6	5	4	3	2	1	0
FMT	SE35	IDW	XX	RGH	SP0	RS1	RS0

FMT = Format Enable
(Active state = 1)

If active, the WD60C31B is set for a format track mode when WRTGATE is received.

SE35 = Media Select
(Active state = 1)

When active, the WD60C31B sets the internal operation for 3.5-inch, ANSI continuous composite format sector sizes.

IDW = Disable Internal ID and Data Window Generator (Active State = 1)

Normally, the WD60C31B generates internal windows for predicting the location of the ID and data fields. When this bit is active, the internal window generator for ID and data is defeated. Instead, the WD60C31B relies on an external signal, SEQOUT from the WD10C00. SEQOUT, along with RDGATE, selects the type of field the WD60C31B is expecting to read. (The default sector size is 746 and 1360 bytes). A typical situation is as follows: The WD10C00 waits for a SPDET and then raises a read gate. The WD60C31B searches for an address mark. The WD60C31B then sends the ID field to the WD10C00. When the WD10C00 finds the appropriate number of IDs, read gate is dropped. SEQOUT is sent to the WD60C31B to identify the next read operation as a search for a data sync mark. This feature is primarily used with soft-sectored media.

RGH = Read Gate Hold
(Active state = 1)

When active, the DLYRGT signal is extended to the read channel by nine RRCLKs. This occurs only if READGATE is raised and lowered in the ID field. This is useful when maintaining the PLL phase mode between consecutive ID fields. The Read Gate signal from the WD10C00 must be dropped after each ID field.

SP0 = Speed Tolerance Selection
(5.25-inch only)

The programmer sets the expected spindle motor tolerance. This tolerance changes sector mark detection windows. When this bit is 0, the sector mark window is set for a .5% speed tolerance. When this bit is 1, the window is set to a 1% speed tolerance.

RS1	RS0	MODE
0	0	Fixed Window - 12 clocks, .5% speed tolerance
0	1	Fixed Window - 18 clocks, 1% speed tolerance
1	0	Progressive Windows - The resync window is initially set to a minimum value (six 2FRCLKs). If a resync is not found, the resync window is increased by four clocks for each resync that is not found.
1	1	Progressive Windows - The resync window is initially set to a minimum value (eight 2FRCLKs). Window increases by eight clocks for each resync that is not found. Maximum window = 24 clocks.

7.13 THIRD CONFIGURATION: ADDRESS X'C'

Write/read:

7	6	5	4	3	2	1	0
ID1	ID0	SMS	T4	RDI	DCI	DC0	SME

ID1,0 = ID Status Select Bits

These bits select which status byte of four possible bytes to read from Address E.

ID1	ID0	
0	0	Control Register
0	1	ID Error Status
1	0	Present ID/Data Sync Read
1	1	Reserved

SMS = Small SYNCDET Enable (Active State = 1)

When enabled, this bit reduces the size of the SYNCDET to one NRZI bit. Normally, the SYNCDET signal is set during Bit 1 of the Address Mark byte and remains set until RDGATE is dropped. If this mode is enabled, the SYNCDET is only a pulse. During the reading of the ID fields, the RDGATE can remain on throughout all the ID fields. The SYNCDET is raised for each ID address Mark that is found. However, in both cases RDGATE must be dropped before reading the data field.

T4 = TOFWIN Window Size MSB (Active state = 1)

This bit is used in conjunction with T3 through T0 of the Sync Threshold/Size register. This bit extends the size of TOFWIN byte from 0 to 31 2FRCLKs. This is the MSB of the count value.

RDI = Read Gate/SPDET Interrupt Mask (Active state = 1)

When this bit is set, an interrupt is generated if RDGATE is active when the SPDET is sent.

DC1,0 = Data Segment Transfer Count (used in Mode 2 and Mode 3 operations)

If a Data Sync is not detected for a given minimum threshold, the programmer can select a Resync as the synchronization mark for the data field. DC1 and DC0 define the quantity of data segments that are sent to the WD10C00 before the Resync detection logic is enabled. A data segment is the quantity of data bytes between Resync marks as defined in the Rsync Error Threshold/Data Segment Size Register, Address X'8'.

DC1	DC0	DATA SEGMENTS
0	0	1
0	1	2
1	0	3
1	1	4

SME = Pseudo Sector Mark Error Enable (Active state = 1)

When active, a pseudo sector mark error flag is set and an interrupt is generated (if Bit 4 of the Primary Configuration is set). This error occurs if a sector mark is not detected, an SMDET is generated due to a timeout, and a write operation is attempted. In addition, the DLYWGT signal is disabled to the drive.

7.14 ID COMPARE PRESET REGISTER: ADDRESS X'D'

Write/read:

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

The microprocessor loads the ID field with the Sector byte, Track Low byte, and Track High byte which is used during the ID on-the-fly comparison. The Sector byte must be loaded first, then Track Low and Track High. Repeated reads are necessary to obtain these three values. The ID Status Register, Address E, contains a value that identifies which value is being read.

7.15 ID CONTROL/STATUS REGISTER: ADDRESS X'E'

Write:

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

3ID = 3 ID Enable
(Active state = 1)

When this bit is set, the special 3 ID on-the-fly mode is enabled. In this mode the WD60C31B reads the IDs for the WD10C00 and relays this information to the WD10C00.

IDE = ID Error Interrupt Enable
(Active state = 1)

When this bit is set, an interrupt is generated whenever the ID Compare is completed and an error is detected.

RCM = Read Complete Interrupt Mask
(Active state = 1)

When this bit is set, an interrupt is generated whenever the end of a data field read operation is reached.

REM = Resync Threshold Error Interrupt Mask
(Active state = 1)

When this bit is set, an interrupt is generated whenever the Resync Error Counter is activated.

TAE = Track Autoincrement Enable
(Active state = 1)

When this bit is active the Track High and Track Low bytes can be incremented whenever the maximum sector is detected and the last ID comparison is good.

SAE = Sector Autoincrement Enable
(Active state = 1)

When this bit is active, the expected sector value can be incremented after a good ID comparison.

IT1,0 = ID Compare Threshold Bits

These bits define the quantity of good ID field(s) which must be detected before the WD60C31B flags the WD10C00 of a good operation. IT1 is the MSB.

IT1	IT0	Good IDS Detected
0	0	Not valid
0	1	1
1	0	2
1	1	3

Read:

This address location can contain three possible status bytes. The Third Configuration Register, ID1 (Bit 7) and ID0 (Bit 6) determine which is status byte is to be read.

Control Register (ID1 = 0, ID0 = 0)

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

ID Compare Error Status (ID1 = 0, ID0 = 1)

7	6	5	4	3	2	1	0
SP	C3	C2	C1	I3	I2	I1	ICE

SP = Pseudo Sector Mark Detect
(Active state = 1)

When active, no sector mark is detected within the internal sector mark wihdow. A pseudo SPDET is generated. This bit is cleared when an authentic sector mark is detected.

C3 through C1 = ID Cyclic Redundancy Check (CRC) Error

These error bits occur under the following conditions: ID AM is detected, ID Track and sector bytes are compared and a CRC fault exists. C3 is status for the Third ID; C2 for the second ID.

I3 through I1 = ID AM and ID Field Match

These status bits are active whenever an ID AM is found and the ID field track and sector bytes match. The ID Threshold limit set in the ID Control Register determines the validity of this status.

ICE = ID Compare Error
(Active state = 1)

This bit is set whenever the ID Threshold (set by the Control Register) is not met by the end of the ID zone. An interrupt can also be generated if enabled in the ID control Register.

Present ID/Data Sync Status (ID1 = 1, ID0 = 0)

7	6	5	4	3	2	1	0
DS3	DS2	DS1	DS0	PIR1	PIR0	DR	XX

DS3 through 0 = Reserved

DR = Data RDGATE/SPDET Error
(Active state = 1)

When active, this bit indicates that RDGATE was active when SPDET was generated. RDGATE active is due to an extended data field read operation. This bit is cleared when writing to Address 1.

PIR1,0 = Reserved

7.16 SECTOR PER TRACK: ADDRESS X'F'

Write/read:

7	6	5	4	3	2	1	0
RSP	SC6	SC5	SC4	SC3	SC2	SC1	SC0

RSP = Read Stop Enable (Active State = 1)

SC6 through SC0 = Sector per Track

The user defines the number of sectors per track. This register is important whenever the autoincrement function is enabled in the ID control Register. Whenever the predicted ID field matches the maximum sectors per track, the end of the ID field is reached, and the ID Threshold has been met or exceeded, then the internal sector counter sets the sector byte to zero.

A.0 FORMAT DESCRIPTION

The following section describes the functionality of the WD60C31B as it relates to the ANSI Standard Continuous-composite Format for 5.25-inch and 3.5-inch optical drives. The WD60C31B can perform a track format operation on media which is unformatted. This device also performs ID voting functions that previously were handled by the WD10C00.

A.1 OPTICAL FORMAT

The ANSI specified Continuous-Composite Optical Media format is intended for use in Write Only RAM Memory (WORM) and magneto-optic drive applications. The WD60C31B is tailored for this application. The WD60C31B is programmable in order to accommodate future changes to the present format.

A.2 SECTOR FORMAT DESCRIPTION

The sector format is divided into three primary zones. The first zone is the ID area which contains the Sector Mark and three unique ID fields. The second zone is the drive area which contains the Mirror Mark, Flag, and Aauto Laser Power Control (ALPC) fields. The Mirror Mark and ALPC are for servo use. The Flag field is for WORM applications. Flag and ALPC are not used in 3.5-inch applications. The third zone is the data field which contains data, cyclic redundancy check (CRC) and error correction code (ECC).

A.3 SECTOR MARK

The five-byte sector mark is intended to be detected without recourse to use of the phase-locked loop. The pattern does not exist in data. Sector marks are identified by alternating long marks of three and five NRZ bit times.

A.4 VFO AREAS

There are three different lockup areas designated as VFO1, VFO2, and VFO3. The recorded information for VFO1 and VFO3 is identical in length and pattern. The area for VFO2 has one of two possible patterns and is four bytes shorter than VFO1 and VFO3.

Given that there are three concatenated ID fields and RLL 2,7 modulation coding is used, the conditions leading into each VFO2 area will be different depending on the last byte of CRC recorded in the preceding ID field.

A different VFO pattern prior to ID2 and ID3 is needed in order to allow the last byte of CRC to achieve correct decoding. Note that while the entering pattern is different, the VFO2 fields always end in the same pattern. The choice between the two patterns for VFO2 depends on the content of the last byte of CRC in the ID field immediately preceding the one being read.

A.5 ADDRESS MARK (AM)

The Address Mark is a special pattern, not used in RLL 2,7 data, and is a run-length violation for RLL (2,7) encoding.

A.6 ID AND CRC

The ID field consists of 5 bytes, allocated as follows:

- 2 bytes of track address, MSB/LSB.
- 1 byte of sector address:
  Bits 7,6 = ID number, (specifies one of three ID fields)
  00 = 1st ID
  01 = 2nd ID
  10 = 3rd ID
  Bit 5 = Reserved for future expansion, (S/B 0)
  Bits 4-0 = Sector Number, (binary value, most significant bit = 4)

The CRC consists of 2 bytes derived from the previous 3 bytes of ID information and using the polynomial:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The CRC calculation begins with the registers containing all 1's. (Refer to CCITT CRC standard). Input and output sequence uses MSB first.

NAME	FUNCTION	PATTERN
SM	Sector Mark	Special Redundant Pattern = 5 3 3 7 3 3 3 3 5 Channel code bit pattern following sector mark = 0010010010
VFO1, VFO2, VFO3	Lockup Field	VFO1= 01001001001...010010 VFO2= 10010010010...010010 VFO2= 00010010010...010010 VFO3= 01001001001...010010 *Note that VFO2 varies according to previous CRC pattern.*
AM	Address Mark	(Bit/Byte Sync) 16 code bits, (1 byte) 0100 1000 0000 0100
SYNC	Redundant Sync for data	Triple sync pattern 0100 0010 0100 0010 0010 0010 0100 0100 1000 0010 0100 1000
ID	Track number (2B) Sector number (1B)	High order/low order Bits 7-6 = ID Number (ID 0-2) Bit 5 = Reserved, (S/B 0) Bits 4-0 = Sector Number
CRC	ID field check bytes	CCITT Polynomial =1's
PA	Postamble	Allows last CRC byte closure under RLL (2,7) modulation
ODF	Offset Detection Flag	Unwritten, no grooves
Gap	Gap (Splice)	Unwritten - 3 byte areas
FLAG	Indicates written block continuous pulse	(5-byte area, decision by majority) 1001001001001001001001001001001001.
ALPC	Auto Laser Power Control	Blank 2-byte zone
DATA	User data, control, CRC, ECC and Resync	See Figures A-1 through A-4
BUFFER	Used for RPM timing margins	Unwritten area
RESYNC	Data field byte Sync	16 code bits (1byte) 0010 0000 0010 0100

TABLE A-1. SECTOR FIELD FUNCTIONS

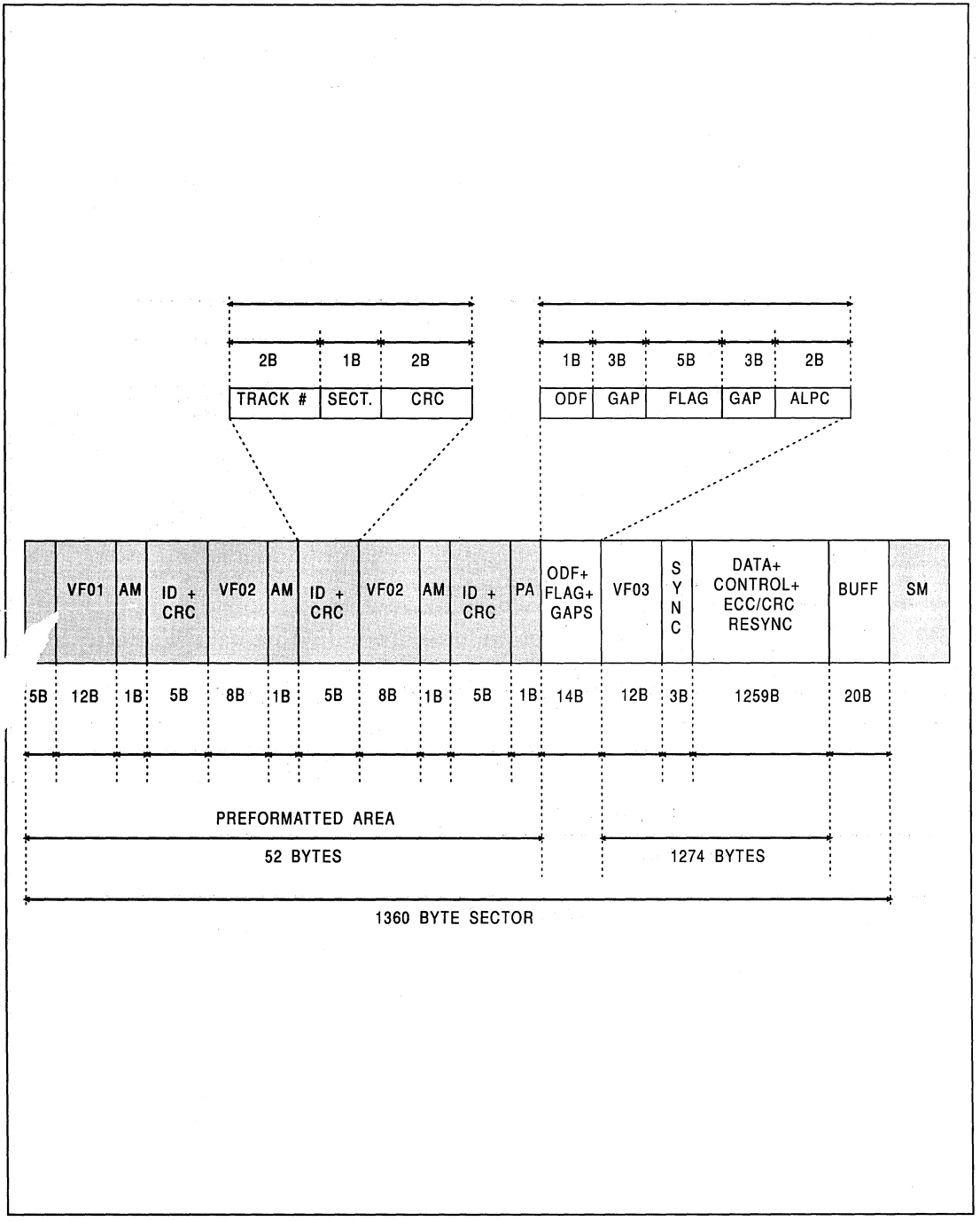

FIGURE A-1. 5.25-INCH, 1024-BYTE FORMAT

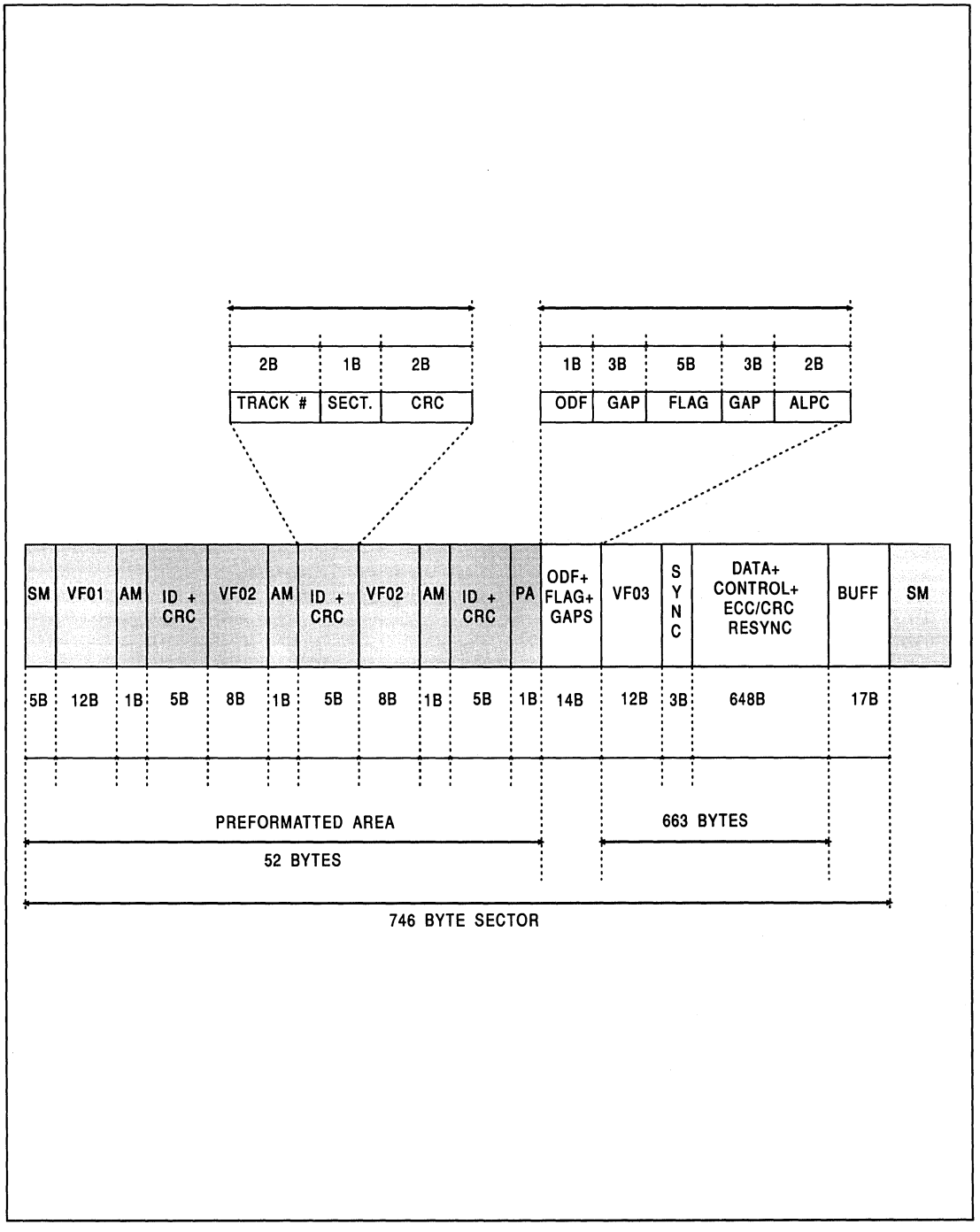

FIGURE A-2. 5.25-INCH, 512-BYTE FORMAT

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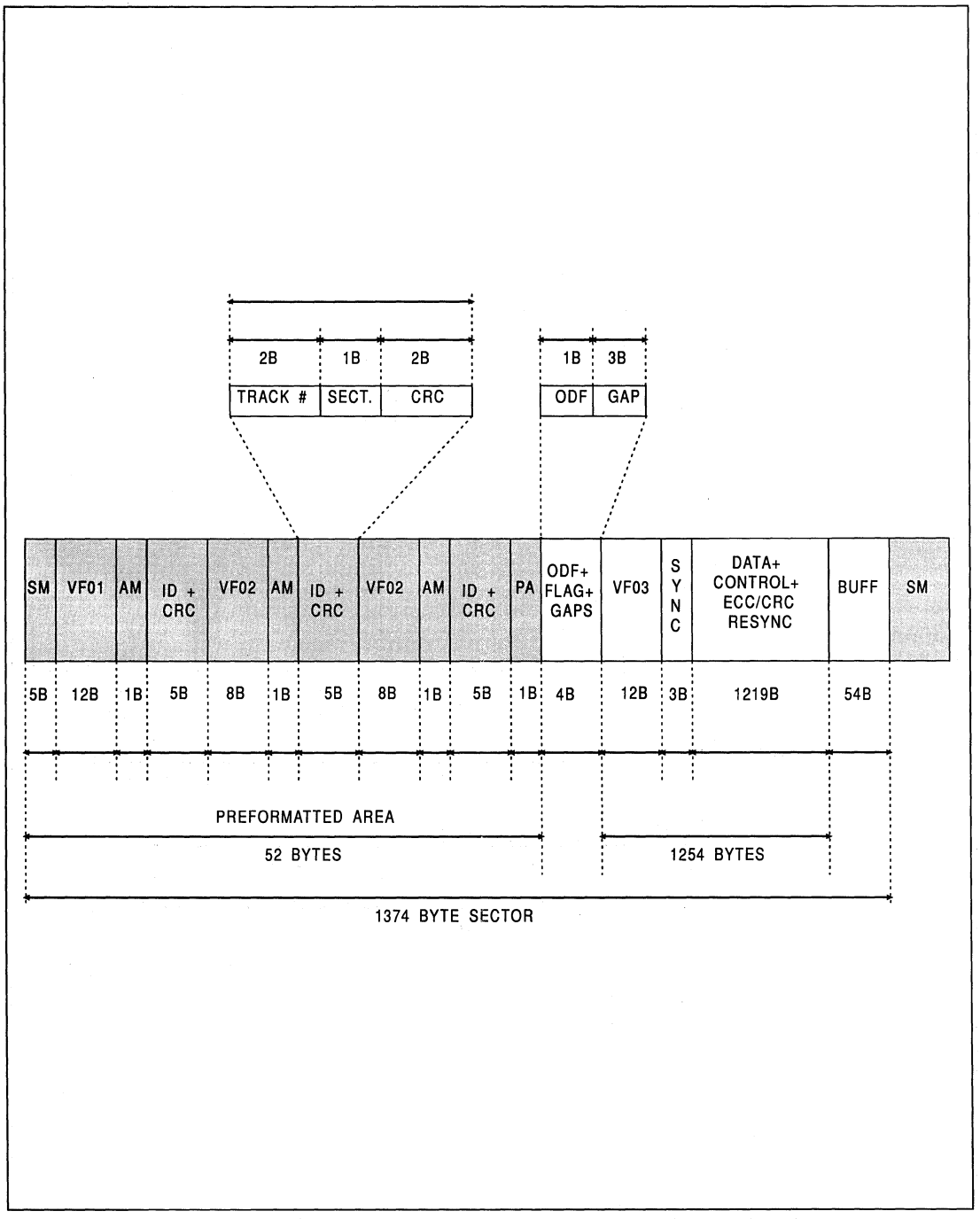

FIGURE A-3. 3.5-INCH, 1024-BYTE FORMAT

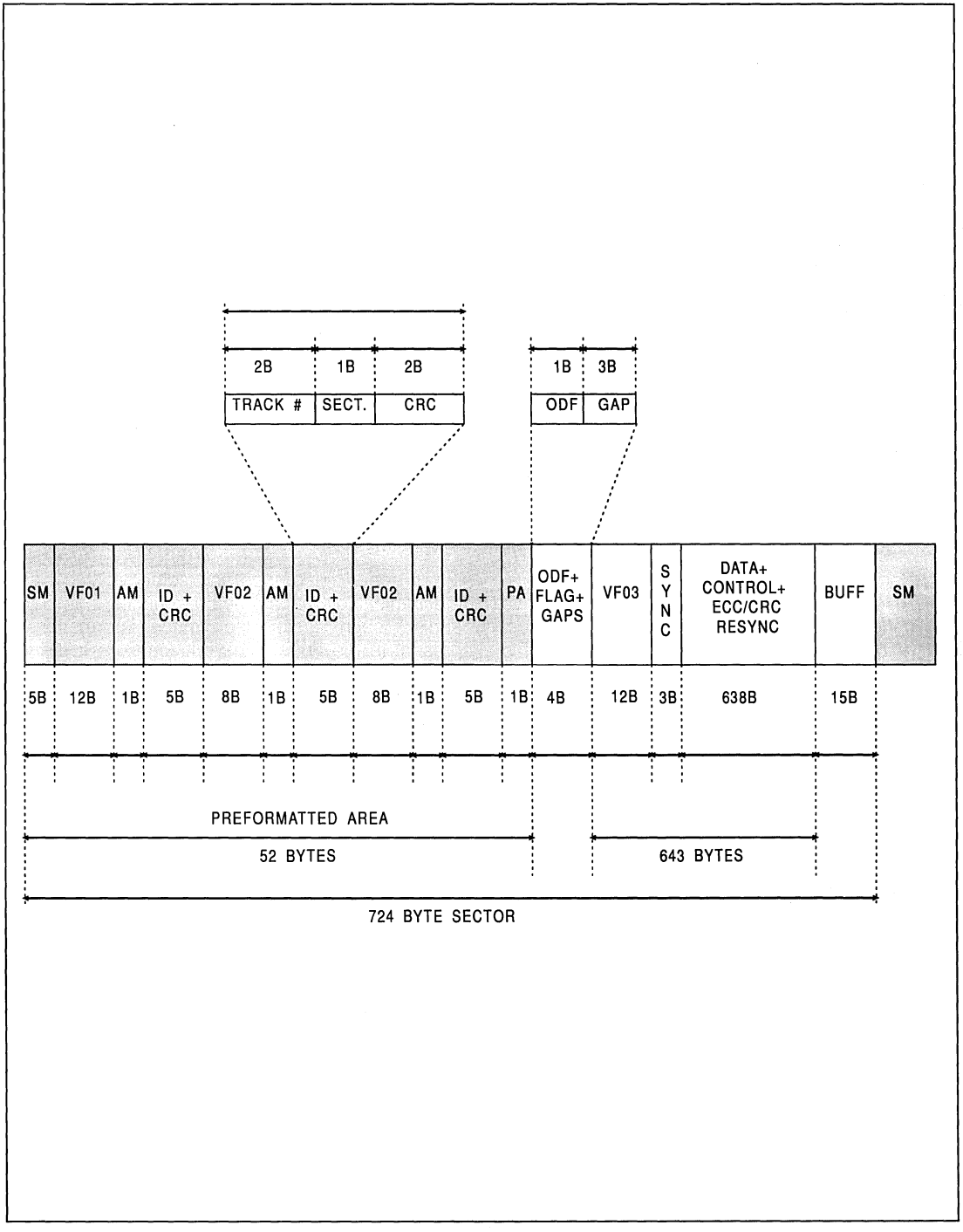

FIGURE A-4. 3.5-INCH, 512-BYTE FORMAT

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A.7 POSTAMBLE (PA)

The last portion of the preformatted area (PA) consists of a one postamble byte on the third ID field. Due to the use of the RLL 2,7 encoding scheme, the framing of the last byte of CRC in the last ID field is uncertain within a few bit times. The postamble allows the last byte of CRC to achieve closure and permits the ID field to always end in a predictable manner.
This is necessary in order to locate the Offset Detection Flag/Mirror Mark in a consistent manner.

A.8 ODF / MIRROR MARK

The Offset Detection Flag (ODF) or Mirror Mark is an area with no grooves or preformatted data. The purpose is to allow track offset detection within the drive.

A.9 FLAG

The flag field prevents inadvertent write operations over previously written data in WORM drive applications. The flag may be written after successful completion of the write operation or during the same pass. The use of this field is optional. It is not used in 3.5-inch format.

A.10 AUTO LASER POWER CONTROL (ALPC)

The Auto Laser Power Control is a grooved test area for calibration of the laser power levels used by the drive. It is not used in 3.5-inch format.

A.11 DATA FIELD

The data field consists of 1024 bytes of user data and 223 bytes of CRC/ECC/Resync information, plus 12 bytes of control information. A 512-byte data field is optional. The 3.5-inch format has reduced the pointer field to xxx bytes for the 512-byte sector.

A.12 RESYNC

The resync mark reestablishs byte synchronization when it is lost during a data segment. (A data segment consists of the bytes of data, usually 15 or 20 bytes, between resync marks.)

Resync marks are used in only the Data/Control/ECC/CRC field. Resync marks are written within the data as shown in Figures A1 through A4.

A.13 BUFFER

Motor speed tolerances and some electrical and mechanical tolerances require a buffer zone at the end of each sector. No written information is present in the buffer. The buffer field is a 1-byte postamble to the data field to allow closure of channel bits in the RLL 2,7 encoding scheme. During format, however, this area is filled with a high-frequency pattern of "100".

B.0 WD60C31 FUNCTIONS

B.1 READ OPERATIONS

The WD60C31B is responsible for the detection of the following special format marks:

B.1.1 SECTOR MARK

The WD60C31B is constantly in a sector mark detection mode. If a sector mark is detected (3 of 5 majority), a (Pseudo Sector Mark Dectect) SPDET pulse goes to the WD10C00. If no sector mark is detected at the end of each sector, the WD60C31B creates a SPDET. The created SPDET is based on a worst case speed tolerance of +/-.5 % or 1%. This mark is detected under a window, .5% or 1%, thereby minimizing misdetection.

B.1.2 ID ADDRESS MARK

The WD60C31B examines the input RLL bit stream whenever an ID field area is expected and RDGATE is active. RDGATE should be applied after a SPDET is sent. The RLL pattern is programmable by the microprocessor. The RRCLKs are paused when RDGATE is raised and NRZI goes from high to low. Once the ID AM is detected, the RRCLKs begin again. The NRZI data stream is a byte of zeros and the ID field (Track High byte, Track Low byte, and sector byte) follows. A SYNCDET pulse is sent along with the first ID address byte. The WD10C00 should be programmed to wait for the SYNCDET signal and expect the Track High byte to be the Address Mark. The WD10C00 then performs a bit-for-bit comparison and CRC verification. The WD60C31B can also be placed in another mode, the ID Search mode. This mode should be used whenever the Track High byte is not predictable. This is used to satisfy WD10C00 requirements. In this mode, the SYNCDET signal is moved forward one byte. This means that this signal becomes active during the byte of zeros preceding the Track High byte. The WD10C00 should be programmed to wait for the SYNCDET and an address mark of zeros. A bit-for-bit comparison over the complete ID field is performed. The WD10C00 stores the full ID field in its internal registers. The Normal mode only stores the Track Low byte, sector byte, and CRC.

B.1.3 DATA ADDRESS MARK

The WD60C31B examines the input RLL bit stream whenever the Data field area is expected and RDGATE is active. The RLL pattern that is expected is microprocessor programmable. In addition, the level of pattern correlation is programmable. A SYNCDET pulse is sent whenever a comparison is made. This pulse is sent along with a psuedo-address mark NRZ byte of '00's. The WD10C00 is programmed to make this comparison.

B.1.4 DATA RESYNC MARKS

The WD60C31B detects and removes the Resync marks from the NRZI data stream. An internal window is generated which predicts the location of the next resync. This window minimizes the probability of misdetection In normal mode, the internal resync window is opened if RDGATE is raised in the data field, the Data Sync has been detected, and a data segment has passed. Four programmabale window sizes are available: two fixed sizes and two variable sizes. The ANSI specification states that the number of bytes in a data segment is 15 or 20. The WD60C31B permits the microprocessor to set the value from 0 to 31 bytes. A value of zero assumes that there are no resyncs. In addition, the Resync mark pattern can also be programmed. In an error recovery mode, RDGATE must be applied in a data field, but the Data Sync Mark need not be detected. Instead, the Resync mark is the first mark to be detected. The first resync window is opened after a preprogrammed number of bytes are sent to the WD10C00. This means that the WD10C00 receives the exact number of data bytes per sector. This mode is used if the data sync is undetectable after lowering the Data Sync Threshold value.

B.2 WRITE FUNCTIONS

During write, the WD10C00 and WD60C31B must write in the Media Data Format the following pattern: 1) VFO field, 2) Data Address Mark, 3) Encoded RLL Data, 4) Data Resync Marks, and 5) Data Postamble. The WD10C00 sends a dummy VFO pattern that contains the exact number of bytes that are written on the disk. The WD60C31B creates the actual high frequency pattern, "100100". The WD60C31B continues writing this pattern until an AMENA signal is sent from the

WD10C00. This AMENA signal is sent with the last byte of the dummy VFO. When AMENA is received, the VFO is completed at a byte boundary and the Data Sync Mark is injected into the RLL data stream pulse which initiates the writing of the Data Sync Mark. When the WD60C31B inserts the Data Sync Mark or the Rsync Marks into the RLL data stream, the RRCLKs are paused. This action halts the data byte transfer through the WD10C00. In effect, the WD10C00 is unaware of this pause. This pausing of the RRCLKs is also performed during a read operation. The WD10C00 sends data bytes, CRC bytes, and ECC bytes. An AMENA is sent with the last byte of the ECC field. This action ends the insertion of the Resync marks into the encoded RLL data stream. In addition, 3 bytes of pad should be sent after the last byte of ECC. These bytes compensate for the WD60C31B internal pipeline structure and closure requirements of the last bit of the last byte of ECC.

B.3 FORMAT OPERATION

The WD60C31B is also capable of performing a track format operation. This allows the WD60C31B to operate with drives that use either prestamped media or nonstamped media. The format must conform to the prestamped format requirements. The task of formatting the media is shared by the WD10C00 and the WD60C31B. In general, the WD10C00 must 1) keep track of the number of bytes that are written on the track; and 2) inform the WD60C31B when the special marks (sector mark, ID address marks, and Data Sync Mark) are to be inserted into the RLL data stream. The WD60C31B is responsible for encoding and decoding the NRZ serial data from the WD10C00; inserting the special marks mentioned above (also Resync Marks), and predicting the next type of special mark to be written.

The general format sequence is as follows:

1) All special marks are programmed in the WD60C31B.
2) The WD60C31B is set for Track Format (Secondary Configuration Register).
3) The drive provides an Index to the WD10C00.
4) The WD10C00 raises Write Gate when Index is received. The NRZ data transfer begins. The first NRZ data bit this sent must be a 1.
5) Upon receiving Write Gate, the WD60C31B begins writing the first Sector Mark. All subsequent sector marks are written when a specific number of AMENAs are received. The NRZ data from the WD10C00 is internally pipelined within the WD60C31B. When the pipeline is full, the RRCLKs are paused. When the writing of the sector mark is complete the RRCLKs start again and NRZ data encoding begins and is merged into the RLL data stream.
6) The WD60C31B continues to encode the NRZ data until it receives an AMENA. This pulse from the WD10C00 defines the concurrent NRZ data byte as the last byte before the next special mark. The special mark is inserted and encoding continues. RRCLKs are restarted. The WD60C31B keeps track of the quantity of AMENAs that are sent. The type of special mark to be inserted is based on the quantity of AMENA signals received.

B.4 MODULATION METHOD

The modulation method used to record all information on the disk in the formatted areas shall be the Run-Length Limiting (RLL) code known as RLL 2,7.

CODE CONVERSION	
NRZ Input Bits	**RLL 2,7 Channel Code Bits**
10	0100
010	100100
0010	00100100
11	1000
011	001000
0011	00001000
000	000100

B.5 ID VOTING (ON-THE-FLY ID VERIFICATION)

In addition to the previously discussed methods of ID read operations, the WD60C31B can perform ID voting. In this mode, the WD60C31B detects and verifies the validity of the three IDs. The IDs undergo the following test.

- Detection of a valid ID Address Mark byte
- A successful bit-for-bit comparison of the track and sector bytes
- A successful match of CRC from the drive to an internally derived CRC

If these parameters are met, a single ID is considered valid. The user can program the number of IDs which must be found to satisfy a write or read operation. When all conditions are met, the WD60C31B sends the WD10C00 a SYNCDET and an address mark byte of F0 on the NRZI line. If all conditions are not met, the WD60C31B sends a SYNCDET and an address mark byte of FF to the WD10C00.

Track streaming is also supported. This means that the internally stored track and sector values can automatically be incremented when the ID threshold is met. The user must set up three conditions. First, the three ID modes must be enabled. Second, the maximum number of sectors per track must be set. Third, the track and/or sector autoincrement function can be independently enabled. This function minimizes the microprocessor overhead between sector IDs.

WD60C40A

Peripheral Cache

Manager Device

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 ARCHITECTURAL DESCRIPTION

The WD60C40A peripheral cache manager (PCM) is a custom enhancement of the WD60C40, and is intended to be a drop-in replacement for the latter device. The WD60C40A is fully compatible with the WD60C40 as far as functional and timing requirements are concerned. In addition, the WD60C40A provides three new features: longitudinal redundancy checking (LRC), through parity, and an improved slave burst mode protocol (WD Bus Mode).

The WD60C40A peripheral cache manager (PCM) can control 1 Mbyte of dynamic RAM and the buffering required to allow seemingly simultaneous access of this buffer by three requestors. The three requestors are assumed to be two block-oriented devices and a microprocessor.

The two device interfaces to the dynamic RAM are designed to support block-oriented peripheral formatter chips, such as the WD10C00 Hard Disk Formatter, or block-oriented bus interface chips, such as the WD33C93A SCSI Bus Interface Chip. The implication of block-oriented devices is that the devices do not have the capability of randomly accessing data within the memory array. This restriction allows for the removal of the addressing pins that are normally associated with an interface. The 20-bit address counters that are required to select a byte within the array are now incorporated into the WD60C40A.

The buffer control logic interfaces with an external dynamic RAM array and arbitrates the access into this array from the three external sources. The internal arbitrator in the PCM also includes the refresh logic that is internal to the PCM into its arbitration mechanism.

The dynamic RAM memories do not have the random access bandwidth to sustain multiple high-speed devices. The dynamic RAM memories do incorporate a feature known as "page mode" that increases their bandwidth to the point that they can sustain multiple high-speed devices. The dynamic RAMs have a multiplexed address bus width the address into the array being divided into two parts, a row address and a column address. The dynamic RAMs allow a feature that if the next access into the array is in the same row (same page), then only the column address must be updated from the addressing logic. This scheme carries the penalty that a FIFO must be available to hold the data to/from the port to ensure that it can transfer data in a continuous block when a port gains access to the RAM. The PCM incorporates 16 bytes of FIFO into each of the peripheral ports to support the page mode memory architecture. This scheme has the advantage that the memory bandwidth is increased by a factor of about 75% over the random access bandwidth, allowing a large buffer memory to be mechanized by inexpensive dynamic RAMs, but having the performance characteristics of a static RAM buffer.

The external dynamic RAM buffer may be eight bits or nine bits wide. The depth of the array and the organization of the devices that make up the array are as follows:

SIZE	ORGANIZATION		
16 KB	2	16Kb x 4	(+ 64Kb x 1 parity)
64 KB	2	64Kb x 4	(+ 64Kb x 1 parity)
64 KB	8	64Kb x 1	(+ 64Kb x 1 parity)
256 KB	2	256Kb x 4	(+ 256Kb x 1 parity)
256 KB	8	256Kb x 1	(+ 256Kb x 1 parity)
1 MB	2	1Mb x 4	(+ 1Mb x 1 parity)
1 MB	8	1Mb x 1	(+ 1Mb x 1 parity)

Note: The use of static RAM is possible with additional logic.

In the following description, refer to Figure 1, the block diagram of the WD60C40A, and to the example board environment in Figure 2. A typical situation to use as an example of the actions within the part is that of a disk controller. In this example, port 'B' of the device is connected to a bus interface controller (ex. WD33C93A), and port 'A' of the device is connected to a disk interface controller (ex. WD10C00).

The example begins with the assumption that all devices are currently active, the refresh time has arrived, and the microprocessor is requesting a data item. The PCM is currently servicing the FIFO that is attached to the device port 'A'. The microprocessor is currently at a wait bus cycle because of the RDY signal from the PCM being inactive. The PCM moves data to/from the memory and the port 'A' FIFO until the FIFO is full/empty, or the transfer counter of port 'A' is exhausted. If during this sequence, the PCM detects that a dynamic RAM page boundary is

being crossed, the PCM will update the row address, and continue the page mode transfer. While this action is occuring, any byte transfers to/from the other device port are stored in that device port's FIFO. When port 'A' has finished its data transfers, the PCM first services the host data request, then the refresh request(s), both of which have priority over block transfers. The PCM then initiates transfer between the port 'B' FIFO, and the dynamic RAMs.

The PCMs priority system when arbitrating is:

- microprocessor requests
- refresh requests
- the higher priority peripheral channel
- the lower priority peripheral channel

The control of the peripheral channel priority is under firmware control if the channels are peers in their capability of sustaining a pause in their transfers. If a channel is programmed as 'non-pausible', and the other channel is 'pausible' then this channel is given priority in the arbitration mechanism, regardless of the other firmware priority controls. If the channels are peers, such as both being 'pausible' or both being 'non-pausible', then the priority of the channels is controlled by firmware selecting one of the channels as higher priority through option register 2. See also the descriptions of the AHI bit in option register 2, and PAUS bits in the channel control register.

Note that arbitration does not occur until the requestor currently being serviced has completed its entire burst. This means that page mode bursts between the channels and memory are not interrupted by requests from higher priority requestors. There are two exceptions to this general rule. The first exception is a non-pausible device that is selected by firmware as having higher arbiter priority. This channel is then allowed an "urgent request", when its FIFO is almost exhausted. This "urgent request" will send a false end of transfer signal through the other port and cause arbitration to occur, and this channel will then win arbitration if the single cycle devices are not requesting. This is done to minimize the occurence of over/under-run errors in high priority non-pausible devices. The second exception that causes a burst to be halted is for a refresh burst. The refresh request occurs at regular intervals (see option register section for specific details), but if it is not serviced because of a channel burst, then the request is queued into a counter. When four refresh cycles have been queued (about 60 µsec.), then the "urgent request" mechanism will force arbitration, and a burst of four refresh cycles will be performed. This is done to maintain memory data integrity.

The programmable features of the internal logic allow the controller firmware to control and "tune" the actions of the PCM. The PCM needs know if the devices are capable of being throttled. Most devices that attach to peripherals have minimum data buffering, so the port logic must be programmed to look for overrun/underrun situations when the FIFO is full/empty. Some devices that attach to busses or other peripherals that have variable data rates, are capable of being 'stalled' when the FIFO is full/empty, and the port logic is capable of holding the port until the FIFO is ready.

The PCM also implements a "pipelined" pointer mechanism that allows the programmer to set the pointer (buffer address) of the current device transfer, and if required, set the pointer of the next transfer, while the current transfer is taking place. This address is held in the address pointer holding register to be automatically transferred to the address pointer at the end of the current transfer. If the next transfer's buffer is contiguous with the current transfer's buffer, then the address pointer "pipeline" need not be loaded, and when the next transfer begins the address pointer will continue from its current position. This address is therefore only necessary if the next transfer is at a memory address that is not contiguous with the end of the current transfer. The transfer counter is always loaded from the transfer counter holding register at the start of a new block transfer, but the transfer counter holding register need only be reloaded if the block size of a transfer needs to be changed. When the current transfer finishes, the firmware can be interrupted, while the hardware continues directly into the next transfer. With this mechanism, the firmware now has a block time to determine what is to be done when this transfer finishes, rather than doing this during the inter-block gap times. If pipelined (ie. continuous) transfers are required, then microprocessor action is required whenever the pipeline becomes empty. If the next transfer is the same size as the current, and contiguous in address, then the firmware need only issue a new channel start command. Alternatively, the firmware can load new values into the "pipeline" registers before issuing the

start, and dynamically control the transfer size and buffer location. The firmware can poll the status or wait for an interrupt (if enabled) to indicate that the holding registers are available.

The device channels are mechanized with eight or nine data lines, and five control/handshake lines. Four control signals are programmable to allow interfaceing to multiple types of device controller chips. Features such as the master/slave relationships between the PCM and the external peripheral controller, the polarity and timing of the signals that do the handshake, input/output control direction, and the mode that the control lines emulate are all programmable.

1.2 FEATURES

- 5 Volt only operational power.
- 1.25 micron CMOS for low power consumption.
- 84 pin JEDEC PLCC or 84-pin JEDEC PQFP packages.
- Supports dynamic memory configurations from 16 KB to 1 MB.
- Supports static memory configurations.
- Supports parity on the memory array.
- Supports parity on peripheral ports.
- Supports parity pass-through (parity is passed through a device with the data and not regenerated at the device's outputs).
- Supports longitudinal redundancy checking (LRC) on peripheral ports and FIFOs.
- Aggregate memory bandwidth of greater than 9.0 Mbytes/sec, using industry standard 100 ns. dynamic RAMs.
- Supports two peripheral channels.
- High Speed Channels support peripheral data rates of:

  6.25 Mbytes/sec as bus master with 25 MHz input clock, the maximum data rate is input clock divided by 4.

  10.0 Mbytes/sec as bus slave, with 25 MHZ input clock, the maximum data rate is input clock divided by 2.5.
- Programmable configuration of device channel interface.
- Internal FIFOs on peripheral channels.
- Supports independant transfers on both peripheral ports and microprocessor simultaneously.
- Large memory allows peripheral controllers to be implemented that "decouple" the host and disk transfer rates, maintaining 1:1 disk interleave regardless of host transfer rate.
- Provides "minimum chip count" solution for mechanizing a peripheral cache controller.
- Supports high-speed microprocessor bus cycles, such as Intel* 80186 or 80188 processors running at 12.5 MHz (no wait state required when accessing the PCM registers).

1.2.1 Longitudinal Redundancy Checking

Both channels must operate as the bus master when using the LRC feature. LRC generation and checking takes place between the channel data bus input and output buffers and the channel FIFO. The LRC calculations do not include the parity bit. Refer to Section 4.12 for more information.

1.2.2 Through Parity

Parity is passed through the chip with the data and not regenerated at the chip's output. This makes it possible to chain "send status" in the WD33C93A.

1.2.3 Western Digital Bus Mode

The slave burst DMA protocol is modified in order to use the pipelining capability of the WD60C40A with the SBIC. As the WD60C40A nears the end of a burst, it switches to a single-byte transfer protocol to avoid over/under-flowing the FIFO. In the old implementation, the WD60C40 waits to deassert DRQ when both DACK and the _RD or _WR strobe is asserted. This may result in the SBIC sending two bytes instead of just one. The WD60C40 will be confused if the SBIC sends two bytes on the last request. The new implementation fixes this by having the WD60C40A deassert DRQ upon the assertion of DACK, thus guaranteeing that the SBIC sends only one byte.

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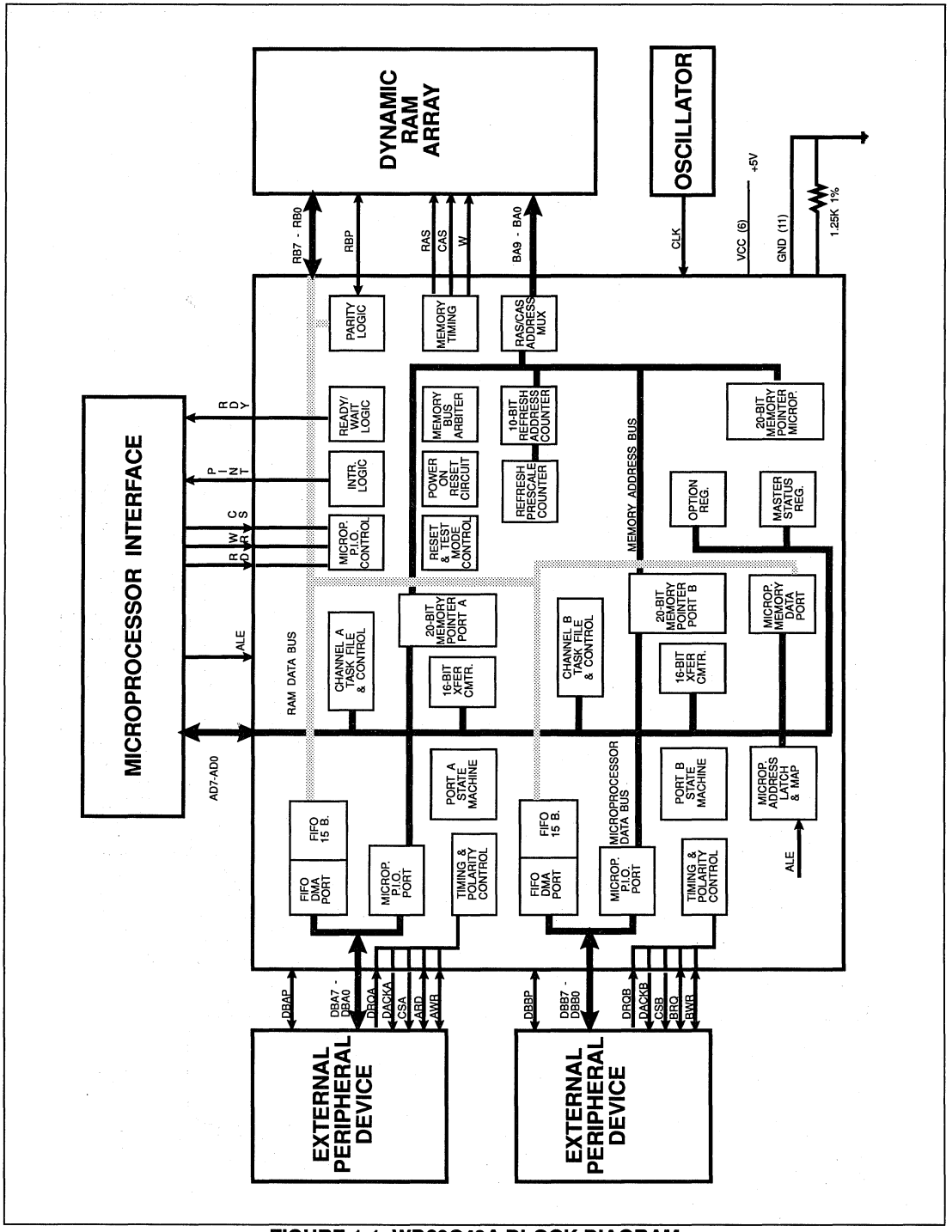

FIGURE 1-1. WD60C40A BLOCK DIAGRAM

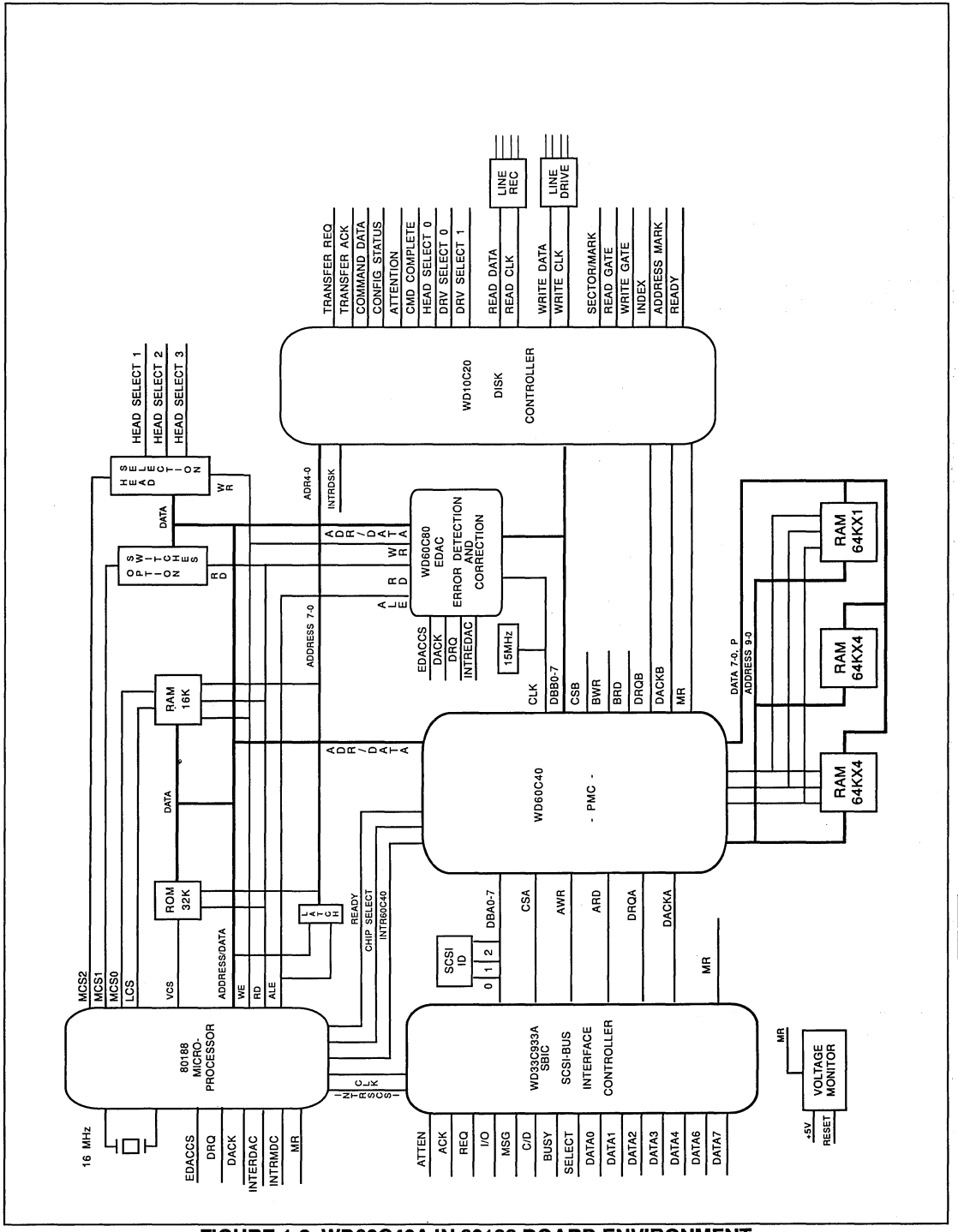

FIGURE 1-2. WD60C40A IN 80188 BOARD ENVIRONMENT

2.0 PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O
1,22,30,43, 56,64	V_{CC}	+5 Volt power supply connection	I
2,11,21,23, 29,42,44,57, 63,65,75	GND	Ground power supply connection	I
3 thru 10	AD0 thru AD7	µP ADDRESS/DATA BUS	I/O
12 thru 19	DBB0 thru DBB7	DEVICE BUS B DATA	I/O
20	DBBP	DEVICE BUS B PARITY BIT	I/O
24	$\overline{CSB}$	CHANNEL SELECT B	O
25	DRQB	DEVICE PORT B CYCLE REQUEST	I/O[1]
26	DACKB	DEVICE PORT B CYCLE ACKNOWLEDGE	I/O[2]
27	$\overline{BRD}$	DEVICE PORT B READ STROBE	I/O
28	$\overline{BWR}$	DEVICE PORT B WRITE STROBE	I/O
31 thru 38	RB7 thru RB0	DYNAMIC RAM DATA BUS	I/O
39	RBP	DYNAMIC RAM PARITY BIT	I/O
40	W/$\overline{WE}$	DYNAMIC RAM WRITE/STATIC RAM $\overline{WE}$	O
41	$\overline{CAS}$/$\overline{OE}$	DYNAMIC RAM $\overline{CAS}$/STATUS RAM $\overline{OE}$	O
45	$\overline{RAS}$	RAM ROW ADDRESS STROBE	O
46 thru 55	BA0[3] thru BA9	RAM ADDRESS BUS[3]	O
58	$\overline{AWR}$	DEVICE PORT A WRITE STROBE	I/O
59	$\overline{ARD}$	DEVICE PORT A READ STROBE	I/O
60	DACKA	DEVICE PORT A CYCLE ACKNOWLEGE	I/O[2]
61	DRQA	DEVICE PORT A CYCLE REQUEST	I/O[1]
62	$\overline{CSA}$	CHANNEL SELECT A	O
66	DBAP	DEVICE BUS A PARITY BIT	I/O
67 thru 74	DBA7 thru DBA0	DEVICE BUS A DATA BUS	I/O
76	CLK	CLOCK	I
77	$\overline{RST}$	RESET	I
78	$\overline{CS}$	µP BUS CHIP SELECT	I
79	$\overline{WR}$	µP BUS WRITE CYCLE STROBE	I
80	$\overline{RD}$	µP BUS READ CYCLE STROBE	I
81	ALE	µP ADDRESS STROBE	I
82	$\overline{PINT}$	µP INTERRUPT REQUEST	O[4]
83	RDY	µP WAIT CONTROL	O[4]
84	RBIAS[5]	RESISTOR BIAS[5]	I

NOTES:

1 I = WD60C40A bus master mode. O = WD60C40A bus slave mode

2 I = WD60C40A bus slave mode. O = WD60C40A bus master mode.

3 BA0 is the LSB.

4 Open drain output

TABLE 2-1. PIN DESCRIPTIONS

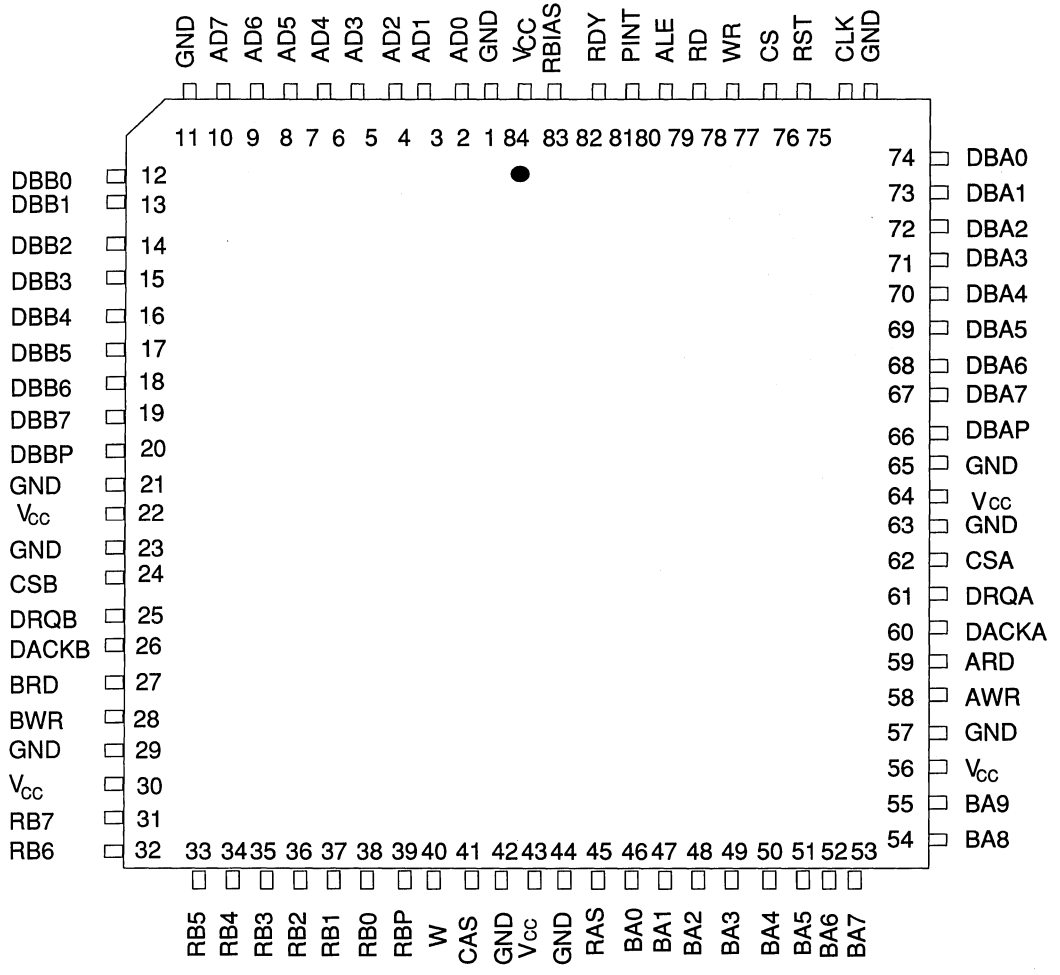

FIGURE 2-1. PIN DESIGNATION

3.0 NON-CHANNEL REGISTERS

The PCM was intended for use with the Intel 80186 processor and as such has been designed to interface easily with the 16-bit data bus of that processor. This is not to say that it cannot easily attach to other 8-bit or 16-bit microprocessors like Intel 8085, 8051, or 8096. The main requirement is that it be supplied with a multiplexed address/data bus with A7 to A0 multiplexed with D7 to D0 in that order.

As the PCM has only an eight bit data bus and it was decided not to handle the BHE signal, there are certain characteristics of the PCM that need explaining. First, all internal registers appear on even and the following odd byte address. This is because address signal A0 is not used inside of the PCM. The order of the registers was also arranged so that they appear in the order that they would normally be programmed. This allows the PCM to be attached to the 80186 and string move operations used to allow the fastest possible handling of loading the PCM.

Finally, the registers associated with the operation of the PCM itself do not decode the signal A7 so that they appear in both halves of the register map, facilitating an easier modulization of the driving firmware. Only the even addresses of the registers will be shown. Refer to pages 10 through 35 for a summary of all the non-channel registers.

3.1 OPTION REGISTER

Address = 60H or E0H
Read/write register

7	6	5	4	3	2	1	0
MPAR	CAW1	CAW0	SRAM	RRC3	RRC2	RRC1	RRC0

The option register is a read/write only register to the firmware. The bits represent settings of options that must be selected to match the board design. There is the facility to read option switches and allow the firmware to assertain the hardware configuration in user 'adjustable' implementations. This register should be the first written after a reset sequence, and should not be written to thereafter unless another reset sequence has occurred.

3.1.1 RRC3 Through RRC0 Refresh Rate Count Field

The refresh rate count field indicates to the PCM the prescale count to use for determing the refresh rate of the dynamic RAMs. The value of the refresh rate count field is effectively multiplied by 32, then subtracted from 512 to determine the number of clocks that will occur between refresh cycles. The value of this field is dependent upon the frequency of the PCMs clock. The following table shows the relationship of clock frequency, and refresh rate count field values, to produce 15.6 microsecond refresh cycles (for standard 128 cycle 2 ms. dynamic RAMs).

Field Value	Cycle Count	Freq. Range[1] Low	High	Refresh Intrvl[2] Low	High
12	128	8.2	10.2	15.6	12.5
11	160	10.4	12.2	15.4	13.1
10	192	12.4	14.2	15.5	13.5
9	224	14.4	16.4	15.6	13.7
8	256	16.6	18.4	15.4	13.9
7	288	18.6	20.4	15.5	14.1
6	320	20.6	22.4	15.5	14.3
5	352	22.6	24.4	15.6	14.4

[1] Frequency ranges are in MHz.
[2] Refresh intervals are in µs.
NOTE:
The other field values are valid but are unlikely to be useful to the customer.

3.1.2 SRAM Static Ram Mode (bit 4)

The Static Ram Mode bit informs the PCM that the memory array is composed of static RAMs. When the bit is set, the PCM is in static RAM mode. This changes the signals that the PCM uses to access the memory array. Because of the multiplexed address bus of dynamic RAMs, it will be necessary for an external latch to be added to demultiplex the address lines. In addition, external address decoding will be necessary to expand the

RAM to the full addressable capability. To assist in this, two of the RAM control signals change when the static RAM bit is set. First, the RAS signal is used to control the external latch that is to demultiplex the address, when a valid row address is available on BA8 to BA0. RAS is intended to drive the clock input of a 74F373 type octal D-type latch, there is a direct analogy to the operation of dynamic RAMs at this point, with the exception that the row address latch is external to the memory devices. Secondly, static RAMs also have different read and write characteristics to dynamic RAMs. In dynamic mode, the W signal, signals the RAMs that a write cycle is about to occur, with the actual write action being generated by the falling edge of the CAS signal. This is known as early write mode. A read would occur if the CAS signal went active (low) with the W signal inactive (high). In static mode, the W and CAS signals change to support the separate WE and OE signals of static RAMs. In static mode, the CAS becomes the OE signal, still being active low but it will only occur on RAM read cycles, having the same shape and timing as for dynamic RAM cycles. The W signal becomes the WE signal, still being active low and only occuring in write cycles, but of a shape and timing similar to the CAS/OE signal. Finally, the arbitration logic no longer receives refresh requests as the static RAMs require no refresh, of course. At this stage it should be noted that the static RAM configuration is still liable to the row change overhead, when a row boundary is crossed during a burst of data cycles between the peripheral port FIFO and the memory.

The PCM is initialized to a special state at power up to ensure that there is no activity on the RAM control pins. This feature is used in the "power start" of the dynamic RAMs, which need to be left for a minimum time after power up. Please refer to the "Reset Sequences" section of this document for a description.

3.1.3 CAW1, CAW0 Column Address Width Field (bits 6,5)

The column address width field informs the PCM the type of RAM array that it is dealing with. The PCM uses the field to control the address multiplexer to the RAMs, and to determine the page mode boundaries of the RAMs. When a new page is detected, then the PCM executes a new RAS cycle, RAS goes inactive to precharge the RAS signal and then RAS goes active to latch the new row address and establish access in the new RAM page.

This field has no affect if the SRAM bit (bit 4) is set. When the SRAM mode is in effect, the PCM is forced to the ten bit column address mode.

00 = 10-bit column address (1meg DRAM). Bits 19 - 10 are the output on BA9 - BA0 during RAS time. Bits 9 - 0 are the output on BA9 - BA0 during CAS time.

01 = 9-bit column address (256K DRAM). Bits 18 - 9 are the output on BA9 - BA0 during RAS time. Bits 8 - 0 are the output on BA8 - BA0 during CAS time.

10 = 8-bit column address (64K DRAM). Bits 17 - 8 are the output on BA9 - BA0 during RAS time. Bits 7 - 0 are the output on BA7 - BA0 during CAS time.

11 = 6-bit column address (16K DRAM). Bits 15 - 6 are the output on BA9 - BA0 during RAS time. Bits 5 - 0 are the output on BA5 - BA0 during CAS time.

3.1.4 MPAR = Memory Parity Enable (bit 7)

The parity enable bit informs the PCM that the memory array has a parity bit attached. When the bit is set, the PCM generates odd parity (the sum of all one bits including the parity bit will be an odd number) on memory writes, and checks parity on memory reads. If there is even parity on a memory read, the PCM will cause a parity error interrupt in the appropriate status register. When the bit is reset, the PCM will not generate parity on a write, or check parity on a read. The microprocessor firmware can use this bit to test the parity logic of the PCM, when there is parity memory. When the parity enable bit is reset, the RBP pin of the PCM will be at a logic one level during a write cycle.

3.2 OPTION REGISTER 2

Address = 62H or E2H
Read/write register
The option register 2 is initialized to zero by the PCM reset sequence

7	6	5	4	3	2	1	0
0	0	NOWAIT	WAITE	AHI	INTE	BINTE	AINTE

3.2.1 AINTE A Channel Interrupt Enable

The A channel interrupt enable bit allows interrupts from the "A" peripheral channel to exit the PCM by way of the PINT pin. This allows the programmer the capability to selectively disable interrupts from this channel while still allowing PCM interrupts from the other PCM resources. This bit only affects the transmission of the channels interrupt to the PINT pin, and does not affect the operation of any of the channels interrupt enables, or interrupt status flags.

3.2.2 BINTE B Channel Interrupt Enable

'A' CHANNEL	'B' CHANNEL	AHI PRIORITY
Non-pausible	Pausible	X A Channel
Pausible	Non-pausible	X B Channel
Non-pausible	Non-pausible	1 A Channel
Non-pausible	Non-pausible	0 B Channel
Pausible	Pausible	1 A Channel

This bit performs the same function as AINTE, but for the "B" channel.

3.2.3 WAITE Wait Enable

This bit is the master enable for any PCM wait condition to exit the PCM by the RDY pin. This allows the programmer the capability to selectively disable the RDY pin from the PCM. This bit only affects the transmission of the wait to the RDY pin, and does not affect the operation of any of the PCM wait sequences, or status.

3.2.4 NOWAT Non-waitable Microprocessor Interface (bit 5)

The "non-waitable" bit is used to distinguish to the PCM that the microprocessor or board design does not support the RDY function to extend bus cycles. This bit controls how the PCM performs accesses to the data buffer and programmed I/O to the peripheral ports. This bit is reset by the PCM reset sequence.

When this bit is a zero, the PCM is to be used in a board with multiple devices sharing the microprocessor ready signal. The internal "ready" status of the PCM is gated with the CS signal, so only when the PCM is selected does it drive RDY. When the microprocessor accesses the data buffer or the peripherals for programmed I/O, the PCM asserts RDY low to halt the bus cycle until it can perform the access. The PCM uses the leading edge of the data strobe to trigger the access, and if the firmware is writing data, then there is a specified time from the leading edge of the strobe that write data must become available within. When the access is complete, the PCM deasserts the RDY signal and allows the bus cycle to finish.

When this bit is a one, the PCM is used in a configuration with a microprocessor that does not support wait states, and the RDY signal is normally used as a status signal to a microprocessor's PIO input pin and polled by the firmware, or the internal status of the RDY pin is polled through the PCM task file register. In this configuration, the PCM does not gate the CS signal with the internal RDY status, so the RDY status is available continuously. The PCM uses the trailing edge of the strobe to trigger the access, and as such there is no timing requirement on the write data from leading edge of strobe.

3.3 MASTER STATUS REGISTER

Address = 64H or E4H
Read/write register

7	6	5	4	3	2	1	0
DNR	0	0	PRNR	BANR	PPE	BINTR	AINTR

3.3.1 AINTR Channel A Interrupt Request Read only bit BINTR Channel B Interrupt Request Read only bit

Setting AINTR (BINTR) indicates that the channel detected a situation requiring microprocessor action. The normal use of the interrupt is that the channel has completed an operation. The interrupt bit does not indicate if the operation was completed successfully, or if it terminated because of an error. The channel interrupt bit for each channel resets when the microprocessor clears all the interrupting states in the particular channel status register. This bit represents the 'or' function of all the interrupt conditions in the channel.

3.3.2 PPE Processor Parity Error

The processor parity error bit is set when a buffer read operation from the microprocessor interface resulted in a parity error. The bit is reset by the writing a one to the PPE bit. Writing a zero to PPE does not affect this bit.

3.3.3 BANR Buffer Access Not Ready Read only bit

The PCM "buffer access not ready" status bit is used to signal the microprocessor that the PCM is currently performing an access of the buffer and the registers that are associated with the buffer are not available. When the access is complete, this bit will be reset. See also the "DNR" bit in the master status register.

3.3.4 PRNR Power Reset Not Ready (bit 4) Read only bit

The PCM "power reset not ready" status bit is used to signal the microprocessor that the PCM is currently performing a power on reset sequence, or a programmed reset sequence, and all registers in the PCM except this register are not available. When the reset sequence is complete, this bit will be reset. See also the "DNR" bit in the master status register.

3.3.5 DNR Device Not Ready (bit 7) Read only bit

The PCM "device not ready" status bit is used to signal the microprocessor that the PCM is currently performing a task that does not allow access to some resource in the PCM. The bit is essentially a logical 'or' of four conditions in the device that require multiple clock times to resolve themselves. The conditions are:

- the buffer manager reset sequence
- the microprocessor access of the buffer memory
- the microprocessor access of either of the peripheral ports for programmed I/O.

When the power is applied to the PCM, or firmware issues a soft reset, the bit sets indicating that all internal registers except this register are inaccessable. This bit will then reset when the PCM has completed its reset sequence. The "PRNR" bit in the master status register will also reflect this condition.

When the microprocessor accesses either of the peripheral ports for programmed I/O, or the microprocessor accesses the data buffer, the "device not ready" will reflect the status of the RDY pin of the PCM. This feature allows the firmware to 'poll' the PCM during these accesses when the board design or the microprocessor does not support the RDY function in hardware. The three accesses that cause this bit go to true are all independent, and can be occuring simultaneously. Because of the 'or' mechanism the bit will be false only when all accesses have completed.

When the microprocessor interface does support the RDY function, then there is no need to check this bit after the PCM has completed its reset sequence. When this bit is set because of RDY, the microprocessor is still in a wait state while the specific access is performed, and when the microprocessor is released from the wait state, then this bit is known to be reset.

3.4 BUFFER DATA LATCH

Address = 68H or E8H
Read/write register

7	6	5	4	3	2	1	0
BDL7	BDL6	BDL5	BDL4	BDL3	BDL2	BDL1	BDL0

The buffer data latch register holds the data last transferred between the microprocessor and buffer. The register is in the task file address space, so access of the register does not cause RDY to go false (no wait states). Access of the buffer data latch not cause the triggering of a buffer access.

The register is used when the board or microprocessor does not support the RDY function in hardware. Refer to the buffer access register description for specific details of the interaction of this register and the Buffer Access Register. The register is also useful for diagnostic purposes to test the PCM internal data path between the microprocessor and the internal task file.

3.5 MICROPROCESSOR ADDRESS POINTER

Address = 6EH or EEH (MP19 - MP16)
6CH or ECH (MP15 - MP08)
6AH or EAH 9MP07 - MP00)
Read/write register

7	6	5	4	3	2	1	0
0	0	0	0	MP19	MP18	MP17	MP16
MP15	MP14	MP13	MPM12	MP11	MP10	MP09	MP08
MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00

MP19 through MP00 Microprocessor Address Pointer

The Microprocessor Address Pointer is a 20-bit register/counter that supplies the address lines to the buffer memory when the microprocessor is requesting a buffer data access. These registers may be read or written when the "BANR" bit in the master status register is reset, to show or set the current RAM window. If the microprocessor accesses the buffer through the Autoincrement Access Register, then this pointer will increment after the access has been performed.

3.6 TEST ADDRESS AND STATUS REGISTER

Address = 78H or F8H
Read/write register

7	6	5	4	3	2	1	0
TAS7	TAS6	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0

The Test Address and Status register is a window into the internal logic of the PCM to allow greater visibility of the internal functioning of the device, and therefor greater test comprehensiveness.

The PMC contains an address register that can be loaded when a microprocessor write to the Test Address and Status Register occurs. This allows the selection of several internal registers and counters, and state machine registers, and the subsequent display of their content by reading this location.

This location also interacts with the Reset and Test register to invoke the test functions. Specifically there is an interlock so that test mode is more difficult to invoke, and less prone to be enabled accidently. The sequence to enable test mode is to write 80H to this register when all the test bits in the Reset and Test register are zero. This must be followed with a write to the Reset and Test register with the selected test mode (the soft reset bit must be zero). Then write F0H to this register. Once this procedure has been executed, then write the test address to this location, and read this location to view the desired internal status. When test mode is invoked, the only way to restore normal operation is to issue a soft reset, or assert the RST pin.

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3.7 RESET AND TEST REGISTER

Address = 7AH or FAH
Write only register

7	6	5	4	3	2	1	0
SWRST	0	BRST	ARST	TSMEM	CNTRT	MTPBF	MTPAF

The Reset and test register allows a software reset of the PCM device. It is important that, during the normal operation, the value written to this register is 80H. This register is also used for setting test modes and a value in this register other than 80H causes the PCM to behave unpredictably to the user. The actions that occur when the register is written with 80H are identical to those that occur during power up, and the reset sequences that are described in the reset sequences section. This register is register is initialized to 00H when either the reset input pin (RST) is asserted, or the software reset function is invoked.

3.7.1 MTPAF Microprocessor to Port A FIFO Test (bit 0)

The microprocessor to port A FIFO test is used to verify the integrity of the internal data paths from/to the port FIFO, and to allow testing of the FIFO data cells. When this bit is set, the memory controller sets the data path from the memory side of the port FIFO to the buffer access register in the microprocessor section. The port should be in loopback mode, and when the microprocessor writes or reads the buffer access register the data will be transferred from/to the port FIFO instead of the external memory. Specifically, if the port has the DIR bit set so that data is to go from memory to the peripheral, then the microprocessor would write to the buffer access register, and the data would be read back from the FIFO through the channel data latch in loop back mode. The reverse direction has the microprocessor writing to the channel data latch, and reading the resultant data in the buffer access register.

3.7.2 MTPBF Microprocessor to Port B FIFO Test (bit 1)

This is identical to bit 0 but uses the B channel.

3.7.3 CNTRT Counter Test Mode (bit 2)

When this bit is set, the 16 and 20 bit counters will be divided along 4 bit boundaries, and the carry input to these boundaries will be forced true. The example is of the Buffer Address Pointer, if it is initially set to 12345H, when an access through the autoincrement access register is made, the counter will contain as its next value 23456H. The counters affected by this bit are:

- port A address pointer
- port A transfer counter
- port A EDAC idle counter
- port B address pointer
- port B transfer counter
- port B EDAC idle counter
- buffer address pointer
- refresh address counter.

3.7.4 TSMEM Tristate Memory Interface (bit 3)

When this bit is set the control signals to the memory interface are forced to a tristate mode, to allow testing of the memory devices by an external test machine.

3.7.5 ARST A Channel Reset (bit 4)

When written with a one causes the 'A' Channel to receive a reset. This reset does not affect the memory controller, or the other peripheral channel. The reset is removed when a zero is written into the bit, or a PCM reset sequence is initiated. When a channel is receiving a reset it will have its PNRA bit in its Channel Status Register set.

3.7.6 BRST B Channel Reset (bit 5)

This is identical to bit 4 but resets the 'B' Channel.

3.7.7 SWRST Software Reset (bit 7)

When written with a one causes initiation of the PCM reset sequence. This bit is self resetting when the PCM completes the reset sequence (denoted by the PRNR bit in the master status register being cleared), and initiates the PCM reset sequence on the trailing edge of the write strobe of this register.

3.8 BUFFER ACCESS REGISTER

Address = 7CH or FCH
Read/write register

7	6	5	4	3	2	1	0
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0

The Buffer Access Register is the window that the microprocessor uses to load/store data to/from the buffer memory. The microprocessor address pointer supplies the address to/from which the RAM transfer will be made.

When the microprocessor and board design support the RDY function in hardware, (the NOWAT bit is zero), then this register passes the data through to/from the microprocessor and buffer. The leading edge of the microprocessors read or write strobe causes a "not ready" signal to the microprocessor, holding this state until memory arbitration and the actual data transfer has been accomplished. When the transfer is complete by RDY going true, then the cycle will end and the task is complete. There is no need of the buffer data latch when using the PCM in this mode.

In the case where the RDY function is not supported in the hardware, (the NOWAT bit is one), then the firmware must perform a program sequence to complete a transfer. If the microprocessor is writing data to the buffer, then it will write to this register and data will be latched along with the fact it is a write. The trailing edge of the strobe will cause the PCM to request arbitration for the buffer. The firmware is free at this time to perform other tasks, or poll the "DNR" status bit or the "BANR" in the Master Status Register, or poll the PCM RDY pin. When the access is complete then "not ready" will go false, and the firmware is again allowed to access the buffer.

If the microprocessor desires to read the buffer, then it must first read this register and discard the data. This action is only used to initiate the arbiter request, and latch the fact it is a read access. The trailing edge of the strobe will cause the buffer access to initiate. When the "not ready" condition goes false, then the data that was fetched is available in this register, and also in the Buffer Data Latch. Note that reading the Buffer Data Latch does not cause a "not ready" condition, or perform another access of the buffer, where if data is read from this register then another access will be initiated.

3.9 AUTOINCREMENT ACCESS REGISTER

Address = 7E or FE
Read/write register

7	6	5	4	3	2	1	0
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0

The autoincrement data register performs the identical function of the buffer access register with the added feature that at the end of the data transaction, the microprocessor address pointer increments to the next address.

If the firmware desires to read or write a small block of data in the buffer, then access through this register will simplify the programming sequence. When the PCM is in the "waitable" microprocessor mode, then firmware need only continuously read or write data through this register. The transfer of data to/from the buffer occurs while the microprocessor is in a wait state, and the incrementing of the Microprocessor Address Pointer occurs in the intervening time between consecutive microprocessor bus cycles. If the PCM is in the "non-waitable" microprocessor mode, then firmware must poll the "not ready" status between accesses of this register. In this mode when reading a string of bytes from the buffer, if the last byte is accessed from this register, then another buffer access will occur, and the address pointer will be incremented. If this is not desired, then the last byte read from the buffer should be read from the buffer data latch instead of from this register.

The autoincrement access register is intended for use when small blocks of data are to be moved to/from the buffer while both ports are transferring data. If a large amount of data is to be moved to/from the microprocessor it is suggested that one of the ports be used in loopback mode, to achieve the maximum data transfer rate.

4.0 DEVICE CHANNELS

Channel A Address = 40H
Channel B Address = C0H
Read/write register - not pipelined

7	6	5	4	3	2	1	0
LPBM	PPE	DKPL	RQPL	SDTC	DLY	SC1	SC0

NOTE: There is an A or B appended to each bit name corresponding to the appropriate channel.

There are two device channels that the PCM controls. The channel registers are independent and identical across the two channels. Within the PCM the channels appear as 64-byte memory spaces in the chips total address space of 256 bytes. The channels are referred to as A, and B, with channel A being the 64 bytes of address space from 00H to 3FH, channel B being the 64 bytes of address space from 80H to BFH. Because the devices attached to the channels get their address lines (if necessary) directly from the microprocessor bus the even only address characteristic of the internal registers does not apply.

The registers that control the channels, are in the 32 bytes of address space that immediately follow the respective channels address space. The registers for channel A are in the address space of 40H to 5FH. The registers for channel B are in the address space of C0H to DFH. As these registers are internal, the odd addresses in the channel's respective address blocks are just a ghost image of the registers at the even addresses.

When the controller firmware accesses a register that controls a channel, the microprocessor will not have to wait for access, because these registers are all within the PCM chip, and are always available for immediate access. When the controller firmware accesses a register in a device on a channel, the PCM must evaluate the state and mode of the channel to determine if access of the register is possible. If the PCM is the bus master, then it will arbitrate the access of the channel, and will insert wait states for the microprocessor. The number of wait states for this access is dependant upon both the strobe timing of the channel, and the arbitration time of the channel. If the PCM is in slave mode it will not attempt the access but cause an I/O error interrupt and status to occur.

The channels function is to allow access between a peripheral device and the data buffer. The characteristics of any transfer have both fixed and variable components. The fixed components are associated with the peripheral device and the hardware that will perform the transfer. These components are set at the beginning of the total transfer, and do not vary for the duration of the transfer. The variable components of the transfer are associated with the data buffer itself, and the arrangement of data, and the firmware control of the data. The fixed components are not 'pipelined', and are set by firmware at the start of a (group of) transfer(s).

The channel 'pipeline' mechanism allows firmware to control the data buffer on the fly. In applications where the firmware is attempting to either control a ring buffer or a cache, the mechanism allows the firmware to 'look ahead' to its next operation.

The registers have been organized in the order in which they would normally be programmed. It is especially important to ensure that the timing register is set up before the control register.

4.1 CHANNEL TIMING REGISTER

The channel timing register is used to control hardware actions that occur during a transfer to the external device. The action the register performs is that of controlling the pulse timing on the channel when the PCM is the bus master. This allows peripheral devices of various timing characteristics to be interfaced to the PCM. The register also defines to the channel logic specific characteristics of the external peripheral device, such as its handshake signal polarities, and parity capability.

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The firmware is only allowed to write to the channel timing register when the channel is idle. The channel state machine will set the I/O error bit in the channel interrupt status register if the channel timing register is written while the channel is busy.

All bits in the register are cleared by the reset sequence.

4.1.1 SC0(1)A (SC0(1)B) Channel Strobe Control Field

The channel strobe control field is a two bit field that is used to control the width of the read and write strobes to the peripheral devices when the channel is in modes where the PCM is the bus master (DMA), or when doing PIO operations. The width of the strobes is programmable by setting the field. When the PCM is doing DMA cycles, for values of 0,1,2,3 the strobes will be 2,4,6,8 clocks wide respectively. When the PCM is doing PIO cycles, for values of 0,1,2,3 the strobes will be 4,6,8,10 clocks wide respectively.

4.1.2 DLYA (DLYB) Delay Strobe Bit

Normally, the $\overline{CS}$ and DACK signals go active two PCM clock before the $\overline{RD}$ or $\overline{WR}$ signals. When this bit is set, this period is extended by 2 PCM clocks. The primary use of this feature is for external decoding logic if multiple peripheral devices exist on the channel.

4.1.3 SDTCA (SDTCB) Strobe Deasserted Time Control Bit

This bit is relevant when the PCM is the bus master and in burst data transfer mode, then this bit is used to control the time that the $\overline{RD}$ and $\overline{WR}$ signals are deasserted. When this bit is zero, the $\overline{RD}$ and $\overline{WR}$ strobes will be deasserted for two PCM clocks during a data burst. When this bit is one, the $\overline{RD}$ and $\overline{WR}$ signals will be deasserted for 4 PCM clocks during a data burst.

4.1.4 RQPLA (RQPLB) DMA Request Polarity Bit

This bit controls the polarity of the PCM port DRQ pin. When this bit is set the PCM will consider the DRQ pin as active high. This is true whether this pin is receiving the request when the PCM is bus master or transmitting the request when the PCM is bus slave.

4.1.5 DKPLA (DKPLB) DMA Acknowledge Polarity Bit

This bit controls the polarity of the PCM port DACK pin. When this bit is set, the PCM will consider the DACK pin as active high. This is true whether this pin is transmitting the acknowledge when the PCM is bus master or receiving the acknowledge when the PCM is bus slave. Note that both the above situations occur when EDAC redundancy byte counting is enabled.

4.1.6 PPEA (PPEB) Port Parity Enable Bit

The device port can be optionally set to check the parity on transfers to the PCM from the peripheral device. Odd parity is supported and is generated when this bit is set. When this bit is set, all reads (data going into PCM) of the device channel by the PCM (either as master or slave) will result in parity checking being done, and interrupts being generated if even parity is detected. It should be noted that **ALL** transfers, including programmed I/O, are checked if this bit is set. When the PPE bit is reset, the port parity bit will be at a logic one level when data is transferring from the PCM to the peripheral device.

4.1.7 LPBMA (LPBMB) Loop Back Mode Enable

The purpose of this bit is to enable the microprocessor to use the FIFO to speed block transfers between the microprocessor and the buffer RAM. When set, this bit paths the channel data latch to the FIFO. It inactivates the outputs of the channel ($\overline{CS}$, DACK, DRQ, $\overline{WR}$, $\overline{RD}$, and data bus). The microprocessor will appear to the channel as an external device and the channel will appear as if in slave mode. More explicitly the loopback mode sets the channel to a state of a non-pausible slave mode. In this state the microprocessor can transfer data to/from the FIFO at its maximum speed with the channel monitoring the FIFO for overrun/underrun conditions. The channel mode bits in the Channel Control Register need not be changed, but the Direction, and Interrupt Enable bits need to be programmed as if programming for an external transfer. In all other channel registers programming is as if for a

normal external transfer, with the normal pipeline mechanisms in operation. Note the Direction bit in the Channel Control Register still needs to reflect the direction of transfer to/from an external device. As such the direction bit is SET for a transfer from the buffer to microprocessor (similar to a peripheral write command), though the microprocessor issues READ cycles to access the FIFO data.

4.2 CHANNEL CONTROL REGISTER

Channel A Address = 42H
Channel B Address = C2H
Read/write register - not pipelined

7	6	5	4	3	2	1	0
SLAV	BRST	DISK	EDAC	PAUS	DIR	IVE	IBE

NOTE: There is an A or B appended to to each bit name corresponding to the appropriate channel.

Where the Timing Control Register sets the physical environment of the interface with the external device, the Channel Control Register sets the logical environment of the interface. The register contains two types of parameters about the transfer being programmed. The high order five bits are used to identify the logical protocol that the PCM is going to use to interface to the external device. The low three bits are used to set a firmware environment to control the manbagement of the transfer direction and interrupts desired.

The firmware is only allowed to write to the chanbnel control register when the channel is idle. The channel state machine will set the I/O error bit in the channel interrupt status register if the channel c ontrol register is written while the channel is busy.

Whenever the firmware writes to the channel control register, the PCM will take 10 PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

The register is initalized to A8H by the rest sequence.

4.2.1 IBEA (IBEB) Interrupt on Busy Bit

The busy interrupt bit indicates to the channel that the microprocessor desires an interrupt when the channel very busy status bit transitions from a one to a zero.

4.2.2 DIRA (DIRB) Channel Transfer Direction Bit

The channel transfer direction bit is used to inform the PCM the direction of the transfer of this channel. The PCM uses this information to determine the read/write control of the buffer. When the transfer direction bit is a zero, the device is transferring data to the buffer (device read mode, buffer write mode). When the transfer direction bit is a one, the device is transferring data from the buffer (device write mode, buffer read mode).

The transfer direction bit is used by the channel logic to position the transfer counter, and the input of the FIFO to the source of the data. When the direction bit is a zero, (data transfer from the peripheral to the buffer), the transfer counter is monitoring the device handshake signals, and the count reflects the number of bytes that remain to be transferred from the peripheral device, to the input of the FIFO. When the transfer count exhausts and the FIFO goes empty, the logic will signal the end of this transfer if EDAC mode is not

in effect. If EDAC mode is in effect, the channel will monitor the DACK pin to count EDAC trans fers, and when the EDAC idle counter exhausts and the FIFO is empty, it will signal the end of this transfer.

When the direction bit is a one, (data transfer from the buffer to the peripheral), the transfer counter is monitoring the buffer signals, and the count reflects the number of bytes that remain to be transferred from the buffer to the input of the

FIFO. When the transfer count exhausts and the FIFO goes empty, the logic will signal the end of this transfer if EDAC mode is not in effect. If EDAC mode is in effect when the FIFO goes empty, the channel will monitor the DACK pin to count EDAC transfers, and when the EDAC idle counter exhausts it will signal the end of this transfer.

4.2.3 PAUSA (PAUSB) Channel Pause Control Bit (bit 3)

The bit is used by the memory arbiter. When this port is pausible (this bit set), and the other port is non-pausible (this bit reset), then the other port will have higher priority in the memory arbiter. If this bit is set the same in both channel control registers, then priority is determined by the "AHI" bit in the option 2 register.

This bit enables the "urgent request" logic. Because it controls priority, if the highest priority port's FIFO is near to overrun/underrun condition, then an "urgent request" is sent to the arbiter to stop the other port's burst and force arbitration.

4.2.4 EDACA (EDACB) EDAC Idle Enable (bit 4)

The EDAC Idle Enable bit is used to allow the port interface to share control of the peripheral bus with the WD60C80 EDAC device. The EDAC (Error Detection And Correction) is used in disk applications to append redundancy information to data blocks to allow error correction. The bit when set will allow the PCM to strip this information and not transfer it to the buffer on reads, and to allow the EDAC to append the information to the device data on writes. The EDAC bit is only relevant when the channel is programmed to be a bus master. The Channel EDAC Idle Counter contains a count of the number of redundancy bytes to ignore between data transfers. When this bit is set the transfer counter must be programmed for a single block size. When the transfer count exhausts the channel will tri-state the DACK pin and begin to count DACK pulses until the EDAC idle counter exhausts. While the EDAC idle counter is enabled, no transfers are allowed between the port and the FIFO (the redundancy bytes transfer between peripheral and the EDAC device). When the EDAC idle count exhausts the channel will then continue normal pipeline operations if the firmware has programmed them.

4.2.5 DISKA (DISKB) Disk Type Device (bit 5); BRSTA (BRSTB) Burst Transfer Device (bit 6); SLAVA (SLAVB) Slave Mode Interface (bit 7)

These three bits are used collectively to define to the port logic the type of peripheral device it will interface with, and the protocol to use with the interface signals. The signals will be described as per their individual significance, and then their collective significance. The names are derived from relationships they assume when the bit is set.

The SLAVE bit is used to instruct the channel that the external device is the bus master, and as such will control the $\overline{WR}$ and $\overline{RD}$ interface signals. When the bit is zero, the PCM is the bus master and controls the $\overline{WR}$ and $\overline{RD}$ signals. The master/slave relationship controls whether the PCM has the capability of performing programmed I/O on the external bus. When the microprocessor attempts to do programmed I/O and the channel is in a master and non-disk mode, the channel will arbitrate the external bus and interleave the programmed I/O with the DMA transfers the external device is requesting. When the channel is in slave mode, programmed I/O is rejected. If the microprocessor attempts programmed I/O an I/O error interrupt and status are asserted.

The BURST bit defines to the channel that the multiple bytes may be transferred between the external device and the FIFO with a single iteration of the protocol pins (DRQ and DACK). When the bit is a zero then SINGLE cycle mode, where an iteration of the protocol pins result in a single byte being transferred.

The DISK bit defines to the channel that the external device is a disk formatter device, and causes the protocol pins to maintain a different protocol than the normal REQUEST and ACKNOWLEDGE. When the bit is a zero then the normal DRQ and DACK protocol is enforced. Programmed I/O is inhibited when in a disk mode.

In the following text the three bits are grouped with the ordering of SLAVA (SLAVB), BRSTA (BRSTB), and DISKA (DISKB).

4.2.6 000 DMA Single Cycle Master

In this mode, the DRQ pin is the data request and is an input, the DACK pin is the data acknowledge and an output. In this mode, the PCM is con sidered to be the bus master, and the peripheral chip is the bus slave. The peripheral device uses the DACK signal to qualify the data strobes from the PCM. The WR pin is a low true output pin from the PCM, and is active when the PCM is programmed with a channel transfer direction bit set, and the peripheral device has requested service. The WR signal is used to clock data from the PCM to the peripheral device. The RD pin is a low true output pin from the PCM, and is active when the PCM is programmed with a channel transfer direction bit cleared, and the peripheral device has requested service. The RD signal is used to clock data from the peripheral device to the PCM. The PCM will also use the WR and RD signals when the microprocessor requests programmed input/output of the peripheral device. At this time, the PCM will output the chip select signal to the peripheral device. The timing of the WR and RD signals is programmed in the timing control register of the channel.

In the Single Cycle DMA mode, the PCM will cycle the DACK signal for each byte transferred. The peripheral device can use the DACK signal to deassert its DRQ. This mode is designed to interface with older DMA style peripherals that interfaced with the Intel 8237 DMA chip. This mode will only transfer a byte when the channel FIFO is capable, therefore it is implied that overrun/underrun detection is the responsibility of the peripheral device. The channel will continue to transfer data if a parity error is detected, with the channel counters being captured at the time the error is detected. This mode is compatible with the EDAC device, and supports interleave of programmed I/O through the port and the DMA transfers.

4.2.7 001 DMA Single Cycle Disk

This mode is specifically for the ADS10C00 Disk Formatter Chip. The interface is the same as the DMA Single Cycle Master mode, in that the peripheral device requests service with the DRQ signal, and the PCM which is the bus master acknowledges the request with the DACK signal. The timing of the DACK signal is modified for the ADS10C00 requirements, with the leading edge of the DACK being returned asynchronously in response to the DRQ, and the data and trailing edge occuring synchronous to the PCM clock. In the DMA single cycle disk mode the WR and RD signals are not used. Instead the direction of data transfer is known to both the external device, and the PCM device, so the direction strobes are not required. In this mode the DACK signal is all that is required, as it acts both as an acknowledgement of data transfer, but also as the timing strobe. In this mode the PCM will attempt to transfer a byte on demand from the external device. If the channel FIFO becomes empty or full when another byte transfer is to take place, the channel will latch the data late occurance, and capture the channel counters for the firmware. The transfer will continue until the current transfer count is exhausted. If a parity error is detected during the transfer, the parity error status is latched along with the channel counters, and the transfer continues until the transfer counter exhausts. Since the ADS10C00 device supplies a seperate port for programmed I/O, then programmed I/O through the PCM port is not allowed in this mode. This mode is compatible with the EDAC device.

4.2.8 010 DMA Burst Cycle Master

This mode, tuned for the WD33C93 device, is the same as the DMA Single Cycle Master with the exception that at the end of the data strobe (either WR or RD) the DRQ signal is sampled, and if it is still active and the channel FIFO is capable of transferring another byte, the channel logic will keep the DACK signal asserted, and proceed to transfer another byte of data. This burst sequence will continue until either the external device deasserts DRQ, or the channel FIFO becomes unable to transfer another byte, or the microprocessor has requested a programmed I/O cycle on the external bus. The channel will continue to transfer data if a parity error is detected. This mode allows the highest data rate of the PCM bus master modes, but also requires the bus slave to deassert the DRQ in the shortest amount of time.

When the PCM is programmed for strobe timing of 2 PCM clocks (SC1A(B), SC0A(B) = 00), and strobe deassert time of 2 PCM clocks (SDTCA(B) = 0) then the PCM is capable of transferring data at 1/4 the PCM clock rate. This yields a transfer rate of 6.25 Mbytes per second with a 25 MHz clock to the PCM. **(DRQ deassertion time needs to be strictly followed to guarantee reliable operation.)** Since the DACK signal does not change for multiple byte bursts, this mode is incompatible with the EDAC device.

4.2.9 011 Programmed I/O Mode

This mode is used to allow programmed I/O to occur to slave devices. Since it is a master mode then programmed I/O is enabled, but since it does not specify one of the specified interface protocols of bus masters, then it will not perform any peripheral transfers, and the DACK output will remain inactive at all times. When programmed I/O is to occur in a slave such as the WD50C1X configuration, then the firmware will set this mode while programmed I/O is to occur, and set the slave mode again after the programmed I/O is complete. Note that for DMA Single Cycle Master mode, and DMA Burst Cycle Master mode, that programmed I/O requests are interleaved with the data transfers, and there is no need to set Programmed I/O mode to do programmed I/O.

4.2.10 100 Single Cycle Slave Mode

The Single Cycle Slave Mode is similar to the DMA Single Cycle Master Mode, with the sense of the master/slave relationship reversed. In this mode the PCM is assumed to be attached to a host system bus as a DMA slave device. In this mode the sense of the DRQ and the DACK pins are reversed, in that the PCM makes the DRQ pin an output, and requests data from the bus master, and the DACK pin is used by the bus master to signal the PCM that the data transaction is to take place. In this mode it is the responsibility of the bus master to drive the data strobe lines during a data transaction. This configuration is targeted for the XT* environment, and the interface is consistent with the protocol of the Intel 8237 DMA chip, when programmed as it is in that environment.

4.2.11 101 Unused and Reserved Mode

4.2.12 110 Burst Cycle Slave Mode

This mode is similar to the Single Cycle Slave Mode, with the exception that the PCM will not deassert the DRQ output signal unless the FIFO does not have the capability of accepting another byte of data.

4.2.13 111 Slave Burst Mode Disk

In this mode, the connotation of the DRQ pin and the DACK pin change. The PCM is considered to be the bus slave, and the peripheral device is considered to be the bus master. The DRQ pin in this mode becomes an input, and monitors the BDRQ of the peripheral device. The DACK pin in this mode becomes an output, and signals the peripheral device when the peripheral device can continue with its next burst of data. For this discussion, the DACK pin will be referred to as BRDY. The WR pin and the RD pin in this mode are driven by the external bus master, the disk formatter. The protocol of the DRQ and BRDY signals is meant to accomodate the WD50C1X series of disk formatter devices. If the disk formatter is reading the disk then it will transfer a sectors worth data to the FIFO and set DRQ active. It will then wait for the PCM to assert BRDY to indicate that it can proceed with the next sector transfer. If the PCM exhausts its transfer count, and the pipeline register is empty, the PCM will not assert BRDY until the channel pointers have been set for the next transfer. If the PCM has not exhausted its transfer count, or continues in a pipeline operation, then it will send BRDY to the disk formatter to let it proceed with its transfer. If the disk formatter is writing to the disk, it will assert DRQ at the start of the transfer, and wait for BRDY. The PCM will assert BRDY when the channel is started and data is available in the FIFO. At the end of the sector transfer the disk formatter will again signal with DRQ if it desires to continue. If the PCM has the proper conditions to allow the next transfer it will again send BRDY. When programmed I/O is to occur to the WD50C1X device, the firmware must first set the channels mode to master for programmed I/O, then perform the programmed I/O, then return to this mode before starting the channel. If an error occurs (either parity error or data late error) during the transfer of data, the PCM will latch the errorstatus, and the channel counters. When the disk formatter again sends BDRQ the PCM will not send the BRDY signal, effectively halting the disk formatter from proceeding. The user can

handle the error condition in one of two ways. The user can issue a stop to the channel, and clear the error, then restart the channel which will then allow the disk formatter to proceed when it sees BRDY. The user can supply external hardware to allow the firmware to reset the disk formatter, as the formatter chip is known to be in a state where write gate is not being asserted.

4.3 CHANNEL STATUS REGISTER

Channel A Address = 44H
Channel B Address = C4H
Read only register

7	6	5	4	3	2	1	0
0	0	DKST	RQST	PNR	FMT	VBSY	BSY

NOTE:There is an A or B appended to each bit name corresponding to the appropriate channel.

4.3.1 BSYA (BSYB) Channel Busy Status

The channel is currently engaged in a transfer.

4.3.2 VBSYA (VBSYB) Channel Very Busy Status

Specifically, this status bit indicates that the pipeline registers cannot be written into. One reason these registers are not available is because the channel is currently engaged in a transfer, and the pipeline registers of the transfer counter and the buffer pointers are currently loaded with the values of the next transfer.. The two status bits inform the firmware the state of the channel. When the two bits are both false, then the channel is currently idle, and the firmware can load the buffer pointer and transfer counter, and initiate an operation on the device. When the busy status is set, but the very busy status is false, the channel is in the busy state. In this state the pipeline registers are available for the firmware to load the values of the next transfer. When the firmware loads the pipeline registers and issues the start channel pulse, the channel will show very busy status. This status is the very busy state and indicates to the firmware that the channel is not available for any new pointers.

4.3.3 FMTA (FMTB) Channel FIFO Empty Status (Bit 2)

Indicates the current status of the channel FIFO.

4.3.4 PNRA (PNRB) Port Not Ready Status (Bit 3)

The PCM "port not ready" status bit is used to signal the microprocessor that the PCM is currently performing a programmed I/O access of the peripheral, and the registers that are associated with the channels programmed I/O are not available. When the access is complete, this bit will be reset. See also the "DNR" bit in the master status register. This bit is also set if the channel is currently receiving a reset.

4.3.5 RQSTA (RQSTB) Channel DRQ Pin Status (Bit 4)

In order to allow the firmware to poll the state of devices while the channel is in slave mode, the state of the channel's DRQ pin is available on this bit. The DRQ is an input which has programmable polarity. This bit DOES NOT show the actual level of the DRQ pin but rather the logical state; set if DRQ is active, and reset if DRQ is inactive.

4.3.6 DKSTA (DKSTB) Channel DACK Pin Status (bit 5)

Indicates the logical state of the channel DACK pin.

4.4 CHANNEL INTERRUPT STATUS REGISTER

Channel A Address = 46H
Channel B Address = C6H
Read and write/clear bits

7	6	5	4	3	2	1	0
AERR	IOPE	IOE	REJ	LATE	PERR	VBI	BSYI

4.4.1 BSYIA (BSYIB) Interrupt From Busy

This status bit will be set when the busy interrupt bit in the channels control register (bit 0) is set, and the channel busy status bit transi tions from a one to a zero (the channel state transitions from busy to idle). This bit is cleared when a one is written to it.

4.4.2 VBIA (VBIB) Interrupt From Very Busy

This status bit will be set when the very busy interrupt bit in the channels control register (bit 1) is set, and the channel very busy status bit transitions from a one to a zero (the channel state transitions from very busy to busy). This bit is cleared when a one is written to it.

4.4.3 PERRA (PERRB) Channel Parity Error Bit

The channel parity error bit indicates to the firmware that the channel detected a parity error during a read of data either from the dynamic RAMs, or from the peripheral device. When the channel detects a parity error, it will interrupt the microprocessor, set the channel parity error flag. The transfer will continue until the end of the current block, at which time the PCM will wait for the firmware to clear the error and restart transfers.

When the transfer direction is from the buffer to the peripheral then the error occurred in the memory, and the firmware can determine the location of the parity error by reading the current value of the channel pointer, which was captured at the time of the error. When the transfer direction is from the peripheral device to the buffer, then the error occurred on the channel external interface, and the transfer counter will determine the exact byte in error. This bit is cleared when a one is written to it.

4.4.4 LATEA (LATEB) Channel Data Late Error Bit (bit 3)

The channel data late error bit indicates to the firmware that the channel detected a data overrun/underrun error during a transfer of data to/from the channel FIFO. When the channel detects a data late error, it will interrupt the microprocessor, set the channel data late error status. The detection of the overrun/underrun condition is disabled by the channels pause bit being set. This bit is cleared when a one is written to it.

4.4.5 REJA (REJB) Channel Command Reject Error Bit (bit 4)

The channel command reject error bit indicates to the firmware that there was an attempt to start a transfer when the channel had very busy status bit set, or without clearing the channel after an error. When the channel detects this condition it will interrupt the microprocessor, and set the command reject status. The transfer will not be affected. When the current transfer finishes the channel will not perform the next transfer in the pipeline because it is assumed that the pipeline register was corrupted previous to the erroneous start. No transfer will be initiated by the erroneous

start command. This bit is cleared when a one is written to it.

4.4.6 IOEA (IOEB) I/O Error Bit (bit 5)

The channel I/O error bit indicates to the firmware that there was an attempt to do a programmed I/O cycle to a channel that was in slave mode, or the channel control register was written while the channel was busy. The I/O error does not halt a transfer in progress, or corrupt an external transfer. The status indicates to the microprocessor that the previous programmed I/O transaction did not transfer valid data, or the load of the channel control register did not take place. This bit is cleared when a one is written to it.

4.4.7 IOPEA (IOPEB) Programmed I/O Parity Error (bit 6)

The channel programmed I/O parity error bit indicates to the firmware that a parity error occurred during a programmed I/O read of the peripheral device. The detection of a programmed I/O parity error does not affect a transfer in progress if the programmed I/O cycle was interleaved with device data transfers in either the DMA Single Cycle Master mode, or the DMA Burst Cycle Master mode. This bit is cleared when a one is written to it.

4.4.8 AERRA (AERRB) Any Error Bit (bit 7)

The Any Error status bit is a read only bit, and is the logical 'or' of the five error status bits. It is provided for convenience to the firmware to easily determine if the previous operation was successful.

sistor through an option jumper to either V_{CC} or GND will passively pull the data line to the desired signal level. The PCM will latch the state of the data bus lines at the end of its reset sequence, so there is a minimum of 5 µs. plus 16 PCM clocks for the resistor to pull the signal to an acceptable level. The value of the resistor is derived from the reset sequence time, and the capacitance of the data lines. The maximum resistor value should be used to reduce the DC and AC loading of the data lines. Since the channel data latch is used for other functions, it is a requirement of the firmware that if the reset status is to be saved, that the firmware must read the channel data latch and save it in its local memory before attempting either programmed I/O to/from the external device, or to put the channel in loopback mode.

4.5 CHANNEL DATA LATCH

Channel A Address = 48H
Channel B Address = C8H
Read / write register

7	6	5	4	3	2	1	0
CDL7	CDL6	CDL5	CDL4	CDL3	CDL2	CDL1	CDL0

NOTE: There is an A or B appended to each bit name corresponding to the appropriate channel.

The Channel Data Latch holds the data associated with 3 different functions performed on the channel. The access of the register does not cause a wait condition.

The first function is that of the "Reset Status Latch." When the PCM is reset either by power being applied, or by writing into the PCM reset register, the PCM samples the channel bus and saves the data in the channel data latch for the firmware. The intent is that the board designer will install passive resistor networks that allow option jumper status to be reflected on the channel bus at reset time. There is an assumption here that the external device will tri-state the channel data bus bits during the power reset condition. With the PCM and the external device both tri-state, a resistor through an option jumper to either V_{CC} or GND will passively pull the data line to the desired signal level. The PCM will latch the state of the data bus lines at the end of its reset sequence, so there is a minimum of 5 µs plus 16 PCM clocks for the resistor to pull the signal to an acceptable level. The value of the resistor is dereived from the reset sequence time, and the capacitance of the data lines. The maximum resistor value should be used to reduce the DC and AC loading of the data lines. Since the channel data latch is used for other functions, it is a requirement of the firmware that if the reset status is to be savbed, that the firmware must read the channel data latch and save it in its local memory before attempting either programmed I/O to/from the external device, or to put the channel in loopback mode.

The second function of the channel data latch is for the loopback mode of the channel. In the loopback mode the microprocessor will read data from this latch, and write data to the latch without wait states. The channel logic will transfer the data between the latch and the FIFO, and check for overrun conditions. See also the "LPBMA" ("LPBMB") bit in the Channel Timing Register.

The third function is that of the port programmed I/O data latch. When the "RDY" function is supported in hardware, then programmed I/O proceeds through the normal address space reserved for external peripheral I/O. The leading edge of the microprocessors read or write strobe causes a "not ready" signal to the microprocessor, holding this state until arbitration for the peripheral port and the actual data transfer has been accomplished. When the transfer is complete by RDY going true, then the cycle will end and the task is complete. In this case this register is not used, though it still performs its intended function of capturing the programmed I/O data to/from the peripheral.

In the case where the RDY function is not supported in the hardware, then the firmware must perform a program sequence to complete a transfer. If the microprocessor is writing data to the port, then it will write to the programmed I/O data space, and data will be latched along with the fact it is a write. The trailing edge of the strobe will cause the PCM to request arbitration for the channel. The firmware is free at this time to perform other tasks, or poll the "DNR" status bit or the "PNRA" ("PNRB") in the Channel Status Register, or poll the PCM RDY pin. When the access is complete then "not ready" will go false, and the firmware is again allowed to access the channel for programmed I/O.

If the microprocessor desires to read the channel, then it must first read from the programmed I/O data space, and discard the data. This action is only used to initiate the arbiter request, and latch the fact it is a read access. The trailing edge of the strobe will cause the buffer access to initiate. When the "not ready" condition goes false, then the data that was fetched is available in this

register, and also in the programmed I/O data space. If the data is then read from the programmed I/O data space, then another programmed I/O cycle will be initiated, while if the data is read from this register, another programmed I/O access will not take place.

4.6 CHANNEL BUFFER POINTER

Channel A Address = 4EH (BP19 - BP16)
Channel A Address = 4CH (BP15 - BP08)
Channel A Address = 4AH (BP07 - BP00)
Channel B Address = CEH (BP19 - BP16)
Channel B Address = CCH (BP15 - BP08)
Channel B Address = CAH (BP07 - BP00)
Pseudo-read/write registers

7	6	5	4	3	2	1	0
0	0	0	0	BP19	BP18	BP17	BP16
BP15	BP14	BP13	BP12	BP11	BP10	BP09	BP08
BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00

NOTE: There is an A or B appended to each bit name corresponding to the appropriate channel.

BP19A (BP19B) through BP00A (BP00B) Buffer Pointer Address Bits

The channel buffer pointer is composed of three registers that contain the 20 bit memory address of the data. The actual hardware that mechanizes the buffer pointer is a presettable 20 bit counter, which is the actual pointer, a 20 bit holding register connected to the preset inputs of the counter (the pipeline register), and a 20 bit latch connected to the outputs of the counter for reading the counter. The microprocessor can actually only load the pipeline register from its data bus. When the firmware writes to any of the bytes in the buffer address pointer, a flag in the PCM is set to remember that the pipeline register was written. The channel state machine will use this flag to indicate that the buffer address pointer is to be loaded with a new value. When the channel state machine enters the "busy" state it will test and clear the flag, and load the counter from the holding register if the flag was set. See also the description of channel "states" in the Channel Start Register.

If the channel enters the "busy" state and the flag is cleared, indicating that firmware did not load the pipeline register, then the counter continues from its current position. The firmware then can mechanize a ring buffer system with only the firmware overhead of writing the starting address at the initial transfer, and then only issuing start commands for succeeding transfers. The data will then appear as a single large contiguous block. If data is to be transferred from discontiguous areas of the data buffer as in a cache buffer system, then the firmware has the added overhead of writing the next address to the pipeline register for each transfer segment that is not contiguous.

If the microprocessor desires to read the counter while it is active, the firmware must first write to the capture pointer register, which will make a copy of the counter at the time, and the microprocessor can then read the 3 bytes of address without any sampling errors. When the channel detects an error during a transfer it will copy the counter to the capture latch register for reading. When the channel transitions to the idle state, and the previous operation had no error, the address pointer is automatically copied to the capture latch register for reading.

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4.7 CHANNEL TRANSFER COUNTER

Channel A Address = 52H (TC15 - TC08)
Channel A Address = 50H (TC07 - TC00)
Channel B Address = D2H (TC15 - TC08)
Channel B Address = D0H (TC07 - TC00)
Pseudo-read/write registers

7	6	5	4	3	2	1	0
TC15	TC14	TC13	TC12	TC11	TC10	TC09	TC08
TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00

TC15 through TC00 Transfer Counter Bits

The channel transfer counter appears as a read/write register, but in fact it is a write only register, and a read only counter. When the firmware writes to the transfer counter it is writing to a pipeline register. When the transfer counter is read, it is reading a capture latch that is loaded from the actual counter. The reason for this mechanization is that the pipeline register needs to hold the byte count of the transfer, and to load this value into the counter each time the channel begins an operation. This value only need change when the firmware requires a different granularity of data. When the channel detects an error, both the address pointer and the transfer counter are captured. The data that the firmware requires is how far into the transfer the operation proceeded before the error was detected. When the firmware reads the actual counter, the value is the residual count of the number of bytes that are left in the transfer, and from this information the firmware can deduce the number of bytes that transferred sucessfully. The firmware can also sample the current transfer counter by writing to the Channel Pointer Capture Register.

The channel transfer counter is composed of two registers that contain the 16 bit value that is the number of data bytes of the current transfer. The actual hardware that mechanizes the transfer counter is a presettable 16 bit down counter, which is the actual counter, and a 16 bit holding register which is the pipeline. The counter is unidirectional going from number of bytes that is desired to be transferred, to zero. The microprocessor can actually only load the pipeline register from its data bus.

When the Channel Start Register is set, and the channel is currently idle, then the channel state machine will load the transfer counter from the pipeline register, and start the operation. At this time the pipeline register is now free, and the firmware can load the transfer count of the next transfer into the pipeline register.

It should be noted here that for most devices that are envisioned, the block size that will be entered into the transfer counter, will be the sector (frame, etc.) size of the attached block oriented device and from that time the firmware will probably not load the transfer counter pipeline register. Hence if the firmware starts the channel again, the transfer counter will continually be updated with the block size of the device, without the firmware repeatedly loading the value on each transfer. The transfer count can be multiples of the device block size, if the firmware desires to cluster blocks together and view them as larger data items. A special case exists when EDAC Idle Enable control bit is set in the Channel Control register, in that the transfer counter is used to count the number of bytes between redundancy fields, and therefore can not be multiples of the block size.

4.8 CHANNEL START REGISTER

Channel A Address = 54H
Channel B Address = D4H
Write onlyregister

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel start register, the PCM will take ten PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

Under normal conditions the PCM will have the channel enabled before the device is armed for a transfer. The exception to this is likely to be a programmable device that requires the PCM to be the bus slave (eg. WD501X type devices). In that case the mode will have to be changed to slave after the firmware has set up the device, as there is no programmed I/O facility in slave mode. It should be noted that once the operation of the peripheral device has been started, it may assume master status at any time, and as such, can fight the PCM if the firmware does not enter slave mode before this happens. Also, delay in starting the transfer by writing to this register, may result in over/underrun errors in the peripheral device. Writing into the channel start register will produce varied responses from the channel, depending upon the current mode and state of the channel.

When the channel is in the idle state (busy and very busy status are both cleared), and the firmware writes into the channel start register, this indicates to the channel that the firmware desires the channel to begin operations. The channel state machine will load the transfer counter from the transfer counter pipeline register, and if the channel buffer address pointer pipeline has been written into, it will load the buffer pointer from the pipeline register, the flag for the address pointer will be reset, and channel busy status will set. When the busy status is set the pipeline registers are now available for the firmware to write the parameters of the next transfer.

When the channel is in the busy state (busy status set, and very busy status cleared), and the firmware writes into the channel start register, this indicates to the channel that the firmware desires the channel to continue operations when the current operation finishes. The channel very busy status will set. When the very busy status is set the pipeline registers are not available for the firmware to write. The channel is now considered to be in the very busy state. The channel will clear the very busy status and exit the very busy state when the current transfer completes. When the transfer completes the channel state machine will advance to the busy state and perform the same sequences that are described going from idle to busy. The channel counters are now set with values for the new transfer and the pipeline registers are again available for the firmware to queue the parameters of another transfer and issue another start.

When the channel is in the very busy state (busy and very busy status are both set), and the firmware writes into the channel start register, this will cause the channel to set the command rejected status and terminate operations on the channel when the current transfer completes. The channel state machine assumes that the firmware has corrupted the values in the pipeline when it issued the last start command. When the current operation completes the channel state machine will stay in the command reject error state until a channel stop is issued, which will then bring the state machine back to idle.

Finally, any attempt to start a channel with an uncleared error will result in a command reject error.

4.9 CHANNEL STOP REGISTER

Channel A Address = 56H
Channel B Address = D6H
Writeonly register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel stop register, the PCM will take ten PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

4.10 CHANNEL POINTER CAPTURE REGISTER

Channel A Address = 58H
Channel B Address = D8H
Write only register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel pointer capture register, the PCM will take ten PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

When channel pointer capture register is written into, the capture latches for the channel pointer and channel transfer counter will sample the current state of the counters. This allows the microprocessor to detect the current position of the pointer and counter while they are active.

4.11 EDAC IDLE COUNTER

Channel A Address = 5AH
Channel B Address = DAH
Pseudo-read/write register

7	6	5	4	3	2	1	0
EC07	EC06	EC05	EC04	EC03	EC02	EC01	EC00

In order for the PCM to function with an external Error Detection and Correction device (EDAC), it is necessary for the PCM to be able to ignore (or "idle") while data transfers intended for or generated by the EDAC device transpire. To this end, each channel has an 8 bit down counter called the EDAC idle counter. It is mechanized by an 8-bit holding register that is loaded by the microprocessor with the number of bytes that should be ignored at the end of each block transferred, and an 8-bit down counter, decremented on the trailing edge of DACK once the PCM has finished its transfer. This counter is not latched like the address pointers and transfer counters, so any attempt to read this counter while it is running may result in synchronization errors. This value need only be set, to suit the EDAC device being used, after a reset condition. Thereafter the EDAC mode can be enabled and disabled using the EDAC Idle Enable Bit in the Channel Control Register.

4.12 LONGITUDINAL REDUNDANCY CHECKING REGISTER

Channel A Address = 5CH
Channel B Address = DCH
Read/write register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Both A and B channels must operate as the bus master when using the LRC feature. LRC generation and checking takes place between the channel data bus input and output buffers and the channel FIFO. The LRC calculations do not include the parity bit.

An LRC error on a transfer from the buffer memory to the peripheral causes the WD60C40A to force a parity error on the last data byte to the peripheral. Because of the timings required for this feature, the LRC byte does not go through the FIFO on these transfers.

Enabling the LRC option splits the existing 16-bit transfer counters into 12-bit block counters and 4-bit modulo counters. The WD60C40A effectively breaks up a transfer into several blocks, and each block has its associated LRC byte. The programmed value of the block counter specifies the length of these blocks, and the value in the modulo counter plus one indicates the number of blocks which make up the entire transfer, allowing up to 16 blocks per Channel Start.

The host has both read and write access to the LRC register to facilitate aborting transfers and subsequently resuming them. Since the LRC is calculated as the data enters the WD60C40A channel, the LRC byte after a Channel Stop includes the calculations for any data left in the WD60C40A FIFO. The host assumes responsibility for adjusting the LRC register to account for any data left in the peripheral device FIFO to ensure a correct LRC byte for the entire data block. Writing to the LRC register disables the normal zeroing of this register by the Channel Start command, enabling the host to resume the aborted transfer.

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5.0 MICROPROCESSOR INTERFACE

The PCM interface to the controller microprocessor is designed to be compatible with microprocessors of the multiplexed address/data bus design. It is specifically targeted to interface to Intel 80186 microprocessor with no external logic, but with some external logic the PCM can interface to other microprocessors that have multiplexed buses, or to non-multiplexed bus microprocessors. Speed penalties will exist for these implementations.

The PCM appears to the microprocessor as a contiguous address space of 256 bytes. The 8 bit address that decodes the unique location within the PCM is supplied by 8 multiplexed address/data pins. The address bit 0 is however ignored as all internal registers are mechanised to appear on even byte boundaries to suit the 80186. The PCM latches the address during the ADDRESS LATCH ENABLE signal. The 8 bits are used as both address information at ALE time, and data information at all other times. The PCM latches the bus address on all microprocessor cycles, but only responds to those cycles that are accompanied by the chip select signal. This signal is derived by the controller designer by doing a decode of the address information above bit A07, or using the already decoded outputs of the 80186. The controller designer has the flexibility to map the PCM's address space into the microprocessors memory space, or the I/O space, or a combination of both.

The PCM's interface includes a general interrupt signal to inform the microprocessor of changes of states of status within the PCM, and two signals to control the direction and timing of microprocessor bus cycles that involve the PCM. There are also two signals that allow the PCM to synchronize resource sharing for the microprocessor. When the PCM detects a bus cycle within its address range (chip select asserted), it decodes the address that it has latched, and determines the resource that is to be accessed. The PCM has control of four general resources (internal registers, buffer memory, channel A, and channel B), and maps these resources into the address space.

The microprocessor interface deviates at this point depending upon the microprocessor that is interfaced, and the microprocessor and board design to support the READY/WAIT signal. In the case where the microprocessor and board design support the RDY function, the PCM uses the microprocessor RDY line to hold the microprocessor in a wait condition if the resource is not ready for immediate access. The internal register set of the PCM does not insert any wait states. The access of the other resources may or may not insert wait states.

If the microprocessor is accessing a device on one of the peripheral device channels, the local bus arbitrator for that channel will deassert RDY to the microprocessor until the channel is free for the microprocessor access to proceed. When the channel has been acquired the PCM will assert CSA or CSB (peripheral chip select) to select the peripheral device. When the access of the peripheral device is finished, the PCM will assert RDY, which will allow the microprocessor to proceed. If the access of the peripheral channel results in an I/O error, there will be no wait states inserted. If the microprocessor is accessing the buffer RAM, the memory arbiter will deassert RDY to the microprocessor until the buffer access has been done.

In the case where the microprocessor or the board design does not support the RDY function, the previously described actions to initiate the PCM function are identical. The difference is when the PCM deasserts the RDY function. In this case the microprocessor will not go into a wait condition, and is free to continue executing code. Internally, the PCM latches the access initiated, and the direction of the access, and proceeds to complete the access without holding the microprocessor. Data latches in each port and the buffer area will hold the data for the microprocessor while the access is in the arbitration queue. The microprocessor now has the responsibility of testing status (either in a PCM internal register, or the RDY signal), and when the access is complete, and to fetch the accessed data if the access was a read.

6.0 I/O MEMORY MAP

The PCM has within it four resources that the controller's firmware can access. The first resource is the PCM's register file. This consists of various registers that the firmware can read and write to both control the operation of the PCM, and sense the status of operations. The registers that are associated with a particular channel, are in an address space that is adjacent to the channel, and registers that are not associated with a particular channel use a partial decode of addressing so they are made to appear in both channels address space. Since these registers are dedicated to the microprocessor, there is no arbitration required to access these registers, and bus cycles to these registers involve no wait states.

The second resource that the PCM controls is the memory array. The memory array is made to appear to the firmware as a single memory location. The access to the actual memory location must be arbitrated along with accesses from the two peripheral channels, so access to the buffer memory may encounter some significant delays when there is heavy buffer traffic. The addressing of the memory array can either be static by loading the microprocessor page register, or can be made to autoincrement when searching through the data buffer.

The other two resources that the PCM controls are the device buses. The two device buses are made to appear as 64 byte spaces. Channel A devices appear in the offset range of 00H to 3FH. Channel B devices appear in the offset range of 80H to BFH. The actual registers that can be accessed through the channel, and the locations that they are made to appear at are under control of the board designer.

FCH	DATA BUFFER
E0H	BUFFER MGR. REGISTERS
C0H	CHANNEL B REGISTERS
80H	CHANNEL B
7CH	DATA BUFFER
60H	BUFFER MGR. REGISTERS
40H	CHANNEL A REGISTERS
00H	CHANNEL A

7.0 INTERRUPTS

All interrupt conditions within the PCM are grouped into a single interrupt line going out of the WD60C40A. Individual interrupt conditions can be enabled/disabled within the PCM, but there is no prioritization of interrupts within the device. Interrupt conditions are reset when the firmware writes a one to the bit to clear the particular interrupt condition.

8.0 RESET SEQUENCES

The PCM chip will be initialized when the $\overline{RST}$ pin is asserted, or the firmware writes a one into the soft reset bit of the PCM reset register. When the PCM is reset, it aborts all transfers, sets channel control registers to 00 and tri-states the port's control lines ($\overline{RD}$, $\overline{WR}$, DRQ, $\overline{DACK}$), disables refresh by resetting the RAM control logic to a special state, and clears all interrupts. The firmware is responsible for setting up refresh and initializing the RAM to suit the dynamic RAM requirements. Resetting the PCM terminates access of the dynamic RAM array, allowing the idle time requirement of dynamic RAMs at power on. When the PCM option register is written to, this signals the PCM that the idle time requirement of the dynamic RAM array has passed, and the PCM will begin refresh cycles if refresh is enabled, it is the requirement of the controller firmware to delay the required idle time interval from power on condition before writing into the PCM's option register, to delay the required time interval from enabling refresh until the dynamic RAMs are ready for operation, and to initialize the memory array to proper parity. The PCM is initialized to static RAM mode by master reset. When the PCM is reset, the memory signals will be deasserted, and the channel control signals will all be tri-state. The memory signals will return to normal operation when the firmware writes into the option register. The channel signals will return to normal operation when the firmware writes into the channel control register. It should be noted that programmed I/O to the peripheral port can not be performed until the channel control register is written as master mode after a reset.

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9.0 READY SEQUENCES AND LATENCIES

The RDY (ready) signal will be asserted low when the PCM has an internal resource that is unavailable to the firmware. Then time that the signal will be asserted depends upon the mode that the microprocessor interface is in, and the resource that is being accessed. When the PCM is in the 'waitable' microprocessor mode, the RDY signal will assert low when the internal address decode with CS selects a resource. The resource will start its access three PCM clocks after the microprocessor's data strobe asserts. When the PCM is in the 'non-waitable' mode, the RDY signal will assert low 30 ns. after the microprocessor's data strobe ends. The resource will start its access after the three PCM clocks for synchronization. These times are in addition to the following discussion which describes the components that determine the time of the particular access.

When the firmware accesses the buffer, the time the access takes is dependant upon the microprocessor's placement in the memory arbitration scheme, and any latency associated with its request occuring while a port data burst is in progress. The microprocessor is the highest priority device in the memory arbitration scheme, since it is a single cycle device, and its request period can be controlled by the firmware. The latency associated with a port data burst is found from the equation:

TBRST = 2 (N) + 4 (P+1) expressed in PCM clocks

N = number of bytes in the ports burst

P = number of RAS cycles occuring during the burst, or # of page boundaries crossed during burst.

Example: If the port transfers 22 bytes during the burst, and crosses a page boundary, then the total burst will require 52 PCM clocks. For a PCM clock frequency of 16 Mhz. this will be a time of 3.25 microseconds.

The N factor in the above equation depends upon the number of bytes in the FIFO when the burst begins, and the memory transfer rate, and the peripheral transfer rate. The value of N should be determined by simulation but an estimation can be made from the equation:

N = MTR (IFBC) / (MTR - PTR)

MTR = memory transfer rate, 1/2 PCM clock frequency

PTR = peripheral transfer rate, (in MHz)

IFBC = initial FIFO byte count at start of burst

NOTE:

IFBC is in the range of 0 to 15 for WD60C40

The memory transfer rate when the port is in a burst is two PCM clocks per byte. If the PCM is supplied with a 16 MHz clock, then the memory trans fer rate will be 8 MHz (8 Mbytes/second). The peripheral transfer rate is supplied in the same terms as the memory transfer rate. As an example the WD33C93A SCSI interface peripheral is capable of a transfer rate of 4 Mbytes/second, or 4 MHz. The FIFO size in the PCM is 15 bytes. If these values are applied to the equation, and use the value of 14 bytes for the initial FIFO condition, the result is 29 bytes for the expected burst. At the memory transfer rate of 8 Mbytes per second, this would yield a burst time of 3.625 microseconds.

It can be seen that as the peripheral transfer rate approaches the memory transfer rate, the denominator of the equation approaches zero, and the size of the burst increases rapidly. Therefore if the PCM is designed into a system with the peripheral transfer rate very close to the memory transfer rate, large microprocessor buffer access times can be expected. The size of burst is limited by the refresh mechanism of the PCM. The PCM will queue up to four refreshes, and then force an ar bitration, which the microprocessor will win because it is highest priority. In a system that has refreshes programmed at the normal rate of 15.6 microseconds, this effectively limits the maximum burst and the maximum latency to about 62 microseconds.

10.0 NON-CHANNEL REGISTERS MAP

7	6	5	4	3	2	1	0	REGISTER/ ADDRESS
MPAR	CAW1	CAW0	SRAM	RRC3	RRC2	RRC	RRC0	OPT 60H or E0H
0	0	NOWAIT	WAITE	AHI	INTE	BINTE	AINTE	OP2 62H or E2H
DNR	0	0	PRNR	BANR	PPE	BINTR	AINTR	MSR 64H or E4H
0	0	0	0	0	0	0	0	66H or E6H
BDL7	BDL6	BDL5	BDL4	BDL3	BDL2	BDL1	BDL0	BDL 68H or E8H
MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	MAP 6AH or EAH
MP15	MP14	MP13	MP12	MP11	MP10	MP09	MP08	6CH or ECH
0	0	0	0	MP19	MP18	MP17	MP16	6EH or EEH
TAS7	TAS6	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0	TAS 78H or F8H[1]
SWRST	0	BRST	ARST	TSMEM	CNTRT	MTPBF	MTPAF	RTR 7AH or FAH
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0	BAR 7CH or FCH
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0	AAR 7EH or FEH

NOTES
All "odd" addresses willl access the "even" address that is one lower.
[1]Contents of addresses 70H (or F0H) through 76H (or F6H) must be written as 00 and read as 00.

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11.0 CHANNEL REGISTERS MAP

7	6	5	4	3	2	1	0	REGISTER/ ADDRESS
LPBM	PPE	DKPL	RQPL	SDTC	DLY	SC1	SC0	CTR 40H or C0H
SLAV	BRST	DISK	EDAC	PAUS	DIR	IVE	IBE	CCR 42H or C2H
0	0	DKST	RQST	PNR	FMT	VBSY	BSY	CSR 44H or C4H
AERR	IOPE	IOE	REJ	LATE	PERR	VB1	BSY1	ISR 46H or C6H
CDL7	CDL6	CDL5	CDL4	CDL3	CDL2	CDL1	CDL0	CDL 4BH or C8H
BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00	CBP 4AH or CAH
BP15	BP14	BP13	BP12	BP11	BP10	BP09	BP08	4CH or CCH
0	0	0	0	BP19	BP18	BP17	BP16	4EH or CEH
TC07 TC15	TC06 TC14	TC05 TC13	TC04 TC12	TC03 TC11	TC02 TC10	TC01 TC09	TC00 TC08	CTC 50H or D0H 52H or D2H
0	0	0	0	0	0	0	0	CST 54H or D4H
0	0	0	0	0	0	0	0	CSP 56H or D6H
0	0	0	0	0	0	0	0	CCP 58H or D8H
EC07	EC06	EC05	EC04	EC03	EC02	EC01	EC00	CEC 5AH or DAH
0	0	0	0	0	0	0	0	Reserved 5CH or DCH
0	0	0	0	0	0	0	0	Reserved 5EH or DEH

NOTE:
There is an A or B appended to each bit name corresponding to the appropriate channel.

12.0 DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Supply	V_{CC}	4.5	5.5	V
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Ouptut Low Voltage I_{OL} = 2.0 mA	V_{OL}		0.4	V
Output High Voltage, IOH = 400 µA	V_{OH}	2.8		V
Leakage Current Low	I_{LL}		10	µA
Leakage Current High	I_{LH}		-10	µA
Supply Current	I_{CC}		100	mA
Power Dissipation	PD		500	mW

The output loading depends on the pin function and are as follows:

IOL	IOH	SIGNAL NAME
6 mA	-2.5mA	AD7 to AD0
2 mA	-1.0 mA	CSA, CSB DRQA, DRQB DACKA, DACKB ARD, BRD AWR, BWR DBA7 to DBA0, DBAP DBB7 to DBB0, DBBP RB7 to RB0, RBP BA9 to BA0 RAS, CAS, W
6 mA	O.D.	RDY PINT

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13.0 MISCELLANEOUS CHARACTERISTICS

Operating Temperature	0^{o} to 70^{o} C
Absolute Maximum Ratings	All voltages referenced to V_{SS}
V_{CC}	7.0 Volts
Voltage to any pin	-0.3 to V_{CC} + 0.3 Volts
Storage Temperature	-40^{o} to $+125^{o}$ C

NOTE:

Maximum limits indicate the point where permanent device damage occurs. Continuous operation at these limits is not intended, and should be limited to those conditions specified in Electrical Characteristics sections.

14.0 TIMING SPECIFICATION

In these timing diagrams the following assumptions have been made:

(1) As port B is identical to port A, only port A timings need be shown.

(2) The DRQA signal has been programmed as active HIGH.

(3) The DACKA signal has been programmed as active LOW.

(4) The timing specifications assume the following loading on each pin.

MAX LOADING	PIN NAMES
120 PF MAX	BA9 to BA0 RB7 to RB0, $\overline{RB}$P RAS, CAS, $\overline{W}$
100 PF MAX.	AD7 to AD0
50 PF MAX.	CSA, CSB DACKA, DACKB ARD, BRD AWR, BWR DBA7 to DBA0, DBAP DBB7 to DBB0, DBBP RDY PINT

The timing diagrams use the following nomenclature:

REF

The Reference number on the timing waveform diagram.

NAME

Abbreviated Symbol by which the timing is referred.

DESCRIPTION

Description of the timing referred.

REFERENCE

The reference edge to which the timing is specified.

LE = Leading edge

TE = Trailing edge

RE = Rising edge

FE = Falling edge

IC = Initial Condition

R/S

Classification of requirement/specification.

R = Requirement of the external circuit.

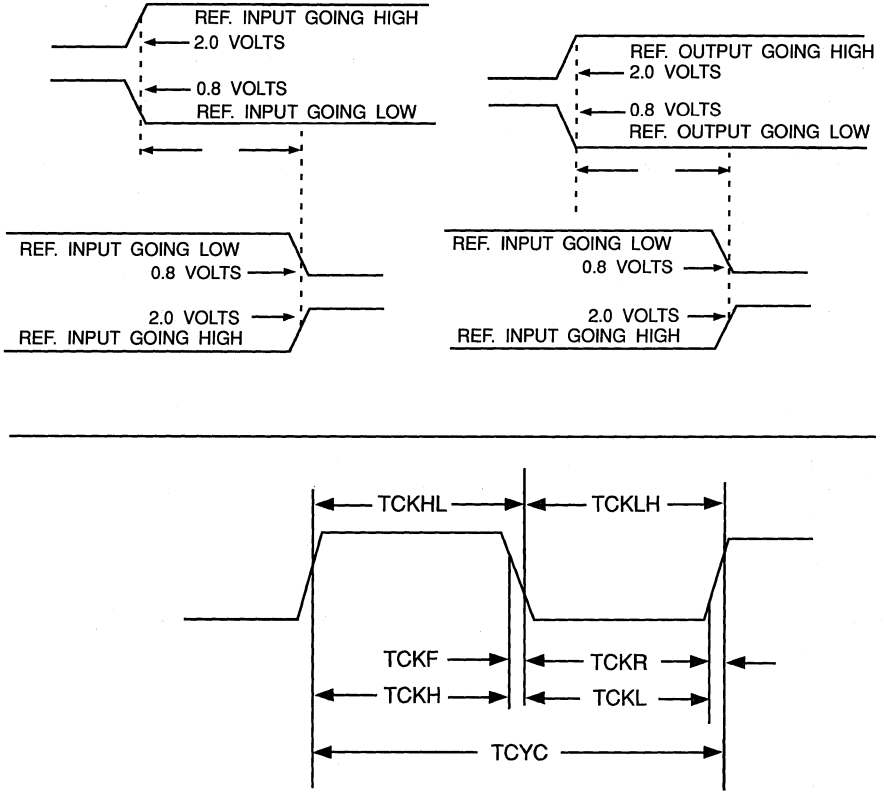
S = WD60C40 output timing specification.

TIMING

Value, unit, and characteristic of timing.

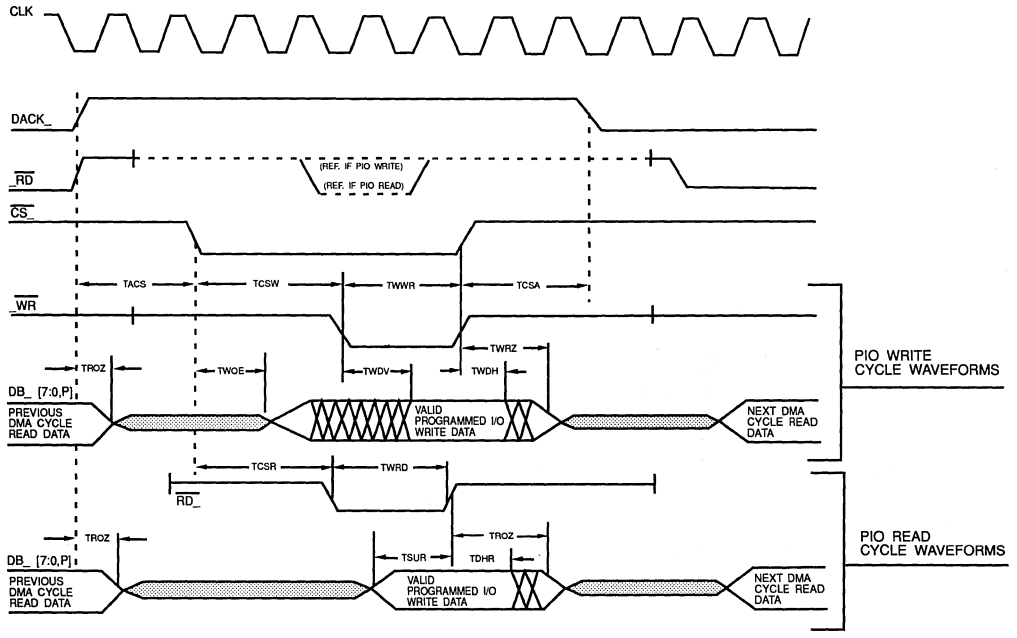
AC TIMINGS

** RAM PORT VIL = 0.8 VOLTS, VIH = 2.4 VOLTS
VOL = 0.8 VOLTS, VOH = 2.4 VOLTS



NAME	REF	R/S	MINIMUM	MAXIMUM
TCYC = Input Clock Period		R	40 NS	
TCKL = Input Clock Low		R	17 NS	
TCKH = Input Clock High		R	17 NS	
TCKR = Input Clock Rise		R		5 NS
TCKF = Input Clock Fall		R		5 NS
TCKHL = Input Clock High to Low		R	20 NS	
TCKLH = Input Clock Low to High		R	20 NS	

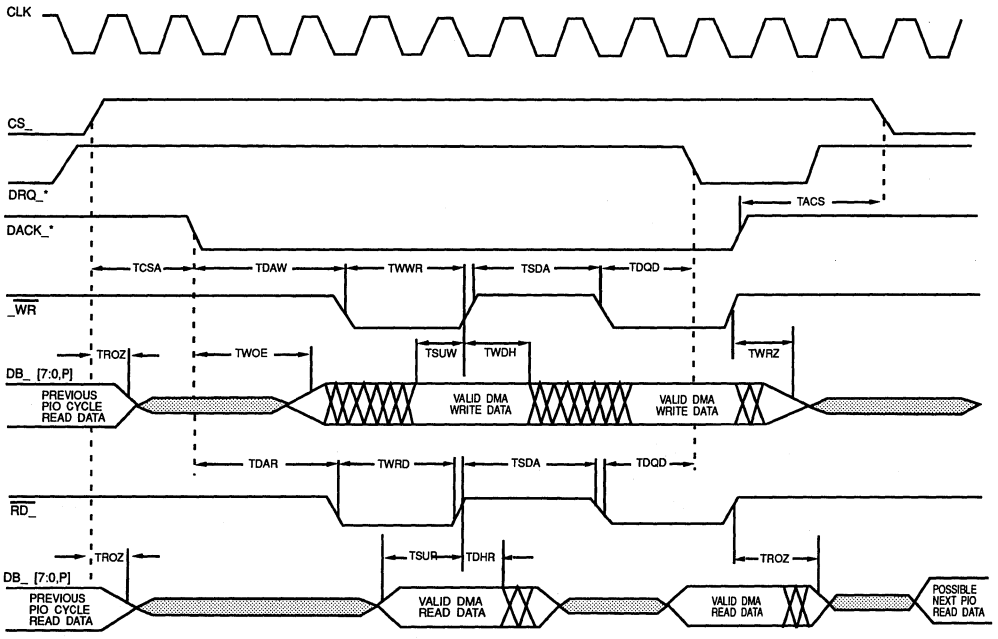
FIGURE 14-1. RISE/FALL AND MISC. TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TCSW = Chip Select to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	4 TCYC - 15 NS	10 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TWDV = Time to Data Valid in Write	LE	S		40 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TCSR = Chip Select to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	4 TCYC - 15 NS	10 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **

** If SDTC in Section 4.1 is set, then value is 4 TCYC

FIGURE 14-2. PIO READ/WRITE OF EXTERNAL DEVICES



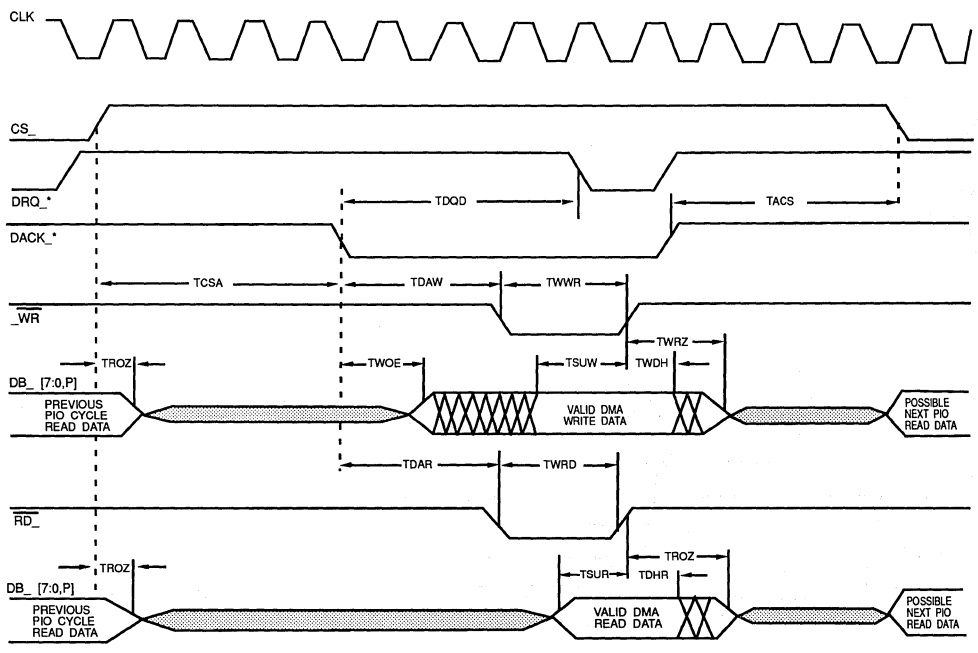
NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS

* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

FIGURE 14-3. DMA BURST MODE TRANSFERS



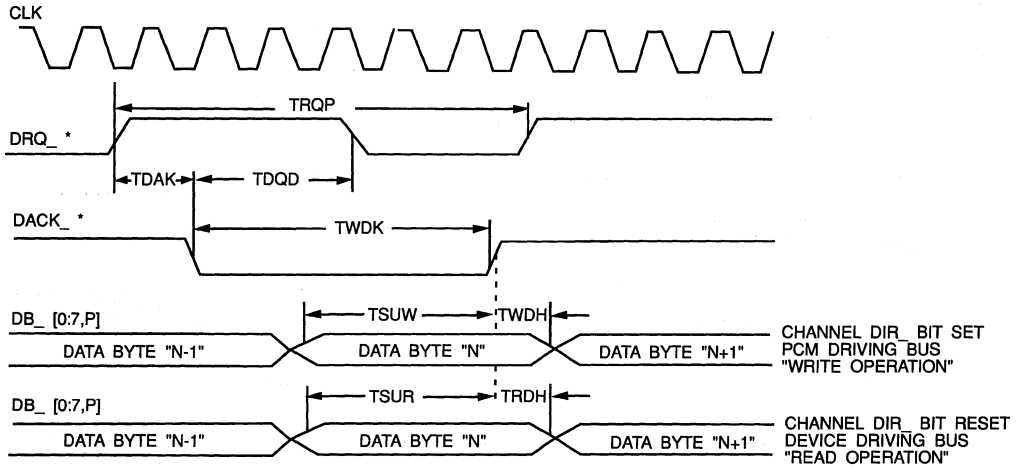
NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS

* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

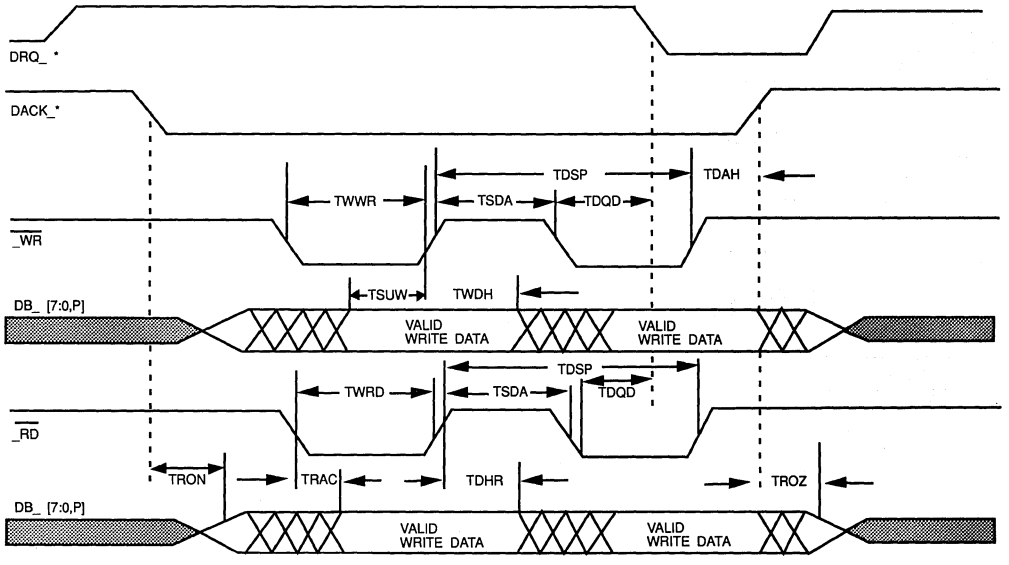
FIGURE 14-4. DMA SINGLE CYCLE MODE



NAME	REF	R/S	MINIMUM	MAXIMUM
TDAK = Time DRQ to Acknowledge	LE	S		35 NS
TDQD = Time to DRQ Deasserted	LE	R		3 TCYC
TRQP = Time of Request Period		R	6.5 TCYC	
TWDK = Width of DACK Signal		S	3.5 TCYC	5.5 TCYC + 15 NS
TSUW = Data Setup Time of Write Data	TE	S	2 TCYC - 40 NS	
TWDH = Data Hold Time of Write Data	TE	S	TCKH - 5 NS	
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	

* DRQ polarity shown high true; DACK polarity shown low true
** If SDTC in Section 4.1 is set, then value is 4 TCYC
*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state

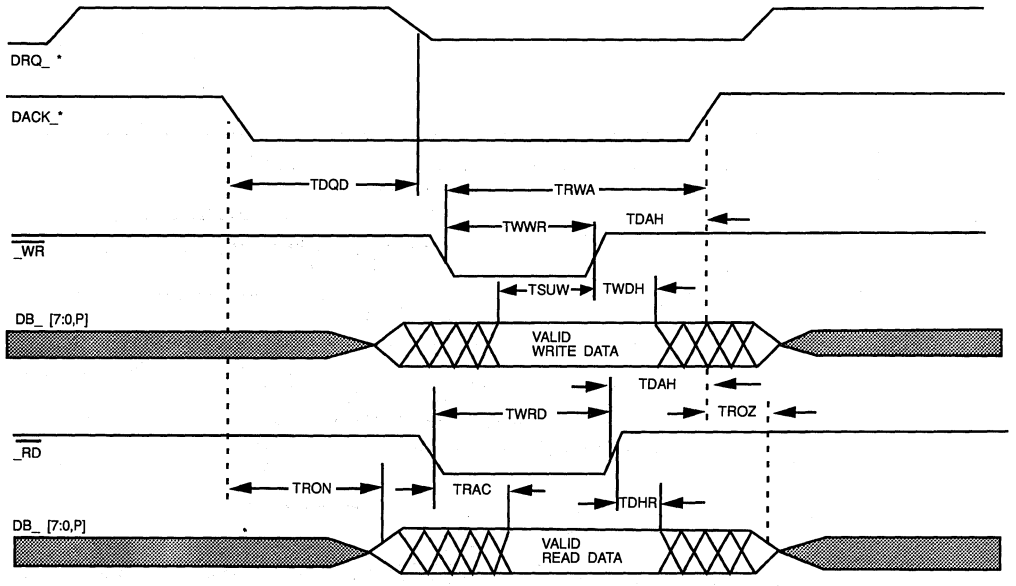
FIGURE 14-5. BUS MASTER DISK MODE



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR - Width of Write Strobe		R	50 NS	
TSDA = Time of Strobe Deactivated		R	50 NS	
TDQD = Time to DRQ Deasserted	LE	S		35 NS
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	TE	R	0 NS	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRON = Time Read Output Enable from DACK (If DIR bit is set)	LE	S	0 NS	50 NS
TWRD = Width of Read Strobe		R	50 NS	
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data		S	10 NS	45 NS
TROZ = Time of Read Strobe to High Z		S		50 NS

* DRQ polarity shown high true; DACK polarity shown low true

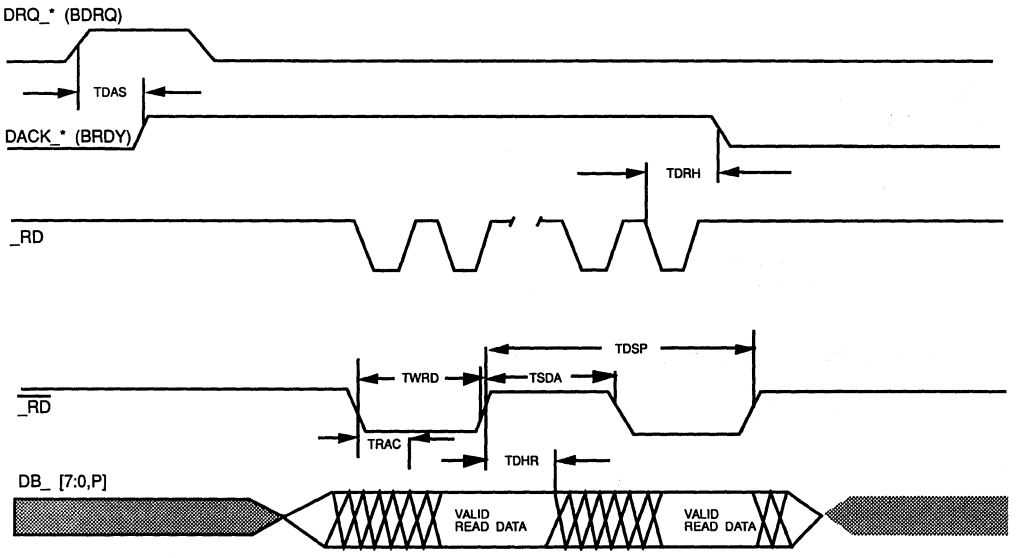
FIGURE 14-6. SLAVE BURST MODE TRANSFERS



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR - Width of Write Strobe		R	50 NS	
TDQD = Time to DRQ Deasserted	LE	S	1.5 TCYC	3.5 TCYC + 15 NS
TDAH = Time of DACK Hold	TE	R	0 NS	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRON = Time Read Output Enable from DACK (If DIR bit is set)	LE	S	0 NS	50 NS
TWRD = Width of Read Strobe		R	50 NS	
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data	TE	S	10 NS	45 NS
TROZ = Time of Read Strobe to High Z	TE	S		50 NS
TRWA = Time of R/W to DACK Inactive	LE	S	2 TCYC + 15 NS	

* DRQ polarity shown high true; DACK polarity shown low true

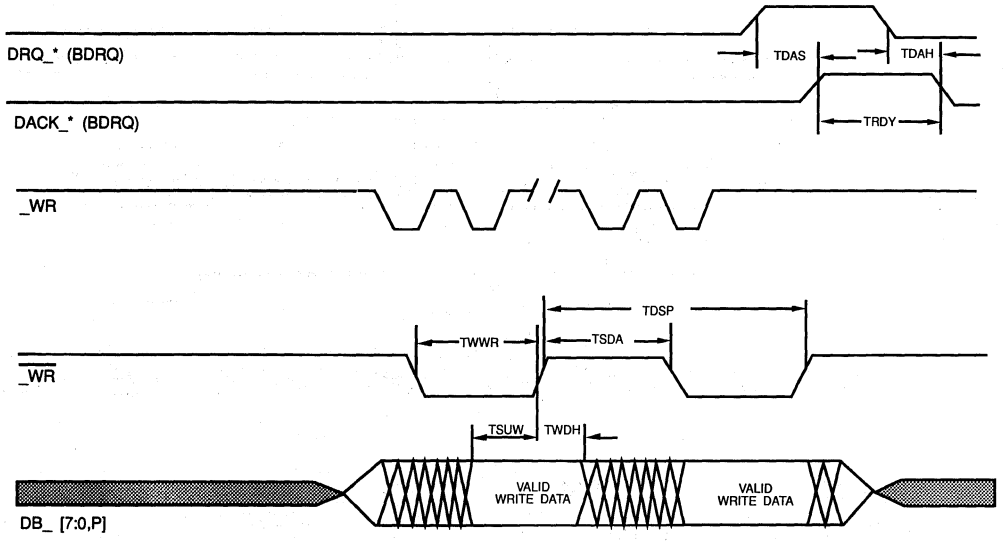
FIGURE 14-7. SLAVE SINGLE CYCLE TRANSFER



NAME	REF	R/S	MINIMUM	MAXIMUM
TDAS = Time of DACK Setup	LE	S	3.5 TCYC	5.5 TCYC + 15 NS
TSDA = Time of Strobe Deactivated		R	50 NS	
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	LE	S		6 TCYC
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data	LE	S	10 NS	
TWRD = Width of Read Strobe		R	50 NS	

* DRQ polarity shown high true; DACK polarity shown low true

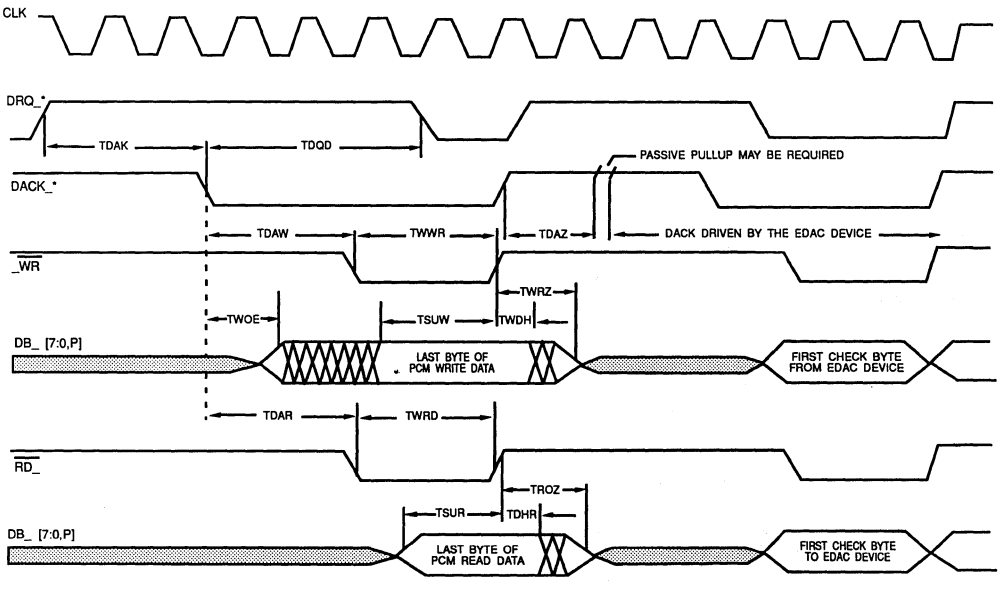
FIGURE 14-8. SLAVE BURST DISK MODE (READ)



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR = Width of Write Strobe		R	50 NS	
TSDA = Time of Strobe Deactivated		R	50 NS	
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	TE	R	2 TCYC	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRDY = Width of BRDY (DACK)		R	10 TCYC	
TDAS = Time of DACK Setup		S		6 TCYC

* DRQ polarity shown high true; DACK polarity shown low true

FIGURE 14-9. SLAVE BURST DISK MODE (WRITE)



NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	6.5 TCYC
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS
TDAZ = Time to Dack High Z	TE	S		6 TCYC

* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

FIGURE 14-10. EDAC MODE (DMA SINGLE CYCLE)

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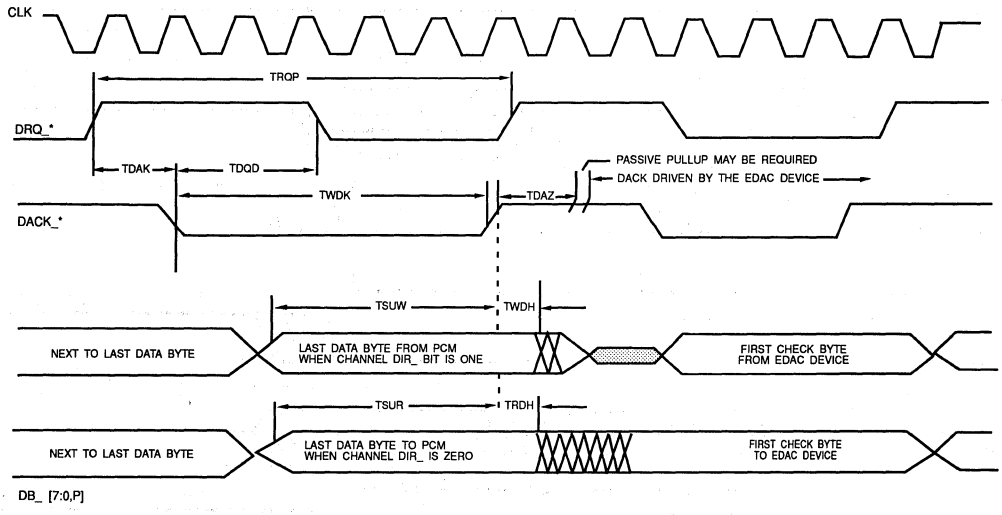


NAME	REF	R/S	MINIMUM	MAXIMUM
TDAK = Time DRQ to Acknowledge	LE	S		35 NS
TDQD = Time to DRQ Deasserted	LE	R		3 TCYC
TRQP = Time of Request Period		R	6.5 TCYC	
TWDK = Width of DACK Signal		S	3.5 TCYC	5.5 TCYC + 15 NS
TSUW = Data Setup Time of Write Data	TE	S	2 TCYC - 40 NS	
TWDH = Data Hold Time of Write Data	TE	S	TCKH - 5 NS	
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TDAZ = Time to DACK High Z	TE	S		6 TCYC

* DRQ polarity shown high true; DACK polarity shown low true
** If SDTC in Section 4.1 is set, then value is 4 TCYC
*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state

FIGURE 14-11. EDAC MODE (DMA DISK)

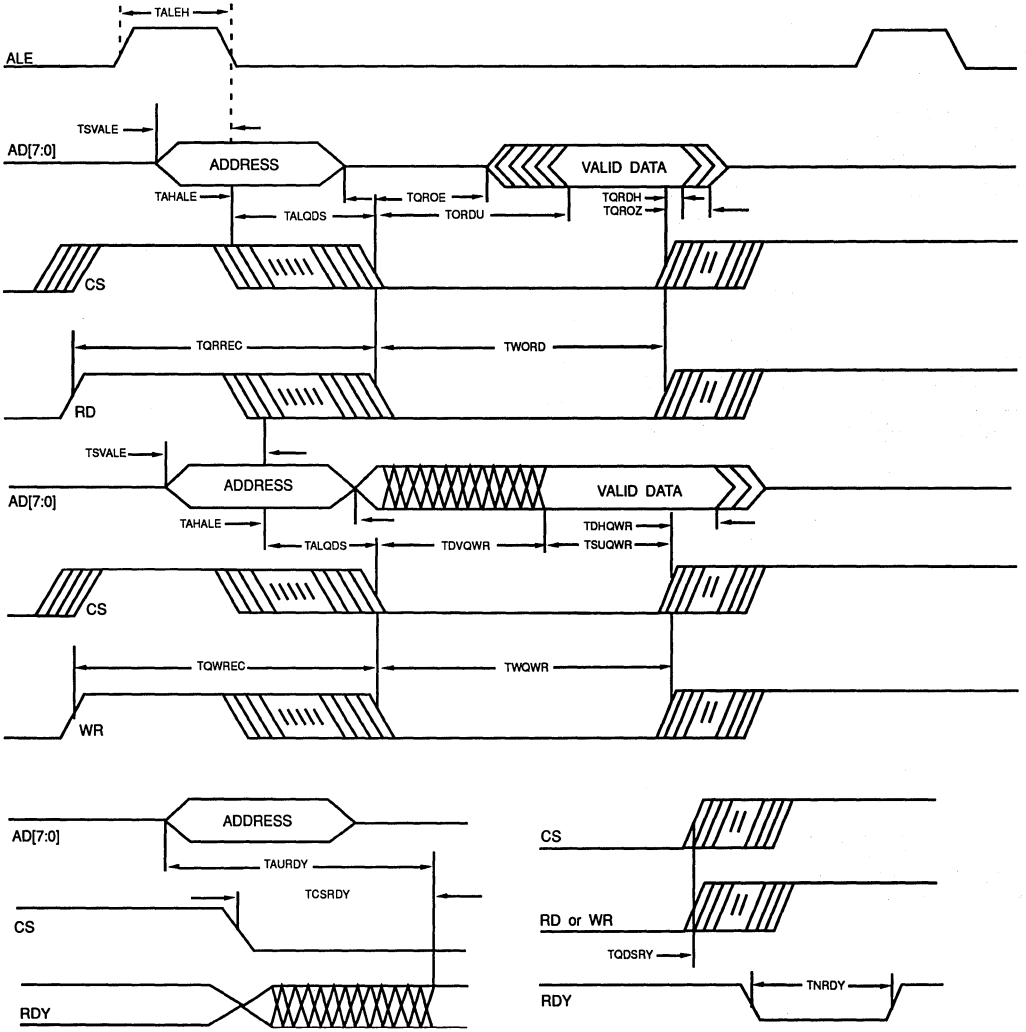
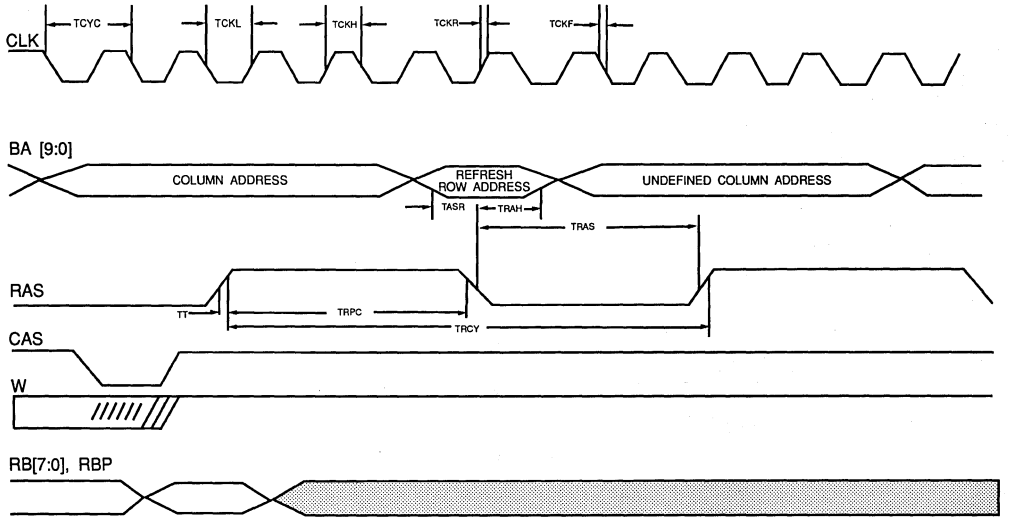


FIGURE 14-12. MICROPROCESSOR BUS TIMING

NAME	REF.	R/S	TIMING
TALEH = ALE High Pulse Width		R	35 NS MIN.
TSVALE = Address Setup Before T.E. ALE	TE	R	15 NS MIN.
TAHALE = Address Hold after T.E. ALE	TE	R	15 NS MIN.
TALQDS = ALE T.E. to Qualified Data Strobe	TE	R	30 NS MIN.
TWORD = Pulse Width Qualified Read Strobe		R	110 NS MIN.
TQROE = Qualified Read Strobe to Output Enabled	LE	S	40 NS MAX.
TQRDV = Qualified Read Strobe to Data Valid	LE	S	95 NS MAX.
TQRDH = Data Hold from Qualified Read Strobe	TE	S	0 NS MIN.
TQROZ = T.E. Qualified Read Strobe to High Impedance	TE	S	60 NS MAX.
TQRREC = Recovery Time after Qualified Read Strobe	TE	R	120 NS MIN.
TWQWR = Pulse Width Qualified Write Strobe		R	110 NS MIN.
TDVQWR = Data Valid from L.E. Qualified Write	*	R	3 CLK MAX.
TSUQWR = Data Setup to T.E. Qualified Write	TE	R	30 NS MIN.
TDHQWR = Data Hold from T.E. Qualified Write	TE	R	10 NS MIN.
TQWREC = Recovery Time after Qualified Write Strobe	TE	R	120 NS MIN.
Waitable Microprocessor Interface			
TAURDY = Address Valid to Ready Valid	LE	S	50 NS MAX.
TCSRDY = Chip Select to Readh Valid	LE	S	35 NS MAX.
Non-Waitable Microprocessor Interface			
TQDSRY = T.E. Qualified Data Strobe to Not Ready	TE	S	60 NS MAX.
Either Microprocessor Interface			
TNRDY = Time Not Ready	**	S	6 CLK MIN.

* Required in Waitable Mode Only
** See Section 5.0 for maximum

TABLE 14-1. MICROPROCESSOR BUS TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TCYC = Input CLock Period		R	40 NS	
TCKL = Input Clock Low		R	17 NS	
TCKH = Input Clock High		R	17 NS	
TCKR = Input Clock Rise		R		5 NS
TCKF = Input Clock Fall		R		5 NS
TRAS = Time of RAS Low		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	TRFC **
TRFC = Refresh Cycle Time (Programmable)		S	32 TCYC	512 TCYC ***
TT = Transition Time All Outputs		S	3 NS	20 NS

** This specification assumes no other memory requests other than Refresh.
*** This is the maximum programmable value. The programmed value is based on DRAM specification.

FIGURE 14-13. RAS ONLY REFRESH TIMING

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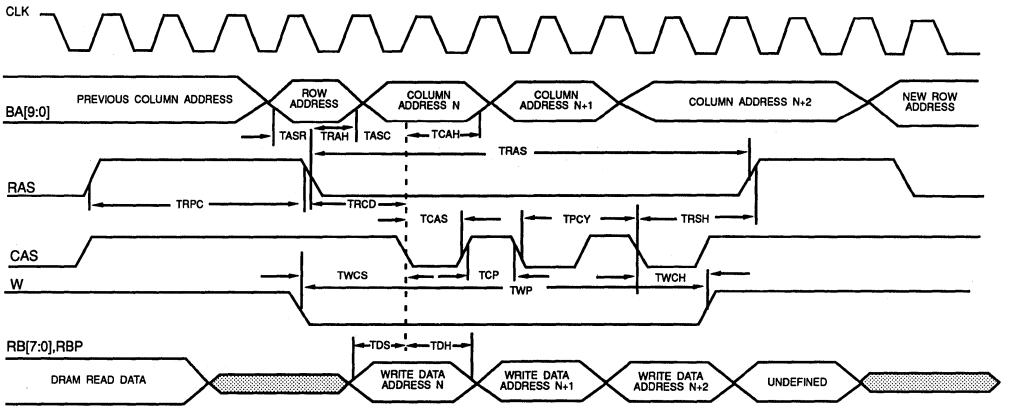
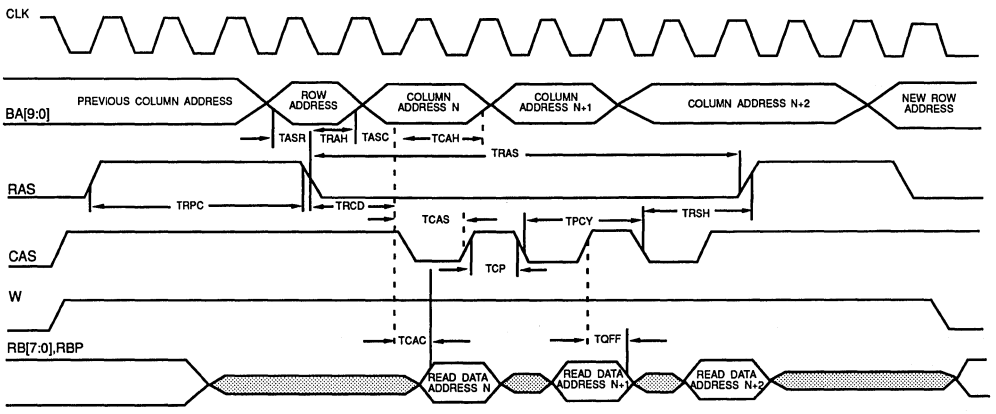


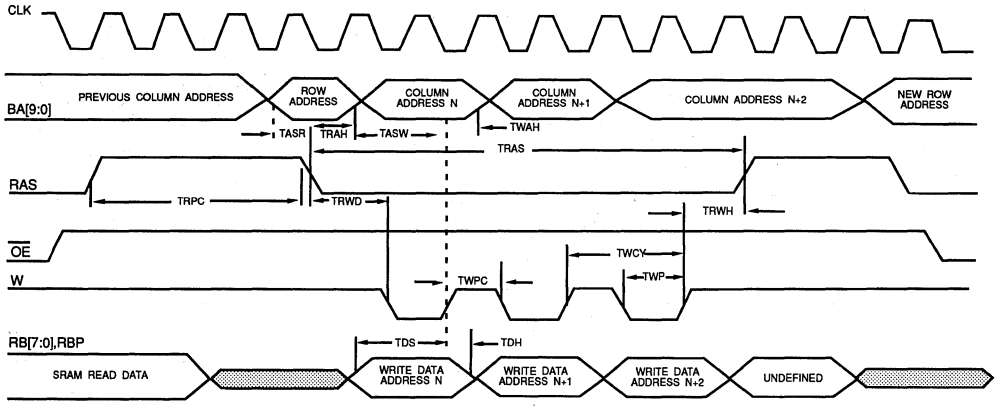
NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRCD = L.E. RAS to L.E. CAS Delay	LE	S	2 TCYC - 25 NS	
TCAS = Time of CAS Asserted		S	TCYC	
TCP = Time of CAS Precharge (CAS High)		S	TCYC - 20 NS	
TWP = Time of Write Asserted		S	2 TCYC	
TASC = Address Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TCAH = Address Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TDS = Data Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TDH = Data Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TRSH = RAS Hold from L.E. CAS	LE	S	TCYC	
TWCS = Write Setup to L.E. CAS	LE	S	TCYC	
TWCH = Write Hold from L.E. CAS	LE	S	TCYC	

FIGURE 14-14. PAGE MODE WRITE TIMING



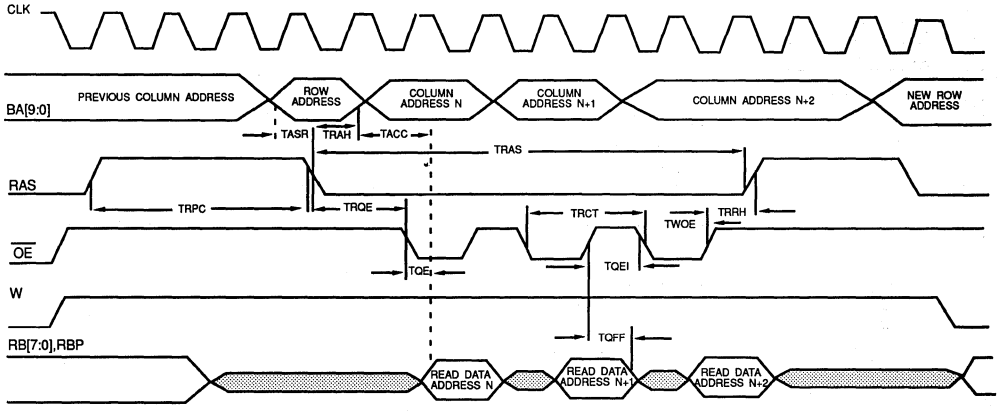
NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRCD = L.E. RAS to L.E. CAS Delay	LE	S	1.5 TCYC - 5 NS	
TCAS = Time of CAS Asserted		S	TCYC	
TCP = Time of CAS Precharge (CAS High)		S	TCYC - 20 NS	
TASC = Address Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TCAH = Address Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TRSH = RAS Hold from L.E. CAS	LE	S	TCYC	
TCAC = CAS Access Time	LE	R		TCYC
TOFF = Data High-Z Delay	TE	R	0 NS	30 NS

FIGURE 14-15. PAGE MODE READ TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRWD = L.E. RAS to L.E. Write Delay	LE	S	2 TCYC - 25 NS	
TWCY = Write Cycle		S	2 TCYC	
TWPC = Time of Write Precharge (Write High)		S	TCYC - 20 NS	
TWP = Time of Write Asserted		S	TCYC	
TASW = Address Setup to T.E. Write	TE	S	1.5 TCYC - 15 NS	
TWAH = Address Hold from T.E. Write	TE	S	5 NS	
TDS = Data Setup to T.E. Write	TE	S	1.5 TCYC - 15 NS	
TDH = Data Hold from T.E. Write	TE	S	5 NS	
TRWH = RAS Hold Time from T.E. Write	TE	S	0 NS	

FIGURE 14-16. STATIC RAM WRITE TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC - 15 NS	
TT = Transition Time All Outputs		S	3 NS	20 NS
TROE	LE	S	2 TCYC - 25 NS	
TWOE		S	TCYC	
TOEI		S	TCYC - 20 NS	
TACC		R	TCYC	1.5 TCYC - 15 NS
TRRH	TE	S	0 NS	
TOE	LE	R		TCYC
TOFF	TE	R	0 NS	30 NS
TRCT		S	2 TCYC	

FIGURE 14-17. STATIC RAM READ TIMING

15.0 PACKAGE DIAGRAMS

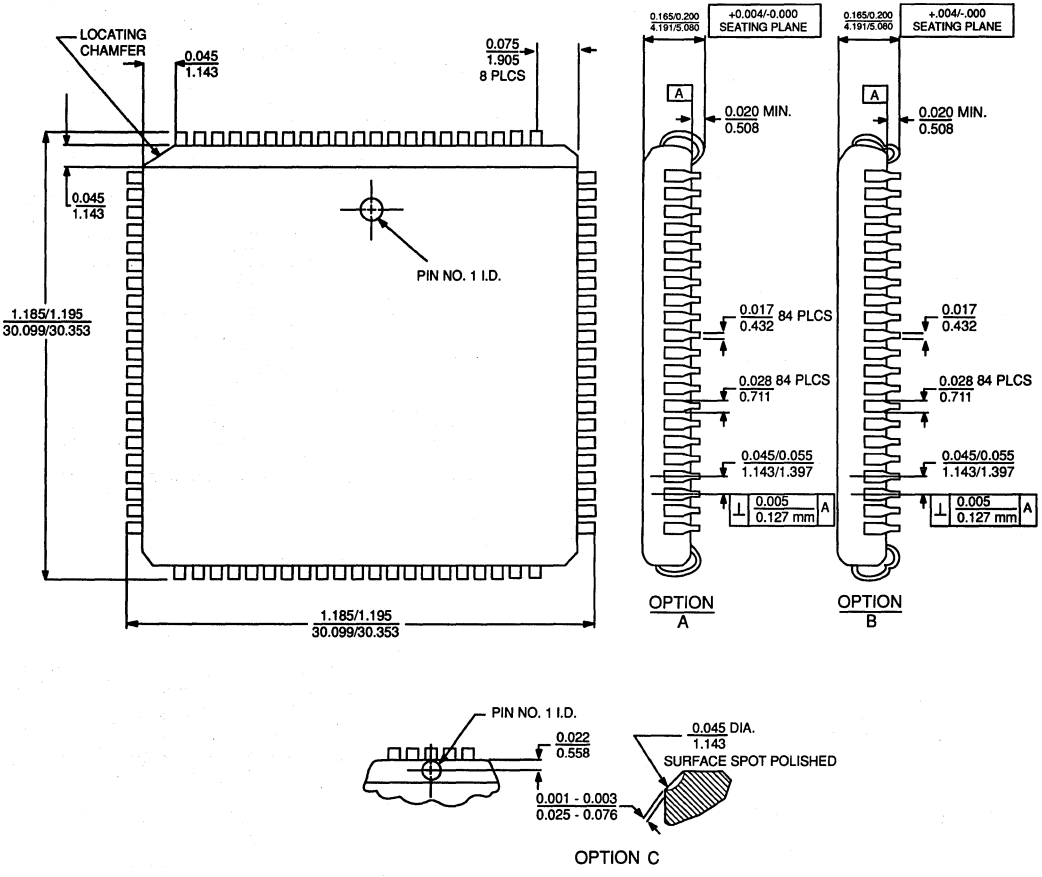


FIGURE 15-1. 84 LEAD PLCC

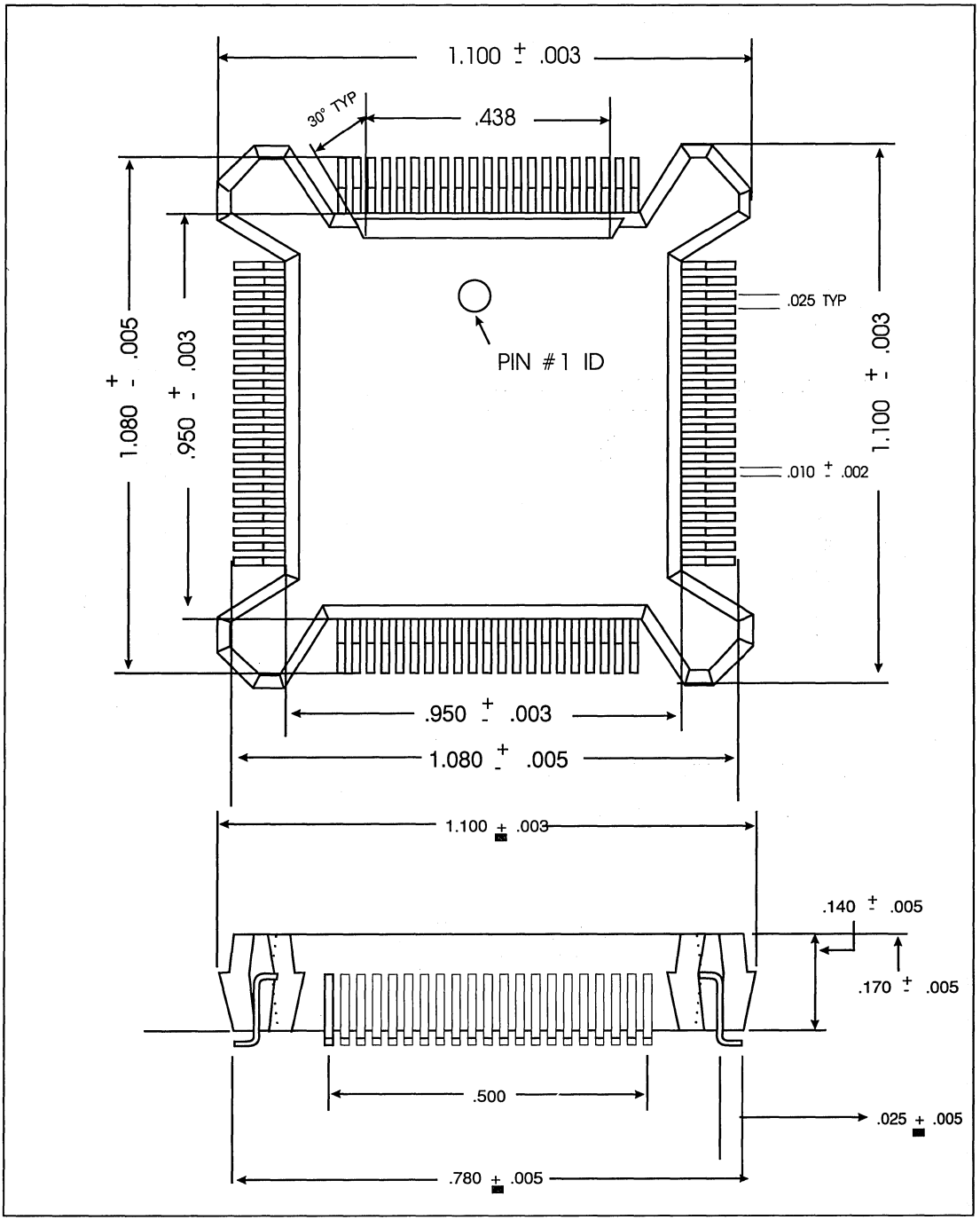


FIGURE 15-2. 84 LEAD PQFP

WD60C80

Error Detection and

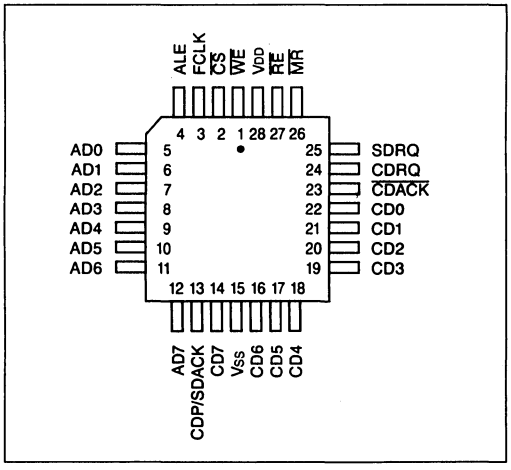
Correction Chip (EDAC)

WESTERN DIGITAL

WD60C80
Error Detection and Correction Chip (EDAC)

FEATURES

- High speed on-the-fly Reed-Solomon encoding and error detection up to 3 Mbyte/sec when clocked at 24 MHz. (Maximum clock frequency = 25.0 MHz)
  - —On-the-fly generation of check bytes and syndrome bytes. No latency associated with the code generation
  - —Programmable polynomial selections (degrees 4, 8, 16)
  - —Programmable interleave selections (1, 2, 3, 4, 5, 8, 10)
  - —Optional 4-byte GF(256) CRC
  - —Corrects up to 8-byte per interleave, or 80 bytes per sector
  - —Low redundancy overhead (7.8% for 1Kbyte sector, degree 16 and 5 interleaves, no CRC)
  - —Degree 16 and CRC polynomials are compatible with ANSI X3B11 standard
  - —Programmable sector size up to 2.5Kbyte (including data, CRC and ECC) in one-byte increments
  - —Write (ECC generation) and read (error detection) mode of operations
- Generates syndrome bytes compatible with the high-speed correction software algorithm licensed by Western Digital Corporation
  - —Zero latency delay for sectors with no error
  - —Supports correction of single byte error in 200 μsec using 8MHz 80188 microprocessor
- Fully independent processor port, allowing taskfile access at any time at all, independent of controller bus activity
  - —Full complement of programmable options and status information
  - —Status bytes with interleave-in-error number
  - —Supports simultaneous redundancy read/syndrome output transfers
- The internal 4-byte data path FIFO to capture data streams up to 1/5 the clock frequency (5.0 Mbyte/sec max.) without handshaking
  - —Optionally supports the parity bit on the controller bus
- The internal 20-byte syndrome FIFO to support continuous back-to-back transfer with minimal gap length
  - —Supports DMA or programmed I/O up to 1/5 the clock frequency (5.0 Mbyte/sec max.)
  - —Syndrome bytes can be directed to the controller bus to support single RAM application
- Low cost single chip Error Detection and Correction
- Protocol compatible with the WD60C40 PCM and WD10C00 Disk SerDes
- Using Hyperbolic Drivers™ to suppress power/ground transient noise
- Single +5V supply
- 28 pin PLCC package
- Implemented in 1¼ μm dual metal CMOS technology



WD60C80
DEVICE PINOUT

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PIN DESCRIPTIONS

PIN	SYMBOL	PIN NAME	DESCRIPTION
1	$\overline{WE}$	Write Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile write operation by the processor.
2	$\overline{CS}$	Chip Select	TTL Input, Low Active; Controls the Taskfile access by the processor. The pin must be set high during the reset.
3	FCLK	Fast Clock	TTL Input; The primary clock input. f $\leq$25 MHz. The frequency must be greater than or equal to the nominal bit transfer rate for the application.
4	ALE	Address Latch Enable	TTL Input, High Active; The high level latches the multiplexed address vector on AD1-AD3 pins to the internal address register to control the Taskfile access.
5-12	AD0-AD7	Processor Data Bus	TTL Bidirectional, True Level; Multiplexed data/address bus used by the processor to access the internal Taskfile Registers and Syndrome transfer.
13	CDP/SDACK		TTL Bidirectional; Dual-Function Pin.
	CDP	CD bus Parity	TTL Bidirectional, True level; The parity bit input/output for the CD bus.
	SDACK	Syndrome DMA Acknowledge	TTL Input; Active Level Programmable. The external DMA controller indicating that the DMA cycle is granted.
14-22	CD0-CD7	Controller Data Bus	TTL Bidirectional, True Level; (Less Pin 15) Data, CRC, ECC bytes are transferred to/from the target disk controller via this bus. An option exists to use this bus for the Syndrome transfer.
15	VSS	Logic/Power Ground	
23	$\overline{CDACK}$	Controller Bus DMA Acknowledge	TTL Bidirectional, Low Active; During the data read phase, WD60C80 reads the data on CD bus while this signal (input) is active. During the redundancy read/write phases WD60C80 inputs/outputs the CRC/check bytes while this signal (output) is active.
24	CDRQ	Controller Bus DMA Request	TTL Input, High Active; DMA Request from the target disk controller. It is sampled and used for $\overline{REQ}$ ACK protocol between the WD60C80 and the controller/buffer manager during the redundancy read/ write phase of the operation.
25	SDRQ	Syndrome DMA Request	TTL Output, High Active; Indicates to the external DMA controller that syndrome bytes are ready to be transferred.
26	$\overline{MR}$	Master Reset	TTL Input, Low Active; Initializes the chip to the power-on default condition.
27	$\overline{RE}$	Read Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile read operation by the processor.
28	VDD	Power Supply	+5 V $\pm$ 10%

DESCRIPTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed, CMOS LSI, designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical for optical or magnetic disk drives, tape drives and communication links.

INTRODUCTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed CMOS LSI designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical.

The WD60C80 generates the Reed-Solomon code with the coefficients from GF(256) with the generator polynomials of degree four, eight or 16. It also generates 4-bytes GF(256) CRC code in order to (a) detect mis-corrections and (b) support extended correction to correct up to 16 bytes of error per interleave (depending on the polynomial degree chosen). The degree 16 polynomial and the CRC are the standard adopted by ANSI X3B11 committee to be used for optical disk storage.

Using degree 16 polynomials and 10 interleaves (interleave factors are programmable between one to 10 in seven steps), the WD60C80 can correct up to 80 bytes per sector of data with only 160 bytes of ECC overhead (164 if CRC is used).

The WD60C80 can be used to (a) generate ECC bytes (hereafter referred to as "check bytes" or "redundancies", interchangeably) by reading in the data field, or (b) generate the syndrome by reading the potentially erred data field and redundancies. The external processor needs to perform the actual data correction using the syndrome bytes. The software support is available from Western Digital Corporation.

The WD60C80 can be clocked as high as 25.0 MHz, and has the maximum byte/sec throughput of 1/8 the clock frequency. If this minimum clock frequency requirement is met, it can synchronize itself to the data flow and performs its function properly. Therefore, if an application calls for multiple data rates, this device can handle it without having its clock switched.

The WD60C80 can support the average data rate of up to three Mbyte/sec when clocked at 24 MHz, with the short burst (four bytes of less) of up to 4.8 Mbyte/sec. The code is generated on-the-fly at the data rate. It supports the sector size (including the check bytes and CRC) up to 2,550 bytes in one byte increment. Syndrome bytes can be transferred at the maximum speed of 4.8 Mbyte/sec when clocked at 24 MHz, and the internal 20-byte syndrome FIFO allows continuous back-to-back transfer of sectors with minimal inter-sector gap lengths.

In order to support the high data rate reliably, it employs the proprietary Hyperbolic Driver to suppress power/ground transient noise. The ground level transient noise is kept to less than 400 mV at all times.

The WD60C80 is applicable to all areas where error correction is important to maintain high data throughput and integrity such as controllers for optical or magnetic disk drives, tape drives and communication links.

The device is implemented using 1¼ μm double metal CMOS process, and packaged in a 28-pin PLCC. It requires a single + 5.0 Volt $\pm$ 10% supply and rated at the full specification in the temperature range of 0°C to 70°C.

ARCHITECTURE

The WD60C80 has two operation modes;
a) Read mode and
b) Write mode.

In read mode, it reads a full block of data and redundancies. The acquired data may contain errors, so it generates the redundancy code internally, and compares them with the acquired redundancies to generate syndrome bytes. These syndrome bytes, equal in number to the redundancy bytes, are transferred to the external processor, who will process the information and actually perform the error correction.

In write mode, the WD60C80 reads just the data bytes, generates redundancies, and appends them to the end of the data byte flow. This formatting function is performed on the bus by arbitrating between the WD60C80 and the external buffer manager.

The WD60C80 relies on an external processor to setup the desired configuration or to recover from operational failure by reading or writing the internal taskfile registers, there is a seperate 8-bit port for that purpose. This port can be accessed at any time regardless of the activity of the data/redundancy generator.

In order to perform the above functions, the WD60C80 has three distinctive interfaces.

a) The processor interface (ALE, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ pins)
b) The controller interface (CDRQ, $\overline{CDACK}$ pins)
c) The syndrome transfer interface (SDRQ, SDACK pins).

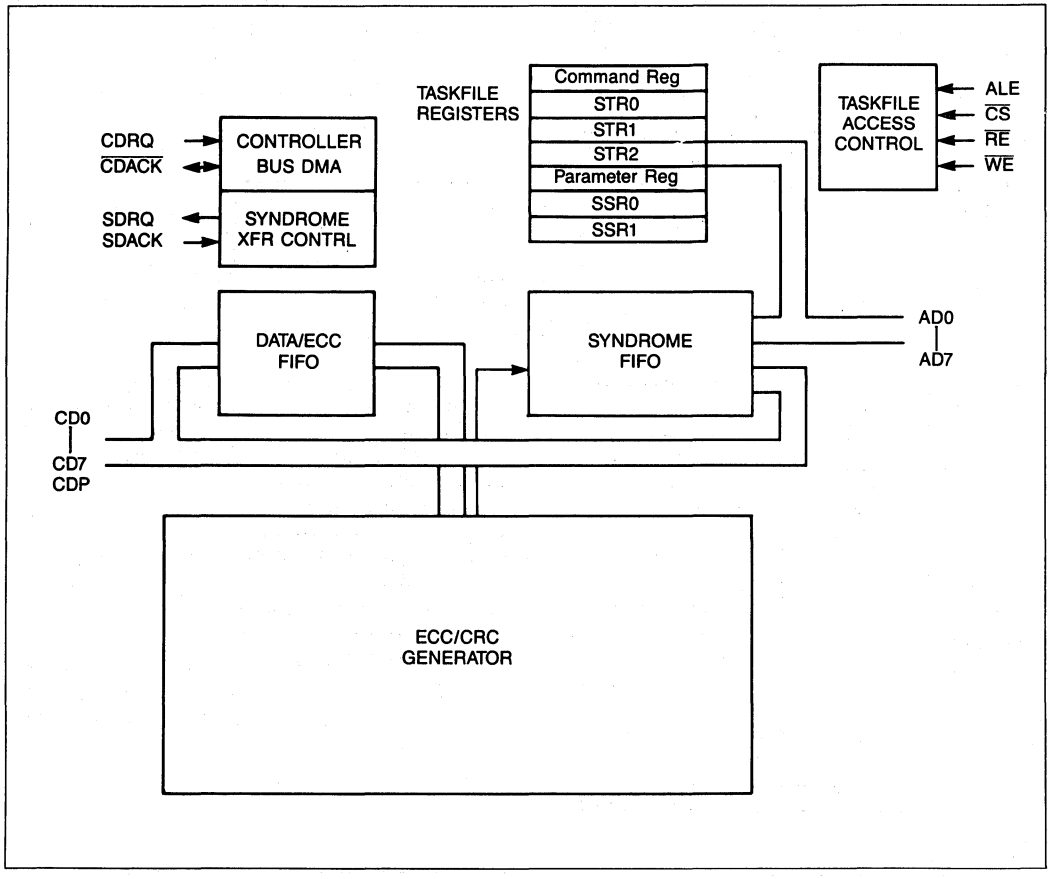
The controller bus and syndrome transfer interfaces are simple REQ-ACK protocol of a regular DMA controller. It has two physical ports or busses, eight bits wide each.

a) The processor bus (designated ADx in the pin description)
b) The controller bus (designated CDx in the pin description).

The controller interface works exclusively on the controller bus, (designated as CDx in the pin-out description) handling the target (e.g., disk controller) data reads and writes, while the processor interface works exclusively for the processor bus, and used to access the internal taskfile registers. The syndrome transfer interface works on either the processor bus or the controller bus, depending on the chosen option, to transfer syndrome/status bytes during the read operation.

The controller bus has an optional ninth bit, which is used as the parity bit for higher data integrity. The WD60C80 can generate and check for odd parity on each byte read/written. It is activated by properly setting the Parameter Register.

Because the device is packaged in a 28-pin PLCC, two pin functions are multiplexed on one physical pin and hence not available at the same time. If the parity generation/checking is to be supported on the controller bus, the DMA mode syndrome transfer must be given up, since SDACK (Syndrome DMA Acknowledge) and CDP (Controller Bus Parity bit) are assigned the same pin. This pin can be only programmed to function as one of the two. Some DMA devices (most ones with memory to memory transfer capability) and integrated processors (such as Intel™ i80188/86) have their DMA function implemented like a programmed I/O (i.e., generates Address and $\overline{RE}$ or $\overline{WE}$, rather than issuing a DMA $\overline{Acknowledge}$), which allows for syndrome DMA transfer and parity checking at the same time.



WD60C80 SIMPLIFIED BLOCK DIAGRAM

Data/ECC FIFO is bidirectional, allowing the data and ECC/CRC bytes to pass through in the appropriate directions. It is four-byte deep, and has special control logic that lets a data byte pass through right into the ECC and CRC generator if the FIFO is empty, in order to improve the overall throughput.

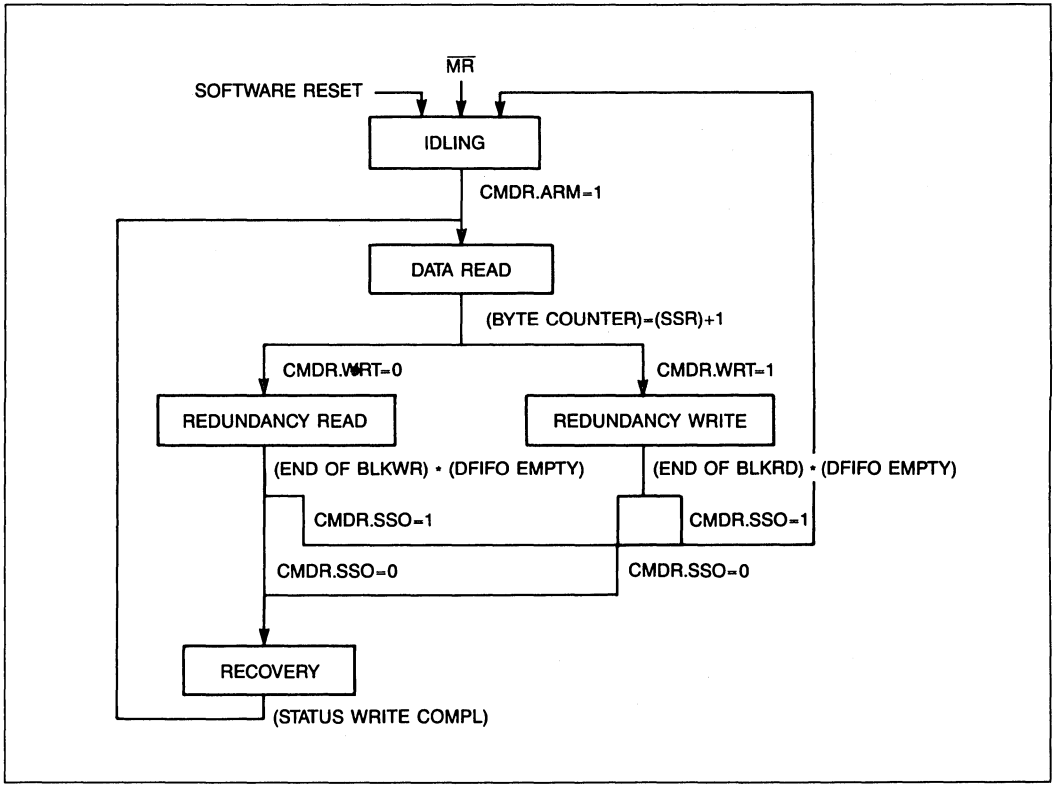
Syndrome FIFO is unidirectional (read-only) FIFO used to smooth the transfer of CRC residue, syndrome and status bytes. Its output can be directed to either the controller bus or the processor bus.

There are seven taskfile registers on the processor bus. They can be read/written at any time, independent of the controller bus activity, allowing the external processor to interact with the device without any special protocol.

Control Sequences

The WD60C80 has five independent states as listed below:

1) Idling	WD60C80 is completely dormant.
2) Data Read	WD60C80 reads data bytes from the CDbus.
3) Redundancy Write	WD60C80 writes ECC/CRC to the CDbus.
4) Redundancy Read	WD60C80 reads ECC/CRC from the CDbus.
5) Recovery	End of a block and reinitialize for the next.



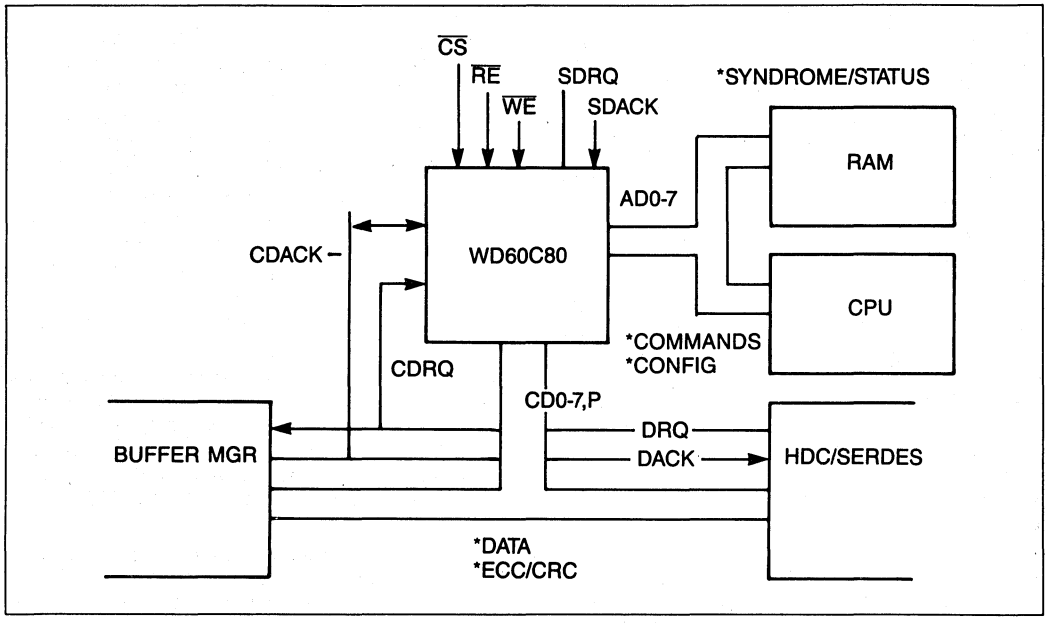
WD60C80 BASIC CONTROL FLOW DIAGRAM

(END OF BLKWR) = All ECC/CRC bytes written out to the data/ECC FIFO.
(END OF BLKRD) = All ECC/CRC bytes processed and the last syndrome byte is output to the syndrome FIFO.
(STATUS WRITE COMPL) = The final status bytes written to the syndrome FIFO.

The operational details and the hardware protocol on the bus transactions on each state are described in the following sections.

Basic Topology

The WD60C80 is designed to be placed between a buffer manager and a target peripheral device (e.g., disk serdes). It is assumed that the buffer manager and the target will transfer the data bytes using REQ-ACK protocol. The buffer manager is normally the DMA master, with the target peripheral being the permanent slave.



WD60C80 BASIC TOPOLOGY

The WD60C80 listens to the CD bus and (when ARMed), picks up a byte every time CDACK pulses, as a valid data byte. When all data bytes are read and processed, the WD60C80 becomes a temporary bus master (i.e., it performs the REQ-ACK protocol with the target peripheral device) and transfers the ECC and CRC bytes. Unless it is used with a buffer manager device such as the WD60C40 that has a special arbitration mode with WD60C80, some external support logic is required between the buffer manager DMA and the WD60C80 to give this device the control of the bus during Redundancy Read/Write phases.

During the Redundancy Read phase, the WD60C80 generates syndrome bytes equal in number with the ECC bytes. They are output through (by default,) the processor bus to the CPU memory. It performs the REQ-ACK protocol with the external DMA controller (in DMA mode) as a slave device. Optionally, the syndrome bytes can be output through the controller bus, though due to the external bus arbitration overhead, the throughput of the transfer will be much lower in this case.

Controller Bus Interface

The "Controller Bus" refers to the CD0 through CD7 pins plus the optional CDP pin which is multiplexed with SDACK function. They are used to connect the WD60C80 to the bus between the buffer manager device and the target peripheral controller device. Depending on the option chosen, it can also be a port to transfer the syndrome/status bytes during the READ operation. This bus behaves in three different manners depending on the state the device is in.

Data Read Phase

The data read phase (state) is entered when the ARM bit of the command register is set high. The WD60C80 CD bus behaves passively in this mode, with all the CDx pins and the CDACK pin being inputs. CDRQ pin is inactive in this phase. When the CDACK signal (issued by the buffer manager) becomes active (low), the WD60C80 grabs the data byte on the CD0 through CD7 pins and stores it into the internal FIFO. Care should be taken that it does not necessarily get the data byte at the trailing edge of the CDACK pulse, but can actually gets it anytime after four clock cycles after the leading edge of the pulse.

This is done to speed up the internal processing of the data, to shrink the blank time between the Data Read Phase and the Redundancy Write Phase. Also it should be noted that the $\overline{CDACK}$ pulse needs to be wider than 2.0 clock cycles to insure a proper read.

The average transfer cycle on the controller bus during this phase should not exceed one eighth of the WD60C80 clock frequency, which is the rate at which the device processes a byte. But in order to be more flexible, the transfer cycles can proceed at the maximum rate of one fifth the clock frequency (e.g., at 25.0 MHz clocking, up to 5 Mbyte/sec) for a short span, up to about 10 bytes in length. A longer burst than that can result in a data FIFO overflow.

If the average data rate is slower than one eighth the clock frequency, then the WD60C80 will slow down automatically and synchronize itself to the bus transaction. Therefore, there is no need to tweak the clock frequency of the device to match any special data rate, as long as the frequency is high enough.

Redundancy Write Phase

The WD60C80 enters the Redundancy Write Phase (State) if the WRITE operation is chosen in the command register, and the prescribed number of bytes (in the sector size register) are read from the controller bus and finished processing inside the ECC generator.

In this phase, the WD60C80 performs REQ-ACK protocol with the target peripheral device, outputting the generated ECC and CRC bytes to the controller bus. The $\overline{CDACK}$ pin as well as all the CDx pins become outputs, and CDRQ input gets activated, the WD60C80 becoming the temporary bus master. Unless it is used with a buffer manager like the WD60C40 which knows when to release the bus, some external support logic is necessary between the buffer manager and the WD60C80, isolating the buffer manager from the DMA protocol to transfer the ECC/CRC bytes. In particular, the DACK output of the buffer DMA device must be tri-stated.

Notice when the WD60C80 shifts from the Data Read Phase to the Redundancy Write Phase, there is more than a "Byte Time (eight clock cycles)" before the first ECC/CRC byte can be output after the last data byte is loaded. The worst case latency of 12 clock cycles if the data FIFO is empty prior to receiving the last data byte; the best case is ten clock cycles.

Some target devices such as a disk serdes cannot tolerate the data transfer latency longer than one byte time, so some extra support logic between the WD60C80 and the target controller device is necessary to support those devices. A few examples for this logic are:

1) Place a data holding register or FIFO in front of the target device so that the controller won't run out of data before the WD60C80 can output the first ECC/CRC bytes. This register should be bidirectional, for dealing with the Read operation.
2) Set the WD60C80's clock frequency high enough so that the worst case switch-over time is narrower than the "one byte time" of the target controller device. This method is applicable if the required data rate is significantly less than the specified maximum clock frequency of the WD60C80.

After the WD60C80 takes over the bus, it transfers the ECC/CRC bytes pretty much at the target data rate (eight clock cycles/byte, if FCLK frequency is matched to the target data rate). If it is requested and there are a few bytes accumulated in the data FIFO, then it can transfer as fast as six clock cycles/byte.

Notice it does not cause a FIFO overflow, if the CDRQ pin is held inactive (low) for an extended period of time. The WD60C80 will stop generating redundancies when the FIFO is full.

When all the ECC bytes are generated and the data FIFO becomes empty (i.e., all of them are transferred to the target device), then the WD60C80 changes its state to the Recovery Phase. The $\overline{CDACK}$ pin becomes an input again, and the final status information is output to the Syndrome FIFO, where the processor can read it.

The WD60C80 changes its state to either the Data Read Phase for the next block if the Multiple Sector Operation is selected, or to the Idling Phase if the Single Sector Operation is selected.

Redundancy Read Phase

The WD60C80 enters Redundancy Read Phase (State) if READ operation is chosen in the command register and the last data byte is input through the controller bus, then processed internally.

Similar to the Redundancy Write Phase, it performs REQ-ACK protocol with the target controller device as a temporary bus master, but to read CRC/ECC the part of the block. Same restrictions and support logic requirements apply as the Redundancy Write case. Notice at the end of the block, it takes longer to get ready for the next block in the READ operation than the WRITE operation, because the data/ECC FIFO may become full when the last ECC byte is read from the controller bus, due to the read-ahead feature on this device. If the transfer is taking place at the WD60C80 data rate or less, and therefore not utilizing the read-ahead feature, then it should take just as long as the WRITE mode operation to get back to the Data Read Phase of the next block (Multiple Sector Operation).

If extra CDRQs are generated by the target controller at the end of the block, the WD60C80 will generate spurious $\overline{CDACK}$ pulse and loads whatever is on

the CD bus at the time. Since the internal state machine knows how many ECC bytes it should process, it will not fetch these spurious bytes from the FIFO. This prevents the FIFO from becoming empty, and consequently, prevents the WD60C80 from going into Recovery Phase. This can cause a system hang-up, so care should be taken.

When the Syndrome-on-the-Controller-Bus option is selected, the syndrome output also takes place on this bus, physically. The transfer is controlled by the SDRQ pin (output) and SDACK pin (input), and the bus arbitration between the two channels of the DMA is expected to be done external to this device. When two transfers collide on the bus, neither transfer takes place and consequently, both transfers are broken. This is an option meant for a low cost application where data buffer and the syndrome information share the same physical RAM, and it is not expected to be used for high throughput applications, where a large overhead associated with the DMA arbitration cannot be tolerated.

Processor Bus Interface

The processor bus refers to the AD0 through AD7 pins controlled by ALE, $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$ pins. Depending on the options, the SDRQ and SDACK pins also control this bus. This bus is used primarily by the external processor to setup the operation modes/configurations of the WD60C80 as well as reading the operational/error status of the device. It is also used as the port to transfer syndrome/status bytes during the READ operation, by default.

Internal Register Interface

The internal taskfile read/write interface is native to the Intel 8085, 80186, 80188 and 8051 series of processors. Other processors with multiplexed address/data bus can be readily supported, but some external logic is needed to support processors with non-multiplexed bus.

In order to ease the interfacing to the 16-bit processors, some of which insist on even or odd boundaries for byte accesses, all internal registers of the WD60C80 are mirrored on even and odd addresses.

The processor can read any register at any time, without disturbing the internal operation. Before writing to any of these registers, however, it is suggested to soft reset the device (set the RST bit on the command register). If any options or configurations are changed while the device is active, it can disrupt the current operation, and in the worst case, it can hang up (The soft reset is effective even in the case of hang up). Consequently, it is suggested that all setups are made before the command register is written with the ARM bit set active.

When the Syndrome FIFO is read by the processor, care should be taken that the $\overline{CS}$ $\overline{RE}$ signal is wider than 2.0 clock cycles of the WD60C80, or it can upset the internal FIFO pointers. This situation is usually detected by the Syndrome/Status stream that is longer than expected. Because the pointer information cannot be accessed from the outside of the device, it is not possible to detect when the error happened, leading to a possible miscorrection.

Syndrome/Status Transfer

When the WD60C80 is operating in the READ mode, it generates syndrome bytes as it reads ECC bytes from the target controller device through the controller bus. They can be read using either PIO (programmed I/O) mode access, where the access is made just like another register read, or DMA mode, where the SDRQ pin and the SDACK pin are used to perform REQ-ACK protocol.

Code Description and Performance

The WD60C80 implements Reed Solomon error correcting code of degree 16, distance 17, long distance code. There are 16 redundancy (ECC) bytes generated per interleave, and it is capable of correcting up to eight symbol (byte) errors per interleave in any combinations of random and burst errors. This polynomial is compatible with the ANSI X3B11 error detection and correction encoding standard for 5¼ inch optical storage devices.

The 32-bit CRC code covered by the same format standard is also supported. The same CRC polynomial is used regardless of the selection of the ECC polynomials.

In addition, to support high density magnetic storage devices which do not require such a wide correction span, degree four and eight polynomials are provided for smaller ECC overhead (four and eight bytes per interleave, respectively), narrower correction span (two and four bytes per interleave, respectively), and shorter correction time (software dependent).

The device supports seven different interleave factors to optimize between the ECC overhead and correctable burst error length, once a proper polynomial is chosen. It supports one (no interleave), two, three, four, five, eight and 10-way interleaving. Because the coefficients of the generator polynomial is chosen from the GF(256), there can be only 255 symbols or bytes, per interleave including the ECC bytes. For that reason, the data field length of a block cannot exceed 255 times the interleave factor, less ECC/CRC overhead.

(The Maximum Data Field Length)
= 255 X (Interleave Factor) –
(ECC Overhead)–(CRC Overhead)

Number of ECC/Syndrome Bytes generated
(ECC Overhead)

Polynomial	Interleave Factors 1	2	3	4	5	8	10
Degree 16	16	32	48	64	80	128	160
Degree 8	8	16	24	32	40	64	80
Degree 4	4	8	12	16	20	32	40 (Bytes)

CRC Overhead = 0 if CRC is disabled.
= 4 if CRC is enabled.

Example:
For Degree 16, 10 interleave, no CRC,
(The Maximum Data Field Length)
= 255 X 10–160–0
= 2,390 Bytes

When used on 512-data-byte physical block, degree 16 polynomial, with five-way interleave with the CRC enabled, there are 103 data bytes in the first two interleaves and 102 bytes in the last three interleaves. The interleaves 0, 2, 3 and 4 include a byte each of CRC, which are also protected by the ECC, then each interleave has 16 bytes of redundancy (ECC).

EXAMPLE BLOCK FORMAT
(Degree 16, five interleaves, with CRC)

INTERLEAVE

0	1	2	3	4	
D0	D1	D2	D3	D4	→ ROW 0 PARITY
D5	D6	D7	D8	D9	→ ROW 1 PARITY
D10	D11	D12	D13	D14	→ ROW 2 PARITY
D15	D16	D17			→ ROW 3 PARITY
		D507	D508	D509	→ ROW 101 PARITY
D510	D511	CRC0	CRC1	CRC2	→ ROW 102 PARITY (UP TO D511)
CRC3	R0	R1	R2	R3	
R4	R5	R6	R7	R8	USED TO COMPUTE CRC0-CRC3
R9					
					LEGENDS:
		R71	R72	R73	D0-D511: 512 BYTES DATA
					CRC0-CRC3: 4 BYTES CRC
R74	R75	R76	R77	R78	CR0-R79: 80 BYTES ECC
R79					

They are output to the target peripheral controller in the order of D0 through D511, CRC0 through CRC3, R0 through R79.

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Supported Polynomials

This section contains the definition of the polynomials supported by the WD60C80. Knowledge of the Reed-Solomon Code is assumed.

Finite Field Definition

This definition is common to all the polynomials including CRC.

Let β^i represent elements of a finite field generated by the polynomial over GF(2):

$p(x) = X^8 + X^5 + X^3 + X^2 + 1$

The elements of the finite field employed by the code are:

$\alpha^i = (\beta^i)^{88}$

ECC Generator polynomial for degree 16

Degree 16, distance 17, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=120}^{135} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 92 160 86 11 68 2 1 167 1 2 68 11 86 160 92 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Sixteen bytes per interleave.

Guaranteed Correction Span: Eight random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 8

Degree eight, distance nine, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=124}^{131} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 114 71 86 130 86 71 114 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Eight bytes per interleave.

Guaranteed Correction Span: Four random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 4

Degree four, distance five, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=126}^{129} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 64 61 64 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Four bytes per interleave.

Guaranteed Correction Span: Two random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

CRC Generator polynomial

The data field CRC code is specially constructed so that its residue can be adjusted as correction occurs. When correction is complete, the residue shall have been adjusted to zero.

Degree four, distance five, coefficients from GF(256)

$$g(x) = \prod_{i=136}^{139} (x + \alpha^i)$$

CRC Generator polynomial coefficients in decimal are:
1 232 194 35 198

Code Type: Reed-Solomon CRC operating on bytes.

Redundancy: Four bytes per sector, regardless of the number of interleave.

Statistical Detection Capability: The data field CRC code fails to detect an uncorrectable sector with probability of 2.3E-10 undetected uncorrectable sectors per uncorrectable sector.

Special Considerations:
1) The CRC code is applied to the XOR sum of data bytes across the interleaves.
2) Redundancy bytes are not inverted before writing.
3) The shift register implementing the code is initialized to zero.

Probability of uncorrectable error

Uncorrectable error rate is defined as the ratio of uncorrectable events to total bits transferred, and expressed in the formula below:

(Uncorrectable Error Rate)

$$= \frac{\text{Block Errors}}{\text{Bit}} = \frac{1}{kn} \sum_{i>e}^{n} \binom{n}{i} p^i (1-p)^{n-i}$$

where $\binom{n}{r} = \frac{n!}{r!\,(n-r)!}$

- n = Interleave length in symbols
- e = Maximum number of symbol errors correctable per interleave
- k = Symbol width in bits (8 bits for WD60C80)
- p = Raw symbol error probability (symbol errors/symbol)

(This formula is quoted from "Product Description for the NG8510", Data Systems Technology.)

It is assumed that error bursts occur at random intervals and each burst is assumed to affect a single symbol (one byte). If error bursts cluster or if error bursts span more than one symbol, the actual uncorrectable error rate will be greater. If each burst

is assumed to affect two symbols, the uncorrectable error rate becomes twice, and so on. A more complex computation is required when each burst is assumed to affect more than the number of interleaves employed.

Miscorrection Probability

Miscorrection probability of the code is 1.6E-6. Only those error events where the number of symbols in error in a single interleave exceeds eight are subject to miscorrection. The probability of transferring undetected erroneous data is the product of the probability of having more than eight errors in an interleave and the miscorrection probability of the code. For the degree 16 code, this probability is 7.7E-23 for a raw burst error rate of 1.0E-4.

Correction Software Support

The WD60C80 requires a companion software algorithm. This algorithm normally resides in the ROM of the external processor. Western Digital licenses the software implementing the required algorithm.

Internal Register Description

The WD60C40 has seven internal taskfile registers to set its operation modes, select programmable options and configurations, and report operational status. They are all accessed through the processor port using standard CPU interface with multiplexed address/data bus.

Register Map

The internal taskfile registers are mapped by the lower 4-bits of multiplexed address lines. For ease of interfacing to 16-bit processors, some of which require byte accesses to be on even or odd address boundaries, all registers are mirrored on even and odd addresses.

The address bits are latched by the internal address register which retains its contents until the next access, upon the ALE pulse input. Hence if a processor does not have a multiplexed bus, it can load the register address first by pulsing the ALE pin, then perform a read or a write in the next instruction.

A3,A2,1,0	HEX	SYMBOL	NAME	R/W,R/O	WIDTH
000X	0,1	CMDR	Command Register	R/W	8 bits
001X	2,3	STR0	Status Register 0	R/O	8 bits
010X	4,5	STR1	Status Register 1		8 bits
011X	6,7	STR2	Status Register 2		8 bits
100X	8,9	PRMR	Parameter Register	R/W	8 bits
101X	A,B	SSR1	Sector Size Register	R/W	4 bits
110X	C,D	SSR0	Sector Size Register		8 bits
111X	E,F		Syndrome FIFO	R/O	8 bits

Command Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CMDR	FT	SCB	CRC	SSO	WRT	ARM	RSV	RST

The Command Register is a Read/Write register that is used to set the WD60C80's operating mode. Since this register is used to activate/deactivate the device, writing to this register should be the last in the set up procedure.

Bit 0 RST–Software Reset/Abort Current Operation
Setting this bit high forces the internal reset logic to be activated, and the WD60C80 will halt current operation and clear itself to the default state. The following items are cleared:

- Command Register except RST bit.
- Parameter Register.
- Sector Size Registers.
- Status Registers.
- All internal state machines.
- Both (Data, Syndrome) internal FIFOs.

This bit does not clear by itself, so it needs to be set and then reset later by the external processor. It needs to be left set longer than four cycles of the input clock.

Bit 1 RSV – Reserved
This bit is reserved for a future enhancement.

Bit 2 ARM – Activate WD60C80 Function
This bit, when set high, activates the internal state machine of the WD60C80 to begin its operation by listening to the CD-bus activity. When low, the device is completely dormant. The taskfile should be initialized and set up prior to setting this bit.

Bit 3 WRT – Write Operation
When set high, the WD60C80 performs a write operation i.e., reads a block of data and outputs specified CRC/ECC. If it is low (default after reset), it performs a read operation (i.e., reads a block of data), CRC and ECC and generates a block of syndrome bytes, to be read by the external processor.

Bit 4 SSO – Single Sector Operation
When set high, the WD60C80 will operate on one block of data before clearing the ARM bit and disabling itself. The external processor has to activate the device before it can process another block. All other register content will be preserved.
When low (default after reset), it stays active and processes consecutive blocks of data until the ARM bit is externally cleared to a low.

Bit 5 CRC – CRC Encoding Enable
When set high, the WD60C80 activates its internal 32-bit CRC generator on read and write operations for extended correction and lower miscorrection probability. It adds four extra bytes to each block, between the data field and the redundancy field.

When low (default after reset), it disables the CRC generator.

Bit 6 SCB – Syndrome Transfer on Controller Bus
When set high, the WD60C80 directs the syndrome byte output to the controller bus (CDx pins) during the read operation thus enabling the user to share a single RAM for storing read/write data and syndrome information. Notice the option is valid only if the DMA transfer option is selected on the Parameter Register.

The parity check/generation option therefore is not available. When this mode of operation is chosen, it is the system designer's responsibility to arbitrate the controller bus between the data/ECC transfer and syndrome transfer. Due to this overhead, the actual throughput of the bus tends to be low, and the application should be limited to a low transfer rate environment.

When it is low (default after reset), the device directs the syndrome bytes through the processor bus, and the external processor or DMA device can perform the transfer with either PIO or DMA option

Bit 7 FT – FIFO Threshold ON

When set high, the WD60C80 delays setting the SDRQ pin until at least 10 bytes are accumulated inside the syndrome FIFO. This guarantees the burst DMA transfer of at least 10 bytes, reducing bus arbitration overhead between the processor and the DMA device, when the bus bandwidth requirement is high.

When set low (default after reset), the device sets SDRQ every time there is a byte in the syndrome FIFO. In either case, the SDRQ will clear itself when the last byte in the FIFO is being read.

Parameter Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PRMR	PCD	SDH	DMA	PS1	PS0	IS2	IS1	IS0

The Parameter Register is a Read/Write register that is used to set the operating configuration of WD60C80.

Bit 0-2 IS0-2 – Interleave Factor Selection Code
These three bits are used to specify the interleave factor of the ECC. For more details on interleaving.

IS2	IS1	IS0	Interleave Factor
0	0	0	5 (Default after reset)
0	0	1	10
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	8
1	1	X	1 (i.e., no interleaving)
(X = Don't Care)			

Bit 3-4 PS0-1 – Polynomial Selection Code
These two bits are used to specify the ECC polynomials to be used for the WD60C80 operation.

PS1	PS0	Polynomial
0	0	Degree 16 (Default after reset)
0	1	Degree 8
1	X	Degree 4
(X = Don't Care)		

Bit 5 DMA – Syndrome DMA Transfer Option
(Parity Check/Generation Disable) If this bit is set high, it enables the DMA mode operation on the syndrome transfer during the read, and disables the parity checker/generator. The DMA mode and parity checking are mutually exclusive options, because they share the same pin (CDP/SDACK) for their function. For DMA mode operation, this pin functions as SDACK, along with SDRQ, to perform Request-Acknowledge protocol.

The syndrome bytes will be output through the processor or the controller bus depending on the selection made in the Command Register. Notice this is the only way to direct the syndrome to the controller bus.

If this bit is set low (default after reset), then the syndrome transfer is performed in PIO (Programmed I/O) mode, where the external processor/DMA device accesses the syndrome FIFO as an internal register through the processor bus. An ALE pulse must be used to latch the address of the syndrome FIFO (0E Hex), then the device activates $\overline{CS}$ and $\overline{RE}$ to read it. Notice that to properly shift the internal FIFO pointer, $\overline{CS}$ $\overline{RE}$ pulse width must be wider than two FCLK cycles. In this mode, the CDP/SDACK pin becomes

the parity bit for the controller bus (CDx pins). When a byte is output from this bus, an odd parity (the total number of "high" bits in the nine bit field is odd) is output on this pin. If parity check is also enabled (see PCD bit), the WD60C80 will inspect the incoming data for odd parity (odd number of "high" bits at the CD0-CD7 and CDP pins) at the trailing edge of $\overline{\text{CDACK}}$ signal (input).

Using the PIO access method, the external processor can read the syndrome FIFO regardless of DMA bit setting. However, it can upset the byte count of the a DMA device if the processor tries to read the FIFO concurrently.

Bit 6 SDH – SDACK Pin Polarity Option (High Active)

This bit is used to control the polarity of SDACK pin, when DMA option is selected. When set high, the SDACK becomes a high active signal.

If set low, it becomes a low active signal, much like the $\overline{\text{CDACK}}$ pin. It defaults to active low after reset.

Bit 7 PCD – Parity Check Disable Option

This bit disables the parity checker, while leaving the parity generator ON. In order for this bit to be effective, the DMA bit must be set low, or both parity checker and generator is disabled.

After reset, this bit is set low, enabling the parity checker.

Sector Size Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SSRO	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
SSR1					SS11	SS10	SS9	SS8

(INTERLEAVE FACTOR + 1) ≤ (SSR) ≤ (INTERLEAVE FACTOR X 255) – 1

The Sector Size Register is a Read/Write register that is used to set the length of the data field of a block. The register is 12-bit long, divided into the least significant 8-bit and the most significant 4-bit registers. The external processor is expected to set these registers to (number of data bytes - 1) prior to ARMing the device.

The contents of these registers are not decremented on each byte transferred, but rather, used to compare with the output of the internal data byte counter. Therefore, once they are loaded, the value stays intact until another value is loaded. This makes it convenient for multiple sector operation.

Example:

In order to set for the data field length of 1,024 bytes,
(Sector Size Register) = 1,024 - 1 = 1,023 = 3FF Hex
Store FF Hex to SSR0
Store 03 Hex to SSR1

Although it is a 12-bit register, the maximum data field length is limited to 255 times the specified interleave factor. This limitation is imposed by the finite field theory, which limits the length of any interleave to be less than or equal to 255 bytes due to the usage of coefficients from GF(256). The WD60C80 hardware requires at least one byte of data in each interleave to insure proper operation, therefore the minimum data field length is one plus the interleave factor. Violation of this rule may lead to all-zero CRC and all-FF(Hex) ECC bytes.

Example:

If degree 16, 10 interleave is selected,
11 ≤ (SECTOR SIZE REGISTER) ≤ 2,389.
The total sector length (less ID field) is:
(SECTOR SIZE REGISTER) + 1 + 4 (CRC BYTES) + 160 (ECC BYTES)

(SECTOR SIZE REG) + 1	4	160 Bytes
DATA FIELD	CRC	ECC

Status Registers

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
STRO	N/U	N/U	PERR*	DFO*	SFO	EERR	SDRQ!	BUSY!
STR1	I7E	I6E	I5E	I4E	I3E	I2E	I1E	I0E
STR2	N/U	CERR	PERR*	DFO*	SFO	EERR	I9E	I8E

N/U = Not Used

All bits are cleared at the end of the data field except:
* marked bits clear at the end of the current block.
! marked bits are real time signals and not latched.

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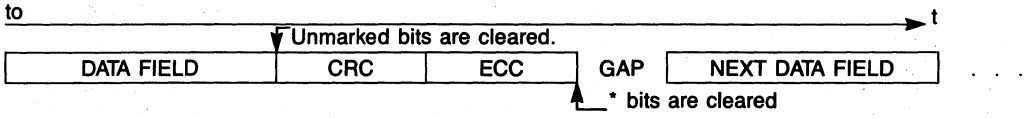


The Status Registers are Read-Only registers that report operational status and error conditions of WD60C80. The values of STR1 and STR2 at the end of each block are also sent to the syndrome FIFO to be read by the host processor during read or write operations to check for any failures. STR0 is intended for general checking of the operational status of the device, so a few bits of information are covered in both STR0 and STR2.

Byte 0 Bit 0 BUSY – Device Busy
This is a real time signal indicating the active status of the WD60C80. When ARM = 1 is written to the command register, this bit is set high, indicating the active status. When a single sector operation is specified, this bit is cleared at the end of each block. Otherwise it stays ON until the ARM bit is externally cleared or reset/abort is activated.

Byte 0 Bit 1 SDRQ – Syndrome Transfer DMA Request

This is a real time signal indicating the syndrome FIFO has syndrome/status bytes inside and ready for transfer. This is similar to the SDRQ pin, except it ignores the FIFO threshold option. It is intended to be used with the PIO mode of syndrome transfer operation.

Byte 0 Bit 2 EERR – ECC Error Found
Byte 2 Bit 2
This is a latched status indicating that during the read operation, the device found a discrepancy(ies) between the internally generated ECC and retrieved ECC.

When this bit is set high, one or more of the "Interleave n in error" bits should also be set high. If there is an error(s), this bit is set during the ECC field of the block in question, and stays valid until the end of the data field of the next block.

Byte 0 Bit 3 SFO – Syndrome FIFO Overflow
Byte 2 Bit 3
This is a latched status indicating that during the read operation, the syndrome FIFO suffered an overflow due to insufficient access by the processor or DMA device. A syndrome byte is generated every time a redundancy byte is received and processed, and the system is expected to read them out at least at the data rate. The syndrome FIFO is 20-byte deep to smooth out the traffic on the bus, but most operations generate more than 20 bytes of syndrome/status. When an overflow occurs, the syndrome transfer logic still delivers the correct number of bytes, but there will be several garbage bytes among those transferred. This bit stays valid until the end of the data field of the next block.

Byte 0 Bit 4 DFO – Data FIFO Overflow
Byte 2 Bit 4
This is a latched status indicating that during the read or write operation, the data FIFO suffered an overflow, due to excessive transfer on the controller bus, or the FCLK frequency is too low. The device is expected to be clocked at least eight times the required data rate in byte/sec, and it is capable of supporting a 10-byte burst of 1/5 the clock frequency. Since the WD60C80 does not have any means of handshaking during the data read phase, any transfer rate adjustment must be made between the buffer manager and the target device, such as a disk controller, on the controller bus. When the overflow occurs, the device typically appears to be operating properly, except it has this error flag set and most likely generates wrong CRC and ECC codes. This bit stays valid till the end of the current block.

Byte 0 Bit 5 PERR – Parity Error Detected on Controller Bus

Byte 2 Bit 5
This is a latched status indicating parity error detection on the controller bus during the read or write operation. During the data read phase (if PIO option is selected and Parity Check is enabled), the WD60C80 checks for odd parity on the controller bus at the trailing edge of the $\overline{\text{CDACK}}$ signal (input). An odd parity is when you an have odd number of "high" bits in the nine-bits field (CD0-CD7, CDP). If any error is detected, this flag is set and stays valid until the end of the current block. This error flag, however, does not disturb other operations of the device, so its operation will complete as normal. It is the responsibility of the system firmware to analyze and recover from the error.

Byte 1 Bit 0 I0E – Interleave 0 in Error
This is a latched status indicating an ECC error(s) is detected in the first interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 1 I1E – Interleave 1 in Error
This is a latched status indicating an ECC error(s) is detected in the second interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 2 I2E – Interleave 2 in Error
This is a latched status indicating an ECC error(s) is detected in the third interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 3 I3E – Interleave 3 in Error
This is a latched status indicating an ECC error(s) is detected in the fourth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 4 I4E – Interleave 4 in Error
This is a latched status indicating an ECC error(s) is detected in the fifth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 5 I5E – Interleave 5 in Error
This is a latched status indicating an ECC error(s) is detected in the sixth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 6 I6E – Interleave 6 in Error
This is a latched status indicating an ECC error(s) is detected in the seventh interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 7 I7E – Interleave 7 in Error
This is a latched status indicating an ECC error(s) is detected in the eighth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 0 I8E – Interleave 8 in Error
This is a latched status indicating an ECC error(s) is detected in the ninth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

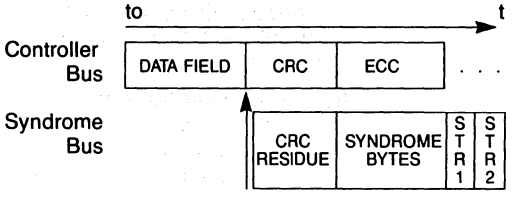
Byte 2 Bit 1 I9E – Interleave 9 in Error
This is a latched status indicating an ECC error(s) is detected in the tenth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 6 CERR – CRC Error Detected
This is a latched status indicating a CRC error is detected during the read operation. The processor should be able to find non-zero CRC residue. This bit is set during the CRC field and stays valid until the end of the data field of the next block.

Syndrome FIFO

Syndrome FIFO is a Read-Only 20-byte deep FIFO register used to transfer syndrome / status bytes during the read operation. It can be accessed either in DMA or in PIO mode, by setting up the Parameter Register properly. Even if it is set up for DMA mode transfer, the processor can still read it through PIO mode access, but the reverse is not true. Its status is indicated by the SDRQ pin and the SDRQ bit in the status register byte 0.

Timing Relationship between the Data flow and Syndrome Transfer



Syndrome FIFO cleared

During the read operation, the host must read through this FIFO, four bytes of CRC residue (if CRC option is set), syndrome bytes (number of bytes varies depending on the ECC polynomial and the interleave factor) and two bytes of final status (copies of status register byte 1 and 2, at the end of the block), in that order. During the CRC and ECC field, one byte is generated every eight FCLK cycles, and accumulated in this FIFO. It is the host's responsibility to read them out before the FIFO overflow occurs, or he can lose several syndrome bytes.

Number of Syndrome Bytes generated

	Interleave Factors							
Polynomial	**1**	**2**	**3**	**4**	**5**	**8**	**10**	
Degree 16	16	32	48	64	80	128	160	
Degree 8	8	16	24	32	40	64	80	
Degree 4	4	8	12	16	20	32	40	(Bytes)

(Total # of bytes to be transferred)
= CRC Residue (4) + Syndrome Bytes + Status Bytes (2)

During the write operation, no syndrome bytes are generated, but two bytes of final status are reported through this FIFO at the end of each block.

Regardless of FIFO threshold option, SDRQ will be set high (true) at the end of the block.

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The syndrome FIFO is cleared of its contents at the end of the data field of every block. So the external host has until the end of the next data field to finish reading the syndrome bytes, as long as there is no FIFO overflow.

The host can read them out as fast as one fifth of the clock frequency, but care must be taken to insure the $\overline{CS}$ $\overline{RE}$ pulse width (PIO mode) or SDACK width (DMA mode) to be more than 2.0 clock cycles. The supported DMA protocol is the slave side of demand driven burst transfer (i.e., SDRQ stays high (true) as long as there is a byte in the FIFO), and the external master DMA device can read them out in a burst, until SDRQ clears.

If, for any reason, the DMA device tries to read the syndrome FIFO when SDRQ is not set, not only it is likely to get a garbage byte, but that may also also upset the internal FIFO pointer, thereby making the next-to-be-read syndrome byte inaccessible. This situation is not reported in the status register, so one must be careful to insure sufficient setup and hold time for the DMA protocol.

DC ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings indicate where permanent damage to the device may occur if exceeded. Continuous operation at these limits is not intended and should be avoided.

Operating Temperature ..... 0°C (32°F) to 70°F (158°F)
Storage Temperature ..... −55°C (−67°F) to +125°C (257°F)
Minimum Voltage on any pin with respect to V_{SS} ..... −0.3V
Maximum Voltage on any pin with respect to V_{DD} ..... +0.3V
V_{DD} with respect to V_{SS} ..... +7.0V

DC OPERATING CHARACTERISTICS

The following characteristics apply to the WD60C80 device in the given conditions, in the ambient temperature between 0°C and 70°C.

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
V_{DD}	Power Supply Voltage	4.50	5.00	5.50	V	[1]
I_{DD}	Power Supply Current			25.0	mA	[1]

[1] Ta = 0°C, FCLK frequency = 25.0 MHz, all outputs open.

FOR ALL INPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{IL}	Input Leakage Current			10.0	μA	[2]
V_{IL}	Input Low Level Voltage			0.8	V	
V_{IH}	Input High Level Voltage	2.0			V	

[2] Input Voltage = V_{DD}

FOR ALL OUTPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{OZ}	Output Leakage Current			10.0	μA	[3]
V_{OH}	Output High Level Voltage	2.8 2.8			V V	[4] [6]
V_{OL}	Output Low Level Voltage			0.4 0.4	V V	[5] [7]

[3] Output Voltage = V_{DD}
[4] Applies to AD0 through AD7 pins only. Io = −2.5 mA
[5] Applies to AD0 through AD7 pins only. Is = +6.0 mA
[6] Applies to all other output/bidirectional pins. Io = −1.0 mA
[7] Applies to all other output/bidirectional pins. Is = +2.0 mA

DC OPERATING CHARACTERISTICS (continued)

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{LU}	Latch Up Current	±40			mA	

AC TIMING CHARACTERISTICS

REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING

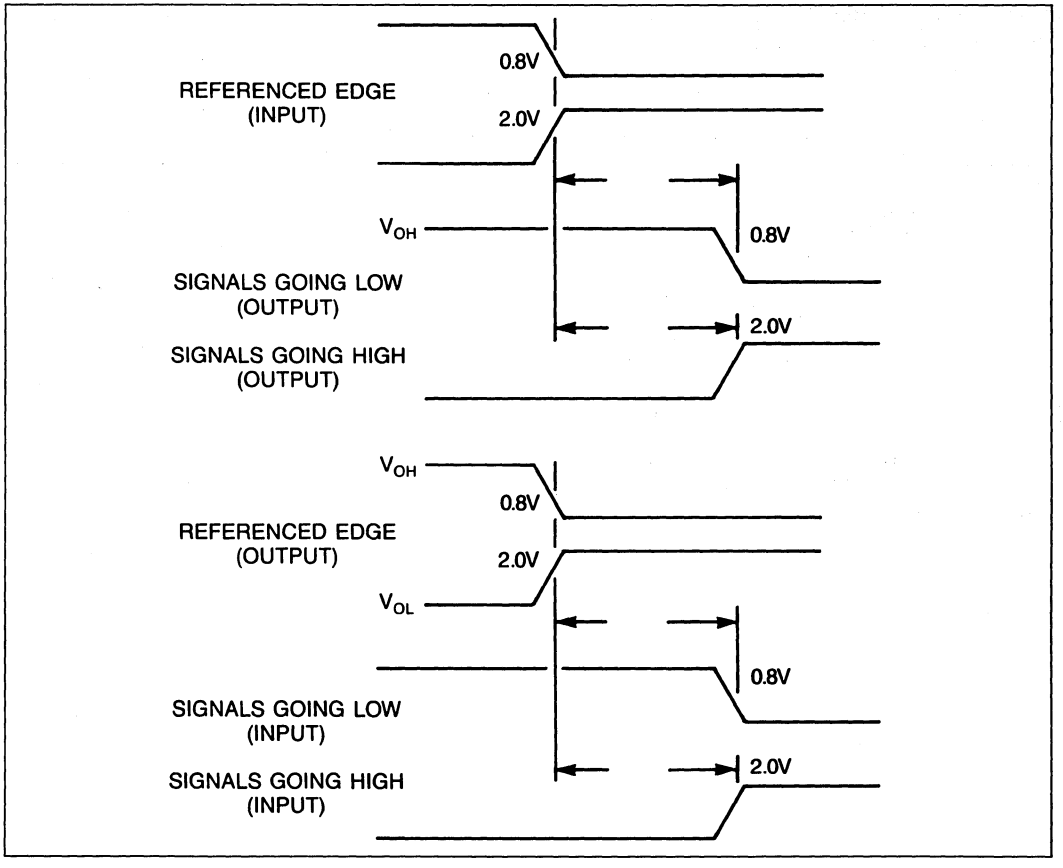
* Reference Number on the Timing Waveform Diagram.

* Abbreviated Symbol the Timing is Referred.

* The Reference Edge to which the Timing is Specified.
  L.E. = Leading Edge
  T.E. = Trailing Edge
  I.C. = Initial Condition

* Classification of Requirement/Specification
  R = Requirement on the External Interface
  S = WD60C80 Output Timing Specification

All the timing specifications assume the voltage levels shown below.
Capacitive loading on AD0-AD7 pins are 100 pF, and all other outputs are 50 pF.



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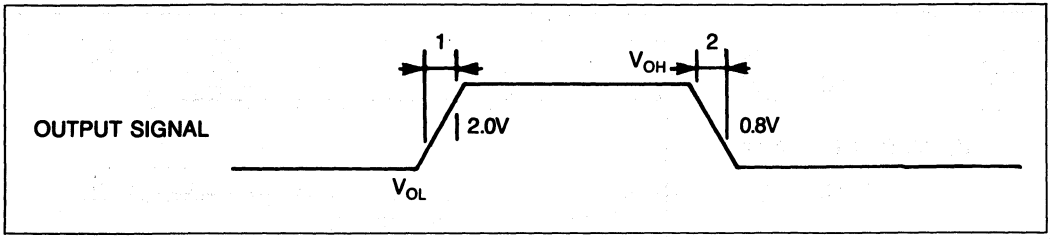
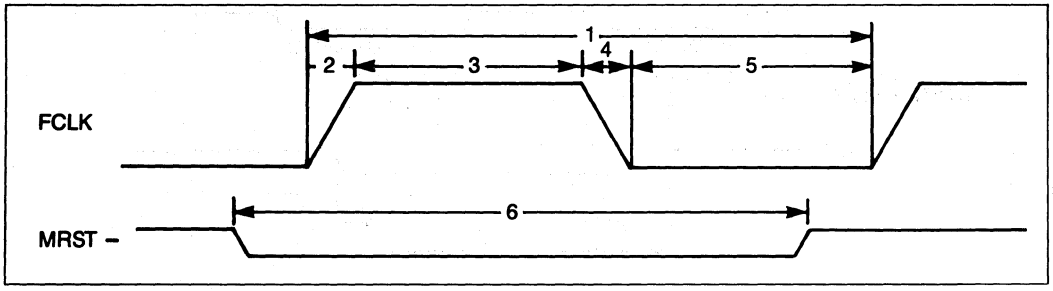


REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	TR	Output Rise Time	From V_{OL} to 2.0V	S	25 nsec Max
2	TF	Output Fall Time	From V_{OH} to 0.8V	S	25 nsec Max

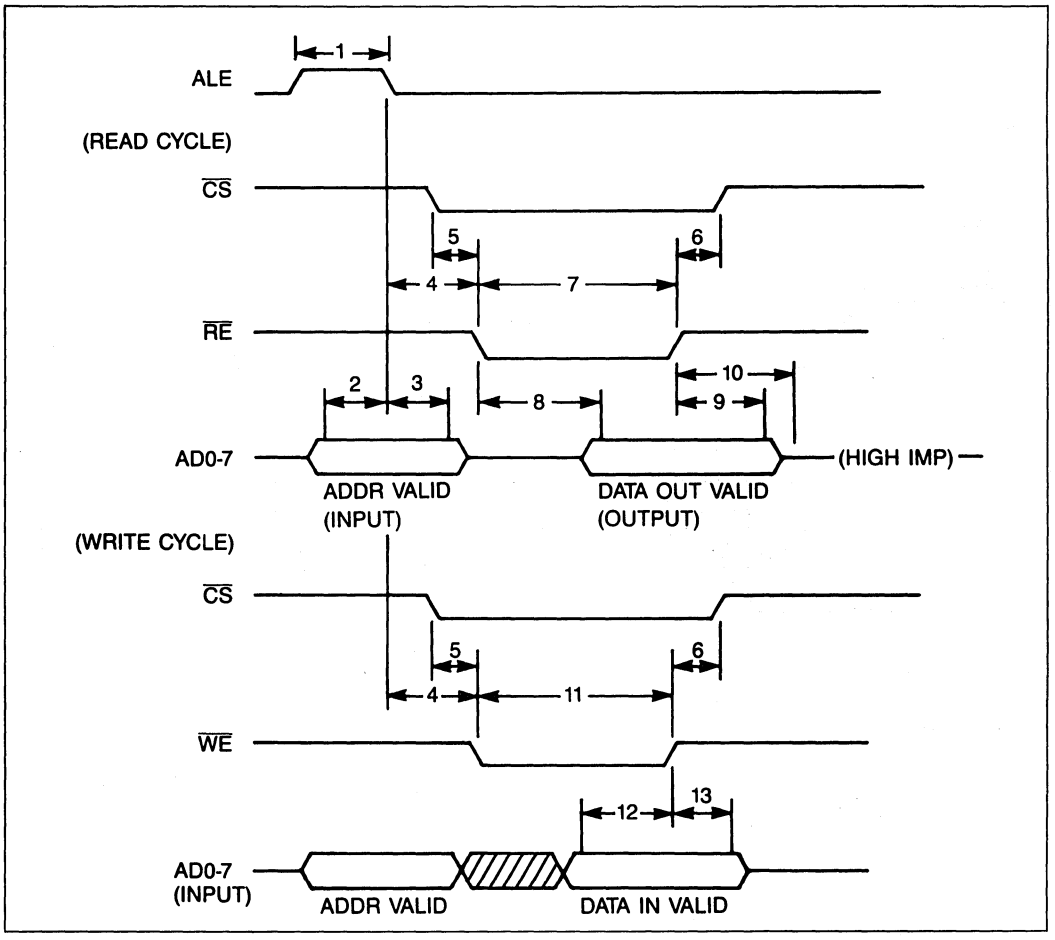
OUTPUT RISE/FALL TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	CLK	FCLK Cycle Time*		R	40 nsec Min [1]
				R	60 nsec Min [2]
2	TCR	FCLK Rise Time		R	10 nsec Max
3	TCH	FCLK High Time		R	.4 CLK Min
4	TCF	FCLK Fall Time		R	10 nsec Max
5	TCL	FCLK Low Time		R	.4 CLK Min
6	TMR	$\overline{MR}$ Pulse Width		R	80 CLK Min

* This specification is used to define several other timings.
[1] The maximum clock frequency is 25 MHz if Degree 4 or Degree 8 polynomial is selected.
[2] If the Degree 16 polynomial is selected, the maximum clock frequency is 16.7 MHz.

CLOCK/RESET TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TALW	ALE Pulse Width		R	50 nsec	Min
2	TADS	Address Setup Time	Before T.E., ALE	R	15 nsec	Min
3	TADH	Address Hold Time	After T.E., ALE	R	15 nsec	Min
4	TRWD	RE/We Setup Time	After T.E., ALE	R	15 nsec	Min
5	TCSE	$\overline{CS}$ Setup Time	Before L.E., RE/WE	R	0 nsec	Min
6	THLD	$\overline{CS}$ Hold Time	After T.E., RE/WE	R	0 nsec	Min
7	TRE	$\overline{RE}$ Pulse Width		R	120 nsec	Min
					2.0 CLK	Min [1]
8	TDAC	Data Output Delay	After L.E., $\overline{RE}$	S	95 nsec	Max
9	TDOH	Data Hold Time	After T.E., $\overline{RE}$	S	20 nsec	Min
10	TDOT	Data Bus High imp.	After T.E., $\overline{RE}$	S	75 nsec	Max
11	TWE	$\overline{WE}$ Pulse Width		R	130 nsec	Min
12	TDS	Data Setup Time	Before T.E., $\overline{WE}$	R	50 nsec	Min
13	TDH	Data Hold Time	After T.E., $\overline{WE}$	R	10 nsec	Min

[1] This restriction applies only when reading the syndrome FIFO.

TASKFILE ACCESS TIMING
(Including PIO mode Syndrome Transfer)

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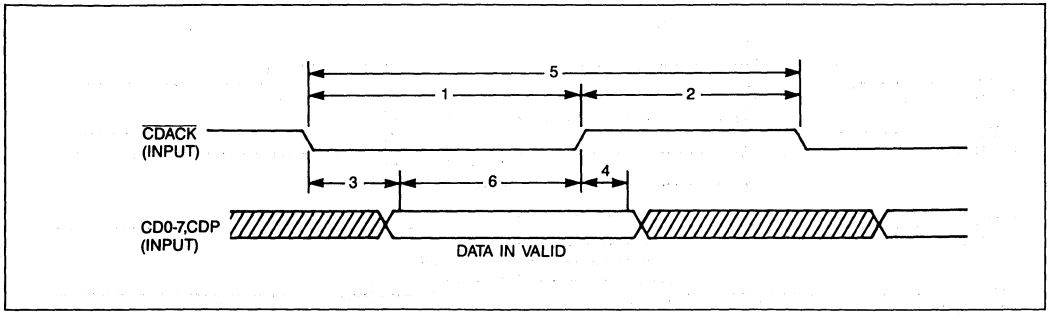
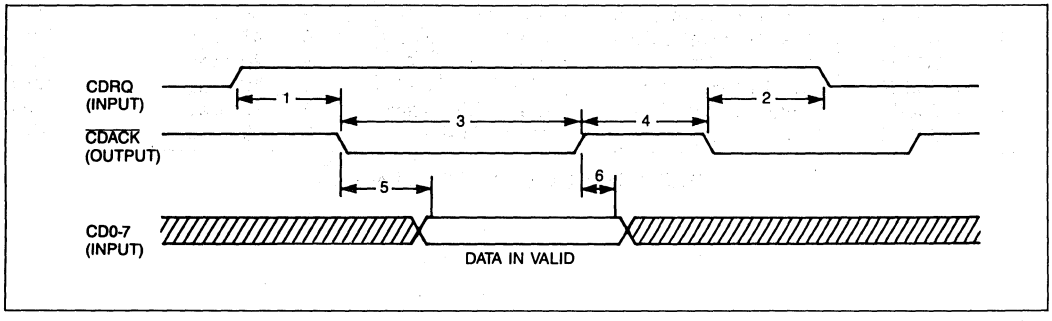
CONTROLLER BUS TIMING



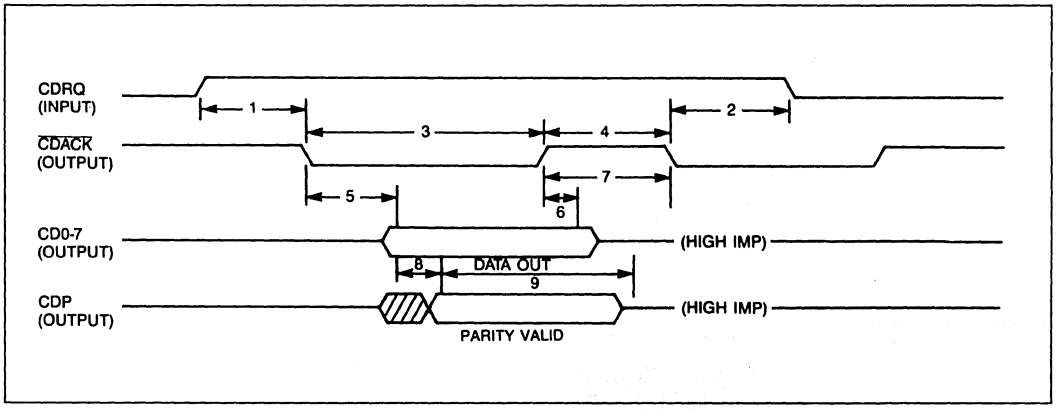
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDK1	CDACK INP Pulse Width		R	2.0 CLK + 10nsec	Min
					100 μsec	Max
2	TCDC1	Transfer Recovery Time	After T.E. CDACK	R	2.0 CLK + 20 nsec	Min
3	TACC1	Data Access Time	After L.E. CDACK	R	4.0 CLK – 80 nsec	Max
4	TCDH1	Data Hold Time	After T.E. CDACK	R	10 nsec	Min
5	TCCDK	Transfer/Cycle Time	Between L.E. CDACK	R	5.0 CLK	Min
6	TCDS1	Data Setup Time	Before T.E. CDACK	R	40 nsec	Min

REDUNDANCY READ TIMING



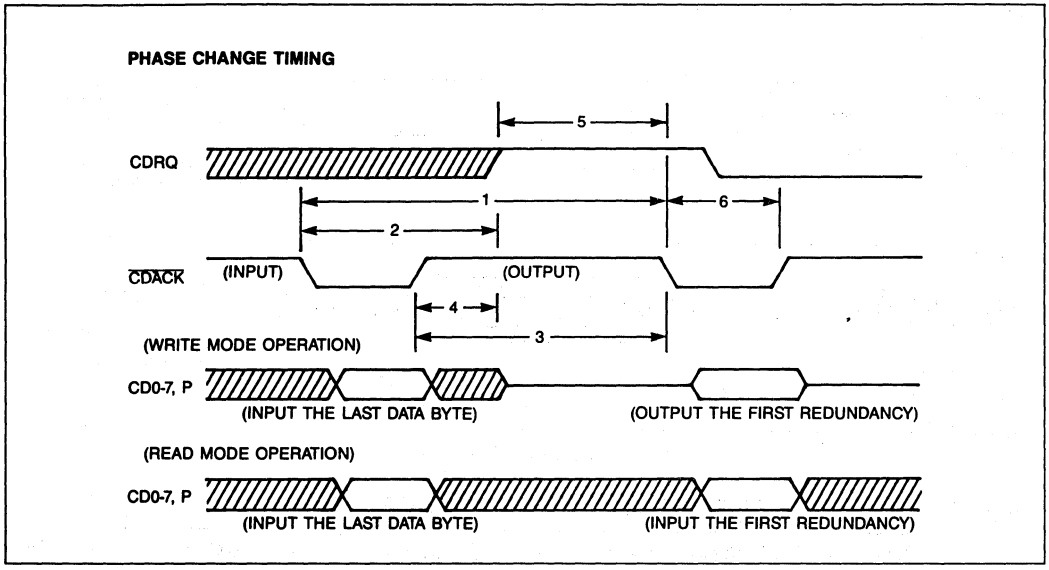
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., DRQ	S	2.0 CLK	Min
					4.0 CLK + 20 nsec	Max
2	TDRR	CDRQ Reset Timing	After L.E., CDACK	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TDCD2	CDACK Recovery Time	After T.E., CDACK	S	2.0 CLK	Min
5	TACC2	Data Valid Delay Time	After L.E., CDACK	S	4.0 CLK – 80 nsec	Max
6	TCDH2	Data Hold Time	After T.E., CDACK	S	10 nsec	Min

DATA READ TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., CDRQ	S	2.0 CLK	Min
					4.0 CLK + 20 nsec	Max
2	TDRR	CDRQ Reset Timing	After L.E., $\overline{\text{CDACK}}$	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TCDC2	CDACK Recovery Time	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK	Min
5	TCDD	Data Valid Delay Time	After L.E., $\overline{\text{CDACK}}$	S	45 nsec	Max
6	TCDH2	Data Hold Time	After T.E., $\overline{\text{CDACK}}$	S	20 nsec	Min
7	TCDOT	Data Bus High Imp.	After T.E., $\overline{\text{CDACK}}$	S	50 nsec	Max
8	TCDPD	Parity Bit Delay Time	After CD0-7 Valid	S	20 nsec	Max
9	TCDPT	Parity Bit High Imp.	After CD0-7 H.I.	S	10 nsec	Max

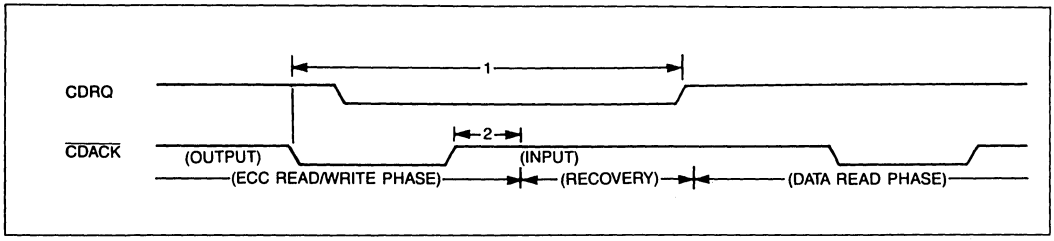
REDUNDANCY OUTPUT TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
***WRITE Mode Operation (Assumes FIFO empty prior to receiving the last data)**					
1	TSOLW	Switch Over Cycle Time	After L.E., $\overline{\text{CDACK}}$	S	10.0 CLK Min [1] 12.0 CLK + 25 nsec Max [1]
2	TCDLW	$\overline{\text{CDACK}}$ Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	4.0 CLK Min [2] 6.0 CLK + 25 nsec Max [2]
3	TSOTW	Switch Over Delay	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK Min
4	TCDTW	$\overline{\text{CDACK}}$ Direc. Reversal	After T.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min
***READ Mode Operation (Assumes FIFO not full after receiving the last data)**					
1	TSOLR	Switch Over Cycle Time	After L.E., $\overline{\text{CDACK}}$	S	6.0 CLK Min [1] 8.0 CLK + 24 nsec Max [1]
2	TCDLR	$\overline{\text{CDACK}}$ Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	4.0 CLK Min [2] 6.0 CLK + 25 nsec Max [2]
3	TSOTR	Switch over Delay	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK Min
4	TCDTR	$\overline{\text{CDACK}}$ Direc. Reversal	After T.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min
***WRITE/READ Operations**					
5	TCDD	$\overline{\text{CDACK}}$ Synchro Delay	After L.E., CDRQ	S	4.0 CLK + 20 nsec Min [3]
6	TCDK2	$\overline{\text{CDACK}}$ Out Pulse Width		S	4.0 CLK − 40 nsec Min

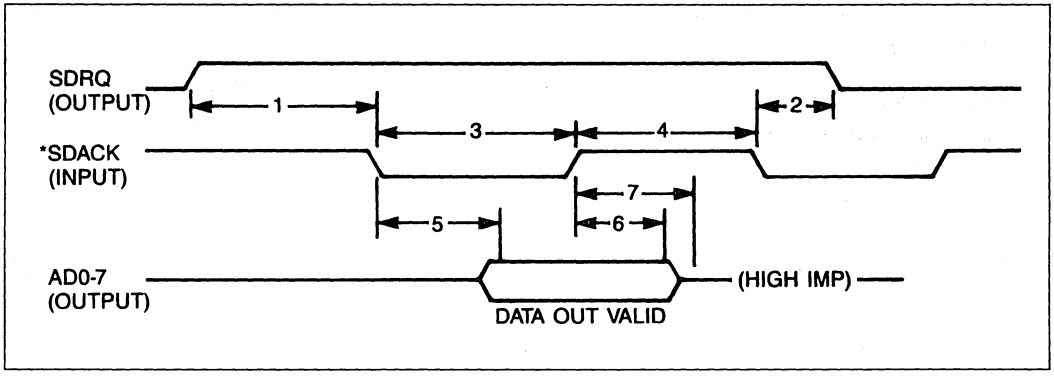
[1] This specification applies if TSOTR/W is met.
[2] This specification applies if TCDTR/W is met.
[3] This specification supercedes TSOLR/W and TCDLR/W.

PHASE CHANGE TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	TSWI	Interblock Gap Time	After L.E., $\overline{\text{CDACK}}$	R	15.0 CLK Min (Write OP) 47.0 CLK Min (Read OP)
2	TCDI	CDACK Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min

INTER-BLOCK GAP TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD1	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S	80 nsec	Max
3	TSDK1	SDACK Pulse Width		R	3.0 CLK	Min
4	TSDC1	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA1	Data Output Delay	After L.E., SDACK	S	85 nsec	Max
6	TSDH1	Data Hold time	After T.E., SDACK	S	40 nsec	Min
7	TSDT1	Data Bus High Imp.	After T.E., SDACK	S	85 nsec	Max

DMA TRANSFER TIMING (SYNDROME ON PROCESSOR BUS)

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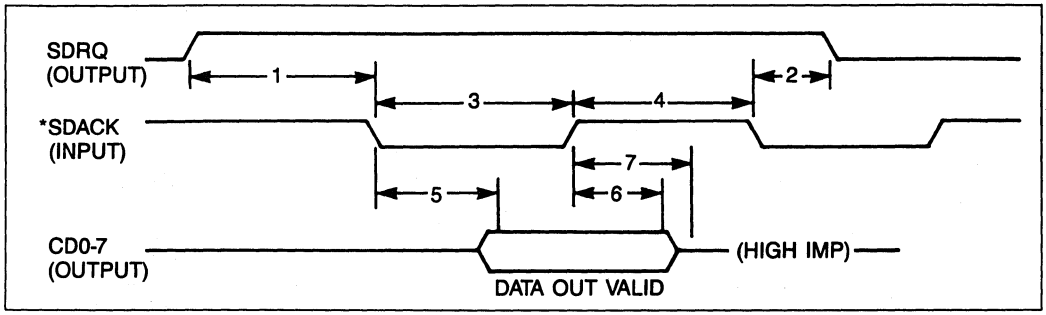
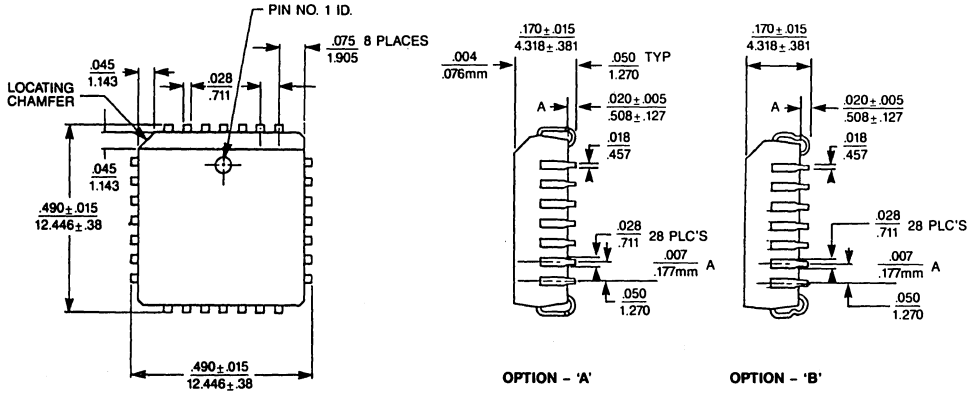


REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD2	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S		
3	TSDK2	SDACK Pulse Width		R	4.0 CLK	Min
4	TSDC2	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA2	Data Output Delay	After L.E., SDACK	S	110 nsec	Max
6	TSDH2	Data Hold Time	After T.E., SDACK	S	40 nsec	Max
7	TSDT2	Data Bus High Imp.	After T.E., SDACK	S	120 nsec	Max

* SDACK low active option is shown.

SYNDROME TRANSFER TIMING (SYNDROME ON CONTROLLER BUS)

PACKAGE INFORMATION



28 LEAD PLASTIC "JH"

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WD61C23A

High Performance

Hard Disk Controller

WESTERN DIGITAL

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1.0 DESCRIPTION

The WD61C23A is a high integration, high performance, low cost controller for hard disk drives. This device contains XT and AT interfaces, buffer manager, and disk data formatter. The disk data formatter only controls the formatting and serialization of the disk drive data. Head positioning, head selection, etc. are expected to be supported by other devices. This device, together with the WD61C12 servo/spindle controller and the WD10C27 ENDEC/Data Synchronizer/Frequency Synthesizer device, forms a high performance, high integration chip set for embedded drives.

1.1 FEATURES

1.1.1 Host Interface

- Compatible with PC/AT and PC/XT interfaces
- Supports PC/AT I/O speeds up to 16 MHz
- Internal 24 mA drivers and Schmitt-trigger receivers for direct connection to the PC/XT or PC/AT system bus
- Host transfer rates up to 5 Mwords/sec (10 Mbyte/sec)
- Master/slave mode allows two AT drives on one connector. Hardware ignores host commands when drive is not selected.
- DMA and PIO data transfers. Supports EISA-type B DMA (4 Mbytes/sec).
- Automatic DRQ assertion in AT mode for Write, Write Buffer, Write Long, and Format commands
- Automated Task File update in AT mode for Read, Write, Read Multiple, and Write Multiple commands allows multiple sectors to be transferred without microcontroller intervention. Programmable delay from end of transfer to next HIRQ pulse
- Directly support AT IDE, two-chip select interface or standard AT, one-chip select, four address interface
- PCMCIA interface support ($\overline{\text{HIRQ}}$ and HRST polarity control
- Supports non-AT compatible DRQ enable bit in Fixed Disk Register
- Guaranteed wide index status to AT host
- High current I/O ports to handle $\overline{\text{PDIAG}}$ and $\overline{\text{DASP}}$ controls in AT mode
- Reset control logic combines hard and soft resets from host and generates either system reset, microcontroller interrupt, or both

1.1.2 Buffer Manager

- Direct interface for up to 256 Kbytes of static RAM
- Up to 13.5 Mbyte/sec RAM bandwidth (27 MHz crystal)
- Supports scatter-gather and segmented caching
- Multisector arming of buffers reduces firmware overhead requirements
- Supports Write Caching (allows control of auto-DRQ buffer address)
- Automatic segment wrap control for segment sizes from 4 Kbytes to 256 Kbytes
- 24 byte host FIFO and 12 byte disk FIFO

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1.1.3 SERDES

- Data rate of 27 Mbps NRZ
- Supports embedded servo
- Proprietary data field segmentation allows for optimal selection of servo sample frequency, ZBR support, and defect management. Up to four segments per data field.
- Multiple defect management schemes supported: byte level push-down, sector level push-down, and sector relocation.
- Software selectable 56-bit ECC, 32-bit ECC, or 16-bit CRC for data fields
- Degree 6, 3-way interleaved Reed Solomon ECC with inlaid 32-bit CRC. Can correct single bursts up to 17-bits on-the-fly without microcontroller intervention. Can correct up to nine random bytes using software correction.
- Data Byte Sync redundancy
- ID redundancy
- Software selectable 32-bit ECC or 16-bit CRC for ID fields
- Supports both CHS (cylinder, head, sector) and LBA (logical block address) ID formats. Autoincrement of three byte LBA for multisector commands.
- Supports sector size up to 4096 bytes (743 with Reed-Solomon ECC)
- Supports 5-bit head number field and 12-bit cylinder number field in CHS mode
- Dual-port register file allows full time access to the SERDES state
- Fast abort of SERDES execution
- WF/WUS filter and asynchronous WF/WUS latching
- Automatic power-down of SERDES when idle

1.1.4 Miscellaneous

- Supports Intel-type and Motorola-type microcontrollers. Muxed address/data bus.
- Compatible with the newer high performance microcontrollers such as the Siemens 80C166 and the NEC 78K6 series.
- Programmable $\overline{\text{MCINT}}$ polarity
- All interrupt sources are individually maskable
- $\overline{\text{MCS}}$ pin can be tied to the same source as the WD61C12 and WD10C27 for simpler interfacing to microcontrollers
- Version number of part posted in disk data formatter register after reset
- Internal crystal oscillator
- Low power sleep modes: maximum 50 mW Idle1, 25 mW Idle2, 2.5 µW Standby power
- Direct control of external FET to power drive circuits
- Low power 1.25 micron CMOS design
- Available in 100-pin MQFP and SQFP packages

2.0 SIGNAL DESCRIPTION

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
3	100	BA15	O	**Buffer Address 15** Buffer address when connected to 64K x 4, 128K x 8, or 256K x 4 SRAM devices.
		$\overline{\text{BCS0}}$	O	**$\overline{\text{Buffer Chip Sel 0}}$** Buffer RAM chip select when connected to two 32K x 8 SRAM devices.
4	1	BA16	O	**Buffer Address 16** Buffer address when connected to 128K to 256K bytes of SRAM.
		$\overline{\text{BCS1}}$	O	**$\overline{\text{Buffer Chip Sel 1}}$** Buffer RAM chip select when connected to two 32K x 8 SRAM devices.
5	2	BA17	O	**Buffer Address 17** Buffer address when connected to 256 Kbytes of SRAM.
6	3	HCIO2	I/O	**High Current I/O 2** This is a 24 mA open drain output which can be used for the DRIVE ACTIVE/SLAVE PRESENT ($\overline{\text{DASP}}$) signal on the AT IDE cable. HCIO2 can also be used as an open drain general purpose I/O.
7	4	$\overline{\text{CS0}}$/HA9	I	**$\overline{\text{Chip Select 0}}$** This signal is decoded from the AT/XT bus and is used to qualify $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ when accessing the Control Block Registers.
8	5	$\overline{\text{CS1}}$/$\overline{\text{HCS}}$	I	**$\overline{\text{Chip Select 1}}$** This signal is decoded from the AT address bus and is used to qualify $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ when accessing the Control Block Registers. $\overline{\text{CS1}}$ is ignored in XT mode.
9	6	HCIO1	I/O	**High Current I/O 1** This is a 24 mA open drain output which can be used for the Passed Diagnostic ($\overline{\text{PDIAG}}$) signal on the AT IDE cable. HCIO1 can also be used as an open drain general purpose I/O.

TABLE 2-1. SIGNAL DESCRIPTION

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NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
10	7	$\overline{\text{IOCS16}}$	O	**$\overline{\text{I/O Chip Select 16}}$** This output is used to indicate fast 16-bit data transfers in AT mode. It is asserted for all PIO Data Port transfers except for ECC byte transfers. It can optionally be used in DMA mode to suppress wait states during DMA cycles.
11	8	HIRQ/$\overline{\text{HIRQ}}$	O	**Interrupt Request /$\overline{\text{Interrupt Request}}$** HIRQ indicates to the PC/AT or PC/XT that a data block transfer is requested or a command has been completed. $\overline{\text{HIRQ}}$ is the active low version of this function, if HPOL = 1
12	9	DREQ	O	**DMA Request** This signal is used in DMA mode to control data transfers. This output is tristated at power-up.
13	10	$\overline{\text{DACK}}$	I	**$\overline{\text{DMA Acknowledge}}$** DACK is asserted by the Host in response to the DREQ signal assertion in order to complete the DMA handshake. It qualifies IOR and IOW during DMA Data Port transfers.
14	11	NC	NA	**No Connect** No Connection.
15	12	VSS	NA	**Ground** Ground
16	13	VDD	NA	**+5V** + 5V
17	14	$\overline{\text{IOR}}$	I	**$\overline{\text{IOR Read}}$** IOR is asserted by the PC/AT or PC/XT host together with CS0, CS1, or DACK to read an internal register or the FIFO.
18	15	$\overline{\text{IOW}}$	I	**$\overline{\text{I/O Write}}$** IOW is asserted by the PC/AT or PC/XT host together with CS0, CS1, or DACK to write an internal register or the FIFO.
19-26	16-23	HD15 THRU HD8	I/O	**Host Data 15 thru Host Data 8** These eight pins are used for the upper byte of 16-bit host data transfers. When in 8-bit mode these pins are optionally terminated to Vcc interally.
27	24	VSS	NA	**Ground** Ground.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
28	25	HRST/	I	**Host Reset** This input, when asserted will reset the WD61C23A and cause a reset interrupt to the microcontroller. Assertion of this input will cause RESET to be asserted when the DRO control bit is 0.
		HRST		**Host Reset** HRST is the active high version of this function, if HPOL = 1.
29 30 31	26 27 28	HA1 HA0 HA2	I I I	**Host Address 1, Host Address 0, Host Address 2** These three inputs are used to select which internal host register is selected. The register set is a function of the AT/XT mode select bit. HA2 is not used in XT mode.
32	29	VSS	NA	**Ground** Ground.
33-40	30-37	HD7 THRU HD0	O	**Host Data 7 thru Host Data 0** These eight pins are used to transfer 8-bit data as well as to access the host registers.
41	38	VDD	NA	**+ 5V** + 5V
42	39	VSS	NA	**Ground** Ground.
43	40	SCT	I	**Sector** In hard sector mode SCT is used to indicate the start of a sector. It also indicates the position of embedded servo burst when data field segmentation is used.
44	41	IDX	I	**Index** Index input is used to define the beginning of a track.
45	42	SGATE	I	**Servo Gate** SGATE is an input from the servo control which is asserted over the servo fields. It is used to disable the AME/AMD handshake as well as to inhibit RWB over the servo fields.
46	43	WF/WUS	I	**Write Fault/Write Unsafe** Schmitt-triggered Write Fault/Write Unsafe input.
47	44	RWB	O	**Read/Write** RWB is an open drain output used to control the pulse detector and head preamp.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
48	45	ALE	I	**Address Latch Enable** ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0).
49	46	$\overline{MRE}$	I	**$\overline{Microcontroller\ Read\ Enable}$** MRE is asserted by the local microcontroller to read an internal register or the buffer.
		DS	I	**Data Strobe** DS is used by Motorola-type microcontrollers to enable the data transfer.
50-57	47-54	AD0 THRU AD7	I/O	**Address/Data 0 thru Address/Data 7** The multiplexed address/data lines are used to load the register address on the falling edge of ALE, and are used for data transfers to/from the local microcontroller.
58	55	$\overline{MCS}$	I	**$\overline{Microcontroller\ Chip\ Select}$** This signal is decoded from the upper microcontroller address and is used internally to qualify MRE and MWE when accessing registers or the buffer.
59	56	$\overline{PWR}$	NA	**$\overline{Power}$** Power is used to drive an external FET to control power down for the rest of the drive circuits.
60	57	$\overline{MWE}$ MRWB	I	**Microcontroller Write Enable,** **Microcontroller Read/$\overline{Write}$** MWE is asserted by the local microcontroller to write an internal register or the buffer. MR/$\overline{W}$ is used by Motorola-type microcontrollers to control the direction of data transfers.
61	58	$\overline{MCINT}$	O	**$\overline{Microcontroller\ Interrupt}$** This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, MCINT is asserted when the controller is selected.
62	59	RBIAS	NA	**Bias Resistor** This pin is connected to a 1 Kohm 1% resistor to control the output driver transition speed to minimize switching noise.
63	60	XIN	I	**Crystal Input** Crystal oscillator input. The crystal frequency is twice the buffer data rate.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
64	61	XOUT	O	**Crystal Out** Crystal oscillator output.
65	62	VSS	NA	**Ground** Ground.
66	63	$\overline{\text{RESET}}$	I/O	**$\overline{\text{Reset}}$** Open-drain output, can be wire-ORed with an external reset. The WD61C23A will reset all logic when this input is asserted. When the host issues a soft reset or asserts the HRST pin, then this output will be asserted as long as the DRO control bit is 0.
67	64	WCKO	O	**Write Clock Output** WCKO is an output generated from RRCK and is used to clock WDATA into the external ENDEC.
68	65	WDATA	O	**Write Data** WDATA is the NRZ data written to the disk or external ENDEC.
69	66	RRCK	I	**Read/Reference Clock** RRCK is used to shift in the RDATA during reads and to shift out the WDATA during writes. RRCK is also used to control the internal sequencer.
70	67	RDATA	I	**Read Data** RDATA is NRZ read data from the disk or external ENDEC.
71	68	RGATE	O	**Read Gate** RGATE is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.
72	69	ENCEN	O	**Encode Enable** ENCEN is asserted when valid data is to be written to the disk/ENDEC. It enables the encoding function and is negated on Write Fault (WF/WUS) or if the Abort port is written.
73	70	AME	O	**Address Mark Enable** The Address Mark Enable signal is used to control the writing of and searching for Address Marks when connected to an ESDI disk drive or external ENDEC.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
74	71	$\overline{\text{AMDETECT}}$	I	**$\overline{\text{AM Detect}}$** In soft sector mode, AMD asserted low indicates that the external ESDI drive or ENDEC has detected an Address Mark.
		$\overline{\text{SYNDET}}$	I	**$\overline{\text{Sync Detect}}$** $\overline{\text{SYNDET}}$ is asserted by an ENDEC device when it has detected a byte sync character, if sync detection is done in the ENDEC.
75	72	$\overline{\text{BWE}}$	O	**$\overline{\text{Buffer Write Enable}}$** BWE is asserted by the chip to write data into the external SRAM buffer.
76	73	$\overline{\text{BOE}}$	O	**$\overline{\text{Buffer Output Enable}}$** BOE is asserted by the chip to read data from the external SRAM buffer.
77-84	74-81	BD0 THRU BD7	I/O	**Buffer Data 0 thru Buffer Data 7** Buffer data bus, which connects directly to a static RAM. Also used to read up to eight configuration pullup resistors.
1,2 85-90, 92-94, 97-100	98,99 82-87, 89-91, 94-97	BA0 THRU BA14	O	**Buffer Address 0 thru Buffer Address 14** Buffer address bus, for direct connection up to 256 Kbytes of SRAM.
91	82	VDD	NA	**+ 5V** + 5V
95	92	VSS	NA	**Ground** Ground.
96	95	VSS	NA	**Ground** Ground.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the MQFP
** Pin numbers are for the SQFP

3.0 ARCHITECTURE

The WD61C23A is a high performance, high integration, low cost hard disk controller designed for PC/At and PC/XT applications. It is a 100-pin CMOS VLSI device which contains a disk formatter and serializer (SERDES), buffer manager, and host interface logic. The WD61C23A will support 1:1 interleave and disk data rates up to 27 Mbits/sec NRZ and 8- or 16-bit host data transfers up to 10 Mbytes/sec (5 Mwords/sec).

The WD61C23A includes four major blocks. The host interface connects directly to a PC/AT or PC/XT-type bus. The WD61C23A has 24 mA high current drivers and Schmitt trigger inputs on the host port which allow it to be connected directly to the PC/AT or PC/XT bus. The host interface includes advanced DMA logic that supports high speed burst transfers such as EISA-type B DMA. The device contains features designed to reduce the amount of real-time interaction needed by the microcontroller to manage the host protocol. The device pinout has been optimized for XT and AT IDE applications.

The local microcontroller interface is used to interface to a microcontroller such as the 8051, 80C196 (16 MHz), 68HC11, Siemens 80C166 (40 MHz), NEC K6 (40 MHz), etc. It has an 8-bit muxed address/data bus. It has a chip select input allowing it to be accessed anywhere in the microcontroller's address space. Internal logic decodes this 8-bit address and only allows access in a limited range of the 256 location register space. This allows the WD61C23A to use the same chip select as the WD61C12 servo/spindle chip and the WD10C27 ENDEC/data synchronizer/frequency synthesis chip.

The buffer manager can control multiple sector buffers up to 256 Kbytes using static RAM and allows simultaneous access from both the host and the disk. The pipelined architecture allows sophisticated scatter-gather and segmented buffer management as well as simple ring buffering. Multisector arming and automatic pointer segment wrap control ease the microcontroller overhead.

The SERDES contains a formatter which can support advanced defect management schemes, zone bit recording, hard or soft sectoring, and programmable format. The SERDES supports multitrack commands automatically. An NRZ interface is used to connect to an external ENDEC. Data integrity is insured through 16-bit CRC, 32-bit ECC, or 56-bit polynomials, and degree 6, three-way interleaved Reed-Solomon ECC. Additional options support Data Byte Sync redundancy and ID field redundancy.

3.1 HOST INTERFACE ORGANIZATION

The WD61C23A host interface is designed to connect to the IBM PC/XT or IBM PC/AT system bus as well as the system bus of any PC/XT or PC/AT clone. The WD61C23A has high current drivers and Schmitt receivers which allow for direct connection to the system bus. The host interface is inactive at power-up. The host interface is controlled by the AT/XT control bit in General Control Register 2 which is written by the local microcontroller.

3.1.2 XT Host Interface

When the AT/$\overline{XT}$ control bit is written to 0, then the WD61C23A is in PC/$\overline{XT}$-compatible interface mode. In this mode the $\overline{CS0}$ chip select should be active when I/O ports 320 hex through 323 hex are addressed for the primary controller in the XT system and for I/O ports 324 through 327 for the secondary controller. HA0 and HA1 select which register is being accessed. HA2 and $\overline{CS1}$ are not used in this mode and are optionally terminated to V_{DD} through internal registers.

Data transfers in this mode may be either PIO or DMA and can be either 8- or 16-bits wide. When 8-bit data transfer mode is selected, then the upper eight host data inputs may be optionally terminated to V_{DD} through internal registers.

3.1.2 AT Host Interface

When the AT/$\overline{XT}$ control bit is written to 1, then the WD61C23A is in PC/AT-compatible interface mode. $\overline{CS0}$ should be active when I/O ports 1F0 hex through 1F7 hex are addressed for the primary controller in the AT system. $\overline{CS1}$ should be active when 3F6 hex and 3F7 hex are addressed. Addresses 170 through 177 hex ($\overline{CS0}$) and 376, 377 hex ($\overline{CS1}$) are used for the secondary controller.

Buffer data transfers can be either PIO or DMA and can be either 8 or 16 bits. The ECC byte transfers

in a long mode read or write commands are always 8 bits. All other register transfers are 8 bits. When 16-bit PIO data transfers occur for port 0 then the IOCS16 output will be asserted. There is an option to allow the IOCS16 to be asserted during PIO transfers on DMA commands. There is also an option to allow IOCS16 to be asserted during DMA transfers, allowing an interarchitecture high speed DMA transfer mode. There is also an option to allow nonstandard host register bits to control the DMA interface.

There are additional features to alleviate the microcontroller from some of the real-time requirements of the AT host interface. First, there is a mode to automatically arm the first buffer transfer for Write, Write Long, Write Buffer, and Format commands. This buffer may be selected to be either buffer 0 of the buffer pointed to by the Host Buffer Pointer Pipeline registers. This feature allows write operations to be cached. When this mode is used, care should be taken to ensure that the buffer selection (both ADQBC bit and pipeline registers) are only modified when ABSY=1 in the Drive Status registers.

Secondly, the WD61C23A can be programmed to automatically sequence the AT task file during multisector Read, Write, Read Multiple, and Write Multiple data transfers. When this option is used, the microcontroller need only maintain the host buffer manager and the WD61C23A will automatically update the task file before releasing each sector or group of sectors to the host.

The microcontroller sets up the logical sectors per track and heads per cylinder parameters and the internal state machine will automatically handle logical track boundaries. Hardware in the part will automatically reset the Auto Task-File Update bit (ATU) upon receipt of a new command to prevent an unwanted task file increment at the start of any of the auto-DRQ commands mentioned above.

It is therefore important that the microcontroller pulse the RHBM bit in the Buffer Command Register at the start of any new command.

The AT task file is implemented as a dual port RAM allowing full time access by the microcontroller. This is true even when the internal state machine updates the task file and is independent of the state of the ABSY status bit.

There are features in the part to handle the IDE dual drive interface. First, there is internal hardware to allow only the selected drive to assert the bus interface signals. Secondly, the WD61C23A will only go busy on commands when it is the selected drive. The exception to this is on the Controller Diagnostic command. For this command the WD61C23A will go busy regardless of which drive is currently selected. Also on the Controller Diagnostic command, hardware in the WD61C23A will force the drive selection bit in the host Drive/Head Register to select drive 0.

The WD61C23A has two features that allow the part to be easily interfaced to the PCMCIA interface. First, the polarities of the HIRQ/HIRQ and HRST/HRST pins are programmable. Secondly, the part supports a single chip select, four address host decode option in addition to the traditional IDE two-chip select, three address interface.

The part also includes high current outputs and Schmitt receivers to handle the DASP and PDIAG IDE signals. This helps to eliminate external glue logic needed to implement an IDE drive. HCIO1 (PDIAG) will be set and HCIO2 (DASP) will be cleared upon any reset. In addition, HCIO1 (PDIAG) will be set upon receipt of a Controller Diagnostic command in AT mode.

3.2 MICROCONTROLLER INTERFACE

The microcontroller controls the Host Interface mode (PCAT or PCXT) and controls the buffer manager and the SERDES. The microcontroller is told to perform any required tasks by the assertion of the $\overline{\text{MCINT}}$ output. There are a number of sources for this $\overline{\text{MCINT}}$ and they are individually maskable. The polarity of the $\overline{\text{MCINT}}$ output is programmable.

In PCXT mode, $\overline{\text{MCINT}}$ is asserted when the controller is selected. In PCAT mode $\overline{\text{MCINT}}$ will be asserted when the Host writes to the command register. $\overline{\text{MCINT}}$ will be asserted whenever a buffer address is transferred from a pipeline register to the appropriate pointer.

$\overline{\text{MCINT}}$ is also asserted by the detection of a host soft or hard reset, FIFO error, or by the SERDES.

The microcontroller can have either the Intel-type (8051 or 80C196) or the Motorola-type (68HC11) interface. The WD61C23A has the built-in logic to sense the processor interface type and can therefore be directly interfaced to either type processor. Data and address are transferred via an 8-bit multiplexed bus. The WD61C23A has been designed to share a common chip select with the WD61C12 servo/spindle controller and the WD10C27 ENDEC/data synchronizer/frequency synthesizer.

3.3 BUFFER MANAGER DESCRIPTION

The buffer manager can control multiple sector buffers totalling up to 256 Kbytes using static RAM. The sector buffers can be any size up to 4095 bytes, excluding ECC, and can be located on any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM concurrently. The buffer manager handles the arbitration between the host interface and the disk formatter. Both address counters have a pipeline register that can be loaded with a new buffer address while a transfer is in progress. This allows discontiguous buffer locations to be linked without the loss of RAM bandwidth between blocks. The transfer length on the host side is controlled by a 12-bit transfer count register. The disk transfer length is controlled by the disk formatter.

The buffer manager has two pipelined block counters allowing up to 256 blocks (sectors) to be armed at one time. This eliminates the sector-by sector buffer interrupt handling required by earlier controllers. Secondly, a segment wrap control feature allows the buffer memory to be broken into several smaller buffer segments with automatic wrap from the end of each segment back to the start. The segment sizes are programmable from 4 Kbytes to 256 Kbytes.

Both ports have FIFOs allowing sustained host bandwidth of 5 Mwords/sec for 16-bit wide transfers and 10 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 12.5 Mbytes/sec when using a 25 MHz crystal.

The local microcontroller accesses the buffer RAM by using the Disk Buffer Manager logic. It first loads the desired starting address into the Disk Buffer Pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (Register 3E) the data will be read/written through the disk formatter's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction at a time as set by the DRWB control bit. When the microcontroller is accessing the buffer, the disk formatter must be idle.

There is a special mode in the buffer manager that allows the microcontroller to sense the presence of external pullups on the BD bus. These pullups can be used to reconfigure the firmware. To use this feature, the microcontroller writes the RDCF bit to 1 and then after 5 µsec reads the configuration port. If a pullup is present on a BD line then the appropriate bit in the configuration register will be read as a 1. If there is no external pullup then the bit will be read as a 0.

3.4 DISK FORMATTER DESCRIPTION

The WD61C23A has a high speed disk formatter which can handle the requirements of high performance embedded drives. The WD61C23A has an NRZ interface which allows it to be connected to an external ENDEC.

The formatter supports data rates up to 27 Mbit/sec. Software selectable 16-bit CRC, 32-bit ECC, and 56-bit ECC polynomials ensure data reliability.

The WD61C23A qualifies NRZ disk data using the Sector (SCT) and Address Mark Detect (AMD) signals, and controls the Read Gate and Write Gate timing.

The disk data formats are software programmable. The WD61C23A supports both soft and hard sectoring. The gaps and PLO fields are programmable. The ID is programmable in size from 4 to 12 bytes. The extra bytes can be used for flag information for defect management, or for size information for segmenting data fields around defects or around servo bursts. With this feature, zone bit recording with embedded servo positioning is possible with minimal processor overhead.

The disk formatter has internal control logic to automatically support zone bit recording and defect management without microcontroller intervention. Logic in the disk formatter will interpret the ID information pertaining to segmentation and automatically step around servo fields and defects. In addition, the disk formatter will interpret special flag information in the ID for detecting the last sector on a track to support sector push down defect management and multitrack commands. Finally, the disk formatter will interpret another ID flag bit to detect that a sector has been relocated to a spare area on the drive. In this case the disk formatter can be configured to automatically read out a pointer to the spare sector used to replace the defective sector.

WD61C40A

Peripheral Cache

Manager Device

WESTERN DIGITAL

TABLE OF CONTENTS

1.0 INTRODUCTION

1.1 FEATURES

- High-speed host bus transfers
  10.0 MTransfers per second in 16-bit mode (20 MBytes/s)
- Parallel disk interface - 80 Mbits NRZ in parallel mode (10 MBytes maximum, 5 MBytes nominal)
- Reed Solomon ECC data field
  - — Degree 6 with 3-way interleave with or without 4 CRC bytes
  - — Single burst on-the-fly correction
  - — Maximum of three bursts/interleave/sector correction with microprocessor intervention
  - — Maximum guaranteed single burst correction of 17 bits for on-the-fly operation
  - — Four byte ID CRC
- Data sector defect skipping support - programmable defect skip size
- Enhanced buffer management
- Memory segmentation
- Shared host/disk buffer count
- Embedded servo support
- Zoned bit recording support
- Five port buffer management (host, disk, refresh, microprocessor, and ECC correction)
- Configurable buffer support with or without parity
- Programmable memory speed
- Disk Longitudinal Redundancy Checking (LRC) on write operations over logical blocks
- Pipelined buffer address/data counters for host and disk (2 levels)
- RAM-based writable disk control store
- Pass-through parity, checked on inputs of the host/disk FIFOs
- Minimum microprocessor intervention required
- Single +5V supply with low power mode
- 132-pin PQFP package with complete functionality
- Dedicated 8-bit port for high-speed microprocessor
- 25 MHz 80186 microprocessor support

1.2 GENERAL DESCRIPTION

The WD61C40A is a high-performance CMOS VLSI device that controls data transfers between the host port and the disk port through the local data buffer. It is primarily intended as a companion device to the WD33C96 Small Computer System Interface (SCSI) Controller.

The WD61C40A joins the basic functions of the WD10C01 and WD60C40A into a single package. It also provides additional functions:

- Reed Solomon on-the-fly ECC
- Parallel disk data bus
- Sector defect skipping
- Buffer memory segmentation
- Host-disk buffer count
- Enhanced control store functionality
- Wider host and buffer buses for improved bus bandwidth
- Minimal microprocessor intervention
- Skip mask support

There are two areas of major performance improvements. The first area is data transfer rate. The WD61C40A can maintain 20 Mbyte host port transfers and 5 Mbyte disk port transfers at a system clock of 47 MHz. This type of performance is achieved through the usage of a 16-bit host bus, a 16-bit buffer bus and an 8-bit disk bus. The disk port can also achieve a maximum transfer rate of 10 Mbytes.

The second area of improvement is key system functions. For example, the disk controller has on-chip Reed Solomon ECC: generation, detection and correction logic. Defect skipping (the ability to write and read data around flaws on the disk) maximizes disk capacity while minimizing sector reallocation. The buffer manager also reduces microprocessor support. The buffer segmentation and skip mask modes reduce interrupts to the microprocessor. Block mode operation also reduces interrupts.

The WD61C40A is flexible in a variety of ways. Three ports (host, disk, and buffer) support multi-

ple pin configurations. The port data widths are 16 bits for host and 8 bits for the disk. Each port supports parity or no parity checking. The Disk Controller is based upon a writable control store. The user can define the disk format of choice rather than using a fixed track format. The defect skipping option permits the dynamic variation of sector format during a read or write operation. This option operates equally well with embedded or dedicated servos.

The WD61C40A also includes several features to improve testability of the device:

- All RAM and register files contain internal Built-in Self-test (BIST) logic.
- Most registers are readable.
- Provides test modes for the large transfer counter, address pointers and major internal logic blocks.
- The I/O pins include the I/O Mapping Test feature for printed circuit board testing.
- The disk port contains logic which guarantees data integrity (LRC checking) across the WD33C96/WD61C40A boundary.
- The Writable Control Store RAM is read-writable by the microprocessor.

2.0 ARCHITECTURE

The WD61C40A is divided into four major sections. these sections are the disk control logic, the buffer management control, microprocessor interface and the host port logic.

The Disk Port contains a 64 x 32 writable control store, the ID field control logic with defect skipping control, a 32 byte data FIFO, and the ECC checking/generation/correction logic.

The host port contains the host control logic and a 32 byte FIFO.

The microprocessor interface contains logic which supports a microprocessor with a multiplexed data/address bus and wait state capabilities. This includes Intel's family of 80196 and 80186 devices.

The buffer interface contains the buffer arbitration control and the DMA address pointers (refresh, host port, disk port, ECC correction, microprocessor access).

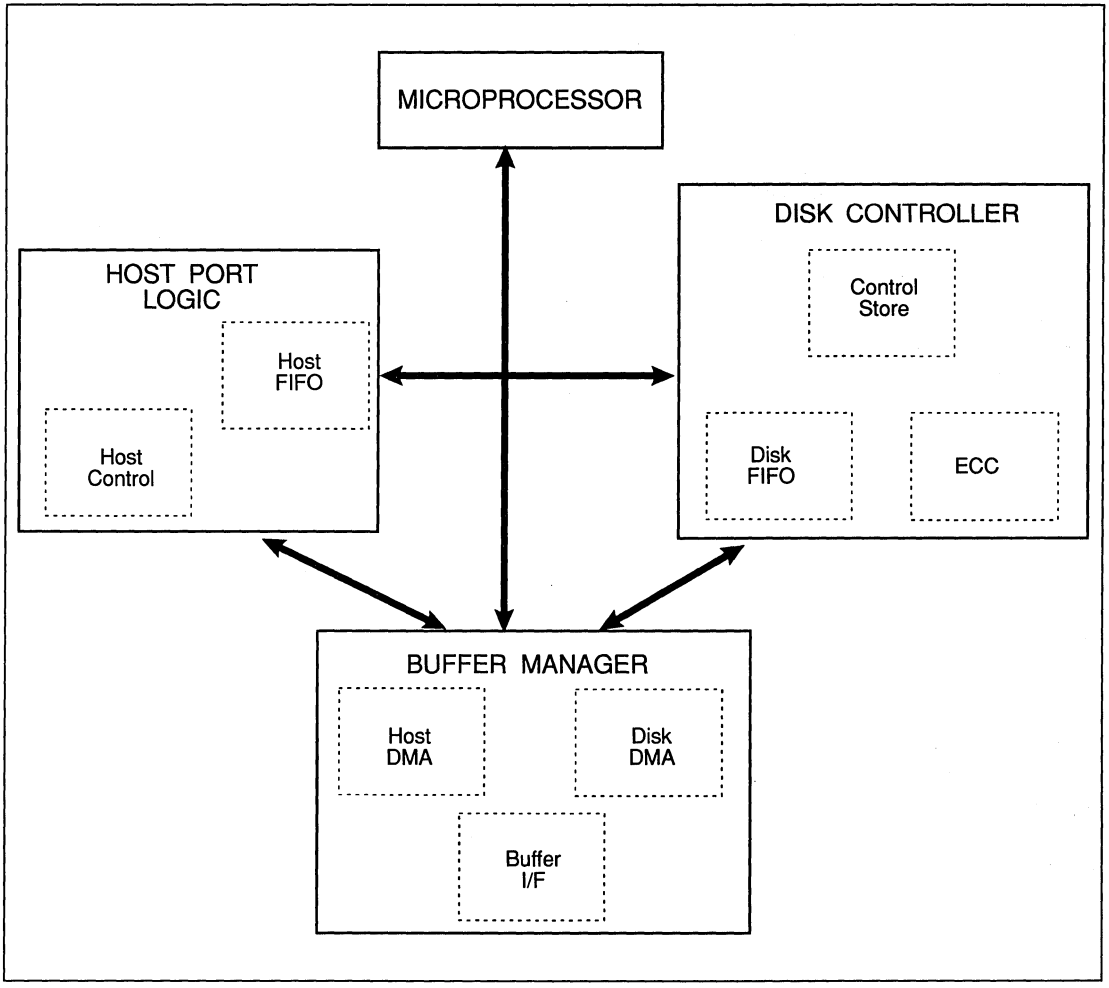

FIGURE 2-1. BLOCK DIAGRAM OF THE WD61C40A

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3.0 INTERFACES

3.1 MICROPROCESSOR INTERFACE

The WD61C40A supports 8-bit microprocessors with multiplexed address/data busses. All the internal registers are accessible through this bus. The microprocessor accesses these registers using the following control signals: WEB, REB, ALE, CSB and RDYB. The device must be externally mapped into a 256-byte space. A chip select, CSB, must be presented to this device for any read or write access. The WD61C40A sends a ready signal, RDYB, to the microprocessor whenever an extended read or write strobe is required. This is done when the microprocessor wishes to access the buffer memory.

3.2 HOST PORT INTERFACE

The host port is a generic DMA data port. Data transfer speeds and data widths are programmable. The data can be transferred in a 16-bit mode. The maximum transfer speed is 10 MTransfers per second. The host port DMA logic is programmable. Both master and slave DMA operations are supported. The polarity of the DREQ and DACK signals are programmable to be active high or low.

3.3 DISK PORT INTERFACE

The disk port is constructed around a WD10C01-like architecture. The disk port is controlled by a 64 x 32-bit writable control store. the disk port now supports a parallel data path. This path can support a 10 MByte transfer rate. All of the WD10C01 control signals and most of the general port bits are supported.

3.4 BUFFER PORT INTERFACE

The buffer port is designed to support 16-bit DRAM configurations up to 4 MWords. The memory size, parity option and bus timing are all programmable features.

4.0 SIGNAL DESCRIPTION

4.1 SIGNAL TO PIN LOCATION

Figure 4-1 is a pin diagram of the 132-pin WD61C40A. Table 4-1 lists the pin assignments.

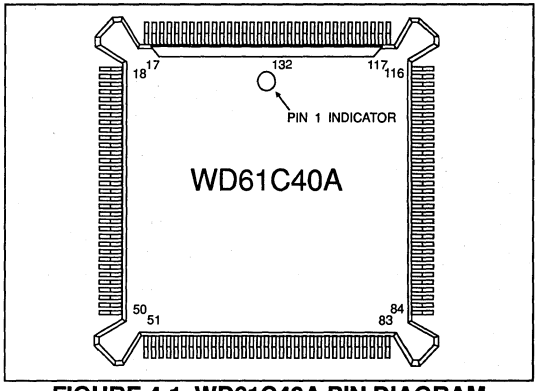

FIGURE 4-1. WD61C40A PIN DIAGRAM

4.2 DETAILED SIGNAL DESCRIPTION

Table 4-2 provides signal descriptions.

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VCC	34	BF11	67	RESET	100	GPX0
2	N/C	35	BF12	68	VCC	101	VCC
3	GND	36	GND	69	GPY4	102	DATA7
4	A10	37	BF13	70	TSTB	103	GND
5	A9	38	BF14	71	N/C	104	DATA6
6	A8	39	BF15	72	BDPH	105	GPX2
7	A7	40	BFPH	73	BD15	106	DATA5
8	A6	41	GND	74	BD14	107	GPX3
9	GND	42	N/C	75	BD13	108	DATA4
10	A5	43	INT2	76	BD12	109	GND
11	A4	44	INT	77	GND	110	DATA3
12	A3	45	RDY	78	BD11	111	GPX5
13	A2	46	ALE	79	BD10	112	DATA2
14	A1	47	WEB	80	BD9	113	DATA1
15	A0	48	CSB	81	BD8	114	DATA0
16	CASB	49	REB	82	BDPL	115	DATAP
17	GND	50	VCC	83	GND	116	GND
18	MEMWB	51	GND	84	BD7	117	RRCLK
19	RASB	52	AD7	85	BD6	118	WRTCLK
20	BF0	53	AD6	86	BD5	119	GND
21	BF1	54	AD5	87	BD4	120	AMENA
22	BF2	55	AD4	88	GND	121	RDGATE
23	GND	56	GND	89	BD3	122	WRTGATE
24	BF3	57	AD3	90	BD2	123	SEQOUT
25	BF4	58	AD2	91	BD1	124	GPX6
26	BF5	59	AD1	92	BD0	125	GPX7
27	BF6	60	AD0	93	GND	126	AMDET
28	BF7	61	GND	94	DRQ	127	SMDET
29	GND	62	GPY0	95	DACK	128	IDXDET
30	BFPL	63	GPY1	96	PREB	129	COMPLT
31	BF8	64	GPY2	97	PWEB	130	DRVFLT
32	BF9	65	N/C	98	GPX4	131	WRAP
33	BF10	66	OSC	99	GPX1	132	N/C

TABLE 4-1. WD61C40A PIN ASSIGNMENTS

PIN	MNEMONIC	I/O	DESCRIPTION
MICROPROCESSOR INTERFACE			
43	INT2	O	**Secondary Interrupt Request** This active-high output signal is asserted when any of the disk DMA interrupts are active.
44	INT	O	**Interrupt Request** This active-high output signal is asserted to alert the microprocessor to the completion or termination of a command.
45	RDYB	O	**Ready** This open-drain output controls the microprocessor's wait logic. (Active low)
46	ALE	I	**Address Latch Enable** This signal is used to load the address of the desired register.
47	WEB	I	**Write Enable** This signal is active low and used with the CSB signal to write to the registers.
48	CSB	I	**Chip Select** This active-low signal qualifies REB and WEB signals when the microprocessor is accessing a register.
49	REB	I	**Read Enable** This active-low signal is used with the CSB signal to read the registers.
52-55 57, 60	AD7-AD0	I/O	**Microprocessor Data/Address Bus**

TABLE 4-2. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
72	BDPH	I/O	**Parity of the Upper DMA Bus** Odd parity for BD15 through BD8.
82	BDPL	I/O	**Parity of the Lower DMA Bus** Odd parity ofr BD7 through BD0.
81-78 76-73	BD[8:15]	I/O	**Host DMA Bus** Upper 8 bits of host DMA bus.
92-89 87-84	BD[0:7]	I/O	**Host DMA Bus** Lower 8 bits of host DMA bus.
94	DREQ	I/O	**DMA Request** Programmable DMA request.
95	DACK	I/O	**DMA Acknowledge** Programmable DMA Acknowledge.
96	DREB	I/O	**DMA Read Enable** (active low)
97	DWEB	I/O	**DMA Write Enable** (active low)

TABLE 4-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
			DISK INTERFACE
62-64, 69	GPY[0:3]	I/O	**General Purpose Port** These pins can be configured as a generic input or output pins.
100,99, 105,107, 98, 111, 124, 125	GPX[0:7]	I/O	**General Purpose Port** These pins can be configured as a generic input or output pins.
114, 113 112, 110 108, 106 104, 102	DATA[0:7]	I/O	**Disk Drive Parallel Data Bus**
115	DATAP	I/O	**Disk Drive Parallel Data Bus Parity**
117	RRCLK	I	**Read Reference Clock** This clock is generated by the Disk Read Channel. All WD61C40A disk control and data signals are synchronized to this clock.
118	WRTCLK	O	**Write Clock** This signal is the inversion of RRCLK.
120	AMENA	O	**Address Mark Enable** In write mode, this signal indicates to the write channel that an address mark byte is being sent on the DATA[0:7] lines. In read mode, this signal flags the read channel as to the type of sync bytes to be detected. When RDGATE and WRTGATE are inactive, this signal indicates a search for an ID Address mark. (This signal is not tristated under reset conditions.)
121	RDGATE	O	**Read Gate** This signal is controlled by the Control Store (This signal is not tristated under reset conditions.)
122	WRTGATE	I	**Write Gate** This signal is controlled by the Control Store. (This signal is not tristated under reset conditions.)
123	SEQOUT	O	**Sequence Out** This is a general purpose control signal that is directed by Control Store.
126	AMDET	I	**Address Mark Detect** The Read Channel generates this signal when an ID address mark (or optional sync byte) is detected.
127	SMDET	I	**Sector Mark Detect** This signal is generated by the read/write logic when a sector mark is found.

TABLE 4-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
			DISK INTERFACE (Continued)
128	IDXDET	O	**Index Detect** This signal is generated by the read/write logic when an index mark is detected.
129	CMPLT	I	**Seek Complete** This is a general purpose flag from the drive electronics. When this signal is active an interrupt can be generated by the WD61C40A.
130	DRVFLT	I	**Drive Fault** This is a general purpose flag from the drive electronics. This is typically an indication of a drive failure. When this signal is active, an interrupt is generated by the WD61C40A. As an option, the Control Store can respond to this error condition and jump to the error routine.
131	WRAP	I	**WRAP Check** This pin is used to verify that the REGATE, WRTGATE, and AMENA signals are properly connected to the drive electronics. An interrupt is also generated when an error is detected.
			BUFFER PORT INTERFACE
15-10 8-4	A[0:10]	O	**Buffer Address Pins**
16	CASB	O	**Primary Column Address Strobe**
18	MEMWB	O	**Memory Write**
19	RASB	O	**Row Address Strobe**
20-22, 24-28	BF[0:7]	I/O	**Buffer Data Bus (LSB)**
30	BFPL	I/O	**Buffer Data Parity Bit (LSB)**, odd parity.
31-35 37-39	BF[8:15]	I/O	**Buffer Data Bus (MSB)**
40	BFPH	I/O	**Buffer Data Parity (MSB)**, odd parity.

TABLE 4-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS
66	OSC	I	**Clock** - maximum 47 MHz.
67	RESETB	I	**Hard Reset** This active-low input sets the WD61C40A in power-on-reset condition. All the drivers are set into inactive state.
70	TSTB	I	**I/O Test Enable** When active low the WD61C40A is in I/O Map Test.
1, 101, 68, 50	VCC	I	**+5V Power Supply**
119, 116, 109, 93, 88,83, 77, 61, 56, 51, 41, 36, 29, 23, 17, 9, 3	GND	I	**Ground**

TABLE 4-2. SIGNAL DESCRIPTION (Continued)

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WD16C452/552	C0312
WD16C550	C0308
WD76C10A/LP/LV	I0527
WD76C20/LV	I0522
WD76C30/LV	I0246
WD7710/LP	I0613
WD7910/LP	I0615

Systems Logic Application Notes:

WD7600	A0108

Imaging Data Sheets:

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WD90C00	P0540
WD90C11, WD90C11A	P0548
WD90C20, WD90C20A	P0545
WD90C22	P0546
WD90C26	P0637
WD90C31	P0405
WD90C55	P0639

Imaging Application Notes:

WD90CXX	A0109

Storage Data Sheets:

Title	Order Number
WD10C01A	S0521
WD10C27	S0225
WD33C92A	S0231
WD33C93B	S0229
WD33C95A, WD33C96A	S0232
WD37C65C	S0702
WD42C22C	S0344
WD60C31B	S0430
WD60C40A	S0624
WD60C80	S0434
WD61C23	S0431
WD61C40A	S0435

Storage Application Notes:

WD10C2XX	A0103
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